

# ARM<sup>®</sup> Compiler

Version 6.00

## Software Development Guide

**ARM<sup>®</sup>**

# ARM® Compiler

## Software Development Guide

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### Release Information

### Document History

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# Preface

This preface introduces the *ARM® Compiler Software Development Guide*.

This section contains the following subsections:

- [About this book on page 8.](#)

## About this book

The ARM Compiler Software Development Guide provides tutorials and examples to develop code for various ARM architecture-based processors.

## Using this book

This book is organized into the following chapters:

### **Chapter 1 Introducing the Toolchain**

Provides an overview of the ARM compilation tools, and shows how to compile a simple code example.

### **Chapter 2 Diagnostics**

Describes the format of compiler toolchain diagnostic messages and how to control the diagnostic output.

### **Chapter 3 Compiling C and C++ Code**

Describes how to compile C and C++ code with `armclang`.

### **Chapter 4 Assembling Assembly Code**

Describes how to assemble assembly source code with `armclang` and `armasm`.

### **Chapter 5 Linking Object Files to Produce an Executable**

Describes how to link object files to produce an executable image with `armlink`.

### **Chapter 6 Optimization**

Describes how to use `armclang` to optimize for either code size or performance, and the impact of the optimization level on the debug illusion.

### **Chapter 7 Coding Considerations**

Describes how you can use programming practices and techniques to increase the portability, efficiency and robustness of your C and C++ source code.

### **Chapter 8 Language Compatibility and Extensions**

Describes the language extensions that the compiler supports.

## Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

## Typographic conventions

*italic*

Introduces special terminology, denotes cross-references, and citations.

**bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

monospace

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.



**monospace**

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

***monospace italic***

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

**monospace bold**

Denotes language keywords when used outside example code.

**<and>**

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>
```

**SMALL CAPITALS**

Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

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# Chapter 1

## Introducing the Toolchain

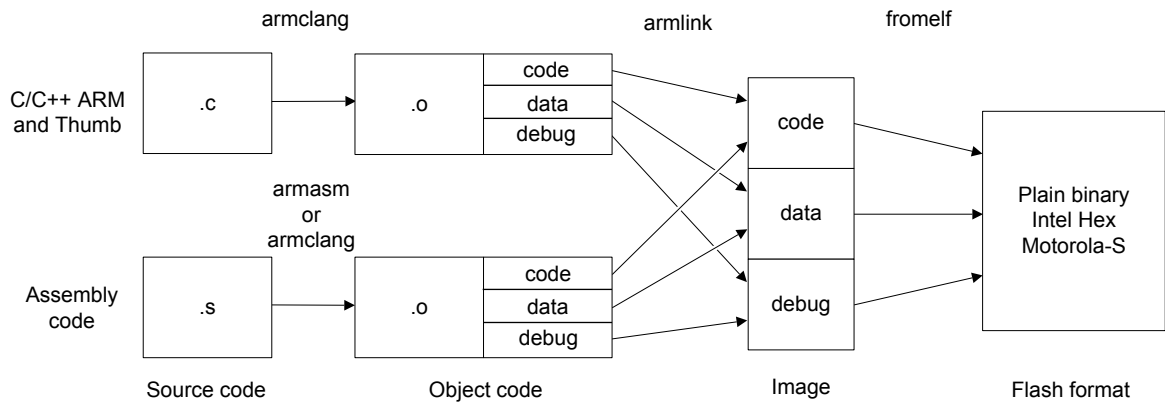
Provides an overview of the ARM compilation tools, and shows how to compile a simple code example.

It contains the following sections:

- *1.1 Toolchain overview on page 1-11.*
- *1.2 Common compiler toolchain options on page 1-12.*
- *1.3 "Hello world" example on page 1-15.*
- *1.4 Passing options from the compiler to the linker on page 1-16.*

## 1.1 Toolchain overview

The ARM Compiler 6 compilation tools allow you to build executable images, partially linked object files, and shared object files, and to convert images to different formats.



**Figure 1-1 Compiler toolchain**

The ARM compiler toolchain comprises the following tools:

### **armclang**

The `armclang` compiler and assembler. This compiles C and C++ code, and assembles A32, A64, and T32 GNU syntax assembly code.

### **armasm**

The legacy assembler. This assembles A32, A64, and T32 ARM syntax assembly code.

Only use `armasm` for legacy ARM syntax assembly code. Use the `armclang` assembler and GNU syntax for all new assembly files.

### **armlink**

The linker. This combines the contents of one or more object files with selected parts of one or more object libraries to produce an executable program.

### **armar**

The librarian. This enables sets of ELF object files to be collected together and maintained in archives or libraries. You can pass such a library or archive to the linker in place of several ELF files. You can also use the archive for distribution to a third party for further application development.

### **fromelf**

The image conversion utility. This can also generate textual information about the input image, such as disassembly and its code and data size.

## **Related tasks**

[1.3 "Hello world" example on page 1-15.](#)

## **Related references**

[1.2 Common compiler toolchain options on page 1-12.](#)

## 1.2 Common compiler toolchain options

Lists the most commonly used command-line options for each of the tools in the compiler toolchain.

### armclang common options

See the *armclang Reference Guide* for more information about armclang command-line options.

Common armclang options include the following:

**Table 1-1 armclang common options**

Option	Description
-c	Performs the compilation step, but not the link step.
-x	Specifies the language of source files, -xc or -xc++ for example.
-std	Specifies the language standard to compile for, -std=c90 for example.
--target=arch-vendor-os-env	Enables code generation for the selected ARM architecture, for example --target=aarch64-arm-none-eabi or --target=armv8a-arm-none-eabi.
-marm	Requests that the compiler targets the A32 instruction set, --target=armv8a-arm-none-eabi -marm for example.  The -marm option is only valid with AArch32 targets, for example --target=armv8a-arm-none-eabi. The compiler ignores the -marm option and generates a warning with AArch64 targets.
-mthumb	Requests that the compiler targets the T32 instruction set, --target=armv8a-arm-none-eabi -mthumb for example.  The -mthumb option is only valid with AArch32 targets, for example --target=armv8a-arm-none-eabi. The compiler ignores the -mthumb option and generates a warning with AArch64 targets.
-g	Generates DWARF debug tables.
-E	Executes only the preprocessor step.
-I	Adds the specified directories to the list of places that are searched to find included files.
-o	Specifies the name of the output file.
-Onum	Specifies the level of performance optimization to use when compiling source files.
-Os	Balances code size against code speed.
-Oz	Optimizes for code size.
-S	Outputs the disassembly of the machine code generated by the compiler.
-###	Displays diagnostic output showing the options that would be used to invoke the compiler and linker. Neither the compilation nor the link steps are performed.

### armlink common options

See the *armlink User Guide* for more information about armlink command-line options.

Common armlink options include the following:

**Table 1-2 armlink common options**

Option	Description
<code>--force_scanlib</code>	<p>The compiler does not generate <code>\$\$Lib\$Request</code> symbols when building objects, so <code>armlink</code> does not automatically link with the ARM libraries, resulting in the following messages:</p> <pre>Warning: L6665W: Neither Lib\$\$Request\$\$armlib Lib\$\$Request\$\$cpplib defined, not searching ARM libraries. Error: L6411E: No compatible library exists with a definition of startup symbol __main.</pre> <p>Invoke <code>armlink</code> with <code>--force_scanlib</code> to link with the ARM libraries. When compiling and linking in one step, the compiler automatically passes this option to <code>armlink</code>.</p>
<code>--cpu=name</code>	Sets the target processor.
<code>--fpu=name</code>	Selects the target floating-point unit (FPU) architecture
<code>--ro_base</code>	Sets the load and execution addresses of the region containing the RO output section to a specified address.
<code>--rw_base</code>	Sets the execution address of the region containing the RW output section to a specified address.
<code>--scatter</code>	Creates an image memory map using the scatter-loading description contained in the specified file.
<code>--split</code>	Splits the default load region containing the RO and RW output sections, into separate regions.
<code>--entry</code>	Specifies the unique initial entry point of the image.
<code>--info</code>	Displays information about linker operation, for example <code>--info=exceptions</code> displays information about exception table generation and optimization.
<code>--list=filename</code>	Redirects diagnostics output from options including <code>--info</code> and <code>--map</code> to the specified file.
<code>--map</code>	Displays a memory map containing the address and the size of each load region, execution region, and input section in the image, including linker-generated input sections.
<code>--symbols</code>	Lists each local and global symbol used in the link step, and their values.

### armar common options

See the *armar User Guide* for more information about `armar` command-line options.

Common `armar` options include the following:

**Table 1-3 armar common options**

Option	Description
<code>--debug_symbols</code>	Includes debug symbols in the library.
<code>-a pos_name</code>	Places new files in the library after the file <code>pos_name</code> .
<code>-b pos_name</code>	Places new files in the library before the file <code>pos_name</code>
<code>-d file_list</code>	Deletes the specified files from the library.
<code>--sizes</code>	Lists the Code, RO Data, RW Data, ZI Data, and Debug sizes of each member in the library.
<code>-t</code>	Prints a table of contents for the library.

### fromelf common options

See the *fromelf User Guide* for more information about `fromelf` command-line options.

Common `fromelf` options include the following:

**Table 1-4 fromElf common options**

Option	Description
--elf	Selects ELF output mode.
--text [ <i>options</i> ]	Displays image information in text format.  The optional <i>options</i> specify additional information to include in the image information. Valid <i>options</i> include -c to disassemble code, and -s to print the symbol and versioning tables.
--info	Displays information about specific topics, for example --info=totals lists the Code, RO Data, RW Data, ZI Data, and Debug sizes for each input object and library member in the image.

### armasm common options

See the *armasm User Guide* for more information about *armasm* command-line options.

———— **Note** —————

Only use *armasm* to assemble legacy ARM syntax assembly code. Use GNU syntax for new assembly files, and assemble with the *armclang* assembler.

Common *armasm* options include the following:

**Table 1-5 armasm common options**

Option	Description
--cpu= <i>name</i>	Sets the target processor.
-g	Generates DWARF debug tables.
--fpu= <i>name</i>	Selects the target floating-point unit (FPU) architecture
-o	Specifies the name of the output file.

## 1.3 "Hello world" example

This example shows how to build a simple C program `hello_world.c` with `armclang` and `armlink`.

### Procedure

1. Create a C file `hello_world.c` with the following content:

```
#include <stdio.h>

main()
{
    printf("Hello World");
}
```

2. Compile the C file `hello_world.c` with the following command:

```
armclang -c hello_world.c
```

The `-c` option tells the compiler to perform the compilation step only.

The compiler creates an object file `hello_world.o`

3. Link the file:

```
armlink -o hello_world.axf --force_scanlib hello_world.o
```

The `-o` option tells the linker to name the output image `hello_world.axf`, rather than using the default image name `__image.axf`.

The `--force_scanlib` option tells `armlink` to link with the ARM libraries. This option is mandatory when running `armlink` directly. When `armclang` calls `armlink`, this option is automatically enabled.

4. Use a DWARF 4 compatible debugger to load and run the image.

The compiler produces debug information that is compatible with the DWARF 4 standard.

## 1.4 Passing options from the compiler to the linker

By default, when you run `armclang` the compiler automatically invokes the linker, `armlink`.

A number of `armclang` options control the behavior of the linker. These options are translated to equivalent `armlink` options.

**Table 1-6** `armclang` linker control options

<code>armclang</code> Option	<code>armlink</code> Option	Description
<code>-e</code>	<code>--entry</code>	Specifies the unique initial entry point of the image.
<code>-L</code>	<code>--userlibpath</code>	Specifies a list of paths that the linker searches for user libraries.
<code>-l</code>	<code>--library</code>	Add the specified library to the list of searched libraries.
<code>-rdynamic</code>	<code>--export-dynamic</code>	If an executable has dynamic symbols, export all externally visible symbols rather than only referenced symbols.
<code>-u</code>	<code>--undefined</code>	Prevents the removal of a specified symbol if it is undefined.

In addition, the `-Xlinker` and `-wl` options let you pass options directly to the linker from the compiler command line. These options perform the same function, but use different syntaxes:

- The `-Xlinker` option specifies a single option, a single argument, or a single option=argument pair. If you want to pass multiple options, use multiple `-Xlinker` options.
- The `-wl`, option specifies a comma-separated list of options and arguments or option=argument pairs.

For example, the following are all equivalent because `armlink` treats the single option `--list=diag.txt` and the two options `--list diag.txt` equivalently:

```
-Xlinker --list -Xlinker diag.txt -Xlinker --split
```

```
-Xlinker --list=diag.txt -Xlinker --split
```

```
-wl,--list,diag.txt,--split
```

```
-wl,--list=diag.txt,--split
```

———— **Note** —————

The `-###` compiler option produces diagnostic output showing exactly how the compiler and linker are invoked, displaying the options for each tool. With the `-###` option, `armclang` only displays this diagnostic output. It does not compile source files or invoke `armlink`.

The following example shows how to use the `-Xlinker` option to pass the `--split` option to the linker, splitting the default load region containing the RO and RW output sections into separate regions:

```
armclang hello_world.c -Xlinker --split
```

You can use `fromelf --text` to compare the differences in image content:

```
armclang hello_world.c -o hello_world_DEFAULT.axf
armclang hello_world.c -o hello_world_SPLIT.axf -Xlinker --split
fromelf --text hello_world_DEFAULT.axf > hello_world_DEFAULT.txt
fromelf --text hello_world_SPLIT.axf > hello_world_SPLIT.txt
```

Use a file comparison tool, such as the UNIX `diff` tool, to compare the files `hello_world_DEFAULT.txt` and `hello_world_SPLIT.txt`.



## Chapter 2

# Diagnostics

Describes the format of compiler toolchain diagnostic messages and how to control the diagnostic output.

It contains the following sections:

- [2.1 Understanding diagnostics](#) on page 2-18.
- [2.2 Options for controlling diagnostics with armclang](#) on page 2-20.
- [2.3 Options for controlling diagnostics with the other tools](#) on page 2-21.

## 2.1 Understanding diagnostics

All the tools in the ARM Compiler 6 toolchain produce detailed diagnostic messages, and let you control how much or how little information is output.

The format of diagnostic messages and the mechanisms for controlling diagnostic output are different for `armclang` than for the other tools in the toolchain.

### Message format for `armclang`

`armclang` produces messages in the following format:

```
file:line:col: type: message
```

where:

*file*

The filename that generated the message.

*line*

The line number that generated the message.

*col*

The column number that generated the message.

*type*

The type of the message, for example error or warning.

*message*

The message text.

For example:

```
hello.c:7:3: error: use of undeclared identifier 'i'
i++;
^
1 error generated.
```

### Message format for other tools

The other tools in the toolchain (such as `armasm` and `armlink`) produce messages in the following format:

```
type: prefix id suffix: message_text
```

Where:

*type*

is one of:

**Internal fault**

Internal faults indicate an internal problem with the tool. Contact your supplier with feedback.

**Error**

Errors indicate problems that cause the tool to stop.

**Warning**

Warnings indicate unusual conditions that might indicate a problem, but the tool continues.

**Remark**

Remarks indicate common, but sometimes unconventional, tool usage. These diagnostics are not displayed by default. The tool continues.

*prefix*

indicates the tool that generated the message, one of:

- A - `armasm`
- L - `armlink` or `armar`
- Q - `fromelf`

*id* a unique numeric message identifier.  
*suffix* indicates the type of message, one of:

- E - Error
- W - Warning
- R - Remark

*message\_text* the text of the message.

For example:

```
Error: L6449E: While processing /home/scratch/a.out: I/O error writing file '/home/scratch/a.out': Permission denied
```

### Related concepts

[2.2 Options for controlling diagnostics with armclang on page 2-20.](#)

[2.3 Options for controlling diagnostics with the other tools on page 2-21.](#)

## 2.2 Options for controlling diagnostics with armclang

A number of options control the output of diagnostics with the armclang compiler.

See *Controlling Errors and Warnings* in the *Clang Compiler User's Manual* for full details about controlling diagnostics with armclang.

The following are some of the common options that control diagnostics:

- Werror  
Turn warnings into errors.
- Werror=foo  
Turn warning foo into an error.
- Wno-error=foo  
Leave warning foo as a warning even if -Werror is specified.
- Wfoo  
Enable warning foo.
- Wno-foo  
Suppress warning foo.
- w  
Suppress all warnings.
- Weverything  
Enable all warnings.

Where a message can be suppressed, the compiler provides the appropriate suppression flag in the diagnostic output.

For example, by default armclang checks the format of printf() statements to ensure that the number of % format specifiers matches the number of data arguments. The following code generates a warning:

```
printf("Result of %d plus %d is %d\n", a, b);  
  
armclang -c hello.c  
hello.c:25:36: warning: more '%' conversions than data arguments [-Wformat]  
  printf("Result of %d plus %d is %d\n", a, b);
```

To suppress this warning, use -Wno-format:

```
armclang -c hello.c -Wno-format
```

### Related references

[7 Coding Considerations on page 7-37.](#)

### Related information

[The LLVM Compiler Infrastructure Project.](#)  
[Clang Compiler User's Manual.](#)

## 2.3 Options for controlling diagnostics with the other tools

A number of different options control diagnostics with the `armasm`, `armlink`, `armar`, and `fromelf` tools.

The following options control diagnostics:

- `--brief_diagnostics`  
armasm only. Uses a shorter form of the diagnostic output. In this form, the original source line is not displayed and the error message text is not wrapped when it is too long to fit on a single line.
- `--diag_error=tag[, tag]...`  
Sets the specified diagnostic messages to Error severity.
- `--diag_remark=tag[, tag]...`  
Sets the specified diagnostic messages to Remark severity.
- `--diag_style=arm|ide|gnu`  
Specifies the display style for diagnostic messages.
- `--diag_suppress=tag[, tag]...`  
Suppresses the specified diagnostic messages.
- `--diag_warning=tag[, tag]...`  
Sets the specified diagnostic messages to Warning severity.
- `--errors=filename`  
Redirects the output of diagnostic messages to the specified file.
- `--remarks`  
armlink only. Enables the display of remark messages (including any messages redesignated to remark severity using `--diag_remark`).

For example, to downgrade a warning message with the number 1293 to Remark severity, use the following command:

```
armasm --diag_remark=1293 ...
```

# Chapter 3

## Compiling C and C++ Code

Describes how to compile C and C++ code with `armclang`.

It contains the following sections:

- *3.1 Specifying a target architecture, processor, and instruction set on page 3-23.*
- *3.2 Using PCH files to reduce compile time on page 3-25.*
- *3.3 Using inline assembly code on page 3-26.*
- *3.4 Using intrinsics on page 3-27.*
- *3.5 Preventing the use of floating-point instructions and registers on page 3-28.*

## 3.1 Specifying a target architecture, processor, and instruction set

When compiling code, the compiler must know which architecture or processor to target, and which instruction set to use.

### Command-line syntax

To specify a target architecture with `armclang`, use the `--target` command-line option:

```
--target=arch-vendor-os-env
```

Supported targets are as follows:

`aarch64-arm-none-eabi`

The AArch64 state of the ARMv8 architecture. This target supports the A64 instruction set. This is the default target.

`armv8a-arm-none-eabi`

The AArch32 state of the ARMv8 architecture. This target supports the A32 and T32 instruction sets.

---

———— **Note** —————

The `--target` option is an `armclang` option. For all of the other tools, such as `armasm` and `armlink`, use the `--cpu`, `--fpu`, and `--device` options to specify target processors and architectures.

---

Targeting an architecture with `--target` generates generic code that runs on any processor with that architecture. If you want to optimize your code for a particular processor, use the `-mcpu` option. The `-mcpu` option supports the following values:

- `cortex-a53`
- `cortex-a57`

Processors in AArch64 state execute A64 instructions. Processors in AArch32 state can execute A32 or T32 instructions. To specify the target instruction set for AArch32 state, use the following command-line options:

- `-marm` targets the A32 instruction set. This is the default for the `armv8a-arm-none-eabi` target.
- `-mthumb` targets the T32 instruction set.

---

———— **Note** —————

The `-marm` and `-mthumb` options are only valid with AArch32 targets, for example `--target=armv8a-arm-none-eabi`. The compiler ignores the `-marm` and `-mthumb` options and generates a warning with AArch64 targets.

### Command-line examples

ARM Compiler 6 lets you compile for the following combinations of architecture and instruction set:

**Table 3-1 Compiling for different combinations of architecture and instruction set**

Architecture	Processor	Instruction set	armclang command
ARMv8 AArch32 state	Generic	A32	armclang --target=armv8a-arm-none-eabi -marm test.c or, because -marm is the default for AArch32 targets: armclang --target=armv8a-arm-none-eabi test.c
ARMv8 AArch32 state	Cortex-A57	A32	armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a57 -marm test.c or, because -marm is the default for AArch32 targets: armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a57 test.c
ARMv8 AArch32 state	Cortex-A53	A32	armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a53 -marm test.c or, because -marm is the default for AArch32 targets: armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a53 test.c
ARMv8 AArch32 state	Generic	T32	armclang --target=armv8a-arm-none-eabi -mthumb test.c
ARMv8 AArch32 state	Cortex-A57	T32	armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a57 -mthumb test.c
ARMv8 AArch32 state	Cortex-A53	T32	armclang --target=armv8a-arm-none-eabi -mcpu=cortex-a53 -mthumb test.c
ARMv8 AArch64 state	Generic	A64	armclang --target=aarch64-arm-none-eabi test.c or, because --target=aarch64-arm-none-eabi is the default: armclang test.c
ARMv8 AArch64 state	Cortex-A57	A64	armclang --target=aarch64-arm-none-eabi -mcpu=cortex-a57 test.c or, because --target=aarch64-arm-none-eabi is the default: armclang -mcpu=cortex-a57 test.c
ARMv8 AArch64 state	Cortex-A53	A64	armclang --target=aarch64-arm-none-eabi -mcpu=cortex-a53 test.c or, because --target=aarch64-arm-none-eabi is the default: armclang -mcpu=cortex-a53 test.c



## 3.2 Using PCH files to reduce compile time

Precompiled Header files can help reduce compilation time when the same header file is used by multiple source files.

When compiling source files, the included header files are also compiled. If a header file is included in more than one source file, it is recompiled when each source file is compiled. Also, header files can introduce many lines of code, but the primary source files that include them can be relatively small. Therefore, it is often desirable to avoid recompiling a set of header files by precompiling them. These are referred to as PCH files.

To generate a PCH file using `armclang`, use the `-x Language-header` option, for example:

```
armclang -x c-header test.h -o test.h.pch
```

To use an existing PCH file, use the `-include` option, for example:

```
armclang -include test.h test.c -o test
```

———— **Note** ————

`armclang` does not automatically use PCH files for headers that are included within a source file using `#include`. Use the `-include` option if you want to make use of existing PCH files.

See *Precompiled Headers* in the *Clang Compiler User's Manual* for full details about controlling diagnostics with `armclang`.

### Related information

[Clang Compiler User's Manual.](#)

### 3.3 Using inline assembly code

The compiler provides an inline assembler that enables you to write optimized assembly language routines, and to access features of the target processor not available from C or C++.

The `__asm` keyword can incorporate inline GCC syntax assembly code into a function. For example:

```
#include <stdio.h>

int add(int i, int j)
{
    int res = 0;
    __asm (
        "ADD %[result], %[input_i], %[input_j]"
        : [result] "=r" (res)
        : [input_i] "r" (i), [input_j] "r" (j)
    );
    return res;
}

int main(void)
{
    int a = 1;
    int b = 2;
    int c = 0;

    c = add(a,b);

    printf("Result of %d + %d = %d\n", a, b, c);
}
```

———— **Note** —————

The inline assembler does not support legacy assembly code written in ARM assembler syntax.

The general form of an `__asm` inline assembly statement is:

```
__asm(code [: output_operand_list [: input_operand_list [:
clobbered_register_list]]]);
```

*code* is the assembly code. In this example, this is "ADD %[result], %[input\_i], %[input\_j]".

*output\_operand\_list* is an optional list of output operands, separated by commas. Each operand consists of a symbolic name in square brackets, a constraint string, and a C expression in parentheses. In this example, there is a single output operand: [result] "=r" (res).

*input\_operand\_list* is an optional list of input operands, separated by commas. Input operands use the same syntax as output operands. In this example there are two input operands: [input\_i] "r" (i), [input\_j] "r" (j).

*clobbered\_register\_list* is an optional list of clobbered registers. In this example, this is omitted.

## 3.4 Using intrinsics

Compiler intrinsics are functions provided by the compiler. They enable you to easily incorporate domain-specific operations in C and C++ source code without resorting to complex implementations in assembly language.

The C and C++ languages are suited to a wide variety of tasks but they do not provide in-built support for specific areas of application, for example, *Digital Signal Processing* (DSP).

Within a given application domain, there is usually a range of domain-specific operations that have to be performed frequently. However, often these operations cannot be efficiently implemented in C or C++. A typical example is the saturated add of two 32-bit signed two's complement integers, commonly used in DSP programming. The following example shows a C implementation of a saturated add operation:

```
#include <limits.h>
int L_add(const int a, const int b)
{
    int c;
    c = a + b;
    if (((a ^ b) & INT_MIN) == 0)
    {
        if ((c ^ a) & INT_MIN)
        {
            c = (a < 0) ? INT_MIN : INT_MAX;
        }
    }
    return c;
}
```

Using compiler intrinsics, you can achieve more complete coverage of target architecture instructions than you would from the instruction selection of the compiler.

An intrinsic function has the appearance of a function call in C or C++, but is replaced during compilation by a specific sequence of low-level instructions. The following example shows how to access the `L_add` saturated add intrinsic:

```
#include <dspfns.h> /* Include ETSI intrinsics */
...
int a, b, result;
...
result = L_add(a, b); /* Saturated add of a and b */
```

The use of compiler intrinsics offers a number of performance benefits:

- The low-level instructions substituted for an intrinsic might be more efficient than corresponding implementations in C or C++, resulting in both reduced instruction and cycle counts. To implement the intrinsic, the compiler automatically generates the best sequence of instructions for the specified target architecture. For example, the `L_add` intrinsic maps directly to the A32 assembly language instruction `qadd`:
 

```
QADD r0, r0, r1 /* Assuming r0 = a, r1 = b on entry */
```
- More information is given to the compiler than the underlying C and C++ language is able to convey. This enables the compiler to perform optimizations and to generate instruction sequences that it could not otherwise have performed.

These performance benefits can be significant for real-time processing applications. However, care is required because the use of intrinsics can decrease code portability.

## 3.5 Preventing the use of floating-point instructions and registers

You can instruct the compiler to prevent the use of floating-point instructions and floating-point registers.

The method depends on whether you are compiling for AArch32 state or AArch64 state:

- When compiling for AArch64 state (the default), use the `-mgeneral-regs-only` option:

```
armclang -mgeneral-regs-only test.c
```

- When compiling for AArch32 state, use the `-mfpu=none` option:

```
armclang --target=armv8a-arm-none-eabi -mfpu=none test.c
```

If you specify `-mfpu=none`, you must specify `-mfloat-abi=soft`. This is the default if you omit the `-mfloat-abi` option. Use of `-mfloat-abi=hard`, `softfp` generates an error.

# Chapter 4

## Assembling Assembly Code

Describes how to assemble assembly source code with `armclang` and `armasm`.

It contains the following sections:

- [4.1 Assembling GNU and ARM syntax assembly code on page 4-30.](#)
- [4.2 Preprocessing assembly code on page 4-31.](#)

## 4.1 Assembling GNU and ARM syntax assembly code

The ARM compiler 6 toolchain can assemble both GNU and ARM syntax assembly language source code.

GNU and ARM are two different syntaxes for assembly language source code. They are similar, but have a number of differences. For example, GNU syntax identifies labels by the presence of a colon, while ARM syntax identifies labels by their position at the start of a line.

The following examples show both GNU and ARM syntax assembly code for adding the integers 8 and 6 together.

GNU syntax assembly:

```
.text
main:
    push    {r4-r5,lr}
    mov     r4,#8
    mov     r5,#6
    add     r0,r4,r5
```

ARM syntax assembly:

```
AREA |.text|,CODE,READONLY
main
    push    {r4-r5,lr}
    mov     r4,#8
    mov     r5,#6
    add     r0,r4,r5
END
```

Use GNU syntax for newly created assembly files. Use the `armclang` assembler to assemble GNU assembly language source code. Typically, you invoke the `armclang` assembler as follows:

```
armclang -c -o file.o file.s
```

You might have legacy assembly source files that use the ARM syntax. Use `armasm` to assemble legacy ARM syntax assembly code. Typically, you invoke the `armasm` assembler as follows:

```
armasm --cpu=8-A.64 -o file.o file.s
```

## 4.2 Preprocessing assembly code

Assembly code that contains C directives, for example `#include` or `#define`, must be resolved by the C preprocessor prior to assembling.

By default, `armclang` uses the assembly code source file suffix to determine whether or not to run the C preprocessor:

- The `.s` (lower-case) suffix indicates assembly code that does not require preprocessing.
- The `.S` (upper-case) suffix indicates assembly code that requires preprocessing.

The `-x` option lets you override the default by specifying the language of the source file, rather than inferring the language from the file suffix. Specifically, `-x assembler-with-cpp` indicates that the assembly code contains C directives and `armclang` must run the C preprocessor. The `-x` option only applies to input files that follow it on the command line.

To preprocess an assembly code source file, do one of the following:

- Ensure that the assembly code filename has a `.S` suffix.

For example:

```
armclang -E test.S
```

- Use the `-x assembler-with-cpp` option to tell `armclang` that the assembly source file requires preprocessing.

For example:

```
armclang -E -x assembler-with-cpp test.s
```

---

**Note**

The `-E` option specifies that `armclang` only executes the preprocessor step.

The `-x` option is a GCC-compatible option. See the GCC documentation for a full list of valid values.

# Chapter 5

## Linking Object Files to Produce an Executable

Describes how to link object files to produce an executable image with `arm1ink`.

It contains the following sections:

- [5.1 Linking object files to produce an executable on page 5-33.](#)



## 5.1 Linking object files to produce an executable

The linker combines the contents of one or more object files with selected parts of any required object libraries to produce executable images, partially linked object files, or shared object files.

The command for invoking the linker is:

```
armlink options input-file-list
```

where:

*options*

are linker command-line options.

*input-file-list*

is a space-separated list of objects, libraries, or *symbol definitions* (symdefs) files.

For example, to link the object file `hello_world.o` into an executable image `hello_world.axf`:

```
armlink --force_scanlib -o hello_world.axf hello_world.o
```

---

### Note

The compiler does not generate `$$Lib$Request` symbols when building objects, so `armlink` does not automatically link with the ARM libraries, resulting in the following messages:

```
Warning: L6665W: Neither Lib$$Request$$armlib Lib$$Request$$cpplib defined, not searching ARM libraries.
```

```
Error: L6411E: No compatible library exists with a definition of startup symbol __main.
```

Invoke `armlink` with `--force_scanlib` to link with the ARM libraries. When compiling and linking in one step, the compiler automatically passes this option to `armlink`.

---

# Chapter 6

## Optimization

Describes how to use `armclang` to optimize for either code size or performance, and the impact of the optimization level on the debug illusion.

It contains the following sections:

- [6.1 Optimizing for code size or performance on page 6-35.](#)
- [6.2 How optimization affects the debug illusion on page 6-36.](#)

## 6.1 Optimizing for code size or performance

The compiler and associated tools use numerous techniques for optimizing your code. Some of these techniques improve the performance of your code, while other techniques reduce the size of your code.

These optimizations often work against each other. That is, techniques for improving code performance might result in increased code size, and techniques for reducing code size might reduce performance. For example, the compiler can unroll small loops for higher performance, with the disadvantage of increased code size.

By default, `armclang` does not perform optimization. That is, the default optimization level is `-O0`.

The following `armclang` options help you optimize for code performance:

`-O0` | `-O1` | `-O2` | `-O3`

Specify the level of optimization to be used when compiling source files, where `-O0` is the minimum and `-O3` is the maximum.

`-Ofast`

Enables all the optimizations from `-O3` along with other aggressive optimizations that might violate strict compliance with language standards.

The following `armclang` options help you optimize for code size:

`-Os`

Performs optimizations to reduce the image size at the expense of a possible increase in execution time, balancing code size against code speed.

`-Oz`

Optimizes for code size.

In addition, choices you make during coding can affect optimization. For example:

- Optimizing loop termination conditions can improve both code size and performance. In particular, loops with counters that decrement to zero usually produce smaller, faster code than loops with incrementing counters.
- Manually unrolling loops by reducing the number of loop iterations, but increasing the amount of work done in each iteration can improve performance at the expense of code size.
- Reducing debug information in objects and libraries reduces the size of your image.
- Using inline functions offers a trade-off between code size and performance.
- Using intrinsics can improve performance.

## 6.2 How optimization affects the debug illusion

The precise optimizations performed by the compiler depend both on the level of optimization chosen, and whether you are optimizing for performance or code size.

The lowest optimization level, `-O0`, provides the best debug experience. Increasing levels of optimization results in an increasingly degraded debug view.

# Chapter 7

## Coding Considerations

Describes how you can use programming practices and techniques to increase the portability, efficiency and robustness of your C and C++ source code.

It contains the following sections:

- *7.1 Optimization of loop termination in C code* on page 7-38.
- *7.2 Loop unrolling in C code* on page 7-40.
- *7.3 Compiler optimization and the volatile keyword* on page 7-42.
- *7.4 Stack use in C and C++* on page 7-44.
- *7.5 Methods of minimizing function parameter passing overhead* on page 7-46.
- *7.6 Inline functions* on page 7-47.
- *7.7 Integer division-by-zero errors in C code* on page 7-48.
- *7.8 About trapping integer division-by-zero errors with `__aeabi_idiv0()`* on page 7-49.
- *7.9 About trapping integer division-by-zero errors with `__rt_raise()`* on page 7-50.
- *7.10 Identification of integer division-by-zero errors in C code* on page 7-51.

## 7.1 Optimization of loop termination in C code

Loops are a common construct in most programs. Because a significant amount of execution time is often spent in loops, it is worthwhile paying attention to time-critical loops.

The loop termination condition can cause significant overhead if written without caution. Where possible:

- Use simple termination conditions.
- Write count-down-to-zero loops.
- Use counters of type **unsigned int**.
- Test for equality against zero.

Following any or all of these guidelines, separately or in combination, is likely to result in better code.

The following table shows two sample implementations of a routine to calculate  $n!$  that together illustrate loop termination overhead. The first implementation calculates  $n!$  using an incrementing loop, while the second routine calculates  $n!$  using a decrementing loop.

**Table 7-1 C code for incrementing and decrementing loops**

Incrementing loop	Decrementing loop
<pre>int fact1(int n) {     int i, fact = 1;     for (i = 1; i &lt;= n; i++)         fact *= i;     return (fact); }</pre>	<pre>int fact2(int n) {     unsigned int i, fact = 1;     for (i = n; i != 0; i--)         fact *= i;     return (fact); }</pre>

The following table shows the corresponding disassembly of the machine code produced by `armclang -Os -S --target=armv8a-arm-none-eabi` for each of the sample implementations above.

**Table 7-2 C Disassembly for incrementing and decrementing loops**

Incrementing loop	Decrementing loop
<pre>fact1:     mov     r1, r0     mov     r0, #1     cmp     r1, #1     bxlt    lr     mov     r2, #0 .LBB0_1:     add     r2, r2, #1     mul     r0, r0, r2     cmp     r1, r2     bne     .LBB0_1     bx     lr</pre>	<pre>fact2:     mov     r1, r0     mov     r0, #1     cmp     r1, #0     bxeq    lr .LBB1_1:     mul     r0, r0, r1     subs   r1, r1, #1     bne     .LBB1_1     bx     lr</pre>

Comparing the disassemblies shows that the ADD and CMP instruction pair in the incrementing loop disassembly has been replaced with a single SUBS instruction in the decrementing loop disassembly. Because the SUBS instruction updates the status flags, including the Z flag, there is no requirement for an explicit CMP `r1, r2` instruction.

In addition to saving an instruction in the loop, the variable `n` does not have to be available for the lifetime of the loop, reducing the number of registers that have to be maintained. This eases register allocation. It is even more important if the original termination condition involves a function call. For example:

```
for (...; i < get_limit(); ...);
```

The technique of initializing the loop counter to the number of iterations required, and then decrementing down to zero, also applies to **while** and **do** statements.

## 7.2 Loop unrolling in C code

Loops are a common construct in most programs. Because a significant amount of execution time is often spent in loops, it is worthwhile paying attention to time-critical loops.

Small loops can be unrolled for higher performance, with the disadvantage of increased code size. When a loop is unrolled, the loop counter requires updating less often and fewer branches are executed. If the loop iterates only a few times, it can be fully unrolled so that the loop overhead completely disappears. The compiler unrolls loops automatically at `-O3 -Otime`. Otherwise, any unrolling must be done in source code.

———— **Note** —————

Manual unrolling of loops might hinder the automatic re-rolling of loops and other loop optimizations by the compiler.

The advantages and disadvantages of loop unrolling can be illustrated using the two sample routines shown in the following table. Both routines efficiently test a single bit by extracting the lowest bit and counting it, after which the bit is shifted out.

The first implementation uses a loop to count bits. The second routine is the first implementation unrolled four times, with an optimization applied by combining the four shifts of `n` into one shift.

Unrolling frequently provides new opportunities for optimization.

**Table 7-3 C code for rolled and unrolled bit-counting loops**

Bit-counting loop	Unrolled bit-counting loop
<pre>int countbit1(unsigned int n) {     int bits = 0;     while (n != 0)     {         if (n &amp; 1) bits++;         n &gt;&gt;= 1;     }     return bits; }</pre>	<pre>int countbit2(unsigned int n) {     int bits = 0;     while (n != 0)     {         if (n &amp; 1) bits++;         if (n &amp; 2) bits++;         if (n &amp; 4) bits++;         if (n &amp; 8) bits++;         n &gt;&gt;= 4;     }     return bits; }</pre>

The following table shows the corresponding disassembly of the machine code produced by the compiler for each of the sample implementations above, where the C code for each implementation has been compiled using `armclang -O5 -S --target=armv8a-arm-none-eabi`.



**Table 7-4 Disassembly for rolled and unrolled bit-counting loops**

Bit-counting loop	Unrolled bit-counting loop
<pre> countbit1:     mov     r1, r0     mov     r0, #0     cmp     r1, #0     bxeq    lr     mov     r2, #0 .LBB0_1:     and     r3, r1, #1     cmp     r2, r1, lsr #1     add     r0, r0, r3     lsr    r3, r1, #1     mov     r1, r3     bne    .LBB0_1     bx     lr </pre>	<pre> countbit2:     mov     r1, r0     mov     r0, #0     cmp     r1, #0     bxeq    lr     mov     r2, #0 .LBB1_1:     and     r3, r1, #1     cmp     r2, r1, lsr #4     add     r0, r0, r3     ubfx   r3, r1, #1, #1     add     r0, r0, r3     ubfx   r3, r1, #2, #1     add     r0, r0, r3     ubfx   r3, r1, #3, #1     add     r0, r0, r3     lsr    r3, r1, #4     mov     r1, r3     bne    .LBB1_1     bx     lr </pre>

The unrolled version of the bit-counting loop is faster than the original version, but has a larger code size.

## 7.3 Compiler optimization and the volatile keyword

Higher optimization levels can reveal problems in some programs that are not apparent at lower optimization levels, for example, missing **volatile** qualifiers.

This can manifest itself in a number of ways. Code might become stuck in a loop while polling hardware, multi-threaded code might exhibit strange behavior, or optimization might result in the removal of code that implements deliberate timing delays. In such cases, it is possible that some variables are required to be declared as **volatile**.

The declaration of a variable as **volatile** tells the compiler that the variable can be modified at any time externally to the implementation, for example, by the operating system, by another thread of execution such as an interrupt routine or signal handler, or by hardware. Because the value of a **volatile**-qualified variable can change at any time, the actual variable in memory must always be accessed whenever the variable is referenced in code. This means the compiler cannot perform optimizations on the variable, for example, caching its value in a register to avoid memory accesses. Similarly, when used in the context of implementing a sleep or timer delay, declaring a variable as **volatile** tells the compiler that a specific type of behavior is intended, and that such code must not be optimized in such a way that it removes the intended functionality.

In contrast, when a variable is not declared as **volatile**, the compiler can assume its value cannot be modified in unexpected ways. Therefore, the compiler can perform optimizations on the variable.

The use of the **volatile** keyword is illustrated in the two sample routines in the following table. Both of these routines read a buffer in a loop until a status flag `buffer_full` is set to true. The state of `buffer_full` can change asynchronously with program flow.

The two versions of the routine differ only in the way that `buffer_full` is declared. The first routine version is incorrect. Notice that the variable `buffer_full` is not qualified as **volatile** in this version. In contrast, the second version of the routine shows the same loop where `buffer_full` is correctly qualified as **volatile**.

**Table 7-5 C code for nonvolatile and volatile buffer loops**

Nonvolatile version of buffer loop	Volatile version of buffer loop
<pre>int buffer_full; int read_stream(void) {     int count = 0;     while (!buffer_full)     {         count++;     }     return count; }</pre>	<pre>volatile int buffer_full; int read_stream(void) {     int count = 0;     while (!buffer_full)     {         count++;     }     return count; }</pre>

The following table shows the corresponding disassembly of the machine code produced by the compiler for each of the examples above, where the C code for each implementation has been compiled using `armclang -Os -S --target=armv8a-arm-none-eabi`.

**Table 7-6 Disassembly for nonvolatile and volatile buffer loop**

Nonvolatile version of buffer loop	Volatile version of buffer loop
<pre> read_stream:   movw    r0, :lower16:buffer_full   movt    r0, :upper16:buffer_full   ldr     r1, [r0]   mvn     r0, #0 .LBB0_1:   add     r0, r0, #1   cmp     r1, #0   beq     .LBB0_1    ; infinite loop   bx     lr           </pre>	<pre> read_stream:   movw    r1, :lower16:buffer_full   mvn     r0, #0   movt    r1, :upper16:buffer_full .LBB1_1:   ldr     r2, [r1]    ; buffer_full   add     r0, r0, #1   cmp     r2, #0   beq     .LBB1_1   bx     lr           </pre>

In the disassembly of the nonvolatile version of the buffer loop in the above table, the statement `LDR r1, [r0]` loads the value of `buffer_full` into register `r1` outside the loop labeled `.LBB0_1`. Because `buffer_full` is not declared as **volatile**, the compiler assumes that its value cannot be modified outside the program. Having already read the value of `buffer_full` into `r0`, the compiler omits reloading the variable when optimizations are enabled, because its value cannot change. The result is the infinite loop labeled `.LBB0_1`.

In contrast, in the disassembly of the volatile version of the buffer loop, the compiler assumes the value of `buffer_full` can change outside the program and performs no optimizations. Consequently, the value of `buffer_full` is loaded into register `r2` inside the loop labeled `.LBB1_1`. As a result, the loop `.LBB1_1` is implemented correctly in assembly code.

To avoid optimization problems caused by changes to program state external to the implementation, you must declare variables as **volatile** whenever their values can change unexpectedly in ways unknown to the implementation.

In practice, you must declare a variable as **volatile** whenever you are:

- Accessing memory-mapped peripherals.
- Sharing global variables between multiple threads.
- Accessing global variables in an interrupt routine or signal handler.

The compiler does not optimize the variables you have declared as **volatile**.

## 7.4 Stack use in C and C++

C and C++ both use the stack intensively.

For example, the stack holds:

- The return address of functions.
- Registers that must be preserved, as determined by the *ARM Architecture Procedure Call Standard for the ARM 64-bit Architecture (AAPCS64)*, for instance, when register contents are saved on entry into subroutines.
- Local variables, including local arrays, structures, unions, and in C++, classes.

Some stack usage is not obvious, such as:

- Local integer or floating point variables are allocated stack memory if they are spilled (that is, not allocated to a register).
- Structures are normally allocated to the stack. A space equivalent to `sizeof(struct)` padded to a multiple of 16 bytes is reserved on the stack. The compiler tries to allocate structures to registers instead.
- If the size of an array is known at compile time, the compiler allocates memory on the stack. Again, a space equivalent to `sizeof(struct)` padded to a multiple of 16 bytes is reserved on the stack.

———— **Note** —————

Memory for variable length arrays is allocated at runtime, on the heap.

- Several optimizations can introduce new temporary variables to hold intermediate results. The optimizations include: CSE elimination, live range splitting and structure splitting. The compiler tries to allocate these temporary variables to registers. If not, it spills them to the stack.
- Generally, code compiled for processors that support only 16-bit encoded Thumb instructions makes more use of the stack than A64 code, ARM code and code compiled for processors that support 32-bit encoded Thumb instructions. This is because 16-bit encoded Thumb instructions have only eight registers available for allocation, compared to fourteen for ARM code and 32-bit encoded Thumb instructions.
- The AAPCS64 requires that some function arguments are passed through the stack instead of the registers, depending on their type, size, and order.

### Methods of estimating stack usage

Stack use is difficult to estimate because it is code dependent, and can vary between runs depending on the code path that the program takes on execution. However, it is possible to manually estimate the extent of stack utilization using the following methods:

- Link with `--callgraph` to produce a static callgraph. This shows information on all functions, including stack use.

This uses DWARF frame information from the `.debug_frame` section. Compile with the `-g` option to generate the necessary DWARF information.

- Link with `--info=stack` or `--info=summarystack` to list the stack usage of all global symbols.
- Use the debugger to set a watchpoint on the last available location in the stack and see if the watchpoint is ever hit.
- Use the debugger, and:
  1. Allocate space in memory for the stack that is much larger than you expect to require.
  2. Fill the stack space with copies of a known value, for example, `0xDEADDEAD`.
  3. Run your application, or a fixed portion of it. Aim to use as much of the stack space as possible in the test run. For example, try to execute the most deeply nested function calls and the worst case

path found by the static analysis. Try to generate interrupts where appropriate, so that they are included in the stack trace.

4. After your application has finished executing, examine the stack space of memory to see how many of the known values have been overwritten. The space has garbage in the used part and the known values in the remainder.
5. Count the number of garbage values and multiply by `sizeof(value)`, to give their size, in bytes.

The result of the calculation shows how the size of the stack has grown, in bytes.

- Use Fixed Virtual Platforms (FVP), and define a region of memory where access is not allowed directly below your stack in memory, with a map file. If the stack overflows into the forbidden region, a data abort occurs, which can be trapped by the debugger.

### Methods of reducing stack usage

In general, you can lower the stack requirements of your program by:

- Writing small functions that only require a small number of variables.
- Avoiding the use of large local structures or arrays.
- Avoiding recursion, for example, by using an alternative algorithm.
- Minimizing the number of variables that are in use at any given time at each point in a function.
- Using C block scope and declaring variables only where they are required, so overlapping the memory used by distinct scopes.

The use of C block scope involves declaring variables only where they are required. This minimizes use of the stack by overlapping memory required by distinct scopes.

## 7.5 Methods of minimizing function parameter passing overhead

There are a number of ways in which you can minimize the overhead of passing parameters to functions.

For example:

- In AArch64 state, 8 integer and 8 floating point arguments (16 in total) can be passed efficiently. In AArch32 state, ensure that functions take four or fewer arguments if each argument is a word or less in size. In C++, ensure that nonstatic member functions take no more than one fewer argument than the efficient limit, because of the implicit `this` pointer argument that is usually passed in `R0`.
- Ensure that a function does a significant amount of work if it requires more than the efficient limit of arguments, so that the cost of passing the stacked arguments is outweighed.
- Put related arguments in a structure, and pass a pointer to the structure in any function call. This reduces the number of parameters and increases readability.
- For 32-bit architectures, minimize the number of `long long` parameters, because these take two argument words that have to be aligned on an even register index.
- For 32-bit architectures, minimize the number of `double` parameters when using software floating-point.

## 7.6 Inline functions

Inline functions offer a trade-off between code size and performance. By default, the compiler decides for itself whether to inline code or not.

See the Clang documentation for more information about inline functions.

### Related information

*[Language Compatibility.](#)*

## 7.7 Integer division-by-zero errors in C code

For targets that do not support the SDIV divide instruction, you can trap and identify integer division-by-zero errors with the appropriate C library helper functions, `__aeabi_idiv0()` and `__rt_raise()`

### Related concepts

*7.8 About trapping integer division-by-zero errors with `__aeabi_idiv0()` on page 7-49.*

*7.9 About trapping integer division-by-zero errors with `__rt_raise()` on page 7-50.*

*7.10 Identification of integer division-by-zero errors in C code on page 7-51.*



## 7.8 About trapping integer division-by-zero errors with `__aeabi_idiv0()`

You can trap integer division-by-zero errors with the C library helper function `__aeabi_idiv0()` so that division by zero returns some standard result, for example zero.

Integer division is implemented in code through the C library helper functions `__aeabi_idiv()` and `__aeabi_uidiv()`. Both functions check for division by zero.

When integer division by zero is detected, a branch to `__aeabi_idiv0()` is made. To trap the division by zero, therefore, you only have to place a breakpoint on `__aeabi_idiv0()`.

The library provides two implementations of `__aeabi_idiv0()`. The default one does nothing, so if division by zero is detected, the division function returns zero. However, if you use signal handling, an alternative implementation is selected that calls `__rt_raise(SIGFPE, DIVBYZERO)`.

If you provide your own version of `__aeabi_idiv0()`, then the division functions call this function. The function prototype for `__aeabi_idiv0()` is:

```
int __aeabi_idiv0(void);
```

If `__aeabi_idiv0()` returns a value, that value is used as the quotient returned by the division function.

## 7.9 About trapping integer division-by-zero errors with `__rt_raise()`

By default, integer division by zero returns zero. If you want to intercept division by zero, you can re-implement the C library helper function `__rt_raise()`.

The function prototype for `__rt_raise()` is:

```
void __rt_raise(int signal, int type);
```

If you re-implement `__rt_raise()`, then the library automatically provides the signal-handling library version of `__aeabi_idiv0()`, which calls `__rt_raise()`, then that library version of `__aeabi_idiv0()` is included in the final image.

In that case, when a divide-by-zero error occurs, `__aeabi_idiv0()` calls `__rt_raise(SIGFPE, DIVBYZERO)`. Therefore, if you re-implement `__rt_raise()`, you must check `(signal == SIGFPE) && (type == DIVBYZERO)` to determine if division by zero has occurred.

## 7.10 Identification of integer division-by-zero errors in C code

On entry into `__aeabi_idiv0()`, the link register LR contains the address of the instruction *after* the call to the `__aeabi_uidiv()` division routine in your application code.

The offending line in the source code can be identified by looking up the line of C code in the debugger at the address given by LR.

# Chapter 8

## Language Compatibility and Extensions

Describes the language extensions that the compiler supports.

It contains the following sections:

- [8.1 Language compatibility and extensions on page 8-53.](#)

## 8.1 Language compatibility and extensions

`armclang` conforms to the Clang 3.4 specification for language compatibility, language extensions, and C++ status. See the Clang documentation for more information.

Specifically, see the following:

- Language compatibility:  
<http://clang.llvm.org/compatibility.html>
- Language extensions:  
<http://clang.llvm.org/docs/LanguageExtensions.html>
- C++ status:  
[http://clang.llvm.org/cxx\\_status.html](http://clang.llvm.org/cxx_status.html)

See the *armclang Reference Guide* for information about ARM-specific language extensions.

### Related information

*armclang Reference Guide*.