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**Arm® Cortex®-A32 Processor Technical Reference Manual**

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</tr>
<tr>
<td>C10.37</td>
<td>ID Register 5</td>
<td>C10-548</td>
</tr>
<tr>
<td>C10.38</td>
<td>ID Register 6</td>
<td>C10-549</td>
</tr>
<tr>
<td>C10.39</td>
<td>ID Register 7</td>
<td>C10-550</td>
</tr>
<tr>
<td>C10.40</td>
<td>ID Register 8</td>
<td>C10-551</td>
</tr>
<tr>
<td>C10.41</td>
<td>ID Register 9</td>
<td>C10-552</td>
</tr>
<tr>
<td>C10.42</td>
<td>ID Register 10</td>
<td>C10-553</td>
</tr>
<tr>
<td>C10.43</td>
<td>ID Register 11</td>
<td>C10-554</td>
</tr>
<tr>
<td>C10.44</td>
<td>ID Register 12</td>
<td>C10-555</td>
</tr>
<tr>
<td>C10.45</td>
<td>ID Register 13</td>
<td>C10-556</td>
</tr>
<tr>
<td>C10.46</td>
<td>ID Register 14</td>
<td>C10-557</td>
</tr>
<tr>
<td>C10.47</td>
<td>ID Register 15</td>
<td>C10-558</td>
</tr>
<tr>
<td>C10.48</td>
<td>ID Register 16</td>
<td>C10-559</td>
</tr>
<tr>
<td>C10.49</td>
<td>ID Register 17</td>
<td>C10-560</td>
</tr>
<tr>
<td>C10.50</td>
<td>ID Register 18</td>
<td>C10-561</td>
</tr>
<tr>
<td>C10.51</td>
<td>ID Register 19</td>
<td>C10-562</td>
</tr>
<tr>
<td>C10.52</td>
<td>ID Register 20</td>
<td>C10-563</td>
</tr>
<tr>
<td>C10.53</td>
<td>ID Register 21</td>
<td>C10-564</td>
</tr>
<tr>
<td>C10.54</td>
<td>ID Register 22</td>
<td>C10-565</td>
</tr>
<tr>
<td>C10.55</td>
<td>ID Register 23</td>
<td>C10-566</td>
</tr>
<tr>
<td>C10.56</td>
<td>ID Register 24</td>
<td>C10-567</td>
</tr>
<tr>
<td>C10.57</td>
<td>ID Register 25</td>
<td>C10-568</td>
</tr>
<tr>
<td>C10.58</td>
<td>ID Register 26</td>
<td>C10-569</td>
</tr>
<tr>
<td>C10.59</td>
<td>ID Register 27</td>
<td>C10-570</td>
</tr>
<tr>
<td>C10.60</td>
<td>ID Register 28</td>
<td>C10-571</td>
</tr>
<tr>
<td>C10.61</td>
<td>ID Register 29</td>
<td>C10-572</td>
</tr>
<tr>
<td>C10.62</td>
<td>ID Register 30</td>
<td>C10-573</td>
</tr>
<tr>
<td>C10.63</td>
<td>ID Register 31</td>
<td>C10-574</td>
</tr>
<tr>
<td>C10.64</td>
<td>ID Register 32</td>
<td>C10-575</td>
</tr>
<tr>
<td>C10.65</td>
<td>ID Register 33</td>
<td>C10-576</td>
</tr>
<tr>
<td>C10.66</td>
<td>ID Register 34</td>
<td>C10-577</td>
</tr>
<tr>
<td>C10.67</td>
<td>ID Register 35</td>
<td>C10-578</td>
</tr>
<tr>
<td>C10.68</td>
<td>ID Register 36</td>
<td>C10-579</td>
</tr>
<tr>
<td>C10.69</td>
<td>ID Register 37</td>
<td>C10-580</td>
</tr>
<tr>
<td>C10.70</td>
<td>ID Register 38</td>
<td>C10-581</td>
</tr>
<tr>
<td>C10.71</td>
<td>ID Register 39</td>
<td>C10-582</td>
</tr>
<tr>
<td>C10.72</td>
<td>ID Register 40</td>
<td>C10-583</td>
</tr>
<tr>
<td>C10.73</td>
<td>ID Register 41</td>
<td>C10-584</td>
</tr>
<tr>
<td>C10.74</td>
<td>ID Register 42</td>
<td>C10-585</td>
</tr>
<tr>
<td>C10.75</td>
<td>ID Register 43</td>
<td>C10-586</td>
</tr>
<tr>
<td>C10.76</td>
<td>ID Register 44</td>
<td>C10-587</td>
</tr>
<tr>
<td>C10.77</td>
<td>ID Register 45</td>
<td>C10-588</td>
</tr>
<tr>
<td>C10.78</td>
<td>ID Register 46</td>
<td>C10-589</td>
</tr>
<tr>
<td>C10.79</td>
<td>ID Register 47</td>
<td>C10-590</td>
</tr>
<tr>
<td>C10.80</td>
<td>ID Register 48</td>
<td>C10-591</td>
</tr>
</tbody>
</table>
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Preface

This preface introduces the Arm® Cortex®-A32 Processor Technical Reference Manual.

It contains the following:

- *Feedback* on page 22.
About this book

This Technical Reference Manual is for the Cortex®-A32 processor. It provides reference documentation and contains programming details for registers. It also describes the memory system, the caches, the interrupts, and the debug features.

Product revision status

The \texttt{rm\textsubscript{pn}} identifier indicates the revision status of the product described in this book, for example, \texttt{r1p2}, where:

\begin{itemize}
  \item \texttt{rm} Identifies the major revision of the product, for example, \texttt{r1}.
  \item \texttt{pn} Identifies the minor revision or modification status of the product, for example, \texttt{p2}.
\end{itemize}

Intended audience

This manual is written for system designers, system integrators, and programmers who are designing or programming a System-on-Chip (SoC) that uses the Cortex®-A32 processor.

Using this book

This book is organized into the following chapters:

\textbf{Part A Functional Description}

This part describes the main functionality of the Cortex-A32 processor.

\textbf{Chapter A1 Introduction}

This chapter provides an overview of the Cortex-A32 processor and its features.

\textbf{Chapter A2 Technical Overview}

This chapter describes the structure of the Cortex-A32 processor.

\textbf{Chapter A3 Clocks, Resets, and Input Synchronization}

This chapter describes the clocks of the Cortex-A32 processor. It also describes the reset options.

\textbf{Chapter A4 Power Management}

This chapter describes the power domains and the power modes in the Cortex-A32 processor.

\textbf{Chapter A5 Cache Behavior and Cache Protection}

This chapter describes the CPU and SCU cache protection features of the Cortex-A32 processor.

\textbf{Chapter A6 L1 Memory System}

This chapter describes the L1 instruction cache and data cache.

\textbf{Chapter A7 L2 Memory System}

This chapter describes the L2 memory system and the \textit{Snoop Control Unit} (SCU) that is tightly integrated with it.

\textbf{Chapter A8 AXI Master Interface}

This chapter describes the AXI master memory interface.

\textbf{Chapter A9 ACE Master Interface}

This chapter describes the ACE master interface.

\textbf{Chapter A10 CHI Master Interface}

This chapter describes the CHI master memory interface.

\textbf{Chapter A11 ACP Slave Interface}

This chapter describes the ACP slave interface.

\textbf{Chapter A12 GIC CPU Interface}

This chapter describes the \textit{Generic Interrupt Controller} (GIC) CPU interface of the processor.

\textbf{Part B Register Descriptions}

This part describes the non-debug registers of the Cortex-A32 processor.
Chapter B1 AArch32 system registers
This chapter describes the system registers in the AArch32 state.

Chapter B2 GIC registers
This chapter describes the GIC registers.

Chapter B3 Generic Timer registers
This chapter describes the Generic Timer registers.

Part C Debug
This part describes the debug functionality and registers of the Cortex-A32 processor.

Chapter C1 Debug
This chapter describes the debug features of the processor.

Chapter C2 PMU
This chapter describes the Performance Monitor Unit (PMU) of the processor.

Chapter C3 ETM
This chapter describes the Embedded Trace Macrocell (ETM) of the processor.

Chapter C4 CTI
This chapter describes the cross-trigger components of the processor.

Chapter C5 Direct access to internal memory
This chapter describes the direct access to internal memory that caches and TLBs use.

Chapter C6 AArch32 debug registers
This chapter describes the debug registers in the AArch32 execution state and shows examples of how to use them.

Chapter C7 Memory-mapped debug registers
This chapter describes the debug memory-mapped registers and shows examples of how to use them.

Chapter C8 ROM table
This chapter describes the ROM table that debuggers can use to determine which components are implemented. It also describes the ROM table registers.

Chapter C9 PMU registers
This chapter describes the PMU registers.

Chapter C10 ETM registers
This chapter describes the ETM registers.

Chapter C11 CTI registers
This chapter describes the CTI registers.

Part D Appendices

Appendix A Signal Descriptions
This appendix describes the signals at the external interfaces of the processor.

Appendix B AArch32 UNPREDICTABLE Behaviors
The cases in which the Cortex-A32 processor implementation diverges from the preferred behavior described in Armv8 AArch32 UNPREDICTABLE behaviors.

Appendix C Revisions
This appendix describes the technical changes between released issues of this book.

Glossary
The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.
See the *Arm® Glossary* for more information.

**Typographic conventions**

*italic*

Introduces special terminology, denotes cross-references, and citations.

**bold**

Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

**monospace**

Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

**monospace**

Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

**monospace italic**

Denotes arguments to monospace text where the argument is to be replaced by a specific value.

**monospace bold**

Denotes language keywords when used outside example code.

<and>

Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

**SMALL CAPITALS**

Used in body text for a few terms that have specific technical meanings, that are defined in the *Arm® Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

**Timing diagrams**

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

![Figure 1  Key to timing diagram conventions](image)

**Signals**

The signal conventions are:
Signal level

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n

At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

- Arm® AMBA® AXI and ACE Protocol Specification AXI, AXI4, and AXI4-Lite, ACE and ACE-Lite (IHI 0022).
- Arm® Low Power Interface Specification Q-Channel and P-Channel Interfaces (IHI 0068).
- Arm® Generic Interrupt Controller Architecture Specification (IHI 0069).
- Arm® CoreSight™ Architecture Specification (IHI 0029).

The following confidential books are only available to licensees:

- Arm® Cortex®-A32 Processor Integration Manual (100245).
- Arm® AMBA® 5 CHI Protocol Specification (IHI 0050).
- Arm® Armv8 AAarch32 UNPREDICTABLE behaviors (PRD03-GENC-010544).

Other publications

This section lists relevant documents published by third parties:


Note

Arm floating-point terminology is largely based on the earlier ANSI/IEEE Std 754-1985 issue of the standard. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.
Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:
• The product name.
• The product revision or version.
• An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to errata@arm.com. Give:
• The number 100241_0100_00_en.
• If applicable, the page number(s) to which your comments refer.
• A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

Note

Arm tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.
Part A

Functional Description
Chapter A1
Introduction

This chapter provides an overview of the Cortex-A32 processor and its features.

It contains the following sections:
A1.1 About the Cortex®-A32 processor

The Cortex-A32 processor is a product designed to give mid-range instruction execution performance with low power consumption. It is highly configurable, allowing you to select features that are appropriate for the SoC in which it is used.

The major configuration options are:

- One to four Armv8-A compliant cores with automatic data cache coherency.
- One shared L2 cache.
- An AXI, ACE, or CHI system bus interface.

The processor also contains:

- Logic to help with power management.
- GICv4 interrupt capability.
- A complete CoreSight subsystem to support embedded debug in each core.
- An optional ACP that allows for I/O coherent operations with an external master, for example a DMA engine.

The following figure shows an example configuration with four cores, an L2 cache, and a CHI system bus interface.

![Example processor configuration](image)

\[Figure \text{A1-1} \text{ Example processor configuration}\]

Related information

A1.2 Features on page A1-27
A1.3 Implementation options on page A1-28
A1.4 Supported standards and specifications on page A1-30
A1.5 Test features on page A1-31
A2.1 Components on page A2-36
A2.2 Interfaces on page A2-40
A1.2 Features

The Cortex-A32 processor includes the following features:

- Full implementation of the Armv8-A A32 and T32 instruction sets.
- The AArch32 execution state at all Exception levels (EL0 to EL3).
- In-order pipeline with direct and indirect branch prediction.
- Separate Level 1 (L1) data and instruction side memory systems with a Memory Management Unit (MMU).
- Level 2 (L2) memory system that provides cluster memory coherency.
- Optional L2 cache.
- Cache protection in the form of Error Correction Code (ECC) or parity on all RAM instances, except for the L2 victim RAM. There are two implementation options:
  — CPU cache protection.
  — Snoop Control Unit (SCU)-L2 cache protection.
- TrustZone®.
- Optional data engine that implements the Advanced SIMD and floating-point architecture support.
- Optional Cryptographic Extension. This architectural extension is only available if the data engine is present.
- Armv8 debug logic.
- Performance Monitoring Unit (PMU).
- Optional Embedded Trace Macrocell (ETM) that supports instruction trace only.
- Optional Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor.
- Generic Timers supporting 64-bit count input from an external system counter.

Related information

A1.3 Implementation options on page A1-28
A1.4 Supported standards and specifications on page A1-30
A6.1 About the L1 memory system on page A6-86
A7.1 About the L2 memory system on page A7-92
A5.7 About cache protection on page A5-80
A1.3 Implementation options

The Cortex-A32 processor is highly configurable. Build-time configuration options make it possible to meet functional requirements with the smallest possible area and power.

In a configuration with more than one core, Advanced SIMD and floating-point support can be implemented on all cores, zero cores, or a subset of cores. If the Cryptographic Extension is included, it is included on all cores that implement Advanced SIMD and floating-point support. All cores have the same build-time configuration for other features.

The following table lists the implementation options for a core.

Table A1-1 Implementation options for a core

<table>
<thead>
<tr>
<th>Feature</th>
<th>Range of options</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 instruction cache size</td>
<td>• 8K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 16K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 32K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 64K</td>
<td></td>
</tr>
<tr>
<td>L1 data cache size</td>
<td>• 8K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 16K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 32K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 64K</td>
<td></td>
</tr>
<tr>
<td>CPU cache protection</td>
<td>• Included</td>
<td>• Not available if the L2 cache is implemented without SCU-L2 cache protection.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td>• Also protects the L1 duplicate tags in the SCU.</td>
</tr>
<tr>
<td>GIC CPU interface</td>
<td>• Included</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>ETM</td>
<td>• Included</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>Advanced SIMD and floating-point support</td>
<td>• Included</td>
<td>Advanced SIMD and floating-point support is configured on a per-core basis.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>Cryptographic Extension</td>
<td>• Included</td>
<td>If the Cryptographic Extension is included, then it is included on all cores that implement Advanced SIMD and floating-point support. There is no option to implement the Cryptographic Extension without Advanced SIMD and floating-point support.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
</tbody>
</table>

The following table lists the implementation options at build time for the processor.

Table A1-2 Implementation options for the processor

<table>
<thead>
<tr>
<th>Feature</th>
<th>Range of options</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of cores</td>
<td>• 1</td>
<td>All cores have the same build-time configuration.</td>
</tr>
<tr>
<td></td>
<td>• 2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 4</td>
<td></td>
</tr>
<tr>
<td>Main bus interface</td>
<td>• AMBA 4 AXI</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• AMBA 4 ACE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• AMBA 5 CHI</td>
<td></td>
</tr>
<tr>
<td>Feature</td>
<td>Range of options</td>
<td>Notes</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-----------------------------------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>L2 cache</td>
<td>• Included</td>
<td>If it is present, all cores share one L2 cache.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>L2 cache size</td>
<td>• 128K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 256K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 512K</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 1024K</td>
<td></td>
</tr>
<tr>
<td>L2 data RAM input latency</td>
<td>• 1 cycle</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 2 cycles</td>
<td></td>
</tr>
<tr>
<td>L2 data RAM output latency</td>
<td>• 2 cycles</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 3 cycles</td>
<td></td>
</tr>
<tr>
<td>SCU-L2 cache protection</td>
<td>• Included</td>
<td>Protects the L2 tag and L2 data RAMs with ECC.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>Accelerator Coherency Port (ACP)</td>
<td>• Included</td>
<td>Part of the SCU-L2. If the processor does not include an L2 cache, it cannot implement the ACP.</td>
</tr>
<tr>
<td></td>
<td>• Not included</td>
<td></td>
</tr>
<tr>
<td>Debug memory map</td>
<td>• v8 debug memory map</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• v7 debug memory map</td>
<td></td>
</tr>
</tbody>
</table>

**Related information**

*A2.2 Interfaces* on page A2-40  
*A5.5 Invalidating or cleaning a cache* on page A5-78  
*A6.1 About the L1 memory system* on page A6-86  
*A7.1 About the L2 memory system* on page A7-92  
*A5.7 About cache protection* on page A5-80  
*Chapter A12 GIC CPU Interface* on page A12-135  
*C1.6 Debug memory map* on page C1-371  
*C3.1 About the ETM* on page C3-386
A1.4 Supported standards and specifications

The Cortex-A32 processor implements the Armv8-A architecture and some architecture extensions. It also supports various interconnect, interrupt, timer, debug, and trace architectures.

Table A1-3 Compliance with standards and specifications

<table>
<thead>
<tr>
<th>Architecture specification or standard</th>
<th>Version</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Arm architecture</td>
<td>Armv8-A</td>
<td>• AArch32 execution state at all Exception levels.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• A32 and T32 instruction sets.</td>
</tr>
<tr>
<td>Arm architecture extensions</td>
<td>• Advanced SIMD and floating-point support</td>
<td>• You cannot implement floating-point without Advanced SIMD.</td>
</tr>
<tr>
<td></td>
<td>• Cryptographic Extension</td>
<td>• You cannot implement the Cryptographic Extension without the Advanced SIMD and floating-point support.</td>
</tr>
<tr>
<td>Interconnect</td>
<td>• AMBA 4 AXI</td>
<td>You can also connect the processor to an AMBA 3 AXI interconnect.</td>
</tr>
<tr>
<td></td>
<td>• AMBA 4 ACE</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• AMBA 5 CHI</td>
<td></td>
</tr>
<tr>
<td>Generic Interrupt Controller</td>
<td>v4</td>
<td>-</td>
</tr>
<tr>
<td>Generic Timer</td>
<td>Armv8-A</td>
<td>-</td>
</tr>
<tr>
<td>PMU</td>
<td>v3</td>
<td>-</td>
</tr>
<tr>
<td>Debug</td>
<td>Armv8</td>
<td>-</td>
</tr>
<tr>
<td>CoreSight</td>
<td>v2</td>
<td>-</td>
</tr>
<tr>
<td>Embedded Trace Macrocell</td>
<td>ETMv4</td>
<td>-</td>
</tr>
</tbody>
</table>

Related information

Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile
Arm® AMBA® 5 CHI Protocol Specification
Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite
Arm® Generic Interrupt Controller Architecture Specification
Arm® CoreSight™ Architecture Specification
Arm® ETM Architecture Specification, ETMv4
A1.5 Test features

The Cortex-A32 processor provides test signals that enable the use of both ATPG and MBIST to test the processor and its memory arrays.

Related information
A.20 DFT interface signals on page Appx-A-648
A.21 MBIST interface signals on page Appx-A-649
A1.6 Design tasks

The Cortex-A32 processor is delivered as a synthesizable Register Transfer Level (RTL) description in the Verilog HDL. Before you can use it, you must implement, integrate, and program it.

A different party can perform each of the following tasks. Each task can include implementation and integration choices that affect the behavior and features of the processor.

Implementation
The implementer configures and synthesizes the RTL to produce a hard macrocell. This task includes integrating RAMs into the design.

Integration
The integrator connects the macrocell into a SoC. This task includes connecting it to a memory system and peripherals.

Programming
It is the last task. The system programmer develops the software to configure and initialize the processor and tests the application software.

The operation of the final device depends on the following:

Build configuration
The implementer chooses the options that affect how the RTL source files are pre-processed. These options usually include or exclude logic that affects one or more of the area, maximum frequency, and features of the resulting macrocell.

Configuration inputs
The integrator configures some features of the processor by tying inputs to specific values. These configuration settings affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

Software configuration
The programmer configures the processor by programming particular values into registers. The configuration choices affect the behavior of the processor.
A1.7 Product revisions

This section describes the differences in functionality between product revisions.

- **r0p0**
  First release.

- **r0p1**
  There are no functional changes in this release.

- **r1p0**
  New CP15SDISABLE2 signal and new asymmetric floating-point/NEON feature.
Chapter A2

Technical Overview

This chapter describes the structure of the Cortex-A32 processor.

It contains the following sections:

• *A2.1 Components* on page A2-36.
• *A2.2 Interfaces* on page A2-40.
• *A2.3 About system control* on page A2-42.
• *A2.4 About the Generic Timer* on page A2-43.
• *A2.5 About the memory model* on page A2-44.
A2.1 Components

The Cortex-A32 processor consists of:

- One to four cores, each with its own governor block. The governor block provides functionality that remains required when the core is in retention.
- An SCU-L2 memory system block. The SCU maintains data coherency between the L1 data caches and the L2 cache. It also connects the cores to an external memory system using an AXI, ACE, or CHI master interface. A mini-SCU replaces the SCU in configurations that do not require the SCU functionality. The mini-SCU is instantiated in implementations that are configured with a single core, no L2 cache, no CPU cache protection, and an AXI master interface.

The processor also integrates CoreSight components, and optionally integrates cache protection and the Cryptographic Extension.

The following figure shows a top-level functional diagram of the Cortex-A32 processor.

Instruction Fetch Unit (IFU)

The IFU obtains instructions from the instruction cache or from external memory and predicts the outcome of branches in the instruction stream. It passes the instructions to the Data Processing Unit (DPU) for processing.
In implementations with CPU cache protection, parity bits protect the L1 Instruction cache data and tag RAMs by enabling the detection of any single-bit error. If an error is detected, the line is invalidated and fetched again.

**Data Processing Unit (DPU)**

The DPU decodes and executes instructions. It executes instructions that require data transfer to or from the memory system by interfacing to the Data Cache Unit (DCU). The DPU includes the Performance Monitor Unit (PMU), the Advanced SIMD and floating-point support, and the Cryptographic Extension.

**PMU**

The PMU provides six performance monitors that can be configured to gather statistics on the operation of each core and the memory system. The information can be used for debug and code profiling.

**Advanced SIMD and floating-point support**

Advanced SIMD is a media and signal processing architecture that adds instructions primarily for audio, video, 3-D graphics, image, and speech processing. The floating-point architecture provides support for single-precision and double-precision floating-point operations.

--- Note ---

The Advanced SIMD architecture, its associated implementations, and supporting software, are also referred to as NEON technology.

---

**Cryptographic Extension**

The optional Cortex-A32 processor Cryptographic Extension supports the Armv8 Cryptographic Extensions. It can be configured at implementation time and applies to all cores that implement Advanced SIMD and floating-point support. The Cryptographic Extension adds new instructions to Advanced SIMD that accelerate:

- Advanced Encryption Standard (AES) encryption and decryption.
- The Secure Hash Algorithm (SHA) functions SHA-1, SHA-224, and SHA-256.
- Finite field arithmetic used in algorithms such as Galois/Counter Mode and Elliptic Curve Cryptography.

**Memory Management Unit (MMU)**

The MMU provides fine-grained memory system control through a set of virtual-to-physical address mappings and memory attributes that are held in translation tables. These are loaded into the Translation Lookaside Buffer (TLB) when a location is accessed. The TLB entries include global and application specific identifiers to prevent context switch TLB flushes. They also include Virtual Machine Identifiers (VMIDs) to prevent TLB flushes on virtual machine switches by the hypervisor.

**Micro TLBs**

The first level of caching for the translation table information is a micro TLB of ten entries. It is implemented on each of the instruction and data sides. All main TLB related maintenance operations result in flushing both the instruction and data micro TLB.

**Main TLB**

A unified main TLB handles misses from the micro TLBs.

In implementations with CPU cache protection, parity bits protect the TLB RAMs by enabling the detection of any single-bit error. If an error is detected, the entry is flushed and fetched again.
L1 data-side memory system
The L1 data-side memory system includes the *Data Cache Unit* (DCU), the *Store Buffer* (STB), and the *Bus Interface Unit*.

**DCU**
The DCU manages all load and store operations.

In implementations with CPU cache protection, parity bits protect the L1 Data cache tag RAMs and dirty RAMs. The L1 Data cache data RAMs are protected using Error Correction Codes (ECC). The ECC scheme is Single Error Correct Double Error Detect (SECDED). The DCU includes a combined local and global exclusive monitor that is used by the Load-Exclusive/Store-Exclusive instructions.

**STB**
The STB holds store operations when they have left the load/store pipeline in the DCU and have been committed by the DPU. The STB can request access to the cache RAMs in the DCU, request the BIU to initiate linefills, or request the *Bus Interface Unit* (BIU) to write out the data on the external write channel. External data writes are through the SCU.

The STB is also used to queue maintenance operations before they are broadcast to other cores in the processor.

**BIU**
The BIU contains the SCU interface and buffers to decouple the interface from the L1 Data cache and STB. The BIU and the SCU always operate at the processor frequency.

**Governor**
The governor block, outside the core, includes all functions that must remain operating while a core is in retention mode.

**GIC CPU interface**
The GIC CPU interface is a memory-mapped interface through which a core receives an interrupt. The GIC Distributor can read and write the GIC CPU interface registers even while the core is in retention mode.

**Generic timer**
The Generic Timer has an interface to an external system counter. It provides a consistent view of time, which can be used to schedule events and trigger interrupts. It is also used by the retention circuits in the processor.

**L2 Memory System**
The L2 memory system contains the L2 cache pipeline and all the logic that maintains memory coherence between the cores in the cluster.

**SCU**
The SCU connects the cores to the external memory system through the master memory interface. It also maintains data cache coherency between the cores and arbitrates L2 requests from the cores.

**mini-SCU**
The mini-SCU replaces the SCU in certain uniprocessor configurations that do not require data cache coherency with other masters in the system. That is, implementations that are configured to have a single core, no L2 cache, no CPU cache protection, and an AXI interface. The mini-SCU bridges between the master interface of the core and the AXI master interface of the processor.
L2 cache

Each Cortex-A32 cluster can include an optional L2 cache that participates in the coherency protocol. Each L2 cache is 8-way set associative, supports 64-byte cache lines, and has a configurable cache RAM size between 128KB and 1MB.

ACP

The ACP interface cannot be configured without an L2 cache because it reuses buffering and data paths implemented for the L2 cache to achieve optimal efficiency. The main advantage of the ACP interface is its ability to allocate data in the L2 cache RAMs.

Debug and trace components

Cross-trigger

The Cross Trigger Matrix (CTM) combines the CoreSight Cross Trigger Interface (CTI) channel signals from all the cores so that a single cross trigger channel interface is presented in the Cortex-A32 processor. This module can combine up to four internal channel interfaces corresponding to each core along with one external channel interface.

Debug ROM

The Cortex-A32 processor has a debug ROM which is a CoreSight feature.

ETM

The ETM trace unit is a build-time configuration option. This module performs real-time instruction flow tracing that complies with the ETM architecture.

Related information
A2.2 Interfaces on page A2-40
A6.1 About the L1 memory system on page A6-86
A7.1 About the L2 memory system on page A7-92
Chapter A3 Clocks, Resets, and Input Synchronization on page A3-45
Chapter A4 Power Management on page A4-53
A2.2 Interfaces

The Cortex-A32 processor has several interfaces to connect it to a SoC.

![Diagram showing the interfaces of the Cortex-A32 processor]

**Table A2-1 Cortex-A32 interfaces**

<table>
<thead>
<tr>
<th>Purpose</th>
<th>Technology</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU events</td>
<td></td>
<td>Performance events provide useful information on the operation of the processor that you can use for debug and code profiling. A subset of available performance events is exported on the PMU event bus.</td>
</tr>
<tr>
<td>Trace</td>
<td>ATB</td>
<td>Optional Outputs trace information for debugging. The ATB interface is compatible with the CoreSight architecture.</td>
</tr>
<tr>
<td>Memory</td>
<td>AXI, ACE, or CHI</td>
<td>ACE can also be used with AXI peripherals.</td>
</tr>
<tr>
<td>ACP</td>
<td>AXI</td>
<td>Optional This slave interface reduces software cache maintenance operations when the cores share memory regions with other masters and allows other masters to allocate data into the L2 cache. It allows an external master to make coherent requests to shared memory, but it does not support cache maintenance, coherency, barrier, or DVM transactions.</td>
</tr>
<tr>
<td>Debug</td>
<td>APB</td>
<td>Allows access to debug registers and resources, for example, to set watchpoints and breakpoints.</td>
</tr>
<tr>
<td>Cross-trigger</td>
<td>CTI</td>
<td>This external interface is connected to the CoreSight CTI corresponding to each core through a simplified CTM.</td>
</tr>
<tr>
<td>Design for Test (DFT)</td>
<td></td>
<td>Allows an industry standard Automatic Test Pattern Generation (ATPG) tool to test logic.</td>
</tr>
<tr>
<td>Memory Built-In Self Test (MBIST)</td>
<td></td>
<td>Provides support for manufacturing test of the memories embedded in the Cortex-A32 processor.</td>
</tr>
<tr>
<td>Power management</td>
<td>Q-channel</td>
<td>Enables communication to an external power controller.</td>
</tr>
</tbody>
</table>

**Related information**

Chapter A9 ACE Master Interface on page A9-107
Chapter A10 CHI Master Interface on page A10-119
Chapter A8 AXI Master Interface on page A8-99
C1.2 Debug access on page C1-367
C2.1 About the PMU on page C2-376
C3.1 About the ETM on page C3-386
C4.1 About the cross-trigger on page C4-394

Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, and ACE and ACE-Lite
Arm® AMBA® 5 CHI Protocol Specification
Arm® CoreSight™ Architecture Specification
A2.3 About system control

The system registers control and provide status information for the functions that the processor implements.

The main functions of the system registers are:

• Overall system control and configuration.
• MMU configuration and management.
• Configuration and management of the L1 and the L2 caches.
• System performance monitoring.
• GIC configuration and management.

The system registers are accessible in the AArch32 Execution state. Some of the system registers are accessible through the memory-mapped or external debug interfaces. The CP15SDISABLE2 input disables write access to the following system registers:

• System Control Register (SCTLR).
• Translation Table Base Register 1 (TTBR1).
• Translation Table Base Control Register (TTBCR).
• Domain Access Control Register (DACR).
• Primary Region Remap Register (PRRR).
• Normal Memory Remap Register (NMRR).
• Memory Attribute Indirection Register 0 (MAIR0).
• Memory Attribute Indirection Register 1 (MAIR1).
• Vector Base Address Register (VBAR).
• Monitor Vector Base Address Register (MVBAR).
• Interrupt Controller Monitor System Register Enable (ICC_MSRE).
• Non-Secure Address Control Register (NSACR).
• Secure Debug Enable Register (SDER).
• Secure Debug Control Register (SDCR).

Related reference

B1.1 AArch32 register summary on page B1-144
A2.4 About the Generic Timer

The Generic Timer can schedule events and trigger interrupts that are based on an incrementing counter value. It generates timer events as active-LOW interrupt outputs and event streams.

The Cortex-A32 processor does not include the system counter. This resides in the SoC. The system counter value is distributed to the Cortex-A32 processor with a synchronous binary encoded 64-bit bus, CNTVALUEB[63:0].

Because CNTVALUEB[63:0] is generated from a system counter that typically operates at a slower frequency than the processor clock, CLKIN, the CNTCLKKEN input is provided. CNTCLKKEN is registered inside the processor and then used as a clock enable for CNTVALUEB[63:0]. This allows a multicycle path to be applied to the CNTVALUEB[63:0]. The following figure shows the interface.

![Generic Timer interface diagram](image)

Figure A2-3  Generic Timer interface

The value on CNTVALUEB[63:0] is required to be stable whenever the internally registered version of the CNTCLKKEN clock enable is asserted. CNTCLKKEN must be synchronous and balanced with respect to CLKIN and must toggle at integer ratios of the processor CLKIN.

Related information

A.6 Generic Timer signals on page Appx-A-625
A2.5 About the memory model

The processor views memory as a linear collection of bytes numbered in ascending order from zero. For example, bytes 0-3 hold the first stored word, and bytes 4-7 hold the second stored word.

The processor can store words in memory in big-endian or little-endian format. Instructions are always little-endian.

Related information

ARM® Architecture Reference Manual ARMv8, for ARMv8-A architecture profile
Chapter A3
Clocks, Resets, and Input Synchronization

This chapter describes the clocks of the Cortex-A32 processor. It also describes the reset options.

It contains the following sections:

• A3.1 Clocks on page A3-46.
• A3.2 Input synchronization on page A3-47.
• A3.3 Resets on page A3-48.
A3.1 Clocks

The Cortex-A32 processor has a single clock input, \texttt{CLKIN}. All cores in the Cortex-A32 processor and the SCU are clocked with a distributed version of \texttt{CLKIN}.

The Cortex-A32 processor has the following clock enable signals:

- \texttt{PCLKENDBG}.
- \texttt{ACLKENM}.
- \texttt{ACLKENS}.
- \texttt{SCLKEN}.
- \texttt{ATCLKEN}.
- \texttt{CNTCLKEN}.

For more information, see the \textit{Arm\textsuperscript{®} Cortex\textsuperscript{®}-A32 Processor Integration Manual}. 
A3.2 Input synchronization

The Cortex-A32 processor synchronizes certain input signals. The SoC can present these inputs asynchronously. All other external signals must be synchronous with reference to \( \text{CLKIN} \).

Input signals that the Cortex-A32 processor synchronizes:

- \( \text{nCORERESET} \).
- \( \text{nCPUPORESET} \).
- \( \text{nFIQ} \).
- \( \text{nIRQ} \).
- \( \text{nL2RESET} \).
- \( \text{nMBISTRESET} \).
- \( \text{nPRESETDBG} \).
- \( \text{nREI} \).
- \( \text{nSEI} \).
- \( \text{nVFIQ} \).
- \( \text{nVIRQ} \).
- \( \text{nVSEI} \).
- \( \text{CLREXMONREQ} \).
- \( \text{CPUQREQn} \).
- \( \text{CTICHOUTACK} \).
- \( \text{CTIIRQACK} \).
- \( \text{DBGEN} \).
- \( \text{EDBGRQ} \).
- \( \text{EVENTI} \).
- \( \text{L2FLUSHREQ} \).
- \( \text{L2QREQn} \).
- \( \text{NEONQREQn} \).
- \( \text{NIDEN} \).
- \( \text{SPIDEN} \).
- \( \text{SPNIDEN} \).

Input signals that the Cortex-A32 processor synchronizes under certain conditions:

- \( \text{CTICHIN} \).

The synchronized \( \text{CTICHIN} \) input signals are used only if the \( \text{CISBYPASS} \) input signal is deasserted LOW. If the \( \text{CISBYPASS} \) signal is asserted HIGH the \( \text{CTICHIN} \) synchronizers are not used, and the SoC must present the \( \text{CTICHIN} \) synchronously to \( \text{CLKIN} \).
A3.3 Resets

The Cortex-A32 processor has active-LOW reset input signals that can be asynchronously asserted HIGH to LOW, or deasserted LOW to HIGH.

\[ n_{CPUPORESET}[CN:0] \]

Where \( CN \) is the number of cores minus one.

Power On reset signals. These primary, cold reset signals initialize all resettable registers in the corresponding core, including debug registers and ETM registers.

\[ n_{CORERESET}[CN:0] \]

These primary reset signals initialize all resettable registers in the corresponding core, not including debug registers and ETM registers.

\[ n_{PRESETDBG} \]

This single, processor-wide signal resets the integrated CoreSight components that connect to the external PCLK domain, such as debug logic.

\[ n_{L2RESET} \]

This single, processor-wide signal resets all resettable registers in the L2 memory system and the logic in the SCU or mini-SCU.

\[ n_{MBISTRESET} \]

An external MBIST controller can use this signal to reset the entire SoC. The \( n_{MBISTRESET} \) signal resets all resettable registers in the cluster, for entry into, and exit from, MBIST mode.

Reset synchronization logic inside the processor ensures that reset deassertion is synchronous for all resettable registers. The processor clock is not required for reset assertion, but it must be present for reset deassertion to ensure reset synchronization.

In general, the reset time only requires three processor clock cycles.

\[ \text{Note} \]

The application of a retention state can affect how long reset assertion is required. You must hold the reset signal active-LOW until the power returns and the unit or processor is ready for the reset to take effect if:

- The Advanced SIMD and floating-point unit of a core undergoing a reset is in retention state.
- A core that is being reset is in retention state.

The time that is taken for retention exit and the behavior of the power controller varies by partner and by implementation.

The following table describes the valid reset signal combinations. All other combinations of reset signals are illegal. In the table, \( n \) designates the core that is reset.
<table>
<thead>
<tr>
<th>Reset combination</th>
<th>Signals</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cluster cold reset</td>
<td>nCPUPORESET[CN:0]</td>
<td>all = 0</td>
<td>All logic is held in reset.</td>
</tr>
<tr>
<td></td>
<td>nCORERESET[CN:0]</td>
<td>all = X</td>
<td>nCORERESET can be asserted, but is not required.</td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Cluster cold reset with debug active</td>
<td>nCPUPORESET[CN:0]</td>
<td>all = 0</td>
<td>All cores are held in reset so they can be powered up. The L2 is held in</td>
</tr>
<tr>
<td></td>
<td>nCORERESET[CN:0]</td>
<td>all = X</td>
<td>reset, but must remain powered up. This enables external debug over power</td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>1</td>
<td>down for the cluster.</td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>0</td>
<td>nCORERESET can be asserted, but is not required.</td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Individual core cold reset with debug</td>
<td>nCPUPORESET[CN:0]</td>
<td>[n] = 0</td>
<td>Individual core is held in reset, so that the core can be powered up.</td>
</tr>
<tr>
<td>active</td>
<td>nCORERESET[CN:0]</td>
<td>[n] = X</td>
<td>This enables external debug over power down for the core that is held in</td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>1</td>
<td>reset.</td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>1</td>
<td>nCORERESET can be asserted, but is not required.</td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Individual core warm reset with trace</td>
<td>nCPUPORESET[CN:0]</td>
<td>[n] = 1</td>
<td>Individual core is held in reset.</td>
</tr>
<tr>
<td>and debug active</td>
<td>nCORERESET[CN:0]</td>
<td>[n] = 0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Debug logic reset</td>
<td>nCPUPORESET[CN:0]</td>
<td>all = 1</td>
<td>Cluster debug logic is held in reset.</td>
</tr>
<tr>
<td></td>
<td>nCORERESET[CN:0]</td>
<td>all = 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Reset combination</td>
<td>Signals</td>
<td>Value</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------</td>
<td>--------------------------------</td>
<td>-------</td>
<td>------------------------------</td>
</tr>
<tr>
<td>MBIST reset</td>
<td>nCPUPORESET[CN:0]</td>
<td>all = 1</td>
<td>All logic is held in reset.</td>
</tr>
<tr>
<td></td>
<td>nCORERESET[CN:0]</td>
<td>all = 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>Normal state</td>
<td>nCPUPORESET[CN:0]</td>
<td>all = 1</td>
<td>No logic is held in reset.</td>
</tr>
<tr>
<td></td>
<td>nCORERESET[CN:0]</td>
<td>all = 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nPRESETDBG</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nL2RESET</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>nMBISTRESET</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

**Warm reset**

The following figure shows the Warm reset sequence for the Cortex-A32 processor.

![Warm reset timing](image)

**Figure A3-1 Warm reset timing**

Individual core Warm reset initializes all logic in a single core apart from its Debug, ETM, breakpoint, and watchpoint logic. Breakpoints and watchpoints for that core are retained. You must apply the correct sequence before applying Warm reset to that core.

For individual processor Warm reset:
- You must apply steps 1 to 6 in the core powerdown sequence, see A4.6 Powering down an individual core on page A4-61, and wait until STANDBYWF1 is asserted, indicating that the core is idle, before asserting nCORERESET for that core.
- nCORERESET for that core must assert for at least 3 CLK cycles.
- nL2RESET must not assert while any individual core is active.
- nPRESETDBG must not assert while any individual core is actively being debugged in normal operating mode.

**Note**

If core dynamic retention using the CPU Q-channel interface is used, the core must be in quiescent state with STANDBYWF1 asserted and CPUQREQn, CPUQACCEPTn, and CPUQACCEPT must be LOW before nCORERESET is applied.
WARMRSTREQ and DBGRSTREQ

When the Reset Request bit in the RMR register is set to 1, the processor asserts the WARMRSTREQ signal and the SoC reset controller can use this request to trigger a Warm reset of the core. An external debugger might also request a Warm reset of the core by asserting DBGRSTREQ.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for information about the recommended code sequence to use, to request a Warm reset.

You must apply steps 1 on page A4-61 to 6 on page A4-61 in the core powerdown sequence in *A4.6 Powering down an individual core on page A4-61*, and wait until STANDBYWFI asserts indicating the processor is idle, before asserting nCORERESET for that core. nCORERESET must satisfy the timing requirements described in the Warm reset section.
Chapter A4
Power Management

This chapter describes the power domains and the power modes in the Cortex-A32 processor.

It contains the following sections:

- A4.1 Power domains on page A4-54.
- A4.2 Power modes on page A4-57.
- A4.3 Core Wait for Interrupt on page A4-58.
- A4.4 Core Wait for Event on page A4-59.
- A4.5 L2 Wait for Interrupt on page A4-60.
- A4.6 Powering down an individual core on page A4-61.
- A4.7 Powering up an individual core on page A4-62.
- A4.8 Powering down the processor without system driven L2 flush on page A4-63.
- A4.9 Powering up the processor without system driven L2 flush on page A4-64.
- A4.10 Powering down the processor with system driven L2 flush on page A4-65.
- A4.11 Powering up the processor with system driven L2 flush on page A4-66.
- A4.13 Exiting Dormant mode on page A4-68.
- A4.14 Event communication using WFE or SEV on page A4-69.
- A4.15 Communication to the Power Management Controller on page A4-70.
- A4.16 STANDBYWF[3:0] and STANDBYWFIL2 signals on page A4-71.
- A4.17 Q-channel on page A4-72.
A4.1 Power domains

A core or a processor can support different power domains. Each power domain has valid and accepted power states.

The Cortex-A32 processor provides mechanisms and support to control both dynamic and static power dissipation. The individual cores in the Cortex-A32 processor support four main levels of power management which correspond to the power domains shown in the following table:

<table>
<thead>
<tr>
<th>Power domain</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDMINERV A</td>
<td>Includes the SCU, the optional L2 cache control logic, and debug registers that are described as being in the debug domain.</td>
</tr>
<tr>
<td>PDL2</td>
<td>Includes the L2 data RAM, L2 tag RAM, L2 victim RAM, and the SCU duplicate tag RAM.</td>
</tr>
<tr>
<td>PDCPU&lt;n&gt;</td>
<td>Includes the optional Advanced SIMD and floating-point support, the L1 cache and TLB RAMs, and the debug registers that are described as being in the processor domain. n is 0, 1, 2, or 3. It represents core 0, core 1, core 2, or core 3. If a core is not present, the corresponding power domain is not present.</td>
</tr>
<tr>
<td>PDCPUADVSIMD&lt;n&gt;</td>
<td>Represents the Advanced SIMD and floating-point block of core n. n is 0, 1, 2, or 3. It represents core 0, core 1, core 2, or core 3. If a core is not present, the corresponding power domain is not present.</td>
</tr>
</tbody>
</table>

The separate PDMINERV A and PDL2 power domains can remain active even when all the cores are powered down. It means that the processor can continue to accept snoops from external devices to access the L2 cache.

The following figure shows an example of the domains embedded in a System-on-Chip (SoC) power domain.
Figure A4-1  Power domains

The power domains can be controlled independently to give different combinations of powered-up and powered-down domains. However, only some powered-up and powered-down domain combinations are valid and supported.

Table A4-2  Power state description

<table>
<thead>
<tr>
<th>Power state</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>Block is power gated</td>
</tr>
<tr>
<td>Ret</td>
<td>Logic or RAM retention power only</td>
</tr>
<tr>
<td>On</td>
<td>Block is active</td>
</tr>
</tbody>
</table>

The following tables show the supported power domain states for the processor.

--- Caution ---

States that are not shown in the tables are unsupported and must not occur.

Table A4-3  Supported processor power states

<table>
<thead>
<tr>
<th>Power domains</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDMINERVA</td>
<td></td>
</tr>
<tr>
<td>PDL2</td>
<td></td>
</tr>
<tr>
<td>PDCPU&lt;n&gt;</td>
<td></td>
</tr>
<tr>
<td>Off</td>
<td>Off</td>
</tr>
<tr>
<td></td>
<td>Off</td>
</tr>
<tr>
<td></td>
<td>Processor off.</td>
</tr>
<tr>
<td>Off</td>
<td>On/Ret</td>
</tr>
<tr>
<td></td>
<td>Off</td>
</tr>
<tr>
<td></td>
<td>L2 cache dormant mode.</td>
</tr>
</tbody>
</table>
### Table A4-3  Supported processor power states (continued)

<table>
<thead>
<tr>
<th>Power domains</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDMINERVA</td>
<td></td>
</tr>
<tr>
<td>PDL2</td>
<td></td>
</tr>
<tr>
<td>PDCPU&lt;n&gt;</td>
<td></td>
</tr>
<tr>
<td>On</td>
<td>See Table A4-4  Supported core power states on page A4-56</td>
</tr>
<tr>
<td>Ret</td>
<td>Processor on, L2 RAMs retained. All cores either off or in WFX. This is an L2 RAM retention entry or residency condition.</td>
</tr>
<tr>
<td>On</td>
<td>See Table A4-4  Supported core power states on page A4-56</td>
</tr>
<tr>
<td>Ret</td>
<td>Processor on, L2 RAMs retained. At least one core running. This is a transient condition.</td>
</tr>
<tr>
<td>On</td>
<td>See Table A4-4  Supported core power states on page A4-56</td>
</tr>
<tr>
<td>On</td>
<td>Processor on, SCU/L2 RAMs active.</td>
</tr>
</tbody>
</table>

The following table describes the supported power domain states for individual cores. The power domain state in each core is independent of all other cores.

### Table A4-4  Supported core power states

<table>
<thead>
<tr>
<th>Power domains</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PDCPU</td>
<td></td>
</tr>
<tr>
<td>PDADVSIMD</td>
<td></td>
</tr>
<tr>
<td>Off</td>
<td>Core off.</td>
</tr>
<tr>
<td>On</td>
<td>Core on. Advanced SIMD and floating-point on.</td>
</tr>
<tr>
<td>Ret Ret</td>
<td>Core retention. Core logic and Advanced SIMD and floating-point in retention.</td>
</tr>
</tbody>
</table>

You must follow the dynamic power management and powerup and powerdown sequences described in the following sections. Any deviation from these sequences can lead to unpredictable results.
A4.2 Power modes

The processor supports the following power modes:

Normal mode
This is the normal mode of operation in which all of the processor functionality is available. The Cortex-A32 processor uses gated clocks to disable inputs to unused functional blocks. Only the logic used to perform an operation consumes any dynamic power.

Standby mode
When a Cortex-A32 core is in standby mode, it is architecturally clock gated at the top of the clock tree. Each core in the cluster can be put in standby mode separately from the other cores, by executing a *Wait for Interrupt* (WFI) or *Wait for Event* (WFE) instruction.

L2 standby mode
When all the cores are in standby mode and the L2 memory system is idle.

Individual core shutdown mode
The PDCPU power domain for an individual core is shut down and the state held in this domain is lost.

Cluster shutdown mode
The PDMINERVA, PDL2, and all PDCPU power domains are shut down and the state held in these domains is lost.

Dormant mode (optional)
All the cores and L2 control logic are powered down while the L2 cache RAMs are powered up and retain state. The RAM blocks that remain powered up during Dormant mode are:

- L2 tag RAMs.
- L2 data RAMs.
- L2 victim RAM.

Retention mode
Contact Arm for information about retention state.
A4.3 Core Wait for Interrupt

Programmers can use the *Wait for Interrupt* (WFI) instruction to cause the core to enter a low-power state.

Wait for Interrupt is a feature of the Armv8-A architecture that puts the core in a low-power state by disabling most of the clocks in the core while keeping the core powered up. Apart from a small dynamic power overhead on the logic to enable the core to wake up from WFI low-power state, this reduces the power drawn to static leakage current only.

When executing the WFI instruction, the core waits for all instructions in the core to retire before entering the idle or low power state. The WFI instruction ensures that all explicit memory accesses that occurred before the WFI instruction in program order have retired. For example, the WFI instruction ensures that the following instructions received the required data or responses from the L2 memory system:

- Load instructions.
- Cache and TLB maintenance operations.
- Store exclusive instructions.

In addition, the WFI instruction ensures that store instructions have updated the cache or have been issued to the SCU.

While the core is in WFI low-power state, the clocks in the core are temporarily enabled without causing the core to exit WFI low-power state, when any of the following events are detected:

- A snoop request that must be serviced by the core L1 Data cache.
- A cache or TLB maintenance operation that must be serviced by the core L1 Instruction cache, data cache, or TLB.
- An APB access to the debug or trace registers residing in the core power domain.

Exit from WFI low-power state occurs when the core detects a reset or one of the WFI wake up events as described in the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile*.

On entry into WFI low-power state, STANDBYWFI for that core is asserted. Assertion of STANDBYWFI guarantees that the core is in idle and low-power state. STANDBYWFI continues to assert even if the clocks in the core are temporarily enabled because of an L2 snoop request, cache or TLB maintenance operation, or an APB access.

STANDBYWFI does not indicate completion of L2 memory system transactions initiated by the processor. All Cortex-A32 processor implementations contain an L2 memory system. This includes implementations without an L2 cache.
A4.4 Core Wait for Event

A core can use the *Wait for Event* (WFE) instruction to cause the core to enter a low-power state.

*Wait for Event* (WFE) is a feature of the Armv8-A architecture. It can be used by a locking mechanism based on events to put the core in a low-power state by disabling most of the clocks in the core while keeping the core powered-up. Apart from a small dynamic power overhead on the logic to enable the core to wake up from WFE low-power state, this reduces the power drawn to static leakage current only.

When executing the WFE instruction, the core waits for all instructions in the core to complete before entering the idle or low-power state.

If the event register is set, execution of a WFE instruction does not cause entry into standby state, but clears the event register.

While the core is in WFE low-power state, the clocks in the core are temporarily enabled without causing the core to exit WFE low-power state, when any of the following events are detected:

- An L2 snoop request that must be serviced by the core L1 Data cache.
- A cache or TLB maintenance operation that must be serviced by the core L1 Instruction cache, data cache, or TLB.
- An APB access to the debug or trace registers residing in the core power domain.

Exit from WFE low-power state occurs when the core detects a reset, the assertion of the EVENTI input signal, or one of the WFE wake-up events as described in the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile*.

On entry into WFE low-power state, STANDBYWFE for that core is asserted. Assertion of STANDBYWFE guarantees that the core is in idle and low-power state. STANDBYWFE continues to assert even if the clocks in the core are temporarily enabled because of an L2 snoop request, cache or TLB maintenance operation, or an APB access.

**CLREXMON request and acknowledge signaling**

When the CLREXMONREQ input is asserted, it signals the clearing of an external global exclusive monitor and acts as a WFE wake-up event to all the cores in the cluster.

The CLREXMONREQ signal has a corresponding CLREXMONACK response signal. This forms a standard 2-wire, 4-phase handshake that can be used to signal across the voltage and frequency boundary between the core and system.

The following figure shows the CLREXMON request and acknowledge handshake. When the request signal is asserted, it continues to assert until an acknowledge is received. When the request is deasserted, the acknowledge can then deassert.

Figure A4-2 CLREXMON request and acknowledge handshake
A4.5 L2 Wait for Interrupt

When all the cores are in WFI low-power state, the shared L2 memory system logic that is common to all the cores can also enter a WFI low-power state.

Entry into L2 WFI low-power state can occur only if specific requirements are met and the following sequence applied:

- All cores are in WFI low-power state and therefore, the STANDBYWFI output for each core is asserted. Assertion of all the cores STANDBYWFI outputs guarantees that all the cores are in idle and low-power state. All clocks in the cores, with the exception of a small amount of clock wakeup logic, are disabled.
- If configured with ACE, the SoC asserts the input pin ACINACTM to idle the AXI master interface. It indicates that no snoop requests will be made from the external memory system.
- If configured with a CHI interface, the SoC asserts the input pin SINACT to idle the CHI master interface. It indicates that no snoop requests will be made from the external memory system.
- If configured with an ACP interface, the SoC asserts the AINACTS input pin to idle the ACP interface. It indicates that the SoC sends no more transactions on the ACP interface.

When the L2 memory system completes the outstanding transactions for AXI, ACE, or CHI interfaces, it can then enter the L2 WFI low-power state. On entry into L2 WFI low-power state, STANDBYWFIL2 is asserted. Assertion of STANDBYWFIL2 guarantees that the L2 memory system is idle and does not accept new transactions.

Exit from L2 WFI low-power state occurs on one of the following events:

- A physical IRQ or FIQ interrupt.
- A debug event.
- Powerup or warm reset.

When a core exits permanently from WFI low-power state, STANDBYWFI for that core is deasserted. When the L2 memory system logic exits from WFI low-power state, STANDBYWFIL2 is deasserted. The SoC must continue to assert ACINACTM or SINACT until STANDBYWFIL2 has deasserted.

The following figure shows the L2 WFI timing for a 4-core configuration.

![Figure A4-3 L2 Wait For Interrupt timing](image-url)
A4.6 Powering down an individual core

To enable a core to be powered down, the implementation must place the core on a separately controlled power supply. In addition, you must clamp the outputs of the core to benign values while the entire cluster is powered down.

To power down the core, apply the following sequence:

**Procedure**

1. Disable the data cache, by clearing the SCTLR.C bit, or the HSCTLR.C bit if in Hyp mode. This prevents more data cache allocations and causes cacheable memory attributes to change to Normal Non-cacheable. Subsequent loads and stores do not access the L1 or L2 caches.

2. Clean and invalidate all data from the L1 Data cache. The SCU duplicate tag RAMs for this core are now empty. This prevents any new data cache snoops or data cache maintenance operations from other cores in the cluster being issued to this core.

3. Disable data coherency with other cores in the cluster, by clearing the CPUECTLR.SMPEN bit. Clearing the SMPEN bit enables the core to be taken out of coherency by preventing the core from receiving cache or TLB maintenance operations broadcast by other cores in the cluster.

4. Execute an ISB instruction to ensure that all of the register changes from the previous steps have been committed.

5. Execute a DSB SY instruction to ensure that all cache, TLB, and branch predictor maintenance operations issued by any core in the cluster device before the SMPEN bit was cleared have completed.

6. Execute a WFI instruction and wait until the STANDBYWFI output is asserted to indicate that the core is in idle and low-power state.

7. Deassert DBGPWRDUP LOW. This prevents any external debug access to the core.

8. Activate the core output clamps.

9. Assert nCPUPORESET LOW.

10. Remove power from the PDCPU power domain.
A4.7 Powering up an individual core

To power up an individual core, apply the following sequence:

1. Assert `nCPUPORESET` LOW. Ensure `DBGPWRDUP` is held LOW to prevent any external debug access to the core.
2. Apply power to the PDCPU power domain. Keep the state of the signals `nCPUPORESET` and `DBGPWRDUP` LOW.
3. Release the core output clamps.
4. Deassert resets.
5. Set the CPUECTL.R.SMPEN bit to 1 to enable snooping into the core.
6. Assert `DBGPWRDUP` HIGH to allow external debug access to the core.
7. If required, use software to restore the state of the core as it was before powerdown.
A4.8 Powering down the processor without system driven L2 flush

When powering down the processor, the PDMINERVA, PDL2, and PDCPU power domains are shut down and all state is lost. In this section, the lead core is defined as the last core to switch off.

To power down the processor, apply the following sequence. For device powerdown, all operations on a lead core must occur after the equivalent step on all non-lead cores.

**Procedure**

1. Ensure all non-lead cores are in shutdown mode, see *A4.6 Powering down an individual core* on page A4-61.
2. Follow steps 1 on page A4-61 and 2 on page A4-61 in *A4.6 Powering down an individual core* on page A4-61.
3. If the ACP interface is configured, ensure that any master connected to the interface does not send new transactions, then assert **AINACTS**.
4. Clean and invalidate all data from the L2 Data cache.
5. Follow steps 3 on page A4-61 to 10 on page A4-61 in *A4.6 Powering down an individual core* on page A4-61.
6. In an ACE configuration, assert **ACINACTM** or, in a CHI configuration, assert **SINACT**. Then, wait until the **STANDBYWFIL2** output is asserted to indicate that the L2 memory system is idle. All Cortex-A32 processor implementations contain an L2 memory system, including implementations without an L2 cache. This applies to implementations that use the mini-SCU and implementations that use the SCU.
7. Activate the cluster output clamps.
8. Remove power from the PDMINERVA and PDL2 power domains.
A4.9 **Powering up the processor without system driven L2 flush**

When powering down the processor, the PDMINERVA, PDL2, and PDCPU power domains are shut down and all state is lost.

To power up the processor, apply the following sequence:

**Procedure**

1. For each core in the cluster, assert nCPUPORESET LOW.
2. Assert nL2RESET LOW and hold L2RSTDISABLE LOW.
3. Apply power to the PDMINERVA and PDL2 domains while keeping the signals described in steps 1 on page A4-64 and 2 on page A4-64 LOW.
4. Release the cluster output clamps.
5. Continue a normal cold reset sequence.
Powering down the processor with system driven L2 flush

When powering down the processor, the PDMINERVA, PDL2, and PDCPU power domains are shut down and all state is lost.

To power down the cluster, apply the following sequence:

Procedure

1. Ensure all cores are in shutdown mode, see A4.6 Powering down an individual core on page A4-61.
2. If the ACP interface is configured, ensure that any master connected to the interface does not send new transactions, then assert AINACTS. This is necessary to prevent ACP transactions from allocating new entries in the L2 cache while the hardware cache flush is occurring.
3. Assert L2FLUSHREQ HIGH.
4. Hold L2FLUSHREQ HIGH until L2FLUSHDONE is asserted.
5. Deassert L2FLUSHREQ.
6. In an ACE configuration, assert ACINACTM or, in a CHI configuration, assert SINACT. Then, wait until the STANDBYWFIL2 output is asserted to indicate that the L2 memory system is idle. All Cortex-A32 processor implementations contain an L2 memory system, including implementations without an L2 cache. This applies to implementations that use the mini-SCU and implementations that use the SCU.
7. Activate the cluster output clamps.
8. Remove power from the PDMINERVA and PDL2 power domains.
A4.11 Powering up the processor with system driven L2 flush

To power up the processor, apply the following sequence:

**Procedure**

1. For each core in the cluster, assert \( n_{\text{CPUPORESET}} \) LOW.
2. Assert \( n_{\text{L2RESET}} \) LOW and hold \( L_{\text{2RSTDISABLE}} \) LOW.
3. Apply power to the PDMINERVA and PDL2 domains while keeping the signals described in steps 1 on page A4-66 and 2 on page A4-66 LOW.
4. Release the cluster output clamps.
5. Continue a normal cold reset sequence.
A4.12 Entering Dormant mode

The processor can enter Dormant mode if certain requirements are met.

To support Dormant mode, you must ensure:

- That the L2 cache RAMs are in a separate power domain.
- That all inputs to the L2 cache RAMs are clamped to benign values. This avoids corrupting data when the cores and L2 control power domains enter and exit power down state.

Before entering Dormant mode, the architectural state of the cluster, excluding the contents of the L2 cache RAMs that remain powered up, must be saved to external memory.

To enter Dormant mode, apply the following sequence:

**Procedure**

1. Disable the data cache by clearing the SCTLR.C bit, or the HSCTLR.C bit if in Hyp mode. This prevents more data cache allocations and causes cacheable memory attributes to change to Normal Non-cacheable. Subsequent loads and stores do not access the L1 or L2 caches.

2. Clean and invalidate all data from the L1 Data cache. The SCU duplicate tag RAM for this core is now empty. This prevents any new data cache snoops or data cache maintenance operations from other cores in the cluster being issued to this core.

3. Disable data coherency with other cores in the cluster, by clearing the CPUECTLR.SMPEN bit. Clearing the SMPEN bit enables the core to be taken out of coherency by preventing the core from receiving cache or TLB maintenance operations broadcast by other cores in the cluster.

4. Save architectural state, if required. These state saving operations must ensure that the following occur:
   - All Arm registers, including the CPSR and SPSR, are saved.
   - All system registers are saved.
   - All debug related state is saved.

5. Execute an ISB instruction to ensure that all of the register changes from the previous steps have been committed.

6. Execute a DSB instruction to ensure that all cache, TLB, and branch predictor maintenance operations issued by any core in the cluster before the SMPEN bit was cleared have completed. In addition, this ensures that all state saving has completed.

7. Execute a WFI instruction and wait until the STANDBYWFI output is asserted, to indicate that the core is in idle and low-power state.

8. Repeat the previous steps for all cores, and wait for all STANDBYWFI outputs to be asserted.

9. If the ACP interface is configured, ensure that any master connected to the interface does not send new transactions, then assert AINACTS.

10. If ACE is implemented, the SoC asserts the input pin ACINACTM to idle the AXI master interface after all snoop transactions have been sent on the interface. If CHI is implemented, the SoC asserts the input pin SINACT.

   When the L2 has completed the outstanding transactions for the AXI master and slave interfaces, STANDBYWFL2 is asserted to indicate that L2 memory system is idle. All Cortex-A32 processor implementations contain an L2 memory system, including implementations without an L2 cache.

11. When STANDBYWFI and STANDBYWFL2 are asserted for all cores, the cluster is ready to enter Dormant mode. This applies to implementations that use the mini-SCU as well as implementations that use the SCU.

12. Activate the L2 cache RAM input clamps.

13. Remove power from the PDCPU and PDMINERVA power domains.
A4.13 Exiting Dormant mode

As part of the exit from Dormant mode to Normal state, the SoC must perform a cold reset sequence. The SoC must assert the reset signals until power is restored. After power is restored, the cluster exits the cold reset sequence, and the architectural state must be restored.

To exit Dormant mode, apply the following sequence:

1. Apply a normal cold reset sequence. You must apply resets to the cores and the L2 memory system logic until power is restored. During this reset sequence, \textbf{L2RSTDISABLE} must be held HIGH to disable the L2 cache hardware reset mechanism.
2. When power has been restored, release the L2 cache RAM input clamps.
3. Continue a normal cold reset sequence with \textbf{L2RSTDISABLE} held HIGH.
4. The architectural state must be restored, if required.
A4.14 Event communication using WFE or SEV

An external agent can use the EVENTI pin to participate in a WFE or SEV event communication with the Cortex-A32 processor.

When this pin is asserted, it sends an event message to all the cores in the device. This is similar to executing a SEV instruction on one core in the cluster. This enables the external agent to signal to the cores that it has released a semaphore and that the cores can leave the WFE low-power state. The EVENTI input pin must remain HIGH for at least one CLKIN clock cycle to be visible by the cores.

The external agent can determine that at least one of the cores in the cluster has executed an SEV instruction by checking the EVENTO pin. When SEV is executed by any of the cores in the cluster, an event is signaled to all the cores in the device, and the EVENTO pin is asserted. This pin is asserted HIGH for three CLKIN clock cycles when any core in the cluster executes an SEV instruction.
A4.15  Communication to the Power Management Controller

Communication between the Cortex-A32 processor and the system power management controller can be performed using one or both of the:

- *A4.16 STANDBYWF[3:0] and STANDBYWFIL2 signals* on page A4-71.
- *A4.17 Q-channel* on page A4-72.
A4.16 STANDBYWFI[3:0] and STANDBYWFIL2 signals

The STANDBYWFI[n] signal indicates when an individual core is in idle and low-power state. The power management controller can remove power from an individual core when STANDBYWFI[n] is asserted.

The STANDBYWFIL2 signal indicates when all individual cores and the L2 memory system are in idle and low-power state. A power management controller can remove power from the Cortex-A32 processor when STANDBYWFIL2 is asserted. See A4.8 Powering down the processor without system driven L2 flush on page A4-63 and A4.10 Powering down the processor with system driven L2 flush on page A4-65 for more information.

The Cortex-A32 processor includes a minimal L2 memory system in configurations without an L2 cache. Therefore, the power management controller must always wait for assertion of STANDBYWFIL2 before removing power from the Cortex-A32 processor. This applies to configurations that use the mini-SCU and configurations that use the SCU.

The following figure shows how STANDBYWFI[3:0] and STANDBYWFIL2 correspond to individual cores and the Cortex-A32 processor.

Figure A4-4 STANDBYWFI[3:0] and STANDBYWFIL2 signals
A4.17 Q-channel

Q-channel enables:

- The controller to manage entry to, and exit from, a device quiescent state. Quiescence management is typically of, but not restricted to, clock gated, and power gated retention states, of the device or device partitions.
- The capability to indicate a requirement for exit from the quiescent state. The associated signaling can contain contributions from other devices in the same power domain.
- Optional device capability to deny a quiescence request.
- Safe asynchronous interfacing across clock domains.

For more information, see the *Low Power Interface Specification: Arm Q-Channel and P-Channel Interfaces*. 
Chapter A5
Cache Behavior and Cache Protection

This chapter describes the CPU and SCU cache protection features of the Cortex-A32 processor.

It contains the following sections:

- A5.1 Cached memory types on page A5-74.
- A5.2 Coherency between data caches with the MOESI protocol on page A5-75.
- A5.3 Cache misses, unexpected cache hits, and speculative fetches on page A5-76.
- A5.4 Disabling a cache on page A5-77.
- A5.5 Invalidating or cleaning a cache on page A5-78.
- A5.6 About read allocate mode on page A5-79.
- A5.7 About cache protection on page A5-80.
- A5.8 Error reporting on page A5-82.
- A5.9 Error injection on page A5-83.
A5.1 Cached memory types

The processor can cache data and instructions that meet certain memory attribute criteria.

L1 instruction cache
When the L1 instruction cache is enabled, it caches the following memory types:
• Normal, Inner Write-Back.
• Normal, Inner Write-Through.

L1 data cache
When the L1 data cache is enabled, it can cache the following memory types:
• Normal, Inner Write-Back, Outer Write-Back.

Data might not be allocated if:
• The data is for a non-temporal load.
• The transient hint is set.
• The no-allocate hint is set.
• The processor is in read allocate mode.

L2 cache
If the L2 cache is present and enabled, it can cache the following memory types:
• Normal, Inner Write-Back, Outer Write-Back.

Instruction cache lines are allocated into the L2 cache when they are fetched from the external memory system.

Data cache lines are allocated into the L2 cache when they are evicted from an L1 data cache.

Related information
B1.42 CPU Auxiliary Control Register on page B1-202
A5.2 Coherency between data caches with the MOESI protocol

The processor uses the MOESI protocol to maintain data cache coherency between multiple cores. The DCU stores the MOESI state of the cache line in the tag and dirty RAMs.

MOESI describes the state in which a shareable line can be in an L1 data cache.

Table A5-1  MOESI and AMBA mapping

<table>
<thead>
<tr>
<th>MOESI</th>
<th>AMBA</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Modified</td>
<td>UniqueDirty</td>
<td>The line is in only this cache and is dirty.</td>
</tr>
<tr>
<td>Owned</td>
<td>SharedDirty</td>
<td>The line is possibly in more than one cache and is dirty.</td>
</tr>
<tr>
<td>Exclusive</td>
<td>UniqueClean</td>
<td>The line is in only this cache and is clean.</td>
</tr>
<tr>
<td>Shared</td>
<td>SharedClean</td>
<td>The line is possibly in more than one cache and is clean.</td>
</tr>
<tr>
<td>Invalid</td>
<td>Invalid</td>
<td>The line is not in this cache.</td>
</tr>
</tbody>
</table>

Data coherency is enabled only when the CPUECTRL.SMPEN bit is set. You must set the SMPEN bit before enabling the data cache. If you do not, then the cache is not coherent with other cores and data corruption could occur.

Related information
A5.6 About read allocate mode on page A5-79
B1.43 CPU Extended Control Register on page B1-206
C5.3 Encoding for tag and data in the L1 data cache on page C5-400
A5.3 **Cache misses, unexpected cache hits, and speculative fetches**

The L1 and L2 caches handle problematic cache accesses in predefined ways.

**Cache miss**
On a cache miss, the processor performs Critical Word First filling of the cache.

**Unexpected cache hits**
If the cache reports a hit on a memory location that is marked as Non-Cacheable or Device, this is called an unexpected cache hit. In this architecturally **UNPREDICTABLE** case, the cache might return incorrect data because of the following configurations or settings:
- Improper translation table configuration because the caches are physically addressed.
- The cache is disabled.

Non-Cacheable or Device accesses do not use the result of a cache lookup and therefore ignore any unexpected cache hit.

**Speculative fetches**
Because there can be several unresolved branches in the pipeline, there is no guarantee that the processor executes an instruction. Instruction fetches are therefore speculative. A branch or exceptional instruction in the code stream can cause a pipeline flush and discard the fetched instructions. Because of the prefetching behavior, you must not place read-sensitive devices in the same page as code. Pages with Device memory type attributes are treated as Non-Cacheable Normal Memory when accessed by instruction fetches. You must use the XN (Execute Never) bit in the page table descriptor for a memory region to stop speculative instructions fetches when such memory region contains read-sensitive devices. To avoid speculative fetches to read-sensitive devices when address translation is disabled, these devices must be separated from code in the physical memory map.

**Related information**
*Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile*
A5.4 Disabling a cache

When the instruction cache is disabled:

- Instruction fetches do not access the L1 instruction cache or the L2 unified cache.
- Instruction cache maintenance operations execute normally.
- All instruction fetches to cacheable memory are treated as if they were non-cacheable. This means that instruction fetches might not be coherent with caches in other cores and software must take account of this.

When the data cache is disabled:

- Load and store instructions do not access the L1 data cache or L2 unified cache.
- Instruction fetches do not access the L2 unified cache.
- Data cache maintenance operations to the L1 data cache and the L2 unified cache execute normally.
- All load and store instructions to cacheable memory are treated as if they were non-cacheable. This means that they are not coherent with the caches in this core or the caches in other cores and software must take account of this.

You cannot disable the L1 data cache and the L2 unified cache independently because the same enable bit controls both of them.

If the instruction cache is enabled and the data cache is disabled, then instruction fetches to cacheable memory continue to access the L1 instruction cache but they do not access the L2 unified cache.

Related information

B1.105 System Control Register on page B1-324
A5.5 Invalidating or cleaning a cache

The processor automatically invalidates caches on reset unless suppressed with the DBGL1RSTDISABLE or L2RSTDISABLE pins. It is therefore not necessary for software to invalidate the caches on start-up.

DCIMVAC operations perform an invalidate of the target address. If the data is dirty within the cluster then a clean is performed before the invalidate.

DCISW operations perform both a clean and invalidate of the target set/way. The values of HCR.SWIO and HCR_EL2.SWIO have no effect.

The Armv8-A architecture does not support an operation to invalidate the entire data cache. If this function is required in software, it must be constructed by iterating over the cache geometry and executing a series of individual invalidate by set/way instructions.
A5.6 **About read allocate mode**

The processor supports read allocate mode, also called write streaming mode, both for the L1 and the L2 cache.

Read allocate mode is a performance and power-saving optimization for writing a large block of data.

**Read allocate mode for the L1 data cache**

The L1 data cache supports only a Write-Back policy. It normally allocates a cache line on either a read miss or a write miss, although you can alter this by changing the inner cache allocation hints in the page tables. However, there are some situations where allocating on writes is not wanted, such as executing the C standard library `memset()` function to set a large block of memory to a known value. Writing large blocks of data like this can pollute the cache with unnecessary data. It can also waste power and reduce performance if a linefill must be performed only to discard the linefill data because the entire line was subsequently written by the `memset()` function. Therefore, the core includes logic to detect when the processor has written a full cache line before the linefill completed. If this situation is detected on a threshold number of consecutive linefills, the core switches to read allocate mode.

When the L1 data cache is in read allocate mode:

- Loads behave as normal and can still cause linefills.
- Writes still look up in the cache but if they miss, they write out to L2 rather than starting a linefill.

More than the specified number of linefills might be observed on the master interface, before the core detects that three full cache lines have been written and switches to read allocate mode.

The core continues in read allocate mode until it detects either a cacheable write burst to L2 that is not a full cache line, or there is a load to the same line as is currently being written to L2.

To configure the L1 read allocate mode threshold, use CPUACTLR.L1RADIS.

**Read allocate mode for the L2 cache**

The L2 cache enters read allocate mode after a threshold number of consecutive cache line sized writes to L2 are detected.

When the L2 cache is in read allocate mode:

- Loads behave as normal and can still cause linefills.
- Writes still lookup in the cache but if they miss, they write out to L3 rather than starting a linefill.

L2 read allocate mode continues until there is a cacheable write burst that is not a full cache line, or there is a load to the same line as is currently being written to L3.

To configure the L2 read allocate mode threshold, use CPUACTLR.RADIS.

**Related information**

*B1.42 CPU Auxiliary Control Register on page B1-202*
A5.7 About cache protection

The processor protects against soft errors that result in a RAM bitcell temporarily holding the incorrect value, by writing a new value to the RAM to correct the error. If the error is a hard error that is not corrected by writing to the RAM, for example a physical defect in the RAM, then the processor might get into a livelock because it continually detects and then tries to correct the error.

Some RAMs have Single Error Detect (SED) capability, others have Single Error Correct, Double Error Detect (SECDED) capability. The L1 data cache dirty RAM is Single Error Detect, Single Error Correct (SEDSEC). The processor can make progress and remain functionally correct when there is a single bit error in any RAM. If there are multiple single bit errors in different RAMs or within different protection granules within the same RAM, then the processor also remains functionally correct.

If there is a double bit error in a single RAM within the same protection granule, then the behavior depends on the RAM:

- For RAMs with SECDED capability, the processor detects and reports the error. If the error is in a cache line that contains dirty data, that data might be lost, which then causes data corruption.
- For RAMs with only SED, the processor does not detect a double bit error. This might cause data corruption.

If there are three or more bit errors the processor might or might not detect the errors, depending on the RAM and the position of the errors within the RAM.

The cache protection feature of the processor has a minimal performance impact when no errors are present. When the processor detects an error, it stalls the access that caused the error while it corrects the error. When the correction is complete, the access either continues with the corrected data or is retried. If the access is retried, it either hits in the cache again with the corrected data or misses in the cache and refetches the data from a lower level cache or from main memory.

**Table A5-2 Cache protection behavior of each RAM**

<table>
<thead>
<tr>
<th>RAM</th>
<th>Protection type</th>
<th>Configuration option</th>
<th>Protection granule</th>
<th>Correction behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1 instruction cache tag</td>
<td>Parity, SED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>31 bits</td>
<td>The processor invalidates both lines in the cache set then refetches the requested line from the L2 cache or external memory.</td>
</tr>
<tr>
<td>L1 instruction cache data</td>
<td>Parity, SED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>18 bits</td>
<td></td>
</tr>
<tr>
<td>TLB</td>
<td>Parity, SED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>31 bits or 51 bits</td>
<td>The processor invalidates the entry and starts a new pagewalk to refetch it.</td>
</tr>
<tr>
<td>L1 data cache tag</td>
<td>Parity, SED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>32 bits</td>
<td>The processor cleans the line and invalidates it from the L1 cache. It uses SCU duplicate tags to get the correct address. It refetches the line from the L2 cache or external memory.</td>
</tr>
<tr>
<td>L1 data cache data</td>
<td>ECC, SECDED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>32 bits</td>
<td>The processor cleans the line and invalidates it from the L1 cache. It corrects single bit errors as part of the eviction. It refetches the line from the L2 cache or external memory.</td>
</tr>
<tr>
<td>L1 data cache dirty</td>
<td>Parity, SEDSEC</td>
<td>CPU_CACHE_PROTECTION</td>
<td>1 bit</td>
<td>The processor cleans the line and invalidates it from the L1 cache. It corrects single bit errors as part of the eviction. Only the dirty bit is protected. The other bits are performance hints, therefore do not cause a functional failure if they are incorrect.</td>
</tr>
</tbody>
</table>
Table A5-2  Cache protection behavior of each RAM (continued)

<table>
<thead>
<tr>
<th>RAM</th>
<th>Protection type</th>
<th>Configuration option</th>
<th>Protection granule</th>
<th>Correction behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCU L1 duplicate tag</td>
<td>ECC, SECDED</td>
<td>CPU_CACHE_PROTECTION</td>
<td>33 bits</td>
<td>The processor rewrites the tag with the correct value and retries access. If the error is uncorrectable then the processor invalidates the tag.</td>
</tr>
<tr>
<td>L2 tag</td>
<td>ECC, SECDED</td>
<td>SCU_CACHE_PROTECTION</td>
<td>32 bits</td>
<td>The victim RAM only serves as a performance hint. It does not result in a functional failure if the contents are incorrect.</td>
</tr>
<tr>
<td>L2 victim</td>
<td>None</td>
<td>-</td>
<td>-</td>
<td>The processor corrects the data inline and might stall access for an additional cycle or two while the correction takes place. After correction, the processor might evict the line.</td>
</tr>
<tr>
<td>L2 data</td>
<td>ECC, SECDED</td>
<td>SCU_CACHE_PROTECTION</td>
<td>64 bits</td>
<td></td>
</tr>
</tbody>
</table>

If a correctable ECC error occurs after the first data cache access of a load instruction that takes multiple cycles to complete, and if one of the following conditions has taken place:

- A hardware breakpoint, watchpoint, or vector catch has been set since the first execution that is triggered on re-execution.
- The page tables have been modified since the first execution. This resulted in an instruction or data abort trap being taken on re-execution.

then the register file is updated with data that was successfully read before the correctable ECC error occurred.
A5.8 Error reporting

The processor reports detected errors, including errors that are successfully corrected and those that cannot be corrected, in the CPUMERRSR or L2MERRSR registers. It also signals them on the PMUEVENT bus.

If multiple errors occur on the same clock cycle then only one of them is reported. Errors that cannot be corrected, and therefore might result in data corruption, also cause an abort or external pin to be asserted, so that software can be aware that there is an error and can either attempt to recover or can restart the system. Such errors are:

- Uncorrectable errors in the L2 data RAM when read by an instruction fetch, TLB pagewalk, or load instruction, might result in a precise data abort or prefetch abort.
- Uncorrectable errors in the L2 data RAM when read by a fetch into the L1 data cache from a load, store or preload instruction, or by the hardware prefetcher, might result in an asynchronous exception.
- Uncorrectable errors in the L1 or L2 data RAMs when the line is being evicted from a cache results in the processor asserting the nINTERRIRQ signal. This might be because of a natural eviction, a cache maintenance operation, or a snoop.
- Uncorrectable errors in the L2 tag RAMs or SCU L1 duplicate tag RAMs result in the processor asserting the nINTERRIRQ signal.
- When nINTERRIRQ is asserted it remains asserted until the error is cleared by a write of 0 to the L2 internal asynchronous error bit of the L2ECTLR register.
- Arm recommends that the nINTERRIRQ signal is connected to the interrupt controller so that an interrupt or system error is generated when the signal is asserted.

When a dirty cache line with an error on the data RAMs is evicted from the processor, the write on the master interface still takes place, however if the error is uncorrectable then:

- On AXI and ACE, the write strobes are not set, therefore the incorrect data is not written externally.
- On CHI, the strobes are set, but the response field indicates that there is a data error.

When a snoop hits on a line with an uncorrectable data error the data is returned, if required by the snoop, but the snoop response indicates that there is an error.

If a snoop hits on a tag that has an uncorrectable error, then it is treated as a snoop miss, because the error means that it is unknown if the cache line is valid or not.

In some cases it is possible for an error to be counted more than once. For example, multiple accesses might read the location with the error before the line is evicted as part of the correction process.

Related reference

B1.44 CPU Memory Error Syndrome Register on page B1-208
B1.93 L2 Extended Control Register on page B1-299
B1.94 L2 Memory Error Syndrome Register on page B1-301
A5.9  Error injection

To support testing of error handling software, the processor provides the capability to force double-bit errors to be injected into the L1 D-cache data RAMs, the L2 data RAMs, and the L2 tag RAMs.

Error injection on the L1 D-cache data RAMs is enabled by setting the CPUACTLR.L1DEIEN bit. While this bit is set, double-bit errors are injected on all writes to the L1 D-cache data RAMs for the first word of each 32-byte region. This corresponds to bytes with an address where bits [4:2] are 0b000. The L1 D-cache RAMs can be written to because of:

- Explicit stores from the core.
- Cache line fetches into the cache, as a result of:
  - Load instructions.
  - Store instructions.
  - Preload instructions.
  - Data prefetches.
  - Pagewalks.

Error injection on the L2 data RAMs is enabled by setting the L2ACTLR.L2DEIEN bit. While this bit is set, double-bit errors are injected on all writes to the L2 cache data RAMs. The L2 data RAMs can be written to because of:

- Explicit stores from one of the cores.
- Instruction fetches or prefetches.
- Evictions from the L1 Data cache.
- ACP accesses.

Error injection on the L2 tag RAMs is enabled by setting the L2ACTLR.L2TEIEN bit. While this bit is set, double-bit errors are injected on all writes to the L2 tag RAMs. The L2 cache tag RAMs can be written because of:

- Explicit stores from one of the cores.
- L2 allocations caused by instruction fetches or prefetches.
- Evictions from the L1 Data cache.
- ACP accesses.
- Snoop operations.
- Cache maintenance instructions.
This chapter describes the L1 instruction cache and data cache.

It contains the following sections:

- *A6.1 About the L1 memory system* on page A6-86.
- *A6.3 Program flow prediction* on page A6-88.
- *A6.4 About the internal exclusive monitor* on page A6-89.
- *A6.5 About data prefetching* on page A6-90.
A6.1 About the L1 memory system

The L1 memory system includes several power-saving and performance-enhancing features. These include separate instruction and data caches, which can be configured independently during implementation to sizes of 8KB, 16KB, 32KB, or 64KB.

MMU
The MMU provides fine-grained memory system control through a set of virtual-to-physical address mappings and memory attributes held in translation tables. These are loaded into the Translation Lookaside Buffer (TLB) when a location is accessed. The key features are:
- 10-entry fully-associative instruction micro TLB.
- 10-entry fully-associative data micro TLB.
- 2-way set-associative 512-entry unified main TLB.
- 2-way set-associative 64-entry walk cache.
- 2-way set-associative 64-entry IPA cache.

L1 instruction-side memory system
The L1 instruction-side memory system provides an instruction stream to the DPU. The key features are:
- A dedicated instruction cache that:
  - is virtually indexed and physically tagged.
  - is 2-way set associative.
  - is configurable to be 8KB, 16KB, 32KB, or 64KB.
  - uses a cache line length of 64 bytes.
  - uses a pseudo-random replacement policy.
- A 128-bit read interface to the L2 memory system.
- Dynamic program flow prediction.

L1 data-side memory system
The L1 data-side memory system responds to load and store requests from the DPU. It also responds to snoop requests that have been forwarded by the SCU from other cores or external masters. The key features are:
- A dedicated data cache that:
  - is physically indexed and physically tagged.
  - is 4-way set associative.
  - is configurable to be 8KB, 16KB, 32KB, or 64KB.
  - uses a cache line length of 64 bytes.
  - uses a pseudo-random replacement policy.
- A 128-bit read and 256-bit write interface to the L2 memory system.
- A 64-bit read and 64-bit write path to the DPU.
- Read buffers that service the DCU, the IFU, and the TLB.
- Support for three outstanding data cache misses.
- Support for eight outstanding linefill requests.
- A merging store buffer.
- An internal exclusive monitor.
- An automatic data prefetch engine.
- Write stream detection and optimization (read allocate mode).

Related information
A6.4 About the internal exclusive monitor on page A6-89
A6.5 About data prefetching on page A6-90
A5.6 About read allocate mode on page A5-79
A6.2 TLB Organization

This section describes the organization of the TLB.

Micro TLB
The first level of caching for the translation table information is a micro TLB of ten entries that is implemented on each of the instruction and data sides. All main TLB related maintenance operations result in flushing both the instruction and data micro TLB.

Main TLB
A unified main TLB handles misses from the micro TLBs. It has a 512-entry, 2-way, set-associative structure and supports all VMSAv8 block sizes, except 1GB. If it fetches a 1GB block, the TLB splits it into 512MB blocks and stores the appropriate block for the lookup.

Accesses to the main TLB take a variable number of cycles. The number of cycles depends on the following criteria:
• Competing requests from each of the micro TLBs.
• The TLB maintenance operations in flight.
• The different page size mappings in use.

IPA cache RAM
The Intermediate Physical Address (IPA) cache RAM holds mappings between intermediate physical addresses and physical addresses. Only Non-secure EL1 and EL0 stage 2 translations use this cache. When a stage 2 translation is completed, it is updated and checked whenever a stage 2 translation is required.

Similarly to the main TLB, the IPA cache RAM can hold entries for different sizes.

Walk cache RAM
The walk cache RAM holds the result of a stage 1 translation up to but not including the last level. If the stage 1 translation results in a section or larger mapping then nothing is placed in the walk cache.

The walk cache holds entries fetched from Secure and Non-secure state.
A6.3 Program flow prediction

Program flow prediction is always enabled when the MMU is enabled by setting the appropriate control bit in the relevant system control register.

As a general rule, the flow prediction hardware predicts all branch outcomes regardless of the addressing mode. For example, it predicts the outcomes of the following branch types:

- Conditional branches.
- Unconditional branches.
- Indirect branches that are associated with procedure call and return instructions.
- Branches that switch between A32 and T32 states.

However, the flow prediction hardware does not predict the branch outcomes for the following instructions:

- Data-processing instructions that use the PC as a destination register.
- The BXJ instruction.
- Exception return instructions.

A T32 instruction set branch that is normally encoded as unconditional can be made conditional by inclusion in an If-Then (IT) block. Then it is treated as a conditional branch.

Return stack predictions

The return stack stores the return address and the A32 or T32 instruction set of the instruction after a procedure call type branch instruction. This address is equal to the link register value stored in r14. The following instructions cause a return stack push if predicted:

- BL.
- BLX (immediate).
- BLX (register).

In AArch32 state, the following instructions cause a return stack pop if predicted:

- BX
- LDR pc, [r13], #imm
- LDM r13, {...pc}
- LDM r13, {...pc}!

Related information

B1.105 System Control Register on page B1-324
A6.4 About the internal exclusive monitor

The internal exclusive monitor is a state machine that manages Load-Exclusive or Store-Exclusive instructions, and Clear-Exclusive (CLREX) instructions. Its two states are open and exclusive.

You can use the Load-Exclusive or Store-Exclusive accesses and the Clear-Exclusive instructions to construct semaphores to ensure synchronization between different processes running on the core and also between different cores that are using the same coherent memory locations for the semaphore.

A Load-Exclusive instruction tags a small block of memory for exclusive access. The size of the tagged block is defined by CTR.ERG as 16 words, one cache line.

A Load-exclusive/Store-exclusive instruction is any one of the following:

- Any instruction that has a mnemonic starting with LDREX, STREX, LDAEX, or STLEX.

A Load-Exclusive instruction that causes a transaction with ARLOCKM for AXI/ACE, or Excl for CHI, set to HIGH is expected to receive an EXOKAY response. An OKAY response to a transaction with ARLOCKM for AXI/ACE, or Excl for CHI, set to HIGH indicates that exclusive accesses are not supported at the address of the transaction and causes a Data Abort exception to be taken with a Data Fault Status Code of:

- 0b110101, when using the long descriptor format.
- 0b10101, when using the short descriptor format.

A Load-Exclusive instruction causes ARLOCKM for AXI to be set to HIGH if the memory attributes are:

- Device.
- Normal Inner Non-cacheable and Outer Non-cacheable.
- Normal Inner is not Write-Back or Outer is not Write-Back, and Inner Shareable.
- Normal Inner is not Write-Back or Outer is not Write-Back, and Outer Shareable.

A Load-Exclusive instruction causes ARLOCKM for ACE or Excl for CHI, to be set to HIGH if the memory attributes are:

- Device.
- Normal Inner Non-cacheable and Outer Non-cacheable.
- Normal Inner Write-Back, Outer Write-Back, Outer Shareable, and BROADCASTOUTER is set to HIGH.
- Normal Inner Write-Back, Outer Write-Back, Inner Shareable, and BROADCASTINNER is set to HIGH.
- Normal Inner is not Write-Back or Outer is not Write-Back, and Inner Shareable.
- Normal Inner is not Write-Back or Outer is not Write-Back, and Outer Shareable.

In cases where there is an intervening store operation between an exclusive load and an exclusive store from the same core, the intermediate store does not produce any direct effect on the internal exclusive monitor. The local monitor is in the Exclusive Access state after the exclusive load, remains in the Exclusive Access state after the store, and returns to the Open Access state only after the exclusive store, a CLREX instruction, or an exception return.

However, if the exclusive code sequence is accessing an address in cacheable memory, any cache line eviction that contains that address clears the monitor. Arm therefore recommends that no load or store instructions are placed between the exclusive load and the exclusive store because these additional instructions can cause a cache eviction. Any data cache maintenance instruction can also clear the exclusive monitor.

Related reference

A8.3 AXI transactions on page A8-102
A9.4 ACE transactions on page A9-111
A10.5 CHI transactions on page A10-125
A6.5 About data prefetching

This section describes the software and hardware data prefetching behavior for the processor.

**Preload instructions**

PLD instructions look up in the cache and start a linefill if they miss and are to a cacheable address. These instructions retire as soon as their linefill has started, they do not wait for data to be returned. This enables other instructions to execute while the linefill continues in the background.

PLDW instructions are similar to PLD, except that if they miss, the linefill causes data to be invalidated in other cores and masters so that the line is ready for writing.

PLI instructions are treated as NOPs.

**Automatic data prefetching and monitoring**

The L1 data-side memory system implements an automatic prefetcher that monitors cache misses in the core. When a pattern is detected, the automatic prefetcher starts linefills in the background. The prefetcher recognizes a sequence of data cache misses at a fixed stride pattern that lies in four cache lines, plus or minus. Any intervening stores or loads that hit in the data cache do not interfere with the recognition of the cache miss pattern.

The CPUACTLR enables you to:

- Deactivate the prefetcher.
- Alter the sequence length required to trigger the prefetcher.
- Alter the number of outstanding requests that the prefetcher can make.

Use PLD instructions for data prefetching where short sequences or irregular pattern fetches are required.

**Related information**

*B1.42 CPU Auxiliary Control Register on page B1-202*
Chapter A7
L2 Memory System

This chapter describes the L2 memory system and the Snoop Control Unit (SCU) that is tightly integrated with it.

It contains the following sections:
• A7.1 About the L2 memory system on page A7-92.
• A7.2 Snoop and maintenance requests on page A7-94.
• A7.3 Support for memory types on page A7-95.
• A7.4 Memory type information exported from the processor on page A7-96.
• A7.5 Handling of external aborts on page A7-97.
A7.1 About the L2 memory system

In most configurations, the L2 memory system consists of an integrated SCU that connects the cores in a cluster, an optional, tightly-coupled L2 cache, and an optional ACP interface. In single core, AXI configurations that do not include CPU cache protection, ACP, or an L2 cache, the SCU is replaced with a more area-efficient mini-SCU.

The same system register control bit enables the L1 data cache and the L2 cache.

SCU

The SCU maintains coherency between the L1 and L2 data caches in the processor. It also arbitrates requests for the L2 cache and the AXI, ACE, or CHI master interface.

A coherent request from a core is one that checks for data in the L1 data caches and, if present, the L2 cache. The SCU might send a request to another core to retrieve or invalidate data, or both, depending on the type of coherent request. This request is referred to as a snoop request. If the processor is implemented with an ACE or CHI master interface then the SCU can issue coherent requests on the master interface, which might result in snoop requests being sent to other masters in the system. The SCU might also receive snoop requests from other masters.

The SCU can handle direct cache-to-cache transfers between cores without having to read or write any data to the external memory system. Cache line migration enables dirty cache lines to be moved between cores, and there is no requirement to write back transferred cache line data to the external memory system.

Each core has tag and dirty RAMs that contain the state of the cache line in the L1 data cache. Rather than sending a snoop request to each core to access these for each coherent request, the SCU contains a set of duplicate tags that allows it to check the contents of each L1 data cache. The duplicate tags filter coherent requests so that a snoop request is only sent to a core if the coherent request hits in the corresponding duplicate tags. The duplicate tags are also used to filter snoop requests from the external memory system. This allows the cores and the system to function efficiently even with a high volume of requests.

The SCU does not support hardware management of coherency of the instruction caches. Instruction cache linefills perform coherent reads, however, there is no coherency management of data held in the instruction cache.

mini-SCU

The mini-SCU replaces the SCU in certain uniprocessor configurations that do not require data cache coherency with other masters in the system. That is, implementations that are configured to have a single CPU, no L2 cache, no CPU cache protection, and an AXI interface. The mini-SCU bridges between the master interface of the core and the AXI master interface of the processor.
**L2 cache**

Data cache lines are allocated to the L2 cache only when evicted from the L1 memory system, not when first fetched from the system. The only exceptions to this rule are for memory marked with the inner transient hint, or for non-temporal loads that are only ever allocated to the L2 cache. The L1 cache can prefetch data from the system, without data being evicted from the L2 cache.

Instruction cache lines are allocated to the L2 cache when fetched from the system and can be invalidated during maintenance operations.

The L2 cache is 8-way set associative. The L2 cache tags are looked up in parallel with the SCU duplicate tags. If both the L2 tag and SCU duplicate tag hit, a read accesses the L2 cache in preference to snooping one of the other cores.

L2 RAMs are invalidated automatically at reset unless the **L2RSTDISABLE** signal is set HIGH when the **nL2RESET** signal is deasserted.

Further features of the L2 cache are:
- Configurable size of 128KB, 256KB, 512KB, and 1MB.
- Fixed line length of 64 bytes.
- Physically indexed and tagged.
- Optional ECC protection.
- A pseudo-LRU replacement policy.

**ACP**

Optional 128-bit wide I/O coherent ACP interface that can allocate to the L2 cache.

**Master memory interface**

The SCU connects the cores to the external memory system through a 128-bit-wide master memory interface that uses ACE, CHI, or AXI technology. The memory interface supports integer ratios of the processor clock period up to and including 1:1 and a 40-bit physical address range.

The L2 memory system has two abort mechanisms, a synchronous one and an asynchronous one.

**Related information**

- *A7.5 Handling of external aborts on page A7-97*
- Chapter A9 ACE Master Interface on page A9-107
- Chapter A10 CHI Master Interface on page A10-119
- Chapter A8 AXI Master Interface on page A8-99
- Chapter A11 ACP Slave Interface on page A11-129
A7.2 Snoop and maintenance requests

In implementations that include an ACE or CHI master interface, the SCU controls snoop and maintenance requests to the external memory system with the **BROADCASTINNER**, **BROADCASTOUTER**, and **BROADCASTCACHEMAINT** configuration inputs.

### Table A7-1 Control pins for snoop and maintenance requests

<table>
<thead>
<tr>
<th>Signal</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BROADCASTINNER</td>
<td>1</td>
<td>The inner shareability domain extends beyond the processor. Inner Shareable snoop and maintenance operations are broadcast externally.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The inner shareability domain does not extend beyond the processor.</td>
</tr>
<tr>
<td>BROADCASTOUTER</td>
<td>1</td>
<td>The outer shareability domain extends beyond the processor. Outer shareable snoop and maintenance operations are broadcast externally.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>The outer shareability domain does not extend beyond the processor.</td>
</tr>
<tr>
<td>BROADCASTCACHEMAINT</td>
<td>1</td>
<td>There are external downstream caches and maintenance operations are broadcast externally.</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>There are no downstream caches external to the processor.</td>
</tr>
</tbody>
</table>

If you set the **BROADCASTINNER** pin to HIGH you must also set the **BROADCASTOUTER** pin to HIGH.

In a system that contains a Cortex-A32 processor and another processor in a big.LITTLE configuration, you must ensure the **BROADCASTINNER** and **BROADCASTOUTER** pins on both processors are set to HIGH so that both processors are in the same Inner Shareable domain.

Cacheable loads and stores to a shareability domain, that does not extend beyond the processor can allocate data to the L1 and L2 caches. However, they do not make coherent requests on the master for these accesses. Instead, they use only ReadNoSnoop or WriteNoSnoop transactions. This always includes non-shareable memory, and might include inner shareable and outer shareable memory, depending on the setting of the **BROADCASTINNER** and **BROADCASTOUTER** pins.

If the system sends a snoop to the Cortex-A32 processor for an address that is present in the L1 or L2 cache, but the line in the cache is in a shareability domain that does not extend beyond the cluster, then the snoop is treated as missing in the cluster.
A7.3 Support for memory types

The processor simplifies the coherency logic by downgrading some memory types.

- Memory that is marked as both Inner Write-Back Cacheable and Outer Write-Back Cacheable is cached in the L1 data cache and the L2 cache.
- Memory that is marked Inner Write-Through is downgraded to Non-cacheable.
- Memory that is marked Outer Write-Through or Outer Non-cacheable is downgraded to Non-cacheable, even if the inner attributes are Write-Back cacheable.

The attributes provided on `ARCACHE` or `AWCACHE` in AXI and ACE configurations or MemAttr and SnpAttr in CHI configurations are these downgraded attributes and indicate how the interconnect must treat the transaction.
A7.4 Memory type information exported from the processor

The processor makes attribute information about memory types available through signals for interconnects or bus protocols that require such information.

Some interconnects or bus protocols might require more information about the memory type and, for these cases, the cluster exports the memory attribute information from the translation tables stored in the TLB. These signals are for information only, and do not form part of the AXI, ACE, or CHI protocols.

- In an AXI or ACE configuration, there is a **RDMEMATTR** bus for the read channel and a **WRMEMATTR** bus for the write channel.
- In a CHI configuration, there is a single **REQMEMATTR** bus.

Table A7-2 Bus encoding for memory attributes

<table>
<thead>
<tr>
<th>Bits</th>
<th>Encoding</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>Outer shareable. Always set for device memory or memory that is both inner and outer non-cacheable.</td>
<td>Shareability information is not recorded in the L1 data cache for implementations that use the mini-SCU. <strong>WRMEMATTR[7]</strong> is 0b0 for L1 data cache evictions in these implementations.</td>
</tr>
<tr>
<td>[6:3]</td>
<td>Outer memory type, or device type. If bits[1:0] indicate Device, then: 0b0000 nGnRnE. 0b0100 nGnRE. 0b1000 nGRE. 0b1100 GRE. If bits[1:0] indicate Normal, then: 0b0100 NC. 0b10RW WT. 0b11RW WB. Where R is read allocate hint, W is write allocate hint.</td>
<td>If an Armv7 architecture operating system runs on the processor, the Device memory type matches the nGnRE encoding and the Strongly-Ordered memory type matches the nGnRnE memory type. Outer read allocate hint information is not recorded in the L1 or L2 data caches. <strong>WRMEMATTR[4]</strong> and <strong>REQMEMATTR[4]</strong> are set to 0b1 for data cache evictions.</td>
</tr>
<tr>
<td>[2]</td>
<td>Inner shareable. Anything with bit[7] set must also have bit[2] set.</td>
<td>Shareability information is not recorded in the L1 data cache for implementations that use the mini-SCU. <strong>WRMEMATTR[2]</strong> is 0b0 for L1 data cache evictions in these implementations.</td>
</tr>
<tr>
<td>[1:0]</td>
<td>Inner memory type: 0b0 Device. 0b01 NC. 0b10 WT. 0b11 WB.</td>
<td></td>
</tr>
</tbody>
</table>
A7.5 Handling of external aborts

The memory system handles external aborts using the synchronous abort mechanism, asynchronous abort mechanism, or the nEXTERRIRQ pin as described in this section.

**Synchronous abort mechanism**
External aborts on the following accesses use the synchronous abort mechanism.
- All load accesses.
- All Store Exclusive accesses (STREX, STREXB, STREXH, STREXD, STXR, STXRB, STXRH, STXP, STLXR, STLXRB, STLXRH, and STLXP).

**Asynchronous abort mechanism**
External aborts on the following accesses use the asynchronous abort mechanism.
- Stores to Device memory (except Store Exclusive accesses).
- Stores to Normal memory that is Inner Non-cacheable, Inner Write-Through, Outer Non-cacheable, or Outer Write-Through (except Store Exclusive accesses).
- L1 data cache and L2 cache linefills that receive data from the interconnect in the dirty state.

**nEXTERRIRQ pin**
External aborts on the following accesses cause the nEXTERRIRQ pin to be asserted because the aborts might not relate directly back to a specific core in the cluster.
- All store accesses to Normal memory that is both Inner write-back and Outer write-back.
- Evictions from the L1 data cache or L2 cache.
- DVM Complete transactions.

*Related reference*

B1.93 L2 Extended Control Register on page B1-299
A7.5 Handling of external aborts
Chapter A8
AXI Master Interface

This chapter describes the AXI master memory interface.

It contains the following sections:

• *A8.1 About the AXI master interface* on page A8-100.
• *A8.2 AXI privilege information* on page A8-101.
• *A8.3 AXI transactions* on page A8-102.
• *A8.4 Attributes of the AXI master interface* on page A8-104.
A8.1  About the AXI master interface

You can configure the processor to use the AXI protocol for the master memory interface.

**Read responses**

The AXI master can delay accepting a read data channel transfer by holding **RREADY** LOW for an indeterminate number of cycles. **RREADY** can be deasserted LOW between read data channel transfers that form part of the same transaction.

**Write responses**

The AXI master requires that the slave does not return a write response until it has received the write address.

The AXI master always accepts write responses without delay by holding **BREADY** HIGH.

**Barriers**

You must ensure that your interconnect and any peripherals connected to it do not return a write response for a transaction until that transaction would be considered complete by a later barrier. This means that the write must be observable to all other masters in the system. Arm expects the majority of peripherals to meet this requirement.

**Related information**

*A8.2 AXI privilege information on page A8-101*
A8.2 AXI privilege information

AXI provides information about the privilege level of an access on the ARPROT[0] and AWPROT[0] signals. However, when accesses might be cached or merged together, the resulting transaction can have both privileged and unprivileged data combined. If this happens, the processor marks the transaction as privileged, even if it was initiated by an unprivileged process.

The following table shows exception levels and corresponding ARPROT[0] and AWPROT[0] values.

<table>
<thead>
<tr>
<th>Processor exception level</th>
<th>Type of access</th>
<th>Value of ARPROT[0] and AWPROT[0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>Cacheable read access</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Device, or normal Non-cacheable read access</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL1, EL2, EL3</td>
<td></td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>Cacheable write access</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Device, nGnRnE, nGnRE, and nGRE write</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL1, EL2, EL3</td>
<td></td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Normal Non-cacheable or Device GRE write, except for STREX, STREXB, STREXH, STREXD, STXR, STXRB, STXRH, STXP, STLXR, STLXRB, STLXRH and STLXP to shareable memory</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Normal Non-cacheable write for STREX, STREXB, STREXH, STREXD, STXR STXRB, STXRH, STXP, STLXR, STLXRB, STLXRH and STLXP to shareable memory</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL1, EL2, EL3</td>
<td>Normal Non-cacheable write</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>TLB pagewalk</td>
<td>Privileged access</td>
</tr>
</tbody>
</table>

Table A8-1 ARPROT and AWPROT values
### A8.3 AXI transactions

The processor generates only a subset of all possible AXI transactions on the AXI master interface.

The processor does not generate any FIXED bursts and all WRAP bursts fetch a complete cache line starting with the critical word first. A burst does not cross a cache line boundary.

The cache linefill fetch length is always 64 bytes.

For WriteBack transfers the supported transfers are:
- WRAP 4 128-bit for read transfers (linefills).
- INCR 4 128-bit for write transfers (evictions).
- INCR N (N: 1, 2, or 4) 128-bit write transfers (read allocate).

For Non-cacheable transactions:
- INCR N (N: 1, 2, or 4) 128-bit for write transfers.
- INCR N (N: 1, 2, or 4) 128-bit for read transfers.
- INCR 1 32-bit, 64-bit, and 128-bit for read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive read transfers.

For Device transactions:
- INCR N (N: 1, 2, or 4) 128-bit read transfers.
- INCR N (N: 1, 2, or 4) 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive write transfers.

For translation table walk transactions INCR 1 32-bit, and 64-bit read transfers.

The following points apply to AXI transactions:
- WRAP bursts are only 128-bit.
- INCR 1 can be any size for read or write.
- INCR burst, more than one transfer, are only 128-bit.
- No transaction is marked as FIXED.
- Write transfers with none, some, or all byte strobes LOW can occur.

External memory accesses generate the following transactions in an implementation configured with an AXI master interface.

#### Table A8-2 AXI transactions

<table>
<thead>
<tr>
<th>Attributes</th>
<th>AXI transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Device</td>
<td>-</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Non-cacheable</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
<tr>
<td>Attributes</td>
<td>AXI transaction</td>
</tr>
<tr>
<td>------------</td>
<td>-----------------</td>
</tr>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Write-Back or Write-Through, or Normal, inner Write-Through, outer Write-Back, Write-Through or Non-cacheable, or Normal inner Write-Back outer Non-cacheable or Write-Through</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
<tr>
<td>Normal, inner Write-Back, outer Write-Back</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
</tbody>
</table>

**Related information**

*Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*
A8.4 Attributes of the AXI master interface

The table lists the possible values for the read and write issuing capabilities if the processor includes four cores.

- **n** Number of cores.
- **m** 1 if the processor is configured for the ACP interface, 0 if it is not.

### Table A8-3 AXI master interface attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write issuing capability</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>The cluster can issue a maximum of 16 writes:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Up to 16 writes to Normal memory that is both inner and outer write-back cacheable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Up to 15 writes to all other memory types, including Device, Normal non-cacheable, and Write-through.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any mix of memory types is possible, and each write can be a single write or a write burst.</td>
</tr>
<tr>
<td>Read issuing capability</td>
<td>8n + 4m</td>
<td>8 for each core in the cluster including up to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 8 data linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 4 non-cacheable or Device data reads.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 non-cacheable TLB page-walk read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 3 instruction linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If an ACP is configured, up to 4 ACP linefill requests can be generated.</td>
</tr>
<tr>
<td>Exclusive thread capability</td>
<td>n</td>
<td>Each core can have 1 exclusive access sequence in progress.</td>
</tr>
<tr>
<td>Write ID capability</td>
<td>16</td>
<td>The maximum number of outstanding write IDs is 16. This is the same as the maximum number of outstanding writes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</td>
</tr>
<tr>
<td>Write ID width</td>
<td>5</td>
<td>The ID encodes the source of the memory transaction. See Table A9-7 Encoding for AWIDM[4:0] on page A9-115.</td>
</tr>
<tr>
<td>Read ID capability</td>
<td>8n + 4m</td>
<td>8 for each core in the processor and 4 for the ACP.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</td>
</tr>
<tr>
<td>Read ID width</td>
<td>6</td>
<td>The ID encodes the source of the memory transaction. See Table A9-8 Encoding for ARIDM[5:0] on page A9-115.</td>
</tr>
</tbody>
</table>

In the following table, nn is the core number 0b00, 0b01, 0b10, or 0b11.
### Table A8-4  Encoding for AWIDM[4:0]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Issuing capability per ID</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write ID</td>
<td>0b000nn</td>
<td>1</td>
<td>Core (n) system domain store exclusive</td>
</tr>
<tr>
<td></td>
<td>0b001xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b010xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b011nn</td>
<td>15</td>
<td>Core (n) non-re-orderable device write</td>
</tr>
<tr>
<td></td>
<td>0b1xxxx</td>
<td>1</td>
<td>Write to normal memory, or re-orderable device memory</td>
</tr>
</tbody>
</table>

In the following table, \(n\) is the core number 0b00, 0b01, 0b10, or 0b11.

### Table A8-5  Encoding for ARIDM[5:0]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Issuing capability per ID</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read ID</td>
<td>0b0000nn</td>
<td>4</td>
<td>Core (n) system domain exclusive read or non-reorderable device read</td>
</tr>
<tr>
<td></td>
<td>0b001xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b01xxx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b01xx00</td>
<td>1</td>
<td>ACP read</td>
</tr>
<tr>
<td></td>
<td>0b01xx01</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b01xx1x</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b1xxxxn</td>
<td>1</td>
<td>Core (n) read</td>
</tr>
</tbody>
</table>

These ID and transaction details are provided for information only. Arm strongly recommends that all interconnects and peripherals are designed to support any type and number of transactions on any ID, to ensure compatibility with future products.

**Related information**

*Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*
A8 AXI Master Interface
A8.4 Attributes of the AXI master interface
This chapter describes the ACE master interface.

It contains the following sections:

- A9.1 About the ACE master interface on page A9-108.
- A9.3 ACE privilege information on page A9-110.
- A9.4 ACE transactions on page A9-111.
- A9.5 Attributes of the ACE master interface on page A9-114.
- A9.7 AXI compatibility mode on page A9-117.
A9.1 About the ACE master interface

You can configure the processor to use the ACE protocol for the master memory interface.

Read responses

The ACE master can delay accepting a read data channel transfer by holding RREADY LOW for an indeterminate number of cycles. RREADY can be deasserted LOW between read data channel transfers that form part of the same transaction.

The ACE master asserts the read acknowledge signal RACK HIGH in the ACLK cycle following acceptance of the last read data channel transfer for a transaction. RACK is asserted in AXI compatibility mode in addition to ACE configurations.

• For interoperability of system components, Arm recommends that components interfacing with the ACE master are fully ACE compliant with no reliance on the subset of permitted RACK behavior described for the processor.
• If the interconnect does not perform hazarding between coherent and non-coherent requests, then, after it has returned the first transfer of read data for a non-coherent read, it must return all the remaining read transfers in the transaction, without requiring progress of any snoops to the cluster that could be to the same address.

Write responses

The ACE master requires that the slave does not return a write response until it has received the write address.

The ACE master always accepts write responses without delay by holding BREADY HIGH. It asserts the write acknowledge signal WACK HIGH in the ACLK cycle following acceptance of a write response. WACK is asserted in AXI compatibility mode in addition to ACE configurations.

For interoperability of system components, Arm recommends that components interfacing with the ACE master are fully ACE compliant with no reliance on the subset of permitted BREADY and WACK behavior described for the processor.

Barriers

The processor does not send barrier transactions to the interconnect. All barriers are terminated within the cluster.

You must ensure that your interconnect and any peripherals connected to it do not return a write response for a transaction until that transaction would be considered complete by a later barrier. This means that the write must be observable to all other masters in the system. Arm expects the majority of peripherals to meet this requirement.

Related information

A8.2 AXI privilege information on page A8-101
A9.2 ACE configurations

This section describes the ACE configurations.

--- Note ---

If you want to connect the processor to an AXI interconnect, Arm recommends that you use the AXI processor configuration option. Using the ACE processor configuration option in AXI mode is less area-efficient than the AXI configuration option.

<table>
<thead>
<tr>
<th>Signal</th>
<th>AXI mode</th>
<th>ACE non-coherent</th>
<th>ACE outer coherent</th>
<th>ACE inner coherent</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>No L3 cache</td>
<td>With L3 cache</td>
<td>No L3 cache</td>
</tr>
<tr>
<td>BROADCASTCACHEMAINT</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>BROADCASTOUTER</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>BROADCASTINNER</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The following table shows the key features in each of the supported ACE configurations.

<table>
<thead>
<tr>
<th>Features</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>AXI3 or AXI4 compliance</td>
<td></td>
</tr>
<tr>
<td>ACE compliance</td>
<td></td>
</tr>
<tr>
<td>Barriers on AR and AW channels</td>
<td></td>
</tr>
<tr>
<td>Cache maintenance requests on AR channel</td>
<td></td>
</tr>
<tr>
<td>Snoops on AC channel</td>
<td></td>
</tr>
<tr>
<td>Coherent requests on AR or AW channel</td>
<td></td>
</tr>
<tr>
<td>DVM requests on AR channel</td>
<td></td>
</tr>
<tr>
<td>AXI mode</td>
<td></td>
</tr>
<tr>
<td>ACE non-coherent, no L3 cache</td>
<td>No</td>
</tr>
<tr>
<td>ACE non-coherent, with L3 cache</td>
<td>Yes</td>
</tr>
<tr>
<td>ACE outer coherent</td>
<td></td>
</tr>
<tr>
<td>ACE inner coherent</td>
<td></td>
</tr>
<tr>
<td>No L3 cache</td>
<td></td>
</tr>
<tr>
<td>With L3 cache</td>
<td></td>
</tr>
</tbody>
</table>

Table A9-1 Supported ACE configurations

Table A9-2 Supported features in the ACE configurations
A9.3 ACE privilege information

ACE provides information about the privilege level of an access on the ARPROT[0] and AWPROT[0] signals. However, when accesses might be cached or merged together, the resulting transaction can have both privileged and unprivileged data combined. If this happens, the processor marks the transaction as privileged, even if it was initiated by an unprivileged process.

The following table shows exception levels and corresponding ARPROT[0] and AWPROT[0] values.

<table>
<thead>
<tr>
<th>Processor exception level</th>
<th>Type of access</th>
<th>Value of ARPROT[0] and AWPROT[0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>Cacheable read access</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Device, or normal Non-cacheable read access</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL1, EL2, EL3</td>
<td>Cacheable write access</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>Device, nGnRN, nGnRE, and nGRE write</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Normal Non-cacheable or Device GRE write, except for STREX, STREXB, STREXH, STREXD, STXR, STXRB, STXRH, STXP, STLXR, STLXRB, STLXRH, and STLXP to shareable memory</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0</td>
<td>Normal Non-cacheable write for STREX, STREXB, STREXH, STREXD, STXR STXRB, STXRH, STXP, STLXR, STLXRB, STLXRH, and STLXP to shareable memory</td>
<td>Unprivileged access</td>
</tr>
<tr>
<td>EL1, EL2, EL3</td>
<td>Normal Non-cacheable write</td>
<td>Privileged access</td>
</tr>
<tr>
<td>EL0, EL1, EL2, EL3</td>
<td>TLB pagewalk</td>
<td>Privileged access</td>
</tr>
</tbody>
</table>
The processor generates only a subset of all possible ACE transactions on the ACE master interface. The processor does not generate any FIXED bursts and all WRAP bursts fetch a complete cache line starting with the critical word first. A burst does not cross a cache line boundary.

The cache linefill fetch length is always 64 bytes.

For WriteBack transfers the supported transfers are:

- WRAP 4 128-bit for read transfers (linefills).
- INCR 4 128-bit for write transfers (evictions).
- INCR N (N:1, 2, or 4) 128-bit write transfers (read allocate).

For Non-cacheable transactions:

- INCR N (N:1, 2, or 4) 128-bit for write transfers.
- INCR N (N:1, 2, or 4) 128-bit for read transfers.
- INCR 1 32-bit, 64-bit, and 128-bit for read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit for exclusive read transfers.

For Device transactions:

- INCR N (N:1, 2, or 4) 128-bit read transfers.
- INCR N (N:1, 2, or 4) 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit write transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive read transfers.
- INCR 1 8-bit, 16-bit, 32-bit, 64-bit, and 128-bit exclusive write transfers.

External memory accesses generate the following transactions in an implementation configured with an ACE master interface.

<table>
<thead>
<tr>
<th>Attributes</th>
<th>ACE transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Device</td>
<td>-</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Non-cacheable</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Write-Back or Write-Through, or Normal, inner Write-Through, outer Write-Back, Write-Through or Non-cacheable, or Normal inner Write-Back outer Non-cacheable or Write-Through</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
</tbody>
</table>
The following table shows the ACE transactions that can be generated, and some typical operations that might cause the transactions to be generated. This is not an exhaustive list of ways to generate each type of transaction, because there are many possibilities.

### Table A9-4  ACE transactions (continued)

<table>
<thead>
<tr>
<th>Attributes</th>
<th>ACE transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Normal, inner Write-Back, outer Write-Back</td>
<td>Non-shared</td>
</tr>
<tr>
<td></td>
<td>Inner-shared</td>
</tr>
<tr>
<td></td>
<td>Outer-shared</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ReadNoSnoop</td>
<td>Non-cacheable loads or instruction fetches. Linefills of non-shareable cache lines into L1 or L2.</td>
</tr>
<tr>
<td>ReadOnce</td>
<td>Cacheable loads that are not allocating into the cache, or cacheable instruction fetches when there is no L2 cache.</td>
</tr>
<tr>
<td>ReadClean</td>
<td>Not used.</td>
</tr>
<tr>
<td>ReadNotSharedDirty</td>
<td>Not used.</td>
</tr>
<tr>
<td>ReadShared</td>
<td>L1 Data linefills started by a load instruction, or L2 linefills started by an instruction fetch.</td>
</tr>
<tr>
<td>ReadUnique</td>
<td>L1 Data linefills started by a store instruction.</td>
</tr>
<tr>
<td>CleanUnique</td>
<td>Store instructions that hit in the cache but the line is not in a unique coherence state. Store instructions that are not allocating into the L1 or L2 caches, for example when streaming writes.</td>
</tr>
<tr>
<td>MakeUnique</td>
<td>Store instructions of a full cache line of data, that miss in the caches, and are allocating into the L2 cache.</td>
</tr>
<tr>
<td>CleanShared</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>CleanInvalid</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>MakeInvalid</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>DVM</td>
<td>TLB and instruction cache maintenance instructions.</td>
</tr>
<tr>
<td>DVM complete</td>
<td>DVM sync snoops received from the interconnect.</td>
</tr>
<tr>
<td>Barriers</td>
<td>DMB and DSB instructions. DVM sync snoops received from the interconnect.</td>
</tr>
<tr>
<td>WriteNoSnoop</td>
<td>Non-cacheable store instructions. Evictions of non-shareable cache lines from L1 and L2.</td>
</tr>
<tr>
<td>WriteUnique</td>
<td>Not used.</td>
</tr>
<tr>
<td>WriteLineUnique</td>
<td>Not used.</td>
</tr>
<tr>
<td>WriteBack</td>
<td>Evictions of dirty lines from the L1 or L2 cache, or streaming writes that are not allocating into the cache.</td>
</tr>
<tr>
<td>WriteClean</td>
<td>Evictions of dirty lines from the L2 cache, when the line is still present in an L1 cache. Some cache maintenance instructions.</td>
</tr>
</tbody>
</table>
### Table A9-5  ACE transactions and typical operations (continued)

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>WriteEvict</td>
<td>Evictions of unique clean lines, when configured in the L2ACTLR.</td>
</tr>
<tr>
<td>Evict</td>
<td>Evictions of clean lines, when configured in the L2ACTLR.</td>
</tr>
</tbody>
</table>

**Related information**

*Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*
### A9.5 Attributes of the ACE master interface

The table lists the maximum possible values for the read and write issuing capabilities if the processor includes four cores.

- **n** Number of cores.
- **m** 1 if the processor is configured for the ACP interface, 0 if it is not.

#### Table A9-6 ACE master interface attributes

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write issuing capability</td>
<td>16</td>
<td>The cluster can issue a maximum of 16 writes:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Up to 16 writes to Normal memory that is both inner and outer write-back cacheable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Up to 15 writes to all other memory types, including Device, Normal non-cacheable, and Write-through.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Any mix of memory types is possible, and each write can be a single write or a write burst.</td>
</tr>
<tr>
<td>Read issuing capability</td>
<td>$8n + 4m$</td>
<td>8 for each core in the cluster including up to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 8 data linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 4 non-cacheable or Device data reads.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 non-cacheable TLB page-walk read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 3 instruction linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 5 coherency operations.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 8 DVM messages.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The 8 DVM messages per core can each be two-part DVM messages. They result in up to 16 DVM transactions per core.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If an ACP is configured, up to 4 ACP linefill requests can be generated.</td>
</tr>
<tr>
<td>Exclusive thread capability</td>
<td>n</td>
<td>Each core can have 1 exclusive access sequence in progress.</td>
</tr>
<tr>
<td>Write ID capability</td>
<td>16</td>
<td>The maximum number of outstanding write IDs is 16. This is the same as the maximum number of outstanding writes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</td>
</tr>
<tr>
<td>Write ID width</td>
<td>5</td>
<td>The ID encodes the source of the memory transaction. See Table A9-7 Encoding for AWIDM[4:0] on page A9-115.</td>
</tr>
<tr>
<td>Read ID capability</td>
<td>$8n + 4m$</td>
<td>8 for each core in the processor and 4 for the ACP.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Only Device memory types with nGnRnE or nGnRE can have more than one outstanding transaction with the same AXI ID. All other memory types use a unique AXI ID for every outstanding transaction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Two part DVMs use the same ID for both parts, and therefore can have two outstanding transactions on the same ID.</td>
</tr>
<tr>
<td>Read ID width</td>
<td>6</td>
<td>The ID encodes the source of the memory transaction. See Table A9-8 Encoding for ARIDM[5:0] on page A9-115.</td>
</tr>
</tbody>
</table>

In the following table, nn is the core number 0b00, 0b01, 0b10, or 0b11.
### Table A9-7  Encoding for AWIDM[4:0]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Issuing capability per ID</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write ID</td>
<td>0b000nn</td>
<td>1</td>
<td>Core nn system domain store exclusive</td>
</tr>
<tr>
<td></td>
<td>0b001xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b010xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b011nn</td>
<td>15</td>
<td>Core nn non-re-orderable device write</td>
</tr>
<tr>
<td></td>
<td>0b1xxx</td>
<td>1</td>
<td>Write to normal memory, or re-orderable device memory</td>
</tr>
</tbody>
</table>

In the following table, nn is the core number 0b00, 0b01, 0b10, or 0b11.

### Table A9-8  Encoding for ARIDM[5:0]

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Issuing capability per ID</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read ID</td>
<td>0b0000nn</td>
<td>4</td>
<td>Core nn exclusive read or non-reorderable device read</td>
</tr>
<tr>
<td></td>
<td>0b001xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b01000</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b01001</td>
<td>1</td>
<td>DVM complete</td>
</tr>
<tr>
<td></td>
<td>0b0101x</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b011xx</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b1xxx00</td>
<td>1</td>
<td>ACP read</td>
</tr>
<tr>
<td></td>
<td>0b1xxx01</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b1xxx1x</td>
<td>0</td>
<td>Unused</td>
</tr>
<tr>
<td></td>
<td>0b1xxxx</td>
<td>1</td>
<td>Core nn read</td>
</tr>
</tbody>
</table>

These ID and transaction details are provided for information only. Arm strongly recommends that all interconnects and peripherals are designed to support any type and number of transactions on any ID, to ensure compatibility with future products.

**Related information**

*Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*
## A9.6 Snoop channel properties

The table shows the properties of the ACE channels.

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Snoop acceptance capability</td>
<td>8</td>
<td>The SCU can accept and process a maximum of eight snoop requests from the system. It counts requests from the request being accepted on the AC channel to the response being accepted on the CR channel.</td>
</tr>
<tr>
<td>Snoop latency</td>
<td>Hit</td>
<td>When there is a hit in L2 cache, the best case for response and data is 13 processor cycles. When there is a miss in L2 cache and a hit in L1 cache, the best case for response and data is 16 processor cycles. Latencies can be higher if hazards occur or if there are not enough buffers to absorb requests.</td>
</tr>
<tr>
<td></td>
<td>Miss</td>
<td>Best case six processor cycles when the SCU duplicate tags and L2 tags indicate the miss.</td>
</tr>
<tr>
<td></td>
<td>DVM</td>
<td>The cluster takes a minimum of six cycles to provide a response to DVM packets.</td>
</tr>
</tbody>
</table>
| Snoop filter            | Supported | The cluster provides support for an external snoop filter in an interconnect. It indicates when clean lines are evicted from the processor by sending Evict transactions on the write channel. However there are some cases where incorrect software can prevent an Evict transaction from being sent. Therefore you must ensure that you build any external snoop filter to handle a capacity overflow that sends a back-invalidation to the processor if it runs out of storage. Examples of cases where evicts are not produced include:  
  • Linefills that take external aborts.  
  • Store exclusives that fail.  
  • Mismatched aliases. |
| Supported transactions  | -     | All transactions described by the ACE protocols:  
  • Are accepted on the master interface from the system.  
  • Can be produced on the ACE master interface except:  
    — WriteUnique.  
    — WriteLineUnique.  
    — ReadNotSharedDirty.  
    — ReadClean. |

### Related information

*Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, ACE and ACE-Lite*
A9.7 AXI compatibility mode

The processor implements an AXI3/AXI4 compatibility mode in ACE configurations. With this mode you can use the processor in a standalone environment where the AMBA 4 ACE interface is not required.

To enable the AXI compatibility mode, you must ensure that the BROADCASTINNER, BROADCASTOUTER, and BROADCASTCACHEMAINT input pins are set to LOW.

Note

The AXI build-time configuration option provides a more area-efficient AXI solution than the AXI compatibility mode in ACE configurations.
Chapter A10
CHI Master Interface

This chapter describes the CHI master memory interface.

It contains the following sections:
• A10.1 About the CHI master interface on page A10-120.
• A10.2 CHI configurations on page A10-121.
• A10.3 Attributes of the CHI master interface on page A10-122.
• A10.4 CHI channel properties on page A10-124.
• A10.5 CHI transactions on page A10-125.
A10.1  About the CHI master interface

You can configure the processor to use the CHI protocol for the master memory interface.
A10.2 CHI configurations

This section describes the CHI configurations.

The following table shows the permitted combinations of these signals and the supported configurations in the Cortex-A32 processor, with a CHI bus.

Table A10-1  Supported CHI configurations

<table>
<thead>
<tr>
<th>Signal</th>
<th>Feature</th>
<th>CHI non-coherent</th>
<th>CHI outer coherent</th>
<th>CHI inner coherent</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>No L3 cache</td>
<td>With L3 cache</td>
<td>No L3 cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>With L3 cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>No L3 cache</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>With L3 cache</td>
</tr>
<tr>
<td>BROADCASTCACHEMAINT</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>BROADCASTOUTER</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>BROADCASTINNER</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

The following table shows the key features in each of the supported CHI configurations.

Table A10-2  Supported features in the CHI configurations

<table>
<thead>
<tr>
<th>Features</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cache maintenance requests on TXREQ channel</td>
<td>CHI non-coherent, no L3 cache</td>
</tr>
<tr>
<td>Snoop on RXREQ channel</td>
<td>No</td>
</tr>
<tr>
<td>Coherent requests on TXREQ channel</td>
<td>No</td>
</tr>
<tr>
<td>DVM requests on TXREQ channel</td>
<td>No</td>
</tr>
</tbody>
</table>
A10.3 Attributes of the CHI master interface

The table lists the possible values for the read and write issuing capabilities if the processor includes four cores.

- \( n \)  Number of cores.
- \( m \)  1 if the processor is configured for the ACP interface, 0 if it is not.
- \( w \)  (write issuing capability)+1.

### Table A10-3 Attributes of the CHI master memory interface

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write issuing capability</td>
<td>Configuration dependent</td>
<td>The maximum number of writes varies, depending on the configuration of the processor:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- The number of cores.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- The presence of the L2 cache.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If no L2 cache is configured:</td>
</tr>
<tr>
<td></td>
<td>One core</td>
<td>5 outstanding writes.</td>
</tr>
<tr>
<td></td>
<td>2-4 cores</td>
<td>8 outstanding writes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If an L2 cache is configured:</td>
</tr>
<tr>
<td></td>
<td>One core</td>
<td>7 outstanding writes.</td>
</tr>
<tr>
<td></td>
<td>2-4 cores</td>
<td>10 outstanding writes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A cluster with four cores, with L2 cache, can issue 10 outstanding transactions. A processor with one core, without L2 cache, can issue five outstanding transactions. All outstanding transactions use a unique ID.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8n + 4m + 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8 for each core in the cluster including up to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 8 data linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 4 Non-cacheable or Device data reads.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 1 Non-cacheable TLB page-walk read.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 3 instruction linefills.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 5 coherency operations.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 1 barrier operation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- 8 DVM messages.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If an ACP is configured, up to 4 ACP linefill requests can be generated. 1 barrier operation is generated from the cluster.</td>
</tr>
<tr>
<td>Exclusive thread capability</td>
<td>( n )</td>
<td>Each core can have 1 exclusive access sequence in progress.</td>
</tr>
</tbody>
</table>

Non-Confidential
Table A10-3  Attributes of the CHI master memory interface (continued)

<table>
<thead>
<tr>
<th>Attribute</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transaction ID width</td>
<td>8</td>
<td>The ID encodes the source of the memory transaction. See A9.5 Attributes of the ACE master interface on page A9-114.</td>
</tr>
<tr>
<td>Transaction ID</td>
<td>8n + 4m + w + 1</td>
<td>8 for each core in the cluster in addition to:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 4 for the ACP interface.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 1 for barriers.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• 6 to 11 writes, depending on the write issuing capability.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Unlike in configurations with AXI or ACE, there is never any ID reuse in CHI implementations, regardless of the memory type.</td>
</tr>
</tbody>
</table>

There is no fixed mapping between CHI transaction IDs and cores. Some transaction IDs can be used for either reads or writes.

Related information
A9.5 Attributes of the ACE master interface on page A9-114
Arm® AMBA® 5 CHI Protocol Specification
### A10.4 CHI channel properties

You can configure the processor to use the CHI protocol for the master memory interface

#### Table A10-4 CHI channel properties

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Snoop acceptance capability</td>
<td>10</td>
<td>The SCU can accept and process a maximum of 10 snoop requests from the system.</td>
</tr>
<tr>
<td>DVM acceptance capability</td>
<td>4</td>
<td>The SCU can accept and process a maximum of four DVM transactions from the system. Each of these four transactions can be a two part DVM message. The interconnect must be configured to never send more than four DVM messages to a Cortex-A32 processor, otherwise the system might deadlock.</td>
</tr>
<tr>
<td>Snoop latency</td>
<td>Hit</td>
<td>When there is a hit in L2 cache, the best case for response and data is 11 processor cycles. When there is a miss in L2 cache and a hit in L1 cache, the best case for response and data is 14 processor cycles. Latencies can be higher if hazards occur or if there are not enough buffers to absorb requests.</td>
</tr>
<tr>
<td></td>
<td>Miss</td>
<td>Best case six processor cycles when the SCU duplicate tags and L2 tags indicate the miss.</td>
</tr>
<tr>
<td></td>
<td>DVM</td>
<td>The cluster takes a minimum of six cycles to provide a response to DVM packets.</td>
</tr>
<tr>
<td>Snoop filter</td>
<td>Supported</td>
<td>The cluster provides support for an external snoop filter in an interconnect. It indicates when clean lines are evicted from the processor by sending Evict transactions on the CHI write channel. However, there are some cases where incorrect software can prevent an Evict transaction from being sent, therefore you must ensure that any external snoop filter is built to handle a capacity overflow that sends a back-invalidation to the processor if it runs out of storage.</td>
</tr>
<tr>
<td>Supported transactions</td>
<td>-</td>
<td>All transactions described by the CHI protocol:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Are accepted on the CHI master interface from the system.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Can be produced on the CHI master interface except:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— ReadClean.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— WriteBackPtl.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— WriteCleanPtl.</td>
</tr>
</tbody>
</table>

**Related information**

*Arm® AMBA® 5 CHI Protocol Specification*
A10.5 CHI transactions

CHI transactions are sent to a specific node in the interconnect based on the following criteria:

- Type of access.
- Address of the access.
- Settings of the System Address Map.

Addresses that map to an HN-F node can be marked as cacheable memory in the page tables, and can take part in the cache coherency protocol. Addresses that map to an HN-I or MN must be marked as device or non-cacheable memory.

Table A10-5 CHI transaction IDs

<table>
<thead>
<tr>
<th>Transaction ID</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000nnxxx</td>
<td>Transaction from core nn. Can be a:</td>
</tr>
<tr>
<td></td>
<td>• Read transaction.</td>
</tr>
<tr>
<td></td>
<td>• Write transaction.</td>
</tr>
<tr>
<td></td>
<td>• Cache maintenance transaction.</td>
</tr>
<tr>
<td></td>
<td>• DVM transaction.</td>
</tr>
<tr>
<td></td>
<td>• Barrier transaction.</td>
</tr>
<tr>
<td>001001xx</td>
<td>Transaction from the ACP interface. Can be a read or write.</td>
</tr>
<tr>
<td>00101110</td>
<td>Barrier generated in response to a DVM sync snoop from the interconnect.</td>
</tr>
<tr>
<td>0100xxxx</td>
<td>Eviction from L1 or L2 cache. The number of IDs used depends on the configuration.</td>
</tr>
</tbody>
</table>

Table A10-6 CHI transactions

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>ReadNoSnp</td>
<td>Non-cacheable loads or instruction fetches. Linefills of non-shareable cache lines into L1 or L2.</td>
</tr>
<tr>
<td>ReadOnce</td>
<td>Cacheable loads that are not allocating into the cache, or cacheable instruction fetches when there is no L2 cache.</td>
</tr>
<tr>
<td>ReadClean</td>
<td>Not used.</td>
</tr>
<tr>
<td>ReadShared</td>
<td>L1 Data linefills started by a load instruction, or L2 linefills started by an instruction fetch.</td>
</tr>
<tr>
<td>ReadUnique</td>
<td>L1 Data linefills started by a store instruction.</td>
</tr>
<tr>
<td>CleanUnique</td>
<td>Store instructions that hit in the cache but the line is not in a unique coherence state.</td>
</tr>
<tr>
<td>MakeUnique</td>
<td>Store instructions of a full cache line of data, that miss in the caches, and are allocating into the L2 cache.</td>
</tr>
<tr>
<td>CleanShared</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>CleanInvalid</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>MakeInvalid</td>
<td>Cache maintenance instructions.</td>
</tr>
<tr>
<td>DVMOp</td>
<td>TLB and instruction cache maintenance instructions.</td>
</tr>
<tr>
<td>EOBarrier</td>
<td>DMB instructions.</td>
</tr>
<tr>
<td>ECBARRIER</td>
<td>DSB instructions. DVM sync snoops received from the interconnect.</td>
</tr>
<tr>
<td>WriteNoSnpPtl</td>
<td>Non-cacheable store instructions.</td>
</tr>
<tr>
<td>WriteNoSnpFull</td>
<td>Non-cacheable store instructions, or evictions of non-shareable cache lines from the L1 and L2 cache.</td>
</tr>
<tr>
<td>WriteUniqueFull</td>
<td>Cacheable writes of a full cache line, that are not allocating into L1 or L2 caches, for example streaming writes.</td>
</tr>
<tr>
<td>WriteUniquePtl</td>
<td>Cacheable writes of less than a full cache line that are not allocating into L1 or L2.</td>
</tr>
</tbody>
</table>
External memory accesses generate the following transactions in an implementation configured with a CHI master interface.

### Table A10-6 CHI transactions (continued)

<table>
<thead>
<tr>
<th>Transaction</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>WriteBackFull</td>
<td>Evictions of dirty lines from the L1 or L2 cache.</td>
</tr>
<tr>
<td>WriteBackPtr</td>
<td>Not used.</td>
</tr>
<tr>
<td>WriteCleanFull</td>
<td>Evictions of dirty lines from the L2 cache, when the line is still present in an L1 cache. Some cache maintenance instructions.</td>
</tr>
<tr>
<td>WriteCleanPtr</td>
<td>Not used.</td>
</tr>
<tr>
<td>WriteEvictFull</td>
<td>Evictions of unique clean lines, when configured in the L2ACTLR.</td>
</tr>
<tr>
<td>Evict</td>
<td>Evictions of clean lines, when configured in the L2ACTLR.</td>
</tr>
</tbody>
</table>

### Table A10-7 CHI transactions

<table>
<thead>
<tr>
<th>Attributes</th>
<th>CHI transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Device</td>
<td>-</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Non-cacheable</td>
<td>Non-shared</td>
</tr>
<tr>
<td>Normal, inner Non-cacheable, outer Write-Back or Write-Through, or Normal, inner Write-Through, outer Write-Back, Write-Through or Non-cacheable, or Normal inner Write-Back outer Non-cacheable or Write-Through</td>
<td>Non-shared</td>
</tr>
<tr>
<td>Inner-shared</td>
<td>Non-snoopable</td>
</tr>
<tr>
<td>Outer-shared</td>
<td>Non-snoopable</td>
</tr>
</tbody>
</table>
### Table A10-7  CHI transactions (continued)

<table>
<thead>
<tr>
<th>Attributes</th>
<th>CHI transaction</th>
</tr>
</thead>
<tbody>
<tr>
<td>Memory type</td>
<td>Shareability</td>
</tr>
<tr>
<td>Normal, inner Write-Back, outer Write-Back</td>
<td>Non-shared</td>
</tr>
<tr>
<td>Inner-shared</td>
<td>Inner snoopable</td>
</tr>
<tr>
<td>Outer-shared</td>
<td>Outer snoopable</td>
</tr>
</tbody>
</table>

**Related information**

*Arm® AMBA® 5 CHI Protocol Specification*
Chapter A11
ACP Slave Interface

This chapter describes the ACP slave interface.

It contains the following sections:

• A11.1 About the ACP on page A11-130.
• A11.2 Transfer size support on page A11-131.
• A11.3 ACP performance on page A11-132.
• A11.4 ACP user signals on page A11-133.
A11.1 About the ACP

The optional *Accelerator Coherency Port* (ACP) is implemented as an AXI4 slave interface with some restrictions.

- 128-bit read and write interfaces.
- **ARCACHE** and **AWCACHE** are restricted to Normal, Write-Back, Read-Write-Allocate, Read-Allocate, Write-Allocate, and No-Allocate memory. **ARCACHE** and **AWCACHE** are limited to the values 0b0111, 0b1011, and 0b1111. Other values cause a SLVERR response on **RRESP** or **BRESP**.
- Exclusive accesses are not supported.
- Barriers are not supported. The **BRESP** handshake for a write transaction indicates global observability for that write.
- **ARSIZE** and **AWSIZE** signals are not present and assume a value of 0b100, 16 bytes.
- **ARBURST** and **AWBURST** signals are not present and assume a value of INCR.
- **ARLOCK** and **AWLOCK** signals are not present.
- **ARQOS** and **AWQOS** signals are not present.
- **ARLEN** and **AWLEN** are limited to values 0 and 3.
A11.2 Transfer size support

ACP supports the following read-request transfer size and length combinations:

- 64 byte INCR request characterized by:
  - **ARLEN** is 0x03, 4 beats.
  - **ARADDR** aligned to 64 byte boundary, so **ARADDR[5:0]** is 0b00 0000.
  - **ARSIZE** and **ARBURST** assume values of 0b100 and INCR respectively.

- 16 byte INCR request characterized by:
  - **ARLEN** is 0x00, 1 beat.
  - **ARADDR** aligned to 16 byte boundary, so **ARADDR[3:0]** is 0x0.

ACP supports the following write-request transfer size and length combinations:

- 64 byte INCR request characterized by:
  - **AWLEN** is 0x03, 4 beats.
  - **AWADDR** aligned to 64 byte boundary, so **AWADDR[5:0]** is 0b00 0000.
  - **AWSIZE** and **AWBURST** assume values of 0b100 and INCR respectively.
  - **WSTRB** for all beats must be the same and either all asserted or all deasserted.

- 16 byte INCR request characterized by:
  - **AWLEN** is 0x00, 1 beat.
  - **AWADDR** aligned to 16 byte boundary, so **AWADDR[3:0]** is 0x0.
  - **AWSIZE** and **AWBURST** assume values of 0b100 and INCR respectively.
  - **WSTRB** can take any value.

Requests not meeting these restrictions cause a SLVERR response on **RRESP** or **BRESP**.
A11.3 ACP performance

The ACP interface can support up to four outstanding transactions. These can be any combination of reads and writes.

The master must avoid sending more than one outstanding transaction on the same AXI ID, to prevent the second transaction stalling the interface until the first has completed. If the master requires explicit ordering between two transactions, Arm recommends that it waits for the response to the first transaction before sending the second transaction.

Writes are higher performance when they contain a full cache line of data.

If SCU cache protection is configured, writes of less than 64 bits incur an overhead of performing a read-modify-write sequence if they hit in the L2 cache.

Some L2 resources are shared between the ACP interface and the cores, therefore heavy traffic on the ACP interface might, in some cases, reduce the performance of the cores.

**AXI and ACE** You can use the `ARCACHE` and `AWCACHE` signals to control whether the ACP request causes an allocation into the L2 cache if it misses.

**CHI** To ensure correct ordering of data beats, ACP reads that miss always allocate into the L2 cache.
**A11.4 ACP user signals**

ACP transactions can cause coherent requests to the system. Therefore ACP requests must pass Inner and Outer Shareable attributes to the L2. Use specific encoding to pass the shareability attribute.

<table>
<thead>
<tr>
<th>AxUSER[1:0]</th>
<th>Attribute</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable</td>
</tr>
</tbody>
</table>

This is the same encoding as AxDOMAIN on ACE, except that a value of 0b11 is not supported.
Chapter A12
GIC CPU Interface

This chapter describes the Generic Interrupt Controller (GIC) CPU interface of the processor.

It contains the following sections:

• A12.1 Bypassing the GIC CPU Interface on page A12-136.
• A12.2 Memory map for the GIC CPU interface on page A12-137.
A12.1 Bypassing the GIC CPU Interface

The processor optionally implements the GIC CPU Interface. If present, you can disable it by asserting the GICCDISABLE signal HIGH at reset.

If the GIC is enabled, the input pins nVIRQ and nVFIQ must be tied off to HIGH because the internal GIC CPU interface generates the virtual interrupt signals to the cores. Software controls the nIRQ and nFIQ signals, therefore there is no requirement to tie them HIGH. If you disable the GIC CPU interface, a GIC that is external to the processor can drive the input signals nVIRQ and nVFIQ.

Asserting the GICCDISABLE signal HIGH at reset removes access to the memory-mapped and system GIC CPU Interface registers.

Related information

B1.85 Processor Feature Register 1 on page B1-285
A12.2 Memory map for the GIC CPU interface

The GIC CPU Interface is a memory-mapped interface. It is offset from PERIPHBASE.

If GICCDISABLE is asserted, the registers are not available.

<table>
<thead>
<tr>
<th>Address range</th>
<th>Functional block</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00000-0x01FF</td>
<td>CPU Interface</td>
</tr>
<tr>
<td>0x02000-0x0FFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x10000-0x10FFF</td>
<td>Virtual Interface Control</td>
</tr>
<tr>
<td>0x11000-0x1FFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x20000-0x21FFF</td>
<td>Virtual CPU Interface</td>
</tr>
<tr>
<td>0x22000-0x2EFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x2F000-0x30FFF</td>
<td>Alias of Virtual CPU Interface</td>
</tr>
<tr>
<td>0x31000-0x3FFFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Related information

B1.85 Processor Feature Register 1 on page B1-285
A12 GIC CPU Interface
A12.2 Memory map for the GIC CPU interface
Part B
Register Descriptions
Chapter B1
AArch32 system registers

This chapter describes the system registers in the AArch32 state.

It contains the following sections:
- B1.1 AArch32 register summary on page B1-144.
- B1.2 c0 registers on page B1-146.
- B1.3 c1 registers on page B1-149.
- B1.4 c2 registers on page B1-150.
- B1.5 c3 registers on page B1-151.
- B1.6 c4 registers on page B1-152.
- B1.7 c5 registers on page B1-153.
- B1.8 c6 registers on page B1-154.
- B1.9 c7 registers on page B1-155.
- B1.10 c7 system operations on page B1-156.
- B1.11 c8 system operations on page B1-159.
- B1.12 c9 registers on page B1-161.
- B1.13 c10 registers on page B1-162.
- B1.15 c12 registers on page B1-164.
- B1.16 c13 registers on page B1-166.
- B1.18 c15 registers on page B1-168.
- B1.19 64-bit registers on page B1-169.
- B1.21 AArch32 Virtual memory control registers on page B1-172.
- B1.23 AArch32 Other System control registers on page B1-174.
• B1.24 AArch32 Address registers on page B1-175.
• B1.25 AArch32 Thread registers on page B1-176.
• B1.26 AArch32 Performance monitor registers on page B1-177.
• B1.27 AArch32 Secure registers on page B1-179.
• B1.28 AArch32 Virtualization registers on page B1-180.
• B1.29 AArch32 GIC system registers on page B1-182.
• B1.30 AArch32 Generic Timer registers on page B1-184.
• B1.31 AArch32 Implementation defined registers on page B1-185.
• B1.32 Auxiliary Control Register on page B1-187.
• B1.33 Auxiliary Data Fault Status Register on page B1-189.
• B1.34 Auxiliary ID Register on page B1-190.
• B1.35 Auxiliary Instruction Fault Status Register on page B1-191.
• B1.36 Auxiliary Memory Attribute Indirection Register 0 on page B1-192.
• B1.37 Auxiliary Memory Attribute Indirection Register 1 on page B1-193.
• B1.38 Configuration Base Address Register on page B1-194.
• B1.40 Cache Level ID Register on page B1-198.
• B1.41 Architectural Feature Access Control Register on page B1-200.
• B1.43 CPU Extended Control Register on page B1-206.
• B1.44 CPU Memory Error Syndrome Register on page B1-208.
• B1.45 Cache Size Selection Register on page B1-211.
• B1.46 Cache Type Register on page B1-213.
• B1.47 Domain Access Control Register on page B1-215.
• B1.48 Data Fault Address Register on page B1-216.
• B1.49 Data Fault Status Register on page B1-217.
• B1.50 DFSR with Short-descriptor translation table format on page B1-218.
• B1.51 DFSR with Long-descriptor translation table format on page B1-220.
• B1.52 Encoding of ISS[24:20] when HSR[31:30] is 0b00 on page B1-222.
• B1.53 FCSE Process ID Register on page B1-223.
• B1.54 Hyp Auxiliary Configuration Register on page B1-224.
• B1.55 Hyp Auxiliary Control Register on page B1-225.
• B1.57 Hyp Auxiliary Instruction Fault Status Syndrome Register on page B1-228.
• B1.58 Hyp Auxiliary Memory Attribute Indirection Register 0 on page B1-229.
• B1.59 Hyp Auxiliary Memory Attribute Indirection Register 1 on page B1-230.
• B1.60 Hyp Architectural Feature Trap Register on page B1-231.
• B1.61 Hyp Configuration Register on page B1-234.
• B1.62 Hyp Configuration Register 2 on page B1-240.
• B1.64 Hyp Data Fault Address Register on page B1-245.
• B1.65 Hyp Instruction Fault Address Register on page B1-246.
• B1.66 Hyp IPA Fault Address Register on page B1-247.
• B1.67 Hyp System Control Register on page B1-248.
• B1.68 Hyp Syndrome Register on page B1-252.
• B1.69 Hyp System Trap Register on page B1-253.
• B1.70 Hyp Translation Control Register on page B1-257.
• B1.71 Hyp Vector Base Address Register on page B1-259.
• B1.72 Auxiliary Feature Register 0 on page B1-260.
• B1.73 Debug Feature Register 0 on page B1-261.
• B1.74 Instruction Set Attribute Register 0 on page B1-263.
• B1.75 Instruction Set Attribute Register 1 on page B1-265.
• B1.76 Instruction Set Attribute Register 2 on page B1-267.
• B1.77 Instruction Set Attribute Register 3 on page B1-269.
• B1.78 Instruction Set Attribute Register 4 on page B1-271.
• B1.79 Instruction Set Attribute Register 5 on page B1-273.
• B1.80 Memory Model Feature Register 0 on page B1-275.
• B1.81 Memory Model Feature Register 1 on page B1-277.
• B1.82 Memory Model Feature Register 2 on page B1-279.
• B1.83 Memory Model Feature Register 3 on page B1-281.
• B1.84 Processor Feature Register 0 on page B1-283.
• B1.85 Processor Feature Register 1 on page B1-285.
• B1.86 Instruction Fault Address Register on page B1-287.
• B1.87 Instruction Fault Status Register on page B1-288.
• B1.88 IFSR with Short-descriptor translation table format on page B1-289.
• B1.89 IFSR with Long-descriptor translation table format on page B1-291.
• B1.90 Interrupt Status Register on page B1-293.
• B1.91 L2 Auxiliary Control Register on page B1-295.
• B1.92 L2 Control Register on page B1-297.
• B1.93 L2 Extended Control Register on page B1-299.
• B1.94 L2 Memory Error Syndrome Register on page B1-301.
• B1.95 Memory Attribute Indirection Registers 0 and 1 on page B1-304.
• B1.96 Main ID Register on page B1-307.
• B1.97 Multiprocessor Affinity Register on page B1-309.
• B1.98 Non-Secure Access Control Register on page B1-311.
• B1.99 Normal Memory Remap Register on page B1-313.
• B1.100 Physical Address Register on page B1-315.
• B1.101 Primary Region Remap Register on page B1-316.
• B1.102 Revision ID Register on page B1-319.
• B1.103 Reset Management Register on page B1-320.
• B1.105 System Control Register on page B1-324.
• B1.106 Secure Debug Control Register on page B1-328.
• B1.108 TCM Type Register on page B1-331.
• B1.109 TLB Type Register on page B1-332.
• B1.110 Translation Table Base Control Register on page B1-333.
• B1.111 TTBCR with Short-descriptor translation table format on page B1-334.
• B1.112 TTBCR with Long-descriptor translation table format on page B1-335.
• B1.113 Translation Table Base Register 0 on page B1-338.
• B1.114 TTB0 with Short-descriptor translation table format on page B1-339.
• B1.115 TTB0 with Long-descriptor translation table format on page B1-341.
• B1.116 Translation Table Base Register 1 on page B1-342.
• B1.117 TTB1 with Short-descriptor translation table format on page B1-343.
• B1.118 TTB1 with Long-descriptor translation table format on page B1-345.
• B1.119 Vector Base Address Register on page B1-346.
• B1.120 Virtualization Multiprocessor ID Register on page B1-347.
• B1.121 Virtualization Processor ID Register on page B1-348.
• B1.122 Virtualization Translation Control Register on page B1-349.
B1.1 AArch32 register summary

In AArch32 state, you access the system registers through a conceptual coprocessor, identified as CP15, the System Control Coprocessor.

Within CP15, there is a top-level grouping of system registers by a primary coprocessor register number, c0-c15. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information about using the conceptual System Control Coprocessor in a VMSA context.

The system register space includes System operations system registers and System operations. The description of the system register space describes the permitted access, RO, WO, or RW, to each register or operation.

The following sections describe the CP15 system control registers grouped by CRn order, and are accessed by the MCR and MRC instructions.

- B1.2 c0 registers on page B1-146.
- B1.3 c1 registers on page B1-149.
- B1.4 c2 registers on page B1-150.
- B1.5 c3 registers on page B1-151.
- B1.6 c4 registers on page B1-152.
- B1.7 c5 registers on page B1-153.
- B1.8 c6 registers on page B1-154.
- B1.9 c7 registers on page B1-155.
- B1.10 c7 system operations on page B1-156.
- B1.11 c8 system operations on page B1-159.
- B1.12 c9 registers on page B1-161.
- B1.13 c10 registers on page B1-162.
- B1.15 c12 registers on page B1-164.
- B1.16 c13 registers on page B1-166.
- B1.18 c15 registers on page B1-168.

The following subsection describes the 64-bit registers and provides cross-references to individual register descriptions:

- B1.19 64-bit registers on page B1-169.

In addition to listing the CP15 system registers by CRn ordering, the following subsections describe the CP15 system registers by functional group:

- B1.21 AArch32 Virtual memory control registers on page B1-172.
- B1.23 AArch32 Other System control registers on page B1-174.
- B1.24 AArch32 Address registers on page B1-175.
- B1.26 AArch32 Performance monitor registers on page B1-177.
- B1.28 AArch32 Virtualization registers on page B1-180.
- B1.29 AArch32 GIC system registers on page B1-182.
- B1.31 AArch32 Implementation defined registers on page B1-185.

The following table describes the column headings in the CP15 register summary tables used throughout this section.
<table>
<thead>
<tr>
<th>Heading</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRn</td>
<td>System control primary register number.</td>
</tr>
<tr>
<td>Op1</td>
<td>Arguments to the register access instruction.</td>
</tr>
<tr>
<td>CRm</td>
<td></td>
</tr>
<tr>
<td>Op2</td>
<td></td>
</tr>
<tr>
<td>Name</td>
<td>The name of the register or operation. Some assemblers support aliases that you can use to access the registers and operations by name.</td>
</tr>
<tr>
<td>Reset</td>
<td>Reset value of register.</td>
</tr>
<tr>
<td>Description</td>
<td>Cross-reference to the register description.</td>
</tr>
</tbody>
</table>
B1.2 c0 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value zero are called c0 registers.
<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>MIDR</td>
<td>0x411FD010</td>
<td><em>B1.96 Main ID Register on page B1-307</em></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>CTR</td>
<td>Cache Type Register</td>
<td>0x84448004</td>
<td><em>B1.46 Cache Type Register on page B1-213</em></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>TCMTR</td>
<td>TCM Type Register</td>
<td>0x00000000</td>
<td><em>B1.108 TCM Type Register on page B1-331</em></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>TLBTR</td>
<td>TLB Type Register</td>
<td>0x00000000</td>
<td><em>B1.109 TLB Type Register on page B1-332</em></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>MIDR</td>
<td>Aliases of Main ID Register, <em>B1.96 Main ID Register on page B1-307</em></td>
<td>0x411FD010</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>MPIDR</td>
<td>Multiprocessor Affinity Register</td>
<td>-</td>
<td><em>B1.97 Multiprocessor Affinity Register on page B1-309</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value depends on the primary inputs, CLUSTERIDAFF1 and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CLUSTERIDAFF2, and the number of cores that the device implements.</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>REVIDR</td>
<td>Revision ID Register</td>
<td>0x00000000</td>
<td><em>B1.102 Revision ID Register on page B1-319</em></td>
</tr>
<tr>
<td>c1</td>
<td></td>
<td>ID_PFR0</td>
<td>Processor Feature Register 0</td>
<td>0x00000131</td>
<td><em>B1.84 Processor Feature Register 0 on page B1-283</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_PFR1</td>
<td>Processor Feature Register 1</td>
<td>0x10011011</td>
<td><em>B1.85 Processor Feature Register 1 on page B1-285</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Bits [31:28] are 0x1 if the GIC CPU interface is implemented and enabled, and</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0 otherwise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_DFR0</td>
<td>Debug Feature Register 0</td>
<td>0x03010066</td>
<td><em>B1.73 Debug Feature Register 0 on page B1-261</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Bits [19:16] are 0x1 if ETM is implemented, and 0x0 otherwise.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_AFR0</td>
<td>Auxiliary Feature Register 0</td>
<td>0x00000000</td>
<td><em>B1.72 Auxiliary Feature Register 0 on page B1-260</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_MMFR0</td>
<td>Memory Model Feature Register 0</td>
<td>0x10201105</td>
<td><em>B1.80 Memory Model Feature Register 0 on page B1-275</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_MMFR1</td>
<td>Memory Model Feature Register 1</td>
<td>0x40000000</td>
<td><em>B1.81 Memory Model Feature Register 1 on page B1-277</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_MMFR2</td>
<td>Memory Model Feature Register 2</td>
<td>0x01260000</td>
<td><em>B1.82 Memory Model Feature Register 2 on page B1-279</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_MMFR3</td>
<td>Memory Model Feature Register 3</td>
<td>0x02102211</td>
<td><em>B1.83 Memory Model Feature Register 3 on page B1-281</em></td>
</tr>
<tr>
<td>c2</td>
<td></td>
<td>ID_ISAR0</td>
<td>Instruction Set Attribute Register 0</td>
<td>0x02101110</td>
<td><em>B1.74 Instruction Set Attribute Register 0 on page B1-263</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_ISAR1</td>
<td>Instruction Set Attribute Register 1</td>
<td>0x13112111</td>
<td><em>B1.75 Instruction Set Attribute Register 1 on page B1-265</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_ISAR2</td>
<td>Instruction Set Attribute Register 2</td>
<td>0x21232042</td>
<td><em>B1.76 Instruction Set Attribute Register 2 on page B1-267</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_ISAR3</td>
<td>Instruction Set Attribute Register 3</td>
<td>0x011112131</td>
<td><em>B1.77 Instruction Set Attribute Register 3 on page B1-269</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_ISAR4</td>
<td>Instruction Set Attribute Register 4</td>
<td>0x00011142</td>
<td><em>B1.78 Instruction Set Attribute Register 4 on page B1-271</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID_ISAR5</td>
<td>Instruction Set Attribute Register 5</td>
<td>0x00011121</td>
<td><em>B1.79 Instruction Set Attribute Register 5 on page B1-273</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ID_ISAR5 has the value 0x00011121 if the Cryptographic Extension is not</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>implemented and enabled.</td>
</tr>
<tr>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Name</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>---------------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>1</td>
<td>c0</td>
<td>0</td>
<td>CCSIDR</td>
<td>-</td>
<td><em>B1.39 Cache Size ID Register</em> on page B1-195</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 CLIDR</td>
<td>0x0A200023</td>
<td><em>B1.40 Cache Level ID Register</em> on page B1-198</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>7 AIDR</td>
<td>0x00000000</td>
<td><em>B1.34 Auxiliary ID Register</em> on page B1-190</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value is 0x09200003 if the L2 cache is not implemented.</td>
</tr>
<tr>
<td>2</td>
<td>c0</td>
<td>0</td>
<td>CSSELR</td>
<td>0x00000000</td>
<td><em>B1.45 Cache Size Selection Register</em> on page B1-211</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>VPIDR</td>
<td>0x411FD010</td>
<td><em>B1.121 Virtualization Processor ID Register</em> on page B1-348</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>VMPIDR</td>
<td>-</td>
<td><em>B1.120 Virtualization Multiprocessor ID Register</em> on page B1-347</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value is the value of the Multiprocessor Affinity Register.</td>
</tr>
</tbody>
</table>
B1.3 c1 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value one are called c1 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c1.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>SCTLR</td>
<td>0x00C50838</td>
<td>B1.105 System Control Register on page B1-324</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value depends on inputs, CFGTE, CFGEND, and VINITHI. The value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>listed here assumes these signals are set to LOW.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>ACTLR</td>
<td>0x00000000</td>
<td>B1.32 Auxiliary Control Register on page B1-187</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>CPACR</td>
<td>0x00000000</td>
<td>B1.41 Architectural Feature Access Control Register on page B1-200</td>
</tr>
<tr>
<td>c1</td>
<td>0</td>
<td></td>
<td>SCR</td>
<td>0x00000000</td>
<td>B1.104 Secure Configuration Register on page B1-321</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>SDER</td>
<td>0x00000000</td>
<td>B1.107 Secure Debug Enable Register on page B1-330</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>NSACR</td>
<td>0x00000000</td>
<td>B1.98 Non-Secure Access Control Register on page B1-311</td>
</tr>
<tr>
<td>c3</td>
<td>1</td>
<td></td>
<td>SDCR</td>
<td>0x00000000</td>
<td>B1.106 Secure Debug Control Register on page B1-328</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>HSCTLR</td>
<td>0x03C50838</td>
<td>B1.67 Hyp System Control Register on page B1-248</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>HACTLR</td>
<td>0x00000000</td>
<td>B1.55 Hyp Auxiliary Control Register on page B1-225</td>
</tr>
<tr>
<td>c1</td>
<td>0</td>
<td></td>
<td>HCR</td>
<td>0x00000000</td>
<td>B1.61 Hyp Configuration Register on page B1-234</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>HDCR</td>
<td>0x00000006</td>
<td>B1.63 Hyp Debug Control Register on page B1-242</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>HCPTR</td>
<td>0x0000033FF</td>
<td>B1.60 Hyp Architectural Feature Trap Register on page B1-231</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value depends on the FPU and NEON configuration. If Advanced SIMD</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>and floating-point are implemented, the reset value is 0x0000033FF. If</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Advanced SIMD and floating-point are not implemented, the reset value is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00000BFFF.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>HSTR</td>
<td>0x00000000</td>
<td>B1.69 Hyp System Trap Register on page B1-253</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>HCR2</td>
<td>0x00000000</td>
<td>B1.62 Hyp Configuration Register 2 on page B1-240</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>HACR</td>
<td>0x00000000</td>
<td>B1.54 Hyp Auxiliary Configuration Register on page B1-224</td>
</tr>
</tbody>
</table>
B1.4 c2 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value two are called c2 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c2.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>TTBR0</td>
<td>UNK</td>
<td>B1.113 Translation Table Base Register 0 on page B1-338</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>1</td>
<td>TTBR1</td>
<td>UNK</td>
<td>B1.116 Translation Table Base Register 1 on page B1-342</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>2</td>
<td>TTBCR</td>
<td>0x00000000</td>
<td>B1.110 Translation Table Base Control Register on page B1-333</td>
</tr>
<tr>
<td></td>
<td>c0</td>
<td>4</td>
<td>HTCR</td>
<td>UNK</td>
<td>B1.70 Hyp Translation Control Register on page B1-257</td>
</tr>
<tr>
<td></td>
<td>c1</td>
<td>2</td>
<td>VTCR</td>
<td>UNK</td>
<td>B1.122 Virtualization Translation Control Register on page B1-349</td>
</tr>
</tbody>
</table>

The reset value is 0x00000000 for the Secure copy of the register. The reset value for the EAE bit of the Non-secure copy of the register is 0x0. You must program the Non-secure copy of the register with the required initial value, as part of the processor boot sequence.
B1.5  c3 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value three are called c3 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c3.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>DACR</td>
<td>UNK</td>
<td>B1.47 Domain Access Control Register on page B1-215</td>
</tr>
</tbody>
</table>
B1.6  c4 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value four are called c4 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c4.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c6</td>
<td>0</td>
<td>ICC_PMR</td>
<td>0x00000000</td>
<td>Priority Mask Register</td>
</tr>
</tbody>
</table>

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Non-Confidential
B1.7 c5 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value five are called c5 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c5.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>DFSR</td>
<td>UNK</td>
<td>B1.49 Data Fault Status Register on page B1-217</td>
</tr>
<tr>
<td>1</td>
<td>IFSR</td>
<td>UNK</td>
<td>B1.87 Instruction Fault Status Register on page B1-288</td>
<td></td>
<td></td>
</tr>
<tr>
<td>c1</td>
<td>ADFSR</td>
<td>0x00000000</td>
<td>B1.33 Auxiliary Data Fault Status Register on page B1-189</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>AIFSR</td>
<td>0x00000000</td>
<td>B1.35 Auxiliary Instruction Fault Status Register on page B1-191</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>HADFSR</td>
<td>0x00000000</td>
<td>B1.56 Hyp Auxiliary Data Fault Status Syndrome Register on page B1-227</td>
</tr>
<tr>
<td></td>
<td>HAIFSR</td>
<td>0x00000000</td>
<td>B1.57 Hyp Auxiliary Instruction Fault Status Syndrome Register on page B1-228</td>
<td></td>
<td></td>
</tr>
<tr>
<td>c2</td>
<td>HSR</td>
<td>UNK</td>
<td>B1.68 Hyp Syndrome Register on page B1-252</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### B1.8 c6 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value six are called c6 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c6.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>DFAR</td>
<td>UNK</td>
<td>B1.48 Data Fault Address Register on page B1-216</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>IFAR</td>
<td>UNK</td>
<td>B1.86 Instruction Fault Address Register on page B1-287</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>HDFAR</td>
<td>UNK</td>
<td>B1.64 Hyp Data Fault Address Register on page B1-245</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>HIFAR</td>
<td>UNK</td>
<td>B1.65 Hyp Instruction Fault Address Register on page B1-246</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>HPFAR</td>
<td>UNK</td>
<td>B1.66 Hyp IPA Fault Address Register on page B1-247</td>
</tr>
</tbody>
</table>
B1.9  c7 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value seven are called c7 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c7.

Table B1-9  c7 register summary

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c4</td>
<td>0</td>
<td>PAR</td>
<td>UNK</td>
<td><strong>B1.100 Physical Address Register on page B1-315</strong></td>
</tr>
</tbody>
</table>
B1.10 c7 system operations

System operations are divided into two categories. When the CRn value is c7, these operations are called c7 system operations.

The following table shows the System operations when CRn is c7 and the processor is in AArch32 state. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile. for more information about these operations.
Table B1-10  c7 System operation summary

<table>
<thead>
<tr>
<th>op1</th>
<th>CRm</th>
<th>op2</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c1</td>
<td>0</td>
<td>ICIALLUIS</td>
<td>Invalidate all instruction caches Inner Shareable to PoU</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PoU = Point of Unification. PoU is set by the BROADCASTINNER signal and can be in the L1 data cache or outside of the processor, in which case PoU is dependent on the external memory system.</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>BPIALLIS</td>
<td>Invalidate all entries from branch predictors Inner Shareable</td>
</tr>
<tr>
<td>c5</td>
<td>0</td>
<td></td>
<td>ICIALLU</td>
<td>Invalidate all Instruction Caches to PoU</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>ICIMVAU</td>
<td>Invalidate Instruction Caches by VA to PoU</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>CP15ISB</td>
<td>Instruction Synchronization Barrier operation, this operation is deprecated in Armv8-A</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>BPIALL</td>
<td>Invalidate all entries from branch predictors</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>BPIIMVA</td>
<td>Invalidate VA from branch predictors</td>
</tr>
<tr>
<td>c6</td>
<td>1</td>
<td></td>
<td>DCIMVAC</td>
<td>Invalidate data cache line by VA to PoC</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PoC = Point of Coherence. The PoC is always outside of the processor and is dependent on the external memory system.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>DCISW</td>
<td>Invalidate data cache line by set/way</td>
<td></td>
</tr>
<tr>
<td>c8</td>
<td>0</td>
<td></td>
<td>ATS1CPR</td>
<td>Stage 1 current state PL1 read</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>ATS1CPW</td>
<td>Stage 1 current state PL1 write</td>
<td></td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>ATS1CUR</td>
<td>Stage 1 current state unprivileged read</td>
<td></td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>ATS1CUW</td>
<td>Stage 1 current state unprivileged write</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>ATS12NSOPR</td>
<td>Stages 1 and 2 Non-secure only PL1 read</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>ATS12NSOPW</td>
<td>Stages 1 and 2 Non-secure only PL1 write</td>
<td></td>
</tr>
<tr>
<td></td>
<td>6</td>
<td>ATS12NSOUR</td>
<td>Stages 1 and 2 Non-secure only unprivileged read</td>
<td></td>
</tr>
<tr>
<td></td>
<td>7</td>
<td>ATS12NSOUW</td>
<td>Stages 1 and 2 Non-secure only unprivileged write</td>
<td></td>
</tr>
<tr>
<td>c10</td>
<td>1</td>
<td></td>
<td>DCCMVAC</td>
<td>Clean data cache line by VA to PoC</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>DCCSW</td>
<td>Clean data cache line by set/way</td>
<td></td>
</tr>
<tr>
<td></td>
<td>4</td>
<td>CP15DSB</td>
<td>Data Synchronization Barrier operation, this operation is deprecated in Armv8-A</td>
<td></td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>CP15DMB</td>
<td>Data Memory Barrier operation, this operation is deprecated in Armv8-A</td>
<td></td>
</tr>
<tr>
<td>c11</td>
<td>1</td>
<td></td>
<td>DCCMVAU</td>
<td>Clean data cache line by VA to PoU</td>
</tr>
<tr>
<td>c14</td>
<td>1</td>
<td></td>
<td>DCCIMVAC</td>
<td>Clean and invalidate data cache line by VA to PoC</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>DCCISW</td>
<td>Clean and invalidate data cache line by set/way</td>
<td></td>
</tr>
</tbody>
</table>
Table B1-10  c7 System operation summary (continued)

<table>
<thead>
<tr>
<th>op1</th>
<th>CRm</th>
<th>op2</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>c8</td>
<td>0</td>
<td>ATS1HR</td>
<td>Stage 1 Hyp mode read</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>ATS1HW</td>
<td>Stage 1 Hyp mode write</td>
</tr>
</tbody>
</table>
B1.11  c8 system operations

System operations are divided into two categories. When the CRn value is c8, these operations are called c8 system operations.

The following table shows the System operations when CRn is c8 and the processor is in AArch32 state. See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information about these operations.

Table B1-11  c8 System operations summary

<table>
<thead>
<tr>
<th>op1</th>
<th>CRm</th>
<th>op2</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c3</td>
<td>0</td>
<td>TLBIALLIS</td>
<td>Invalidate entire TLB Inner Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>TLBIMVAIS</td>
<td>Invalidate unified TLB entry by VA and ASID Inner Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>TLBIASIDIS</td>
<td>Invalidate unified TLB by ASID match Inner Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>TLBIMVAIS</td>
<td>Invalidate unified TLB entry by VA all ASID Inner Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>TLBIMVALIS</td>
<td>Invalidate unified TLB entry by VA Inner Shareable, Last level</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>TLBIMVAALIS</td>
<td>Invalidate unified TLB by VA all ASID Inner Shareable, Last level</td>
</tr>
<tr>
<td></td>
<td>c5</td>
<td>0</td>
<td>ITLBIALL</td>
<td>Invalidate instruction TLB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>ITLBIMVA</td>
<td>Invalidate instruction TLB entry by VA and ASID</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>ITLBIASID</td>
<td>Invalidate instruction TLB by ASID match</td>
</tr>
<tr>
<td></td>
<td>c6</td>
<td>0</td>
<td>DTLBIALL</td>
<td>Invalidate data TLB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>DTLBIMVA</td>
<td>Invalidate data TLB entry by VA and ASID</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>DTLBIASID</td>
<td>Invalidate data TLB by ASID match</td>
</tr>
<tr>
<td></td>
<td>c7</td>
<td>0</td>
<td>TLBIALL</td>
<td>Invalidate unified TLB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>TLBIMVA</td>
<td>Invalidate unified TLB by VA and ASID</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>TLBIASID</td>
<td>Invalidate unified TLB by ASID match</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>TLBIMVAA</td>
<td>Invalidate unified TLB entries by VA all ASID</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>TLBIMVAL</td>
<td>Invalidate last level of stage 1 TLB entry by VA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>TLBIMVAAL</td>
<td>Invalidate last level of stage 1 TLB entry by VA all ASID</td>
</tr>
<tr>
<td>op1</td>
<td>CRm</td>
<td>op2</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>---------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>1</td>
<td>TLBIIPAS2IS</td>
<td>TLB Invalidate entry by Intermediate Physical Address, Stage 2, Inner Shareable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>TLBIIPAS2LIS</td>
<td>TLB Invalidate entry by Intermediate Physical Address, Stage 2, Last level, Inner Shareable</td>
</tr>
<tr>
<td>c3</td>
<td>0</td>
<td></td>
<td>TLBIALLHIS</td>
<td>Invalidate entire Hyp unified TLB Inner Shareable</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>TLBIMVAHIS</td>
<td>Invalidate Hyp unified TLB entry by VA Inner Shareable</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
<td>TLBIALLNSNHIS</td>
<td>Invalidate entire Non-secure non-Hyp unified TLB Inner Shareable</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td></td>
<td>TLBIMVALHIS</td>
<td>Invalidate Unified Hyp TLB entry by VA Inner Shareable, Last level</td>
</tr>
<tr>
<td>c4</td>
<td>1</td>
<td></td>
<td>TLBIIPAS2</td>
<td>TLB Invalidate entry by Intermediate Physical Address, Stage 2</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td></td>
<td>TLBIIPAS2L</td>
<td>TLB Invalidate entry by Intermediate Physical Address, Stage 2, Last level</td>
</tr>
<tr>
<td>c7</td>
<td>0</td>
<td></td>
<td>TLBIALLH</td>
<td>Invalidate entire Hyp unified TLB</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>TLBIMVAH</td>
<td>Invalidate Hyp unified TLB entry by VA</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
<td>TLBIALLNSNH</td>
<td>Invalidate entire Non-secure non-Hyp unified TLB</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td></td>
<td>TLBIMVALH</td>
<td>Invalidate Unified Hyp TLB entry by VA, Last level</td>
</tr>
</tbody>
</table>
### B1.12 c9 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value nine are called c9 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c9. See the *Arm*® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c12</td>
<td>0</td>
<td>PMCR</td>
<td>0x41063000</td>
<td>Performance Monitors Control Register</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>PMNCNTEST</td>
<td>UNK</td>
<td>Performance Monitors Count Enable Set Register</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>PMNCNTEST</td>
<td>UNK</td>
<td>Performance Monitors Count Enable Clear Register</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>PMOVSR</td>
<td>UNK</td>
<td>Performance Monitor Overflow Flag Status Clear Register</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>PMSWINC</td>
<td>UNK</td>
<td>Performance Monitors Software Increment Register</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>PMSELR</td>
<td>UNK</td>
<td>Performance Monitors Event Counter Selection Register</td>
<td></td>
</tr>
</tbody>
</table>
| 6   |     | PMCEID0   | 0x6FFFFF00 | C9.3 Performance Monitors Common Event Identification Register 0 on page C9-477  
   |     |          |      | The reset value is 0x6E3FBFFF if L2 cache is not implemented. |
| 7   |     | PMCEID1   | 0x00000000 | C9.4 Performance Monitors Common Event Identification Register 1 on page C9-481 |
| c13 |     | 0     | PMCCNTR      | UNK       | Performance Monitors Cycle Counter                           |
|     |     | 1     | PMXEVTYPER   | UNK       | Performance Monitors Selected Event Type and Filter Register  |
|     |     | 2     | PMXEVCNTR    | UNK       | Performance Monitors Selected Event Counter Register         |
| c14 |     | 0     | PMUSERENR    | 0x00000000 | Performance Monitors User Enable Register                    |
|     |     | 1     | PMINTENSET   | UNK       | Performance Monitors Interrupt Enable Set Register           |
|     |     | 2     | PMINTENCLR   | UNK       | Performance Monitors Interrupt Enable Clear Register         |
|     |     | 3     | PMOVSSSET    | UNK       | Performance Monitor Overflow Flag Status Set Register        |
| 1   | c0  | 2     | L2CTLR       | -         | *B1.92 L2 Control Register on page B1-297*                  
   |     |      |              |           | The reset value depends on the processor configuration.        |
|     |     | 3     | L2ECTLR      | 0x00000000 | *B1.93 L2 Extended Control Register on page B1-299*          |
B1.13 c10 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value ten are called c10 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c10.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c2</td>
<td>0</td>
<td>PRRR</td>
<td>UNK</td>
<td><strong>B1.101 Primary Region Remap Register</strong> on page B1-316</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>0</td>
<td>MAIR0</td>
<td>UNK</td>
<td><strong>B1.95 Memory Attribute Indirection Registers 0 and 1</strong> on page B1-304</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0</td>
<td>NMRR</td>
<td>UNK</td>
<td><strong>B1.99 Normal Memory Remap Register</strong> on page B1-313</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0</td>
<td>MAIR1</td>
<td>UNK</td>
<td><strong>B1.95 Memory Attribute Indirection Registers 0 and 1</strong> on page B1-304</td>
</tr>
<tr>
<td>c3</td>
<td></td>
<td>0</td>
<td>AMAIR0</td>
<td>0x00000000</td>
<td><strong>B1.36 Auxiliary Memory Attribute Indirection Register 0</strong> on page B1-192</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0</td>
<td>AMAIR1</td>
<td>0x00000000</td>
<td><strong>B1.37 Auxiliary Memory Attribute Indirection Register 1</strong> on page B1-193</td>
</tr>
<tr>
<td>4</td>
<td>c2</td>
<td>0</td>
<td>HMAIR0</td>
<td>UNK</td>
<td>Hyp Memory Attribute Indirection Register 0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>HMAIR1</td>
<td>UNK</td>
<td>Hyp Memory Attribute Indirection Register 1</td>
</tr>
<tr>
<td>c3</td>
<td></td>
<td>0</td>
<td>HAMAIR0</td>
<td>0x00000000</td>
<td><strong>B1.58 Hyp Auxiliary Memory Attribute Indirection Register 0</strong> on page B1-229</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>0</td>
<td>HAMAIR1</td>
<td>0x00000000</td>
<td><strong>B1.59 Hyp Auxiliary Memory Attribute Indirection Register 1</strong> on page B1-230</td>
</tr>
</tbody>
</table>

See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.
B1.14 c11 registers

There are no system registers to access when the processor is in AArch32 state and the value of CRn is 11.
B1.15  c12 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value twelve are called c12 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c12.

### Table B1-14  c12 register summary

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>VBAR</td>
<td>0x00000000</td>
<td>B1.119 Vector Base Address Register on page B1-346.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00000000 is the secure reset value and UNK is the non-secure reset value.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>MVBAR</td>
<td>UNK</td>
<td>Monitor Vector Base Address Register. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>RMR</td>
<td>0x00000000</td>
<td>B1.103 Reset Management Register on page B1-320.</td>
</tr>
<tr>
<td>c1</td>
<td>0</td>
<td></td>
<td>ISR</td>
<td>UNK</td>
<td>B1.90 Interrupt Status Register on page B1-293.</td>
</tr>
<tr>
<td>c8</td>
<td>0</td>
<td></td>
<td>ICC_IAR0</td>
<td>-</td>
<td>Interrupt Acknowledge Register 0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>ICC_EOIR0</td>
<td>-</td>
<td>End Of Interrupt Register 0</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>ICC_HPPR0</td>
<td>-</td>
<td>Highest Priority Pending Interrupt Register 0</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICC_BPR0</td>
<td>0x00000002</td>
<td>Binary Point Register 0</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
<td>ICC_AP0R0</td>
<td>0x00000000</td>
<td>Active Priorities 0 Register 0</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td></td>
<td>ICC_AP1R0</td>
<td>0x00000000</td>
<td>Active Priorities 1 Register 0</td>
</tr>
<tr>
<td>c11</td>
<td>1</td>
<td></td>
<td>ICC_DIR</td>
<td>-</td>
<td>Deactivate Interrupt Register</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICC_RPR</td>
<td>-</td>
<td>Running Priority Register</td>
</tr>
<tr>
<td>c12</td>
<td>0</td>
<td></td>
<td>ICC_IAR1</td>
<td>-</td>
<td>Interrupt Acknowledge Register 1</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>ICC_EOIR1</td>
<td>-</td>
<td>End Of Interrupt Register 1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>ICC_HPPR1</td>
<td>-</td>
<td>Highest Priority Pending Interrupt Register 1</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICC_BPR1</td>
<td>0x00000003</td>
<td>Binary Point Register 1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>This is the reset value in non-secure state. In secure state, the reset value is 0x00000002.</td>
</tr>
<tr>
<td></td>
<td>4</td>
<td></td>
<td>ICC_CTLR</td>
<td>0x00000040</td>
<td>Interrupt Control Register</td>
</tr>
<tr>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Name</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>---------------------</td>
<td>-----------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>HVBAR</td>
<td>UNK</td>
<td><em>B1.71 Hyp Vector Base Address Register on page B1-259.</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ICH_AP0R0</td>
<td>0x00000000</td>
<td>Interrupt Controller Hyp Active Priorities Register (0,0)</td>
</tr>
<tr>
<td></td>
<td>c8</td>
<td>0</td>
<td>ICH_AP1R0</td>
<td>0x00000000</td>
<td>Interrupt Controller Hyp Active Priorities Register (1,0)</td>
</tr>
<tr>
<td></td>
<td>c9</td>
<td>0</td>
<td>ICH_VSEIR</td>
<td>0x00000000</td>
<td>Interrupt Controller Virtual System Error Interrupt Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ICC_HSRE</td>
<td>0x00000000</td>
<td>System Register Enable Register for EL2</td>
</tr>
<tr>
<td>c11</td>
<td>0</td>
<td></td>
<td>ICH_HCR</td>
<td>0x00000000</td>
<td>Interrupt Controller Hyp Control Register</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>ICH_VTR</td>
<td>0x90000003</td>
<td>Interrupt Controller VGIC Type Register</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>ICH_MISR</td>
<td>0x00000000</td>
<td>Interrupt Controller Maintenance Interrupt State Register</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICH_EISR</td>
<td>0x00000000</td>
<td>Interrupt Controller End of Interrupt Status Register</td>
</tr>
<tr>
<td></td>
<td>7</td>
<td></td>
<td>ICH_VMCR</td>
<td>0x004C0000</td>
<td>Interrupt Controller Virtual Machine Control Register</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td></td>
<td>ICH_ELRSR</td>
<td>0x0000000F</td>
<td>Interrupt Controller Empty List Register Status Register</td>
</tr>
<tr>
<td>c12</td>
<td>0</td>
<td></td>
<td>ICH_LR0</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>ICH_LR1</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>ICH_LR2</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 2</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICH_LR3</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 3</td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td></td>
<td>ICH_LRC0</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 0</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td></td>
<td>ICH_LRC1</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 1</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td></td>
<td>ICH_LRC2</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 2</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td></td>
<td>ICH_LRC3</td>
<td>0x00000000</td>
<td>Interrupt Controller List Register 3</td>
</tr>
<tr>
<td>6</td>
<td>c12</td>
<td>4</td>
<td>ICC_MCTLR</td>
<td>0x00000040</td>
<td>Interrupt Control Register for EL3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>ICC_MSRE</td>
<td>0x00000000</td>
<td>System Register Enable Register for EL3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>7</td>
<td>ICC_MGRPEN1</td>
<td>0x00000000</td>
<td>Interrupt Controller Monitor Interrupt Group 1 Enable register</td>
</tr>
</tbody>
</table>
The processor can access different 32-bit wide system registers. Registers where CRn has the value thirteen are called c13 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c13.

For information on all registers but FCSE Process ID, see the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>FCSEIDR</td>
<td>0x00000000</td>
<td>B1.53 FCSE Process ID Register on page B1-223</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>UNK</td>
<td>CONTEXTIDR</td>
<td>UNK</td>
<td>Context ID Register</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>UNK</td>
<td>TPIDRURW</td>
<td>UNK</td>
<td>User Read/Write Thread ID Register</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>UNK</td>
<td>TPIDRURO</td>
<td>UNK</td>
<td>User Read-Only Thread ID Register</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>TPIDRPRW</td>
<td>UNK</td>
<td>EL1 only Thread ID Register</td>
</tr>
<tr>
<td>4</td>
<td>c0</td>
<td>2</td>
<td>HTPIDR</td>
<td>UNK</td>
<td>Hyp Software Thread ID Register</td>
</tr>
</tbody>
</table>
The processor can access different 32-bit wide system registers. Registers where CRn has the value fourteen are called c14 registers.

The following table shows the CP15 system registers when the processor is in AArch32 state and the value of CRn is c14. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>CNTFRQ</td>
<td>UNK</td>
<td>Timer Counter Frequency Register</td>
</tr>
<tr>
<td></td>
<td>c1</td>
<td>0</td>
<td>CNTKCTL</td>
<td>-</td>
<td>Timer Control Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value for bits[9:8, 2:0] is 0b0000000.</td>
</tr>
<tr>
<td>c2</td>
<td></td>
<td>0</td>
<td>CNTP_TV_AL</td>
<td>UNK</td>
<td>Physical Timer Value Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>CNTP_CTL</td>
<td>-</td>
<td>Physical Timer Control Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value for bit[0] is 0.</td>
</tr>
<tr>
<td>c3</td>
<td></td>
<td>0</td>
<td>CNTV_TV_AL</td>
<td>UNK</td>
<td>Virtual Timer TimerValue Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>CNTV_CTL</td>
<td>-</td>
<td>Counter-timer Virtual Timer Control Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value for bit[0] is 0.</td>
</tr>
<tr>
<td>c8</td>
<td></td>
<td>0</td>
<td>PMEVCNTR0</td>
<td>UNK</td>
<td>Performance Monitor Event Count Registers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>PMEVCNTR1</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>PMEVCNTR2</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>PMEVCNTR3</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>PMEVCNTR4</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>PMEVCNTR5</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>c12</td>
<td></td>
<td>0</td>
<td>PMEVTYPEP0</td>
<td>UNK</td>
<td>Performance Monitor Event Type Registers</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>PMEVTYPEP1</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>PMEVTYPEP2</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3</td>
<td>PMEVTYPEP3</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4</td>
<td>PMEVTYPEP4</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5</td>
<td>PMEVTYPEP5</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>c15</td>
<td></td>
<td>7</td>
<td>PMCCFILTR</td>
<td>0x00000000</td>
<td>Performance Monitor Cycle Count Filter Register.</td>
</tr>
<tr>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>CNTHCTL</td>
<td>-</td>
<td>Timer Control Register (EL2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value for bit[2] is 0 and for bits[1:0] is 0b11.</td>
</tr>
<tr>
<td>c2</td>
<td></td>
<td>0</td>
<td>CNTHP_TV_AL</td>
<td>UNK</td>
<td>Physical Timer TimerValue (EL2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>CNTHP_CTL</td>
<td>-</td>
<td>Physical Timer Control Register (EL2)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value for bit[0] is 0.</td>
</tr>
</tbody>
</table>
## B1.18 c15 registers

The processor can access different 32-bit wide system registers. Registers where CRn has the value fifteen are called c15 registers.

The following table shows the 32-bit wide system registers you can access when the processor is in AArch32 state and the value of CRn is c15.

### Table B1-17 c15 register summary

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>c0</td>
<td>0</td>
<td>L2ACTLR</td>
<td>0x80000000</td>
<td><em>B1.91 L2 Auxiliary Control Register on page B1-295</em>&lt;br&gt;This is the reset value for an ACE interface. For an AXI interface the reset value is 0x80000008. For a CHI interface the reset value is 0x80004008.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>c3</td>
<td>CBAR</td>
<td></td>
<td><em>B1.38 Configuration Base Address Register on page B1-194</em>&lt;br&gt;The reset value depends on the processor configuration.</td>
</tr>
<tr>
<td>3</td>
<td>c0</td>
<td>0</td>
<td>CDBGDR0</td>
<td>UNK</td>
<td>Cache Debug Data Register 0, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGDR1</td>
<td>UNK</td>
<td>Cache Debug Data Register 1, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGDR2</td>
<td>UNK</td>
<td>Cache Debug Data Register 2, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGDR3</td>
<td>UNK</td>
<td>Cache Debug Data Register 3, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td>c2</td>
<td>0</td>
<td>CDBGDCT</td>
<td>UNK</td>
<td>Cache Debug Data Cache Tag Read Operation Register, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGICT</td>
<td>UNK</td>
<td>Cache Debug Instruction Cache Tag Read Operation Register, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td>c4</td>
<td>0</td>
<td>CDBGDCD</td>
<td>UNK</td>
<td>Cache Debug Cache Debug Data Cache Data Read Operation Register, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGICD</td>
<td>UNK</td>
<td>Cache Debug Instruction Cache Data Read Operation Register, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CDBGTD</td>
<td>UNK</td>
<td>Cache Debug TLB Data Read Operation Register, see <em>C5.1 About direct access to internal memory on page C5-398</em></td>
</tr>
</tbody>
</table>
**B1.19 64-bit registers**

The processor can access 64-bit wide CP15 system registers in AArch32 state.

The following table shows the 64-bit wide CP15 system registers, accessed by the MCRR and MRRC instructions. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

<table>
<thead>
<tr>
<th>Op1</th>
<th>CRm</th>
<th>Name</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>c2</td>
<td>TTBR0</td>
<td>UNK</td>
<td>Translation Table Base Register 0</td>
</tr>
<tr>
<td>1</td>
<td>c2</td>
<td>TTBR1</td>
<td>UNK</td>
<td>Translation Table Base Register 1</td>
</tr>
<tr>
<td>4</td>
<td>c2</td>
<td>HTTBR</td>
<td>UNK</td>
<td>Hyp Translation Table Base Register</td>
</tr>
<tr>
<td>6</td>
<td>c2</td>
<td>VTTBR</td>
<td>UNK</td>
<td>Virtualization Translation Table Base Register</td>
</tr>
<tr>
<td>0</td>
<td>c7</td>
<td>PAR</td>
<td>UNK</td>
<td>B1.100 Physical Address Register on page B1-315</td>
</tr>
<tr>
<td>0</td>
<td>c14</td>
<td>CNTPCT</td>
<td>UNK</td>
<td>Physical Timer Count Register</td>
</tr>
<tr>
<td>1</td>
<td>c14</td>
<td>CNTVCT</td>
<td>UNK</td>
<td>Virtual Timer Count Register</td>
</tr>
<tr>
<td>2</td>
<td>c14</td>
<td>CNTP_CVAL</td>
<td>UNK</td>
<td>Physical Timer CompareValue Register</td>
</tr>
<tr>
<td>3</td>
<td>c14</td>
<td>CNTV_CVAL</td>
<td>UNK</td>
<td>Virtual Timer CompareValue Register</td>
</tr>
<tr>
<td>4</td>
<td>c14</td>
<td>CNTVOFF</td>
<td>UNK</td>
<td>Virtual Timer Offset Register</td>
</tr>
<tr>
<td>6</td>
<td>c14</td>
<td>CNTHP_CVAL</td>
<td>UNK</td>
<td>Physical Timer CompareValue Register</td>
</tr>
<tr>
<td>0</td>
<td>c15</td>
<td>CPUACTLR</td>
<td>0x0000000000000000</td>
<td>B1.42 CPU Auxiliary Control Register on page B1-202</td>
</tr>
<tr>
<td>1</td>
<td>c15</td>
<td>CPUECTLR</td>
<td>0x0000000000000000</td>
<td>B1.43 CPU Extended Control Register on page B1-206</td>
</tr>
<tr>
<td>2</td>
<td>c15</td>
<td>CPUMERRSR</td>
<td>-</td>
<td>B1.44 CPU Memory Error Syndrome Register on page B1-208</td>
</tr>
<tr>
<td>3</td>
<td>c15</td>
<td>L2MERRSR</td>
<td>-</td>
<td>B1.94 L2 Memory Error Syndrome Register on page B1-301</td>
</tr>
</tbody>
</table>
# B1.20 AArch32 Identification registers

The following table shows the identification registers.

## Table B1-19 Identification registers

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MIDR</td>
<td>c0</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>0x411FD010</td>
<td>B1.96 Main ID Register on page B1-307</td>
</tr>
<tr>
<td>CTR</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0x84448004</td>
<td>B1.46 Cache Type Register on page B1-213</td>
</tr>
<tr>
<td>TCMTR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>0x00000000</td>
<td>B1.108 TCM Type Register on page B1-331</td>
</tr>
<tr>
<td>TLBTR</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>0x00000000</td>
<td>B1.109 TLB Type Register on page B1-332</td>
</tr>
<tr>
<td>MPIDR</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>B1.97 Multiprocessor Affinity Register on page B1-309</td>
</tr>
<tr>
<td>REVIDR</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>B1.102 Revision ID Register on page B1-319</td>
</tr>
<tr>
<td>ID_PFR0</td>
<td>c1</td>
<td>0</td>
<td></td>
<td>0</td>
<td>0x00000131</td>
<td>B1.84 Processor Feature Register 0 on page B1-283</td>
</tr>
<tr>
<td>ID_PFR1</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0x10011111</td>
<td>B1.85 Processor Feature Register 1 on page B1-285</td>
</tr>
<tr>
<td>ID_DFR0</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>0x03010066</td>
<td>B1.73 Debug Feature Register 0 on page B1-261</td>
</tr>
<tr>
<td>ID_AFR0</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>0x00000000</td>
<td>B1.72 Auxiliary Feature Register 0 on page B1-260</td>
</tr>
<tr>
<td>ID_MMFR0</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>0x10201105</td>
<td>B1.80 Memory Model Feature Register 0 on page B1-275</td>
</tr>
<tr>
<td>ID_MMFR1</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>0x40000000</td>
<td>B1.81 Memory Model Feature Register 1 on page B1-277</td>
</tr>
<tr>
<td>ID_MMFR2</td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>0x81260000</td>
<td>B1.82 Memory Model Feature Register 2 on page B1-279</td>
</tr>
<tr>
<td>ID_MMFR3</td>
<td></td>
<td></td>
<td></td>
<td>7</td>
<td>0x02102211</td>
<td>B1.83 Memory Model Feature Register 3 on page B1-281</td>
</tr>
<tr>
<td>ID_ISAR0</td>
<td>c2</td>
<td>0</td>
<td></td>
<td>0</td>
<td>0x02101110</td>
<td>B1.74 Instruction Set Attribute Register 0 on page B1-263</td>
</tr>
<tr>
<td>ID_ISAR1</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0x13112111</td>
<td>B1.75 Instruction Set Attribute Register 1 on page B1-265</td>
</tr>
<tr>
<td>ID_ISAR2</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>0x21232042</td>
<td>B1.76 Instruction Set Attribute Register 2 on page B1-267</td>
</tr>
<tr>
<td>ID_ISAR3</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>0x81112113</td>
<td>B1.77 Instruction Set Attribute Register 3 on page B1-269</td>
</tr>
<tr>
<td>ID_ISAR4</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>0x00011142</td>
<td>B1.78 Instruction Set Attribute Register 4 on page B1-271</td>
</tr>
<tr>
<td>Name</td>
<td>CRn</td>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>---------</td>
<td>----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>ID_ISAR5</td>
<td>c0</td>
<td>0</td>
<td>c2</td>
<td>5</td>
<td>0x00011121</td>
<td><a href="#">B1.79 Instruction Set Attribute Register 5</a> on page B1-273</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ID_ISAR5 has the value 0x00010001 if the Cryptographic Extension is not</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>implemented and enabled.</td>
</tr>
<tr>
<td>CCSIDR</td>
<td>1</td>
<td>c0</td>
<td>0</td>
<td>-</td>
<td></td>
<td><a href="#">B1.39 Cache Size ID Register</a> on page B1-195</td>
</tr>
<tr>
<td>CLIDR</td>
<td>1</td>
<td>0</td>
<td>0x0A200023</td>
<td></td>
<td></td>
<td><a href="#">B1.40 Cache Level ID Register</a> on page B1-198</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The value is 0x09200003 if the L2 cache is not implemented.</td>
</tr>
<tr>
<td>AIDR</td>
<td>7</td>
<td>0x00000000</td>
<td>0x00000000</td>
<td></td>
<td></td>
<td><a href="#">B1.34 Auxiliary ID Register</a> on page B1-190</td>
</tr>
<tr>
<td>CSSELR</td>
<td>2</td>
<td>c0</td>
<td>0</td>
<td>0x00000000</td>
<td><a href="#">B1.45 Cache Size Selection Register</a> on page B1-211</td>
<td></td>
</tr>
</tbody>
</table>
### B1.21 AArch32 Virtual memory control registers

The following table shows the virtual memory control registers.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCTLR</td>
<td>c1</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>0x00C50838</td>
<td>32-bit</td>
<td>B1.105 System Control Register on page B1-324</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value depends on inputs, CFGTE, CFGEND, and VINITHI. The value</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>listed here assumes these signals are set to LOW.</td>
</tr>
<tr>
<td>TTBR0</td>
<td>c2</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Translation Table Base Register 0, see B1.113 Translation Table Base</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Register 0 on page B1-338</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
<td>c2</td>
<td>-</td>
<td></td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>TTBR1</td>
<td>c2</td>
<td>0</td>
<td>c0</td>
<td>1</td>
<td>UNK</td>
<td>32-bit</td>
<td>Translation Table Base Register 1, see B1.116 Translation Table Base</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Register 1 on page B1-342</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>c2</td>
<td>-</td>
<td></td>
<td>64-bit</td>
<td></td>
</tr>
<tr>
<td>TTBCR</td>
<td>c2</td>
<td>0</td>
<td>c0</td>
<td>2</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>B1.110 Translation Table Base Control Register on page B1-333</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value is 0x00000000 for the Secure copy of the register. The</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>reset value for the EAE bit of the Non-secure copy of the register is</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x0. You must program the Non-secure copy of the register with the</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>required initial value, as part of the processor boot sequence.</td>
</tr>
<tr>
<td>DACR</td>
<td>c3</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>B1.47 Domain Access Control Register on page B1-215</td>
</tr>
<tr>
<td>PRRR</td>
<td>c10</td>
<td>0</td>
<td>c2</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>B1.101 Primary Region Remap Register on page B1-316</td>
</tr>
<tr>
<td>MAIR0</td>
<td></td>
<td>0</td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>B1.95 Memory Attribute Indirection Registers 0 and 1 on page B1-304</td>
</tr>
<tr>
<td>NMRR</td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>B1.99 Normal Memory Remap Register on page B1-313</td>
<td></td>
</tr>
<tr>
<td>MAIR1</td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>B1.95 Memory Attribute Indirection Registers 0 and 1 on page B1-304</td>
<td></td>
</tr>
<tr>
<td>AMAIR0</td>
<td>c3</td>
<td>0</td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td>B1.36 Auxiliary Memory Attribute Indirection Register 0 on page B1-192</td>
<td></td>
</tr>
<tr>
<td>AMAIR1</td>
<td></td>
<td>1</td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td>B1.37 Auxiliary Memory Attribute Indirection Register 1 on page B1-193</td>
<td></td>
</tr>
<tr>
<td>CONTEXTIDR</td>
<td>c13</td>
<td>0</td>
<td>c0</td>
<td>1</td>
<td>UNK</td>
<td>32-bit</td>
<td>Process ID Register, see the Arm® Architecture Reference Manual Armv8, for</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Armv8-A architecture profile</td>
</tr>
</tbody>
</table>
## B1.22 AArch32 Fault handling registers

The following table shows the Fault handling registers in the AArch32 Execution state.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFSR</td>
<td>c5</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>B1.49 Data Fault Status Register on page B1-217</td>
</tr>
<tr>
<td>IFSR</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>B1.87 Instruction Fault Status Register on page B1-288</td>
</tr>
<tr>
<td>ADFSR</td>
<td>c1</td>
<td></td>
<td></td>
<td>0</td>
<td>0x00000000</td>
<td>B1.33 Auxiliary Data Fault Status Register on page B1-189</td>
</tr>
<tr>
<td>AIFSR</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0x00000000</td>
<td>B1.35 Auxiliary Instruction Fault Status Register on page B1-191</td>
</tr>
<tr>
<td>DFAR</td>
<td>c6</td>
<td></td>
<td></td>
<td>0</td>
<td>UNK</td>
<td>Data Fault Address Register, see the Arm® Architecture Reference Manual</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Armv8, for Armv8-A architecture profile</td>
</tr>
<tr>
<td>IFAR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>Instruction Fault Address Register, see the Arm® Architecture Reference</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Manual Armv8, for Armv8-A architecture profile</td>
</tr>
</tbody>
</table>

The Virtualization registers include additional fault handling registers. See **B1.28 AArch32 Virtualization registers** on page B1-180 for more information.
## B1.23 AArch32 Other System control registers

The following table shows the other system registers.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACTLR</td>
<td>c1</td>
<td>0</td>
<td>c0</td>
<td>1</td>
<td>0x00000000</td>
<td>B1.32 Auxiliary Control Register on page B1-187</td>
</tr>
<tr>
<td>CPACR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>B1.41 Architectural Feature Access Control Register on page B1-200</td>
</tr>
<tr>
<td>FCSEIDR</td>
<td>c13</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>0x00000000</td>
<td>B1.53 FCSE Process ID Register on page B1-223</td>
</tr>
</tbody>
</table>
B1.24 AArch32 Address registers

The following table shows the address translation register and operations.

See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PAR</td>
<td>c7</td>
<td>0</td>
<td>c4</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>B1.100 Physical Address Register on page B1-315</td>
</tr>
<tr>
<td>-</td>
<td>0</td>
<td>c7</td>
<td></td>
<td>-</td>
<td></td>
<td>64-bit</td>
<td></td>
</tr>
</tbody>
</table>
B1.25 AArch32 Thread registers

The following table shows the miscellaneous operations.

See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPIDRURW</td>
<td>c13</td>
<td>0</td>
<td>c0</td>
<td>2</td>
<td>UNK</td>
<td>User Read/Write Thread ID Register</td>
</tr>
<tr>
<td>TPIDRURO</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>UNK</td>
<td>User Read-Only Thread ID Register</td>
</tr>
<tr>
<td>TPIDRPRW</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>UNK</td>
<td>EL1 only Thread ID Register</td>
</tr>
<tr>
<td>HTPIDR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>Hyp Software Thread ID Register</td>
</tr>
</tbody>
</table>
## AArch32 Performance monitor registers

The following table shows the performance monitor registers.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information.

### Table B1-25  Performance monitor registers

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMCR</td>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>0</td>
<td>0x41063000</td>
<td><em>C9.2 Performance Monitors Control Register</em> on page C9-474</td>
</tr>
<tr>
<td>PMCNTENSET</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>Performance Monitors Count Enable Set Register</td>
</tr>
<tr>
<td>PMCNTENCLR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>Performance Monitors Count Enable Clear Register</td>
</tr>
<tr>
<td>PMOVSR</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>UNK</td>
<td>Performance Monitors Overflow Flag Status Register</td>
</tr>
<tr>
<td>PMSWINC</td>
<td></td>
<td></td>
<td></td>
<td>4</td>
<td>UNK</td>
<td>Performance Monitors Software Increment Register</td>
</tr>
<tr>
<td>PMSELR</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td>UNK</td>
<td>Performance Monitors Event Counter Selection Register</td>
</tr>
<tr>
<td>PMCEID0</td>
<td></td>
<td></td>
<td></td>
<td>6</td>
<td>0x6FBBFFFF</td>
<td><em>C9.3 Performance Monitors Common Event Identification Register 0</em> on page C9-477</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>The reset value is 0x6E3FBFFFF if L2 cache is not implemented.</td>
</tr>
<tr>
<td>PMCEID1</td>
<td></td>
<td></td>
<td></td>
<td>7</td>
<td>0x00000000</td>
<td><em>C9.4 Performance Monitors Common Event Identification Register 1</em> on page C9-481</td>
</tr>
<tr>
<td>PMCCNTR</td>
<td>c13</td>
<td>0</td>
<td></td>
<td></td>
<td>UNK</td>
<td>Performance Monitors Cycle Count Register</td>
</tr>
<tr>
<td>PMXEVTYPEPER</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>Performance Monitors Selected Event Type Register</td>
</tr>
<tr>
<td>PMXEVCNTR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>Performance Monitors Event Count Registers</td>
</tr>
<tr>
<td>PMUSERENR</td>
<td>c14</td>
<td>0</td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>Performance Monitors User Enable Register</td>
</tr>
<tr>
<td>PMINTENSET</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td>Performance Monitors Interrupt Enable Set Register</td>
</tr>
<tr>
<td>PMINTENCLR</td>
<td></td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>Performance Monitors Interrupt Enable Clear Register</td>
</tr>
<tr>
<td>PMOVSSET</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td>UNK</td>
<td>Performance Monitor Overflow Flag Status Set Register</td>
</tr>
<tr>
<td>Name</td>
<td>CRn</td>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Reset</td>
<td>Description</td>
</tr>
<tr>
<td>---------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>PMEVCNTR0</td>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>0</td>
<td>UNK</td>
<td>Performance Monitors Event Count Register 0</td>
</tr>
<tr>
<td>PMEVCNTR1</td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVCNTR2</td>
<td></td>
<td>2</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVCNTR3</td>
<td></td>
<td>3</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVCNTR4</td>
<td></td>
<td>4</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVCNTR5</td>
<td></td>
<td>5</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVTYPER0</td>
<td>c12</td>
<td>0</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td>Performance Monitors Selected Event Type Register 0</td>
</tr>
<tr>
<td>PMEVTYPER1</td>
<td></td>
<td>1</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVTYPER2</td>
<td></td>
<td>2</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVTYPER3</td>
<td></td>
<td>3</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVTYPER4</td>
<td></td>
<td>4</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMEVTYPER5</td>
<td></td>
<td>5</td>
<td></td>
<td>0</td>
<td>UNK</td>
<td></td>
</tr>
<tr>
<td>PMCCFILTR</td>
<td>c15</td>
<td>7</td>
<td></td>
<td>0x00000000</td>
<td>UNK</td>
<td>Performance Monitors Cycle Count Filter Register</td>
</tr>
</tbody>
</table>

Table B1-25  Performance monitor registers (continued)
The following table shows the Secure registers.

See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

### Table B1-26 Security registers

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCR</td>
<td>c1</td>
<td>0</td>
<td>c1</td>
<td>0</td>
<td>0x00000000</td>
<td>B1.104 Secure Configuration Register on page B1-321</td>
</tr>
<tr>
<td>SDER</td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td></td>
<td>Secure Debug Enable Register</td>
</tr>
<tr>
<td>NSACR</td>
<td></td>
<td></td>
<td>2</td>
<td>UNK</td>
<td>0x00000000</td>
<td>B1.98 Non-Secure Access Control Register on page B1-311</td>
</tr>
<tr>
<td>VBAR</td>
<td>c12</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>0x00000000</td>
<td>B1.119 Vector Base Address Register on page B1-346</td>
</tr>
<tr>
<td>MVBAR</td>
<td></td>
<td></td>
<td>1</td>
<td>UNK</td>
<td></td>
<td>Monitor Vector Base Address Register</td>
</tr>
<tr>
<td>ISR</td>
<td>c1</td>
<td>0</td>
<td>UNK</td>
<td></td>
<td></td>
<td>Interrupt Status Register</td>
</tr>
</tbody>
</table>

0x00000000 is the secure reset value and UNK is the non-secure reset value.
### AArch32 Virtualization registers

The following table shows the Virtualization registers.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VPIDR</td>
<td>c0</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>0x411F0010</td>
<td>32-bit</td>
<td><em>B1.121 Virtualization Processor ID Register on page B1-348</em></td>
</tr>
<tr>
<td>VMPIDR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HSCTRLR</td>
<td>c1</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>0x30C50838</td>
<td>32-bit</td>
<td><em>B1.67 Hyp System Control Register on page B1-248</em></td>
</tr>
<tr>
<td>HACTLR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td><em>B1.55 Hyp Auxiliary Control Register on page B1-225</em></td>
</tr>
<tr>
<td>HCR</td>
<td>c1</td>
<td>0</td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Hyp Configuration Register</td>
</tr>
<tr>
<td>HDCR</td>
<td></td>
<td>1</td>
<td></td>
<td>0x00000006</td>
<td>32-bit</td>
<td></td>
<td><em>B1.63 Hyp Debug Control Register on page B1-242</em></td>
</tr>
<tr>
<td>HCPTPR</td>
<td></td>
<td>2</td>
<td></td>
<td>0x000033FF</td>
<td>32-bit</td>
<td></td>
<td><em>B1.60 Hyp Architectural Feature Trap Register on page B1-231</em></td>
</tr>
<tr>
<td>HSTR</td>
<td></td>
<td>3</td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td>Hypervisor System Trap Register</td>
</tr>
<tr>
<td>HTCR</td>
<td>c2</td>
<td>4</td>
<td>c0</td>
<td>2</td>
<td>UNK</td>
<td>32-bit</td>
<td><em>B1.70 Hyp Translation Control Register on page B1-257</em></td>
</tr>
<tr>
<td>VTCR</td>
<td></td>
<td>1</td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>Virtualization Translation Control Register</td>
</tr>
<tr>
<td>HTTBR</td>
<td></td>
<td>4</td>
<td>c2</td>
<td>UNK</td>
<td>64-bit</td>
<td></td>
<td>Hyp Translation Table Base Register</td>
</tr>
<tr>
<td>VTTBR</td>
<td></td>
<td>6</td>
<td>c2</td>
<td>UNK</td>
<td>64-bit</td>
<td></td>
<td>Virtualization Translation Table Base Register</td>
</tr>
<tr>
<td>HADFSR</td>
<td>c5</td>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>*B1.56 Hyp Auxiliary Data Fault Status Syndrome Register on page B1-227</td>
</tr>
<tr>
<td>HAIFSR</td>
<td></td>
<td>1</td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td>*B1.57 Hyp Auxiliary Instruction Fault Status Syndrome Register on page B1-228</td>
</tr>
<tr>
<td>HSR</td>
<td>c2</td>
<td>0</td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td><em>B1.68 Hyp Syndrome Register on page B1-252</em></td>
</tr>
<tr>
<td>HDFAR</td>
<td>c6</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Hyp Data Fault Address Register</td>
</tr>
<tr>
<td>HIFAR</td>
<td></td>
<td>2</td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>Hyp Instruction Fault Address Register</td>
</tr>
<tr>
<td>HPFAR</td>
<td></td>
<td>4</td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td></td>
<td>Hyp IPA Fault Address Register</td>
</tr>
<tr>
<td>Name</td>
<td>CRn</td>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Reset</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
<td>-------</td>
<td>-------</td>
<td>------------------------------------------------------------</td>
</tr>
<tr>
<td>HMAIR0</td>
<td>c10</td>
<td>4</td>
<td>c2</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Hyp Memory Attribute Indirection Register 0</td>
</tr>
<tr>
<td>HMAIR1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Hyp Memory Attribute Indirection Register 1</td>
</tr>
<tr>
<td>HAMAIR0</td>
<td>c3</td>
<td>0</td>
<td>0</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>B1.58 Hyp Auxiliary Memory Attribute Indirection Register 0 on page B1-229</td>
<td></td>
</tr>
<tr>
<td>HAMAIR1</td>
<td>1</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>B1.59 Hyp Auxiliary Memory Attribute Indirection Register 1 on page B1-230</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>HVBAR</td>
<td>c12</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Hyp Vector Base Address Register</td>
</tr>
</tbody>
</table>
B1.29 AArch32 GIC system registers

The following table shows the GIC system registers in AArch32 state.

See the Arm® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 for more information.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICC_SGI1R</td>
<td>-</td>
<td>0</td>
<td>c12</td>
<td>-</td>
<td>WO</td>
<td>-</td>
<td>64-bit</td>
<td>SGI Generation Register 1</td>
</tr>
<tr>
<td>ICC_ASGI1R</td>
<td>-</td>
<td>1</td>
<td>c12</td>
<td>-</td>
<td>WO</td>
<td>-</td>
<td>64-bit</td>
<td>Alternate SGI Generation Register 1</td>
</tr>
<tr>
<td>ICC_SGI0R</td>
<td>-</td>
<td>2</td>
<td>c12</td>
<td>-</td>
<td>WO</td>
<td>-</td>
<td>64-bit</td>
<td>SGI Generation Register 0</td>
</tr>
<tr>
<td>ICC_PMR</td>
<td>c4</td>
<td>0</td>
<td>c6</td>
<td>0</td>
<td>RW</td>
<td>-</td>
<td>32-bit</td>
<td>Priority Mask Register</td>
</tr>
<tr>
<td>ICC_IAR0</td>
<td>c12</td>
<td>0</td>
<td>c8</td>
<td>0</td>
<td>RO</td>
<td>-</td>
<td>32-bit</td>
<td>Interrupt Acknowledge Register 0</td>
</tr>
<tr>
<td>ICC_EOIR0</td>
<td>1</td>
<td>WO</td>
<td>-</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>End Of Interrupt Register 0</td>
</tr>
<tr>
<td>ICC_HPPIR0</td>
<td>2</td>
<td>RO</td>
<td>-</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Highest Priority Pending Interrupt Register 0</td>
</tr>
<tr>
<td>ICC_BPR0</td>
<td>3</td>
<td>RW</td>
<td>0x00000002</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Binary Point Register 0</td>
</tr>
<tr>
<td>ICC_AP0R0</td>
<td>4</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Active Priorities 0 Register 0</td>
</tr>
<tr>
<td>ICC_AP1R0</td>
<td>e9</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td>Active Priorities 1 Register 0</td>
</tr>
<tr>
<td>ICC_DIR</td>
<td>c11</td>
<td>1</td>
<td>WO</td>
<td>-</td>
<td></td>
<td></td>
<td>32-bit</td>
<td>Deactivate Interrupt Register</td>
</tr>
<tr>
<td>ICC_RPR</td>
<td>3</td>
<td>RO</td>
<td>-</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Running Priority Register</td>
</tr>
<tr>
<td>ICC_IAR1</td>
<td>c12</td>
<td>0</td>
<td>RO</td>
<td>-</td>
<td></td>
<td></td>
<td>32-bit</td>
<td>Interrupt Acknowledge Register 1</td>
</tr>
<tr>
<td>ICC_EOIR1</td>
<td>1</td>
<td>WO</td>
<td>-</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>End Of Interrupt Register 1</td>
</tr>
<tr>
<td>ICC_HPPIR1</td>
<td>2</td>
<td>RO</td>
<td>-</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Highest Priority Pending Interrupt Register 1</td>
</tr>
<tr>
<td>ICC_BPR1</td>
<td>3</td>
<td>RW</td>
<td>0x00000003</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Binary Point Register 1</td>
</tr>
<tr>
<td>ICC_CTLR</td>
<td>4</td>
<td>RW</td>
<td>0x00000040</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt Control Register</td>
</tr>
<tr>
<td>ICC_SRE</td>
<td>5</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>System Register Enable Register</td>
</tr>
<tr>
<td>ICC_IGRPEN0</td>
<td>6</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt Group Enable Register 0</td>
</tr>
<tr>
<td>ICC_IGRPEN1</td>
<td>7</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt Group Enable Register 1</td>
</tr>
<tr>
<td>ICH_AP0R0</td>
<td>4</td>
<td>c8</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td>Interrupt Controller Hyp Active Priorities Register (0,0)</td>
</tr>
<tr>
<td>ICH_AP1R0</td>
<td>e9</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td>Interrupt Controller Hyp Active Priorities Register (1,0)</td>
</tr>
<tr>
<td>ICH_HSRE</td>
<td>5</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>System Register Enable Register for EL2</td>
</tr>
<tr>
<td>ICH_HCR</td>
<td>c11</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td>Interrupt Controller Hyp Control Register</td>
</tr>
<tr>
<td>ICH_VTR</td>
<td>1</td>
<td>RO</td>
<td>0x090000003</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt Controller VGIC Type Register</td>
</tr>
<tr>
<td>ICH_MISR</td>
<td>2</td>
<td>RO</td>
<td>0x00000000</td>
<td>32-bit</td>
<td></td>
<td></td>
<td></td>
<td>Interrupt Controller Maintenance Interrupt State Register</td>
</tr>
</tbody>
</table>

This is the reset value in non-secure state. In secure state, the reset value is 0x00000002.
<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>CRm</th>
<th>Op1</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICH_EISR</td>
<td>c12</td>
<td>c8</td>
<td>3</td>
<td>RO</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller End of Interrupt Status Register</td>
</tr>
<tr>
<td>ICH_VMCR</td>
<td>7</td>
<td>RW</td>
<td>0x004C0000</td>
<td>32-bit</td>
<td>Interrupt Controller Virtual Machine Control Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_ELRSR</td>
<td>5</td>
<td>RO</td>
<td>0x0000000F</td>
<td>32-bit</td>
<td>Interrupt Controller Empty List Register Status Register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LR0</td>
<td>c12</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 0</td>
<td></td>
</tr>
<tr>
<td>ICH_LR1</td>
<td>1</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LR2</td>
<td>2</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LR3</td>
<td>3</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LRC0</td>
<td>c14</td>
<td>0</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 0</td>
<td></td>
</tr>
<tr>
<td>ICH_LRC1</td>
<td>1</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LRC2</td>
<td>2</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICH_LRC3</td>
<td>3</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller List Register 3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC_MCTLR</td>
<td>6</td>
<td>c12</td>
<td>4</td>
<td>RW</td>
<td>0x0000000000</td>
<td>32-bit</td>
<td>Interrupt Control Register for EL3</td>
</tr>
<tr>
<td>ICC_MSRE</td>
<td>5</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>System Register Enable Register for EL3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ICC_MGRPEN1</td>
<td>7</td>
<td>RW</td>
<td>0x00000000</td>
<td>32-bit</td>
<td>Interrupt Controller Monitor Interrupt Group 1 Enable</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table B1-28 AArch32 GIC system registers (continued)
B1.30 AArch32 Generic Timer registers

The processor implements the architecturally defined Generic Timer registers.

The AArch32 Generic Timer registers are described in B3.1 AArch32 Generic Timer register summary on page B3-362. See also the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile. for more information.
### B1.31 AArch32 Implementation defined registers

IMPLEMENTATION DEFINED registers provide test features and any required configuration options specific to the Cortex-A32 processor.

The following table shows the 32-bit wide implementation defined registers.

#### Table B1-29 Memory access registers

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2CTLR</td>
<td>c9</td>
<td>1</td>
<td>c0</td>
<td>2</td>
<td>-</td>
<td>32-bit</td>
<td><em>B1.92 L2 Control Register on page B1-297</em> The reset value depends on the processor configuration.</td>
</tr>
<tr>
<td>L2ECTLR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0x00000000</td>
<td>32-bit</td>
<td><em>B1.93 L2 Extended Control Register on page B1-299</em></td>
</tr>
<tr>
<td>L2ACTLR</td>
<td>c15</td>
<td>1</td>
<td>c0</td>
<td>0</td>
<td>0x80000000</td>
<td>32-bit</td>
<td><em>B1.91 L2 Auxiliary Control Register on page B1-295</em> This is the reset value for an ACE interface. For an AXI interface the reset value is 0x80000008. For a CHI interface the reset value is 0x80004008.</td>
</tr>
<tr>
<td>CBAR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>32-bit</td>
<td><em>B1.38 Configuration Base Address Register on page B1-194</em> The reset value depends on the processor configuration.</td>
</tr>
<tr>
<td>CDBGDR0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Register 0, see <em>C5.1 About direct access to internal memory</em> for information on how these registers are used.</td>
</tr>
<tr>
<td>CDBGDR1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Register 1, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGDR2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Register 2, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGDR3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Register 3, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGDCT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Cache Tag Read Operation Register, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGICT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Instruction Cache Tag Read Operation Register, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGDCD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Data Cache Data Read Operation Register, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGICD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>Instruction Cache Data Read Operation Register, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>CDBGTD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>UNK</td>
<td>32-bit</td>
<td>TLB Data Read Operation Register, see <em>C5.1 About direct access to internal memory</em></td>
</tr>
<tr>
<td>Name</td>
<td>CRn</td>
<td>CRm</td>
<td>Op1</td>
<td>CRm</td>
<td>Op2</td>
<td>Reset</td>
<td>Width</td>
</tr>
<tr>
<td>---------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>--------------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>CPUACTLR</td>
<td>-</td>
<td>c15</td>
<td>0</td>
<td>c15</td>
<td>-</td>
<td>0x0000000000000000</td>
<td>64-bit</td>
</tr>
<tr>
<td>CPUECTLR</td>
<td>-</td>
<td>c15</td>
<td>1</td>
<td>c15</td>
<td>-</td>
<td>0x0000000000000000</td>
<td>64-bit</td>
</tr>
<tr>
<td>CPUMERRSR</td>
<td>-</td>
<td>c15</td>
<td>2</td>
<td>c15</td>
<td>-</td>
<td>-</td>
<td>64-bit</td>
</tr>
<tr>
<td>L2MERRSR</td>
<td>-</td>
<td>c15</td>
<td>3</td>
<td>c15</td>
<td>-</td>
<td>-</td>
<td>64-bit</td>
</tr>
</tbody>
</table>
**B1.32 Auxiliary Control Register**

The ACTLR characteristics are:

**Purpose**
Controls write access to *IMPLEMENTATION DEFINED* registers in EL2, such as CPUACTLR, CPUECTLR, L2CTLR, L2ECTLR, and L2ACTLR.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 NS</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
The processor does not implement the ACTLR (NS) register. This register is always RES0.

**Attributes**
ACTLR is a 32-bit register.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Figure B1-1 ACTLR bit assignments**

[31:7]
Reserved, RES0.

**L2ACTLR access control, [6]**
L2ACTLR write access control. The possible values are:

0 The register is not write accessible from a lower exception level. This is the reset value.
1 The register is write accessible from EL2.

**L2ECTLR access control, [5]**
L2ECTLR write access control. The possible values are:

0 The register is not write accessible from a lower exception level. This is the reset value.
1 The register is write accessible from EL2.

**L2CTLR access control, [4]**
L2CTLR write access control. The possible values are:

0 The register is not write accessible from a lower exception level. This is the reset value.
1 The register is write accessible from EL2.

[3:2]
Reserved, RES0.
CPUECTRL access control, [1]

CPUECTRL write access control. The possible values are:

0  The register is not write accessible from a lower exception level. This is the reset value.
1  The register is write accessible from EL2.

CPUACTLR access control, [0]

CPUACTLR write access control. The possible values are:

0  The register is not write accessible from a lower exception level. This is the reset value.
1  The register is write accessible from EL2.

To access the ACTLR:

MRC p15, 0, <Rt>, c1, c0, 1 ; Read ACTLR into Rt
MCR p15, 0, <Rt>, c1, c0, 1 ; Write Rt to ACTLR

Register access is encoded as follows:

Table B1-30  ACTLR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0000</td>
<td>001</td>
</tr>
</tbody>
</table>
B1.33 **Auxiliary Data Fault Status Register**

ADFSR

The processor does not implement ADFSR. This register is always **RES0**.
### B1.34 Auxiliary ID Register

**AIDR**

The processor does not implement AIDR. This register is always `RES0`. 
B1.35 Auxiliary Instruction Fault Status Register

AIFSR

The processor does not implement AIFSR. This register is always RES0.
B1.36 Auxiliary Memory Attribute Indirection Register 0

AMAIR0

The processor does not implement AMAIR0. This register is always RES0.
B1.37  Auxiliary Memory Attribute Indirection Register 1

AMAIR1

The processor does not implement AMAIR1. This register is always RES0.
### B1.38 Configuration Base Address Register

The CBAR characteristics are:

**Purpose**

Holds the physical base address of the memory-mapped GIC CPU interface registers.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td></td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
</tr>
<tr>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**

The CBAR is Common to the Secure and Non-secure states.

**Attributes**

CBAR is a 32-bit register.

![Figure B1-2 CBAR bit assignments](image)

**PERIPHBASE[31:18], [31:18]**

If the processor is implemented with the GIC CPU interface, the input `PERIPHBASE[31:18]` determines the reset value. If the GIC CPU interface is not implemented, this field is RAZ.

**[17:8]**

Reserved, `RES0`.

**PERIPHBASE[39:32], [7:0]**

If the processor is implemented with the GIC CPU interface, the input `PERIPHBASE[39:32]` determines the reset value. If the GIC CPU interface is not implemented, this field is RAZ.

To access the CBAR:

```
MRC p15, 1, <Rt>, c15, c3, 0; Read CBAR into Rt
```

Register access is encoded as follows:

![Table B1-31 CBAR access encoding](image)
B1.39  Cache Size ID Register

The CCSIDR characteristics are:

Purpose
Provides information about the architecture of the caches.

Usage constraints
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

If CSSELR indicates a cache that is not implemented, then on a read of the CCSIDR the behavior is constrained unpredictable, and can be one of the following:

- The CCSIDR read is treated as NOP.
- The CCSIDR read is undefined.
- The CCSIDR read returns an unknown value (preferred).

Configurations
There is one copy of this register that is used in both Secure and Non-secure states.

The implementation includes one CCSIDR for each cache that it can access. CSSELR selects which Cache Size ID Register is accessible.

Attributes
CCSIDR is a 32-bit register.

<table>
<thead>
<tr>
<th>31 30 29 28 27</th>
<th>13 12</th>
<th>3 2 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NumSets</td>
<td>Associativity</td>
<td>LineSize</td>
</tr>
</tbody>
</table>

WT, [31]
Indicates support for Write-Through:
0 Cache level does not support Write-Through.

WB, [30]
Indicates support for Write-Back:
0 Cache level does not support Write-Back.
1 Cache level supports Write-Back.

RA, [29]
Indicates support for Read-Allocation:
0 Cache level does not support Read-Allocation.
1 Cache level supports Read-Allocation.

WA, [28]
Indicates support for Write-Allocation:
Cache level does not support Write-Allocation.

Cache level supports Write-Allocation.

NumSets, [27:13]
Indicates the number of sets in cache - 1. Therefore, a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

For more information about encoding, see Table B1-32 CCSIDR encodings on page B1-196.

Associativity, [12:3]
Indicates the associativity of cache - 1. Therefore, a value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2.

For more information about encoding, see Table B1-32 CCSIDR encodings on page B1-196.

LineSize, [2:0]
Indicates the \( \log_2 (\text{number of words in cache line}) \) - 2:

- \( 0b010 \): 16 words per line.

For more information about encoding, see Table B1-32 CCSIDR encodings on page B1-196.

The following table shows the individual bit field and complete register encodings for the CCSIDR. The CSSELR determines which CCSIDR to select.

<table>
<thead>
<tr>
<th>CSSELR</th>
<th>Cache</th>
<th>Size</th>
<th>Complete register encoding</th>
<th>Register bit field encoding</th>
<th>WT</th>
<th>WB</th>
<th>RA</th>
<th>WA</th>
<th>NumSets</th>
<th>Associativity</th>
<th>LineSize</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>L1 Data cache</td>
<td>8KB</td>
<td>0x7003E01A</td>
<td>0x001F 0x003 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x001F 0x003 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16KB</td>
<td>0x7007E01A</td>
<td>0x003F 0x003 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x003F 0x003 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>32KB</td>
<td>0x700FE01A</td>
<td>0x007F 0x003 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x007F 0x003 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>64KB</td>
<td>0x701FE01A</td>
<td>0x00FF 0x003 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x00FF 0x003 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>L1 Instruction cache</td>
<td>8KB</td>
<td>0x2007E00A</td>
<td>0x003F 0x001 0x2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x003F 0x001 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>16KB</td>
<td>0x200FE00A</td>
<td>0x007F 0x001 0x2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x007F 0x001 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>32KB</td>
<td>0x201FE00A</td>
<td>0x00FF 0x001 0x2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x00FF 0x001 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>64KB</td>
<td>0x203FE00A</td>
<td>0x001F 0x001 0x2</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0x001F 0x001 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x2</td>
<td>L2 cache</td>
<td>128KB</td>
<td>0x701FE03A</td>
<td>0x00FF 0x007 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x00FF 0x007 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>256KB</td>
<td>0x703FE03A</td>
<td>0x01FF 0x007 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x01FF 0x007 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>512KB</td>
<td>0x707FE03A</td>
<td>0x03FF 0x007 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x03FF 0x007 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>1024KB</td>
<td>0x70FFE03A</td>
<td>0x07FF 0x007 0x2</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0x07FF 0x007 0x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x3-0xF</td>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

To access the CCSIDR:

\[
\text{MRC p15, 1, <Rt>, c0, c0, 0 ; Read CCSIDR into Rt}
\]

Register access is encoded as follows:
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>0000</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.40 Cache Level ID Register

The CLIDR characteristics are:

**Purpose**

Identifies:
- The type of cache, or caches, implemented at each level.
- The Level of Coherency and Level of Unification for the cache hierarchy.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

CLIDR is a 32-bit register.

<table>
<thead>
<tr>
<th>31 30 29 27 26 24 23 21 20</th>
<th>9 8 6 5 3 2 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICB</td>
<td>LoUU</td>
</tr>
</tbody>
</table>

**Figure B1-4 CLIDR bit assignments**

**ICB, [31:30]**

Inner cache boundary. This field indicates the boundary between the inner and the outer domain.

0b00 Not disclosed in this mechanism.

**LoUU, [29:27]**

Indicates the Level of Unification Uniprocessor for the cache hierarchy:

0b001 L1 cache is the last level of cache that must be cleaned or invalidated when cleaning or invalidating to the point of unification for the processor.

**LoC, [26:24]**

Indicates the Level of Coherency for the cache hierarchy:

0b001 L2 cache not implemented.

0b010 A clean to the point of coherency operation requires the L1 and L2 caches to be cleaned.

**LoUIS, [23:21]**

Indicates the Level of Unification Inner Shareable for the cache hierarchy:

0b001 L2 cache not implemented or BROADCASTINNER set to 0.

The L1 cache is the last level of cache that must be cleaned or invalidated when cleaning or invalidating to the point of unification for the Inner Shareable shareability domain.
L2 cache implemented and **BROADCASTINNER** set to 1.

The L2 cache is the last level of cache that must be cleaned or invalidated when cleaning or invalidating to the point of unification for the Inner Shareable shareability domain.

[20:9]
Reserved, res0.

**Ctype3, [8:6]**
Indicates the type of cache if the processor implements L3 cache:
- 0b000  L3 cache not implemented.

If software reads the Cache Type fields from Ctype1 upwards, after it has seen a value of 0b000, no caches exist at further-out levels of the hierarchy. So, for example, if Ctype2 is the first Cache Type field with a value of 0b000, the value of Ctype3 must be ignored.

**Ctype2, [5:3]**
Indicates the type of cache if the processor implements L2 cache:
- 0b000  L2 cache is not implemented.
- 0b100  L2 cache is implemented as a unified cache.

**Ctype1, [2:0]**
Indicates the type of cache implemented at L1:
- 0b011  Separate instruction and data caches at L1.

To access the CLIDR:

```assembly
MRC p15,1,<Rt>,c0,c0,1 ; Read CLIDR into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>0000</td>
<td>0000</td>
<td>001</td>
</tr>
</tbody>
</table>

**Table B1-34 CLIDR access encoding**
B1.41 Architectural Feature Access Control Register

The CPACR characteristics are:

**Purpose**
Controls access to CP0 to CP13, and indicates which of CP0 to CP13 are implemented.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

The CPACR has no effect on instructions executed at EL2.

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

Bits in the NSACR control Non-secure access to the CPACR fields. See the field descriptions cp10 and cp11.

**Attributes**
CPACR is a 32-bit register.

![Figure B1-5 CPACR bit assignments](image)

**ASEDIS, [31]**
Disable Advanced SIMD functionality:

0  Does not cause any instructions to be **UNDEFINED**. This is the reset value.
1  All instruction encodings that are part of Advanced SIMD, but that are not floating-point instructions, are **UNDEFINED**.

If Advanced SIMD and floating-point are not implemented, this bit is **RES0**.

**[30:24]**
Reserved, **RES0**.

**cp11, [23:22]**
Defines the access rights for CP11, that control the Advanced SIMD and floating-point features. Possible values of the fields are:

0b00  Access denied. Any attempt to access Advanced SIMD and floating-point registers or instructions generates an Undefined Instruction exception. This is the reset value.
0b01  Access at EL1 only. Any attempt to access Advanced SIMD and floating-point registers or instructions from software executing at EL0 generates an Undefined Instruction exception.
0b10  Reserved.
0b11  Full access.
If Advanced SIMD and floating-point are not implemented, this field is \textit{RES0}.

The Advanced SIMD and floating-point features controlled by these fields are:
- Floating-point instructions.
- Advanced SIMD instructions, both integer and floating-point.
- Advanced SIMD and floating-point registers D0-D31 and their views as S0-S31 and Q0-Q15.
- FPSCR, FPSID, MVFR0, MVFR1, MVFR2, FPEXC system registers.

If the cp11 and cp10 fields are set to different values, the behavior is the same as if both fields were set to the value of cp10, in all respects other than the value read back by explicitly reading cp11.

\textbf{cp10, [21:20]}

Defines the access rights for CP10, that control the Advanced SIMD and floating-point features. Possible values of the fields are:
- $0b00$ Access denied. Any attempt to access Advanced SIMD and floating-point registers or instructions generates an Undefined Instruction exception. This is the reset value.
- $0b01$ Access at EL1 only. Any attempt to access Advanced SIMD and floating-point registers or instructions from software executing at EL0 generates an Undefined Instruction exception.
- $0b10$ Reserved.
- $0b11$ Full access.

If Advanced SIMD and floating-point are not implemented, this bit is \textit{RES0}.

The Advanced SIMD and floating-point features controlled by these fields are:
- Floating-point instructions.
- Advanced SIMD instructions, both integer and floating-point.
- Advanced SIMD and floating-point registers D0-D31 and their views as S0-S31 and Q0-Q15.
- FPSCR, FPSID, MVFR0, MVFR1, MVFR2, FPEXC system registers.

\textbf{[19:0]}

Reserved, \textit{RES0}.

To access the CPACR:

\begin{verbatim}
MRC p15,0,<Rt>,c1,c0,2 ; Read CPACR into Rt
MCR p15,0,<Rt>,c1,c0,2 ; Write Rt to CPACR
\end{verbatim}

Register access is encoded as follows:

\begin{table}[h]
\centering
\caption{CPACR access encoding}
\begin{tabular}{|c|c|c|c|c|}
\hline
\textbf{coproc} & \textbf{opc1} & \textbf{CRn} & \textbf{CRm} & \textbf{opc2} \\
\hline
1111 & 000 & 0001 & 0000 & 010 \\
\hline
\end{tabular}
\end{table}
B1.42 CPU Auxiliary Control Register

The CPUACTLR characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED configuration and control options for the processor. There is one 64-bit CPU Auxiliary Control Register for each core in the processor.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td></td>
<td>(NS)</td>
<td></td>
<td></td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

The CPU Auxiliary Control Register can be written only when the system is idle. Arm recommends that you write to this register after a powerup reset, before the MMU is enabled, and before any master interface or ACP traffic begins.

Setting many of these bits can cause significantly lower performance on your code. Therefore, it is suggested that you do not modify this register unless directed by Arm.

**Configurations**

CPUACTLR is common to the Secure and Non-secure states.

**Attributes**

CPUACTLR is a 64-bit register.

![Figure B1-6  CPUACTLR bit assignments](image)

**[63:45]**

Reserved, RES0.

**ENDCCASCI, [44]**

Enable data cache clean as data cache clean/invalidate. The possible values are:

0 Normal behavior, data cache clean operations are unaffected. This is the reset value.

1 Executes data cache clean operations as data cache clean and invalidate. The following operations are affected:
   - DCCSW is executed as DCCISW, DCCMVAU and DCCMVC are executed as DCCIMVC.

---

_reserved_
Reserved, \texttt{RES0}.

\textbf{CDIDIS, [30]}

Disable Cryptographic dual issue. The possible values are:

- \texttt{0}: Enable dual issue of Advanced SIMD and Cryptographic instructions. This is the reset value.
- \texttt{1}: Disable dual issue of Advanced SIMD and Cryptographic instructions.

\textbf{DIDIS, [29]}

Disable Dual Issue. The possible values are:

- \texttt{0}: Enable Dual Issue of instructions. This is the reset value.
- \texttt{1}: Disable Dual Issue of all instructions.

\textbf{RADIS, [28:27]}

Write streaming no-allocate threshold. The possible values are:

- \texttt{00b}: 16th consecutive streaming cache line does not allocate in the L1 or L2 cache.
- \texttt{01b}: 128th consecutive streaming cache line does not allocate in the L1 or L2 cache. This is the reset value.
- \texttt{10b}: 512th consecutive streaming cache line does not allocate in the L1 or L2 cache.
- \texttt{11b}: Disables streaming. All write-allocate lines allocate in the L1 or L2 cache.

\textbf{L1RADIS, [26:25]}

Write streaming no-L1-allocate threshold. The possible values are:

- \texttt{00b}: 4th consecutive streaming cache line does not allocate in the L1 cache. This is the reset value.
- \texttt{01b}: 64th consecutive streaming cache line does not allocate in the L1 cache.
- \texttt{10b}: 128th consecutive streaming cache line does not allocate in the L1 cache.
- \texttt{11b}: Disables streaming. All write-allocate lines allocate in the L1 cache.

\textbf{DTAH, [24]}

Disable transient and no-read-allocate hints for loads. The possible values are:

- \texttt{0}: Normal operation.
- \texttt{1}: Transient and no-read-allocate hints in the MAIR are ignored and treated the same as non-transient, read-allocate types for loads. This is the reset value.

\textbf{STBPFRS, [23]}

Disable ReadUnique request for prefetch streams initiated by STB accesses:

- \texttt{0}: ReadUnique used for prefetch streams initiated from STB accesses. This is the reset value.
- \texttt{1}: ReadShared used for prefetch streams initiated from STB accesses.

\textbf{STBPFDIS, [22]}

Disable prefetch streams initiated from STB accesses:

- \texttt{0}: Enable Prefetch streams initiated from STB accesses. This is the reset value.
- \texttt{1}: Disable Prefetch streams initiated from STB accesses.
Reserved, \texttt{RES0}.

**NPFSTRM, [20:19]**

Number of independent data prefetch streams. The possible values are:

- \texttt{0b00} 1 stream.
- \texttt{0b01} 2 streams. This is the reset value.
- \texttt{0b10} 3 streams.
- \texttt{0b11} 4 streams.

**DSTDIS, [18]**

Enable device split throttle. The possible values are:

- 0 Device split throttle disabled.
- 1 Device split throttle enabled. This is the reset value.

**STRIDE, [17]**

Enable stride detection. The possible values are:

- 0 2 consecutive strides to trigger prefetch. This is the reset value.
- 1 3 consecutive strides to trigger prefetch.

Reserved, \texttt{RES0}.

**L1PCTL, [15:13]**

L1 Data prefetch control. The value of this field determines the maximum number of outstanding data prefetches allowed in the L1 memory system, excluding those generated by software load or PLD instructions. The possible values are:

- \texttt{0b000} Prefetch disabled.
- \texttt{0b001} 1 outstanding prefetch allowed.
- \texttt{0b010} 2 outstanding prefetches allowed.
- \texttt{0b011} 3 outstanding prefetches allowed.
- \texttt{0b100} 4 outstanding prefetches allowed.
- \texttt{0b101} 5 outstanding prefetches allowed. This is the reset value.
- \texttt{0b110} 6 outstanding prefetches allowed.
- \texttt{0b111} 8 outstanding prefetches allowed.

Reserved, \texttt{RES0}.

**DYNSDIS, [11]**

Disable dynamic stride adjustment for prefetch streams. The possible values are:

- 0 Enable dynamic stride adjustment. This is the reset value.
- 1 Disable dynamic stride adjustment.

**DODMBS, [10]**

Disable optimized Data Memory Barrier behavior. The possible values are:

- 0 Enable optimized Data Memory Barrier behavior. This is the reset value.
- 1 Disable optimized Data Memory Barrier behavior.
[9:7]  
Reserved, RES0.

L1DEIEN, [6]  
L1 D-cache data RAM error injection enable. The possible values are:

0  Normal behavior, errors are not injected. This is the reset value.
1  Double-bit errors are injected on all writes to the L1 D-cache data RAMs for the
first word of each 32-byte region.

[5:0]  
Reserved, RES0.

To access the CPUACTLR:

MRRC p15, 0, <Rt>, <Rt2>, c15; Read CPU Auxiliary Control Register
MCRR p15, 0, <Rt>, <Rt2>, c15; Write CPU Auxiliary Control Register

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>0000</td>
<td>1111</td>
</tr>
</tbody>
</table>
B1.43 CPU Extended Control Register

The CPUECTLR characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED configuration and control options for the processor.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

The CPUECTLR can be written dynamically.

**Configurations**

There are no configuration notes.

**Attributes**

CPUECTLR is a 64-bit register.

```
|63|62|51|50|49|48|47|46|45|44|43|42|41|40|39|38|37|36|35|34|33|32|31|30|29|28|27|26|25|24|23|22|21|20|19|18|17|16|15|14|13|12|11|10|9 |8 |7 |6 |5 |4 |3 |2 |1 |0 |
```

Reserved, RES0.

**SMPEN, [6]**

Enable hardware management of data coherency with other cores in the cluster. The possible values are:

- 0 Disables data coherency with other cores in the cluster. This is the reset value.
- 1 Enables data coherency with other cores in the cluster.

Set the SMPEN bit before enabling the caches, even if there is only one core in the system.

**FPRETCTL, [5:3]**

Advanced SIMD and floating-point retention control. The possible values are:

- 0b000 Disable the retention circuit. This is the reset value.
- 0b001 2 Architectural Timer ticks are required before retention entry.
- 0b010 8 Architectural Timer ticks are required before retention entry.
- 0b011 32 Architectural Timer ticks are required before retention entry.
- 0b100 64 Architectural Timer ticks are required before retention entry.
- 0b101 128 Architectural Timer ticks are required before retention entry.
- 0b110 256 Architectural Timer ticks are required before retention entry.
- 0b111 512 Architectural Timer ticks are required before retention entry.
This field is present only if the Advanced SIMD and floating-point support is implemented. Otherwise, it is RES0.

**CPURETCTL, [2:0]**

CPU retention control. The possible values are:

- **0b000**  Disable the retention circuit. This is the reset value.
- **0b001**  2 Architectural Timer ticks are required before retention entry.
- **0b010**  8 Architectural Timer ticks are required before retention entry.
- **0b011**  32 Architectural Timer ticks are required before retention entry.
- **0b100**  64 Architectural Timer ticks are required before retention entry.
- **0b101**  128 Architectural Timer ticks are required before retention entry.
- **0b110**  256 Architectural Timer ticks are required before retention entry.
- **0b111**  512 Architectural Timer ticks are required before retention entry.

To access the CPUECTLR:

- **MRRC p15, 1, <Rt>, <Rt2>, c15**; Read CPU Extended Control Register
- **MCRR p15, 1, <Rt>, <Rt2>, c15**; Write CPU Extended Control Register

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>1111</td>
</tr>
</tbody>
</table>
B1.44 CPU Memory Error Syndrome Register

The CPUMERRSR characteristics are:

**Purpose**

Holds ECC errors on the:
- L1 data RAMs.
- L1 tag RAMs.
- TLB RAMs.

This register is used for recording ECC errors on all processor RAMs.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

A write of any value to the register updates the register to 0000000000000000.

**Attributes**

CPUMERRSR is a 64-bit register.

### Fatal, [63]

Fatal bit. This bit is set to 1 on the first memory error that caused a data abort. It is a sticky bit so that after it is set, it remains set until the register is written.

The reset value is 0.

### [62:48]

Reserved, RES0.

### Other error count, [47:40]

This field is set to 0 on the first memory error and is incremented on any memory error that does not match the RAMID and Bank/Way information in this register while the sticky Valid bit is set.

The reset value is 0.

### Repeat error count, [39:32]

This field is set to 0 on the first memory error and is incremented on any memory error that exactly matches the RAMID and Bank/Way information in this register while the sticky Valid bit is set.

The reset value is 0.
Valid, [31]

Valid bit. This bit is set to 1 on the first memory error. It is a sticky bit so that after it is set, it remains set until the register is written.

The reset value is 0.

RAMID, [30:24]

RAM Identifier. Indicates the RAM in which the first memory error occurred. The possible values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>L1 Instruction tag RAM.</td>
</tr>
<tr>
<td>0x01</td>
<td>L1 Instruction data RAM.</td>
</tr>
<tr>
<td>0x08</td>
<td>L1 Data tag RAM.</td>
</tr>
<tr>
<td>0x09</td>
<td>L1 Data data RAM.</td>
</tr>
<tr>
<td>0x0A</td>
<td>L1 Data dirty RAM.</td>
</tr>
<tr>
<td>0x18</td>
<td>TLB RAM.</td>
</tr>
</tbody>
</table>

[23:21]

Reserved, RES0.

CPUID/Way, [20:18]

Indicates the RAM where the first memory error occurred.

**L1 I-tag RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Way 0</td>
</tr>
<tr>
<td>0x1</td>
<td>Way 1</td>
</tr>
<tr>
<td>0x2-0x7</td>
<td>Unused</td>
</tr>
</tbody>
</table>

**L1 I-data RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Bank 0</td>
</tr>
<tr>
<td>0x1</td>
<td>Bank 1</td>
</tr>
<tr>
<td>0x2-0x7</td>
<td>Unused</td>
</tr>
</tbody>
</table>

**TLB RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Way 0</td>
</tr>
<tr>
<td>0x1</td>
<td>Way 1</td>
</tr>
<tr>
<td>0x2-0x7</td>
<td>Unused</td>
</tr>
</tbody>
</table>

**L1 D-dirty RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Dirty RAM</td>
</tr>
<tr>
<td>0x1-0x7</td>
<td>Unused</td>
</tr>
</tbody>
</table>

**L1 D-tag RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Way 0</td>
</tr>
<tr>
<td>0x1</td>
<td>Way 1</td>
</tr>
<tr>
<td>0x2</td>
<td>Way 2</td>
</tr>
<tr>
<td>0x3</td>
<td>Way 3</td>
</tr>
<tr>
<td>0x4-0x7</td>
<td>Unused</td>
</tr>
</tbody>
</table>

**L1 D-data RAM**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Way0-Bank0</td>
</tr>
<tr>
<td>0x1</td>
<td>Way0-Bank1</td>
</tr>
</tbody>
</table>
Way1-Bank0
Way1-Bank1
...
Way3-Bank1

[17:12]

Reserved, RES0.

**RAM address, [11:0]**

Indicates the index address of the first memory error.

- A fatal error results in the RAMID, Way, and RAM address recording the fatal error, even if the sticky bit is set.
- Only L1 Data data and L1 Data dirty RAMs can signal fatal errors, because all other RAM instances are protected only by parity.
- If two or more memory errors in the same RAM occur in the same cycle, only one error is reported.
- If two or more first memory error events from different RAMs occur in the same cycle, one of the errors is selected arbitrarily.
- If two or more memory error events from different RAMs, that do not match the RAMID, Way, and index information in this register while the sticky Valid bit is set, occur in the same cycle, then the Other error count field is incremented only by one.

To access the CPUMERRSR:

| MRRC p15, 2, </Rt>, </Rt2>, c15; Read CPUMERRSR into Rt and Rt2 |
| MCRR p15, 2, </Rt>, </Rt2>, c15; Write Rt and Rt2 to CPUMERRSR |

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>0010</td>
<td>111</td>
</tr>
</tbody>
</table>
B1.45 Cache Size Selection Register

The CSSELR characteristics are:

**Purpose**

Selects the current CCSIDR, see *B1.39 Cache Size ID Register* on page B1-195, by specifying:
- The required cache level.
- The cache type, either instruction or data cache.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

If the CSSELR level field is programmed to a cache level that is not implemented, then a read of CSSELR returns an **UNKNOWN** value in CSSEL.R-Level.

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

**Attributes**

CSSELR is a 32-bit register.

![Figure B1-9 CSSELR bit assignments](image)

[31:4]

Reserved, **RESO**.

**Level, [3:1]**

Cache level of required cache:
- 0b000  L1.
- 0b001  L2.
- 0b010-0b111  Reserved.

The combination of Level=0b001 and InD=1 is reserved.

**InD, [0]**

Instruction not Data bit:
- 0  Data or unified cache.
- 1  Instruction cache.

The combination of Level=0b001 and InD=1 is reserved.

To access the CSSELR:

MRC p15, 2, <Rt>, c0, c0, 0; Read CSSEL.R into Rt
MCR p15, 2, <Rt>, c0, c0, 0; Write Rt to CSSEL.R
Register access is encoded as follows:

Table B1-39  CSSELR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>010</td>
<td>0000</td>
<td>0001</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.46 Cache Type Register

The CTR characteristics are:

**Purpose**

Provides information about the architecture of the caches.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

CTR is a 32-bit register.

\[
\begin{array}{cccccccc}
31 & 30 & 28 & 27 & 24 & 23 & 20 & 19 & 16 & 15 & 14 & 13 & 4 & 3 & 0 \\
RES0 & CWG & ERG & DminLine & L1lp & RES0 & IminLine & RES1 \\
\end{array}
\]

Figure B1-10 CTR bit assignments

**Reserved, RES1.**

**Reserved, RES0.**

**CWG, [27:24]**

Cache Write-Back granule. \( \log_2 \) of the number of words of the maximum size of memory that can be overwritten as a result of the eviction of a cache entry that has had a memory location in it modified:

\[ 0 \times 4 \quad \text{Cache Write-Back granule size is 16 words.} \]

**ERG, [23:20]**

Exclusives Reservation Granule. \( \log_2 \) of the number of words of the maximum size of the reservation granule that has been implemented for the Load-Exclusive and Store-Exclusive instructions:

\[ 0 \times 4 \quad \text{Exclusive reservation granule size is 16 words.} \]

**DminLine, [19:16]**

\( \log_2 \) of the number of words in the smallest cache line of all the data and unified caches that the processor controls:

\[ 0 \times 4 \quad \text{Smallest data cache line size is 16 words.} \]

**L1lp, [15:14]**

L1 Instruction cache policy. Indicates the indexing and tagging policy for the L1 Instruction cache:
0b10  *Virtually Indexed Physically Tagged* (VIPT).

[13:4]

Reserved, RES0.

**IminLine, [3:0]**

\( \log_2 \) of the number of words in the smallest cache line of all the instruction caches that the processor controls.

\( 0 \times 4 \) Smallest instruction cache line size is 16 words.

To access the CTR:

```
MRC p15,0,<Rt>,c0,c0,1 ; Read CTR into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>010</td>
<td>0000</td>
<td>0000</td>
<td>001</td>
</tr>
</tbody>
</table>

**Table B1-40  CTR access encoding**
**B1.47 Domain Access Control Register**

The DACR characteristics are:

**Purpose**
Defines the access permission for each of the sixteen memory domains.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.
Write access to DACR(S) is disabled when the CP15SDISABLE2 signal is asserted HIGH.
DACR has no function when TTBCR.EAE is set to 1 to select the Long-descriptor translation table format.

**Attributes**
DACR is a 32-bit register.

\[
\begin{array}{cccccccccccccccccc}
\text{D15} & \text{D14} & \text{D13} & \text{D12} & \text{D11} & \text{D10} & \text{D9} & \text{D8} & \text{D7} & \text{D6} & \text{D5} & \text{D4} & \text{D3} & \text{D2} & \text{D1} & \text{D0} \\
\end{array}
\]

Figure B1-11 DACR bit assignments

\[D\text{<}n\text{>, bits [2n+1:2n], for } n = 0 \text{ to } 15, [31:0]\]
Domain \(n\) access permission, where \(n = 0\) to 15. Permitted values are:
- \(0b00\) No access. Any access to the domain generates a Domain fault.
- \(0b01\) Client. Accesses are checked against the permission bits in the translation tables.
- \(0b11\) Manager. Accesses are not checked against the permission bits in the translation tables.

The value \(0b10\) is reserved.

To access the DACR:

```
MRC p15, 0, <Rt>, c3, c0, 0 ; Read DACR into Rt
MCR p15, 0, <Rt>, c3, c0, 0 ; Write Rt to DACR
```

Register access is encoded as follows:

**Table B1-41 DACR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0011</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.48 Data Fault Address Register

The DFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Data Abort exception.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFAR(S)</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
</tr>
<tr>
<td>DFAR(NS)</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

DFAR (S) is architecturally mapped to HDFAR. See *B1.64 Hyp Data Fault Address Register* on page B1-245.

**Attributes**

DFAR is a 32-bit register.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VA of faulting address of synchronous Data Abort exception |

**VA, [31:0]**

The Virtual Address of faulting address of synchronous Data Abort exception.

To access the DFAR:

```
MRC p15, 0, <Rt>, c6, c0, 0 ; Read DFAR into Rt
MCR p15, 0, <Rt>, c6, c0, 0 ; Write Rt to DFAR
```

Register access is encoded as follows:

**Table B1-42 DFAR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0110</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.49 Data Fault Status Register

The DFSR characteristics are:

**Purpose**
Holds status information about the last data fault.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.

There are two formats for this register. The current translation table format determines which format of the register is used.

**Attributes**
DFSR is a 32-bit register.
B1.50 DFSR with Short-descriptor translation table format

DFSR has a specific format when using the Short-descriptor translation table format. The following figure shows the DFSR bit assignments when using the Short-descriptor translation table format.

![DFSR bit assignments for Short-descriptor translation table format](image)

**Figure B1-13** DFSR bit assignments for Short-descriptor translation table format

[31:14] Reserved, RES0.

CM, [13]
Cache maintenance fault. For synchronous faults, this bit indicates whether a cache maintenance operation generated the fault:

0 Abort not caused by a cache maintenance operation.
1 Abort caused by a cache maintenance operation.

ExT, [12]
External abort type. This field indicates whether an AXI Decode or Slave error caused an abort:

0 External abort marked as DECERR.
1 External abort marked as SLVERR.

For aborts other than external aborts this bit always returns 0.

Write not Read bit. This field indicates whether the abort was caused by a write or a read access:

0 Abort caused by a read access.
1 Abort caused by a write access.

For faults on CP15 cache maintenance operations, including the VA to PA translation operations, this bit always returns a value of 1.

FS[4], [10]
Part of the Fault Status field. See bits [3:0] in this table.

[9]
RAZ.

[8]
Reserved, RES0.

Domain, [7:4]
Specifies which of the 16 domains, D15-D0, was being accessed when a data fault occurred.

For permission faults that generate Data Abort exception, this field is UNKNOWN. Armv8 deprecates any use of the domain field in the DFSR.
FS[3:0], [3:0]

Fault Status bits. This field indicates the type of exception generated. Any encoding not listed is reserved:

- `0b00001` Alignment fault.
- `0b00010` Debug event.
- `0b00011` Access flag fault, section.
- `0b00100` Instruction cache maintenance fault.
- `0b00101` Translation fault, section.
- `0b00110` Access flag fault, page.
- `0b00111` Translation fault, page.
- `0b01000` Synchronous external abort, non-translation.
- `0b01001` Domain fault, section.
- `0b01011` Domain fault, page.
- `0b01100` Synchronous external abort on translation table walk, first level.
- `0b01101` Permission fault, section.
- `0b01110` Synchronous external abort on translation table walk, second level.
- `0b01111` Permission fault, second level.
- `0b10000` TLB conflict abort.
- `0b10101` LDREX or STREX abort.
- `0b10110` Asynchronous external abort.
- `0b11000` Asynchronous parity error on memory access.
- `0b11001` Synchronous parity error on memory access.
- `0b11100` Synchronous parity error on translation table walk, first level.
- `0b11110` Synchronous parity error on translation table walk, second level.
B1.51 DFSR with Long-descriptor translation table format

DFSR has a specific format when using the Long-descriptor translation table format.

The following figure shows the DFSR bit assignments when using the Long-descriptor translation table format.

![DFSR Bit Assignments](image)

**Figure B1-14 DFSR bit assignments for Long-descriptor translation table format**

- **[31:14]**
  - Reserved, RES0.

- **CM, [13]**
  - Cache maintenance fault. For synchronous faults, this bit indicates whether a cache maintenance operation generated the fault:
    - 0: Abort not caused by a cache maintenance operation.
    - 1: Abort caused by a cache maintenance operation.

- **ExT, [12]**
  - External abort type. This field indicates whether an AXI Decode or Slave error caused an abort:
    - 0: External abort marked as DECERR.
    - 1: External abort marked as SLVERR.

  For aborts other than external aborts this bit always returns 0.

- **WnR, [11]**
  - Write not Read bit. This field indicates whether the abort was caused by a write or a read access:
    - 0: Abort caused by a read access.
    - 1: Abort caused by a write access.

  For faults on CP15 cache maintenance operations, including the VA to PA translation operations, this bit always returns a value of 1.

- **[10]**
  - Reserved, RES0.

- **[9]**
  - RAO.

- **[8:6]**
  - Reserved, RES0.

- **Status, [5:0]**
  - Fault Status bits. This field indicates the type of exception generated. Any encoding not listed is reserved.
    - \(0b000000\): Address size fault in TTBR0 or TTBR1.
    - \(0b0001LL\): Translation fault, LL bits indicate level.
0b0010LL  Access fault flag, LL bits indicate level.
0b0011LL  Permission fault, LL bits indicate level.
0b010000  Synchronous external abort.
0b010001  Asynchronous external abort.
0b01011L  Synchronous external abort on translation table walk, LL bits indicate level.
0b011000  Synchronous parity error on memory access.
0b011001  Asynchronous parity error on memory access (DFSR only).
0b01111L  Synchronous parity error on memory access on translation table walk, first level, LL bits indicate level.
0b100001  Alignment fault.
0b100010  Debug event.
0b110000  TLB conflict abort.
0b110101  LDREX or STREX abort.

Table B1-43  Encodings of LL bits associated with the MMU fault

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reserved</td>
</tr>
<tr>
<td>0b01</td>
<td>Level 1</td>
</tr>
<tr>
<td>0b10</td>
<td>Level 2</td>
</tr>
<tr>
<td>0b11</td>
<td>Level 3</td>
</tr>
</tbody>
</table>

To access the DFSR:

MRC p15, 0, <Rt>, c5, c0, 0; Read DFSR into Rt
MCR p15, 0, <Rt>, c5, c0, 0; Write Rt to DFSR
B1.52 Encoding of ISS[24:20] when HSR[31:30] is 0b00

For EC values that are nonzero and have the two most-significant bits 0b00, ISS[24:20] provides the condition field for the trapped instruction, together with a valid flag for this field.

The encoding of this part of the ISS field is:

CV, ISS[24]

Condition valid. Possible values of this bit are:

0   The COND field is not valid.
1   The COND field is valid.

When an instruction is trapped, CV is set to 1.

COND, ISS[23:20]

The Condition field for the trapped instruction. This field is valid only when CV is set to 1.

If CV is set to 0, this field is RES0.

When an instruction is trapped, the COND field is set to the condition the instruction was executed with.
B1.53  FCSE Process ID Register

FCSEIDR

The processor does not implement *Fast Context Switch Extension* (FCSE). This register is always `RES0`. 
B1.54  Hyp Auxiliary Configuration Register

HACR

The processor does not implement HACR. This register is always RES0.
**B1.55 Hyp Auxiliary Control Register**

The HACTLR characteristics are:

**Purpose**

Controls write access to **IMPLEMENTATION DEFINED** registers in Non-secure EL1 modes, such as CPUACTLR, CPUECTLR, L2CTLR, L2ECTLR, and L2ACTLR.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

There are no configuration notes.

**Attributes**

HACTLR is a 32-bit register.

![Figure B1-15 HACTLR bit assignments](image)

[31:7]

Reserved, RES0.

**L2ACTLR access control, [6]**

L2ACTLR write access control. The possible values are:

0 The register is not write accessible from Non-secure EL1.

This is the reset value.

1 The register is write accessible from Non-secure EL1.

Write access from Non-secure EL1 also requires ACTLR(S)[6] to be set.

**L2ECTLR access control, [5]**

L2ECTLR write access control. The possible values are:

0 The register is not write accessible from Non-secure EL1.

This is the reset value.

1 The register is write accessible from Non-secure EL1.

Write access from Non-secure EL1 also requires ACTLR(S)[5] to be set.

**L2CTLR access control, [4]**
L2CTLR write access control. The possible values are:

0 The register is not write accessible from Non-secure EL1.
   This is the reset value.
1 The register is write accessible from Non-secure EL1.
   Write access from Non-secure EL1 also requires ACTLR(S)[4] to be set.

[3:2]
Reserved, RES0.

CPUECTLR access control, [1]

CPUECTLR write access control. The possible values are:

0 The register is not write accessible from Non-secure EL1.
   This is the reset value.
1 The register is write accessible from Non-secure EL1.
   Write access from Non-secure EL1 also requires ACTLR(S)[1] to be set.

CPUACTLR access control, [0]

CPUACTLR write access control. The possible values are:

0 The register is not write accessible from Non-secure EL1.
   This is the reset value.
1 The register is write accessible from Non-secure EL1.
   Write access from Non-secure EL1 also requires ACTLR(S)[0] to be set.

To access the HACTLR:

MRC p15,4,<Rt>,c1,c0,1 ; Read HACTLR into Rt
MCR p15,4,<Rt>,c1,c0,1 ; Write Rt to HACTLR

Register access is encoded as follows:

Table B1-44  HACTLR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0000</td>
<td>001</td>
</tr>
</tbody>
</table>
B1.56 Hyp Auxiliary Data Fault Status Syndrome Register

HADFSR

The processor does not implement HADFSR. This register is always RES0.
B1.57  Hyp Auxiliary Instruction Fault Status Syndrome Register

HAIFSR

The processor does not implement HAIFSR. This register is always RES0.
B1.58  Hyp Auxiliary Memory Attribute Indirection Register 0

HAMAIR0

The processor does not implement HAMAIR0. This register is always RES0.
B1.59 Hyp Auxiliary Memory Attribute Indirection Register 1

HAMAIR1

The processor does not implement HAMAIR1. This register is always RES0.
B1.60 Hyp Architectural Feature Trap Register

The HCPTR characteristics are:

**Purpose**
Controls trapping to Hyp mode of Non-secure access, at EL1 or lower, to coprocessors other than CP14 and CP15 and to floating-point and Advanced SIMD functionality. Also controls access from Hyp mode to this functionality.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL2 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

If a bit in the NSACR prohibits a Non-secure access, then the corresponding bit in the HCPTR behaves as RAO/WI for Non-secure accesses. See the bit description for TASE.

**Configurations**
There are no configuration notes.

**Attributes**
HCPTR is a 32-bit register.

TCPAC, [31]
Trap CPACR accesses. The possible values of this bit are:
- 0 Has no effect on CPACR accesses.
- 1 Trap valid Non-secure EL1 CPACR accesses to Hyp mode.

When this bit is set to 1, any valid Non-secure EL1 access to the CPACR is trapped to Hyp mode.
Resets to 0.

[T30:21]
Reserved, RES0.

TTA, [20]
Trap Trace Access.
Not implemented. RES0.

[T19:16]
Reserved, RES0.

TASE, [15]
Trap Advanced SIMD use:

0  If the NSACR settings permit Non-secure use of the Advanced SIMD functionality then Hyp mode can access that functionality, regardless of any settings in the CPACR. This bit value has no effect on possible use of the Advanced SIMD functionality from Non-secure EL1 and EL0 modes.

1  Trap valid Non-secure accesses to Advanced SIMD functionality to Hyp mode.

If Advanced SIMD and floating-point are not implemented, this bit is RAO/WI.

If NSACR.NSASEDIS is set to 1, then on Non-secure accesses to the HCPTR, the TASE bit behaves as RAO/WI.

[14]
Reserved, RES0.

[13:12]
Reserved, RES1.


Trap CP11. The possible values of each of this bit is:

0  If NSACR.cp11 is set to 1, then Hyp mode can access CP11, regardless of the value of CPACR.cp11. This bit value has no effect on possible use of CP11 from Non-secure EL1 and EL0 modes.

1  Trap valid Non-secure accesses to CP11 to Hyp mode.

Any otherwise-valid access to CP11 from:

• A Non-secure EL1 or EL0 state is trapped to Hyp mode.
• Hyp mode generates an Undefined Instruction exception, taken in Hyp mode.

Resets to 0.

If the TCP11 and TCP10 fields are set to different values, the behavior is the same as if both fields were set to the value of TCP10, in all respects other than the value read back by explicitly reading TCP11.

TCP10, [10]

Trap CP10. The possible values of each of this bit is:

0  If NSACR.cp10 is set to 1, then Hyp mode can access CP10, regardless of the value of CPACR.cp10. This bit value has no effect on possible use of CP10 from Non-secure EL1 and EL0 modes.

1  Trap valid Non-secure accesses to CP10 to Hyp mode.

Any otherwise-valid access to CP10 from:

• A Non-secure EL1 or EL0 state is trapped to Hyp mode.
• Hyp mode generates an Undefined Instruction exception, taken in Hyp mode.

Resets to 0.

If the TCP11 and TCP10 fields are set to different values, the behavior is the same as if both fields were set to the value of TCP10, in all respects other than the value read back by explicitly reading TCP11.

[9:0]
Reserved, RES1.
To access the HCPTR:

MRC p15,4,<Rt>,c1,c1,2 ; Read HCPTR into Rt
MCR p15,4,<Rt>,c1,c1,2 ; Write Rt to HCPTR

Register access is encoded as follows:

Table B1-45  HCPTR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0001</td>
<td>010</td>
</tr>
</tbody>
</table>
B1.61 Hyp Configuration Register

The HCR characteristics are:

**Purpose**
Provides configuration controls for virtualization, including defining whether various Non-secure operations are trapped to Hyp mode.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
There are no configuration notes.

**Attributes**
HCR is a 32-bit register.

---

[31] Reserved, RES0.

**TRVM, [30]**
Trap Read of Virtual Memory controls.

When 1, this causes Reads to the EL1 virtual memory control registers from EL1 to be trapped to EL2. This covers the following registers:

SCTLR, TTBR0, TTBR1, TTBCR, DACR, DFSR, IFSR, DFAR, IFAR, ADFSR, AIFSR, PRRR/MAIR0, NMRR/MAIR1, AMAIR0, AMAIR1, and CONTEXTIDR.

The reset value is 0.

**HCD, [29]**

---

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Non-Confidential
Hyp Call Disable. The HCD value is:
0  HVC is enabled at EL1 or EL2.
1  HVC is UNDEFINED at all exception levels.

[28]  Reserved, RES0.

TGE, [27]
Trap General Exceptions. If this bit is set, and SCR_EL3.NS is set, then:
All exceptions that would be routed to EL1 are routed to EL2.
• The SCTLR.M bit is treated as 0 regardless of its actual state, other than for the purpose of
  reading the bit.
• The HCR.FMO,IMO, and AMO bits are treated as 1 regardless of their actual state, other
  than for the purpose of reading the bits.
• All virtual interrupts are disabled.
• Any implementation defined mechanisms for signaling virtual interrupts are disabled.
• An exception return to EL1 is treated as an illegal exception return.
Additionally, if HCR.TGE is 1, the HDCR.{TDRA,TDOSA,TDA} bits are ignored and the
processor behaves as if they are set to 1, other than for the value read back from HDCR.
The reset value is 0.

TVM, [26]
Trap Virtual Memory controls. When 1, this causes Writes to the EL1 virtual memory control
registers from EL1 to be trapped to EL2. This covers the following registers:
SCTLR, TTBR0, TTBR1, TTBCR, DACR, DFSR, IFSR, DFAR, IFAR, ADFSR, AIFSR,
PRRR/MAIR0, NMRR/MAIR1, AMAIR0, AMAIR1, and CONTEXTIDR.
The reset value is 0.

TTLB, [25]
Trap TLB maintenance instructions. When 1, this causes TLB maintenance instructions
executed from EL1 that are not UNDEFINED to be trapped to EL2. This covers the following
instructions:
TLBIALLIS, TLBIMVAIS, TLBIASIDIS, TLBIMVAAIS, TLBIALL, TLBIMVA, TLBIASID, TLBIMVAA,
TLBIMVALIS, TLBIMVAALIS, TLBIMVAL, and TLBIMVAAL.
The reset value is 0.

TPU, [24]
Trap Cache maintenance instructions to Point of Unification. When 1, this causes Cache
maintenance instructions to the point of unification executed from EL1 or EL0 that are not
UNDEFINED to be trapped to EL2. This covers the following instructions:
ICIMVAU, ICIALLU, ICIALLUIS, and DCCMVAU.
The reset value is 0.

TPC, [23]
Trap Data/Unified Cache maintenance operations to Point of Coherency. When 1, this causes
Data or Unified Cache maintenance instructions by address to the point of coherency executed
from EL1 or EL0 that are not UNDEFINED to be trapped to EL2. This covers the following
instructions:
DCIMVAC, DCCIMVAC, and DCCMVAC.
The reset value is 0.
TSW, [22]

Trap Data/Unified Cache maintenance operations by Set/Way. When 1, this causes Data or Unified Cache maintenance instructions by set/way executed from EL1 that are not undefined to be trapped to EL2. This covers the following instructions:

DCISW, DCCSW, and DCCISW.

The reset value is 0.

TAC, [21]

Trap ACTLR accesses. When this bit is set to 1, any valid Non-secure access to the ACTLR is trapped to Hyp mode.

The reset value is 0.

TIDCP, [20]

Trap Implementation Dependent functionality. When 1, this causes accesses to all CP15 MCR and MRC instructions executed from EL1, to be trapped to EL2 as follows:

- CRn is 9, Opcode1 is 0 to 7, CRm is c0, c1, c2, c5, c6, c7, c8, opcode2 is 0 to 7.
- CRn is 10, Opcode1 is 0 to 7, CRm is c0, c1, c4, c8, opcode2 is 0 to 7.
- CRn is 11, Opcode1 is 0 to 7, CRm is c0 to c8, or c15, opcode2 is 0 to 7.

Accesses from EL0 are undefined.

Resets to 0.

TSC, [19]

Trap SMC instruction. When this bit is set to 1, any attempt from a Non-secure EL1 state to execute an SMC instruction, that passes its condition check if it is conditional, is trapped to Hyp mode.

The reset value is 0.

TID3, [18]

Trap ID Group 3. When 1, this causes reads to the following registers executed from EL1 to be trapped to EL2:

ID_PFR0, ID_PFR1, ID_DFR0, ID_AFR0, ID_MMFR0, ID_MMFR1, ID_MMFR2, ID_MMFR3, ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, ID_ISAR4, ID_ISAR5, MVFR0, MVFR1, and MVFR2. Also MRC instructions to any of the following encodings:

- CP15, OPC1 is 0, CRn is 0, CRm is c3, c4, c5, c6, or c7, and Opc2 is 0 or 1.
- CP15, OpC1 is 0, CRn is 0, CRm is c3, and Opc2 is 2.
- CP15, OpC1 is 0, CRn is 0, CRm is 5, and Opc2 is 4 or 5.

The reset value is 0.

TID2, [17]

Trap ID Group 2. When 1, this causes reads (or writes to CSSELR) to the following registers executed from EL1 or EL0 if not undefined to be trapped to EL2:

CTR, CCSIDR, CLIDR, and CSSELR.

The reset value is 0.

TID1, [16]

Trap ID Group 1. When 1, this causes reads to the following registers executed from EL1 to be trapped to EL2:

TCMTR, TLBTR, AIDR, and REVIDR.

The reset value is 0.
TID0, [15]
Trap ID Group 0. When 1, this causes reads to the following registers executed from EL1 or
EL0 if not UNDEFINED to be trapped to EL2:
FPSID and JIDR.
The reset value is 0.

TWE, [14]
Trap WFE. When 1, this causes the WFE instruction executed from EL1 or EL0 to be trapped to
EL2 if the instruction would otherwise cause suspension of execution. For example, if the event
register is not set:
The reset value is 0.

TWI, [13]
Trap WFI. When 1, this causes the WFI instruction executed from EL1 or EL0 to be trapped to
EL2 if the instruction would otherwise cause suspension of execution. For example, if there is
not a pending WFI wake-up event:
The reset value is 0.

DC, [12]
Default cacheable. When this bit is set to 1, and the Non-secure EL1 and EL0 stage 1 MMU is
disabled, the memory type and attributes determined by the stage 1 translation is Normal, Non-
shareable, Inner Write-Back Write-Allocate, Outer Write-Back Write-Allocate.
The reset value is 0.

BSU, [11:10]
Barrier Shareability upgrade. The value in this field determines the minimum shareability
domain that is applied to any barrier executed from EL1 or EL0. The possible values are:
0b00  No effect.
0b01  Inner Shareable.
0b10  Outer Shareable.
0b11  Full System.
The reset value is 0.

FB, [9]
Force broadcast. When 1, this causes the following instructions to be broadcast within the Inner
Shareable domain when executed from Non-secure EL1:
TLBIALL, TLBIMVA, TLBIASID, TLBIMVAA, BPIALL, and ICIALLU.
The reset value is 0.

VA, [8]
Virtual Asynchronous Abort exception. When the AMO bit is set to 1, setting this bit signals a
virtual Asynchronous Abort exception to the Guest OS, when the processor is executing in Non-
secure state at EL0 or EL1.
The Guest OS cannot distinguish the virtual exception from the corresponding physical
exception.
The reset value is 0.
VI, [7]
Virtual IRQ exception. When the IMO bit is set to 1, setting this bit signals a virtual IRQ exception to the Guest OS, when the processor is executing in Non-secure state at EL0 or EL1. The Guest OS cannot distinguish the virtual exception from the corresponding physical exception.
The reset value is 0.

VF, [6]
Virtual FIQ exception. When the FMO bit is set to 1, setting this bit signals a virtual FIQ exception to the Guest OS, when the processor is executing in Non-secure state at EL0 or EL1. The Guest OS cannot distinguish the virtual exception from the corresponding physical exception.
The reset value is 0.

AMO, [5]
Asynchronous Abort Mask Override. When this is set to 1, it overrides the effect of CPSR.A, and enables virtual exception signaling by the VA bit.
The reset value is 0.

IMO, [4]
IRQ Mask Override. When this is set to 1, it overrides the effect of CPSR.I, and enables virtual exception signaling by the VI bit.
The reset value is 0.

FMO, [3]
FIQ Mask Override. When this is set to 1, it overrides the effect of CPSR.F, and enables virtual exception signaling by the VF bit.
The reset value is 0.

PTW, [2]
Protected Table Walk. When 1, if the stage 2 translation of a translation table access made as part of a stage 1 translation table walk at EL0 or EL1 maps that translation table access to Device memory, the access is faulted as a stage 2 Permission fault.
The reset value is 0.

SWIO, [1]
Set/Way Invalidation Override. When 1, this causes EL1 execution of the data cache invalidate by set/way instruction to be treated as data cache clean and invalidate by set/way. DCISW is executed as DCCISW.
This bit is RES1.

VM, [0]
Second stage of Translation enable. When 1, this enables the second stage of translation for execution in EL1 and EL0.
The reset value is 0.

To access the HCR:

MRC p15, 4, <Rt>, c1, c1, 0; Read Hyp Configuration Register
MCR p15, 4, <Rt>, c1, c1, 0; Write Hyp Configuration Register

Register access is encoded as follows:
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0001</td>
<td>000</td>
</tr>
</tbody>
</table>
**B1.62 Hyp Configuration Register 2**

The HCR2 characteristics are:

**Purpose**

Provides additional configuration controls for virtualization.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

This register is accessible only at EL2 or EL3.

**Attributes**

HCR2 is a 32-bit register.

![Figure B1-18 HCR2 bit assignments](image)

[31:2] Reserved, RES0.

**ID, [1]**

Stage 2 Instruction cache disable. When HCR.VM is 1, this forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable for the EL1/EL0 translation regime. The possible values are:

- 0 No effect on the stage 2 of the EL1/EL0 translation regime for instruction accesses.
- 1 Forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable for the EL0/EL1 translation regime.

**CD, [0]**

Stage 2 Data cache disable. When HCR.VM is 1, this forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable for the EL1/EL0 translation regime. The possible values are:

- 0 No effect on the stage 2 of the EL1/EL0 translation regime for data accesses and translation table walks.
- 1 Forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable for the EL0/EL1 translation regime.

To access the HCR2:

```
MRC p15,4,<Rt>,c1,c1,4 ; Read HCR2 into Rt
MCR p15,4,<Rt>,c1,c1,4 ; Write Rt to HCR2
```

Register access is encoded as follows:
Table B1-47  HCR2 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0001</td>
<td>100</td>
</tr>
</tbody>
</table>
B1.63 Hyp Debug Control Register

The HDCR characteristics are:

Purpose
Controls the trapping to Hyp mode of Non-secure accesses, at EL1 or lower, to functions provided by the debug and trace architectures and the Performance Monitor.

Usage constraints
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

Configurations
This register is accessible only at EL2 or EL3.

Attributes
HDCR is a 32-bit register.

Figure B1-19 HDCR bit assignments

[31:12]
Reserved, RES0.

Trap debug ROM address register access.

θ Has no effect on accesses to debug ROM address registers from EL1 and EL0.
1 Trap valid Non-secure EL1 and EL0 access to debug ROM address registers to Hyp mode.

When this bit is set to 1, any valid Non-secure access to the following registers is trapped to Hyp mode:
• DBGDRAR.
• DBGDSAR.

If HCR.TGE is 1 or HDCR.TDE is 1, then this bit is ignored and treated as though it is 1 other than for the value read back from HDCR.

On Warm reset, the field resets to 0.

TDOSA, [10]
Trap Debug OS-related register access:
θ Has no effect on accesses to CP14 Debug registers.
1 Trap valid Non-secure accesses to CP14 OS-related Debug registers to Hyp mode.

When this bit is set to 1, any valid Non-secure CP14 access to the following OS-related Debug registers is trapped to Hyp mode:

- DBGOSLSR.
- DBGOSLAR.
- DBGOSDLR.
- DBGPRCR.

If HCR.TGE is 1 or HDCR.TDE is 1, then this bit is ignored and treated as though it is 1 other than for the value read back from HDCR.

On Warm reset, the field resets to 0.

**TDA, [9]**

Trap Debug Access:

0 Has no effect on accesses to CP14 Debug registers.

1 Trap valid Non-secure accesses to CP14 Debug registers to Hyp mode.

When this bit is set to 1, any valid access to the CP14 Debug registers, other than the registers trapped by the TDRA and TDOASA bits, is trapped to Hyp mode.

If HCR.TGE is 1 or HDCR.TDE is 1, then this bit is ignored and treated as though it is 1 other than for the value read back from HDCR.

On Warm reset, the field resets to 0.

**TDE, [8]**

Trap Debug Exceptions:

0 Has no effect on Debug exceptions.

1 Route Non-secure Debug exceptions to Hyp mode.

When this bit is set to 1, any Debug exception taken in Non-secure state is trapped to Hyp mode.

If HCR.TGE is 1, then this bit is ignored and treated as though it is 1 other than for the value read back from HDCR. This bit resets to 0.

**HPME, [7]**

Hypervisor Performance Monitor Enable:

0 Hyp mode performance monitor counters disabled.

1 Hyp mode performance monitor counters enabled.

When this bit is set to 1, access to the performance monitors that are reserved for use from Hyp mode is enabled. For more information, see the description of the HPMN field.

The reset value of this bit is **UNKNOWN**.

**TPM, [6]**

Trap Performance Monitor accesses:

0 Has no effect on performance monitor accesses.

1 Trap valid Non-secure performance monitor accesses to Hyp mode.

When this bit is set to 1, any valid Non-secure access to the Performance Monitor registers is trapped to Hyp mode. This bit resets to 0. See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information.

**TPMCR, [5]**
Trap Performance Monitor Control Register accesses:

0  Has no effect on PMCR accesses.
1  Trap valid Non-secure PMCR accesses to Hyp mode.

When this bit is set to 1, any valid Non-secure access to the PMCR is trapped to Hyp mode. This bit resets to 0. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

HPMN, [4:0]

Hyp Performance Monitor count. Defines the number of Performance Monitors counters that are accessible from Non-secure EL1 and EL0 modes if unprivileged access is enabled.

In Non-secure state, HPMN divides the Performance Monitors counters as follows. If software is accessing Performance Monitors counter n then, in Non-secure state:

For example, If PMnEVCNTR is performance monitor counter n then, in Non-secure state:

- If \( n \) is in the range \( 0 \leq n < HPMN \), the counter is accessible from EL1 and EL2, and from EL0 if unprivileged access to the counters is enabled.
- If \( n \) is in the range \( HPMN \leq n < \text{PMCR.N} \), the counter is accessible only from EL2. The HPME bit enables access to the counters in this range.

If this field is set to 0, or to a value larger than PMCR.N, then the behavior in Non-secure EL0 and EL1 is CONSTRAINED UNPREDICTABLE, and one of the following must happen:

- The number of counters accessible is an UNKNOWN non-zero value less than PMCR.N.
- There is no access to any counters.

For reads of HDCR.HPMN by EL2 or higher, if this field is set to 0 or to a value larger than PMCR.N, the processor must return a CONSTRAINED UNPREDICTABLE value being one of:

- PMCR.N.
- The value that was written to HDCR.HPMN.
- (The value that was written to HDCR.HPMN) modulo \( 2^h \), where \( h \) is the smallest number of bits required for a value in the range 0 to PMCR.N.

This field resets to \( 0x6 \).

To access the HDCR:

```
MRC p15,4,<Rt>,c1,c1,1 ; Read HDCR into Rt
MCR p15,4,<Rt>,c1,c1,1 ; Write Rt to HDCR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0001</td>
<td>001</td>
</tr>
</tbody>
</table>

Table B1-48  HDCR access encoding
B1.64 Hyp Data Fault Address Register

The HDFAR characteristics are:

**Purpose**
Holds the virtual address of the faulting address that caused a synchronous Data Abort exception that is taken to Hyp mode.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

An execution in a Non-secure EL1 state, or in Secure state, makes the HDFAR UNKNOWN.

**Configurations**
HDFAR (S) is architecturally mapped to DFAR (S). See B1.48 Data Fault Address Register on page B1-216.

**Attributes**
HDFAR is a 32-bit register.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VA of faulting address of synchronous Data Abort exception |

**VA, [31:0]**
The Virtual Address of faulting address of synchronous Data Abort exception.

To access the HDFAR:

- MRC p15, 4, <Rt>, c6, c0, 0 ; Read HDFAR into Rt
- MCR p15, 4, <Rt>, c6, c0, 0 ; Write Rt to HDFAR

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0110</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>

Table B1-49 HDFAR access encoding
B1.65 Hyp Instruction Fault Address Register

The HIFAR characteristics are:

**Purpose**
Holds the virtual address of the faulting address that caused a synchronous Prefetch Abort exception that is taken to Hyp mode.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Execution in any Non-secure mode other than Hyp mode makes HPFAR UNKNOWN.

**Configurations**

HIFAR is architecturally mapped to IFAR (S). See B1.86 Instruction Fault Address Register on page B1-287.

**Attributes**

HIFAR is a 32-bit register.

![HIFAR bit assignments](image)

The Virtual Address of faulting address of synchronous Prefetch Abort exception.

To access the HIFAR:

```
MRC p15, 4, <Rt>, c6, c0, 2 ; Read HIFAR into Rt
MCR p15, 4, <Rt>, c6, c0, 2 ; Write Rt to HIFAR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0110</td>
<td>0000</td>
<td>010</td>
</tr>
</tbody>
</table>

**VA, [31:0]**

The Virtual Address of faulting address of synchronous Prefetch Abort exception.
B1.66 Hyp IPA Fault Address Register

The HPFAR characteristics are:

**Purpose**

Holds the faulting IPA for some aborts on a stage 2 translation taken to Hyp mode.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

Execution in any Non-secure mode other than Hyp mode makes HPFAR **UNKNOWN**.

**Configurations**

There are no configuration notes.

**Attributes**

HPFAR is a 32-bit register.

![Figure B1-22 HPFAR bit assignments](image)

**FIPA[39:12], [31:4]**

Bits [39:12] of the faulting intermediate physical address

**[3:0]**

Reserved, RES0

To access the HPFAR:

```
MRC p15, 4, <Rt>, c6, c0, 4 ; Read HPFAR into Rt
MCR p15, 4, <Rt>, c6, c0, 4 ; Write Rt to HPFAR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0110</td>
<td>0000</td>
<td>100</td>
</tr>
</tbody>
</table>
## B1.67 Hyp System Control Register

The HSCTLR characteristics are:

### Purpose

Provides top level control of the system operation in Hyp mode. This register provides Hyp mode control of features controlled by the Banked SCTLR bits, and shows the values of the non-Banked SCTLR bits.

### Usage constraints

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

### Configurations

There are no configuration notes.

### Attributes

HSCTLR is a 32-bit register.

![HSCTLR bit assignments](image)

**Figure B1-23 HSCTLR bit assignments**

### [31]

Reserved, RES0.

### TE, [30]

Thumb Exception enable. This bit controls whether exceptions taken in Hyp mode are taken in A32 or T32 state:

- 0: Exceptions taken in A32 state.
- 1: Exceptions taken in T32 state.

### [29:28]

Reserved, RES1.

### [27:26]

Reserved, RES0.

### EE, [25]

Exception Endianness. The value of this bit defines the value of the CPSR.E bit on entry to an exception vector, including reset. This value also indicates the endianness of the translation table data for translation table lookups:

- 0: Little endian.
- 1: Big endian.
Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Reserved, RES1.

Reserved, RES0.

Instruction cache enable. This is an enable bit for instruction caches at EL2:

0 Instruction caches disabled at EL2. If HSCTRL.M is set to 0, instruction accesses from stage 1 of the EL2 translation regime are to Normal memory, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable.

1 Instruction caches enabled at EL2. If HSCTRL.M is set to 0, instruction accesses from stage 1 of the EL2 translation regime are to Normal memory, Outer Shareable, Inner Write-Through, Outer Write-Through.

When this bit is 0, all EL2 Normal memory instruction accesses are Non-cacheable.

If this register is at the highest exception level implemented, field resets to 0. Otherwise, its reset value is UNKNOWN.
SETEND Disable:
0  The SETEND instruction is available.
1  The SETEND instruction is UNALLOCATED.

ITD, [7]
IT Disable:
0  The IT instruction functionality is available.
1  All encodings of the IT instruction with hw1[3:0]!=1000 are UNDEFINED and treated as unallocated. All encodings of the subsequent instruction with the following values for hw1 are UNDEFINED (and treated as unallocated):

11xxxxxxxxxxxxxx  All 32-bit instructions, B(2), B(1), Undefined, SVC, Load/Store multiple
1x11xxxxxxxxxxx  Miscellaneous 16-bit instructions
1x100xxxxxxxxxx  ADD Rd, PC, #imm
01001xxxxxxxxxx  LDR Rd, [PC, #imm]
0100x1xxx1111xxx  ADD(4),CMP(3), MOV, BX pc, BLX pc
010001xx1xxxx111  ADD(4),CMP(3), MOV

[6]
Reserved, RES0.

CP15BEN, [5]
CP15 barrier enable:
0  CP15 barrier operations disabled. Their encodings are UNDEFINED.
1  CP15 barrier operations enabled.

[4:3]
Reserved, RES1.

C, [2]
Cache enable. This is an enable bit for data and unified caches at EL2:
0  Data and unified caches disabled at EL2.
1  Data and unified caches enabled at EL2.

When this bit is 0, all EL2 Normal memory data accesses and all accesses to the EL2 translation tables are Non-cacheable.

If this register is at the highest exception level implemented, field resets to 0. Otherwise, its reset value is UNKNOWN.

A, [1]
Alignment check enable. This is the enable bit for Alignment fault checking:
0  Alignment fault checking disabled.
1  Alignment fault checking enabled.

When this bit is 1, all instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, that is taken as a Data Abort exception.
Load/store exclusive and load-acquire/store-release instructions have this alignment check regardless of the value of the A bit.

If this register is at the highest exception level implemented, field resets to 0. Otherwise, its reset value is \texttt{UNKNOWN}.

\textbf{M, [0]}

MMU enable. This is a global enable bit for the EL2 stage 1 MMU:

\begin{itemize}
  \item 0 \quad \text{EL2 stage 1 MMU disabled.}
  \item 1 \quad \text{EL2 stage 1 MMU enabled.}
\end{itemize}

If this register is at the highest exception level implemented, field resets to 0. Otherwise, its reset value is \texttt{UNKNOWN}.

To access the HSCTLR:

\begin{verbatim}
MRC p15,4,<Rt>,c1,c0,0 ; Read HSCTLR into Rt
MCR p15,4,<Rt>,c1,c0,0 ; Write Rt to HSCTLR
\end{verbatim}

Register access is encoded as follows:

\begin{table}[h]
\centering
\caption{HSCTLR access encoding}
\begin{tabular}{|c|c|c|c|}
\hline
\text{coproc} & \text{opc1} & \text{CRn} & \text{CRm} & \text{opc2} \\
\hline
1111 & 100 & 0001 & 0000 & 000 \\
\hline
\end{tabular}
\end{table}
B1.68 Hyp Syndrome Register

The HSR characteristics are:

**Purpose**

Holds syndrome information for an exception taken to Hyp mode.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>RW</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

This register is accessible only at EL2 or EL3.

**Attributes**

HSR is a 32-bit register.

| 31 | 26 25 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EC | ISS     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**EC, [31:26]**

Exception class. The exception class for the exception that is taken in Hyp mode. See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information.

**IL, [25]**

Instruction length. See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information.

**ISS, [24:0]**

Instruction specific syndrome. See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information. The interpretation of this field depends on the value of the EC field. See *B1.52 Encoding of ISS[24:20] when HSR[31:30] is 0b00* on page B1-222.
B1.69  **Hyp System Trap Register**

The HSTR characteristics are:

**Purpose**

Controls trapping to Hyp mode of Non-secure accesses, at EL1 or lower, of use of T32EE, or the CP15 primary registers, \{c0-c3,c5-c13,c15\}.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

This register is accessible only at EL2 or EL3.

**Attributes**

HSTR is a 32-bit register.

---

**[31:17]**

Reserved, RES0.

**TTEE, [16]**

Trap T32EE. This value is:

0 T32EE is not supported.

**T15, [15]**

Trap coprocessor primary register CRn = 15. The possible values are:

0 Has no effect on Non-secure accesses to CP15 registers.

1 Trap valid Non-secure accesses to coprocessor primary register CRn = 15 to Hyp mode.

The reset value is 0.

---

**[14]**

Reserved, RES0.
T13, [13]
Trap coprocessor primary register CRn = 13. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 13 to Hyp mode.

The reset value is 0.

T12, [12]
Trap coprocessor primary register CRn = 12. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 12 to Hyp mode.

The reset value is 0.

Trap coprocessor primary register CRn = 11. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 11 to Hyp mode.

The reset value is 0.

T10, [10]
Trap coprocessor primary register CRn = 10. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 10 to Hyp mode.

The reset value is 0.

T9, [9]
Trap coprocessor primary register CRn = 9. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 9 to Hyp mode.

The reset value is 0.

T8, [8]
Trap coprocessor primary register CRn = 8. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 8 to Hyp mode.

The reset value is 0.

T7, [7]
Trap coprocessor primary register CRn = 7. The possible values are:

0  Has no effect on Non-secure accesses to CP15 registers.
1  Trap valid Non-secure accesses to coprocessor primary register CRn = 7 to Hyp mode.

The reset value is 0.
T6, [6]

Trap coprocessor primary register CRn = 6. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 6 to Hyp mode.

The reset value is 0.

T5, [5]

Trap coprocessor primary register CRn = 5. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 5 to Hyp mode.

The reset value is 0.

[4]
Reserved, RES0.

T3, [3]

Trap coprocessor primary register CRn = 3. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 3 to Hyp mode.

The reset value is 0.

T2, [2]

Trap coprocessor primary register CRn = 2. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 2 to Hyp mode.

The reset value is 0.

T1, [1]

Trap coprocessor primary register CRn = 1. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 1 to Hyp mode.

The reset value is 0.

T0, [0]

Trap coprocessor primary register CRn = 0. The possible values are:
0    Has no effect on Non-secure accesses to CP15 registers.
1    Trap valid Non-secure accesses to coprocessor primary register CRn = 0 to Hyp mode.

The reset value is 0.

To access the HSTR:

\[
\text{MRC p15, 4, <Rt>, c1, c1, 3} \; \text{Read HSTR into Rt}
\]

\[
\text{MCR p15, 4, <Rt>, c1, c1, 3} \; \text{Write Rt to HSTR}
\]

Register access is encoded as follows:
Table B1-53  HSTR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0001</td>
<td>0001</td>
<td>011</td>
</tr>
</tbody>
</table>
**B1.70 Hyp Translation Control Register**

The HTCR characteristics are:

**Purpose**
Controls translation table walks required for the stage 1 translation of memory accesses from Hyp mode, and holds cacheability and shareability information for the accesses.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**
There are no configuration notes.

**Attributes**
HTCR is a 32-bit register.

Figure B1-26 HTCR bit assignments

[31]
Reserved, RES1.

[30:24]
Reserved, RES0.

[23]
Reserved, RES1.

[22:14]
Reserved, RES0.

**SH0, [13:12]**
Shareability attribute for memory associated with translation table walks using TTBR0. The possible values are:

- 0b00 Non-shareable.
- 0b01 Reserved.
- 0b10 Outer shareable.
- 0b11 Inner shareable.

** ORGN0, [11:10]**
Outer cacheability attribute for memory associated with translation table walks using TTBR0. The possible values are:

- 0b00 Normal memory, Outer Non-cacheable.
- 0b01 Normal memory, Outer Write-Back Write-Allocate Cacheable.
- 0b10 Normal memory, Outer Write-Through Cacheable.
Normal memory, Outer Write-Back no Write-Allocate Cacheable.

**IRGN0, [9:8]**

Inner cacheability attribute for memory associated with translation table walks using TTBR0. The possible values are:

- **0b00**: Normal memory, Inner Non-cacheable.
- **0b01**: Normal memory, Inner Write-Back Write-Allocate Cacheable.
- **0b10**: Normal memory, Inner Write-Through Cacheable.
- **0b11**: Normal memory, Inner Write-Back no Write-Allocate Cacheable.

**[7:3]**

Reserved, RES0.

**T0SZ, [2:0]**

Size offset of the memory region addressed by TTBR0. The region size is $2^{(32-TSIZE)}$ bytes.

The processor does not use the implementation-defined bit, HTCR[30], so this bit is RES0.

To access the HTCR:

- **MRC p15, 4, <Rt>, c2, c0, 2**: Read HTCR into Rt
- **MCR p15, 4, <Rt>, c2, c0, 2**: Write Rt to HTCR

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0010</td>
<td>0000</td>
<td>010</td>
</tr>
</tbody>
</table>

Table B1-54 HTCR access encoding
B1.71 Hyp Vector Base Address Register

The HVBAR characteristics are:

**Purpose**

Holds the exception base address for any exception that is taken to Hyp mode.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

There are no configuration notes.

**Attributes**

HVBAR is a 32-bit register.

![HVBAR bit assignments](image)

**Vector Base Address, [31:5]**

Bits[31:5] of the base address of the exception vectors, for exceptions taken in this exception level. Bits[4:0] of an exception vector are the exception offset.

**[4:0]**

Reserved, RES0.

To access the HVBAR:

```
MRC p15, 4, <Rt>, c12, c0, 0 ; Read HVBAR into Rt
MCR p15, 4, <Rt>, c12, c0, 0 ; Write Rt to HVBAR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>1100</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.72 **Auxiliary Feature Register 0**

**ID_AFR0**

The processor does not implement ID_AFR0. This register is always RES0.
B1.73  Debug Feature Register 0

The ID_DFR0 characteristics are:

Purpose
Provides top level information about the debug system in AArch32.

Usage constraints
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

- Must be interpreted with the Main ID Register, MIDR.

Configurations
There is one copy of this register that is used in both Secure and Non-secure states.

Attributes
ID_DFR0 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>PerfMon</td>
<td>MProfDbg</td>
<td>MMapTrc</td>
<td>CopTrc</td>
<td>Reserved</td>
<td>CopSDbg</td>
<td>CopDbg</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure B1-28  ID_DFR0 bit assignments

[31:28]
Reserved, RES0.

PerfMon, [27:24]
Indicates support for performance monitor model:
0x3  Support for Performance Monitor Unit version 3 (PMUv3) system registers.

MProfDbg, [23:20]
Indicates support for memory-mapped debug model for M profile processors:
0x0  Processor does not support M profile Debug architecture.

MMapTrc, [19:16]
Indicates support for memory-mapped trace model:
0x0  ETM is not implemented.
0x1  Support for Arm trace architecture, with memory-mapped access.

In the Trace registers, the ETMIDR gives more information about the implementation.

CopTrc, [15:12]
Indicates support for coprocessor-based trace model:
0x0  Processor does not support Arm trace architecture, with CP14 access.

[11:8]
Reserved, RAZ.

CopSDbg, [7:4]
Indicates support for coprocessor-based Secure debug model:

\( \mathbf{0x6} \) Processor supports v8 Debug architecture, with CP14 access.

**CopDbg, [3:0]**

Indicates support for coprocessor-based debug model:

\( \mathbf{0x6} \) Processor supports v8 Debug architecture, with CP14 access.

To access the ID_DFR0:

\[
\text{MRC p15,0,<Rt>,c0,c1,2} \ ; \text{Read ID_DFR0 into Rt}
\]

Register access is encoded as follows:

<table>
<thead>
<tr>
<th></th>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>1111</strong></td>
<td><strong>000</strong></td>
<td><strong>0000</strong></td>
<td><strong>0001</strong></td>
<td><strong>010</strong></td>
<td></td>
</tr>
</tbody>
</table>

**Table B1-56** ID_DFR0 access encoding
B1.74 Instruction Set Attribute Register 0

The ID_ISAR0 characteristics are:

**Purpose**
Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_ISAR1, ID_ISAR2, ID_ISAR3, ID_ISAR4, and ID_ISAR5. See:
- B1.75 Instruction Set Attribute Register 1 on page B1-265
- B1.76 Instruction Set Attribute Register 2 on page B1-267
- B1.77 Instruction Set Attribute Register 3 on page B1-269
- B1.78 Instruction Set Attribute Register 4 on page B1-271
- B1.79 Instruction Set Attribute Register 5 on page B1-273

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_ISAR0 is a 32-bit register.

```
 31  28  27  24  23  20  19  16  15  12  11  8  7  4  3  0
 RES0  Divide  Debug  Coproc  CmpBranch  Bitfield  BitCount  Swap
```

**Figure B1-29** ID_ISAR0 bit assignments

- **[31:28]**
  Reserved, RES0.

- **Divide, [27:24]**
  Indicates the implemented Divide instructions:
  - $0x2$
    - SDIV and UDIV in the T32 instruction set.
    - SDIV and UDIV in the A32 instruction set.

- **Debug, [23:20]**
  Indicates the implemented Debug instructions:
  - $0x1$
    - BKPT.

- **Coproc, [19:16]**
  Indicates the implemented Coprocessor instructions:
  - $0x0$
    - None implemented, except for separately attributed by the architecture including CP15, CP14, Advanced SIMD and floating-point.

- **CmpBranch, [15:12]**
  Indicates the implemented combined Compare and Branch instructions in the T32 instruction set:
0x1  CBNZ and CBZ.

**Bitfield, [11:8]**

Indicates the implemented bit field instructions:

0x1  BFC, BFI, SBFX, and UBFX.

**BitCount, [7:4]**

Indicates the implemented Bit Counting instructions:

0x1  CLZ.

**Swap, [3:0]**

Indicates the implemented Swap instructions in the A32 instruction set:

0x0  None implemented.

To access the ID_ISAR0:

```
MRC p15, 0, <Rt>, c0, c2, 0 ; Read ID_ISAR0 into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>000</td>
</tr>
</tbody>
</table>

Table B1-57  ID_ISAR0 access encoding
**B1.75 Instruction Set Attribute Register 1**

The ID_ISAR1 characteristics are:

**Purpose**
Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_ISAR0, ID_ISAR2, ID_ISAR3, ID_ISAR4 and ID_ISAR5. See:
- *B1.74 Instruction Set Attribute Register 0* on page B1-263
- *B1.76 Instruction Set Attribute Register 2* on page B1-267
- *B1.77 Instruction Set Attribute Register 3* on page B1-269
- *B1.78 Instruction Set Attribute Register 4* on page B1-271
- *B1.79 Instruction Set Attribute Register 5* on page B1-273

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_ISAR1 is a 32-bit register.

![Figure B1-30 ID_ISAR1 bit assignments](image)

**Jazelle, [31:28]**
Indicates the implemented Jazelle state instructions:
- 0x1 The BXJ instruction, and the J bit in the PSR.

**Interwork, [27:24]**
Indicates the implemented Interworking instructions:
- 0x3 The BX instruction, and the T bit in the PSR.
- The BLX instruction. The PC loads have BX-like behavior.
- Data-processing instructions in the A32 instruction set with the PC as the destination and the S bit clear, have BX-like behavior.

**Immediate, [23:20]**
Indicates the implemented data-processing instructions with long immediates:
- 0x1 The MOV instruction.
- The MOV instruction encodings with zero-extended 16-bit immediates.
- The T32 ADD and SUB instruction encodings with zero-extended 12-bit immediates, and other ADD, ADR, and SUB encodings cross-referenced by the pseudocode for those encodings.

**IfThen, [19:16]**
Indicates the implemented If-Then instructions in the T32 instruction set:
0x1  The IT instructions, and the IT bits in the PSRs.

**Extend, [15:12]**
Indicates the implemented Extend instructions:
0x2  • The SXTB, SXTH, UXTB, and UXTH instructions.
     • The SXTB16, SXTAB, SXTAB16, SXTAH, UXTB16, UXTAB, UXTAB16, and UXTAH instructions.

**Except_AR, [11:8]**
Indicates the implemented A profile exception-handling instructions:
0x1  The SRS and RFE instructions, and the A profile forms of the CPS instruction.

**Except, [7:4]**
Indicates the implemented exception-handling instructions in the A32 instruction set:
0x1  The LDM (exception return), LDM (user registers), and STM (user registers) instruction versions.

**Endian, [3:0]**
Indicates the implemented Endian instructions:
0x1  The SETEND instruction, and the E bit in the PSRs.

To access the ID_ISAR1:

MRC p15, 0, <Rt>, c0, c2, 1 ; Read ID_ISAR1 into Rt

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>001</td>
</tr>
</tbody>
</table>

**Table B1-58  ID_ISAR1 access encoding**
B1.76 Instruction Set Attribute Register 2

The ID_ISAR2 characteristics are:

**Purpose**
Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR3, ID_ISAR4 and ID_ISAR5. See:

- B1.74 Instruction Set Attribute Register 0 on page B1-263
- B1.75 Instruction Set Attribute Register 1 on page B1-265
- B1.77 Instruction Set Attribute Register 3 on page B1-269
- B1.78 Instruction Set Attribute Register 4 on page B1-271
- B1.79 Instruction Set Attribute Register 5 on page B1-273

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_ISAR2 is a 32-bit register.

![Figure B1-31 ID_ISAR2 bit assignments](image)

**Reversal, [31:28]**
Indicates the implemented Reversal instructions:

- 0x2: The REV, REV16, and REVSH instructions.
- The RBIT instruction.

**PSR_AR, [27:24]**
Indicates the implemented A and R profile instructions to manipulate the PSR:

- 0x1: The MRS and MSR instructions, and the exception return forms of data-processing instructions.

The exception return forms of the data-processing instructions are:
- In the A32 instruction set, data-processing instructions with the PC as the destination and the S bit set.
- In the T32 instruction set, the SUBS PC, LR, #N instruction.

**MultU, [23:20]**
Indicates the implemented advanced unsigned Multiply instructions:
The UMULL and UMLAL instructions.
The UMAAL instruction.

MultS, [19:16]
Indicates the implemented advanced signed Multiply instructions.

\[ \text{0x}3 \]
- The SMULL and SMLAL instructions.
- The SMLABB, SMLABT, SMLALBB, SMLALBT, SMLALTB, SMLATB, SMLATT, SMLAWB, SMLAWT, SMULBB, SMULTBB, SMULBT, SMULTBB, SMULTT, SMULWB, SMULWT instructions, and the Q bit in the PSRs.
- The SMLAD, SMLADX, SMLALD, SMLALDX, SMLSD, SMLSDX, SMLSLD, SMLSLDX, SMMLA, SMMLAR, SMMLAS, SMMLSR, SMMLUL, SMMLULR, SMUAD, SMUADX, SMUSD, and SMUSDX instructions.

Mult, [15:12]
Indicates the implemented additional Multiply instructions:

\[ \text{0x}2 \]
The MUL instruction.
The MLA instruction.
The MLS instruction.

MultiAccessInt, [11:8]
Indicates the support for interruptible multi-access instructions:

\[ \text{0x}0 \]
No support. This means the LDM and STM instructions are not interruptible.

MemHint, [7:4]
Indicates the implemented memory hint instructions:

\[ \text{0x}4 \]
The PLD instruction.
The PLI instruction.
The PLDW instruction.

LoadStore, [3:0]
Indicates the implemented additional load/store instructions:

\[ \text{0x}2 \]
The LDRD and STRD instructions.
The Load Acquire (LDAB, LDAH, LDA, LDAEXB, LDAEXH, LDAEX, and LDAEXD) and Store Release (STLB, STLH, STL, STLEXB, STLEXH, STLEX, and STLEXD) instructions.

To access the ID_ISAR2:

\[ \text{MRC p15, 0, } \text{<Rt>, c0, c2, 2 ; Read ID_ISAR2 into Rt} \]

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>Table B1-59 ID_ISAR2 access encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>coproc</td>
</tr>
<tr>
<td>1111</td>
</tr>
</tbody>
</table>
B1.77  Instruction Set Attribute Register 3

The ID_ISAR3 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR4, and ID_ISAR5. See:

- B1.74 Instruction Set Attribute Register 0 on page B1-263
- B1.75 Instruction Set Attribute Register 1 on page B1-265
- B1.76 Instruction Set Attribute Register 2 on page B1-267
- B1.78 Instruction Set Attribute Register 4 on page B1-271
- B1.79 Instruction Set Attribute Register 5 on page B1-273

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_ISAR3 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>16</th>
<th>12</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ThumbEE</td>
<td>TrueNOP</td>
<td>ThumbCopy</td>
<td>TabBranch</td>
<td>SynchPrim</td>
<td>SVC</td>
<td>SIMD</td>
<td>Saturate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ThumbEE, [31:28]**

Indicates the implemented Thumb Execution Environment (T32EE) instructions:

0x0  None implemented.

**TrueNOP, [27:24]**

Indicates support for True NOP instructions:

0x1  True NOP instructions in both the A32 and T32 instruction sets, and additional NOP-compatible hints.

**ThumbCopy, [23:20]**

Indicates the support for T32 non flag-setting MOV instructions:

0x1  Support for T32 instruction set encoding T1 of the MOV (register) instruction, copying from a low register to a low register.

**TabBranch, [19:16]**

Indicates the implemented Table Branch instructions in the T32 instruction set.

0x1  The TBB and TBH instructions.

**SynchPrim, [15:12]**
Indicates the implemented Synchronization Primitive instructions.

\( \text{0x2} \)
- The LDREX and STREX instructions.
- The CLREX, LDREXB, STREXB, and STREXH instructions.
- The LDREXD and STREXD instructions.

**SVC, [11:8]**
Indicates the implemented SVC instructions:

\( \text{0x1} \)
- The SVC instruction.

**SIMD, [7:4]**
Indicates the implemented Single Instruction Multiple Data (SIMD) instructions.

\( \text{0x3} \)
- The SSAT and USAT instructions, and the Q bit in the PSRs.
- The PKHBT, PKHTB, QADD16, QADD8, QASX, QSUB16, QSUB8, QSAX, SADD16, SADD8, SASX, SEL, SHADD16, SHADD8, SHASX, SHSUB16, SHSUB8, SHSAX, SSAT16, SSUB16, SSUB8, SSAX, SXTAB16, SXTB16, UADD16, UADD8, UASX, UHADD16, UHADD8, UHASX, UHSUB16, UHSUB8, UHSAX, UQADD16, UQADD8, UQASX, UQSUB16, UQSUB8, UQSAX, USAD8, USADA8, USAT16, USUB16, USUB8, USAX, UXTAB16, UXTB16 instructions, and the GE[3:0] bits in the PSRs.

**Saturate, [3:0]**
Indicates the implemented Saturate instructions:

\( \text{0x1} \)
- The QADD, QDADD, QDSUB, QSUB and the Q bit in the PSRs.

To access the ID_ISAR3:

\[
\text{MRC p15, 0, } <Rt>, c0, c2, 3 ; \text{Read ID_ISAR3 into Rt}
\]

Register access is encoded as follows:

**Table B1-60**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>011</td>
</tr>
</tbody>
</table>
**B1.78  Instruction Set Attribute Register 4**

The ID_ISAR4 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the processor in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, and ID_ISAR5. See:

- *B1.74 Instruction Set Attribute Register 0 on page B1-263*
- *B1.75 Instruction Set Attribute Register 1 on page B1-265*
- *B1.76 Instruction Set Attribute Register 2 on page B1-267*
- *B1.77 Instruction Set Attribute Register 3 on page B1-269*
- *B1.79 Instruction Set Attribute Register 5 on page B1-273*

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_ISAR4 is a 32-bit register.

![Figure B1-33  ID_ISAR4 bit assignments](image)

**SWP_frac, [31:28]**

Indicates support for the memory system locking the bus for SWP or SWPB instructions:

0x0  SWP and SWPB instructions not implemented.

**PSR_M, [27:24]**

Indicates the implemented M profile instructions to modify the PSRs:

0x0  None implemented.

**SynchPrim_frac, [23:20]**

This field is used with the ID_ISAR3.SynchPrim field to indicate the implemented Synchronization Primitive instructions:

0x0  
- The LDREX and STREX instructions.
- The CLREX, LDREXB, LDREXH, STREXB, and STREXH instructions.
- The LDREXD and STREXD instructions.

**Barrier, [19:16]**

Indicates the supported Barrier instructions in the A32 and T32 instruction sets:

0x1  The DMB, DSB, and ISB barrier instructions.
SMC, [15:12]
Indicates the implemented SMC instructions:

0x1  The SMC instruction.

Writeback, [11:8]
Indicates the support for writeback addressing modes:

0x1  Processor supports all of the writeback addressing modes defined in Armv8.

WithShifts, [7:4]
Indicates the support for instructions with shifts:

0x4  • Support for shifts of loads and stores over the range LSL 0-3.
     • Support for other constant shift options, both on load/store and other instructions.
     • Support for register-controlled shift options.

Unpriv, [3:0]
Indicates the implemented unprivileged instructions:

0x2  • The LDRBT, LDRT, STRBT, and STRT instructions.
     • The LDRHT, LDRSBT, LDRSHT, and STRHT instructions.

To access the ID_ISAR4:

MRC p15, 0, <Rt>, c0, c2, 4 ; Read ID_ISAR4 into Rt

Register access is encoded as follows:

Table B1-61  ID_ISAR4 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>100</td>
</tr>
</tbody>
</table>
**B1.79 Instruction Set Attribute Register 5**

The ID_ISAR5 characteristics are:

**Purpose**

Provides information about the instruction sets that the processor implements.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

ID_ISAR5 must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, and ID_ISAR4. See:

- *B1.74 Instruction Set Attribute Register 0* on page B1-263
- *B1.75 Instruction Set Attribute Register 1* on page B1-265
- *B1.76 Instruction Set Attribute Register 2* on page B1-267
- *B1.77 Instruction Set Attribute Register 3* on page B1-269
- *B1.78 Instruction Set Attribute Register 4* on page B1-271

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_ISAR5 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>CRC32</td>
<td>SHA2</td>
<td>SHA1</td>
<td>AES</td>
<td>SEVL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure B1-34 ID_ISAR5 bit assignments**

[31:20] Reserved, RES0.

**CRC32, [19:16]**

Indicates whether CRC32 instructions are implemented in AArch32 state:

- 0x1 CRC32 instructions are implemented.

**SHA2, [15:12]**

Indicates whether SHA2 instructions are implemented in AArch32 state:

- 0x0 Cryptographic Extensions are not implemented or are disabled.
- 0x1 SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 instructions are implemented.

See the *Cortex®-A32 Processor Cryptographic Extension Technical Reference Manual* for more information.

**SHA1, [11:8]**

Indicates whether SHA1 instructions are implemented in AArch32 state:

- 0x0 Cryptographic Extensions are not implemented or are disabled.
- 0x1 SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions are implemented.
See the *Cortex®-A32 Processor Cryptographic Extension Technical Reference Manual* for more information.

**AES, [7:4]**

Indicates whether AES instructions are implemented in AArch32 state:

- 0x0    Cryptographic Extensions are not implemented or are disabled.
- 0x2    AESE, AESD, AESMC and AESIMC, plus PMULL and PMULL2 instructions operating on 64-bit data.

See the *Cortex®-A32 Processor Cryptographic Extension Technical Reference Manual* for more information.

**SEVL, [3:0]**

Indicates whether the SEVL instruction is implemented:

- 0x1    SEVL implemented to send event local.

To access the ID_ISAR5:

```assembly
MRC p15,0,<Rt>,c0,c2,5 ; Read ID_ISAR5 into Rt
```

Register access is encoded as follows:

### Table B1-62  ID_ISAR5 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0010</td>
<td>101</td>
</tr>
</tbody>
</table>
B1.80 Memory Model Feature Register 0

The ID_MMFR0 characteristics are:

**Purpose**
Provides information about the memory model and memory management support in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_MMFR1, ID_MMFR2, and ID_MMFR3. See:
- *B1.81 Memory Model Feature Register 1* on page B1-277
- *B1.82 Memory Model Feature Register 2* on page B1-279
- *B1.83 Memory Model Feature Register 3* on page B1-281

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_MMFR0 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>InnerShr</td>
<td>FCSE</td>
<td>AuxReg</td>
<td>TCM</td>
<td>ShareLvl</td>
<td>OuterShr</td>
<td>PMSA</td>
<td>VMSA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure B1-35 ID_MMFR0 bit assignments**

**InnerShr, [31:28]**
Indicates the innermost shareability domain implemented:
- $0x1$ Implemented with hardware coherency support.

**FCSE, [27:24]**
Indicates support for Fast Context Switch Extension (FCSE):
- $0x0$ Not supported.

**AuxReg, [23:20]**
Indicates support for Auxiliary registers:
- $0x2$ Support for Auxiliary Fault Status Registers (AIFSR and ADFSR) and Auxiliary Control Register.

**TCM, [19:16]**
Indicates support for TCMs and associated DMAs:
- $0x0$ Not supported.

**ShareLvl, [15:12]**
Indicates the number of shareability levels implemented:
- $0x1$ Two levels of shareability implemented.
**OuterShr, [11:8]**

Indicates the outermost shareability domain implemented:

- 0x1    Implemented with hardware coherency support.

**PMSA, [7:4]**

Indicates support for a *Protected Memory System Architecture* (PMSA):

- 0x0    Not supported.

**VMSA, [3:0]**

Indicates support for a *Virtual Memory System Architecture* (VMSA).

- 0x5    Support for:
  - VMSAv7, with support for remapping and the Access flag.
  - The PXN bit in the Short-descriptor translation table format descriptors.
  - The Long-descriptor translation table format.

To access the ID_MMFR0:

```
MRC p15,0,<Rt>,c0,c1,4 ; Read ID_MMFR0 into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>100</td>
</tr>
</tbody>
</table>

Table B1-63  ID_MMFR0 access encoding
B1.81 Memory Model Feature Register 1

The ID_MMFR1 characteristics are:

**Purpose**
Provides information about the memory model and memory management support in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_MMFR0, ID_MMFR2, and ID_MMFR3. See:
- B1.80 Memory Model Feature Register 0 on page B1-275
- B1.82 Memory Model Feature Register 2 on page B1-279
- B1.83 Memory Model Feature Register 3 on page B1-281

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_MMFR1 is a 32-bit register.

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BPred</td>
<td>L1TstCln</td>
<td>L1Uni</td>
<td>L1Hvd</td>
<td>L1UniSW</td>
<td>L1HvdSW</td>
<td>L1UniVA</td>
<td>L1HvdVA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure B1-36 ID_MMFR1 bit assignments**

**BPred, [31:28]**
Indicates branch predictor management requirements:
- 0x4 For execution correctness, branch predictor requires no flushing at any time.

**L1TstCln, [27:24]**
Indicates the supported L1 Data cache test and clean operations, for Harvard or unified cache implementation:
- 0x0 None supported.

**L1Uni, [23:20]**
Indicates the supported entire L1 cache maintenance operations, for a unified cache implementation:
- 0x0 None supported.

**L1Hvd, [19:16]**
Indicates the supported entire L1 cache maintenance operations, for a Harvard cache implementation:
- 0x0 None supported.

**L1UniSW, [15:12]**
Indicates the supported L1 cache line maintenance operations by set/way, for a unified cache implementation:

0x0     None supported.

L1HvdSW, [11:8]
Indicates the supported L1 cache line maintenance operations by set/way, for a Harvard cache implementation:

0x0     None supported.

L1UniVA, [7:4]
Indicates the supported L1 cache line maintenance operations by MVA, for a unified cache implementation:

0x0     None supported.

L1HvdVA, [3:0]
Indicates the supported L1 cache line maintenance operations by MVA, for a Harvard cache implementation:

0x0     None supported.

To access the ID_MMFR1:

MRC p15, 0, <Rt>, c0, c1, 5; Read ID_MMFR1 into Rt

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>101</td>
</tr>
</tbody>
</table>

Table B1-64  ID_MMFR1 access encoding
B1.82 Memory Model Feature Register 2

The ID_MMFR2 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_MMFR0, ID_MMFR1, and ID_MMFR3. See:

- B1.80 Memory Model Feature Register 0 on page B1-275
- B1.81 Memory Model Feature Register 1 on page B1-277
- B1.83 Memory Model Feature Register 3 on page B1-281

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_MMFR2 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>HWAccFlg</td>
<td>WFIStall</td>
<td>MemBarr</td>
<td>UniTLB</td>
<td>HvdTLB</td>
<td>LL1HvdRng</td>
<td>L1HvdBG</td>
<td>L1HvdFG</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HWAccFlg, [31:28]**

Hardware Access Flag. Indicates support for a Hardware Access flag, as part of the VMSAv7 implementation:

0x0 Not supported.

**WFIStall, [27:24]**

Wait For Interrupt Stall. Indicates the support for *Wait For Interrupt* (WFI) stalling:

0x1 Support for WFI stalling.

**MemBarr, [23:20]**

Memory Barrier. Indicates the supported CP15 memory barrier operations.

0x2 Supported CP15 memory barrier operations are:

- *Data Synchronization Barrier* (DSB).
- *Instruction Synchronization Barrier* (ISB).
- *Data Memory Barrier* (DMB).

**UniTLB, [19:16]**

Unified TLB. Indicates the supported TLB maintenance operations, for a unified TLB implementation.
0x6 Supported unified TLB maintenance operations are:
  • Invalidate all entries in the TLB.
  • Invalidate TLB entry by MVA.
  • Invalidate TLB entries by ASID match.
  • Invalidate instruction TLB and data TLB entries by MVA All ASID. This is a shared unified TLB operation.
  • Invalidate Hyp mode unified TLB entry by MVA.
  • Invalidate entire Non-secure EL1 and EL0 unified TLB.
  • Invalidate entire Hyp mode unified TLB.
  • TLBIMVALIS, TLBIMVAALIS, TLBIMVALHIS, TLBIMVAL, TLBIMVAAL, and TLBIMVALH.
  • TLBIIPAS2IS, TLBIIPAS2LIS, TLBIIPAS2, and TLBIIPAS2L.

HvdTLB, [15:12]
Harvard TLB. Indicates the supported TLB maintenance operations, for a Harvard TLB implementation:

0x0 Not supported.

LL1HvdRng, [11:8]
L1 Harvard cache Range. Indicates the supported L1 cache maintenance range operations, for a Harvard cache implementation:

0x0 Not supported.

L1HvdBG, [7:4]
L1 Harvard cache Background fetch. Indicates the supported L1 cache background prefetch operations, for a Harvard cache implementation:

0x0 Not supported.

L1HvdFG, [3:0]
L1 Harvard cache Foreground fetch. Indicates the supported L1 cache foreground prefetch operations, for a Harvard cache implementation:

0x0 Not supported.

To access the ID_MMFR2:

\[ \text{MRC p15,0,<Rt>,c0,c1,6 ; Read ID_MMFR2 into Rt} \]

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>110</td>
</tr>
</tbody>
</table>

Table B1-65 ID_MMFR2 access encoding
### B1.83 Memory Model Feature Register 3

The ID_MMFR3 characteristics are:

**Purpose**

Provides information about the memory model and memory management support in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_MMFR0, ID_MMFR1, and ID_MMFR2. See:

- B1.80 Memory Model Feature Register 0 on page B1-275
- B1.81 Memory Model Feature Register 1 on page B1-277
- B1.82 Memory Model Feature Register 2 on page B1-279

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

ID_MMFR3 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supersec</td>
<td>CMemSz</td>
<td>CohWalk</td>
<td>Reserved</td>
<td>MaintBcst</td>
<td>BPMaint</td>
<td>CMaintSW</td>
<td>CMaintVA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure B1-38 ID_MMFR3 bit assignments**

**Supersec, [31:28]**

Supersections. Indicates support for supersections:

0x0 Supersections supported.

**CMemSz, [27:24]**

Cached Memory Size. Indicates the size of physical memory supported by the processor caches:

0x2 1TByte, corresponding to a 40-bit physical address range.

**CohWalk, [23:20]**

Coherent walk. Indicates whether translation table updates require a clean to the point of unification:

0x1 Updates to the translation tables do not require a clean to the point of unification to ensure visibility by subsequent translation table walks.

**[19:16]**

Reserved, RES0.

**MaintBcst, [15:12]**

Maintenance broadcast. Indicates whether cache, TLB and branch predictor operations are broadcast:
Cache, TLB and branch predictor operations affect structures according to shareability and defined behavior of instructions.

**BPMaint, [11:8]**

Branch predictor maintenance. Indicates the supported branch predictor maintenance operations.

- **0x2** Supported branch predictor maintenance operations are:
  - Invalidate all branch predictors.
  - Invalidate branch predictors by MVA.

**CMaintSW, [7:4]**

Cache maintenance by set/way. Indicates the supported cache maintenance operations by set/way.

- **0x1** Supported hierarchical cache maintenance operations by set/way are:
  - Invalidate data cache by set/way.
  - Clean data cache by set/way.
  - Clean and invalidate data cache by set/way.

**CMaintVA, [3:0]**

Cache maintenance by MVA. Indicates the supported cache maintenance operations by MVA.

- **0x1** Supported hierarchical cache maintenance operations by MVA are:
  - Invalidate data cache by MVA.
    - Invalidate data cache by MVA operations are treated as clean and invalidate data cache by MVA operations on the executing core. If the operation is broadcast to another core then it is broadcast as an invalidate data cache by MVA operation.
  - Clean data cache by MVA.
  - Clean and invalidate data cache by MVA.
  - Invalidate instruction cache by MVA.
  - Invalidate all instruction cache entries.

To access the ID_MMFR3:

```
MRC p15, 0, <Rt>, c0, c1, 7; Read ID_MMFR3 into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>111</td>
</tr>
</tbody>
</table>

Table B1-66  ID_MMFR3 access encoding
B1.84 Processor Feature Register 0

The ID_PFR0 characteristics are:

**Purpose**
Gives top-level information about the instruction sets supported by the processor in AArch32.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Level</th>
<th>Access</th>
<th>Access</th>
<th>Access</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0</td>
<td>(NS)</td>
<td>(S)</td>
<td>EL0</td>
<td>(NS)</td>
</tr>
<tr>
<td>EL1</td>
<td>(NS)</td>
<td>(S)</td>
<td>EL1</td>
<td>(S)</td>
</tr>
<tr>
<td>EL2</td>
<td>(SCR.NS = 1)</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL3</td>
<td>(SCR.NS = 0)</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

ID_PFR0 must be interpreted with ID_PFR1.

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_PFR0 is a 32-bit register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:16]</td>
<td>Reserved, RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[15:12]</td>
<td>State3</td>
<td>Indicates support for Thumb Execution Environment (T32EE) instruction set. This value is:</td>
<td>0x0, Processor does not support the T32EE instruction set.</td>
</tr>
<tr>
<td>[11:8]</td>
<td>State2</td>
<td>Indicates support for Jazelle. This value is:</td>
<td>0x1, Processor supports trivial implementation of Jazelle.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>State1</td>
<td>Indicates support for T32 instruction set. This value is:</td>
<td>0x3, Processor supports T32 encoding after the introduction of Thumb-2 technology, and for all 16-bit and 32-bit T32 basic instructions.</td>
</tr>
<tr>
<td>[3:0]</td>
<td>State0</td>
<td>Indicates support for A32 instruction set. This value is:</td>
<td>0x1, A32 instruction set implemented.</td>
</tr>
</tbody>
</table>

To access the ID_PFR0:
```
MRC p15,0,<Rt>,c0,c1,0 ; Read ID_PFR0 into Rt
```

Register access is encoded as follows:
Table B1-67  ID_PFR0 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.85 Processor Feature Register 1

The ID_PFR1 characteristics are:

**Purpose**
Provides information about the programmers model and architecture extensions supported by the processor.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Must be interpreted with ID_PFR0.

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
ID_PFR1 is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU</td>
<td>Reserved</td>
<td>GenTimer</td>
<td>MProgMod</td>
<td>Security</td>
<td>ProgMod</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Virtualization**
[31:28]
GIC CPU support:
- 0x0: GIC CPU interface is disabled, GICCDISABLE is HIGH, or not implemented.
- 0x1: GIC CPU interface is implemented and enabled, GICCDISABLE is LOW.

[27:20] Reserved, RAZ.

**GenTimer**, [19:16]
Generic Timer support:
- 0x1: Generic Timer implemented.

**Virtualization**, [15:12]
Indicates support for Virtualization:
- 0x1: Virtualization implemented.

**MProgMod**, [11:8]
M profile programmers model support:
- 0x0: Not supported.

**Security**, [7:4]
Security support:
0x1 Security implemented. This includes support for Monitor mode and the SMC
instruction.

**ProgMod, [3:0]**

Indicates support for the standard programmers model for Armv4 and later.

Model must support User, FIQ, IRQ, Supervisor, Abort, Undefined and System modes:

0x1 Supported.

To access the ID_PFR1:

```
MRC p15,0,<Rt>,c0,c1,1 ; Read ID_PFR1 into Rt
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0001</td>
<td>001</td>
</tr>
</tbody>
</table>

**Table B1-68 ID_PFR1 access encoding**
B1.86 Instruction Fault Address Register

The IFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Prefetch Abort exception.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>IFAR(S)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
</tr>
<tr>
<td>IFAR(NS)</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

IFAR (S) is architecturally mapped to HIFAR. See *B1.65 Hyp Instruction Fault Address Register* on page B1-246.

**Attributes**

IFAR is a 32-bit register.

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VA of faulting address of synchronous Prefetch Abort exception |
```

**Figure B1-41 IFAR bit assignments**

**VA, [31:0]**

The Virtual Address of faulting address of synchronous Prefetch Abort exception.

To access the IFAR:

```
MRC p15, 0, <Rt>, c6, c0, 2; Read IFAR into Rt
MCR p15, 0, <Rt>, c6, c0, 2; Write Rt to IFAR
```
### B1.87 Instruction Fault Status Register

The IFSR characteristics are:

**Purpose**

Holds status information about the last instruction fault.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

**Attributes**

IFSR is a 32-bit register.

There are two formats for this register. The current translation table format determines which format of the register is used.
### B1.88 IFSR with Short-descriptor translation table format

IFSR has a specific format when using the Short-descriptor translation table format.

The following figure shows the IFSR bit assignments when using the Short-descriptor translation table format.

![IFSР bit assignments for Short-descriptor translation table format](image)

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:13]</td>
<td>Reserved, <code>RES0</code></td>
</tr>
<tr>
<td><code>ExT</code>,[12]</td>
<td>External abort type. This field indicates whether an AXI Decode or Slave error caused an abort:</td>
</tr>
<tr>
<td>0</td>
<td>Externally marked as <code>DECERR</code></td>
</tr>
<tr>
<td>1</td>
<td>Externally marked as <code>SLVERR</code></td>
</tr>
<tr>
<td>[11]</td>
<td>Reserved, <code>RES0</code></td>
</tr>
<tr>
<td>[9]</td>
<td><code>RAZ</code></td>
</tr>
<tr>
<td>[8:5]</td>
<td>Reserved, <code>RES0</code></td>
</tr>
<tr>
<td><code>FS[3:0]</code>,[4:0]</td>
<td>Fault Status bits. This field indicates the type of exception generated. Any encoding not listed is reserved.</td>
</tr>
<tr>
<td>0b00010</td>
<td>Debug event.</td>
</tr>
<tr>
<td>0b00011</td>
<td>Access flag fault, section.</td>
</tr>
<tr>
<td>0b00101</td>
<td>Translation fault, section.</td>
</tr>
<tr>
<td>0b00110</td>
<td>Access flag fault, page.</td>
</tr>
<tr>
<td>0b00111</td>
<td>Translation fault, page.</td>
</tr>
<tr>
<td>0b01000</td>
<td>Synchronous external abort, non-translation.</td>
</tr>
<tr>
<td>0b01001</td>
<td>Domain fault, section.</td>
</tr>
<tr>
<td>0b01011</td>
<td>Domain fault, page.</td>
</tr>
<tr>
<td>0b01100</td>
<td>Synchronous external abort on translation table walk, first level.</td>
</tr>
<tr>
<td>0b01101</td>
<td>Permission Fault, Section.</td>
</tr>
<tr>
<td>0b01110</td>
<td>Synchronous external abort on translation table walk, second Level.</td>
</tr>
<tr>
<td>0b01111</td>
<td>Permission fault, page.</td>
</tr>
<tr>
<td>0b10000</td>
<td>TLB conflict abort.</td>
</tr>
<tr>
<td>0b11001</td>
<td>Synchronous parity error on memory access.</td>
</tr>
</tbody>
</table>
0b1110  Synchronous parity error on translation table walk, first level.
0b1111  Synchronous parity error on translation table walk, second level.
**B1.89 IFSR with Long-descriptor translation table format**

IFSR has a specific format when using the Long-descriptor translation table format.

The following figure shows the IFSR bit assignments when using the Long-descriptor translation table format.

![IFSR bit assignments for Long-descriptor translation table format](image)

**Figure B1-43 IFSR bit assignments for Long-descriptor translation table format**

- **[31:13]** Reserved, RES0.
- **ExT,[12]**
  - External abort type. This field indicates whether an AXI Decode or Slave error caused an abort:
    - 0: External abort marked as DECERR.
    - 1: External abort marked as SLVERR.
  - For aborts other than external aborts this bit always returns 0.
- **[11:10]** Reserved, RES0.
- **[9]**
  - RAO.
- **[8:6]**
  - Reserved, RES0.
- **Status,[5:0]**
  - Fault Status bits. This field indicates the type of exception generated. Any encoding not listed is reserved.
    - `0b000000` Address size fault in TTBR0 or TTBR1.
    - `0b0001LL` Translation fault, LL bits indicate level.
    - `0b0010LL` Access fault flag, LL bits indicate level.
    - `0b0011LL` Permission fault, LL bits indicate level.
    - `0b010000` Synchronous external abort.
    - `0b0101LL` Synchronous external abort on translation table walk, LL bits indicate level.
    - `0b011000` Synchronous parity error on memory access.
    - `0b0111LL` Synchronous parity error on memory access on translation table walk, LL bits indicate level.
    - `0b100001` Alignment fault.
    - `0b100010` Debug event.
    - `0b110000` TLB conflict abort.
Table B1-69  Encodings of LL bits associated with the MMU fault

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved</td>
</tr>
<tr>
<td>0b01</td>
<td>Level 1</td>
</tr>
<tr>
<td>0b10</td>
<td>Level 2</td>
</tr>
<tr>
<td>0b11</td>
<td>Level 3</td>
</tr>
</tbody>
</table>

If a Data Abort exception is generated by an instruction cache maintenance operation when the Long-descriptor translation table format is selected, the fault is reported as a Cache Maintenance fault in the DFSR or HSR with the appropriate Fault Status code. For such exceptions reported in the DFSR, the corresponding IFSR is **UNKNOWN**.

To access the IFSR:

```
MRC p15, 0, <Rt>, c5, c0, 1; Read IFSR into Rt
MCR p15, 0, <Rt>, c5, c0, 1; Write Rt to IFSR
```

Register access is encoded as follows:

Table B1-70  IFSR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0101</td>
<td>0000</td>
<td>001</td>
</tr>
</tbody>
</table>
B1.90 Interrupt Status Register

The ISR characteristics are:

**Purpose**
Shows whether an IRQ, FIQ, or external abort is pending. An indicated pending abort might be a physical abort or a virtual abort.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td></td>
</tr>
</tbody>
</table>

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
 ISR is a 32-bit register.

<table>
<thead>
<tr>
<th>31</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>A</td>
<td>I</td>
<td>F</td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure B1-44 ISR bit assignments

[31:9]
Reserved, RES0.

A, [8]
External abort pending bit:
0 No pending external abort.
1 An external abort is pending.

I, [7]
IRQ pending bit. Indicates whether an IRQ interrupt is pending:
0 No pending IRQ.
1 An IRQ interrupt is pending.

F, [6]
FIQ pending bit. Indicates whether an FIQ interrupt is pending:
0 No pending FIQ.
1 An FIQ interrupt is pending.

[5:0]
Reserved, RES0.

To access the ISR:

\[\text{MRC p15, 0, } \langle \text{Rt} \rangle, \text{ c12, c1, 1}; \ \text{Read ISR into } \text{Rt}\]

Register access is encoded as follows:
### Table B1-71 ISR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1100</td>
<td>0001</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.91 L2 Auxiliary Control Register

The L2ACTLR characteristics are:

**Purpose**

Provides configuration and control options for the L2 memory system.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

You can write to this register only when the L2 memory system is idle. Arm recommends that you write to this register after a powerup reset before the MMU is enabled and before any AXI, ACE, CHI, or ACP traffic has begun.

If the register must be modified after a powerup reset sequence, to idle the L2 memory system, you must take the following steps:

1. Disable the MMU from each core followed by an ISB to ensure the MMU disable operation is complete, then followed by a DSB to drain previous memory transactions.
2. Ensure that the system has no outstanding AC channel coherence requests to the Cortex-A32 processor.
3. Ensure that the system has no outstanding ACP requests to the Cortex-A32 processor.

When the L2 is idle, the processor can update the L2ACTLR followed by an ISB. After the L2ACTLR is updated, the MMUs can be enabled and normal ACE and ACP traffic can resume.

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

L2ACTLR is a 32-bit register.

Figure B1-45 L2ACTLR bit assignments

<table>
<thead>
<tr>
<th>[31:30]</th>
<th>25 24</th>
<th>15 14 13</th>
<th>4 3 2 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>RES0</td>
<td>RES0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

L2 Victim Control

L2DEIEN, [29]

L2 cache data RAM error injection enable. The possible values are:

0 Normal behavior, errors are not injected. This is the reset value.
1 Double-bit errors are injected on all writes to the L2 cache data RAMs.

<table>
<thead>
<tr>
<th>0b10</th>
<th>This is the default value. Software must not change it.</th>
<th>L2DEIEN</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>L2 Victim Control</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Enable UniqueClean evictions with data</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Disable clean/evict push to external</td>
<td></td>
</tr>
</tbody>
</table>

Non-Confidential
[28:25]
  Reserved, RES0.

L2TEIEN, [24]
  L2 cache tag RAM error injection enable. The possible values are:
  0 Normal behavior, errors are not injected. This is the reset value.
  1 Double-bit errors are injected on all writes to the L2 cache tag RAMs.

[23:15]
  Reserved, RES0.

Enable UniqueClean evictions with data, [14]
  Enables UniqueClean evictions with data. The possible values are:
  0 Disables UniqueClean evictions with data. This is the reset value for ACE.
  1 Enables UniqueClean evictions with data. This is the reset value for CHI.

In AXI implementations, this field is RES0.

[13:4]
  Reserved, RES0.

Disable clean/evict push to external, [3]
  Disables clean/evict push to external. The possible values are:
  0 Enables clean/evict to be pushed out to external. This is the reset value for ACE.
  1 Disables clean/evict from being pushed to external. This is the reset value for CHI.

In AXI implementations, this field is RES1.

[2:0]
  Reserved, RES0.

To access the L2ACTLR:

MRC p15, 1, <Rt>, c15, c0, 0; Read L2ACTLR into Rt
MCR p15, 1, <Rt>, c15, c0, 0; Write Rt to L2ACTLR

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>1111</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>

Table B1-72  L2ACTLR access encoding
B1.92 L2 Control Register

The L2CTLR characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED control options for the L2 memory system.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

L2CTLR is writable. However, all writes to this register are ignored.

**Configurations**

There is one L2CTLR for the Cortex-A32 processor.

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

L2CTLR is a 32-bit register.

![Figure B1-46 L2CTLR bit assignments](image)

[31:26]

Reserved, RES0.

**Number of cores, [25:24]**

Number of cores present:

- **0b00** One core, core 0.
- **0b01** Two cores, core 0 and core 1.
- **0b10** Three cores, cores 0 to 2.
- **0b11** Four cores, cores 0 to 3.

These bits are read-only and the value of this field is set to the number of cores present in the configuration.

[23]

Reserved, RAZ.

**CPU Cache Protection, [22]**

CPU Cache Protection. Core RAMs are implemented:

- **0** Without ECC.
- **1** With ECC.

This field is RO.
SCU-L2 Cache Protection, [21]

SCU-L2 Cache Protection. L2 cache is implemented:

0    Without ECC.
1    With ECC.

This field is RO.

[20:6]

Reserved, RAZ.

L2 Data RAM input latency, [5]

L2 data RAM input latency

0    1-cycle input delay from L2 data RAMs.
1    2-cycle input delay from L2 data RAMs.

This field is RO.

[4:1]

Reserved, RAZ.

L2 Data RAM output latency, [0]

L2 data RAM output latency:

0    2-cycle output delay from L2 data RAMs.
1    3-cycle output delay from L2 data RAMs.

This field is RO.

To access the L2CTLR:

\[ \text{MRC p15, 1, } <\text{Rt}>, c9, c0, 2; \text{ Read L2CTLR into Rt} \]

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>1001</td>
<td>0000</td>
<td>010</td>
</tr>
</tbody>
</table>

Table B1-73  L2CTLR access encoding
B1.93 L2 Extended Control Register

The L2ECTLR characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED control options for the L2 memory system. This register is used for dynamically changing, but implementation specific, control bits.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td></td>
</tr>
</tbody>
</table>

The L2ECTLR can be written dynamically.

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

There is one L2ECTLR for the Cortex-A32 processor.

**Attributes**

L2ECTLR is a 32-bit register.

![Figure B1-47 L2ECTLR bit assignments](image)

[31] Reserved, RES0.

**L2 internal asynchronous error, [30]**

L2 internal asynchronous error caused by L2 RAM double-bit ECC error. The possible values are:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No pending asynchronous error. This is the reset value.</td>
</tr>
<tr>
<td>1</td>
<td>An asynchronous error has occurred.</td>
</tr>
</tbody>
</table>

A write of 0 clears this bit. A write of 1 is ignored.

**AXI, ACE, or CHI asynchronous error, [29]**

AXI, ACE, or CHI asynchronous error indication. The possible values are:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No pending asynchronous error.</td>
</tr>
<tr>
<td>1</td>
<td>An asynchronous error has occurred.</td>
</tr>
</tbody>
</table>

A write of 0 clears this bit. A write of 1 is ignored.
[28:3]

Reserved, \texttt{RES0}.

**L2 dynamic retention control, [2:0]**

L2 dynamic retention control. The possible values are:

- \texttt{0b00} L2 dynamic retention disabled. This is the reset value.
- \texttt{0b01} 2 Generic Timer ticks required before retention entry.
- \texttt{0b10} 8 Generic Timer ticks required before retention entry.
- \texttt{0b11} 32 Generic Timer ticks required before retention entry.
- \texttt{0b100} 64 Generic Timer ticks required before retention entry.
- \texttt{0b101} 128 Generic Timer ticks required before retention entry.
- \texttt{0b110} 256 Generic Timer ticks required before retention entry.
- \texttt{0b111} 512 Generic Timer ticks required before retention entry.

To access the L2ECTLR:

\begin{verbatim}
MRC p15, 1, <Rt>, c9, c0, 3; Read L2ECTLR into Rt
MCR p15, 1, <Rt>, c9, c0, 3; Write Rt to L2ECTLR
\end{verbatim}

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>001</td>
<td>1001</td>
<td>0000</td>
<td>011</td>
</tr>
</tbody>
</table>

\textbf{Table B1-74 L2ECTLR access encoding}
B1.94 L2 Memory Error Syndrome Register

The L2MERRSR characteristics are:

**Purpose**

Holds ECC errors on the:
- L2 data RAMs.
- L2 tag RAMs.
- SCU snoop filter RAMs.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td></td>
</tr>
</tbody>
</table>

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

A write of any value to the register updates the register to 0x0000000000000000.

**Attributes**

L2MERRSR is a a 64-bit register.

**Fatal, [63]**

Fatal bit. This bit is set to 1 on the first memory error that caused a data abort. It is a sticky bit so that after it is set, it remains set until the register is written. The reset value is 0.

**[62:48]**

Reserved, RES0.

**Other error count, [47:40]**

This field is set to 0 on the first memory error and is incremented on any memory error that does not match the RAMID and Bank/Way information in this register while the sticky Valid bit is set.

The reset value is 0.

**Repeat error count, [39:32]**

This field is set to 0 on the first memory error and is incremented on any memory error that exactly matches the RAMID and Bank/Way information in this register while the sticky Valid bit is set.

The reset value is 0.
Valid, [31]

Valid bit. This bit is set to 1 on the first memory error. It is a sticky bit so that after it is set, it remains set until the register is written.

The reset value is 0.

RAMID, [30:24]

RAM Identifier. Indicates the RAM in which the first memory error occurred. The possible values are:

- 0x10 L2 tag RAM.
- 0x11 L2 data RAM.
- 0x12 SCU snoop filter RAM.

[23:22]

Reserved, RES0.

CPUID/Way, [21:18]

Indicates the RAM where the first memory error occurred.

**L2 tag RAM**

- 0x0 Way 0
- 0x1 Way 1
- ...
- 0x6 Way 6
- 0x7 Way 7

**L2 data RAM**

- 0x0 Bank 0
- 0x1 Bank 1
- ...
- 0x6 Bank 7
- 0x8-0x Unused
- F

**SCU snoop filter RAM**

- 0x0 CPU0:Way0
- 0x1 CPU0:Way1
- ...
- 0xE CPU3:Way2
- 0xF CPU3:Way3

[17]

Reserved, RES0.

**RAM Address, [16:3]**

Indicates the index address of the first memory error.

[2:0]

Reserved, RES0.

- A fatal error results in the RAMID, CPU ID/Way and RAM address recording the fatal error, even if the sticky bit was set.
- If two or more memory errors in the same RAM occur in the same cycle, only one error is reported.
• If two or more first memory error events from different RAMs occur in the same cycle, one of the errors is selected arbitrarily, while the Other error count field is incremented only by one.
• If two or more memory error events from different RAMs, that do not match the RAMID, bank, way, or index information in this register while the sticky Valid bit is set, occur in the same cycle, the Other error count field is incremented only by one.

To access the L2MERRSR:

```
MRRC p15, 3, <Rt>, <Rt2>, c15;  Read L2MERRSR into Rt and Rt2
MCRR p15, 3, <Rt>, <Rt2>, c15;  Write Rt and Rt2 to L2MERRSR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>0011</td>
<td>1111</td>
</tr>
</tbody>
</table>
B1.95 Memory Attribute Indirection Registers 0 and 1

The MAIR0 and MAIR1 characteristics are:

**Purpose**

To provide the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations.

**Usage constraints**

These registers are accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Accessible only when using the Long-descriptor translation table format. When using the Short-descriptor format see, instead, B1.101 Primary Region Remap Register on page B1-316 and B1.99 Normal Memory Remap Register on page B1-313.

AttrIndx[2], from the translation table descriptor, selects the appropriate MAIR. Setting AttrIndx[2] to 0 selects MAIR0 and setting AttrIndx[2] to 1 selects MAIR1.

The Secure instance of the register gives the value for memory accesses from Secure state.

The Non-secure instance of the register gives the value for memory accesses from Non-secure states other than Hyp mode.

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

Write access to MAIR0(S) and MAIR1(S) is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**

MAIR0 is a 32-bit register when TTBCR.EAE==1.

<table>
<thead>
<tr>
<th>MAIR0</th>
<th>31</th>
<th>24</th>
<th>23</th>
<th>16</th>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Attr3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>MAIR1</th>
<th>31</th>
<th>24</th>
<th>23</th>
<th>16</th>
<th>15</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Attr7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr6</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Attr4</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Attrm., [7:0]**

Where m is 0-7.

The memory attribute encoding for an AttrIndx[2:0] entry in a Long descriptor format translation table entry, where:

- AttrIndx[2] selects the appropriate MAIR:
  - Setting AttrIndx[2] to 0 selects MAIR0.
- AttrIndx[2:0] gives the value of <n> in Attr<n>.
Table B1-76  Attr<n>[7:4] bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device memory. See Attr&lt;n&gt;[3:0] bit assignments on page B1-305 for the type of Device memory.</td>
</tr>
<tr>
<td>0b00RW, RW not 00</td>
<td>Normal Memory, Outer Write-through transient. The transient hint is ignored.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal Memory, Outer Non-Cacheable.</td>
</tr>
<tr>
<td>0b01RW, RW not 00</td>
<td>Normal Memory, Outer Write-back transient. The transient hint is ignored.</td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal Memory, Outer Write-through non-transient.</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal Memory, Outer Write-back non-transient.</td>
</tr>
</tbody>
</table>

The following table shows the Attr<n>[3:0] bit assignments. The encoding of Attr<n>[3:0] depends on the value of Attr<n>[7:4].

Table B1-77  Attr<n>[3:0] bit assignments

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning when Attr&lt;n&gt;[7:4] is 0000</th>
<th>Meaning when Attr&lt;n&gt;[7:4] is not 0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory</td>
<td>UNPREDICTABLE</td>
</tr>
<tr>
<td>0b00RW, RW not 00</td>
<td>UNPREDICTABLE</td>
<td>Normal Memory, Inner Write-through transient</td>
</tr>
<tr>
<td>0b0100</td>
<td>Device-nGnRE memory</td>
<td>Normal memory, Inner Non-Cacheable</td>
</tr>
<tr>
<td>0b01RW, RW not 00</td>
<td>UNPREDICTABLE</td>
<td>Normal Memory, Inner Write-back transient</td>
</tr>
<tr>
<td>0b1000</td>
<td>Device-nGRE memory</td>
<td>Normal Memory, Inner Write-through non-transient (RW=00)</td>
</tr>
<tr>
<td>0b10RW, RW not 00</td>
<td>UNPREDICTABLE</td>
<td>Normal Memory, Inner Write-through non-transient</td>
</tr>
<tr>
<td>0b1100</td>
<td>Device-GRE memory</td>
<td>Normal Memory, Inner Write-back non-transient (RW=00)</td>
</tr>
<tr>
<td>0b11RW, RW not 00</td>
<td>UNPREDICTABLE</td>
<td>Normal Memory, Inner Write-back non-transient</td>
</tr>
</tbody>
</table>

The following table shows the encoding of the R and W bits that are used, in some Attr<n> encodings in Table B1-76  Attr<n>[7:4] bit assignments on page B1-305 and Table B1-77  Attr<n>[3:0] bit assignments on page B1-305, to define the read-allocate and write-allocate policies:

Table B1-78  Encoding of R and W bits in some Attrm fields

<table>
<thead>
<tr>
<th>R or W</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Do not allocate</td>
</tr>
<tr>
<td>1</td>
<td>Allocate</td>
</tr>
</tbody>
</table>

To access the MAIR0:

```
MRC p15, 0, <Rt>, c10, c2, 0 ; Read MAIR0 into Rt
MCR p15, 0, <Rt>, c10, c2, 0 ; Write Rt to MAIR0
```

Register access is encoded as follows:
Table B1-79  MAIR0 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1010</td>
<td>0010</td>
<td>000</td>
</tr>
</tbody>
</table>

To access the MAIR1:

```
MRC p15, 0, <Rt>, c10, c2, 1    ; Read MAIR1 into Rt
MCR p15, 0, <Rt>, c10, c2, 1    ; Write Rt to MAIR1
```

Register access is encoded as follows:

Table B1-80  MAIR1 access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1010</td>
<td>0010</td>
<td>001</td>
</tr>
</tbody>
</table>
B1.96 Main ID Register

The MIDR characteristics are:

Purpose

Provides identification information for the processor, including an implementer code for the device and a device ID number.

Usage constraints

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Level</th>
<th>Access</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0 (NS)</td>
<td>-</td>
<td>RO</td>
</tr>
<tr>
<td>EL0 (NS)</td>
<td>-</td>
<td>RO</td>
</tr>
<tr>
<td>EL1 (S)</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL1 (S)</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL2 (SCR.NS = 1)</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td>EL3 (SCR.NS = 0)</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Configurations

MIDR is architecturally mapped to the external register MIDR_EL1.

Attributes

MIDR is a 32-bit register.

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>Implementer</td>
</tr>
<tr>
<td>23:20</td>
<td>Variant</td>
</tr>
<tr>
<td>19:16</td>
<td>Architecture</td>
</tr>
<tr>
<td>15:4</td>
<td>PartNum</td>
</tr>
<tr>
<td>3:0</td>
<td>Revision</td>
</tr>
</tbody>
</table>

![Figure B1-50 MIDR bit assignments](image)

Implementer, [31:24]

Indicates the implementer code. This value is:

\( \text{0x41} \) ARM.

Variant, [23:20]

Indicates the variant number of the processor. This is the major revision number \( n \) in the \( r_n \) part of the \( rnpn \) description of the product revision status. This value is:

\( \text{0x1} \) r1p0.

Architecture, [19:16]

Indicates the architecture code. This value is:

\( \text{0xF} \) Defined in the CPuid scheme.

PartNum, [15:4]

Indicates the primary part number. This value is:

\( \text{0xD01} \) Cortex-A32 processor.

Revision, [3:0]

Indicates the minor revision number of the processor. This is the minor revision number \( n \) in the \( p_n \) part of the \( rnpn \) description of the product revision status. This value is:

\( \text{0x0} \) r1p0.

To access the MIDR:

\[ \text{MRC p15, 0, <Rt>, c0, c0, 0; Read MIDR into Rt} \]
Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>111</td>
<td>000</td>
<td>0000</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>

The MIDR can be accessed through the external debug interface, offset 0xD00.
B1.97 Multiprocessor Affinity Register

The MPIDR characteristics are:

**Purpose**

Provides an additional core identification mechanism for scheduling purposes in a cluster. EDDEVAFF0 is a read-only copy of MPIDR accessible from the external debug interface.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Configurations**

The MPIDR is mapped to external EDDEVAFF0 register. There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

MPIDR is a 32-bit register.

<table>
<thead>
<tr>
<th>31 30 29</th>
<th>25 24</th>
<th>16 15</th>
<th>8 7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>M U</td>
<td>RES0</td>
<td>Aff2</td>
<td>Aff1</td>
<td>Aff0</td>
</tr>
<tr>
<td>MT</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure B1-51 MPIDR bit assignments**

- **M, [31]**
  - Reserved, RES1.

- **U, [30]**
  - Indicates a uniprocessor system, as distinct from core 0 in a multiprocessor system. This value is one of:
    - 0 — Processor is part of a multiprocessor system. This is the value for implementations with more than one core, and for implementations with an ACE or CHI interface.
    - 1 — Processor is part of a uniprocessor system. This is the value for single core implementations with an AXI master interface.

- **[29:25]**
  - Reserved, RES0.

- **MT, [24]**
  - Indicates whether the lowest level of affinity consists of logical cores that are implemented using a multi-threading type approach. This value is:
    - 0 — Performance of cores at the lowest affinity level is largely independent.

- **Aff2, [23:16]**
  - Affinity level 2. Second highest level affinity field.
  - Indicates the value read in the CLUSTERIDAFF2 configuration signal.
Aff1, [15:8]
Affinity level 1. Third highest level affinity field.
Indicates the value read in the CLUSTERIDAFF1 configuration signal.

Aff0, [7:0]
Affinity level 0. Lowest level affinity field.
Indicates the core number in the Cortex-A32 processor. The possible values are:

- 0x0: A processor with one core only.
- 0x0, 0x1: A cluster with two cores.
- 0x0, 0x1, 0x2: A cluster with three cores.
- 0x0, 0x1, 0x2, 0x3: A cluster with four cores.

To access the MPIDR:

```
MRC p15,0,<Rt>,c0,c0,5 ; Read MPIDR into Rt
```

Register access is encoded as follows:

**Table B1-82 MPIDR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0000</td>
<td>101</td>
</tr>
</tbody>
</table>

The EDDEVAFF0 can be accessed through the external debug interface, offset 0xFA8.
B1.98  Non-Secure Access Control Register

The NSACR characteristics are:

**Purpose**
Defines the Non-secure access permission to CP0 to CP13.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RW</td>
<td>RW</td>
<td></td>
</tr>
</tbody>
</table>

Any read or write to NSACR in Secure EL1 state in AArch32 is trapped as an exception to EL3.

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states. Write access to NSACR is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**
NSACR is a 32-bit register.

![Figure B1-52 NSACR bit assignments](image)

**[31:16]**
Reserved, RES0.

**NSASEDIS, [15]**
Disable Non-secure Advanced SIMD functionality:

0 This bit has no effect on the ability to write CPACR.ASEDIS, this is the reset value.
1 When executing in Non-secure state, the CPACR.ASEDIS bit has a fixed value of 1 and writes to it are ignored.

If Advanced SIMD and floating-point are not implemented, this bit is RES0.

**[14:12]**
Reserved, RES0.

**cp11, [11]**
Non-secure access to CP11 enable:

0 Secure access only. Any attempt to access CP11 in Non-secure state results in an Undefined Instruction exception. If the processor is in Non-secure state, the corresponding bits in the CPACR ignore writes and read as 0b00, access denied. This is the reset value.
1 Secure or Non-secure access.

If Advanced SIMD and Floating-point are not implemented, this bit is RES0.
**cp10, [10]**

Non-secure access to CP10 enable:

- 0 Secure access only. Any attempt to access CP10 in Non-secure state results in an Undefined Instruction exception. If the processor is in Non-secure state, the corresponding bits in the CPACR ignore writes and read as 0b00, access denied. This is the reset value.
- 1 Secure or Non-secure access.

If Advanced SIMD and floating-point are not implemented, this bit is **res0**.

**[9:0]**

Reserved, **res0**.

If the CP11 and CP10 fields are set to different values, the behavior is CONSTRAINED UNPREDICTABLE. It is the same as if both fields were set to the value of CP10, in all respects other than the value read back by explicitly reading CP11.

To access the NSACR:

```
MRC p15, 0, <Rt>, c1, c1, 2 ; Read NSACR into Rt
MCR p15, 0, <Rt>, c1, c1, 2 ; Write Rt to NSACR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0001</td>
<td>0001</td>
<td>010</td>
</tr>
</tbody>
</table>

**Table B1-83 NSACR access encoding**
**B1.99 Normal Memory Remap Register**

The NMRR characteristics are:

**Purpose**
Provides additional mapping controls for memory regions that are mapped as Normal memory by their entry in the PRRR.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

The register is:
- Used in conjunction with the PRRR.
- Not accessible when using the Long-descriptor translation table format.

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.

Write access to NMRR(S) is disabled when the CP15SDisable2 signal is asserted HIGH.

**Attributes**
NMRR is a 32-bit register when TTBCR.EAE is 0.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| OR7 | OR6 | OR5 | OR4 | OR3 | OR2 | OR1 | OR0 | IR7 | IR6 | IR5 | IR4 | IR3 | IR2 | IR1 | IR0 |

**Figure B1-53 NMRR bit assignments**

**ORn, [2n+17:2n+16]**
Outer Cacheable property mapping for memory attributes n, where n is 0-7, if the region is mapped as Normal memory by the PRRR.TRn entry. n is the value of the TEX[0], C and B bits, see Memory attributes and the n value for the PRRR field descriptions on page B1-317. The possible values of this field are:
- 0b00 Region is Non-cacheable.
- 0b01 Region is Write-Back, Write-Allocate.
- 0b10 Region is Write-Through, no Write-Allocate.
- 0b11 Region is Write-Back, no Write-Allocate.

**IRn, [2n+1:2n]**
Inner Cacheable property mapping for memory attributes n, where n is 0-7, if the region is mapped as Normal Memory by the PRRR.TRn entry. n is the value of the TEX[0], C and B bits, see Memory attributes and the n value for the PRRR field descriptions on page B1-317. The possible values of this field are the same as those given for the ORn field.

To access the NMRR:

```
MRC p15, 0, <Rt>, c10, c2, 1 ; Read NMRR into Rt
MCR p15, 0, <Rt>, c10, c2, 1 ; Write Rt to NMRR
```

Register access is encoded as follows:
Table B1-84  NMRR access encoding

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1010</td>
<td>0010</td>
<td>001</td>
</tr>
</tbody>
</table>
B1.100 Physical Address Register

PAR

The processor does not use any implementation-defined bits in the 32-bit format or 64-bit format PAR. Bit[8] is RES0. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.
The PRRR characteristics are:

**Purpose**
Controls the top level mapping of the TEX[0], C, and B memory region attributes.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

PRRR is not accessible when the Long-descriptor translation table format is in use. See, instead, *B1.95 Memory Attribute Indirection Registers 0 and 1* on page B1-304.

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.

Write access to PRRR(S) is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**
PRRR is a 32-bit register when TTBCR.EAE==0.

![PRRR bit assignments](image)

**NOSn, [24+n]**
Outer Shareable property mapping for memory attributes $n$, where $n$ is 0-7, if the region is mapped as Normal Shareable. $n$ is the value of the TEX[0], C and B bits concatenated. The possible values of each NOS$n$ bit are:

- $0$ Memory region is Outer Shareable.
- $1$ Memory region is Inner Shareable.

The value of this bit is ignored if the region is Normal or Device memory that is not Shareable.

**[23:20]**
Reserved, RES0.

**NS1, [19]**
Mapping of $S = 1$ attribute for Normal memory. This bit gives the mapped Shareable attribute for a region of memory that:

- Is mapped as Normal memory.
- Has the $S$ bit set to 1.

The possible values of the bit are:

- $0$ Region is not Shareable.
Region is Shareable.

NS0, [18]
Mapping of S = 0 attribute for Normal memory. This bit gives the mapped Shareable attribute for a region of memory that:
- Is mapped as Normal memory.
- Has the S bit set to 0.

The possible values of the bit are the same as those given for the NS1 bit, bit[19].

DS1, [17]
Mapping of S = 1 attribute for Device memory. This bit gives the mapped Shareable attribute for a region of memory that:
- Is mapped as Device memory.
- Has the S bit set to 1.

This field has no significance in the processor.

DS0, [16]
Mapping of S = 0 attribute for Device memory. This bit gives the mapped Shareable attribute for a region of memory that:
- Is mapped as Device memory.
- Has the S bit set to 0.

This field has no significance in the processor.

TRn, [2n+1:2n]
Primary TEX mapping for memory attributes n, where n is 0-7. n is the value of the TEX[0], C and B bits, see Memory attributes and the n value for the PRRR field descriptions on page B1-317. This field defines the mapped memory type for a region with attributes n. The possible values of the field are:
- \(0b00\) Device (nGnRnE).
- \(0b01\) Device (not nGnRnE).
- \(0b10\) Normal Memory.
- \(0b11\) Reserved, effect is UNPREDICTABLE.

The following table shows the mapping between the memory region attributes and the n value used in the PRRR.nOSn and PRRR.TRn field descriptions.

<table>
<thead>
<tr>
<th>Attributes</th>
<th>n value</th>
</tr>
</thead>
<tbody>
<tr>
<td>TEX[0]</td>
<td>C</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Large physical address translations use Long-descriptor translation table formats and MAIR0 replaces the PRRR, and MAIR1 replaces the NMRR. For more information see B1.95 Memory Attribute Indirection Registers 0 and 1 on page B1-304.

To access the PRRR:

```
MRC p15, 0, <Rt>, c10, c2, 0    ; Read PRRR into Rt
MCR p15, 0, <Rt>, c10, c2, 0    ; Write Rt to PRRR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1010</td>
<td>0010</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.102 Revision ID Register

The REVIDR characteristics are:

**Purpose**
Provides implementation-specific minor revision information that can be interpreted only in conjunction with the Main ID Register.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
REVIDR is a 32-bit register.

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ID number |
```

**Figure B1-55 REVIDR bit assignments**

**ID number, [31:0]**
Implementation-specific revision information. The reset value is determined by the specific Cortex-A32 processor implementation.

```
0x00000000
```

Revision code is zero.

To access the REVIDR:
```
MRC p15, 0, <Rt>, c0, c0, 6; Read REVIDR into Rt
```

Register access is encoded as follows:

**Table B1-87 REVIDR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>000</td>
<td>000</td>
<td>110</td>
</tr>
</tbody>
</table>
B1.103 Reset Management Register

The RMR characteristics are:

**Purpose**
Controls the execution state that the processor boots into and allows request of a warm reset.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
RMR is a 32-bit register.

![RMR bit assignments](image)

**[31:2]**
Reserved, `RES0`.

**RR, [1]**
Reset Request. The possible values are:
0  This is the reset value.
1  Requests a warm reset. This bit is set to 0 by either a cold or warm reset.

The bit is strictly a request.
The RR bit drives the `WARMRSTREQ` output signal.

**AA64, [0]**
Reserved, `RES0`.

To access the RMR:

```
MRC p15,0,<Rt>,c12,c0,2 ; Read RMR into Rt
MCR p15,0,<Rt>,c12,c0,2 ; Write Rt to RMR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>1100</td>
<td>0000</td>
<td>010</td>
</tr>
</tbody>
</table>

Table B1-88 RMR access encoding
B1.104 Secure Configuration Register

The SCR characteristics are:

**Purpose**

Defines the configuration of the current security state. It specifies:
- The security state of the processor, Secure or Non-secure.
- What state the processor branches to, if an IRQ, FIQ or external abort occurs.
- Whether the CPSR.F and CPSR.A bits can be modified when SCR.NS = 1.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td></td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Any read or write to SCR in Secure EL1 state in AArch32 is trapped as an exception to EL3.

**Configurations**

The SCR is a Restricted access register that exists only in the Secure state.

**Attributes**

SCR is a 32-bit register.

![SCR bit assignments](image)

**Figure B1-57 SCR bit assignments**

[31:14]

Reserved, RES0.

TWE, [13]

Trap *wfe* instructions. The possible values are:

0 *wfe* instructions are not trapped. This is the reset value.

1 *wfe* instructions executed in any mode other than Monitor mode are trapped to Monitor mode as *undefined* if the instruction would otherwise cause suspension of execution, that is if:
- The event register is not set.
- There is not a pending WFE wakeup event.
- The instruction does not cause another exception.

TWI, [12]
Trap WFI instructions. The possible values are:

0  WFI instructions are not trapped. This is the reset value.
1  WFI instructions executed in any mode other than Monitor mode are trapped to Monitor mode as UNDEFINED if the instruction would otherwise cause suspension of execution.

[11:10]  
Reserved, RES0.

SIF, [9]  
Secure Instruction Fetch. When the processor is in Secure state, this bit disables instruction fetches from Non-secure memory. The possible values are:

0  Secure state instruction fetches from Non-secure memory permitted. This is the reset value.
1  Secure state instruction fetches from Non-secure memory not permitted.

HCE, [8]  
Hyp Call enable. This bit enables use of the HVC instruction from Non-secure EL1 modes. The possible values are:

0  The HVC instruction is UNDEFINED in any mode. This is the reset value.
1  The HVC instruction enabled in Non-secure EL1, and performs a Hyp Call.

SCD, [7]  
Secure Monitor Call disable. Makes the SMC instruction UNDEFINED in Non-secure state. The possible values are:

0  SMC executes normally in Non-secure state, performing a Secure Monitor Call. This is the reset value.
1  The SMC instruction is UNDEFINED in Non-secure state.

A trap of the SMC instruction to Hyp mode takes priority over the value of this bit.

nET, [6]  
Not Early Termination. This bit disables early termination.

This bit is not implemented, RES0.

AW, [5]  
A bit writable. This bit controls whether CPSR.A can be modified in Non-secure state:
• CPSR.A can be modified only in Secure state. This is the reset value.
• CPSR.A can be modified in any security state.

FW, [4]  
F bit writable. This bit controls whether CPSR.F can be modified in Non-secure state:
• CPSR.F can be modified only in Secure state. This is the reset value.
• CPSR.F can be modified in any security state.

EA, [3]  
External Abort handler. This bit controls which mode takes external aborts. The possible values are:

0  External aborts taken in abort mode. This is the reset value.
1  External aborts taken in Monitor mode.

FIQ, [2]  
FIQ handler. This bit controls which mode takes FIQ exceptions. The possible values are:
0FIQs taken in FIQ mode. This is the reset value.
1FIQs taken in Monitor mode.

**IRQ, [1]**

IRQ handler. This bit controls which mode takes IRQ exceptions. The possible values are:
0IRQs taken in IRQ mode. This is the reset value.
1IRQs taken in Monitor mode.

**NS, [0]**

Non-secure bit. Except when the processor is in Monitor mode, this bit determines the security state of the processor. The possible values are:
0Processor is in secure state. This is the reset value.
1Processor is in non-secure state.

To access the SCR:

| MRC p15,0,<Rt>,c1,c1,0 ; Read SCR into Rt |
| MCR p15,0,<Rt>,c1,c1,0 ; Write Rt to SCR |

Register access is encoded as follows:

<p>| Table B1-89 SCR access encoding |</p>
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0001</td>
<td>0001</td>
<td>000</td>
</tr>
</tbody>
</table>
**B1.105 System Control Register**

The SCTLR characteristics are:

**Purpose**

Provides the top level control of the system, including its memory system.

**Usage constraints**

The SCTLR is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Control bits in the SCTLR that are not applicable to a VMSA implementation read as the value that most closely reflects that implementation, and ignore writes.

Some bits in the register are read-only. These bits relate to non-configurable features of an implementation, and are provided for compatibility with previous versions of the architecture.

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

Write access to SCTLR(S) is disabled when the **CP15DISABLE2** signal is asserted HIGH.

**Attributes**

SCTLR is a 32-bit register.

![SCTLR bit assignments](image)

Reserved, RES0.

**TE, [30]**

T32 Exception enable. This bit controls whether exceptions are taken in A32 or T32 state:

- 0 Exceptions, including reset, taken in A32 state.
- 1 Exceptions, including reset, taken in T32 state.

The input **CFGTE** defines the reset value of the TE bit.

**AFE, [29]**

Access Flag Enable. This bit enables use of the AP[0] bit in the translation descriptors as the Access flag. It also restricts access permissions in the translation descriptors to the simplified model:
In the translation table descriptors, AP[0] is an access permissions bit. The full range of access permissions is supported. No Access flag is implemented. This is the reset value.

1 In the translation table descriptors, AP[0] is the Access flag. Only the simplified model for access permissions is supported.

TRE, [28]

TEX remap enable. This bit enables remapping of the TEX[2:1] bits for use as two translation table bits that can be managed by the operating system. Enabling this remapping also changes the scheme used to describe the memory region attributes in the VMSA:

0 TEX remap disabled. TEX[2:0] are used, with the C and B bits, to describe the memory region attributes. This is the reset value.

1 TEX remap enabled. TEX[2:1] are reassigned for use as bits managed by the operating system. The TEX[0], C and B bits are used to describe the memory region attributes, with the MMU remap registers.

[27:26]

Reserved, res0.

EE, [25]

Exception Endianness bit. The value of this bit defines the value of the CPSR.E bit on entry to an exception vector, including reset. This value also indicates the endianness of the translation table data for translation table lookups:

0 Little endian.
1 Big endian.

The input CFGEND defines the reset value of the EE bit.

[24]

Reserved, res0.

[23:22]

Reserved, res1.

[21]

Reserved, res0.

UWXN, [20]

Unprivileged write permission implies EL1 Execute Never (XN). This bit can be used to require all memory regions with unprivileged write permissions to be treated as XN for accesses from software executing at EL1.

0 Regions with unprivileged write permission are not forced to be XN, this is the reset value.

1 Regions with unprivileged write permission are forced to be XN for accesses from software executing at EL1.

WXN, [19]

Write permission implies Execute Never (XN). This bit can be used to require all memory regions with write permissions to be treated as XN.

0 Regions with write permission are not forced to be XN, this is the reset value.

1 Regions with write permissions are forced to be XN.

nTWE, [18]
Not trap WFE.

0 If a WFE instruction executed at EL0 would cause execution to be suspended, such as if the event register is not set and there is not a pending WFE wakeup event, it is taken as an exception to EL1 using the 0x1 ESR code.

1 WFE instructions are executed as normal.

[17]
Reserved, RES0.

nTWI, [16]
Not trap WFI.

0 If a WFI instruction executed at EL0 would cause execution to be suspended, such as if there is not a pending WFI wakeup event, it is taken as an exception to EL1 using the 0x1 ESR code.

1 WFI instructions are executed as normal.

[15:14]
Reserved, RES0.

V, [13]
Vectors bit. This bit selects the base address of the exception vectors:

0 Normal exception vectors, base address 0x00000000. Software can remap this base address using the VBAR.

1 High exception vectors, base address 0xFFFF0000. This base address is never remapped.

The input VINITHI defines the reset value of the V bit.

I, [12]
Instruction cache enable bit. This is a global enable bit for instruction caches:

0 Instruction caches disabled. If SCTLR.M is set to 0, instruction accesses from stage 1 of the EL0/EL1 translation regime are to Normal memory, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable.

1 Instruction caches enabled. If SCTLR.M is set to 0, instruction accesses from stage 1 of the EL0/EL1 translation regime are to Normal memory, Outer Shareable, Inner Write-Through, Outer Write-Through.

[11]
Reserved, RES1

[10:9]
Reserved, RES0

SED, [8]
SETEND Disable:

0 The SETEND instruction is available.

1 The SETEND instruction is UNALLOCATED.

ITD, [7]
IT Disable:

0 The IT instruction functionality is available.
All encodings of the IT instruction with hw1[3:0]!=1000 are UNDEFINED and treated as unallocated. All encodings of the subsequent instruction with the following values for hw1 are UNDEFINED (and treated as unallocated):

**11xxxxxxxxxxxxxx**  All 32-bit instructions, B(2), B(1), Undefined, SVC, Load/Store multiple

**1x1xxxxxxxxxxxxx**  Miscellaneous 16-bit instructions

**1x100xxxxxxxxxxx**  ADD Rd, PC, #imm

**01001xxxxxxxxxxx**  LDR Rd, [PC, #imm]

**0100x1xx1111xxx**  ADD(4),CMP(3), MOV, BX pc, BLX pc

**010001xx1xxxx111**  ADD(4),CMP(3), MOV

THEE, [6]
Reserved, RES0.

**CP15BEN, [5]**
CP15 barrier enable.

0  CP15 barrier operations disabled. Their encodings are UNDEFINED.
1  CP15 barrier operations enabled.

[4:3]
Reserved, RES1.

**C, [2]**
Cache enable. This is a global enable bit for data and unified caches:

0  Data and unified caches disabled, this is the reset value.
1  Data and unified caches enabled.

**A, [1]**
Alignment check enable. This is the enable bit for Alignment fault checking:

0  Alignment fault checking disabled, this is the reset value.
1  Alignment fault checking enabled.

**M, [0]**
MMU enable. This is a global enable bit for the MMU stage 1 address translation:

0  EL1 and EL0 stage 1 MMU disabled.
1  EL1 and EL0 stage 1 MMU enabled.

To access the SCTLR:

```
MRC p15, 0, <Rt>, c1, c0, 0 ; Read SCTLR into Rt
MCR p15, 0, <Rt>, c1, c0, 0 ; Write Rt to SCTLR
```

Register access is encoded as follows:

**Table B1-90  SCTLR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0001</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>
B1.106 Secure Debug Control Register

The SDCR characteristics are:

**Purpose**

Controls debug and performance monitors functionality in Secure state.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>NS</td>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>EL1</td>
<td></td>
<td></td>
<td>SCR.NS = 1</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL2</td>
<td></td>
<td></td>
<td>SCR.NS = 0</td>
<td>-</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Configurations**

Write access to SDCR is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**

SDCR is a 32-bit register.

![SDCR bit assignments](image)

**Figure B1-59 SDCR bit assignments**

- **[31:22]**
  - Reserved, RES0.

- **EPMAD, [21]**
  - External debugger access to Performance Monitors registers disabled. This disables access to these registers by an external debugger:
    - 0 Access to Performance Monitors registers from external debugger is permitted. This is the reset value.
    - 1 Access to Performance Monitors registers from external debugger is disabled, unless overridden by authentication interface.

- **EDAD, [20]**
  - External debugger access to breakpoint and watchpoint registers disabled. This disables access to these registers by an external debugger:
    - 0 Access to breakpoint and watchpoint registers from external debugger is permitted. This is the reset value.
    - 1 Access to breakpoint and watchpoint registers from external debugger is disabled, unless overridden by authentication interface.

- **[19:18]**
  - Reserved, RES0.

- **SPME, [17]**
  - Secure performance monitors enable. This allows event counting in Secure state:
0 Event counting prohibited in Secure state, unless overridden by the authentication interface.
   This is the reset value.
1 Event counting allowed in Secure state.

[16]
Reserved, RES0.

SPD, [15:14]

AArch32 secure privileged debug. Enables or disables debug exceptions in Secure state, other than Software breakpoint instructions. The possible values are:
0b00 Legacy mode. Debug exceptions from Secure EL1 are enabled by the authentication interface.
0b10 Secure privileged debug disabled. Debug exceptions from Secure EL1 are disabled.
0b11 Secure privileged debug enabled. Debug exceptions from Secure EL1 are enabled.
The value 0b01 is reserved.
If debug exceptions from Secure EL1 are enabled, then debug exceptions from Secure EL0 are also enabled.
Otherwise, debug exceptions from Secure EL0 are enabled only if SDER32_EL3.SUIDEN is 1.
SPD is ignored in Non-secure state. Debug exceptions from Software breakpoint instruction debug events are always enabled.

[13:0]
Reserved, RES0.

To access the SDCR:

MRC p15,0,<Rt>,c1,c3,1 ; Read SDCR into Rt
MCR p15,0,<Rt>,c1,c3,1 ; Write Rt to SDCR

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0001</td>
<td>0011</td>
<td>001</td>
</tr>
</tbody>
</table>

Table B1-91 SDCR access encoding
B1.107 Secure Debug Enable Register

The SDER characteristics are:

**Purpose**
Controls invasive and non-invasive debug in the Secure EL0 state.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**
This register is accessible only in Secure state.
Write access to SDER is disabled when the **CP15SDDISABLE2** signal is asserted HIGH.

**Attributes**
SDER is a 32-bit register.

![SDER bit assignments](image)

Figure B1-60 SDER bit assignments

[31:2] Reserved, RES0.

**SUNIDEN, [1]**
Secure User Non-invasive Debug Enable. The possible values are:
0 Non-invasive debug not permitted in Secure EL0 state. This is the Warm reset value.
1 Non-invasive debug permitted in Secure EL0 state.

**SUIDEN, [0]**
Secure User Invasive Debug Enable. The possible values are:
0 Invasive debug not permitted in Secure EL0 state. This is the Warm reset value.
1 Invasive debug permitted in Secure EL0 state.

To access the SDER:

MRC p15,0,<Rt>,c1,c1,1 ; Read SDER into Rt
MCR p15,0,<Rt>,c1,c1,1 ; Write Rt to SDER

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0001</td>
<td>0001</td>
<td>001</td>
</tr>
</tbody>
</table>

Table B1-92 SDER access encoding
**B1.108 TCM Type Register**

TCMTR

The processor does not implement the features described by the TCMTR. This register is always RAZ.
B1.109  TLB Type Register

TLBTR

The processor does not implement the features described by the TLBTR. This register is always RAZ.
B1.110 Translation Table Base Control Register

The TTBCR characteristics are:

**Purpose**
Determines which of the Translation Table Base Registers defines the base address for a translation table walk required for the stage 1 translation of a memory access from any mode other than Hyp mode. Also controls the translation table format and, when using the Long-descriptor translation table format, holds cacheability and shareability information.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

The processor does not use the implementation-defined bit, TTBCR[30], when using the Long-descriptor translation table format, so this bit is RES0.

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.
Write access to TTBCR(S) is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**
TTBCR is a 32-bit register.
There are two formats for this register. TTBCR.EAE determines which format of the register is used.
**B1.111 TTBCR with Short-descriptor translation table format**

TTBCR has a specific format when using the Short-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBCR bit assignments when TTBCR.EAE is 0.

![TTBCR bit assignments, TTBCR.EAE is 0](image)

**EAE, [31]**

Extended Address Enable.

0 Use the 32-bit translation system, with the Short-descriptor translation table format.

**[30:6]**

Reserved, RES0.

**PD1, [5]**

Translation table walk disable for translations using TTBR1. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR1. The possible values are:

0 Perform translation table walks using TTBR1.

1 A TLB miss on an address that is translated using TTBR1 generates a Translation fault. No translation table walk is performed.

**PD0, [4]**

Translation table walk disable for translations using TTBR0. This bit controls whether a translation table walk is performed on a TLB miss for an address that is translated using TTBR0. The possible values are:

0 Perform translation table walks using TTBR0.

1 A TLB miss on an address that is translated using TTBR0 generates a Translation fault. No translation table walk is performed.

**[3]**

Reserved, RES0.

**N, [2:0]**

Indicate the width of the base address held in TTBR0. In TTBR0, the base address field is bits[31:14-N]. The value of N also determines:

- Whether TTBR0 or TTBR1 is used as the base address for translation table walks.
- The size of the translation table pointed to by TTBR0.

N can take any value from 0 to 7, that is, from 0b000 to 0b111.

When N has its reset value of 0, the translation table base is compatible with Armv5 and Armv6.

Resets to 0.
B1.112  TTBCR with Long-descriptor translation table format

TTBCR has a specific format when using the Long-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBCR bit assignments when TTBCR.EAE is 1.

![Figure B1-62 TTBCR bit assignments, TTBCR.EAE is 1](image)

EAE, [31]

Extended Address Enable:

1 Use the 40-bit translation system, with the Long-descriptor translation table format.

[30]

Reserved, RES0.

SH1, [29:28]

Shareability attribute for memory associated with translation table walks using TTBR1:

- 0b00 Non-shareable.
- 0b10 Outer Shareable.
- 0b11 Inner Shareable.

Other values are reserved.

Resets to 0.

ORGN1, [27:26]

Outer cacheability attribute for memory associated with translation table walks using TTBR1:

- 0b00 Normal memory, Outer Non-cacheable.
- 0b01 Normal memory, Outer Write-Back Write-Allocate Cacheable.
- 0b10 Normal memory, Outer Write-Through Cacheable.
- 0b11 Normal memory, Outer Write-Back no Write-Allocate Cacheable.

Resets to 0.

IRGN1, [25:24]

Inner cacheability attribute for memory associated with translation table walks using TTBR1:

- 0b00 Normal memory, Inner Non-cacheable.
- 0b01 Normal memory, Inner Write-Back Write-Allocate Cacheable.
- 0b10 Normal memory, Inner Write-Through Cacheable.
- 0b11 Normal memory, Inner Write-Back no Write-Allocate Cacheable.

Resets to 0.

EPD1, [23]
Translation table walk disable for translations using TTBR1. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR1:

0  
Perform translation table walks using TTBR1.

1  
A TLB miss on an address that is translated using TTBR1 generates a Translation fault. No translation table walk is performed.

A1, [22]  
Selects whether TTBR0 or TTBR1 defines the ASID:

0  TTBR0.ASID defines the ASID.
1  TTBR1.ASID defines the ASID.

[21:19]  
Reserved, RES0.

T1SZ, [18:16]  
The size offset of the memory region addressed by TTBR1. The region size is $2^{32-T1SZ}$ bytes. Resets to 0.

[15:14]  
Reserved, RES0.

SH0, [13:12]  
Shareability attribute for memory associated with translation table walks using TTBR0:

00  Non-shareable.
01  Outer Shareable.
11  Inner Shareable.

Other values are reserved.
Resets to 0.

ORGN0, [11:10]  
Outer cacheability attribute for memory associated with translation table walks using TTBR0:

00  Normal memory, Outer Non-cacheable.
01  Normal memory, Outer Write-Back Write-Allocate Cacheable.
10  Normal memory, Outer Write-Through Cacheable.
11  Normal memory, Outer Write-Back no Write-Allocate Cacheable.

Resets to 0.

IRGN0, [9:8]  
Inner cacheability attribute for memory associated with translation table walks using TTBR0:

00  Normal memory, Inner Non-cacheable.
01  Normal memory, Inner Write-Back Write-Allocate Cacheable.
10  Normal memory, Inner Write-Through Cacheable.
11  Normal memory, Inner Write-Back no Write-Allocate Cacheable.

Resets to 0.
**EPD0, [7]**
Translation table walk disable for translations using TTBR0. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR0:

0  Perform translation table walks using TTBR0.
1  A TLB miss on an address that is translated using TTBR0 generates a Translation fault. No translation table walk is performed.

**[6:3]**
Reserved, RES0.

**T0SZ, [2:0]**
The size offset of the memory region addressed by TTBR0. The region size is $2^{32-T0SZ}$ bytes.
Resets to 0.

To access the TTBCR:

```
MRC p15,0,<Rt>,c2,c0,0 ; Read TTBR0 into Rt
MCR p15,0,<Rt>,c2,c0,0 ; Write Rt to TTBR0
```

Register access is encoded as follows:

**Table B1-93 TTBCR access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0010</td>
<td>0000</td>
<td>010</td>
</tr>
</tbody>
</table>
B1.113 Translation Table Base Register 0

The TTBR0 characteristics are:

**Purpose**
Holds the base address of translation table 0, and information about the memory it occupies. This is one of the translation tables for the stage 1 translation of memory accesses from modes other than Hyp mode.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Used in conjunction with the TTBCR. When the 64-bit TTBR0 format is used, cacheability and shareability information is held in the TTBCR and not in TTBR0.

**Configurations**
There are separate Secure and Non-secure instances of this register at EL3.

**Attributes**
TTBR0 is:
- A 32-bit register when TTBCR.EAE is 0.
- A 64-bit register when TTBCR.EAE is 1.

There are different formats for this register. TTBCR.EAE determines which format of the register is used.
**B1.114 TTBR0 with Short-descriptor translation table format**

TTBR0 has a specific format when using the Short-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBR0 bit assignments when TTBCR.EAE is 0.

![TTBR0 bit assignments](image)

**Figure B1-63 TTBR0 bit assignments, TTBCR.EAE is 0**

**TTB0, [31:7]**

Translation table base 0 address, bits[31:x], where x is 14-(TTBCR.N). Bits [x-1:7] are RES0.

The value of x determines the required alignment of the translation table, that must be aligned to $2^x$ bytes.

If bits [x-1:7] are not all zero, this is a misaligned Translation Table Base Address. Its effects are **CONSTRAINED UNPREDICTABLE**, where bits [x-1:7] are treated as if all the bits are zero. The value read back from those bits is the value written.

**IRGN[0], [6]**

See bit[0] for description of the IRGN field.

**NOS, [5]**

Not Outer Shareable bit. Indicates the Outer Shareable attribute for the memory associated with a translation table walk that has the Shareable attribute, indicated by TTBR0.S is 1. The possible values are:

- 0 Outer Shareable.
- 1 Inner Shareable.

This bit is ignored when TTBR0.S is 0.

**RGN, [4:3]**

Region bits. Indicates the Outer cacheability attributes for the memory associated with the translation table walks. The possible values are:

- 00 Normal memory, Outer Non-cacheable.
- 01 Normal memory, Outer Write-Back Write-Allocate Cacheable.
- 10 Normal memory, Outer Write-Through Cacheable.
- 11 Normal memory, Outer Write-Back no Write-Allocate Cacheable.

**[2]**

Reserved, RES0.

**S, [1]**

Shareable bit. Indicates the Shareable attribute for the memory associated with the translation table walks. The possible values are:

- 0 Non-shareable.
IRGN[1], [0]

Inner region bits. Indicates the Inner Cacheability attributes for the memory associated with the translation table walks. The possible values of IRGN[1:0] are:

- \(0b00\) Normal memory, Inner Non-cacheable.
- \(0b01\) Normal memory, Inner Write-Back Write-Allocate Cacheable.
- \(0b10\) Normal memory, Inner Write-Through Cacheable.
- \(0b11\) Normal memory, Inner Write-Back no Write-Allocate Cacheable.

The encoding of the IRGN bits is counter-intuitive, with register bit[6] being IRGN[0] and register bit[0] being IRGN[1]. This encoding is chosen to give a consistent encoding of memory region types and to ensure that software written for Armv7 without the Multiprocessing Extensions can run unmodified on an implementation that includes the functionality introduced by the Armv7 Multiprocessing Extensions.

To access the TTBR0 when TTBCR.EAE is 0:

| MRC p15,0,<Rt>,c2,c0,0 ; Read TTBR0 into Rt |
| MCR p15,0,<Rt>,c2,c0,0 ; Write Rt to TTBR0 |

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>Table B1-94 TTBR0 access encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>coproc</td>
</tr>
<tr>
<td>111</td>
</tr>
</tbody>
</table>
TTBR0 has a specific format when using the Long-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBR0 bit assignments when TTBCR.EAE is 1.

![TTBR0 bit assignments, TTBCR.EAE is 1](image)

[63:56]
Reserved, RES0.

ASID, [55:48]
An ASID for the translation table base address. The TTBCR.A1 field selects either TTBR0.ASID or TTBR1.ASID.

BADDR[47:x], [47:0]
Translation table base address, bits[47:x]. Bits [x-1:0] are RES0.

x is based on the value of TTBCR.T0SZ, and is calculated as follows:
- If TTBCR.T0SZ is 0 or 1, \( x = 5 - \text{TTBCR.T0SZ} \).
- If TTBCR.T0SZ is greater than 1, \( x = 14 - \text{TTBCR.T0SZ} \).

The value of x determines the required alignment of the translation table, that must be aligned to \( 2x \) bytes.

If bits [x-1:3] are not all zero, this is a misaligned Translation Table Base Address. Its effects are constrained unpredictable, where bits [x-1:0] are treated as if all the bits are zero. The value read back from those bits is the value written.

To access the TTBR0 when TTBCR.EAE==1:

```
MRRC p15,0,<Rt>,<Rt2>,c2 ; Read 64-bit TTBR0 into Rt (low word) and Rt2 (high word)
MCRR p15,0,<Rt>,<Rt2>,c2 ; Write Rt (low word) and Rt2 (high word) to 64-bit TTBR0
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>0000</td>
<td>0010</td>
</tr>
</tbody>
</table>

Table B1-95 TTBR0 access encoding
B1.116 Translation Table Base Register 1

The TTBR1 characteristics are:

**Purpose**

Holds the base address of translation table 1, and information about the memory it occupies. This is one of the translation tables for the stage 1 translation of memory accesses from modes other than Hyp mode.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Used in conjunction with the TTBCR. When the 64-bit TTBR1 format is used, cacheability and shareability information is held in the TTBCR and not in TTBR1. See B1.110 Translation Table Base Control Register on page B1-333.

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

Write access to TTBR1(S) is disabled when the CP15SDISABLE2 signal is asserted HIGH.

**Attributes**

TTBR1 is:

- A 32-bit register when TTBCR.EAE is 0.
- A 64-bit register when TTBCR.EAE is 1.

There are two formats for this register. TTBCR.EAE determines which format of the register is used.
**B1.117 TTBR1 with Short-descriptor translation table format**

TTBR1 has a specific format when using the Short-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBR1 bit assignments when TTBCR.EAE is 0.

![TTBR1 bit assignments, TTBCR.EAE is 0](image)

**TTB1, [31:7]**
Translation table base 1 address, bits[31:x], where x is 14-(TTBCR.N). Bits [x-1:7] are RES0.

The translation table must be aligned on a 16KByte boundary.

If bits [x-1:7] are not all zero, this is a misaligned Translation Table Base Address. Its effects are CONSTRAINED UNPREDICTABLE, where bits [x-1:7] are treated as if all the bits are zero. The value read back from those bits is the value written.

**IRGN[0], [6]**
See IRGN[1] below for description of the IRGN field.

**NOS, [5]**
Not Outer Shareable bit. Indicates the Outer Shareable attribute for the memory associated with a translation table walk that has the Shareable attribute, indicated by TTBR0.S is 1. The possible values are:

0 Outer Shareable.
1 Inner Shareable.

This bit is ignored when TTBR0.S is 0.

**RGN, [4:3]**
Region bits. Indicates the Outer cacheability attributes for the memory associated with the translation table walks. The possible values are:

00 Normal memory, Outer Non-cacheable.
01 Normal memory, Outer Write-Back Write-Allocate Cacheable.
10 Normal memory, Outer Write-Through Cacheable.
11 Normal memory, Outer Write-Back no Write-Allocate Cacheable.

**IMP, [2]**
Reserved, RES0.

**S, [1]**
Shareable bit. Indicates the Shareable attribute for the memory associated with the translation table walks. The possible values are:

0 Non-shareable.
1 Shareable.

**IRGN[1], [0]**
Inner region bits. Indicates the Inner Cacheability attributes for the memory associated with the translation table walks. The possible values of IRGN[1:0] are:

- **0b00**: Normal memory, Inner Non-cacheable.
- **0b01**: Normal memory, Inner Write-Back Write-Allocate Cacheable.
- **0b10**: Normal memory, Inner Write-Through Cacheable.
- **0b11**: Normal memory, Inner Write-Back no Write-Allocate Cacheable.

The encoding of the IRGN bits is counter-intuitive, with register bit[6] being IRGN[0] and register bit[0] being IRGN[1]. This encoding is chosen to give a consistent encoding of memory region types and to ensure that software written for Armv7 without the Multiprocessing Extensions can run unmodified on an implementation that includes the functionality introduced by the Armv7 Multiprocessing Extensions.

To access the TTBR1 when TTBCR.EAE is 0:

```
MRC p15, 0, <Rt>, c2, c0, 1 ; Read TTBR1 into Rt
MCR p15, 0, <Rt>, c2, c0, 1 ; Write Rt to TTBR1
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0010</td>
<td>000</td>
<td>001</td>
</tr>
</tbody>
</table>

Table B1-96 TTBR1 access encoding
TTBR1 with Long-descriptor translation table format

TTBR1 has a specific format when using the Long-descriptor translation table format. TTBCR.EAE determines which format of the register is in use.

The following figure shows the TTBR1 bit assignments when TTBCR.EAE is 1.

![TTBR1 bit assignments, TTBCR.EAE is 1](image)

**Figure B1-66 TTBR1 bit assignments, TTBCR.EAE is 1**

- **[63:56]**
  - Reserved, RES0.

- **ASID, [55:48]**
  - An ASID for the translation table base address. The TTBCR.A1 field selects either TTBR0.ASID or TTBR1.ASID.

- **BADDR[47:x], [47:0]**
  - Translation table base address, bits[47:x]. Bits [x-1:0] are RES0.
  - x is based on the value of TTBCR.T0SZ, and is calculated as follows:
    - If TTBCR.T0SZ is 0 or 1, x = 5 - TTBCR.T0SZ.
    - If TTBCR.T0SZ is greater than 1, x = 14 - TTBCR.T0SZ.
  - The value of x determines the required alignment of the translation table, that must be aligned to 2x bytes.

  If bits [x-1:3] are not all zero, this is a misaligned Translation Table Base Address. Its effects are constrained unpredictable, where bits [x-1:0] are treated as if all the bits are zero. The value read back from those bits is the value written.

To access the 64-bit TTBR1 when TTBCR.EAE = 1:

```
MRRC p15, 1, <Rt>, <Rt2>, c2 ; Read 64-bit TTBR1 into Rt (low word) and Rt2 (high word)
MCRR p15, 1, <Rt>, <Rt2>, c2 ; Write Rt (low word) and Rt2 (high word) to 64-bit TTBR1
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>0001</td>
<td>0010</td>
</tr>
</tbody>
</table>

Table B1-97 TTBR0 access encoding
B1.119 Vector Base Address Register

The VBAR characteristics are:

**Purpose**

Holds the exception base address for exceptions that are not taken to Monitor mode or to Hyp mode when high exception vectors are not selected.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Software must program the Non-secure instance of the register with the required initial value as part of the processor boot sequence.

**Configurations**

There are separate Secure and Non-secure instances of this register at EL3.

Write access to VBAR(S) is disabled when the **CP15SDISABLE2** signal is asserted HIGH.

**Attributes**

VBAR is a 32-bit register.

![Figure B1-67 VBAR bit assignments](image)

**Vector Base Address, [31:5]**

Bits[31:5] of the base address of the exception vectors, for exceptions taken in this exception level. Bits[4:0] of an exception vector are the exception offset.

[4:0]

Reserved, **RES0**.

To access the VBAR:

```
MRC p15, 0, <Rt>, c12, c0, 0 ; Read VBAR into Rt
MCR p15, 0, <Rt>, c12, c0, 0 ; Write Rt to VBAR
```

Register access is encoded as follows:

![Table B1-98 VBAR access encoding](image)
B1.120 Virtualization Multiprocessor ID Register

The VMPIDR characteristics are:

**Purpose**

Provides the value of the Virtualization Multiprocessor ID. This is the value returned by Non-secure EL1 reads of MPIDR.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

This register is accessible only at EL2 or EL3.

**Attributes**

VMPIDR is a 32-bit register.

VMPIDR resets to the value of MPIDR.

![VMPIDR bit assignments](image)

**VMPIDR, [31:0]**

MPIDR value returned by Non-secure EL1 reads of the MPIDR. The MPIDR description defines the subdivision of this value. See Figure B1-51 MPIDR bit assignments on page B1-309.

To access the VMPIDR:

```
MRC p15,4,<Rt>,c0,c0,5 ; Read VMPIDR into Rt
MCR p15,4,<Rt>,c0,c0,5 ; Write Rt to VMPIDR
```

Register access is encoded as follows:

![VMPIDR access encoding](image)
B1.121 Virtualization Processor ID Register

The VPIDR characteristics are:

**Purpose**

Holds the value of the Virtualization Processor ID. This is the value returned by Non-secure EL1 reads of MIDR. See Figure B1-50 MIDR bit assignments on page B1-307.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2</th>
<th>EL3 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>-</td>
</tr>
</tbody>
</table>

**Configurations**

There are no configuration notes.

**Attributes**

VPIDR is a 32-bit register.

VPIDR resets to the value of MIDR.

![VPIDR bit assignments](image)

**VPIDR, [31:0]**

MIDR value returned by Non-secure PL1 reads of the MIDR. The MIDR description defines the subdivision of this value. See Figure B1-50 MIDR bit assignments on page B1-307.

To access the VPIDR:

```
MRC p15,4,<Rt>,c0,c0,0 ; Read VPIDR into Rt
MCR p15,4,<Rt>,c0,c0,0 ; Write Rt to VPIDR
```

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0000</td>
<td>0000</td>
<td>000</td>
</tr>
</tbody>
</table>

Table B1-100 VPIDR access encoding
B1.122 Virtualization Translation Control Register

The VTCR characteristics are:

**Purpose**

Controls the translation table walks required for the stage 2 translation of memory accesses from Non-secure modes other than Hyp mode, and holds cacheability and shareability information for the accesses.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

Used in conjunction with VTTBR, that defines the translation table base address for the translations.

**Configurations**

This register is accessible only at EL2 or EL3.

**Attributes**

VTCR is a 32-bit register.

![VTCR bit assignments](image)

[31]

Reserved, RES1.

[30:14]

Reserved, RES0.

**SH0, [13:12]**

Shareability attribute for memory associated with translation table walks using TTBR0.

- 0b00: Non-shareable.
- 0b01: Reserved.
- 0b10: Outer Shareable.
- 0b11: Inner Shareable.

**ORGN0, [11:10]**

Outer cacheability attribute for memory associated with translation table walks using TTBR0.

- 0b00: Normal memory, Outer Non-cacheable.
- 0b01: Normal memory, Outer Write-Back Write-Allocate Cacheable.
- 0b10: Normal memory, Outer Write-Through Cacheable.
- 0b11: Normal memory, Outer Write-Back no Write-Allocate Cacheable.
IRGN0, [9:8]

Inner cacheability attribute for memory associated with translation table walks using TTBR0.

- **0b00**  Normal memory, Inner Non-cacheable.
- **0b01**  Normal memory, Inner Write-Back Write-Allocate Cacheable.
- **0b10**  Normal memory, Inner Write-Through Cacheable.
- **0b11**  Normal memory, Inner Write-Back no Write-Allocate Cacheable.

SL0, [7:6]

Starting level for translation table walks using VTTBR:

- **0b00**  Start at second level.
- **0b01**  Start at first level.

[5]

Reserved, RES0.

S, [4]

Sign extension bit. This bit must be programmed to the value of T0SZ[3]. If it is not, then the stage 2 T0SZ value is treated as an **UNKNOWN** value within the legal range that can be programmed.

T0SZ, [3:0]

The size offset of the memory region addressed by TTBR0. The region size is \(2^{32-\text{T0SZ}}\) bytes.

To access the VTCR:

- **MRC p15, 4, <Rt>, c2, c1, 2; Read VTCR into Rt**
- **MCR p15, 4, <Rt>, c2, c1, 2; Write Rt to VTCR**

Register access is encoded as follows:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>100</td>
<td>0010</td>
<td>0001</td>
<td>010</td>
</tr>
</tbody>
</table>

**Table B1-101  VTCR access encoding**
This chapter describes the GIC registers.

It contains the following sections:

- **B2.1 CPU interface register summary** on page B2-352.
- **B2.2 Active Priority Register** on page B2-353.
- **B2.3 CPU Interface Identification Register** on page B2-354.
- **B2.4 Virtual interface control register summary** on page B2-355.
- **B2.5 VGIC Type Register** on page B2-356.
- **B2.6 Virtual CPU interface register summary** on page B2-357.
- **B2.7 VM Active Priority Register** on page B2-358.
- **B2.8 VM CPU Interface Identification Register** on page B2-359.
B2.1 CPU interface register summary

Each CPU interface block provides the interface for a Cortex-A32 processor that interfaces with a GIC distributor within the system.

Each CPU interface provides a programming interface for:
- Enabling the signaling of interrupt requests by the CPU interface.
- Acknowledging an interrupt.
- Indicating completion of the processing of an interrupt.
- Setting an interrupt priority mask for the processor.
- Defining the preemption policy for the processor.
- Determining the highest priority pending interrupt for the processor.
- Generating SGIs.

For more information on the CPU interface, see the Arm® Generic Interrupt Controller Architecture Specification.

The following table lists the registers for the CPU interface.

All the registers in the following table are word-accessible. Registers not described in this table are RES0. See the Arm® Generic Interrupt Controller Architecture Specification for more information.

Table B2-1 CPU interface register summary

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>GICC_CTLR</td>
<td>RW</td>
<td>0x00000000</td>
<td>CPU Interface Control Register</td>
</tr>
<tr>
<td>0x0004</td>
<td>GICC_PMR</td>
<td>RW</td>
<td>0x00000000</td>
<td>Interrupt Priority Mask Register</td>
</tr>
<tr>
<td>0x0008</td>
<td>GICC_BPR</td>
<td>RW</td>
<td>0x00000002</td>
<td>Binary Point Register (Secure)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0x00000003</td>
<td>(Non-secure)</td>
</tr>
<tr>
<td>0x000C</td>
<td>GICC_IAR</td>
<td>RO</td>
<td>-</td>
<td>Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>0x0010</td>
<td>GICC_EOIR</td>
<td>WO</td>
<td>-</td>
<td>End Of Interrupt Register</td>
</tr>
<tr>
<td>0x0014</td>
<td>GICC_RPR</td>
<td>RO</td>
<td>0x000000FF</td>
<td>Running Priority Register</td>
</tr>
<tr>
<td>0x0018</td>
<td>GICC_HPPR</td>
<td>RO</td>
<td>0x000003FF</td>
<td>Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>0x001C</td>
<td>GICC_ABPR</td>
<td>RW</td>
<td>0x00000003</td>
<td>Aliased Binary Point Register</td>
</tr>
<tr>
<td>0x0020</td>
<td>GICC_AIAR</td>
<td>RO</td>
<td>-</td>
<td>Aliased Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>0x0024</td>
<td>GICC_AEOIR</td>
<td>WO</td>
<td>-</td>
<td>Aliased End of Interrupt Register</td>
</tr>
<tr>
<td>0x0028</td>
<td>GICC_AHPPIR</td>
<td>RO</td>
<td>0x000003FF</td>
<td>Aliased Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>0x00D0</td>
<td>GICC_APR0</td>
<td>RW</td>
<td>0x00000000</td>
<td>B2.2 Active Priority Register on page B2-353</td>
</tr>
<tr>
<td>0x00E0</td>
<td>GICC_NSPR0</td>
<td>RW</td>
<td>0x00000000</td>
<td>Non-secure Active Priority Register</td>
</tr>
<tr>
<td>0x00FC</td>
<td>GICC_IDR</td>
<td>RO</td>
<td>0x0014243B</td>
<td>B2.3 CPU Interface Identification Register on page B2-354</td>
</tr>
<tr>
<td>0x1000</td>
<td>GICC_DIR</td>
<td>WO</td>
<td>-</td>
<td>Deactivate Interrupt Register</td>
</tr>
</tbody>
</table>
B2.2 Active Priority Register

The GICC_APR0 characteristics are:

**Purpose**
Provides support for preserving and restoring state in power management applications.

**Usage constraints**
This register is banked to provide Secure and Non-secure copies. This ensures that Non-secure accesses do not interfere with Secure operation.

**Configurations**
Available in all configurations.

**Attributes**
See the register summary in *B2.1 CPU interface register summary* on page B2-352.

The Cortex-A32 processor implements the GICC_APR0 according to the recommendations described in the *Arm Generic Interrupt Controller Architecture Specification*.

Table B2-2 Active Priority Register implementation

<table>
<thead>
<tr>
<th>Number of group priority bits</th>
<th>Preemption levels</th>
<th>Minimum value of Secure GICC_BPR</th>
<th>Minimum legal value of Non-secure GICC_BPR</th>
<th>Active Priority Registers implemented</th>
<th>View of Active Priority Registers for Non-secure accesses</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>32</td>
<td>2</td>
<td>3</td>
<td>GICC_APR0 [31:0]</td>
<td>GICC_NSAPR0 [31:16] appears as GICC_APR0 [15:0]</td>
</tr>
</tbody>
</table>
B2.3 CPU Interface Identification Register

The GICC_IIDR characteristics are:

**Purpose**
Provides information about the implementer and revision of the CPU interface.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See the register summary in *B2.1 CPU interface register summary* on page B2-352.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>ProductID</td>
<td>Identifies the product: 0x001 Cortex-A32 processor.</td>
</tr>
<tr>
<td>19:16</td>
<td>Architecture version</td>
<td>Identifies the architecture version of the GIC CPU interface: 0x4 GICv4.</td>
</tr>
<tr>
<td>15:12</td>
<td>Revision</td>
<td>Identifies the revision number for the CPU interface: 0x2 r1p0.</td>
</tr>
<tr>
<td>11:0</td>
<td>Implementer</td>
<td>Contains the JEP106 code of the company that implements the CPU interface: 0x43B Arm.</td>
</tr>
</tbody>
</table>

Figure B2-1 GICC_IIDR bit assignments
B2.4 Virtual interface control register summary

The virtual interface control registers are management registers. Configuration software on the Cortex-A32 processor must ensure they are accessible only by a hypervisor, or similar software.

The following table describes the registers for the virtual interface control registers. All these registers are word-accessible. Registers not described in this table are RES0. See the Arm® Generic Interrupt Controller Architecture Specification for more information.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>GICH_HCR</td>
<td>RW</td>
<td>0x00000000</td>
<td>Hypervisor Control Register</td>
</tr>
<tr>
<td>0x004</td>
<td>GICH_VTR</td>
<td>RO</td>
<td>0x90000003</td>
<td>B2.5 VGIC Type Register on page B2-356</td>
</tr>
<tr>
<td>0x008</td>
<td>GICH_VMCR</td>
<td>RW</td>
<td>0x004C0000</td>
<td>Virtual Machine Control Register</td>
</tr>
<tr>
<td>0x010</td>
<td>GICH_MISR</td>
<td>RO</td>
<td>0x00000000</td>
<td>Maintenance Interrupt Status Register</td>
</tr>
<tr>
<td>0x020</td>
<td>GICH_EISR0</td>
<td>RO</td>
<td>0x00000000</td>
<td>End of Interrupt Status Registers</td>
</tr>
<tr>
<td>0x030</td>
<td>GICH_ELRSR0</td>
<td>RO</td>
<td>0x0000000F</td>
<td>Empty List Register Status Registers</td>
</tr>
<tr>
<td>0x0F0</td>
<td>GICH_APR0</td>
<td>RW</td>
<td>0x00000000</td>
<td>Active Priorities Register</td>
</tr>
<tr>
<td>0x100</td>
<td>GICH_LR0</td>
<td>RW</td>
<td>0x00000000</td>
<td>List Register 0</td>
</tr>
<tr>
<td>0x104</td>
<td>GICH_LR1</td>
<td>RW</td>
<td>0x00000000</td>
<td>List Register 1</td>
</tr>
<tr>
<td>0x108</td>
<td>GICH_LR2</td>
<td>RW</td>
<td>0x00000000</td>
<td>List Register 2</td>
</tr>
<tr>
<td>0x10C</td>
<td>GICH_LR3</td>
<td>RW</td>
<td>0x00000000</td>
<td>List Register 3</td>
</tr>
</tbody>
</table>
B2.5 VGIC Type Register

The GICH_VTR characteristics are:

**Purpose**

Holds information on number of priority bits, number of preemption bits, and number of List Registers implemented.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See the register summary in *B2.4 Virtual interface control register summary on page B2-355*.

**Figure B2-2 GICH_VTR bit assignments**

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRIbits</td>
<td>Indicates the number of priority bits implemented, minus one:</td>
<td>0x4</td>
</tr>
<tr>
<td>PREbits</td>
<td>Indicates the number of preemption bits implemented, minus one:</td>
<td>0x4</td>
</tr>
<tr>
<td>RES0</td>
<td>Reserved, RES0.</td>
<td></td>
</tr>
<tr>
<td>ListRegs</td>
<td>Indicates the number of implemented List Registers, minus one:</td>
<td>0x3</td>
</tr>
</tbody>
</table>

**PRIbits, [31:29]**

Indicates the number of priority bits implemented, minus one:

- 0x4 Five bits of priority and 32 priority levels.

**PREbits, [28:26]**

Indicates the number of preemption bits implemented, minus one:

- 0x4 Five bits of preemption and 32 preemption levels.

**[25:6]**

Reserved, RES0.

**ListRegs, [5:0]**

Indicates the number of implemented List Registers, minus one:

- 0x3 Four List Registers.
B2.6 Virtual CPU interface register summary

The virtual CPU interface forwards virtual interrupts to a connected Cortex-A32 processor, subject to the normal GIC handling and prioritization rules.

The virtual interface control registers control virtual CPU interface operations. In particular, the virtual CPU interface uses the contents of the List registers to determine when to signal virtual interrupts. When a core accesses the virtual CPU interface, the List registers are updated. For more information on the virtual CPU interface, see the Arm® Generic Interrupt Controller Architecture Specification.

The following table describes the registers for the virtual CPU interface.

All the registers in the following table are word-accessible. Registers not described in this table are RES0.

See the Arm® Generic Interrupt Controller Architecture Specification for more information.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>GICV_CTLR</td>
<td>RW</td>
<td>0x00000000</td>
<td>VM Control Register</td>
</tr>
<tr>
<td>GICV_PMR</td>
<td>RW</td>
<td>0x00000000</td>
<td>VM Priority Mask Register</td>
</tr>
<tr>
<td>GICV_BPR</td>
<td>RW</td>
<td>0x00000002</td>
<td>VM Binary Point Register</td>
</tr>
<tr>
<td>GICV_IAR</td>
<td>RO</td>
<td>-</td>
<td>VM Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>GICV_EOIR</td>
<td>WO</td>
<td>-</td>
<td>VM End Of Interrupt Register</td>
</tr>
<tr>
<td>GICV_RPR</td>
<td>RO</td>
<td>0x000000FF</td>
<td>VM Running Priority Register</td>
</tr>
<tr>
<td>GICV_HPPIR</td>
<td>RO</td>
<td>0x000003FF</td>
<td>VM Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>GICV_ABPR</td>
<td>RW</td>
<td>0x00000003</td>
<td>VM Aliased Binary Point Register</td>
</tr>
<tr>
<td>GICV_AIAR</td>
<td>RO</td>
<td>-</td>
<td>VM Aliased Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>GICV_AEOIR</td>
<td>WO</td>
<td>-</td>
<td>VM Aliased End of Interrupt Register</td>
</tr>
<tr>
<td>GICV_AHPPIR</td>
<td>RO</td>
<td>0x000003FF</td>
<td>VM Aliased Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>GICV_APR0</td>
<td>RW</td>
<td>0x00000000</td>
<td>B2.7 VM Active Priority Register on page B2-358</td>
</tr>
<tr>
<td>GICV_IIDR</td>
<td>RO</td>
<td>0x014243B</td>
<td>B2.8 VM CPU Interface Identification Register on page B2-359</td>
</tr>
<tr>
<td>GICV_DIR</td>
<td>WO</td>
<td>-</td>
<td>VM Deactivate Interrupt Register</td>
</tr>
</tbody>
</table>
B2.7 VM Active Priority Register

GICV_APR0

For software compatibility, this register is present in the virtual CPU interface. However, in a virtualized system, it is not used when preserving and restoring state.

The GICV_APR0 characteristics are:

Purpose
For software compatibility, this register is present in the virtual CPU interface. However, in a virtualized system, it is not used when preserving and restoring state.

Usage constraints
Reading the content of this register and then writing the same values must not change any state because there is no requirement to preserve and restore state during a powerdown.

Configurations
Available in all configurations.

Attributes
See the register summary in B2.6 Virtual CPU interface register summary on page B2-357.

The Cortex-A32 processor implements the GICV_APR0 as an alias of GICH_APR0.
B2.8 VM CPU Interface Identification Register

The GICV_IIDR characteristics are:

**Purpose**
Provides information about the implementer and revision of the virtual CPU interface.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See the register summary in *B2.6 Virtual CPU interface register summary* on page B2-357.

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:20</td>
<td>ProductID</td>
<td>0x001 Cortex-A32 processor.</td>
</tr>
<tr>
<td>19:16</td>
<td>Architecture version</td>
<td>0x4 GICv4.</td>
</tr>
<tr>
<td>15:12</td>
<td>Revision</td>
<td>0x2 r1p0.</td>
</tr>
<tr>
<td>11:0</td>
<td>Implementer</td>
<td>0x43B Arm.</td>
</tr>
</tbody>
</table>

**Figure B2-3** GICV_IIDR bit assignments

ProductID, [31:20]
Identifies the product:
0x001 Cortex-A32 processor.

Architecture version, [19:16]
Identifies the architecture version of the GIC CPU Interface:
0x4 GICv4.

Revision, [15:12]
Identifies the revision number for the CPU interface:
0x2 r1p0.

Implementer, [11:0]
Contains the JEP106 code of the company that implements the CPU interface:
0x43B Arm.
Chapter B3

Generic Timer registers

This chapter describes the Generic Timer registers.

It contains the following section:

• B3.1 AArch32 Generic Timer register summary on page B3-362.
### B3.1 AArch32 Generic Timer register summary

The following table shows the AArch32 Generic Timer registers.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for information about these registers.

<table>
<thead>
<tr>
<th>Name</th>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTFRQ</td>
<td>c14</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Counter-timer Frequency register</td>
</tr>
<tr>
<td>CNTPCT</td>
<td>-</td>
<td>0</td>
<td>c14</td>
<td>-</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Kernel Control register</td>
</tr>
<tr>
<td>CNTKCTL</td>
<td>c14</td>
<td>0</td>
<td>c1</td>
<td>0</td>
<td>-</td>
<td>32-bit</td>
<td>Counter-timer Physical Count register</td>
</tr>
<tr>
<td>CNTP_TV_AL</td>
<td>c2</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Counter-timer Physical Timer Value register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTP_CTL</td>
<td>1</td>
<td>-</td>
<td>32-bit</td>
<td>Counter-timer Physical Timer Control register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTV_TV_AL</td>
<td>c3</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Counter-timer Virtual Timer Value register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTV_CTL</td>
<td>1</td>
<td>-</td>
<td>32-bit</td>
<td>Counter-timer Virtual Timer Control register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTVCT</td>
<td>-</td>
<td>1</td>
<td>c14</td>
<td>-</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Virtual Count register</td>
</tr>
<tr>
<td>CNTP_CVAL</td>
<td>2</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Physical Timer Compare Value register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTV_CVAL</td>
<td>3</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Virtual Timer Compare Value register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTVOFF</td>
<td>4</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Virtual Offset register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTHCTL</td>
<td>c14</td>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>-</td>
<td>32-bit</td>
<td>Counter-timer Hyp Control register</td>
</tr>
<tr>
<td>CNTHP_TV_AL</td>
<td>c2</td>
<td>0</td>
<td>UNK</td>
<td>32-bit</td>
<td>Counter-timer Hyp Physical Timer Value register</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTHP_CTL</td>
<td>1</td>
<td>-</td>
<td>32-bit</td>
<td>Counter-timer Hyp Physical Timer Control register</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNTHP_CVAL</td>
<td>-</td>
<td>6</td>
<td>c14</td>
<td>-</td>
<td>UNK</td>
<td>64-bit</td>
<td>Counter-timer Hyp Physical Timer Compare Value register</td>
</tr>
</tbody>
</table>
Part C
Debug
Chapter C1
Debug

This chapter describes the debug features of the processor.

It contains the following sections:

• C1.1 About debug methods on page C1-366.
• C1.2 Debug access on page C1-367.
• C1.3 Effects of resets on debug registers on page C1-368.
• C1.4 External access permissions to debug registers on page C1-369.
• C1.5 Debug events on page C1-370.
• C1.6 Debug memory map on page C1-371.
• C1.7 Debug signals on page C1-373.
• C1.8 Changing the authentication signals for debug on page C1-374.
C1.1 About debug methods

The processor is part of a debug system and supports both self-hosted and external debug.

The following figure shows a typical external debug system.

![Debug System Diagram](image)

**Figure C1-1 External debug system**

**Debug host**

A computer, for example a personal computer, that is running a software debugger such as the DS-5 Debugger. With the debug host, you can issue high-level commands, such as setting a breakpoint at a certain location or examining the contents of a memory address.

**Protocol converter**

The debug host sends messages to the debug target using an interface such as Ethernet. However, the debug target typically implements a different interface protocol. A device such as DSTREAM is required to convert between the two protocols.

**Debug target**

The lowest level of the system implements system support for the protocol converter to access the debug unit using the Advanced Peripheral Bus (APB) slave interface. An example of a debug target is a development system with a test chip or a silicon part with a processor.

**Debug unit**

Helps debugging software that is running on the processor:

- Hardware systems that are based on the processor.
- Operating systems.
- Application software.

With the debug unit, you can:

- Stop program execution.
- Examine and alter process and coprocessor state.
- Examine and alter memory and the state of the input or output peripherals.
- Restart the processor.

For self-hosted debug, the debug target runs additional debug monitor software that runs on the Cortex-A32 processor itself. This way, it does not require expensive interface hardware to connect a second host computer.

**Related information**

*C1.2 Debug access* on page C1-367
C1.2 Debug access

The processor implements the Armv8 Debug architecture and debug events. Accessing system registers allows the processor to access certain debug registers directly. The external debug interface enables both external and self-hosted debug agents to access debug registers.

The partitioning of debug register access is as follows:

**Debug registers**
Access is based on the system registers and is memory-mapped. You can access the debug register map using the APB slave port.

**PMU**
Access is based on the system registers and is memory-mapped. You can access the performance monitor registers using the APB slave port.

**ETM**
Access is memory-mapped.

**CTI**
Access is based on the debug registers and is memory-mapped.

![Figure C1-2 External debug interface](image)

**Related information**

*Chapter C4 CTI on page C4-393*

*Appendix A Signal Descriptions on page Appx-A-617*
C1.3 Effects of resets on debug registers

Some of the processor reset signals affect the debug registers.

nCPUPRESET

Cold reset that covers reset of the processor logic and the integrated debug functionality.

The signal initializes the processor logic, including the debug, Embedded Trace Macrocell (ETM) trace unit, breakpoint, watchpoint logic, and performance monitors logic.

nCORERESET

Warm reset that covers reset of the processor logic.

The signal resets some of the debug and performance monitor logic.

nPRESETDBG

External debug reset that covers the resetting of the external debug interface and has no impact on the processor functionality.

The signal initializes the shared debug APB, Cross Trigger Interface (CTI), and Cross Trigger Matrix (CTM) logic.

Related information
A3.3 Resets on page A3-48
Appendix A Signal Descriptions on page Appx-A-617
C1.4 External access permissions to debug registers

External access permission to the debug registers is subject to the conditions at the time of the access. The following table describes the processor response to accesses to the debug registers.

Table C1-1 Conditions on external register access to debug registers

<table>
<thead>
<tr>
<th>Name</th>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>EDPRSR.PU is 0</td>
<td>The processor power domain is completely off or in a low-power state in which the processor power domain registers cannot be accessed. If debug power is off, then all external debug and memory-mapped register accesses return an error.</td>
</tr>
<tr>
<td>DLK</td>
<td>EDPRSR.DLK is 1</td>
<td>OS Double Lock is locked.</td>
</tr>
<tr>
<td>OSLK</td>
<td>OSLR_EL1.OSLK is 1</td>
<td>OS Lock is locked.</td>
</tr>
<tr>
<td>EDAD</td>
<td>AllowExternalDebugAccess() == FALSE</td>
<td>External debug access is disabled. When an error is returned because of an EDAD condition code, the highest priority error condition, EDPRSR.SDAD is set to 1. Otherwise SDAD is unchanged.</td>
</tr>
<tr>
<td>SLK</td>
<td>Memory-mapped interface only</td>
<td>Software lock is locked. For the external debug interface, ignore this column.</td>
</tr>
<tr>
<td>Default</td>
<td></td>
<td>None of the conditions apply, normal access.</td>
</tr>
</tbody>
</table>

The following table shows an example of external register condition codes for access to a debug register. To determine the access permission for the register, scan the columns from left to right. Stop at the first column a condition is true, the entry gives the access permission of the register and scanning stops.

Table C1-2 Code example for the conditions on external register access to debug registers

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>RO/WI</td>
<td>RO</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
C1.5 Debug events

A debug event can be either a software debug event or a halting debug event. A core responds to a debug event in one of the following ways: ignores it, takes a debug exception, or enters debug state.

In the processor, watchpoint debug events are always synchronous. Memory hint instructions and cache clean operations, except DC ZVA, DC IVAC, and DCIMVAC, do not generate watchpoint debug events. Store exclusive instructions generate a watchpoint debug event even when the check for the control of exclusive monitor fails. For watchpoint debug events, except those resulting from cache maintenance operations, the value reported in DFAR is guaranteed to be no lower than the address of the watchpointed location rounded down to a multiple of 16 bytes.

The powerup reset signal, nCPUPORESET, sets the Debug OS Lock. For the debug events and debug register accesses to operate normally, the Debug OS Lock must be cleared.

Related information
A3.3 Resets on page A3-48
A.4 Reset signals on page Appx-A-621
Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile
C1.6 Debug memory map

The basic memory map supports up to four cores in the cluster. You can configure the mapping as a v8 or as a v7 Debug memory map.

The following table shows the address mapping for the debug APB components when you configure them for a v8 Debug memory map. Each component in the table requires 4KB and uses the bottom 4KB of each 64KB region. The remaining 60KB of each region is reserved. The table indicates the mapped component if it is present, otherwise the field is reserved.

<table>
<thead>
<tr>
<th>Address offset [21:0]</th>
<th>Mapped to</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000000 - 0x000FFF</td>
<td>APB ROM table for the processor</td>
</tr>
<tr>
<td>0x010000 - 0x010FFF</td>
<td>Core 0 Debug</td>
</tr>
<tr>
<td>0x020000 - 0x020FFF</td>
<td>Core 0 CTI</td>
</tr>
<tr>
<td>0x030000 - 0x030FFF</td>
<td>Core 0 PMU</td>
</tr>
<tr>
<td>0x040000 - 0x040FFF</td>
<td>Core 0 Trace</td>
</tr>
<tr>
<td>0x041000 - 0x10FFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x110000 - 0x110FFF</td>
<td>Core 1 Debug</td>
</tr>
<tr>
<td>0x120000 - 0x120FFF</td>
<td>Core 1 CTI</td>
</tr>
<tr>
<td>0x130000 - 0x130FFF</td>
<td>Core 1 PMU</td>
</tr>
<tr>
<td>0x140000 - 0x140FFF</td>
<td>Core 1 Trace</td>
</tr>
<tr>
<td>0x141000 - 0x20FFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x210000 - 0x210FFF</td>
<td>Core 2 Debug</td>
</tr>
<tr>
<td>0x220000 - 0x220FFF</td>
<td>Core 2 CTI</td>
</tr>
<tr>
<td>0x230000 - 0x230FFF</td>
<td>Core 2 PMU</td>
</tr>
<tr>
<td>0x240000 - 0x240FFF</td>
<td>Core 2 Trace</td>
</tr>
<tr>
<td>0x241000 - 0x30FFFF</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x310000 - 0x310FFF</td>
<td>Core 3 Debug</td>
</tr>
<tr>
<td>0x320000 - 0x320FFF</td>
<td>Core 3 CTI</td>
</tr>
<tr>
<td>0x330000 - 0x330FFF</td>
<td>Core 3 PMU</td>
</tr>
<tr>
<td>0x340000 - 0x340FFF</td>
<td>Core 3 Trace</td>
</tr>
<tr>
<td>0x341000 - 0x3FFFFF</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The following table shows the address mapping for the debug components when you configure them for a v7 Debug memory map. The table indicates the mapped component if it is present, otherwise the field is reserved.
### Table C1-4 Address mapping for APB components in a v7 Debug memory map

<table>
<thead>
<tr>
<th>Address offset [21:0]</th>
<th>Mapped to</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000 - 0x0FFF</td>
<td>APB ROM table for the processor</td>
</tr>
<tr>
<td>0x01000 - 0x07FFF</td>
<td>Reserved for other debug components</td>
</tr>
<tr>
<td>0x08000 - 0x0FFFF</td>
<td>Reserved for future expansion</td>
</tr>
<tr>
<td>0x10000 - 0x10FFF</td>
<td>Core 0 Debug</td>
</tr>
<tr>
<td>0x11000 - 0x11FFF</td>
<td>Core 0 PMU</td>
</tr>
<tr>
<td>0x12000 - 0x12FFF</td>
<td>Core 1 Debug</td>
</tr>
<tr>
<td>0x13000 - 0x13FFF</td>
<td>Core 1 PMU</td>
</tr>
<tr>
<td>0x14000 - 0x14FFF</td>
<td>Core 2 Debug</td>
</tr>
<tr>
<td>0x15000 - 0x15FFF</td>
<td>Core 2 PMU</td>
</tr>
<tr>
<td>0x16000 - 0x16FFF</td>
<td>Core 3 Debug</td>
</tr>
<tr>
<td>0x17000 - 0x17FFF</td>
<td>Core 3 PMU</td>
</tr>
<tr>
<td>0x18000 - 0x18FFF</td>
<td>Core 0 CTI</td>
</tr>
<tr>
<td>0x19000 - 0x19FFF</td>
<td>Core 1 CTI</td>
</tr>
<tr>
<td>0x1A000 - 0x1AFFF</td>
<td>Core 2 CTI</td>
</tr>
<tr>
<td>0x1B000 - 0x1BFFF</td>
<td>Core 3 CTI</td>
</tr>
<tr>
<td>0x1C000 - 0x1FFFF</td>
<td>Core 0 Trace</td>
</tr>
<tr>
<td>0x1D000 - 0x1DFFF</td>
<td>Core 1 Trace</td>
</tr>
<tr>
<td>0x1E000 - 0x1EFFF</td>
<td>Core 2 Trace</td>
</tr>
<tr>
<td>0x1F000 - 0x1FFFF</td>
<td>Core 3 Trace</td>
</tr>
</tbody>
</table>
C1.7 Debug signals

The DBGPWRDUP and DBGL1RSTDISABLE signals are subject to particular rules.

You must set the DBGPWRDUP signal LOW before removing power to the processor domain. After power is restored to the processor domain, the DBGPWRDUP signal must be asserted HIGH. The EDPRSR.PU bit reflects the value of this DBGPWRDUP signal. DBGPWRDUP must be tied HIGH if the particular implementation does not support separate processor and SCU power domains.

When you set it HIGH, the DBGL1RSTDISABLE input signal disables the automatic, hardware-controlled invalidation with nCORERESET or nCPUPORESET of the L1 data cache after the processor is reset. You must use DBGL1RSTDISABLE only to debug a reset that an external watchdog triggered. This signal makes the contents of the L1 data cache from before the reset observable after the reset. If reset is asserted while an L1 data cache eviction or L1 data cache fetch is performed, the accuracy of those cache entries is not guaranteed. You must not use the DBGL1RSTDISABLE signal to disable the automatic, hardware controlled invalidation of the L1 data cache in normal processor powerup sequences. This is because there is no guarantee that the L1 data cache invalidation sequence is synchronized to the duplicate L1 tags in the SCU. The DBGL1RSTDISABLE signal applies to all cores in the cluster. Each core samples the signal when nCORERESET or nCPUPORESET is asserted. If the functionality offered by the DBGL1RSTDISABLE input signal is not required, the input must be tied to LOW.

Related information

A.14 Debug signals on page Appx-A-641
C1.8 Changing the authentication signals for debug

The NIDEN, DBGEN, SPIDEN, and SPNIDEN input signals are either tied off to some fixed value or controlled by some external device. If software running on the processor has control over an external device that drives the authentication signals, it must change the signal value using the specified procedure.

Procedure

1. Execute an implementation-specific sequence of instructions to change the signal value. For example, a single STR instruction might write certain values to a control register in a system peripheral.
2. If step 1 on page C1-374 involves any memory operation, issue a DSB instruction.
3. Issue an ISB instruction or exception entry or exception return.
4. Poll the DBGAUTHSTATUS_EL1 register to check whether the processor has already detected the changed value of these signals. This check is required because the system might not issue the signal change to the processor until several cycles after the DSB instruction completes.

Next Steps

Software cannot perform debug or analysis operations that depend on the new value of the authentication signals until this procedure is complete. The same rules apply when the debugger has control of the processor through the Instruction Transfer Register, EDITR, while in debug state. You can determine the relevant combinations of the DBGEN, NIDEN, SPIDEN, and SPNIDEN values by polling DBGAUTHSTATUS_EL1.

Related information

A.14 Debug signals on page Appx-A-641
This chapter describes the *Performance Monitor Unit* (PMU) of the processor.

It contains the following sections:

- C2.1 About the PMU on page C2-376.
- C2.2 External register access permissions to the PMU registers on page C2-377.
- C2.3 Performance monitoring events on page C2-378.
- C2.4 PMU interrupts on page C2-382.
- C2.5 Exporting PMU events on page C2-383.
C2.1 About the PMU

The processor includes performance monitors that enable you to gather various statistics on the operation of the processor and its memory system during runtime. They provide useful information that you can use when debugging or profiling code.

The PMU provides six counters. Each counter can count any of the events available in the processor. The absolute counts that the PMU records might vary because of pipeline effects. This variability only has an impact on the operation of the PMU when a counter is enabled for a short time.

![PMU block diagram](image)

**Event interface**

Events from all other units from across the design are provided to the PMU.

**System register and APB interface**

You can program the PMU registers using the system registers or external APB interface.

**Counters**

The PMU has six 32-bit performance counters and one 64-bit cycle counter. The performance counters increment when they are enabled based on events.

**PMU register interfaces**

The processor supports access to the performance monitor registers from the internal system register interface or external debug interface.

**Related information**

- C2.3 Performance monitoring events on page C2-378
- C4.2 Cross-trigger inputs and outputs on page C4-395
C2.2 External register access permissions to the PMU registers

External access permission to the PMU registers is subject to conditions at the time of the access. The following table describes the processor response to accesses through the external debug interface.

<table>
<thead>
<tr>
<th>Name</th>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>EDPRSR.PU is 0</td>
<td>Processor power domain is completely off or in a low-power state where the processor power domain registers cannot be accessed.</td>
</tr>
<tr>
<td>DLK</td>
<td>EDPRSR.DLK is 1</td>
<td>OS Double Lock is locked.</td>
</tr>
<tr>
<td>OSLK</td>
<td>OSLR_EL1.OSLK is 1</td>
<td>OS Lock is locked.</td>
</tr>
<tr>
<td>EPMAD</td>
<td>AllowExternalPMUAccess() == FALSE</td>
<td>External performance monitors access is disabled. When an error is returned because of an EPMAD condition code, and it is the highest priority error condition, EDPRSR.SPMAD is set to 1. Otherwise SPMAD is unchanged.</td>
</tr>
<tr>
<td>SLK</td>
<td>Memory-mapped interface only</td>
<td>Software lock is locked. For the external debug interface, ignore this column.</td>
</tr>
<tr>
<td>Default</td>
<td>-</td>
<td>None of the conditions apply, normal access.</td>
</tr>
</tbody>
</table>

To determine the access permission for the register, scan the columns from left to right in the register usage constraints table. An example is shown in Table C2-2 Example for external register condition code on page C2-377. Stop at the first column in which the condition is true. The entry gives the register access permission and scanning stops.

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO/WI</td>
<td>RO</td>
</tr>
</tbody>
</table>
C2.3 Performance monitoring events

The PMU monitors events in the processor and uses reference numbers for significant ones.

The following table shows the bit position of each event on the event bus. Event reference numbers that are not listed are reserved.

<table>
<thead>
<tr>
<th>Number</th>
<th>Event mnemonic</th>
<th>PMU event bus to external</th>
<th>PMU event bus to trace</th>
<th>Event name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>SW_INCR</td>
<td>-</td>
<td>-</td>
<td>Software increment. The register is incremented only on writes to the Software Increment Register.</td>
</tr>
<tr>
<td>0x01</td>
<td>L1I_CACHE_REFILL</td>
<td>[0]</td>
<td>[0]</td>
<td>L1 Instruction cache refill.</td>
</tr>
<tr>
<td>0x02</td>
<td>L1I_TLB_REFILL</td>
<td>[1]</td>
<td>[1]</td>
<td>L1 Instruction TLB refill.</td>
</tr>
<tr>
<td>0x03</td>
<td>L1D_CACHE_REFILL</td>
<td>[2]</td>
<td>[2]</td>
<td>L1 Data cache refill.</td>
</tr>
<tr>
<td>0x04</td>
<td>L1D_CACHE</td>
<td>[3]</td>
<td>[3]</td>
<td>L1 Data cache access.</td>
</tr>
<tr>
<td>0x05</td>
<td>L1D_TLB_REFILL</td>
<td>[4]</td>
<td>[4]</td>
<td>L1 Data TLB refill.</td>
</tr>
<tr>
<td>0x06</td>
<td>LD_RETIRED</td>
<td>[5]</td>
<td>[5]</td>
<td>Instruction that is architecturally executed, condition check pass - load.</td>
</tr>
<tr>
<td>0x07</td>
<td>ST_RETIRED</td>
<td>[6]</td>
<td>[6]</td>
<td>Instruction that is architecturally executed, condition check pass - store.</td>
</tr>
<tr>
<td>0x08</td>
<td>INST_RETIRED</td>
<td>[7]</td>
<td>[7]</td>
<td>Instruction that is architecturally executed.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[8]</td>
<td>[8]</td>
<td>Two instructions are architecturally executed. Counts every cycle in which two instructions are architecturally retired. Event 0x08, INST_RETIRED, always counts when this event counts.</td>
</tr>
<tr>
<td>0x09</td>
<td>EXC_TAKEN</td>
<td>[9]</td>
<td>[9]</td>
<td>Exception taken.</td>
</tr>
<tr>
<td>0x0A</td>
<td>EXC_RETURN</td>
<td>[10]</td>
<td>[10]</td>
<td>Exception return.</td>
</tr>
<tr>
<td>0x0C</td>
<td>PC_WRITE_RETIRED</td>
<td>[12]</td>
<td>[12]</td>
<td>Instruction that is architecturally executed, condition check pass, software change of the PC.</td>
</tr>
<tr>
<td>0x0D</td>
<td>BR_IMMED_RETIRED</td>
<td>[13]</td>
<td>[13]</td>
<td>Instruction that is architecturally executed, immediate branch.</td>
</tr>
<tr>
<td>0x0E</td>
<td>BR_RETURN_RETIRED</td>
<td>-</td>
<td>-</td>
<td>Instruction that is architecturally executed, condition code check pass, procedure return.</td>
</tr>
<tr>
<td>0x0F</td>
<td>UNALIGNED_LDST_RETIRED</td>
<td>[14]</td>
<td>[14]</td>
<td>Instruction that is architecturally executed, condition check pass, unaligned load or store.</td>
</tr>
<tr>
<td>0x10</td>
<td>BR_MIS_PRED</td>
<td>[15]</td>
<td>[15]</td>
<td>Mispredicted or not predicted branch that is speculatively executed.</td>
</tr>
<tr>
<td>0x11</td>
<td>CPU_CYCLES</td>
<td>-</td>
<td>-</td>
<td>Cycle.</td>
</tr>
<tr>
<td>0x12</td>
<td>BR_PRED</td>
<td>[16]</td>
<td>[16]</td>
<td>Predictable branch that is speculatively executed.</td>
</tr>
<tr>
<td>0x13</td>
<td>MEM_ACCESS</td>
<td>[17]</td>
<td>[17]</td>
<td>Data memory access.</td>
</tr>
<tr>
<td>Number</td>
<td>Event mnemonic</td>
<td>PMU event bus to external</td>
<td>PMU event bus to trace</td>
<td>Event name</td>
</tr>
<tr>
<td>-------</td>
<td>---------------</td>
<td>---------------------------</td>
<td>------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>0x14</td>
<td>L1I_CACHE</td>
<td>[18]</td>
<td>[18]</td>
<td>L1 Instruction cache access.</td>
</tr>
<tr>
<td>0x15</td>
<td>L1D_CACHE_WB</td>
<td>[19]</td>
<td>[19]</td>
<td>L1 Data cache writeback.</td>
</tr>
<tr>
<td>0x16</td>
<td>L2D_CACHE</td>
<td>[20]</td>
<td>[20]</td>
<td>L2 Data cache access.</td>
</tr>
<tr>
<td>0x17</td>
<td>L2D_CACHE_REFILL</td>
<td>[21]</td>
<td>[21]</td>
<td>L2 Data cache refill.</td>
</tr>
<tr>
<td>0x18</td>
<td>L2D_CACHE_WB</td>
<td>[22]</td>
<td>[22]</td>
<td>L2 Data cache write-back.</td>
</tr>
<tr>
<td>0x19</td>
<td>BUS_ACCESS</td>
<td>-</td>
<td>-</td>
<td>Bus access.</td>
</tr>
<tr>
<td>0x1A</td>
<td>MEMORY_ERROR</td>
<td>-</td>
<td>-</td>
<td>Local memory error.</td>
</tr>
<tr>
<td>0x1D</td>
<td>BUS_CYCLES</td>
<td>-</td>
<td>-</td>
<td>Bus cycle.</td>
</tr>
<tr>
<td>0x1E</td>
<td>CHAIN</td>
<td>-</td>
<td>-</td>
<td>Odd performance counter chain mode.</td>
</tr>
<tr>
<td>0x60</td>
<td>BUS_ACCESS_LD</td>
<td>-</td>
<td>-</td>
<td>Bus access - Read.</td>
</tr>
<tr>
<td>0x61</td>
<td>BUS_ACCESS_ST</td>
<td>-</td>
<td>-</td>
<td>Bus access - Write.</td>
</tr>
<tr>
<td>0x7A</td>
<td>BR_INDIRECT_SPEC</td>
<td>-</td>
<td>-</td>
<td>Branch that is speculatively executed - Indirect branch.</td>
</tr>
<tr>
<td>0x86</td>
<td>EXC_IRQ</td>
<td>-</td>
<td>-</td>
<td>Exception taken, IRQ.</td>
</tr>
<tr>
<td>0x87</td>
<td>EXC_FIQ</td>
<td>-</td>
<td>-</td>
<td>Exception taken, FIQ.</td>
</tr>
<tr>
<td>0xC0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>External memory request.</td>
</tr>
<tr>
<td>0xC1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Non-cacheable external memory request.</td>
</tr>
<tr>
<td>0xC2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Linefill because of prefetch.</td>
</tr>
<tr>
<td>0xC4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Entering read allocate mode.</td>
</tr>
<tr>
<td>0xC5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Read allocate mode.</td>
</tr>
<tr>
<td>0xC6</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Pre-decode error.</td>
</tr>
<tr>
<td>0xC7</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Data Write operation that stalls the pipeline because the store buffer is full.</td>
</tr>
<tr>
<td>0xC8</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>SCU Snooped data from another core for this core.</td>
</tr>
<tr>
<td>0xC9</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Conditional branch that is executed.</td>
</tr>
<tr>
<td>0xCA</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Indirect branch that is mispredicted.</td>
</tr>
<tr>
<td>0xCB</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Indirect branch that is mispredicted because of address miscompare.</td>
</tr>
<tr>
<td>0xCC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Conditional branch that is mispredicted.</td>
</tr>
<tr>
<td>0xD0</td>
<td>-</td>
<td>[23]</td>
<td>[23]</td>
<td>L1 Instruction Cache (data or tag) memory error.</td>
</tr>
<tr>
<td>0xD1</td>
<td>-</td>
<td>[24]</td>
<td>[24]</td>
<td>L1 Data Cache (data, tag, or dirty) memory error, correctable or non-correctable.</td>
</tr>
<tr>
<td>0xD2</td>
<td>-</td>
<td>[25]</td>
<td>[25]</td>
<td>TLB memory error.</td>
</tr>
</tbody>
</table>
### Table C2-3 Performance monitoring events (continued)

<table>
<thead>
<tr>
<th>Number</th>
<th>Event mnemonic</th>
<th>PMU event bus to external</th>
<th>PMU event bus to trace</th>
<th>Event name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE0</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle that the DPU IQ is empty and that is not because of a recent micro-TLB miss, an instruction cache miss or a pre-decode error.</td>
</tr>
<tr>
<td>0xE1</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle the DPU IQ is empty and there is an instruction cache miss being processed.</td>
</tr>
<tr>
<td>0xE2</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle the DPU IQ is empty and there is an instruction micro-TLB miss being processed.</td>
</tr>
<tr>
<td>0xE3</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle the DPU IQ is empty and there is a pre-decode error being processed.</td>
</tr>
<tr>
<td>0xE4</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle there is an interlock that is not because of an Advanced SIMD or floating-point instruction, and not because of a load/store instruction waiting for data to calculate the address in the AGU. Stall cycles because of a stall in Wr, typically awaiting load data, are excluded.</td>
</tr>
<tr>
<td>0xE5</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle there is an interlock that is because of a load/store instruction waiting for data to calculate the address in the AGU. Stall cycles because of a stall in Wr, typically awaiting load data, are excluded.</td>
</tr>
<tr>
<td>0xE6</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle there is an interlock that is because of an Advanced SIMD or floating-point instruction. Stall cycles because of a stall in the Wr stage, typically awaiting load data, are excluded.</td>
</tr>
<tr>
<td>0xE7</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle there is a stall in the Wr stage because of a load miss.</td>
</tr>
<tr>
<td>0xE8</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Attributable Performance Impact Event. Counts every cycle there is a stall in the Wr stage because of a store.</td>
</tr>
<tr>
<td>Number</td>
<td>Event mnemonic</td>
<td>PMU event bus to external</td>
<td>PMU event bus to trace</td>
<td>Event name</td>
</tr>
<tr>
<td>--------</td>
<td>----------------</td>
<td>---------------------------</td>
<td>------------------------</td>
<td>------------</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>[26]</td>
<td>[26]</td>
<td>L2 (data or tag) memory error, correctable or non-correctable.</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>[27]</td>
<td>[27]</td>
<td>SCU snoop filter memory error, correctable or non-correctable.</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>[28]</td>
<td>-</td>
<td>Advanced SIMD and floating-point retention active.</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>[29]</td>
<td>-</td>
<td>Core retention active.</td>
</tr>
</tbody>
</table>
C2.4 PMU interrupts

The processor asserts the nPMUIRQ signal when an interrupt occurs that the PMU generated.

You can route this signal to an external interrupt controller for prioritization and masking. It is the only mechanism that signals this interrupt to the processor.

This interrupt is also driven as a trigger input to the CTI.

Related information
C4.2 Cross-trigger inputs and outputs on page C4-395
C2.5 Exporting PMU events

Some of the PMU events are exported to the ETM trace unit and the Cross Trigger Interface (CTI) to enable them to be monitored. Furthermore, the processor exports some PMU events on the PMUEVENT bus to external hardware.

Related information

Chapter C3 ETM on page C3-385
Chapter C4 CTI on page C4-393
Chapter C3
ETM

This chapter describes the *Embedded Trace Macrocell* (ETM) of the processor.

It contains the following sections:

- *C3.1 About the ETM* on page C3-386.
- *C3.2 Configuration options for the ETM unit and trace resources* on page C3-388.
- *C3.3 Resetting the ETM* on page C3-390.
- *C3.4 Programming and reading ETM trace unit registers* on page C3-391.
C3.1 About the ETM

The ETM trace unit is a build-time configuration option. This module performs real-time instruction flow tracing that complies with the ETM architecture. As a CoreSight component, it is part of the Arm real-time debug solution.

![ETM functional blocks](image)

**Filtering and triggering resources**
You can limit the amount of trace data that the ETM generates through filtering. For example, you can configure the ETM to generate trace only in a certain address range. More complicated filtering options, in the style of a logic analyzer, are also available.

The ETM trace unit can also generate a trigger signal to the Trace Capture Device to stop capturing trace.

**Processor interface**
Monitors the behavior of the processor and generates P0 elements that are executed instructions and exceptions that the ETM traces in program order.

**Trace generation**
Generates various trace packets that are based on P0 elements.

**FIFO**
The ETM generates trace in a highly compressed form. The FIFO can flatten trace bursts. When it becomes full, it signals overflow so that the trace generation logic does not generate any new trace until the FIFO becomes empty. The period without trace generation results in a gap in the trace in the debugger view.

**Trace out**
Trace from FIFO is output on the synchronous ATB interface.

**Syncbridge**
The ATB interface from the trace out block goes through an ATB synchronous bridge.

**Interaction with the Performance Monitoring Unit (PMU)**
The processor includes a PMU that enables counting events, such as cache misses, over a period. All PMU architectural events are available to the ETM trace unit through the extended input facility. The ETM trace unit uses four extended external input selectors to access the PMU events. Each selector can independently select one of the PMU events, which is then active for the cycles where the relevant events occur. Any ETM event register can access the selected event.

The processor supports only a memory-mapped interface to trace registers.
All trace register accesses through the external debug interface behave as if the processor power domain is powered down when debug double lock is set.

*Related information*

*Arm® CoreSight Architecture Specification*

*Chapter C2 PMU on page C2-375*
### C3.2 Configuration options for the ETM unit and trace resources

The ETM unit is configurable. The processor implements options for the ETM unit and its resources.

**Table C3-1 Configuration of trace generation**

<table>
<thead>
<tr>
<th>Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction address size in bytes</td>
<td>8</td>
</tr>
<tr>
<td>Data address size in bytes</td>
<td>0</td>
</tr>
<tr>
<td>Data value size in bytes</td>
<td>0</td>
</tr>
<tr>
<td>Virtual Machine ID size in bytes</td>
<td>1</td>
</tr>
<tr>
<td>Context ID size in bytes</td>
<td>4</td>
</tr>
<tr>
<td>Support for conditional instruction tracing</td>
<td>Not implemented</td>
</tr>
<tr>
<td>Support for tracing of data</td>
<td>Not implemented</td>
</tr>
<tr>
<td>Support for tracing of load and store instructions as P0 elements</td>
<td>Not implemented</td>
</tr>
<tr>
<td>Support for cycle counting in the instruction trace</td>
<td>Implemented</td>
</tr>
<tr>
<td>Support for branch broadcast tracing</td>
<td>Implemented</td>
</tr>
<tr>
<td>Exception levels implemented in Non-secure state</td>
<td>EL2, EL1, EL0</td>
</tr>
<tr>
<td>Exception levels implemented in Secure state</td>
<td>EL3, EL1, EL0</td>
</tr>
<tr>
<td>Number of events supported in the trace</td>
<td>4</td>
</tr>
<tr>
<td>Return stack support</td>
<td>Implemented</td>
</tr>
<tr>
<td>Tracing of SError exception support</td>
<td>Implemented</td>
</tr>
<tr>
<td>Instruction trace cycle counting minimum threshold</td>
<td>1</td>
</tr>
<tr>
<td>Size of Trace ID</td>
<td>7 bits</td>
</tr>
<tr>
<td>Synchronization period support</td>
<td>Read-write</td>
</tr>
<tr>
<td>Global timestamp size</td>
<td>64 bits</td>
</tr>
<tr>
<td>Number of cores available for tracing</td>
<td>1</td>
</tr>
<tr>
<td>ATB trigger support</td>
<td>Implemented</td>
</tr>
<tr>
<td>Low-power behavior override</td>
<td>Implemented</td>
</tr>
<tr>
<td>Stall control support</td>
<td>Implemented</td>
</tr>
<tr>
<td>Support for no overflows in the trace</td>
<td>Not implemented</td>
</tr>
</tbody>
</table>

**Table C3-2 Configuration of trace resources**

<table>
<thead>
<tr>
<th>Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of resource selection pairs implemented</td>
<td>8</td>
</tr>
<tr>
<td>Number of external input selectors implemented</td>
<td>4</td>
</tr>
<tr>
<td>Number of external inputs implemented</td>
<td>30, 4 CTI + 26 PMU</td>
</tr>
<tr>
<td>Number of counters implemented</td>
<td>2</td>
</tr>
<tr>
<td>Reduced function counter implemented</td>
<td>Not implemented</td>
</tr>
</tbody>
</table>
Table C3-2  Configuration of trace resources (continued)

<table>
<thead>
<tr>
<th>Description</th>
<th>Configuration</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of sequencer states implemented</td>
<td>4</td>
</tr>
<tr>
<td>Number of Virtual Machine ID comparators implemented</td>
<td>1</td>
</tr>
<tr>
<td>Number of Context ID comparators implemented</td>
<td>1</td>
</tr>
<tr>
<td>Number of address comparator pairs implemented</td>
<td>4</td>
</tr>
<tr>
<td>Number of single-shot comparator controls</td>
<td>1</td>
</tr>
<tr>
<td>Number of processor comparator inputs implemented</td>
<td>0</td>
</tr>
<tr>
<td>Data address comparisons implemented</td>
<td>Not implemented</td>
</tr>
<tr>
<td>Number of data value comparators implemented</td>
<td>0</td>
</tr>
</tbody>
</table>
C3.3  Resetting the ETM

The reset for the ETM trace unit is the same as a cold reset for the processor. If the ETM trace unit is reset, tracing stops until the ETM trace unit is reprogrammed and re-enabled.

A warm reset of the processor does not reset the ETM trace unit. Therefore it is possible to trace through warm processor reset. However, if the processor is reset using warm reset, the trace unit might not be able to trace the last few instructions before the reset.
C3.4 Programming and reading ETM trace unit registers

You program and read the ETM trace unit registers using the Debug APB interface.

The processor does not have to be in the debug state while you program the ETM trace unit registers.

When you are programming the ETM trace unit registers, you must enable all the changes at the same time. Otherwise if you reprogram the counter, it might start to count based on incorrect events before the correct setup is in place for the trigger condition.

To disable the ETM trace unit, use the TRCPRGCTRLR.EN bit.

![Diagram of programming ETM trace unit registers]

Figure C3-2 Programming ETM trace unit registers

Related information

C10.2 Programming Control Register on page C10-506
C10.3 Status Register on page C10-507
C3 ETM

C3.4 Programming and reading ETM trace unit registers
This chapter describes the cross-trigger components of the processor.

It contains the following sections:

- *C4.1 About the cross-trigger* on page C4-394.
- *C4.2 Cross-trigger inputs and outputs* on page C4-395.
C4.1 About the cross-trigger

The Cross-Trigger Interface (CTI) enables the debug logic, ETM trace unit, and PMU to interact with each other and with other CoreSight components. For example, you configure the CTI to generate an interrupt when the ETM trace unit trigger event occurs.

The single external cross-trigger channel interface of the processor connects to the CTI of each core through a Cross Trigger Matrix (CTM). Trigger inputs and trigger outputs connect debug components in the processor and CoreSight CTI blocks. The external CTM output is driven by the OR of the internal CTI outputs. Each internal CTI input is driven by the OR of the other internal CTI outputs and the external CTM input.

Figure C4-1  Cross-trigger components
C4.2 Cross-trigger inputs and outputs

Outputs from the PMU, the ETM, and the debug subsystem are cross-trigger inputs to the processor CTI. The CTI then generates cross-trigger outputs to other components in the SoC.

Table C4-1  Cross-trigger inputs

<table>
<thead>
<tr>
<th>CTI input</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>DBGTRIGGER, pulsed</td>
<td>Pulsed on entry to debug state.</td>
</tr>
<tr>
<td>1</td>
<td>PMUIRQ</td>
<td>PMU-generated interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This signal is the same as nPMUIRQ with inverted polarity.</td>
</tr>
<tr>
<td>2</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>EXTOUT[0]</td>
<td>Output from the ETM unit of Core&lt;N&gt;.</td>
</tr>
<tr>
<td>5</td>
<td>EXTOUT[1]</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>EXTOUT[2]</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>EXTOUT[3]</td>
<td></td>
</tr>
</tbody>
</table>

Table C4-2  Cross-trigger outputs

<table>
<thead>
<tr>
<th>CTI output</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>EDBGRQ</td>
<td>Causes the processor to enter debug state</td>
</tr>
<tr>
<td>1</td>
<td>DBGRESTART</td>
<td>Causes the processor to exit debug state</td>
</tr>
<tr>
<td>2</td>
<td>CTIIRQ</td>
<td>CTI interrupt</td>
</tr>
<tr>
<td>3</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>EXTIN[0]</td>
<td>ETM trace unit external input</td>
</tr>
<tr>
<td>5</td>
<td>EXTIN[1]</td>
<td>ETM trace unit external input</td>
</tr>
<tr>
<td>6</td>
<td>EXTIN[2]</td>
<td>ETM trace unit external input</td>
</tr>
<tr>
<td>7</td>
<td>EXTIN[3]</td>
<td>ETM trace unit external input</td>
</tr>
</tbody>
</table>
C.2 Cross-trigger inputs and outputs
Chapter C5
Direct access to internal memory

This chapter describes the direct access to internal memory that caches and TLBs use.

It contains the following sections:

- C5.1 About direct access to internal memory on page C5-398.
- C5.2 Encoding for tag and data in the L1 instruction cache on page C5-399.
- C5.3 Encoding for tag and data in the L1 data cache on page C5-400.
- C5.4 Encoding for the main TLB RAM on page C5-402.
- C5.5 Encoding for walk cache on page C5-406.
- C5.6 Encoding for IPA cache on page C5-407.
C5.1 About direct access to internal memory

System registers provide access to the internal memory that the caches and TLBs use. This functionality can be useful when investigating issues where the coherency between the data in the cache and data in system memory is broken.

The appropriate memory block and location are selected using write-only CP15 registers and the data is read from read-only CP15 registers. These operations are available only in EL3. In all other modes, executing the CP15 instruction results in an Undefined Instruction exception.

**Table C5-1 AArch32 CP15 registers used to access internal memory**

<table>
<thead>
<tr>
<th>Function</th>
<th>Access</th>
<th>CP15 operation</th>
<th>Rd Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Register 0</td>
<td>Read-only</td>
<td>MRC p15, 3, &lt;Rd&gt;, c15, c0, 0</td>
<td>Data</td>
</tr>
<tr>
<td>Data Register 1</td>
<td>Read-only</td>
<td>MRC p15, 3, &lt;Rd&gt;, c15, c0, 1</td>
<td>Data</td>
</tr>
<tr>
<td>Data Register 2</td>
<td>Read-only</td>
<td>MRC p15, 3, &lt;Rd&gt;, c15, c0, 2</td>
<td>Data</td>
</tr>
<tr>
<td>Data Register 3</td>
<td>Read-only</td>
<td>MRC p15, 3, &lt;Rd&gt;, c15, c0, 3</td>
<td>Data</td>
</tr>
<tr>
<td>Data Cache Tag Read Operation Register</td>
<td>Write-only</td>
<td>MCR p15, 3, &lt;Rd&gt;, c15, c2, 0</td>
<td>Set/Way</td>
</tr>
<tr>
<td>Instruction Cache Tag Read Operation Register</td>
<td>Write-only</td>
<td>MCR p15, 3, &lt;Rd&gt;, c15, c2, 1</td>
<td>Set/Way</td>
</tr>
<tr>
<td>Data Cache Data Read Operation Register</td>
<td>Write-only</td>
<td>MCR p15, 3, &lt;Rd&gt;, c15, c4, 0</td>
<td>Set/Way/Offset</td>
</tr>
<tr>
<td>Instruction Cache Data Read Operation Register</td>
<td>Write-only</td>
<td>MCR p15, 3, &lt;Rd&gt;, c15, c4, 1</td>
<td>Set/Way/Offset</td>
</tr>
<tr>
<td>TLB Data Read Operation Register</td>
<td>Write-only</td>
<td>MCR p15, 3, &lt;Rd&gt;, c15, c4, 2</td>
<td>Index/Way</td>
</tr>
</tbody>
</table>

**Related information**

*C5.4 Encoding for the main TLB RAM on page C5-402*
C5.2 Encoding for tag and data in the L1 instruction cache

The following table shows the format of the Instruction Cache Tag Read Operation Register and the Instruction Cache Data Read Operation Register.

The set-index range parameter (S) is determined by the following formula:
\[ S = \log_2(\text{size of the instruction cache in bytes} / 2) \]

<table>
<thead>
<tr>
<th>Bit field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>Cache Way</td>
</tr>
<tr>
<td>[30:S]</td>
<td>Unused</td>
</tr>
<tr>
<td>[S-1:6]</td>
<td>Set index</td>
</tr>
<tr>
<td>[5:2]</td>
<td>Line offset</td>
</tr>
<tr>
<td>[1:0]</td>
<td>Unused</td>
</tr>
</tbody>
</table>

The following table shows the format of the information in Data Register 0 following an Instruction Cache Tag Read Operation.

Table C5-3 Instruction cache tag data format

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>Unused.</td>
</tr>
<tr>
<td>[30:29]</td>
<td>Valid and set mode:</td>
</tr>
<tr>
<td>0b00</td>
<td>A32.</td>
</tr>
<tr>
<td>0b01</td>
<td>T32.</td>
</tr>
<tr>
<td>0b11</td>
<td>Invalid.</td>
</tr>
<tr>
<td>[28]</td>
<td>Non-secure state (NS).</td>
</tr>
<tr>
<td>[27:0]</td>
<td>Tag address.</td>
</tr>
</tbody>
</table>

The Instruction Cache Data Read Operation returns two entries from the cache in Data Register 0 and Data Register 1 corresponding to the 16-bit aligned offset in the cache line:

- **Data Register 0**: Bits[19:0] data from cache offset+ 0b00.
- **Data Register 1**: Bits[19:0] data from cache offset+ 0b10.

In A32 state these two fields combined always represent a single predecoded instruction. In T32 state, they can represent any combination of 16-bit and partial or full 32-bit instructions.
C5.3 Encoding for tag and data in the L1 data cache

The following table shows the format of the Data Cache Tag Read Operation Register and the Data Cache Data Read Operation Register. The Data Cache Tag Read Operation and the Data Cache Data Read Operation use the same encoding but the latter includes an additional field to locate the appropriate doubleword in the cache line.

The set-index range parameter (S) is determined by the following formula:

\[ S = \log_2(\text{size of the data cache in bytes}/4). \]

<table>
<thead>
<tr>
<th>Bit field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:30]</td>
<td>Cache way</td>
</tr>
<tr>
<td>[29:S]</td>
<td>Unused</td>
</tr>
<tr>
<td>[S-1:6]</td>
<td>Set index</td>
</tr>
<tr>
<td>[5:3]</td>
<td>Cache doubleword data offset (Data Cache Data Read Operation Register only)</td>
</tr>
<tr>
<td>[2:0]</td>
<td>Unused, RAZ.</td>
</tr>
</tbody>
</table>

The Data Cache Tag Read Operation returns 64 bits of data in Data Register 0 and Data Register 1. This includes the tag information, MOESI coherency state, outer attributes, and valid bit, for the selected cache line. The following table shows the format of the return value. The Cortex-A32 processor encodes the 4-bit MOESI coherency state across two fields of Data Register 0 and Data Register 1.

<table>
<thead>
<tr>
<th>Register</th>
<th>Bit field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Register 1</td>
<td>[31]</td>
<td>Parity bit if ECC is implemented, otherwise RES0.</td>
</tr>
<tr>
<td>Data Register 1</td>
<td>[30:29]</td>
<td>Partial MOESI State, from tag RAM. See Table C5-6 MOESI state on page C5-401.</td>
</tr>
<tr>
<td>Data Register 1</td>
<td>[28]</td>
<td>Non-secure state (NS).</td>
</tr>
<tr>
<td>Data Register 1</td>
<td>[27:0]</td>
<td>Tag Address [39:12].</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[31]</td>
<td>Tag Address [11].</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[30:5]</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[4]</td>
<td>Parity bit if ECC is implemented, otherwise RES0.</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[3]</td>
<td>Dirty copy bit if ECC is implemented, otherwise RES0.</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[2]</td>
<td>Outer Allocation Hint.</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[1]</td>
<td>Outer Shareability, from Dirty RAM.</td>
</tr>
<tr>
<td>Data Register 0</td>
<td>[0]</td>
<td>Partial MOESI state, from Dirty RAM. See Table C5-6 MOESI state on page C5-401.</td>
</tr>
</tbody>
</table>

The Data Cache Data Read Operation returns two entries from the cache in Data Register 0 and Data Register 1 corresponding to the 16-bit aligned offset in the cache line:

**Data Register 0** Bits[31:0] data from cache offset+ 0b0000.

**Data Register 1** Bits[31:0] data from cache offset+ 0b100.
<table>
<thead>
<tr>
<th>Tag RAM partial MOESI bits</th>
<th>Dirty RAM partial MOESI bits</th>
<th>MOESI state</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>x</td>
<td>Invalid (I)</td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td>SharedClean (S)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>SharedDirty (O)</td>
</tr>
<tr>
<td>1x</td>
<td>0</td>
<td>UniqueClean (E)</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>UniqueDirty (M)</td>
</tr>
</tbody>
</table>

**Related information**

*A5.2 Coherency between data caches with the MOESI protocol on page A5-75*
C5.4 Encoding for the main TLB RAM

The Cortex-A32 processor unified TLB is built from a 2-way set-associative RAM based structure. To read the individual entries into the data registers, software must write to the TLB Data Read Operation Register.

The following table shows the format of the TLB Data Read Operation Register.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>Unused</td>
</tr>
<tr>
<td>[30]</td>
<td>TLB way</td>
</tr>
<tr>
<td>[29:9]</td>
<td>Unused</td>
</tr>
<tr>
<td>[8:0]</td>
<td>TLB index</td>
</tr>
</tbody>
</table>

- 0-255  Main TLB RAM
- 256-287 Walk cache RAM
- 288-319 IPA cache RAM
- 320-511 Unused

The TLB Read Data Operation returns the selected entry in Data Register 0-3. The entry uses a 116-bit encoding when parity is enabled and a 113-bit encoding when parity is disabled.

- **Data Register 0[31:0]**  TLB Descriptor[31:0].
- **Data Register 1[31:0]**  TLB Descriptor[63:32].
- **Data Register 2[31:0]**  TLB Descriptor[95:64].
- **Data Register 3[20:0]**  TLB Descriptor[115:96].

The following table shows the data fields in the TLB descriptor.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[115:113]</td>
<td>Parity</td>
<td>If CPU cache protection is not implemented, these bits are absent.</td>
</tr>
</tbody>
</table>
| [112:111] | S2 Level | The stage 2 level that gave this translation:  
0b00  No stage 2 translation performed.  
0b01  Level 1.  
0b10  Level 2.  
0b11  Level 3. |
| [110:108] | S1 Size | The stage 1 size that gave this translation.  
VMSA 8-32 Short-descriptor translation table format:  
0b000  4KB.  
0b010  64KB.  
0b011  1MB.  
0b101  16MB. |
<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[107:104]</td>
<td>Domain</td>
<td>In VMSAv7 format, indicates one of sixteen memory regions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In non-VMSAv7 formats:&lt;br&gt;• Domain[0] stores the contiguous bit information.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Domain[1] stores the page size MSB for the combined page size.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Domain[2] stores the page size MSB for the stage 1 page size.</td>
</tr>
<tr>
<td>[103:96]</td>
<td>Memory Type and shareability</td>
<td>See <a href="#">TLB encoding for memory types and shareability</a>.</td>
</tr>
<tr>
<td>[95]</td>
<td>XS2</td>
<td>Stage2 executable permissions.</td>
</tr>
<tr>
<td>[94]</td>
<td>XS1Nonusr</td>
<td>Non user mode executable permissions.</td>
</tr>
<tr>
<td>[93]</td>
<td>XS1Usr</td>
<td>User mode executable permissions.</td>
</tr>
<tr>
<td>[92-65]</td>
<td>PA</td>
<td>Physical Address.</td>
</tr>
<tr>
<td>[64]</td>
<td>NS, descriptor</td>
<td>Security state allocated to memory region.</td>
</tr>
<tr>
<td>[61:59]</td>
<td>AP or HYP</td>
<td>Access permissions from stage-1 translation, or select EL2 or flag.</td>
</tr>
<tr>
<td>[58]</td>
<td>nG</td>
<td>Not global.</td>
</tr>
<tr>
<td>[57:55]</td>
<td>Size</td>
<td>This field shows the encoding for the combined page size for stage 1 and stage 2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VMSAv8-32 Short-descriptor translation table format:&lt;br&gt;0b000  4KB. &lt;br&gt;0b010  64KB. &lt;br&gt;0b100  1MB. &lt;br&gt;0b110  16MB.</td>
</tr>
<tr>
<td>[54:39]</td>
<td>ASID</td>
<td>Address Space Identifier.</td>
</tr>
<tr>
<td>[38:31]</td>
<td>VMID</td>
<td>Virtual Machine Identifier.</td>
</tr>
<tr>
<td>[30]</td>
<td>NS (walk)</td>
<td>Security state that the entry was fetched in.</td>
</tr>
<tr>
<td>[29:2]</td>
<td>VA</td>
<td>Virtual Address.</td>
</tr>
<tr>
<td>[0]</td>
<td>Valid</td>
<td>Valid bit:&lt;br&gt;0 Entry does not contain valid data. &lt;br&gt;1 Entry contains valid data.</td>
</tr>
</tbody>
</table>

The following table shows the main TLB memory types and shareability.
Table C5-9 TLB encoding for memory types and shareability

<table>
<thead>
<tr>
<th>Bits</th>
<th>Memory type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7]</td>
<td>Device</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WB</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer NC</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Coherent, Inner WB and Outer WB</td>
<td>1</td>
</tr>
<tr>
<td>[6]</td>
<td>Device</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer NC</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WT</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Coherent, Inner WB and Outer WB</td>
<td>Transience:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
</tr>
<tr>
<td>[5:4]</td>
<td>Device</td>
<td>Stage 1 (Non-device) overridden by stage 2 (Device)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WB</td>
<td>Inner type:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer NC</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WT</td>
<td>Inner type:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>Coherent, Inner WB and Outer WB</td>
<td>Inner allocation hint:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
</tr>
</tbody>
</table>
Table C5-9  TLB encoding for memory types and shareability (continued)

<table>
<thead>
<tr>
<th>Bits</th>
<th>Memory type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[3:2]</td>
<td>Device</td>
<td>Device type:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 nGnRnE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 nGnRE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 nGRE.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 GRE.</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WB</td>
<td>Outer allocation hint:</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WT</td>
<td>00 NA.</td>
</tr>
<tr>
<td></td>
<td>Coherent, Inner WB and Outer WB</td>
<td>01 WA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 RA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 WRA.</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer NC</td>
<td>Inner type:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>00 NC.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>01 WB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 WT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11 Unused.</td>
</tr>
<tr>
<td>[1:0]</td>
<td>Device</td>
<td>Shareability:</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WB</td>
<td>00 Non-shareable.</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer NC</td>
<td>01 Unused.</td>
</tr>
<tr>
<td></td>
<td>Non-coherent, Outer WT</td>
<td>10 Outer shareable.</td>
</tr>
<tr>
<td></td>
<td>Coherent, Inner WB and Outer WB</td>
<td>11 Inner shareable.</td>
</tr>
</tbody>
</table>

Related information

*C5.5 Encoding for walk cache* on page C5-406
*C5.6 Encoding for IPA cache* on page C5-407
*C5.1 About direct access to internal memory* on page C5-398
## C5.5 Encoding for walk cache

The following table shows the data fields in the walk cache descriptor.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[115:113]</td>
<td>Parity bits</td>
<td>If CPU cache protection is not implemented, these bits are absent.</td>
</tr>
<tr>
<td>[112:83]</td>
<td>PA</td>
<td>Physical Address of the second, last, translation level.</td>
</tr>
<tr>
<td>[82:60]</td>
<td>VA</td>
<td>Virtual address.</td>
</tr>
<tr>
<td>[59]</td>
<td>VA sign</td>
<td>Virtual address sign bit.</td>
</tr>
<tr>
<td>[58:55]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[54:39]</td>
<td>ASID</td>
<td>Address Space Identifier.</td>
</tr>
<tr>
<td>[38:31]</td>
<td>VMID</td>
<td>Virtual Machine Identifier.</td>
</tr>
<tr>
<td>[30]</td>
<td>NS, walk</td>
<td>Security state that the entry was fetched in.</td>
</tr>
<tr>
<td>[29:23]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[22:19]</td>
<td>Domain</td>
<td>Valid only if the entry was fetched in VMSAv7 format.</td>
</tr>
<tr>
<td>[18:16]</td>
<td>Entry size</td>
<td>Memory size to which entry maps:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b100  1MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b101  2MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b010  8MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b110, 0b011  32MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b001  128MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b111  512MB.</td>
</tr>
<tr>
<td>[15]</td>
<td>NSTable</td>
<td>Combined NSTable bits from first and second-level stage 1 tables or NS descriptor (VMSA).</td>
</tr>
<tr>
<td>[14]</td>
<td>PXNTable</td>
<td>Combined PXNTable bits from stage 1 descriptors up to last level.</td>
</tr>
<tr>
<td>[13]</td>
<td>XNTable</td>
<td>Combined XNTable bit from stage 1 descriptors up to last level.</td>
</tr>
<tr>
<td>[12:11]</td>
<td>APTable</td>
<td>Combined APTable bits from stage 1 descriptors up to last level.</td>
</tr>
<tr>
<td>[10]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[9]</td>
<td>EL2</td>
<td>Set if the entry was fetched in EL2 mode.</td>
</tr>
<tr>
<td>[8:1]</td>
<td>Attrs</td>
<td>Physical attributes of the final level stage 1 table.</td>
</tr>
<tr>
<td>[0]</td>
<td>Valid</td>
<td>Valid bit:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Entry does not contain valid data.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Entry contains valid data.</td>
</tr>
</tbody>
</table>
### C5.6 Encoding for IPA cache

The following table shows the data fields in the IPA cache descriptor.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[115:113]</td>
<td>Parity bits</td>
<td>If CPU cache protection is not implemented, these bits are absent.</td>
</tr>
<tr>
<td>[112:85]</td>
<td>PA</td>
<td>Physical address.</td>
</tr>
<tr>
<td>[84:62]</td>
<td>IPA</td>
<td>Unused lower bits, page size dependent, must be zero.</td>
</tr>
<tr>
<td>[61:59]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[58:55]</td>
<td>Size</td>
<td>Stage 2 page size. The values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0001 4KB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b1001 16KB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0011 64KB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0101 2MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b1011 32MB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0111 512MB.</td>
</tr>
<tr>
<td>[54:39]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[38:31]</td>
<td>VMID</td>
<td>Virtual Machine Identifier.</td>
</tr>
<tr>
<td>[30:12]</td>
<td>-</td>
<td>Reserved, must be zero.</td>
</tr>
<tr>
<td>[11:10]</td>
<td>Entry granule</td>
<td>The values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b00 4KB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b10 16KB.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b01 64KB.</td>
</tr>
<tr>
<td>[4:3]</td>
<td>HAP</td>
<td>Hypervisor access permissions.</td>
</tr>
<tr>
<td>[0]</td>
<td>Valid</td>
<td>The entry contains valid data.</td>
</tr>
</tbody>
</table>
C5 Direct access to internal memory
C5.6 Encoding for IPA cache
Chapter C6
AArch32 debug registers

This chapter describes the debug registers in the AArch32 execution state and shows examples of how to use them.

It contains the following sections:

• C6.1 AArch32 debug register summary on page C6-410.
• C6.2 Debug Breakpoint Control Registers on page C6-412.
• C6.3 Debug Watchpoint Control Registers on page C6-415.
• C6.4 Debug ID Register on page C6-418.
• C6.5 Debug Device ID Register on page C6-420.
• C6.6 Debug Device ID Register 1 on page C6-422.
C6.1 AArch32 debug register summary

This section summarizes the 32-bit and 64-bit debug control registers that are accessible in the AArch32 Execution state from the internal CP14 interface.

These registers, listed in the following table, are accessed by the MCR and MRC instructions in the order of CRn, op2, CRm, Op1 or MCRR and MRRC instructions in the order of CRm, Op1. For those registers not described in this chapter, see the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile.

See the C7.1 Memory-mapped debug register summary on page C7-424 for a complete list of registers accessible from the external debug interface.

Table C6-1 AArch32 debug register summary

<table>
<thead>
<tr>
<th>CRn</th>
<th>Op2</th>
<th>CRm</th>
<th>Op1</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c0</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>DBGIDDR</td>
<td>RO</td>
<td>C6.4 Debug ID Register on page C6-418</td>
</tr>
<tr>
<td>c0</td>
<td>0</td>
<td>c1</td>
<td>0</td>
<td>DBGDSCrint</td>
<td>RO</td>
<td>Debug Status and Control Register, Internal View</td>
</tr>
<tr>
<td>c0</td>
<td>0</td>
<td>c2</td>
<td>0</td>
<td>DBGDCCINT</td>
<td>RW</td>
<td>Debug Comms Channel Interrupt Enable Register</td>
</tr>
<tr>
<td>c0</td>
<td>0</td>
<td>c5</td>
<td>0</td>
<td>DBGDTRTXint</td>
<td>WO</td>
<td>Debug Data Transfer Register, Transmit, Internal View</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>DBGDTRRXint</td>
<td>RO</td>
<td>Debug Data Transfer Register, Receive, Internal View</td>
</tr>
<tr>
<td>c0</td>
<td>0</td>
<td>c6</td>
<td>0</td>
<td>DBGWFAR</td>
<td>RW</td>
<td>Watchpoint Fault Address Register, RES0</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Previously returned information about the address of the instruction that accessed a watchpoint address. This register is now deprecated and is RES0.</td>
</tr>
<tr>
<td>c0</td>
<td>0</td>
<td>c7</td>
<td>0</td>
<td>DBGVCR</td>
<td>RW</td>
<td>Debug Vector Catch Register</td>
</tr>
<tr>
<td>c0</td>
<td>2</td>
<td>c0</td>
<td>0</td>
<td>DBGDTRRXext</td>
<td>RW</td>
<td>Debug Data Transfer Register, Receive, External View</td>
</tr>
<tr>
<td>c0</td>
<td>2</td>
<td>c2</td>
<td>0</td>
<td>DBGDSCext</td>
<td>RW</td>
<td>Debug Status and Control Register, External View</td>
</tr>
<tr>
<td>c0</td>
<td>2</td>
<td>c3</td>
<td>0</td>
<td>DBGDTRRXext</td>
<td>RW</td>
<td>Debug Data Transfer Register, Transmit, External View</td>
</tr>
<tr>
<td>c0</td>
<td>2</td>
<td>c6</td>
<td>0</td>
<td>DBGOSECCR</td>
<td>RW</td>
<td>Debug OS Lock Exception Catch Control Register</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>DBGBVR0</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 0</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>DBGBVR1</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 1</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c2</td>
<td>0</td>
<td>DBGBVR2</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 2</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c3</td>
<td>0</td>
<td>DBGBVR3</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 3</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c4</td>
<td>0</td>
<td>DBGBVR4</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 4</td>
</tr>
<tr>
<td>c0</td>
<td>4</td>
<td>c5</td>
<td>0</td>
<td>DBGBVR5</td>
<td>RW</td>
<td>Debug Breakpoint Value Register 5</td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c0</td>
<td>0</td>
<td>DBGBCR0</td>
<td>RW</td>
<td>C6.2 Debug Breakpoint Control Registers on page C6-412</td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c1</td>
<td>0</td>
<td>DBGBCR1</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c2</td>
<td>0</td>
<td>DBGBCR2</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c3</td>
<td>0</td>
<td>DBGBCR3</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c4</td>
<td>0</td>
<td>DBGBCR4</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>5</td>
<td>c5</td>
<td>0</td>
<td>DBGBCR5</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>6</td>
<td>c0</td>
<td>0</td>
<td>DBGWVR0</td>
<td>RW</td>
<td>Debug Watchpoint Value Register 0</td>
</tr>
<tr>
<td>c0</td>
<td>6</td>
<td>c1</td>
<td>0</td>
<td>DBGWVR1</td>
<td>RW</td>
<td>Debug Watchpoint Value Register 1</td>
</tr>
<tr>
<td>CRn</td>
<td>Op2</td>
<td>CRm</td>
<td>Op1</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>-----------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>c0</td>
<td>6</td>
<td>c2</td>
<td>0</td>
<td>DBGWVR2</td>
<td>RW</td>
<td>Debug Watchpoint Value Register 2</td>
</tr>
<tr>
<td>c0</td>
<td>6</td>
<td>c3</td>
<td>0</td>
<td>DBGWVR3</td>
<td>RW</td>
<td>Debug Watchpoint Value Register 3</td>
</tr>
<tr>
<td>c0</td>
<td>7</td>
<td>c0</td>
<td>0</td>
<td>DBGWCR0</td>
<td>RW</td>
<td>C6.3 Debug Watchpoint Control Registers on page C6-415</td>
</tr>
<tr>
<td>c0</td>
<td>7</td>
<td>c1</td>
<td>0</td>
<td>DBGWCR1</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>7</td>
<td>c2</td>
<td>0</td>
<td>DBGWCR2</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c0</td>
<td>7</td>
<td>c3</td>
<td>0</td>
<td>DBGWCR3</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>c1</td>
<td>0</td>
<td>c0</td>
<td>0</td>
<td>DBGDRAR[31:0]</td>
<td>RO</td>
<td>Debug ROM Address Register</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>c1</td>
<td>-</td>
<td>DBGDRAR[63:0]</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>c1</td>
<td>1</td>
<td>c4</td>
<td>0</td>
<td>DBGBXVR4</td>
<td>RW</td>
<td>Debug Breakpoint Extended Value Register 4</td>
</tr>
<tr>
<td>c1</td>
<td>1</td>
<td>c5</td>
<td>0</td>
<td>DBGBXVR5</td>
<td>RW</td>
<td>Debug Breakpoint Extended Value Register 5</td>
</tr>
<tr>
<td>c1</td>
<td>4</td>
<td>c0</td>
<td>0</td>
<td>DBGOSLAR</td>
<td>WO</td>
<td>Debug OS Lock Access Register</td>
</tr>
<tr>
<td>c1</td>
<td>4</td>
<td>c1</td>
<td>0</td>
<td>DBGOSLSR</td>
<td>RO</td>
<td>Debug OS Lock Status Register</td>
</tr>
<tr>
<td>c1</td>
<td>4</td>
<td>c3</td>
<td>0</td>
<td>DBGOSDLR</td>
<td>RW</td>
<td>Debug OS Double Lock Register</td>
</tr>
<tr>
<td>c1</td>
<td>4</td>
<td>c4</td>
<td>0</td>
<td>DBGPRCR</td>
<td>RW</td>
<td>Debug Power/Reset Control Register</td>
</tr>
<tr>
<td>c2</td>
<td>2</td>
<td>c0</td>
<td>0</td>
<td>DBGDSAR[31:0]</td>
<td>RO</td>
<td>Debug Self Address Register RES0</td>
</tr>
<tr>
<td>-</td>
<td>0</td>
<td>c2</td>
<td>-</td>
<td>DBGDSAR[63:0]</td>
<td>RO</td>
<td>Previously defined the offset from the base address defined in DBGDRAR of</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>the physical base address of the debug registers for the processor. This</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>register is now deprecated and RES0.</td>
</tr>
<tr>
<td>c7</td>
<td>7</td>
<td>c0</td>
<td>0</td>
<td>DBGDEVID2</td>
<td>RO</td>
<td>Debug Device ID Register 2, RES0</td>
</tr>
<tr>
<td>c7</td>
<td>7</td>
<td>c1</td>
<td>0</td>
<td>DBGDEVID1</td>
<td>RO</td>
<td>C6.6 Debug Device ID Register 1 on page C6-422</td>
</tr>
<tr>
<td>c7</td>
<td>7</td>
<td>c2</td>
<td>0</td>
<td>DBGDEVID</td>
<td>RO</td>
<td>C6.5 Debug Device ID Register on page C6-420</td>
</tr>
<tr>
<td>c7</td>
<td>6</td>
<td>c8</td>
<td>0</td>
<td>DBGCLAIMSET</td>
<td>RW</td>
<td>Debug Claim Tag Set Register</td>
</tr>
<tr>
<td>c7</td>
<td>6</td>
<td>c9</td>
<td>0</td>
<td>DBGCLAIMCLR</td>
<td>RW</td>
<td>Debug Claim Tag Clear Register</td>
</tr>
<tr>
<td>c7</td>
<td>6</td>
<td>c14</td>
<td>0</td>
<td>DBGAUTHSTATUS</td>
<td>RO</td>
<td>Debug Authentication Status Register</td>
</tr>
</tbody>
</table>
C6.2 Debug Breakpoint Control Registers

The DBGBCR\textsubscript{n} characteristics are:

**Purpose**

Holds control information for a breakpoint. Each DBGBVR is associated with a DBGBCR to form a *Breakpoint Register Pair* (BRP). DBGBVR\textsubscript{n} is associated with DBGBCR\textsubscript{n} to form BRP\textsubscript{n}.

The range of \( n \) for DBGBCR\textsubscript{n} is 0 to 5.

**Usage constraints**

These registers are accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

DBGBCR\textsubscript{n} are architecturally mapped to the external DBGBCR\textsubscript{n} _EL1 registers.

**Attributes**

See *C6.1 AArch32 debug register summary* on page C6-410.

The debug logic reset value of a DBGBCR\textsubscript{n} is UNKNOWN.

![Figure C6-1 DBGBCR](image)

**[31:24]**

Reserved, res0.

**BT, [23:20]**

Breakpoint Type. This field controls the behavior of Breakpoint debug event generation. This includes the meaning of the value held in the associated DBGBVR\textsubscript{n}, indicating whether it is an instruction address match or mismatch or a Context match. It also controls whether the breakpoint is linked to another breakpoint. The possible values are:

- **0b0000** Unlinked instruction address match.
- **0b0001** Linked instruction address match.
- **0b0010** Unlinked Context ID match.
- **0b0011** Linked Context ID match.
- **0b0100** Unlinked instruction address mismatch.
- **0b0101** Linked instruction address mismatch.
- **0b1000** Unlinked VMID match.
- **0b1001** Linked VMID match.
- **0b1010** Unlinked VMID + Context ID match.
- **0b1011** Linked VMID + Context ID match.
All other values are reserved.

The field break down is:

- **BT[3:1]**: Base type. If the breakpoint is not context-aware, these bits are **RES0**. Otherwise, the possible values are:
  
  - **0b000**: Match address. DBGBVRₙ is the address of an instruction.
  - **0b001**: Match context ID. DBGBVRₙ[31:0] is a context ID.
  - **0b010**: Mismatch address. Behaves as type **0b000** if halting debug-mode is enabled and halting is allowed.

  Otherwise, DBGBVRₙ is the address of an instruction to be stepped.

  - **0b100**: Match VMID. DBGBVRₙ[7:0] is a VMID.
  - **0b101**: Match VMID and context ID. DBGBVRₙ[31:0] is a context ID, and DBGBVRₙ[7:0] is a VMID.

- **BT[0]**: Enable linking.

**LBN, [19:16]**

Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.

**SSC, [15:14]**

Security State Control. Determines the security states that a breakpoint debug event for breakpoint _n_ is generated.

This field must be interpreted with the **Higher Mode Control (HMC)**, and **Privileged Mode Control (PMC)**, fields to determine the mode and security states that can be tested.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for possible values of the fields.

**HMC, [13]**

Hyp Mode Control bit. Determines the debug perspective for deciding when a breakpoint debug event for breakpoint _n_ is generated.

This bit must be interpreted with the SSC and PMC fields to determine the mode and security states that can be tested.

See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for possible values of the fields.

**[12:9]**

Reserved, **RES0**.

**BAS, [8:5]**

Byte Address Select. Defines which half-words a regular breakpoint matches, regardless of the instruction set and execution state. A debugger must program this field as follows:

- **0x3**: Match the T32 instruction at DBGBVRₙ.
- **0xC**: Match the T32 instruction at DBGBVRₙ+2.
- **0xF**: Match the A32 instruction at DBGBVRₙ, or context match.

All other values are reserved.


See the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* for more information on how the BAS field is interpreted by hardware.
[4:3] Reserved, RES0.

PMC, [2:1]
Privileged Mode Control. Determines the exception level or levels that a breakpoint debug event for breakpoint \( n \) is generated.

This field must be interpreted with the SSC and HMC fields to determine the mode and security states that can be tested.

See the Arm\textsuperscript{®} Architecture Reference Manual Armv8, for Armv8-A architecture profile for possible values of the fields.

Bits[2:1] have no effect for accesses made in Hyp mode.

E, [0]
Enable breakpoint. This bit enables the BRP:

\[\begin{array}{lcl}
0 & \rightarrow & \text{BRP disabled.} \\
1 & \rightarrow & \text{BRP enabled.} \\
\end{array}\]

A BRP never generates a breakpoint debug event when it is disabled.

The value of DBGBCR\( n \).E is UNKNOWN on reset. A debugger must ensure that DBGBCR\( n \).E has a defined value before it enables debug.

To access the DBGBCR\( n \):

\texttt{MRC p14, 0, <Rt>, c0, cn, 4; Read Debug Breakpoint Control Register n}
\texttt{MCR p14, 0, <Rt>, c0, cn, 4; Write Debug Breakpoint Control Register n}

The DBGBCR\( n \).EL1 can be accessed through the external debug interface, offset 0x4n8. The range of bits for DBGBCR\( n \).EL1 is 0 to 5.
C6.3 Debug Watchpoint Control Registers

The DBGWCR\(_n\) characteristics are:

**Purpose**

Holds control information for a watchpoint. Each DBGWCR is associated with a
DBGWVR\(_{EL1}\) to form a *Watchpoint Register Pair* (WRP). DBGWCR\(_n\) is associated with
DBGWVR\(_{n EL1}\) to form WRP\(_n\).

The range of \(n\) for DBGBCR\(_n\) is 0 to 3.

**Usage constraints**

These registers are accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

**Configurations**

The DBGWCR\(_n\) are architecturally mapped to the external DBGWCR\(_{n EL1}\) registers.

**Attributes**

See *C6.1 AArch32 debug register summary* on page C6-410.

The debug logic reset value of a DBGWCR\(_{EL1}\) is **UNKNOWN**.

![Figure C6-2 DBGWCR](image)

**[31:29]**

Reserved, RES0.

**MASK, [28:24]**

Address mask. Only objects up to 2GB can be watched using a single mask.

- 0b0000: No mask
- 0b0001: Reserved
- 0b0010: Reserved

Other values mask the corresponding number of address bits, from 0b00011 masking 3 address
bits (0x000007 mask for address) to 0b111111 masking 31 address bits (0xFFFFFFFF mask for
address).

**[23:21]**

Reserved, RES0.

**WT, [20]**

Watchpoint type. Possible values are:

- 0: Unlinked data address match.
- 1: Linked data address match.
On Cold reset, the field reset value is architecturally UNKNOWN.

LBN, [19:16]
Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

On Cold reset, the field reset value is architecturally UNKNOWN.

SSC, [15:14]
Security state control. Determines the Security states under which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.

On Cold reset, the field reset value is architecturally UNKNOWN.

HMC, [13]
Higher mode control. Determines the debug perspective for deciding when a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.

On Cold reset, the field reset value is architecturally UNKNOWN.

BAS, [12:5]
Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVRn is being watched. See the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile for more information.

LSC, [4:3]
Load/store access control. This field enables watchpoint matching on the type of access being made. The possible values are:

\[0b01\] Match instructions that load from a watchpointed address.
\[0b10\] Match instructions that store to a watchpointed address.
\[0b11\] Match instructions that load from or store to a watchpointed address.

All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

Ignored if E is 0.

On Cold reset, the field reset value is architecturally UNKNOWN.

PAC, [2:1]
Privilege of access control. Determines the exception level or levels at which a watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.

On Cold reset, the field reset value is architecturally UNKNOWN.

E, [0]
Enable watchpoint n. Possible values are:

0 Watchpoint disabled.
1 Watchpoint enabled.

On Cold reset, the field reset value is architecturally UNKNOWN.

To access the DBGWCRn:

\[\text{MRC p14, 0, \langle Rt\rangle, c0, cn, 7; Read Debug Watchpoint Control Register n}\]
\[\text{MCR p14, 0, \langle Rt\rangle, c0, cn, 7; Write Debug Watchpoint Control Register n}\]
The DBGWCR\(_n\)_EL1 can be accessed through the external debug interface, offset 0x8n8. The range of \(n\) for DBGWCR\(_n\)_EL1 is 0 to 3.
C6.4 Debug ID Register

The DBGDIDR characteristics are:

**Purpose**

Specifies:

- The version of the Debug architecture that is implemented.
- Some features of the debug implementation.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

See C.6.1 AArch32 debug register summary on page C6-410.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRPs</td>
<td>BRPs</td>
<td>CTX_CMPs</td>
<td>Version</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure C6-3 DBGDIDR bit assignments**

**WRPs, [31:28]**

The number of Watchpoint Register Pairs (WRPs) implemented. The number of implemented WRPs is one more than the value of this field. The value is:

0x3 The processor implements 4 WRPs.

**BRPs, [27:24]**

The number of Breakpoint Register Pairs (BRPs) implemented. The number of implemented BRPs is one more than the value of this field. The value is:

0x5 The processor implements 6 BRPs.

**CTX_CMPs, [23:20]**

The number of BRPs that can be used for Context matching. This is one more than the value of this field. The value is:

0x1 The processor implements two Context matching breakpoints, breakpoints 4 and 5.

**Version, [19:16]**

The Debug architecture version.

0x6 The processor implements Armv8 Debug architecture.

**DEVID_imp, [15]**

Reserved, RAO.
nSUHD_imp, [14]

Secure User Halting Debug not implemented bit. The value is:

1 The processor does not implement Secure User Halting Debug.

PCSR_imp, [13]

Reserved, RAZ.

SE, [12]

EL3 implemented. The value is:

1 The processor implements EL3.

[11:0]

Reserved, RES0.

To access the DBGIDR:

MRC p14, 0, <Rt>, c0, c0, 0; Read Debug ID Register
C6.5 Debug Device ID Register

The DBGDEVID characteristics are:

**Purpose**
Specifies the version of the Debug architecture is implemented, and some features of the debug implementation.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR NS = 1)</th>
<th>EL3 (SCR NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0</td>
<td>EL0</td>
<td>EL1</td>
<td>EL1</td>
<td>EL2</td>
<td>EL3</td>
</tr>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR NS = 1)</td>
<td>(SCR NS = 0)</td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
See *C6.1 AArch32 debug register summary* on page C6-410.

<table>
<thead>
<tr>
<th>31</th>
<th>28</th>
<th>27</th>
<th>24</th>
<th>23</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CIDMask</td>
<td>AuxRegs</td>
<td>DoubleLock</td>
<td>VirtExtns</td>
<td></td>
<td></td>
<td></td>
<td>PCsample</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**CIDMask, [31:28]**
Specifies the level of support for the Context ID matching breakpoint masking capability. This value is:

- 0x0 Context ID masking is not implemented.

**AuxRegs, [27:24]**
Specifies support for the Debug External Auxiliary Control Register. This value is:

- 0x0 None supported.

**DoubleLock, [23:20]**
Specifies support for the Debug OS Double Lock Register. This value is:

- 0x1 The processor supports Debug OS Double Lock Register.

**VirtExtns, [19:16]**
Specifies whether EL2 is implemented. This value is:

- 0x1 The processor implements EL2.

**VectorCatch, [15:12]**
Defines the form of the vector catch event implemented. This value is:

- 0x0 The processor implements address matching form of vector catch.

**BPAddrMask, [11:8]**
Indicates the level of support for the Immediate Virtual Address (IVA) matching breakpoint masking capability. This value is:
0xF     Breakpoint address masking not implemented. DBGBCRn[28:24] are RES0.

WPAddrMask, [7:4]
Indicates the level of support for the DVA matching watchpoint masking capability. This value is:
0x1     Watchpoint address mask implemented.

PCSample, [3:0]
Indicates the level of support for Program Counter sampling using debug registers 40 and 41. This value is:
0x3     EDPCSR, EDCIDSR and EDVIDSR are implemented as debug registers 40, 41, and 42.

To access the DBGDEVID:

```
MRC p14, 0, <Rt>, c7, c2, 7; Read Debug Device ID Register 0
```
C6.6 Debug Device ID Register 1

The DBGDEVID1 characteristics are:

**Purpose**
Adds to the information given by the DBGDIDR by describing other features of the debug implementation.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
See *C6.1 AArch32 debug register summary* on page C6-410.

![Figure C6-5 DBGDEVID1 bit assignments](image-url)

**[31:4]**
Reserved, RES0.

**PCSROffset, [3:0]**
Indicates the offset applied to PC samples returned by reads of EDPCSR. The value is:
0x2  EDPCSR samples have no offset applied and do not sample the instruction set state in the AArch32 state.

To access the DBGDEVID1:

\[ \text{MRC p14, 0, <Rt>, c7, c1, 47 Read Debug Device ID Register 1} \]
Chapter C7
Memory-mapped debug registers

This chapter describes the debug memory-mapped registers and shows examples of how to use them.

It contains the following sections:

- C7.1 Memory-mapped debug register summary on page C7-424.
- C7.2 External Debug Reserve Control Register on page C7-428.
- C7.3 External Debug Integration Mode Control Register on page C7-430.
- C7.4 External Debug Device ID Register 0 on page C7-431.
- C7.5 External Debug Device ID Register 1 on page C7-432.
- C7.6 External Debug Processor Feature Register on page C7-433.
- C7.7 External Debug Feature Register on page C7-435.
- C7.8 External Debug AArch32 Processor Feature Register on page C7-437.
- C7.9 External Debug Peripheral Identification Registers on page C7-438.
- C7.10 External Debug Peripheral Identification Register 0 on page C7-439.
- C7.11 External Debug Peripheral Identification Register 1 on page C7-440.
- C7.12 External Debug Peripheral Identification Register 2 on page C7-441.
- C7.13 External Debug Peripheral Identification Register 3 on page C7-442.
- C7.14 External Debug Peripheral Identification Register 4 on page C7-443.
- C7.15 External Debug Peripheral Identification Register 5-7 on page C7-444.
- C7.16 External Debug Component Identification Registers on page C7-445.
- C7.17 External Debug Component Identification Register 0 on page C7-446.
- C7.18 External Debug Component Identification Register 1 on page C7-447.
- C7.19 External Debug Component Identification Register 2 on page C7-448.
- C7.20 External Debug Component Identification Register 3 on page C7-449.
C7.1 Memory-mapped debug register summary

The following table shows the offset address for the registers that are accessible from the external debug interface.

For those registers not described in this chapter, see the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000-0x01C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x020</td>
<td>EDESR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Event Status Register</td>
</tr>
<tr>
<td>0x024</td>
<td>EDECR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Execution Control Register</td>
</tr>
<tr>
<td>0x028-0x02C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x030</td>
<td>EDWAR[31:0]</td>
<td>RO</td>
<td>64</td>
<td>External Debug Watchpoint Address Register</td>
</tr>
<tr>
<td>0x034</td>
<td>EDWAR[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x038-0x07C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x080</td>
<td>DBGDTRRX_EL0</td>
<td>RW</td>
<td>32</td>
<td>Debug Data Transfer Register, Receive</td>
</tr>
<tr>
<td>0x084</td>
<td>EDITR</td>
<td>WO</td>
<td>32</td>
<td>External Debug Instruction Transfer Register</td>
</tr>
<tr>
<td>0x088</td>
<td>EDSCR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Status and Control Register</td>
</tr>
<tr>
<td>0x08C</td>
<td>DBGDTRTX_EL0</td>
<td>RW</td>
<td>32</td>
<td>Debug Data Transfer Register, Transmit</td>
</tr>
<tr>
<td>0x090</td>
<td>EDRCR</td>
<td>WO</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>0x094</td>
<td>EDACR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Auxiliary Control Register</td>
</tr>
<tr>
<td>0x098</td>
<td>EDECCR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Exception Catch Control Register</td>
</tr>
<tr>
<td>0x09C</td>
<td>-</td>
<td>-</td>
<td>32</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x0A0</td>
<td>EDPCSRlo</td>
<td>RO</td>
<td>32</td>
<td>External Debug Program Counter Sample Register, low word</td>
</tr>
<tr>
<td>0x0A4</td>
<td>EDCIDSR</td>
<td>RO</td>
<td>32</td>
<td>External Debug Context ID Sample Register</td>
</tr>
<tr>
<td>0x0A8</td>
<td>EDVIDSR</td>
<td>RO</td>
<td>32</td>
<td>External Debug Virtual Context Sample Register</td>
</tr>
<tr>
<td>0x0AC</td>
<td>EDPCSRhi</td>
<td>RO</td>
<td>32</td>
<td>External Debug Program Counter Sample Register, high word</td>
</tr>
<tr>
<td>0x0B0-0x2FC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x300</td>
<td>OSLAR_EL1</td>
<td>WO</td>
<td>32</td>
<td>OS Lock Access Register</td>
</tr>
<tr>
<td>0x304-0x30C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x310</td>
<td>EDPRCR</td>
<td>RW</td>
<td>32</td>
<td>External Debug Power/Reset Control Register</td>
</tr>
<tr>
<td>0x314</td>
<td>EDPRSR</td>
<td>RO</td>
<td>32</td>
<td>External Debug Processor Status Register</td>
</tr>
<tr>
<td>0x318-0x3FC</td>
<td>-</td>
<td>-</td>
<td>--</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x400</td>
<td>DBGBV[0:31]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 0</td>
</tr>
<tr>
<td>0x404</td>
<td>DBGBV[0:63]</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>0x408</td>
<td>DBGBCR[0:31]</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Type</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>--------------------------</td>
<td>------</td>
<td>-------</td>
<td>-------------------------------------------------</td>
</tr>
<tr>
<td>0x40C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x410</td>
<td>DBGBVR1_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 1</td>
</tr>
<tr>
<td>0x414</td>
<td>DBGBVR1_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x418</td>
<td>DBGBCR1_EL1</td>
<td>RW</td>
<td>32</td>
<td><a href="#">C6.2 Debug Breakpoint Control Registers on page C6-412</a></td>
</tr>
<tr>
<td>0x41C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x420</td>
<td>DBGBVR2_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 2</td>
</tr>
<tr>
<td>0x424</td>
<td>DBGBVR2_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x428</td>
<td>DBGBCR2_EL1</td>
<td>RW</td>
<td>32</td>
<td><a href="#">C6.2 Debug Breakpoint Control Registers on page C6-412</a></td>
</tr>
<tr>
<td>0x42C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x430</td>
<td>DBGBVR3_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 3</td>
</tr>
<tr>
<td>0x434</td>
<td>DBGBVR3_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x438</td>
<td>DBGBCR3_EL1</td>
<td>RW</td>
<td>32</td>
<td><a href="#">C6.2 Debug Breakpoint Control Registers on page C6-412</a></td>
</tr>
<tr>
<td>0x43C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x440</td>
<td>DBGBVR4_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 4</td>
</tr>
<tr>
<td>0x444</td>
<td>DBGBVR4_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x448</td>
<td>DBGBCR4_EL1</td>
<td>RW</td>
<td>32</td>
<td><a href="#">C6.2 Debug Breakpoint Control Registers on page C6-412</a></td>
</tr>
<tr>
<td>0x44C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x450</td>
<td>DBGBVR5_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Breakpoint Value Register 5</td>
</tr>
<tr>
<td>0x454</td>
<td>DBGBVR5_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x458</td>
<td>DBGBCR5_EL1</td>
<td>RW</td>
<td>32</td>
<td><a href="#">C6.2 Debug Breakpoint Control Registers on page C6-412</a></td>
</tr>
<tr>
<td>0x45C-0x7FC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x800</td>
<td>DBGWVR0_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Watchpoint Value Register 0</td>
</tr>
<tr>
<td>0x804</td>
<td>DBGWVR0_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x808</td>
<td>DBGWCR0_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Watchpoint Control Register 0</td>
</tr>
<tr>
<td>0x80C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x810</td>
<td>DBGWVR1_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Watchpoint Value Register 1</td>
</tr>
<tr>
<td>0x814</td>
<td>DBGWVR1_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x818</td>
<td>DBGWCR1_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Watchpoint Control Register 1</td>
</tr>
<tr>
<td>0x81C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x820</td>
<td>DBGWVR2_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Watchpoint Value Register 2</td>
</tr>
<tr>
<td>0x824</td>
<td>DBGWVR2_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x828</td>
<td>DBGWCR2_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Watchpoint Control Register 2</td>
</tr>
<tr>
<td>0x82C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x830</td>
<td>DBGWVR3_EL1[31:0]</td>
<td>RW</td>
<td>64</td>
<td>Debug Watchpoint Value Register 0</td>
</tr>
<tr>
<td>0x834</td>
<td>DBGWVR3_EL1[63:32]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[C6.2 Debug Breakpoint Control Registers on page C6-412](#)
### Table C7-1  Memory-mapped debug register summary (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x838</td>
<td>DBGWCR3_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Watchpoint Control Register 2</td>
</tr>
<tr>
<td>0x83C-0xCFC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xD00</td>
<td>MIDR_EL1</td>
<td>RO</td>
<td>32</td>
<td>B1.96 Main ID Register on page B1-307</td>
</tr>
<tr>
<td>0xD04-0xD1C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xD20</td>
<td>EDPFR[31:0]</td>
<td>RO</td>
<td>64</td>
<td>C7.6 External Debug Processor Feature Register on page C7-433</td>
</tr>
<tr>
<td>0xD24</td>
<td>EDPFR[63:32]</td>
<td>RO</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>0xD28</td>
<td>EDDFR[31:0]</td>
<td>RO</td>
<td>64</td>
<td>C7.7 External Debug Feature Register on page C7-435</td>
</tr>
<tr>
<td>0xD2C</td>
<td>EDDFR[63:32]</td>
<td>RO</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>0xD30-0xD34</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xD38-0xD3C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xD60</td>
<td>EDAA32PFR</td>
<td>RO</td>
<td>64</td>
<td>C7.8 External Debug AArch32 Processor Feature Register on page C7-437</td>
</tr>
<tr>
<td>0xD64-0xEFC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xF00</td>
<td>EDITCTRL</td>
<td>RW</td>
<td>32</td>
<td>C7.3 External Debug Integration Mode Control Register on page C7-430</td>
</tr>
<tr>
<td>0xF04-0xF9C</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFA0</td>
<td>DBGCLAIMSET_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Claim Tag Set Register</td>
</tr>
<tr>
<td>0xFA4</td>
<td>DBGCLAIMCLR_EL1</td>
<td>RW</td>
<td>32</td>
<td>Debug Claim Tag Clear Register</td>
</tr>
<tr>
<td>0xFA8</td>
<td>EDDEVAFF0</td>
<td>RO</td>
<td>32</td>
<td>B1.97 Multiprocessor Affinity Register on page B1-309</td>
</tr>
<tr>
<td>0xFAC</td>
<td>EDDEVAFF1</td>
<td>RO</td>
<td>32</td>
<td>External Debug Device Affinity Register 1, RES0</td>
</tr>
<tr>
<td>0xFB0</td>
<td>EDLAR</td>
<td>WO</td>
<td>32</td>
<td>External Debug Lock Access Register</td>
</tr>
<tr>
<td>0xFB4</td>
<td>EDLSR</td>
<td>RO</td>
<td>32</td>
<td>External Debug Lock Status Register</td>
</tr>
<tr>
<td>0xFB8</td>
<td>DBGAUTHSTATUS_EL1</td>
<td>RO</td>
<td>32</td>
<td>Debug Authentication Status Register</td>
</tr>
<tr>
<td>0xFBC</td>
<td>EDDEVARCH</td>
<td>RO</td>
<td>32</td>
<td>External Debug Device Architecture Register</td>
</tr>
<tr>
<td>0xFC0</td>
<td>EDDEVID2</td>
<td>RO</td>
<td>32</td>
<td>External Debug Device ID Register 2, RES0</td>
</tr>
<tr>
<td>0xFC4</td>
<td>EDDEVID1</td>
<td>RO</td>
<td>32</td>
<td>C7.5 External Debug Device ID Register 1 on page C7-432</td>
</tr>
<tr>
<td>0xFC8</td>
<td>EDDEVID</td>
<td>RO</td>
<td>32</td>
<td>C7.4 External Debug Device ID Register 0 on page C7-431</td>
</tr>
<tr>
<td>0xFCC</td>
<td>EDDEVTYPE</td>
<td>RO</td>
<td>32</td>
<td>External Debug Device Type Register</td>
</tr>
<tr>
<td>0xFD0</td>
<td>EDPIDR4</td>
<td>RO</td>
<td>32</td>
<td>C7.14 External Debug Peripheral Identification Register 4 on page C7-443</td>
</tr>
<tr>
<td>0xFD4-0xFDCC</td>
<td>EDPIDR5-7</td>
<td>RO</td>
<td>32</td>
<td>C7.15 External Debug Peripheral Identification Register 5-7 on page C7-444</td>
</tr>
<tr>
<td>0xFE0</td>
<td>EDPIDR0</td>
<td>RO</td>
<td>32</td>
<td>C7.10 External Debug Peripheral Identification Register 0 on page C7-439</td>
</tr>
<tr>
<td>0xFE4</td>
<td>EDPIDR1</td>
<td>RO</td>
<td>32</td>
<td>C7.11 External Debug Peripheral Identification Register 1 on page C7-440</td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Type</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>------------</td>
<td>------</td>
<td>-------</td>
<td>---------------------------------------------------------------</td>
</tr>
<tr>
<td>0xFE8</td>
<td>EDPIDR2</td>
<td>RO</td>
<td>32</td>
<td>C7.12 External Debug Peripheral Identification Register 2 on page C7-441</td>
</tr>
<tr>
<td>0xFEC</td>
<td>EDPIDR3</td>
<td>RO</td>
<td>32</td>
<td>C7.13 External Debug Peripheral Identification Register 3 on page C7-442</td>
</tr>
<tr>
<td>0xFF0</td>
<td>EDCIDR0</td>
<td>RO</td>
<td>32</td>
<td>C7.17 External Debug Component Identification Register 0 on page C7-446</td>
</tr>
<tr>
<td>0xFF4</td>
<td>EDCIDR1</td>
<td>RO</td>
<td>32</td>
<td>C7.18 External Debug Component Identification Register 1 on page C7-447</td>
</tr>
<tr>
<td>0xFF8</td>
<td>EDCIDR2</td>
<td>RO</td>
<td>32</td>
<td>C7.19 External Debug Component Identification Register 2 on page C7-448</td>
</tr>
<tr>
<td>0xFFF8</td>
<td>EDCIDR3</td>
<td>RO</td>
<td>32</td>
<td>C7.20 External Debug Component Identification Register 3 on page C7-449</td>
</tr>
</tbody>
</table>
C7.2 External Debug Reserve Control Register

The EDRCR characteristics are:

**Purpose**

This register is used to allow imprecise entry to Debug state and clear sticky bits in EDSCR.

This register is part of the Debug registers functional group.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error</td>
<td>Error</td>
<td>Error</td>
<td>WI</td>
<td>WO</td>
</tr>
</tbody>
</table>

**Configurations**

EDRCR is in the Core power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary* on page C7-424.

EDRCR is a 32-bit register.

![EDRCR bit assignments](image)

**[31:5]**

Reserved, RES0.

**CBRRQ, [4]**

Allow imprecise entry to Debug state. The actions on writing to this bit are:

- 0: No action.
- 1: Allow imprecise entry to Debug state, for example by canceling pending bus accesses. Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.

**CSPA, [3]**

Clear Sticky Pipeline Advance. This bit is used to clear the EDSCR.PipeAdv bit to 0. The actions on writing to this bit are:

- 0: No action.
- 1: Clear the EDSCR.PipeAdv bit to 0.

**CSE, [2]**

Clear Sticky Error. Used to clear the EDSCR cumulative error bits to 0. The actions on writing to this bit are:

- 0: No action
Clear the EDSCR.\{TXU, RXO, ERR\} bits, and, if the processor is in Debug state, the EDSCR.ITO bit, to 0.

[1:0] Reserve, \text{RESO}.

The EDRCR can be accessed through the external debug interface, offset \text{0x90}. 

C7.3 External Debug Integration Mode Control Register

The EDITCTRL characteristics are:

**Purpose**
Enables the external debug to switch from its default mode into integration mode, where test software can control directly the inputs and outputs of the processor, for integration testing or topology detection.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RW</td>
</tr>
</tbody>
</table>

*Table C1-1  Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**
EDITCTRL is in the processor power domain.

**Attributes**
See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-2  EDITCTRL bit assignments](image)

**[31:1]**
Reserved, RES0.

**IME, [0]**
Integration Mode Enable.

RES0: The device does not revert to an integration mode to enable integration testing or topology detection.

The EDITCTRL can be accessed through the external debug interface, offset 0xF00.
C7.4 External Debug Device ID Register 0

The EDDEVID characteristics are:

**Purpose**

Provides extra information for external debuggers about features of the debug implementation.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1  Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**

The EDDEVID is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-3  EDDEVID bit assignments](image)

[31:28]  
Reserved, RES0.

**AuxRegs, [27:24]**

Indicates support for Auxiliary registers:

0x0 None supported.

[23:4]  
Reserved, RES0.

**PC Sample, [3:0]**

Indicates the level of sample-based profiling support using external debug registers 40 to 43:

0x3 EDPCSR, EDCIDSR, and EDVIDSR are implemented.

The EDDEVID can be accessed through the external debug interface, offset 0xFC8.
C7.5 External Debug Device ID Register 1

The EDDEVID1 characteristics are:

**Purpose**
Provides extra information for external debuggers about features of the debug implementation.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**
The EDDEVID1 is in the Debug power domain.

**Attributes**
See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-4 EDDEVID1 bit assignments](image)

**[31:4]**
Reserved, RES0.

**PCSROffset, [3:0]**
Indicates the offset applied to PC samples returned by reads of EDPCSR:
- $0 \times 2$ EDPCSR samples have no offset applied and do not sample the instruction set state.

The EDDEVID1 can be accessed through the external debug interface, offset $0 \times FC4$. 

---

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C7.6 External Debug Processor Feature Register

The EDPFR characteristics are:

**Purpose**

Provides additional information about implemented PE features in AArch64.

**Usage constraints**

This register is accessible as follows:

![Default

RO

Configurations

The EDPFR is in the Debug power domain.

**Attributes**

EDPFR is a 64-bit register.

![Figure C7-5 EDPFR bit assignments](#)

<table>
<thead>
<tr>
<th>63</th>
<th>28</th>
<th>24</th>
<th>20</th>
<th>19</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>GIC</td>
<td>AdvSIMD</td>
<td>FP</td>
<td>EL3</td>
<td>EL2</td>
<td>EL1</td>
<td>EL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[63:28]

Reserved, RES0.

**GIC, [27:24]**

System register GIC interface. Defined values are:

0x0 No System register interface to the GIC is supported.

0x1 System register interface to the GIC CPU interface is supported.

All other values are reserved.

**AdvSIMD, [23:20]**

Advanced SIMD. Defined values are:

0x0 Advanced SIMD is implemented.

0xF Advanced SIMD is not implemented.

All other values are reserved.

**FP, [19:16]**

Floating-point. Defined values are:

0x0 Floating-point is implemented.

0xF Floating-point is not implemented.

All other values are reserved.

**EL3 handling, [15:12]**

EL3 exception handling:

0x0 Instructions can be executed at EL3 in AArch32 state.
EL2 handling, [11:8]

EL2 exception handling:
0x0 Instructions can be executed at EL2 in AArch32 state.

EL1 handling, [7:4]

EL1 exception handling. The possible values are:
0x0 Instructions can be executed at EL1 in AArch32 state.

EL0 handling, [3:0]

EL0 exception handling. The possible values are:
0x0 Instructions can be executed at EL0 in AArch32 state.

The EDPFR[31:0] can be accessed through the external debug interface, offset 0xD20.
The EDPFR[63:32] can be accessed through the external debug interface, offset 0xD24.
C7.7 External Debug Feature Register

The EDDFR characteristics are:

**Purpose**

Provides top level information about the debug system in AArch64.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Default</th>
<th>RO</th>
</tr>
</thead>
</table>

**Configurations**

EDDFR is in the Debug power domain.

**Attributes**

EDDFR is a 64-bit register.

<table>
<thead>
<tr>
<th>Bit Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:32]</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>CTX_CMPs</td>
<td>Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.</td>
</tr>
<tr>
<td>[27:24]</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>WRPs</td>
<td>Number of watchpoints, minus 1. The value of 0b0000 is reserved.</td>
</tr>
<tr>
<td>[19:16]</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>BRPs</td>
<td>Number of breakpoints, minus 1. The value of 0b0000 is reserved.</td>
</tr>
<tr>
<td>PMUVer</td>
<td>Performance Monitors extension version. Indicates whether system register interface to performance monitors extension is implemented. Defined values are: 0x0000 Performance Monitors extension system registers not implemented. 0x0001 Performance Monitors extension system registers implemented, PMUv3. 0x1111 IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. All other values are reserved.</td>
</tr>
<tr>
<td>TraceVer</td>
<td>[7:4]</td>
</tr>
</tbody>
</table>

Figure C7-6 EDDFR bit assignments
Trace support. Indicates whether system register interface to a trace macrocell is implemented. Defined values are:

0x0000 Trace macrocell system registers not implemented.
0x0001 Trace macrocell system registers implemented.

All other values are reserved.

A value of 0x0000 only indicates that no system register interface to a trace macrocell is implemented. A trace macrocell might nevertheless be implemented without a system register interface.

**UNKNOWN, [7:4]**

Reserved, UNKNOWN.

EDDFR[31:0] can be accessed through the external debug interface, offset 0x0D28.

EDDFR[63:32] can be accessed through the external debug interface, offset 0x0D2C.
C7.8 External Debug AArch32 Processor Feature Register

The EDAA32PFR characteristics are:

**Purpose**

Provides additional information about implemented PE features in AArch32.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Default</th>
<th>RO</th>
</tr>
</thead>
</table>

**Configurations**

EDAA32PFR is in the Debug power domain.

**Attributes**

EDAA32PFR is a 64-bit register.

<table>
<thead>
<tr>
<th>63</th>
<th>16</th>
<th>15</th>
<th>12</th>
<th>11</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>AA32EL3</td>
<td>AA32EL2</td>
<td>PMSA</td>
<td>VMSA</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure C7-7 EDAA32PFR bit assignments

[63:16]

Reserved, RES0.

AA32EL3, [15:12]

AArch32 EL3 Exception level handling.

0001 EL3 can be executed in AArch32 Execution State only.

All other values are reserved.

AA32EL2, [11:8]

AArch32 EL2 Exception level handling.

0001 EL2 can be executed in AArch32 Execution State only.

All other values are reserved.

PMSA, [7:4]

Indicates support for an Armv8-R PMSA.

In Armv8-A, the only permitted value is 0x0.

VMSA, [7:4]

Indicates support for an Armv8-R PMSA.

In Armv8-A, the only permitted value is 0x0.

The EDAA32PFR [31:0] can be accessed through the internal memory-mapped interface and the external debug interface, offset 0x060.

The EDAA32PFR [63:32] can be accessed through the internal memory-mapped interface and the external debug interface, offset 0x064.
C7.9 External Debug Peripheral Identification Registers

The External Debug Peripheral Identification Registers provide standard information required for all components that conform to the Arm Debug Interface v5 specification.

The following table lists the External Debug Peripheral Identification Registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peripheral ID4</td>
<td>0x04</td>
<td>0xFD0</td>
</tr>
<tr>
<td>Peripheral ID5</td>
<td>0x00</td>
<td>0xFD4</td>
</tr>
<tr>
<td>Peripheral ID6</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>Peripheral ID7</td>
<td>0x00</td>
<td>0xFDC</td>
</tr>
<tr>
<td>Peripheral ID0</td>
<td>0x11</td>
<td>0xFE0</td>
</tr>
<tr>
<td>Peripheral ID1</td>
<td>0xBD</td>
<td>0xFE4</td>
</tr>
<tr>
<td>Peripheral ID2</td>
<td>0x2B</td>
<td>0xFE8</td>
</tr>
<tr>
<td>Peripheral ID3</td>
<td>0x00</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Only bits[7:0] of each Peripheral ID Register are used, with bits[31:8] reserved. Together, the eight Peripheral ID Registers define a single 64-bit Peripheral ID.
C7.10 External Debug Peripheral Identification Register 0

The EDPIDR0 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**

The EDPIDR0 is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary on page C7-424*.

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Part_0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure C7-8 EDPIDR0 bit assignments*

[31:8]

Reserved, RES0.

**Part_0, [7:0]**

0x01 Least significant byte of the debug part number.

The EDPIDR0 can be accessed through the external debug interface, offset 0xFE0.
C7.11 External Debug Peripheral Identification Register 1

The EDPIDR1 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1  Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**
The EDPIDR1 is in the Debug power domain.

**Attributes**
See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-9 EDPIDR1 bit assignments](image)

[31:8]
Reserved, RES0.

**DES_0, [7:4]**
0xB Arm Limited. This is the least significant nibble of JEP106 ID code.

**Part_1, [3:0]**
0x0 Most significant nibble of the debug part number.

The EDPIDR1 can be accessed through the external debug interface, offset 0xFE4.
C7.12 External Debug Peripheral Identification Register 2

The EDPIDR2 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**

The EDPIDR2 is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-10 EDPIDR2 bit assignments](image)

[31:8]

Reserved, res0.

**Revision, [7:4]**

0x2 r1p0.

JEDEC, [3]

0b1 RAO. Indicates a JEP106 identity code is used.

**DES_1, [2:0]**

0b11 Arm Limited. This is the most significant nibble of JEP106 ID code.

The EDPIDR2 can be accessed through the external debug interface, offset 0xFE8.
C7.13 External Debug Peripheral Identification Register 3

The EDPIDR3 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**

The EDPIDR3 is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary on page C7-424*.

![Figure C7-11 EDPIDR3 bit assignments](image)

[31:8]

Reserved, RES0.

REVAND, [7:4]

0x0 Part minor revision.

CMOD, [3:0]

0x0 Customer modified.

The EDPIDR3 can be accessed through the external debug interface, offset 0xFEC.
C7.14 External Debug Peripheral Identification Register 4

The EDPIDR4 characteristics are:

**Purpose**
- Provides information to identify an external debug component.

**Usage constraints**
- This register is accessible as follows:
  - Off
  - DLK
  - OSLK
  - EDAD
  - SLK
  - Default

Table C1-1 Conditions on external register access to debug registers on page C1-369 describes the condition codes.

**Configurations**
- The EDPIDR4 is in the Debug power domain.

**Attributes**
- See C7.1 Memory-mapped debug register summary on page C7-424.

![Figure C7-12 EDPIDR4 bit assignments](image)

- [31:8]
  - Reserved, Res0.

- Size, [7:4]
  - 0x0: Size of the component. Log2 the number of 4KB pages from the start of the component to the end of the component ID registers.

- DES_2, [3:0]
  - 0x4: Arm Limited. This is the least significant nibble JEP106 continuation code.

The EDPIDR4 can be accessed through the external debug interface, offset 0xFD0.
C7.15 External Debug Peripheral Identification Register 5-7

No information is held in the Peripheral ID5, Peripheral ID6, and Peripheral ID7 Registers. They are reserved for future use and are RES0.
C7.16 External Debug Component Identification Registers

There are four read-only External Debug Component Identification Registers, Component ID0 through Component ID3.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component ID0</td>
<td>0x0D</td>
<td>0xFF0</td>
</tr>
<tr>
<td>Component ID1</td>
<td>0x90</td>
<td>0xFF4</td>
</tr>
<tr>
<td>Component ID2</td>
<td>0x05</td>
<td>0xFF8</td>
</tr>
<tr>
<td>Component ID3</td>
<td>0xB1</td>
<td>0xFFC</td>
</tr>
</tbody>
</table>

The External Debug Component Identification Registers identify Debug as an Arm Debug Interface v5 component.
C7.17 External Debug Component Identification Register 0

The EDCIDR0 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers on page C1-369 describes the condition codes.*

**Configurations**

The EDCIDR0 is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary on page C7-424.*

![EDCIDR0 bit assignments](image)

**[31:8]**

Reserved, `RES0`.

**PRMBL_0, [7:0]**

0x0D

Preamble byte 0.

The EDCIDR0 can be accessed through the external debug interface, offset 0xFF0.
C7.18 External Debug Component Identification Register 1

The EDCIDR1 characteristics are:

Purpose
Provides information to identify an external debug component.

Usage constraints
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

Table C1-1  Conditions on external register access to debug registers on page C1-369 describes the condition codes.

Configurations
The EDCIDR1 is in the Debug power domain.

Attributes
See C7.1 Memory-mapped debug register summary on page C7-424.

Figure C7-14 EDCIDR1 bit assignments

[31:8]
Reserved, RES0.

CLASS, [7:4]
0x9 Debug component.

PRMBL_1, [3:0]
0x0 Preamble.

The EDCIDR1 can be accessed through the external debug interface, offset 0xFFF4.
C7.19 External Debug Component Identification Register 2

The EDCIDR2 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1 Conditions on external register access to debug registers* on page C1-369 describes the condition codes.

**Configurations**

The EDCIDR2 is in the Debug power domain.

**Attributes**

See *C7.1 Memory-mapped debug register summary* on page C7-424.

![Figure C7-15 EDCIDR2 bit assignments](image)

[31:8]

Reserved, RES0.

**PRMBL_2, [7:0]**

0x05 Preamble byte 2.

The EDCIDR2 can be accessed through the external debug interface, offset 0xFF8.
C7.20 **External Debug Component Identification Register 3**

The EDCIDR3 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Table C1-1  Conditions on external register access to debug registers on page C1-369* describes the condition codes.

**Configurations**
The EDCIDR3 is in the Debug power domain.

**Attributes**
See *C7.1 Memory-mapped debug register summary on page C7-424.*

<table>
<thead>
<tr>
<th>31</th>
<th></th>
<th></th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>PRMBL_3</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure C7-16 EDCIDR3 bit assignments*

[31:8]
Reserved, RES0.

PRMBL_3, [7:0]

0xB1  Preamble byte 3.

The EDCIDR3 can be accessed through the external debug interface, offset 0xFFC.
This chapter describes the ROM table that debuggers can use to determine which components are implemented. It also describes the ROM table registers.

It contains the following sections:

- C8.1 About the ROM table on page C8-452.
- C8.2 ROM table register interface on page C8-453.
- C8.3 ROM table register summary on page C8-454.
- C8.4 ROM entry registers on page C8-455.
- C8.5 ROM Table Peripheral Identification Registers on page C8-459.
- C8.6 ROM Table Peripheral Identification Register 0 on page C8-460.
- C8.7 ROM Table Peripheral Identification Register 1 on page C8-461.
- C8.8 ROM Table Peripheral Identification Register 2 on page C8-462.
- C8.9 ROM Table Peripheral Identification Register 3 on page C8-463.
- C8.10 ROM Table Peripheral Identification Register 4 on page C8-464.
- C8.11 ROM Table Peripheral Identification Register 5-7 on page C8-465.
- C8.12 ROM Table Component Identification Registers on page C8-466.
- C8.13 ROM Table Component Identification Register 0 on page C8-467.
- C8.14 ROM Table Component Identification Register 1 on page C8-468.
- C8.15 ROM Table Component Identification Register 2 on page C8-469.
- C8.16 ROM Table Component Identification Register 3 on page C8-470.
C8.1 About the ROM table

The processor includes a ROM table that complies with the Arm CoreSight Architecture Specification. This table contains a list of components such as processor debug units, processor Cross Trigger Interfaces (CTIs), processor Performance Monitoring Units (PMUs), and processor Embedded Trace Macrocell (ETM) trace units. Debuggers can use the ROM table to determine which components are implemented inside the Cortex-A32 processor.

If a component is not included in your configuration of the Cortex-A32 processor, the corresponding debug APB ROM table entry is still present but the component is marked as not present.
C8.2 ROM table register interface

The interface to the ROM table entries is the APB slave port.

See C1.2 Debug access on page C1-367.
## C8.3 ROM table register summary

The following table shows the offsets from the physical base address of the ROM table.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>ROMENTRY0</td>
<td>RO</td>
<td>8.4 ROM entry registers on page C8-455</td>
</tr>
<tr>
<td>0x004</td>
<td>ROMENTRY1</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x008</td>
<td>ROMENTRY2</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x00C</td>
<td>ROMENTRY3</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x010</td>
<td>ROMENTRY4</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x014</td>
<td>ROMENTRY5</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x018</td>
<td>ROMENTRY6</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x01C</td>
<td>ROMENTRY7</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x020</td>
<td>ROMENTRY8</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x024</td>
<td>ROMENTRY9</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x028</td>
<td>ROMENTRY10</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x02C</td>
<td>ROMENTRY11</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x030</td>
<td>ROMENTRY12</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x034</td>
<td>ROMENTRY13</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x038</td>
<td>ROMENTRY14</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x03C</td>
<td>ROMENTRY15</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0x040-0xFCC</td>
<td>-</td>
<td>RO</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0xFD0</td>
<td>ROMPIDR4</td>
<td>RO</td>
<td>8.10 ROM Table Peripheral Identification Register 4 on page C8-464</td>
</tr>
<tr>
<td>0xFD4</td>
<td>ROMPIDR5</td>
<td>RO</td>
<td>8.11 ROM Table Peripheral Identification Register 5-7 on page C8-465</td>
</tr>
<tr>
<td>0xFD8</td>
<td>ROMPIDR6</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFD0</td>
<td>ROMPIDR7</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFE0</td>
<td>ROMPIDR0</td>
<td>RO</td>
<td>8.6 ROM Table Peripheral Identification Register 0 on page C8-460</td>
</tr>
<tr>
<td>0xFE4</td>
<td>ROMPIDR1</td>
<td>RO</td>
<td>8.7 ROM Table Peripheral Identification Register 1 on page C8-461</td>
</tr>
<tr>
<td>0xFE8</td>
<td>ROMPIDR2</td>
<td>RO</td>
<td>8.8 ROM Table Peripheral Identification Register 2 on page C8-462</td>
</tr>
<tr>
<td>0xFEC</td>
<td>ROMPIDR3</td>
<td>RO</td>
<td>8.9 ROM Table Peripheral Identification Register 3 on page C8-463</td>
</tr>
<tr>
<td>0xFF0</td>
<td>ROMCIDR0</td>
<td>RO</td>
<td>8.13 ROM Table Component Identification Register 0 on page C8-467</td>
</tr>
<tr>
<td>0xFF4</td>
<td>ROMCIDR1</td>
<td>RO</td>
<td>8.14 ROM Table Component Identification Register 1 on page C8-468</td>
</tr>
<tr>
<td>0xFF8</td>
<td>ROMCIDR2</td>
<td>RO</td>
<td>8.15 ROM Table Component Identification Register 2 on page C8-469</td>
</tr>
<tr>
<td>0xFFC</td>
<td>ROMCIDR3</td>
<td>RO</td>
<td>8.16 ROM Table Component Identification Register 3 on page C8-470</td>
</tr>
</tbody>
</table>
C8.4 ROM entry registers

The characteristics of the ROMENTRY\(n\) are:

**Purpose**

Indicates to a debugger whether the debug component is present in the debug logic of the processor. There are 16 ROMENTRY registers in the Cortex-A32 processor.

**Usage constraints**

These registers are accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**

**Attributes**

See *C8.3 ROM table register summary on page C8-454*.

![Figure C8-1 ROMENTRY bit assignments](image)

**Address offset, [31:12]** There is one copy of this register that is used in both Secure and Non-secure states.

Address offset for the debug component.

There is one copy of this register that is used in both Secure and Non-secure states. Negative values of address offsets are permitted using the two’s complement of the offset.

**[11:2]**

Reserved, RES0.

**Format, [1]**

Format of the ROM table entry. The value for all ROMENTRY registers is:

0 \> End marker.

1 \> 32-bit format.

**Component present, [0]**

Indicates whether the component is present:

0 \> Component is not present.

1 \> Component is present.

The debug, CTI, and PMU components for core 0 are always present.

The Physical Address of a debug component is determined by shifting the address offset 12 places to the left and adding the result to the Physical Address of the Cortex-A32 processor ROM table.
The following tables show the offset values for all ROMENTRY values when a v8 memory map is implemented and the offset values for all ROMENTRY values when a legacy v7 memory map is implemented.

If a core is not implemented, the ROMENTRY registers for its debug, CTI, PMU, and ETM trace unit components are 0x00000000 when a v8 memory map is implemented and 0x00000002 when a v7 memory map is implemented.

If a core is implemented but the ETM trace unit is not implemented then the corresponding ROMENTRY register is 0x00000002 in both the v7 and v8 memory maps.

<table>
<thead>
<tr>
<th>Name</th>
<th>Debug component</th>
<th>Address offset [31:12]</th>
<th>ROMENTRY value</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMENTRY0</td>
<td>Core 0 Debug</td>
<td>0x00010</td>
<td>0x00010003</td>
</tr>
<tr>
<td>ROMENTRY1</td>
<td>Core 0 CTI</td>
<td>0x00020</td>
<td>0x00020003</td>
</tr>
<tr>
<td>ROMENTRY2</td>
<td>Core 0 PMU</td>
<td>0x00030</td>
<td>0x00030003</td>
</tr>
<tr>
<td>ROMENTRY3</td>
<td>Core 0 ETM</td>
<td>0x00040</td>
<td>0x00040003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY4</td>
<td>Core 1 Debug</td>
<td>0x00110</td>
<td>0x00110003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY5</td>
<td>Core 1 CTI</td>
<td>0x00120</td>
<td>0x00120003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY6</td>
<td>Core 1 PMU</td>
<td>0x00130</td>
<td>0x00130003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY7</td>
<td>Core 1 ETM</td>
<td>0x00140</td>
<td>0x00140003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY8</td>
<td>Core 2 Debug</td>
<td>0x00210</td>
<td>0x00210003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY9</td>
<td>Core 2 CTI</td>
<td>0x00220</td>
<td>0x00220003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY10</td>
<td>Core 2 PMU</td>
<td>0x00230</td>
<td>0x00230003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY11</td>
<td>Core 2 ETM</td>
<td>0x00240</td>
<td>0x00240003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY12</td>
<td>Core 3 Debug</td>
<td>0x00310</td>
<td>0x00310003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY13</td>
<td>Core 3 CTI</td>
<td>0x00320</td>
<td>0x00320003</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>If the component is present.</td>
</tr>
</tbody>
</table>
### Table C8-2 v8 ROMENTRY values (continued)

<table>
<thead>
<tr>
<th>Name</th>
<th>Debug component</th>
<th>Address offset [31:12]</th>
<th>ROMENTRY value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMENTRY14</td>
<td>Core 3 PMU</td>
<td>0x00330</td>
<td>0x00330003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY15</td>
<td>Core 3 ETM</td>
<td>0x00340</td>
<td>0x00340003</td>
<td>If the component is present.</td>
</tr>
</tbody>
</table>

### Table C8-3 Legacy v7 ROMENTRY values

<table>
<thead>
<tr>
<th>Name</th>
<th>Debug component</th>
<th>Address offset [31:12]</th>
<th>ROMENTRY value</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMENTRY0</td>
<td>Core 0 Debug</td>
<td>0x00010</td>
<td>0x00010003</td>
<td></td>
</tr>
<tr>
<td>ROMENTRY1</td>
<td>Core 0 PMU</td>
<td>0x00011</td>
<td>0x00011003</td>
<td></td>
</tr>
<tr>
<td>ROMENTRY2</td>
<td>Core 1 Debug</td>
<td>0x00012</td>
<td>0x00012003</td>
<td></td>
</tr>
<tr>
<td>ROMENTRY3</td>
<td>Core 1 PMU</td>
<td>0x00013</td>
<td>0x00013003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY4</td>
<td>Core 2 Debug</td>
<td>0x00014</td>
<td>0x00014003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY5</td>
<td>Core 2 PMU</td>
<td>0x00015</td>
<td>0x00015003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY6</td>
<td>Core 3 Debug</td>
<td>0x00016</td>
<td>0x00016003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY7</td>
<td>Core 3 PMU</td>
<td>0x00017</td>
<td>0x00017003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY8</td>
<td>Core 0 CTI</td>
<td>0x00018</td>
<td>0x00018003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY9</td>
<td>Core 1 CTI</td>
<td>0x00019</td>
<td>0x00019003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY10</td>
<td>Core 2 CTI</td>
<td>0x0001A</td>
<td>0x0001A003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY11</td>
<td>Core 3 CTI</td>
<td>0x0001B</td>
<td>0x0001B003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY12</td>
<td>Core 0 ETM</td>
<td>0x0001C</td>
<td>0x0001C003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>ROMENTRY13</td>
<td>Core 1 ETM</td>
<td>0x0001D</td>
<td>0x0001D003</td>
<td>If the component is present.</td>
</tr>
<tr>
<td>Name</td>
<td>Debug component</td>
<td>Address offset [31:12]</td>
<td>ROMENTRY value</td>
<td></td>
</tr>
<tr>
<td>--------------</td>
<td>----------------</td>
<td>------------------------</td>
<td>------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>ROMENTRY14</td>
<td>Core 2 ETM</td>
<td>0x001E</td>
<td>0x001E003 If the component is present.</td>
<td></td>
</tr>
<tr>
<td>ROMENTRY15</td>
<td>Core 3 ETM</td>
<td>0x001F</td>
<td>0x001F003 If the component is present.</td>
<td></td>
</tr>
</tbody>
</table>
C8.5  ROM Table Peripheral Identification Registers

The ROM Table Peripheral Identification Registers provide standard information required for all components that conform to the Arm Debug Interface Architecture Specification, ADIv5.0 to ADIv5.2. There are eight registers listed in register number order in the following table.

Table C8-4  Summary of the ROM Table Peripheral Identification Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMPIDR4</td>
<td>0x04</td>
<td>0xFD0</td>
</tr>
<tr>
<td>ROMPIDR5</td>
<td>0x00</td>
<td>0xFD4</td>
</tr>
<tr>
<td>ROMPIDR6</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>ROMPIDR7</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>ROMPIDR0</td>
<td>0xAB for v8 memory map. 0xE1 for v7 memory map.</td>
<td>0xFE0</td>
</tr>
<tr>
<td>ROMPIDR1</td>
<td>0xB4</td>
<td>0xFE4</td>
</tr>
<tr>
<td>ROMPIDR2</td>
<td>0x2B</td>
<td>0xFE8</td>
</tr>
<tr>
<td>ROMPIDR3</td>
<td>0x00</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Only bits[7:0] of each Peripheral ID Register are used, with bits[31:8] reserved. Together, the eight Peripheral ID Registers define a single 64-bit Peripheral ID.
C8.6 ROM Table Peripheral Identification Register 0

The ROMPIDR0 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

**Configurations**
The ROMPIDR0 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary* on page C8-454.

![Figure C8-2 ROMPIDR0 bit assignments](image-url)

[31:8]
Reserved, RES0.

**Part_0, [7:0]**
Least significant byte of the ROM table part number.

- `0x8A` For v8 memory map.
- `0xE1` For v7 memory map.

The ROMPIDR0 can be accessed through the external debug interface, offset `0xFE0`.

C1.4 External access permissions to debug registers on page C1-369 describes the condition codes.
C8.7  ROM Table Peripheral Identification Register 1

The ROMPIDR1 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMPIDR1 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary on page C8-454*.

![Figure C8-3 ROMPIDR1 bit assignments](image)

**[31:8]**
Reserved, `RES0`.

**DES_0, [7:4]**
0xB  Least significant nibble of JEP106 ID code. For Arm Limited.

**Part_1, [3:0]**
0x4  Most significant nibble of the ROM table part number.

The ROMPIDR1 can be accessed through the external debug interface, offset 0xFE4.
C8.8 ROM Table Peripheral Identification Register 2

The ROMPIDR2 characteristics are:

**Purpose**

Provides information to identify an external debug component.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**

The ROMPIDR2 is in the Debug power domain.

**Attributes**

See *C8.3 ROM table register summary* on page C8-454.

![Figure C8-4 ROMPIDR2 bit assignments](image)

[31:8]

Reserved, RES0.

**Revision**, [7:4]

0x2 r1p0.

JEDEC, [3]

0b1 RAO. Indicates a JEP106 identity code is used.

DES_1, [2:0]

0b011 Designer, most significant bits of JEP106 ID code. For Arm Limited.

The ROMPIDR2 can be accessed through the external debug interface, offset 0xFE8.
C8.9 ROM Table Peripheral Identification Register 3

The ROMPIDR3 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMPIDR3 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary on page C8-454*.

![Figure C8-5 ROMPIDR3 bit assignments](image)

[31:8]
Reserved, RES0.

REVAND, [7:4]
0x0 Part minor revision.

CMOD, [3:0]
0x0 Customer modified.

The ROMPIDR3 can be accessed through the external debug interface, offset 0xFEC.
C8.10 ROM Table Peripheral Identification Register 4

The ROMPIDR4 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th></th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMPIDR4 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary on page C8-454*.

![Figure C8-6 ROMPIDR4 bit assignments](image)

[31:8]  
Reserved, RES0.

Size, [7:4]  
0x0 Size of the component. Log2 the number of 4KB pages from the start of the component to the end of the component ID registers.

DES_2, [3:0]  
0x4 Designer, JEP106 continuation code, least significant nibble. For Arm Limited.

The ROMPIDR4 can be accessed through the external debug interface, offset 0xFD0.
C8.11 ROM Table Peripheral Identification Register 5-7

No information is held in the Peripheral ID5, Peripheral ID6, and Peripheral ID7 Registers. They are reserved for future use and are RES0.
C8.12 ROM Table Component Identification Registers

There are four read-only ROM Table Component Identification Registers, Component ID0 through Component ID3.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>ROMCIDR0</td>
<td>0x0D</td>
<td>0xFF0</td>
</tr>
<tr>
<td>ROMCIDR1</td>
<td>0x10</td>
<td>0xFF4</td>
</tr>
<tr>
<td>ROMCIDR2</td>
<td>0x05</td>
<td>0xFF8</td>
</tr>
<tr>
<td>ROMCIDR3</td>
<td>0xB1</td>
<td>0xFFC</td>
</tr>
</tbody>
</table>

The ROM Table Component Identification Registers identify Debug as an Arm Debug Interface v5 component.
C8.13 ROM Table Component Identification Register 0

The ROMCIDR0 characteristics are:

Purpose
Provides information to identify an external debug component.

Usage constraints
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

_C1.4 External access permissions to debug registers on page C1-369_ describes the condition codes.

Configurations
The ROMCIDR0 is in the Debug power domain.

Attributes
See _C8.3 ROM table register summary_ on page C8-454.

![Figure C8-7 ROMCIDR0 bit assignments](image)

<table>
<thead>
<tr>
<th>31</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRMBL_0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[31:8]
Reserved, RES0.

Size, [7:0]
0x0D  Preamble byte 0.

The ROMCIDR0 can be accessed through the external debug interface, offset 0xFF0.
C8.14 ROM Table Component Identification Register 1

The ROMCIDR1 characteristics are:

**Purpose**
Provided information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMCIDR1 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary on page C8-454*.

![Figure C8-8 ROMCIDR1 bit assignments](image)

<table>
<thead>
<tr>
<th>[31:8]</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th>[8]</th>
<th>[7]</th>
<th>[4]</th>
<th>[3]</th>
<th>[0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CLASS</td>
<td></td>
<td></td>
<td></td>
<td>PRMBL_1</td>
</tr>
</tbody>
</table>

[31:8]
Reserved, RES0.

**CLASS, [7:4]**
- 0x1 Component Class. For a ROM table.

**PRMBL_1, [3:0]**
- 0x0 Preamble.

The ROMCIDR1 can be accessed through the external debug interface, offset 0xFF4.
C8.15 ROM Table Component Identification Register 2

The ROMCIDR2 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMCIDR2 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary* on page C8-454.

![Figure C8-9 ROMCIDR2 bit assignments](image)

[31:8]
Reserved, RES0.

PRMBL_2, [7:0]
0x05 Preamble byte 2.

The ROMCIDR2 can be accessed through the external debug interface, offset 0xFF8.
C8.16 ROM Table Component Identification Register 3

The ROMCIDR3 characteristics are:

**Purpose**
Provides information to identify an external debug component.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C1.4 External access permissions to debug registers on page C1-369* describes the condition codes.

**Configurations**
The ROMCIDR3 is in the Debug power domain.

**Attributes**
See *C8.3 ROM table register summary on page C8-454.*

![Figure C8-10 ROMCIDR3 bit assignments](image)

[31:8]
Reserved, RES0.

PRMBL_3, [7:0]
0xB1 Preamble byte 3.

The ROMCIDR3 can be accessed through the external debug interface, offset 0xFFC.
Chapter C9
PMU registers

This chapter describes the PMU registers.

It contains the following sections:

- C9.1 AArch32 PMU register summary on page C9-472.
- C9.2 Performance Monitors Control Register on page C9-474.
- C9.3 Performance Monitors Common Event Identification Register 0 on page C9-477.
- C9.4 Performance Monitors Common Event Identification Register 1 on page C9-481.
- C9.5 Memory-mapped PMU register summary on page C9-483.
- C9.6 Performance Monitors Configuration Register on page C9-486.
- C9.8 Performance Monitors Peripheral Identification Register 0 on page C9-489.
- C9.9 Performance Monitors Peripheral Identification Register 1 on page C9-490.
- C9.11 Performance Monitors Peripheral Identification Register 3 on page C9-492.
- C9.15 Performance Monitors Component Identification Register 0 on page C9-496.
- C9.16 Performance Monitors Component Identification Register 1 on page C9-497.
- C9.18 Performance Monitors Component Identification Register 3 on page C9-499.
C9.1 AArch32 PMU register summary

The PMU counters and their associated control registers are accessible in the AArch32 Execution state from the internal CP15 system register interface with MCR and MRC instructions for 32-bit registers and MCRR and MRRC for 64-bit registers.

The following table gives a summary of the Cortex-A32 PMU registers in the AArch32 Execution state. For those registers not described in this chapter, see the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile.

See the C9.5 Memory-mapped PMU register summary on page C9-483 for a complete list of registers that are accessible from the external debug interface.

C9 PMU registers
C9.1 AArch32 PMU register summary

<table>
<thead>
<tr>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>0</td>
<td>PMCR</td>
<td>RW</td>
<td>32</td>
<td>C9.2 Performance Monitors Control Register on page C9-474</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>1</td>
<td>PMCNTENSET</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Count Enable Set Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>2</td>
<td>PMCNTENCLR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Count Enable Clear Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>3</td>
<td>PMOVSR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Overflow Flag Status Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>4</td>
<td>PMSWINC</td>
<td>WO</td>
<td>32</td>
<td>Performance Monitors Software Increment Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>5</td>
<td>PMSELR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Event Counter Selection Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>6</td>
<td>PMCEID0</td>
<td>RO</td>
<td>32</td>
<td>C9.3 Performance Monitors Common Event Identification Register 0 on page C9-477</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c12</td>
<td>7</td>
<td>PMCEID1</td>
<td>RO</td>
<td>32</td>
<td>C9.4 Performance Monitors Common Event Identification Register 1 on page C9-481</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c13</td>
<td>0</td>
<td>PMCCNTR[31:0]</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Cycle Count Register</td>
</tr>
<tr>
<td>-</td>
<td>0</td>
<td>c9</td>
<td>-</td>
<td>PMCCNTR[63:0]</td>
<td>RW</td>
<td>64</td>
<td></td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c13</td>
<td>1</td>
<td>PMXEVTYPERS</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Selected Event Type Register</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PMCCFILTR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Cycle Count Filter Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c13</td>
<td>2</td>
<td>PMXECNTR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Selected Event Count Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c14</td>
<td>0</td>
<td>PMUSERENR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors User Enable Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c14</td>
<td>1</td>
<td>PMINTENSET</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Interrupt Enable Set Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c14</td>
<td>2</td>
<td>PMINTENCLR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Interrupt Enable Clear Register</td>
</tr>
<tr>
<td>c9</td>
<td>0</td>
<td>c14</td>
<td>3</td>
<td>PMOVSSSET</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitor Overflow Flag Status Set Register</td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>0</td>
<td>PMEVCNTR0</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitor Event Count Registers</td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>1</td>
<td>PMEVCNTR1</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>2</td>
<td>PMEVCNTR2</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>3</td>
<td>PMEVCNTR3</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>4</td>
<td>PMEVCNTR4</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c8</td>
<td>5</td>
<td>PMEVCNTR5</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>
## Table C9-1  PMU register summary in the AArch32 Execution state (continued)

<table>
<thead>
<tr>
<th>CRn</th>
<th>Op1</th>
<th>CRm</th>
<th>Op2</th>
<th>Name</th>
<th>Type</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>0</td>
<td>PMEVTYPE0</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Event Type Registers</td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>1</td>
<td>PMEVTYPE1</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>2</td>
<td>PMEVTYPE2</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>3</td>
<td>PMEVTYPE3</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>4</td>
<td>PMEVTYPE4</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c12</td>
<td>5</td>
<td>PMEVTYPE5</td>
<td>RW</td>
<td>32</td>
<td></td>
</tr>
<tr>
<td>c14</td>
<td>0</td>
<td>c15</td>
<td>7</td>
<td>PMCCFILTR</td>
<td>RW</td>
<td>32</td>
<td>Performance Monitors Cycle Count Filter Register</td>
</tr>
</tbody>
</table>
C9.2 Performance Monitors Control Register

The PMCR characteristics are:

**Purpose**

Provides details of the Performance Monitors implementation, including the number of counters implemented, and configures and controls the counters.

**Usage constraints**

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0</th>
<th>EL0</th>
<th>EL1</th>
<th>EL1</th>
<th>EL2</th>
<th>EL3</th>
<th>EL3</th>
</tr>
</thead>
<tbody>
<tr>
<td>(NS)</td>
<td>(S)</td>
<td>(NS)</td>
<td>(S)</td>
<td>(SCR.NS = 1)</td>
<td>(SCR.NS = 0)</td>
<td></td>
</tr>
<tr>
<td>Config</td>
<td>Config</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
<td>RW</td>
</tr>
</tbody>
</table>

This register is accessible at EL0 when PMUSERENR_EL0.EN is set to 1.

**Configurations**

PMCR[6:0] is architecturally mapped to external PMCR_EL0 register.

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**

PMCR is a 32-bit register.

IMP, [31:24]

Implementer code:

0x41 Arm.

This is a read-only field.

IDCODE, [23:16]

Identification code:

0x06 Cortex-A32.

This is a read-only field.

N, [15:11]

Number of event counters.

0b00110 Six counters.

[10:7]

Reserved, RES0.

LC, [6]

Long cycle count enable. Determines which PMCCNTR bit generates an overflow recorded in PMOVSR[31]. The possible values are:

0 Overflow on increment that changes PMCCNTR[31] from 1 to 0.
Overflow on increment that changes PMCCNTR[63] from 1 to 0.

**DP, [5]**

Disable cycle counter, PMCCNTR when event counting is prohibited:

0  Cycle counter operates regardless of the non-invasive debug authentication settings. This is the reset value.

1  Cycle counter is disabled if non-invasive debug is not permitted and enabled.

This bit is read/write.

**X, [4]**

Export enable. This bit permits events to be exported to another debug device, such as a trace macrocell, over an event bus:

0  Export of events is disabled. This is the reset value.

1  Export of events is enabled.

This bit is read/write and does not affect the generation of Performance Monitors interrupts on the nPMUIRQ pin.

**D, [3]**

Clock divider:

0  When enabled, PMCCNTR counts every clock cycle. This is the reset value.

1  When enabled, PMCCNTR counts every 64 clock cycles.

This bit is read/write.

**C, [2]**

Clock counter reset. This bit is WO. The effects of writing to this bit are:

0  No action. This is the reset value.

1  Reset PMCCNTR_EL0 to 0.

This bit is always RAZ.

Resetting PMCCNTR does not clear the PMCCNTR overflow bit to 0. See the *Arm*® Architecture Reference Manual *Armv8, for Armv8-A architecture profile* for more information.

**P, [1]**

Event counter reset. This bit is WO. The effects of writing to this bit are:

0  No action. This is the reset value.

1  Reset all event counters, not including PMCCNTR, to zero.

This bit is always RAZ.

In Non-secure EL0 and EL1, a write of 1 to this bit does not reset event counters that HDCR.HPMN reserves for EL2 use.

In EL2 and EL3, a write of 1 to this bit resets all the event counters.

Resetting the event counters does not clear any overflow bits to 0.

**E, [0]**

Enable. The possible values of this bit are:

0  All counters, including PMCCNTR, are disabled. This is the reset value.

1  All counters are enabled.
This bit is RW.

In Non-secure EL0 and EL1, this bit does not affect the operation of event counters that HDCR_EL2.HPMN reserves for EL2 use.

On Warm reset, the field resets to 0.

To access the PMCR:

```
MRC p15,0,<Rt>,c9,c12,0 ; Read PMCR into Rt
MCR p15,0,<Rt>,c9,c12,0 ; Write Rt to PMCR
```

The PMCR can be accessed through the external debug interface, offset 0xE04.
C9.3 Performance Monitors Common Event Identification Register 0

The PMCEID0 characteristics are:

**Purpose**
Defines which common architectural and common microarchitectural feature events are implemented.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Config</td>
<td>Config</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

This register is accessible at EL0 when PMUSERENR_EL0.EN is set to 1.

**Configurations**
The PMCEID0 is architecturally mapped to the external register PMCEID0_EL0.

There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
PMCEID0 is a 32-bit register.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Event number</th>
<th>Event mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31]</td>
<td>0x1F</td>
<td>L1D_CACHE_ALLOCATE</td>
<td>L1 Data cache allocate: 0 This event is not implemented.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[30]</td>
<td>0x1F</td>
<td>CHAIN</td>
<td>Chain. For odd-numbered counters, counts once for each overflow of the preceding even-numbered counter. For even-numbered counters, does not count: 1 This event is implemented.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[29]</td>
<td>0x1D</td>
<td>BUS_CYCLES</td>
<td>Bus cycle: 1 This event is implemented.</td>
</tr>
<tr>
<td>Bit</td>
<td>Event number</td>
<td>Event mnemonic</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>--------------</td>
<td>-------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>28</td>
<td>0x1C</td>
<td>TTBR_WRITE_RETIRED</td>
<td>TTBR write, architecturally executed, condition check pass - write to translation table base:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 This event is not implemented.</td>
</tr>
<tr>
<td>27</td>
<td>0x1B</td>
<td>INST_SPEC</td>
<td>Instruction speculatively executed:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>26</td>
<td>0x1A</td>
<td>MEMORY_ERROR</td>
<td>Local memory error:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>25</td>
<td>0x19</td>
<td>BUS_ACCESS</td>
<td>Bus access:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>24</td>
<td>0x18</td>
<td>L2D_CACHE_WB</td>
<td>L2 Data cache Write-Back:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 This event is not implemented if the Cortex-A32 processor has been configured without an L2 cache.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented if the Cortex-A32 processor has been configured with an L2 cache.</td>
</tr>
<tr>
<td>23</td>
<td>0x17</td>
<td>L2D_CACHE_REFILL</td>
<td>L2 Data cache refill:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 This event is not implemented if the Cortex-A32 processor has been configured without an L2 cache.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented if the Cortex-A32 processor has been configured with an L2 cache.</td>
</tr>
<tr>
<td>22</td>
<td>0x16</td>
<td>L2D_CACHE</td>
<td>L2 Data cache access:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0 This event is not implemented if the Cortex-A32 processor has been configured without an L2 cache.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented if the Cortex-A32 processor has been configured with an L2 cache.</td>
</tr>
<tr>
<td>21</td>
<td>0x15</td>
<td>L1D_CACHE_WB</td>
<td>L1 Data cache Write-Back:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>20</td>
<td>0x14</td>
<td>L1I_CACHE</td>
<td>L1 Instruction cache access:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>19</td>
<td>0x13</td>
<td>MEM_ACCESS</td>
<td>Data memory access:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>18</td>
<td>0x12</td>
<td>BR_PRED</td>
<td>Predictable branch speculatively executed:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>Bit</td>
<td>Event number</td>
<td>Event mnemonic</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>--------------</td>
<td>----------------</td>
<td>-------------</td>
</tr>
</tbody>
</table>
| [17] | 0x11         | CPU_CYCLES     | Cycle:  
1   This event is implemented. |
| [16] | 0x10         | BR_MIS_PRED    | Mispredicted or not predicted branch speculatively executed:  
1   This event is implemented. |
| [15] | 0x0F         | UNALIGNED_LDST_RETIRED | Instruction architecturally executed, condition check pass - unaligned load or store:  
1   This event is implemented. |
| [14] | 0x0E         | BR_RETURN_RETIRED | Instruction architecturally executed, condition check pass - procedure return:  
0   This event is not implemented. |
| [13] | 0x0D         | BR_IMMED_RETIRED | Instruction architecturally executed - immediate branch:  
1   This event is implemented. |
| [12] | 0x0C         | PC_WRITE_RETIRED | Instruction architecturally executed, condition check pass - software change of the PC:  
1   This event is implemented. |
| [11] | 0x0B         | CID_WRITE_RETIRED | Instruction architecturally executed, condition check pass - write to CONTEXTIDR:  
1   This event is implemented. |
| [10] | 0x0A         | EXC_RETURN     | Instruction architecturally executed, condition check pass - exception return:  
1   This event is implemented. |
| [9]  | 0x09         | EXC_TAKEN      | Exception taken:  
1   This event is implemented. |
| [8]  | 0x08         | INST_RETIRED   | Instruction architecturally executed:  
1   This event is implemented. |
| [7]  | 0x07         | ST_RETIRED     | Instruction architecturally executed, condition check pass - store:  
1   This event is implemented. |
| [6]  | 0x06         | LD_RETIRED     | Instruction architecturally executed, condition check pass - load:  
1   This event is implemented. |
| [5]  | 0x05         | L1D_TLB_REFILL | L1 Data TLB refill:  
1   This event is implemented. |
<table>
<thead>
<tr>
<th>Bit</th>
<th>Event number</th>
<th>Event mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[4]</td>
<td>0x04</td>
<td>L1D_CACHE</td>
<td>L1 Data cache access:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>[3]</td>
<td>0x03</td>
<td>L1D_CACHE_REFILL</td>
<td>L1 Data cache refill:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>[2]</td>
<td>0x02</td>
<td>L1I_TLB_REFILL</td>
<td>L1 Instruction TLB refill:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>[1]</td>
<td>0x01</td>
<td>L1I_CACHE_REFILL</td>
<td>L1 Instruction cache refill:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
<tr>
<td>[0]</td>
<td>0x00</td>
<td>SW_INCR</td>
<td>Instruction architecturally executed, condition check pass - software increment:</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>1 This event is implemented.</td>
</tr>
</tbody>
</table>

To access the PMCEID0:

```assembly
MRC p15,0,<Rt>,c9,c12,6 ; Read PMCEID0 into Rt
```

The PMCEID0 can be accessed through the external debug interface, offset 0xE20.
C9.4 Performance Monitors Common Event Identification Register 1

The PMCEID1 characteristics are:

**Purpose**
Defines which common architectural and common microarchitectural feature events are implemented.

**Usage constraints**
This register is accessible as follows:

<table>
<thead>
<tr>
<th>Access Level</th>
<th>Mask</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0</td>
<td>(NS)</td>
<td>EL0</td>
</tr>
<tr>
<td>EL0</td>
<td>(S)</td>
<td>EL0</td>
</tr>
<tr>
<td>EL1</td>
<td>(NS)</td>
<td>EL1</td>
</tr>
<tr>
<td>EL1</td>
<td>(S)</td>
<td>EL1</td>
</tr>
<tr>
<td>EL2</td>
<td>(SCR.NS = 1)</td>
<td>EL2</td>
</tr>
<tr>
<td>EL3</td>
<td>(SCR.NS = 0)</td>
<td>EL3</td>
</tr>
</tbody>
</table>

This register is accessible at EL0 when PMUSERENR_EL0.EN is set to 1

**Configurations**
The PMCEID1 is architecturally mapped to the external register PMCEID1_EL0.
There is one copy of this register that is used in both Secure and Non-secure states.

**Attributes**
PMCEID1 is a 32-bit register.

![Figure C9-3 PMCEID1 bit assignments](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Event number</th>
<th>Event mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[16]</td>
<td>0x30</td>
<td>L2I_TLB</td>
<td>Attributable Level 2 instruction TLB access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ This event is not implemented.</td>
</tr>
<tr>
<td>[15]</td>
<td>0x2F</td>
<td>L2D_TLB</td>
<td>Attributable Level 2 data or unified TLB access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ This event is not implemented.</td>
</tr>
<tr>
<td>[14]</td>
<td>0x2E</td>
<td>L2I_TLB_REFILL</td>
<td>Attributable Level 2 instruction TLB refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ This event is not implemented.</td>
</tr>
<tr>
<td>[13]</td>
<td>0x2D</td>
<td>L2D_TLB_REFIL</td>
<td>Attributable Level 2 data or unified TLB refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ This event is not implemented.</td>
</tr>
<tr>
<td>Bit</td>
<td>Event number</td>
<td>Event mnemonic</td>
<td>Description</td>
</tr>
<tr>
<td>-----</td>
<td>--------------</td>
<td>----------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>12</td>
<td>0x2C</td>
<td>L3D_CACHE_WB</td>
<td>Attributable Level 3 data or unified cache write-back.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>11</td>
<td>0x2B</td>
<td>L3D_CACHE</td>
<td>Attributable Level 3 data or unified cache access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>10</td>
<td>0x2A</td>
<td>L3D_CACHE_REFILL</td>
<td>Attributable Level 3 data or unified cache refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>9</td>
<td>0x29</td>
<td>L3D_CACHE_ALLOCATE</td>
<td>Attributable Level 3 data or unified cache allocation without refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>8</td>
<td>0x28</td>
<td>L2I_CACHE_REFILL</td>
<td>Attributable Level 2 instruction cache refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>7</td>
<td>0x27</td>
<td>L2I_CACHE</td>
<td>Attributable Level 2 instruction cache access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>6</td>
<td>0x26</td>
<td>L1I_TLB</td>
<td>Level 1 instruction TLB access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>5</td>
<td>0x25</td>
<td>L1D_TLB</td>
<td>Level 1 data or unified TLB access.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>4</td>
<td>0x24</td>
<td>STALL_BACKEND</td>
<td>No operation issued due to backend.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>3</td>
<td>0x23</td>
<td>STALL_FRONTEND</td>
<td>No operation issued due to the frontend.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>2</td>
<td>0x22</td>
<td>BR_MIS_PRED RETIRED</td>
<td>Instruction architecturally executed, mispredicted branch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>1</td>
<td>0x21</td>
<td>BR RETIRED</td>
<td>Instruction architecturally executed, branch.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
<tr>
<td>0</td>
<td>0x20</td>
<td>L2D_CACHE_ALLOCATE</td>
<td>Level 2 data cache allocation without refill.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>θ  This event is not implemented.</td>
</tr>
</tbody>
</table>

To access the PMCEID1:

```
MRC p15,0,<Rt>,c9,c12,7 ; Read PMCEID1 into Rt
```

The PMCEID1 can be accessed through the external debug interface, offset 0xE24.
### C9.5 Memory-mapped PMU register summary

There are PMU registers that are accessible through the external debug interface.

These registers are listed in the following table. For those registers not described in this chapter, see the *Arm® Architecture Reference Manual* Armv8, for Armv8-A architecture profile.

#### Table C9-4 Memory-mapped PMU register summary

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>PMEVCNTR0_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 0</td>
</tr>
<tr>
<td>0x004</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x008</td>
<td>PMEVCNTR1_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 1</td>
</tr>
<tr>
<td>0x00C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x010</td>
<td>PMEVCNTR2_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 2</td>
</tr>
<tr>
<td>0x014</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x018</td>
<td>PMEVCNTR3_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 3</td>
</tr>
<tr>
<td>0x01C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x020</td>
<td>PMEVCNTR4_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 4</td>
</tr>
<tr>
<td>0x024</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x028</td>
<td>PMEVCNTR5_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Count Register 5</td>
</tr>
<tr>
<td>0x02C-0xF4</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x0F8</td>
<td>PMCCNTR_EL0[31:0]</td>
<td>RW</td>
<td>Performance Monitors Cycle Count Register</td>
</tr>
<tr>
<td>0x0FC</td>
<td>PMCCNTR_EL0[63:32]</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x100-0x3FC</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x400</td>
<td>PMEVTYPER0_EL0</td>
<td>RW</td>
<td>Performance Monitors Event Type Register</td>
</tr>
<tr>
<td>0x404</td>
<td>PMEVTYPER1_EL0</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x408</td>
<td>PMEVTYPER2_EL0</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x40C</td>
<td>PMEVTYPER3_EL0</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x410</td>
<td>PMEVTYPER4_EL0</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x414</td>
<td>PMEVTYPER5_EL0</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x418-0x478</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x47C</td>
<td>PMCCFILTR_EL0</td>
<td>RW</td>
<td>Performance Monitors Cycle Count Filter Register</td>
</tr>
<tr>
<td>0x480-0x8FC</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xC00</td>
<td>PMCNTENSET_EL0</td>
<td>RW</td>
<td>Performance Monitors Count Enable Set Register</td>
</tr>
<tr>
<td>0xC04-0xC1C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xC20</td>
<td>PMCNTENCLR_EL0</td>
<td>RW</td>
<td>Performance Monitors Count Enable Clear Register</td>
</tr>
<tr>
<td>0xC24-0xC3C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0xC40</td>
<td>PMINTENSET_EL1</td>
<td>RW</td>
<td>Performance Monitor Interrupt Enable Set Register</td>
</tr>
<tr>
<td>0xC44-0xC5C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xC60</td>
<td>PMINTENCLR_EL1</td>
<td>RW</td>
<td>Performance Monitors Interrupt Enable Clear Register</td>
</tr>
<tr>
<td>0xC64-0xC7C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xC80</td>
<td>PMOVSCLR_EL0</td>
<td>RW</td>
<td>Performance Monitors Overflow Flag Status Register</td>
</tr>
<tr>
<td>0xC84-0xC9C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xCA0</td>
<td>PMSWINC_EL0</td>
<td>WO</td>
<td>Performance Monitor Software Increment Register</td>
</tr>
<tr>
<td>0xCA4-0xCB0</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xCC0</td>
<td>PMOVSCSET_EL0</td>
<td>RW</td>
<td>Performance Monitors Overflow Flag Status Set Register</td>
</tr>
<tr>
<td>0xCC4-0xCDF</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xE00</td>
<td>PMCFGR</td>
<td>RO</td>
<td>C9.6 Performance Monitors Configuration Register on page C9-486</td>
</tr>
<tr>
<td>0xE04</td>
<td>PMCR_EL0</td>
<td>RW</td>
<td>Performance Monitors Control Register</td>
</tr>
<tr>
<td>0xE08-0xEE8</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xE20</td>
<td>PMCEID0_EL0</td>
<td>RO</td>
<td>C9.3 Performance Monitors Common Event Identification Register 0 on page C9-477</td>
</tr>
<tr>
<td>0xE24</td>
<td>PMCEID1_EL0</td>
<td>RO</td>
<td>C9.4 Performance Monitors Common Event Identification Register 1 on page C9-481</td>
</tr>
<tr>
<td>0xE28-0xFE4</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFA0</td>
<td>PMDEV AFF0</td>
<td>RO</td>
<td>Performance Monitors Device Affinity Register 0, see B1.97 Multiprocessor Affinity Register on page B1-309</td>
</tr>
<tr>
<td>0xFB0</td>
<td>PMLAR</td>
<td>WO</td>
<td>Performance Monitors Lock Access Register</td>
</tr>
<tr>
<td>0xFB4</td>
<td>PMLSR</td>
<td>RO</td>
<td>Performance Monitors Lock Status Register</td>
</tr>
<tr>
<td>0xFB8</td>
<td>PMAUTHSTATUS</td>
<td>RO</td>
<td>Performance Monitors Authentication Status Register</td>
</tr>
<tr>
<td>0xFC0-0xFC8</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFC0</td>
<td>PMDEVTYPE</td>
<td>RO</td>
<td>Performance Monitors Device Type Register</td>
</tr>
<tr>
<td>0xFD0</td>
<td>PMPIDR4</td>
<td>RO</td>
<td>C9.12 Performance Monitors Peripheral Identification Register 4 on page C9-493</td>
</tr>
<tr>
<td>0xFD4</td>
<td>PMPIDR5</td>
<td>RO</td>
<td>C9.13 Performance Monitors Peripheral Identification Register 5-7 on page C9-494</td>
</tr>
<tr>
<td>0xFD8</td>
<td>PMPIDR6</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFD0</td>
<td>PMPIDR7</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFE0</td>
<td>PMPIDR0</td>
<td>RO</td>
<td>C9.8 Performance Monitors Peripheral Identification Register 0 on page C9-489</td>
</tr>
<tr>
<td>0xFE4</td>
<td>PMPIDR1</td>
<td>RO</td>
<td>C9.9 Performance Monitors Peripheral Identification Register 1 on page C9-490</td>
</tr>
<tr>
<td>0xFE8</td>
<td>PMPIDR2</td>
<td>RO</td>
<td>C9.10 Performance Monitors Peripheral Identification Register 2 on page C9-491</td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>--------</td>
<td>--------</td>
<td>------</td>
<td>-------------------------------------------------------------------</td>
</tr>
<tr>
<td>0xFEC</td>
<td>PMPIDR3</td>
<td>RO</td>
<td><a href="#">C9.11 Performance Monitors Peripheral Identification Register 3 on page C9-492</a></td>
</tr>
<tr>
<td>0xFF0</td>
<td>PMCIDR0</td>
<td>RO</td>
<td><a href="#">C9.15 Performance Monitors Component Identification Register 0 on page C9-496</a></td>
</tr>
<tr>
<td>0xFF4</td>
<td>PMCIDR1</td>
<td>RO</td>
<td><a href="#">C9.16 Performance Monitors Component Identification Register 1 on page C9-497</a></td>
</tr>
<tr>
<td>0xFF8</td>
<td>PMCIDR2</td>
<td>RO</td>
<td><a href="#">C9.17 Performance Monitors Component Identification Register 2 on page C9-498</a></td>
</tr>
<tr>
<td>0xFFC</td>
<td>PMCIDR3</td>
<td>RO</td>
<td><a href="#">C9.18 Performance Monitors Component Identification Register 3 on page C9-499</a></td>
</tr>
</tbody>
</table>
C9.6 Performance Monitors Configuration Register

The PMCFGR characteristics are:

**Purpose**
Contains PMU specific configuration data.

**Usage constraints**

The accessibility to the PMCFGR by condition code is:

<table>
<thead>
<tr>
<th>Condition Code</th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>Error</td>
<td>Error</td>
<td>Error</td>
<td>Error</td>
<td>RO</td>
<td>RO</td>
<td></td>
</tr>
</tbody>
</table>

*See [C2.2 External register access permissions to the PMU registers](#) on page C2-377 describes the condition codes.*

**Configurations**
The PMCFGR is in the processor power domain.

**Attributes**

See [C9.5 Memory-mapped PMU register summary](#) on page C9-483.

![Figure C9-4 PMCFGR bit assignments](#)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:17]</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>EX, [16]</td>
<td>Export supported</td>
<td>1 Export is supported. PMCR_EL0.EX is read/write.</td>
</tr>
<tr>
<td>CCD, [15]</td>
<td>Cycle counter has pre-scale</td>
<td>1 PMCR_EL0.D is read/write.</td>
</tr>
<tr>
<td>CC, [14]</td>
<td>Dedicated cycle counter supported</td>
<td>1 Dedicated cycle counter is supported.</td>
</tr>
<tr>
<td>Size, [13:8]</td>
<td>Counter size</td>
<td>0b111111 64-bit counters.</td>
</tr>
<tr>
<td>N, [7:0]</td>
<td>Number of event counters</td>
<td>0x06 Six counters.</td>
</tr>
</tbody>
</table>
The PMCFGR can be accessed through the external debug interface, offset 0xE00.
C9.7 Performance Monitors Peripheral Identification Registers

The Performance Monitors Peripheral Identification Registers provide standard information required for all components that conform to the Arm PMUv3 architecture.

The following table lists the Performance Monitors Peripheral Identification Registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peripheral ID4</td>
<td>0x04</td>
<td>0xFD0</td>
</tr>
<tr>
<td>Peripheral ID5</td>
<td>0x00</td>
<td>0xFD4</td>
</tr>
<tr>
<td>Peripheral ID6</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>Peripheral ID7</td>
<td>0x00</td>
<td>0xFDC</td>
</tr>
<tr>
<td>Peripheral ID0</td>
<td>0xDB</td>
<td>0xFE0</td>
</tr>
<tr>
<td>Peripheral ID1</td>
<td>0xB9</td>
<td>0xFE4</td>
</tr>
<tr>
<td>Peripheral ID2</td>
<td>0x2B</td>
<td>0xFE8</td>
</tr>
<tr>
<td>Peripheral ID3</td>
<td>0x00</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Only bits[7:0] of each Peripheral ID Register are used, with bits[31:8] reserved. Together, the eight Peripheral ID Registers define a single 64-bit Peripheral ID.
C9.8 Performance Monitors Peripheral Identification Register 0

The PMPIDR0 characteristics are:

**Purpose**
- Provides information to identify a Performance Monitor component.

**Usage constraints**
- The PMPIDR0 can be accessed through the external debug interface.
- The accessibility to the PMPIDR0 by condition code is:
  
<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C2.2 External register access permissions to the PMU registers on page C2-377* describes the condition codes.

**Configurations**
- The PMPIDR0 is in the Debug power domain.

**Attributes**
- See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483.*

![Figure C9-5 PMPIDR0 bit assignments](image)

[31:8] Reserve, RES0.

**Part_0, [7:0]**
- 0xDB  Least significant byte of the performance monitor part number.

The PMPIDR0 can be accessed through the external debug interface, offset 0xFE0.
C9.9 Performance Monitors Peripheral Identification Register 1

The PMPIDR1 characteristics are:

**Purpose**
Provides information to identify a Performance Monitor component.

**Usage constraints**
The PMPIDR1 can be accessed through the external debug interface.

The accessibility to the PMPIDR1 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

* C2.2 External register access permissions to the PMU registers on page C2-377 describes the condition codes.

**Configurations**
The PMPIDR1 is in the Debug power domain.

**Attributes**
See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483*.

![Figure C9-6 PMPIDR1 bit assignments](image)

**Bit assignments**

- [31:8] Reserved, RES0.
- DES_0, [7:4]
  - 0x8 Arm Limited. This is the least significant nibble of JEP106 ID code.
- Part_1, [3:0]
  - 0x9 Most significant nibble of the performance monitor part number.

The PMPIDR1 can be accessed through the external debug interface, offset 0xFE4.
C9.10 Performance Monitors Peripheral Identification Register 2

The PMPIDR2 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

**Usage constraints**

The accessibility to the PMPIDR2 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C2.2 External register access permissions to the PMU registers on page C2-377* describes the condition codes.

The PMPIDR2 can be accessed through the external debug interface.

**Configurations**

The PMPIDR2 is in the Debug power domain.

**Attributes**

See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483.*

![Figure C9-7  PMPIDR2 bit assignments](image)

- **Reserved, RES0.**
- **Revision, [7:4]**
  - 0x2 r1p0.
- **JEDEC, [3]**
  - 0b1 RAO. Indicates a JEP106 identity code is used.
- **DES_1, [2:0]**
  - 0b11 Arm Limited. This is the most significant nibble of JEP106 ID code.

The PMPIDR2 can be accessed through the external debug interface, offset 0xFE8.
C9.11 Performance Monitors Peripheral Identification Register 3

The PMPIDR3 characteristics are:

Purpose
Provides information to identify a Performance Monitor component.

Usage constraints
The PMPIDR3 can be accessed through the external debug interface.

The accessibility to the PMPIDR3 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

C2.2 External register access permissions to the PMU registers on page C2-377 describes the condition codes.

Configurations
The PMPIDR3 is in the Debug power domain.

Attributes
See the register summary in C9.5 Memory-mapped PMU register summary on page C9-483.

![PMPIDR3 bit assignments](image)

Figure C9-8 PMPIDR3 bit assignments

[31:8]
Reserved, RES0.

REVAND, [7:4]
0x0 Part minor revision.

CMOD, [3:0]
0x0 Customer modified.

The PMPIDR3 can be accessed through the external debug interface, offset 0xFEC.
C9.12 Performance Monitors Peripheral Identification Register 4

The PMPIDR4 characteristics are:

**Purpose**
Provides information to identify a Performance Monitor component.

**Usage constraints**
The PMPIDR4 can be accessed through the external debug interface.
The accessibility to the PMPIDR4 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C2.2 External register access permissions to the PMU registers on page C2-377* describes the condition codes.

**Configurations**
The PMPIDR4 is in the Debug power domain.

**Attributes**
See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483.*

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure C9-9 PMPIDR4 bit assignments
```

[31:8]
Reserved, RES0.

**Size, [7:4]**

0x0  Size of the component. Log2 the number of 4KB pages from the start of the component to the end of the component ID registers.

**DES_2, [3:0]**

0x4  Arm Limited. This is the least significant nibble JEP106 continuation code.

The PMPIDR4 can be accessed through the external debug interface, offset 0xFD0.
C9.13 Performance Monitors Peripheral Identification Register 5-7

No information is held in the Peripheral ID5, Peripheral ID6, and Peripheral ID7 Registers. They are reserved for future use and are RES0.
C9.14 Performance Monitors Component Identification Registers

There are four read-only PMU Component Identification Registers, Component ID0 through Component ID3.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component ID0</td>
<td>0x0D</td>
<td>0xFF0</td>
</tr>
<tr>
<td>Component ID1</td>
<td>0x90</td>
<td>0xFF4</td>
</tr>
<tr>
<td>Component ID2</td>
<td>0x05</td>
<td>0xFF8</td>
</tr>
<tr>
<td>Component ID3</td>
<td>0xB1</td>
<td>0xFFC</td>
</tr>
</tbody>
</table>

The Performance Monitors Component Identification Registers identify Performance Monitor as Arm PMUv3 architecture.
C9.15 Performance Monitors Component Identification Register 0

The PMCIDR0 characteristics are:

**Purpose**
Provides information to identify a Performance Monitor component.

**Usage constraints**
The PMCIDR0 can be accessed through the external debug interface.

The accessibility to the PMCIDR0 by condition code is:

<table>
<thead>
<tr>
<th>Condition Code</th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

_C2.2 External register access permissions to the PMU registers on page C2-377 describes the condition codes._

**Configurations**
The PMCIDR0 is in the Debug power domain.

**Attributes**
See the register summary in _C9.5 Memory-mapped PMU register summary on page C9-483._

![Figure C9-10 PMCIDR0 bit assignments](image)

<table>
<thead>
<tr>
<th></th>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>21</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>PRMLB_0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**[31:8]**
Reserved, RES0.

**Size, [7:0]**
0x0D Preamble byte 0.

The PMCIDR0 can be accessed through the external debug interface, offset 0xFF0.
C9.16 Performance Monitors Component Identification Register 1

The PMCIDR1 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

**Usage constraints**

The PMCIDR1 can be accessed through the external debug interface.

The accessibility to the PMCIDR1 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C2.2 External register access permissions to the PMU registers on page C2-377* describes the condition codes.

**Configurations**

The PMCIDR1 is in the Debug power domain.

**Attributes**

See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483.*

![Figure C9-11  PMCIDR1 bit assignments](image-url)

**[31:8]**

Reserved, RES0.

**CLASS, [7:4]**

0x9  Debug component.

**PRMBL_1, [3:0]**

0x0  Preamble byte 1.

The PMCIDR1 can be accessed through the external debug interface, offset 0xFF4.
C9.17 Performance Monitors Component Identification Register 2

The PMCIDR2 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

**Usage constraints**

The PMCIDR2 can be accessed through the external debug interface.

The accessibility to the PMCIDR2 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C2.2 External register access permissions to the PMU registers on page C2-377 describes the condition codes.*

**Configurations**

The PMCIDR2 is in the Debug power domain.

**Attributes**

See the register summary in *C9.5 Memory-mapped PMU register summary on page C9-483.*

![Figure C9-12 PMCIDR2 bit assignments](image)

<table>
<thead>
<tr>
<th>[31:8]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**PRMLB_2, [7:0]**

0x05  Preamble byte 2.

The PMCIDR2 can be accessed through the external debug interface, offset 0xFFF8.
C9.18 Performance Monitors Component Identification Register 3

The PMCIDR3 characteristics are:

Purpose
Provides information to identify a Performance Monitor component.

Usage constraints
The PMCIDR3 can be accessed through the external debug interface.

The accessibility to the PMCIDR3 by condition code is:

<table>
<thead>
<tr>
<th>Condition Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
</tr>
<tr>
<td>DLK</td>
</tr>
<tr>
<td>OSLK</td>
</tr>
<tr>
<td>EPMAD</td>
</tr>
<tr>
<td>SLK</td>
</tr>
<tr>
<td>Default</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

C2.2 External register access permissions to the PMU registers on page C2-377 describes the condition codes.

Configurations
The PMCIDR3 is in the Debug power domain.

Attributes
See the register summary in C9.5 Memory-mapped PMU register summary on page C9-483.

[31:8]
Reserved, RES0.

PRMBL_3, [7:0]

0xB1 Preamble byte 3.

The PMCIDR3 can be accessed through the external debug interface, offset 0xFFF.C.
C9 PMU registers

C9.18 Performance Monitors Component Identification Register 3
This chapter describes the ETM registers.

It contains the following sections:

- C10.1 ETM register summary on page C10-503.
- C10.2 Programming Control Register on page C10-506.
- C10.3 Status Register on page C10-507.
- C10.4 Trace Configuration Register on page C10-508.
- C10.5 Branch Broadcast Control Register on page C10-510.
- C10.6 Auxiliary Control Register on page C10-511.
- C10.7 Event Control 0 Register on page C10-513.
- C10.8 Event Control 1 Register on page C10-515.
- C10.9 Stall Control Register on page C10-516.
- C10.10 Global Timestamp Control Register on page C10-517.
- C10.11 Synchronization Period Register on page C10-518.
- C10.12 Cycle Count Control Register on page C10-519.
- C10.13 Trace ID Register on page C10-520.
- C10.14 ViewInst Main Control Register on page C10-521.
- C10.15 ViewInst Include-Exclude Control Register on page C10-523.
- C10.16 ViewInst Start-Stop Control Register on page C10-524.
- C10.17 Sequencer State Transition Control Registers 0-2 on page C10-525.
- C10.18 Sequencer Reset Control Register on page C10-527.
- C10.19 Sequencer State Register on page C10-528.
- C10.20 External Input Select Register on page C10-529.
- C10.21 Counter Reload Value Registers 0-1 on page C10-530.
- C10.22 Counter Control Register 0 on page C10-531.
- C10.23 Counter Control Register 1 on page C10-533.
• C10.24 Counter Value Registers 0-1 on page C10-535.
• C10.25 ID Register 8 on page C10-536.
• C10.26 ID Register 9 on page C10-537.
• C10.27 ID Register 10 on page C10-538.
• C10.28 ID Register 11 on page C10-539.
• C10.29 ID Register 12 on page C10-540.
• C10.30 ID Register 13 on page C10-541.
• C10.31 Implementation Specific Register 0 on page C10-542.
• C10.32 ID Register 0 on page C10-543.
• C10.33 ID Register 1 on page C10-545.
• C10.34 ID Register 2 on page C10-546.
• C10.35 ID Register 3 on page C10-548.
• C10.36 ID Register 4 on page C10-550.
• C10.37 ID Register 5 on page C10-552.
• C10.38 Resource Selection Control Registers 2-16 on page C10-554.
• C10.39 Single-Shot Comparator Control Register 0 on page C10-555.
• C10.40 Single-Shot Comparator Status Register 0 on page C10-556.
• C10.41 OS Lock Access Register on page C10-557.
• C10.42 OS Lock Status Register on page C10-558.
• C10.43 Power Down Control Register on page C10-559.
• C10.44 Power Down Status Register on page C10-560.
• C10.45 Address Comparator Value Registers 0-7 on page C10-561.
• C10.46 Address Comparator Access Type Registers 0-7 on page C10-562.
• C10.47 Context ID Comparator Value Register 0 on page C10-564.
• C10.48 VMID Comparator Value Register 0 on page C10-565.
• C10.49 Context ID Comparator Control Register 0 on page C10-566.
• C10.50 Integration ATB Identification Register on page C10-567.
• C10.51 Integration Instruction ATB Data Register on page C10-568.
• C10.52 Integration Instruction ATB In Register on page C10-569.
• C10.53 Integration Instruction ATB Out Register on page C10-570.
• C10.54 Integration Mode Control Register on page C10-571.
• C10.55 Claim Tag Set Register on page C10-572.
• C10.56 Claim Tag Clear Register on page C10-573.
• C10.57 Device Affinity Register 0 on page C10-574.
• C10.58 Device Affinity Register 1 on page C10-576.
• C10.59 Software Lock Access Register on page C10-577.
• C10.60 Software Lock Status Register on page C10-578.
• C10.61 Authentication Status Register on page C10-579.
• C10.62 Device Architecture Register on page C10-580.
• C10.63 Device ID Register on page C10-581.
• C10.64 Device Type Register on page C10-582.
• C10.65 ETM Peripheral Identification Registers on page C10-583.
• C10.66 ETM Peripheral Identification Register 0 on page C10-584.
• C10.67 ETM Peripheral Identification Register 1 on page C10-585.
• C10.68 ETM Peripheral Identification Register 2 on page C10-586.
• C10.69 ETM Peripheral Identification Register 3 on page C10-587.
• C10.70 ETM Peripheral Identification Register 4 on page C10-588.
• C10.71 ETM Peripheral Identification Register 5-7 on page C10-589.
• C10.72 ETM Component Identification Registers on page C10-590.
• C10.73 ETM Component Identification Register 0 on page C10-591.
• C10.74 ETM Component Identification Register 1 on page C10-592.
• C10.75 ETM Component Identification Register 2 on page C10-593.
• C10.76 ETM Component Identification Register 3 on page C10-594.
C10.1 ETM register summary

This section summarizes the ETM trace unit registers.

All ETM trace unit registers are 32 bits wide. The description of each register includes its offset from a base address. The base address is defined by the system integrator when placing the ETM trace unit in the Debug-APB memory map.

Table C10-1 ETM trace unit register summary

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TRCPRGCTLR</td>
<td>RW</td>
<td>C10.2 Programming Control Register on page C10-506</td>
</tr>
<tr>
<td>TRCSTATR</td>
<td>RO</td>
<td>C10.3 Status Register on page C10-507</td>
</tr>
<tr>
<td>TRCCONFIGR</td>
<td>RW</td>
<td>C10.4 Trace Configuration Register on page C10-508</td>
</tr>
<tr>
<td>TRCAUXCTLR</td>
<td>RW</td>
<td>C10.6 Auxiliary Control Register on page C10-511</td>
</tr>
<tr>
<td>TRCEVENTCTLR0</td>
<td>RW</td>
<td>C10.7 Event Control 0 Register on page C10-513</td>
</tr>
<tr>
<td>TRCEVENTCTLR1</td>
<td>RW</td>
<td>C10.8 Event Control 1 Register on page C10-515</td>
</tr>
<tr>
<td>TRCSTALLCTLR</td>
<td>RW</td>
<td>C10.9 Stall Control Register on page C10-516</td>
</tr>
<tr>
<td>TRCTSCTLR</td>
<td>RW</td>
<td>C10.10 Global Timestamp Control Register on page C10-517</td>
</tr>
<tr>
<td>TRCSYNCPR</td>
<td>RW</td>
<td>C10.11 Synchronization Period Register on page C10-518</td>
</tr>
<tr>
<td>TRCCCTLR</td>
<td>RW</td>
<td>C10.12 Cycle Count Control Register on page C10-519</td>
</tr>
<tr>
<td>TRCBBCCTRL</td>
<td>RW</td>
<td>C10.5 Branch Broadcast Control Register on page C10-510</td>
</tr>
<tr>
<td>TRCTRACEIDR</td>
<td>RW</td>
<td>C10.13 Trace ID Register on page C10-520</td>
</tr>
<tr>
<td>TRCVICTLR</td>
<td>RW</td>
<td>C10.14 ViewInst Main Control Register on page C10-521</td>
</tr>
<tr>
<td>TRCVIIECTRL</td>
<td>RW</td>
<td>C10.15 ViewInst Include-Exclude Control Register on page C10-523</td>
</tr>
<tr>
<td>TRCVISSCTRL</td>
<td>RW</td>
<td>C10.16 ViewInst Start-Stop Control Register on page C10-524</td>
</tr>
<tr>
<td>TRCSEQEVRO</td>
<td>RW</td>
<td>C10.17 Sequencer State Transition Control Registers 0-2 on page C10-525</td>
</tr>
<tr>
<td>TRCSEQEVRI</td>
<td>RW</td>
<td>C10.17 Sequencer State Transition Control Registers 0-2 on page C10-525</td>
</tr>
<tr>
<td>TRCSEQEVR2</td>
<td>RW</td>
<td>C10.17 Sequencer State Transition Control Registers 0-2 on page C10-525</td>
</tr>
<tr>
<td>TRCSEQRSTEVRO</td>
<td>RW</td>
<td>C10.18 Sequencer Reset Control Register on page C10-527</td>
</tr>
<tr>
<td>TRCSEQSTR</td>
<td>RW</td>
<td>C10.19 Sequencer State Register on page C10-528</td>
</tr>
<tr>
<td>TRCEXTINSEL</td>
<td>RW</td>
<td>C10.20 External Input Select Register on page C10-529</td>
</tr>
<tr>
<td>TRCCNTRLDVRO</td>
<td>RW</td>
<td>C10.21 Counter Reload Value Registers 0-1 on page C10-530</td>
</tr>
<tr>
<td>TRCCNTRLDVRI</td>
<td>RW</td>
<td>C10.21 Counter Reload Value Registers 0-1 on page C10-530</td>
</tr>
<tr>
<td>TRCCNTCTRL0</td>
<td>RW</td>
<td>C10.22 Counter Control Register 0 on page C10-531</td>
</tr>
<tr>
<td>TRCCNTCTRL1</td>
<td>RW</td>
<td>C10.23 Counter Control Register 1 on page C10-533</td>
</tr>
<tr>
<td>TRCCNTVR0</td>
<td>RW</td>
<td>C10.24 Counter Value Registers 0-1 on page C10-535</td>
</tr>
<tr>
<td>TRCCNTVR1</td>
<td>RW</td>
<td>C10.24 Counter Value Registers 0-1 on page C10-535</td>
</tr>
<tr>
<td>TRCIDR8</td>
<td>RO</td>
<td>C10.25 ID Register 8 on page C10-536</td>
</tr>
<tr>
<td>TRCIDR9</td>
<td>RO</td>
<td>C10.26 ID Register 9 on page C10-537</td>
</tr>
<tr>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>TRCIDR10</td>
<td>RO</td>
<td>C10.27 ID Register 10 on page C10-538</td>
</tr>
<tr>
<td>TRCIDR11</td>
<td>RO</td>
<td>C10.28 ID Register 11 on page C10-539</td>
</tr>
<tr>
<td>TRCIDR12</td>
<td>RO</td>
<td>C10.29 ID Register 12 on page C10-540</td>
</tr>
<tr>
<td>TRCIDR13</td>
<td>RO</td>
<td>C10.30 ID Register 13 on page C10-541</td>
</tr>
<tr>
<td>TCRIMSPEC0</td>
<td>RW</td>
<td>C10.31 Implementation Specific Register 0 on page C10-542</td>
</tr>
<tr>
<td>TRCIDR0</td>
<td>RO</td>
<td>C10.32 ID Register 0 on page C10-543</td>
</tr>
<tr>
<td>TRCIDR1</td>
<td>RO</td>
<td>C10.33 ID Register 1 on page C10-545</td>
</tr>
<tr>
<td>TRCIDR2</td>
<td>RO</td>
<td>C10.34 ID Register 2 on page C10-546</td>
</tr>
<tr>
<td>TRCIDR3</td>
<td>RO</td>
<td>C10.35 ID Register 3 on page C10-548</td>
</tr>
<tr>
<td>TRCIDR4</td>
<td>RO</td>
<td>C10.36 ID Register 4 on page C10-550</td>
</tr>
<tr>
<td>TRCIDR5</td>
<td>RO</td>
<td>C10.37 ID Register 5 on page C10-552</td>
</tr>
<tr>
<td>TRCRSCTLRn</td>
<td>RW</td>
<td>C10.38 Resource Selection Control Registers 2-16 on page C10-554, n is 2, 15</td>
</tr>
<tr>
<td>TRCSSCCR0</td>
<td>RW</td>
<td>C10.39 Single-Shot Comparator Control Register 0 on page C10-555</td>
</tr>
<tr>
<td>TRCSSCSR0</td>
<td>RW, RO</td>
<td>C10.40 Single-Shot Comparator Status Register 0 on page C10-556</td>
</tr>
<tr>
<td>TRCOSLAR</td>
<td>WO</td>
<td>C10.41 OS Lock Access Register on page C10-557</td>
</tr>
<tr>
<td>TRCOSLSR</td>
<td>RO</td>
<td>C10.42 OS Lock Status Register on page C10-558</td>
</tr>
<tr>
<td>TRCPDCR</td>
<td>RW</td>
<td>C10.43 Power Down Control Register on page C10-559</td>
</tr>
<tr>
<td>TRCPDSR</td>
<td>RO</td>
<td>C10.44 Power Down Status Register on page C10-560</td>
</tr>
<tr>
<td>TRCACVRn</td>
<td>RW</td>
<td>C10.45 Address Comparator Value Registers 0-7 on page C10-561</td>
</tr>
<tr>
<td>TRCACATRn</td>
<td>RW</td>
<td>C10.46 Address Comparator Access Type Registers 0-7 on page C10-562&gt;</td>
</tr>
<tr>
<td>TRCCIDCVR0</td>
<td>RW</td>
<td>C10.47 Context ID Comparator Value Register 0 on page C10-564</td>
</tr>
<tr>
<td>TRCVMIDCVR0</td>
<td>RW</td>
<td>C10.48 VMID Comparator Value Register 0 on page C10-565</td>
</tr>
<tr>
<td>TRCCIDCCTLR0</td>
<td>RW</td>
<td>C10.49 Context ID Comparator Control Register 0 on page C10-566</td>
</tr>
<tr>
<td>TRCITATBIDR</td>
<td>RW</td>
<td>C10.50 Integration ATB Identification Register on page C10-567</td>
</tr>
<tr>
<td>TRCITIDATAR</td>
<td>WO</td>
<td>C10.51 Integration Instruction ATB Data Register on page C10-568</td>
</tr>
<tr>
<td>TRCITIATBINR</td>
<td>RO</td>
<td>C10.52 Integration Instruction ATB In Register on page C10-569</td>
</tr>
<tr>
<td>TRCITIATBOUTR</td>
<td>WO</td>
<td>C10.53 Integration Instruction ATB Out Register on page C10-570</td>
</tr>
<tr>
<td>TRCITCTRL</td>
<td>RW</td>
<td>C10.54 Integration Mode Control Register on page C10-571</td>
</tr>
<tr>
<td>TRCLAIMSET</td>
<td>RW</td>
<td>C10.55 Claim Tag Set Register on page C10-572</td>
</tr>
<tr>
<td>TRCLAIMCLR</td>
<td>RW</td>
<td>C10.56 Claim Tag Clear Register on page C10-573</td>
</tr>
<tr>
<td>TRCDEVAFF0</td>
<td>RO</td>
<td>C10.57 Device Affinity Register 0 on page C10-574</td>
</tr>
<tr>
<td>TRCDEVAFF1</td>
<td>RO</td>
<td>C10.58 Device Affinity Register 1 on page C10-576</td>
</tr>
<tr>
<td>TRCLAR</td>
<td>WO</td>
<td>C10.59 Software Lock Access Register on page C10-577</td>
</tr>
<tr>
<td>TRCLSR</td>
<td>RO</td>
<td>C10.60 Software Lock Status Register on page C10-578</td>
</tr>
<tr>
<td>TRCAUTHSTATUS</td>
<td>RO</td>
<td>C10.61 Authentication Status Register on page C10-579</td>
</tr>
<tr>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------</td>
<td>------</td>
<td>-------------------------------------------------------</td>
</tr>
<tr>
<td>TRCDEVARCH</td>
<td>RO</td>
<td>C10.62 Device Architecture Register on page C10-580</td>
</tr>
<tr>
<td>TRCDEVID</td>
<td>RO</td>
<td>C10.63 Device ID Register on page C10-581</td>
</tr>
<tr>
<td>TRCDEVTYPE</td>
<td>RO</td>
<td>C10.64 Device Type Register on page C10-582</td>
</tr>
<tr>
<td>TRCPIDR4</td>
<td>RO</td>
<td>C10.70 ETM Peripheral Identification Register 4 on page C10-588</td>
</tr>
<tr>
<td>TRCPIDR5</td>
<td>RO</td>
<td>C10.71 ETM Peripheral Identification Register 5-7 on page C10-589</td>
</tr>
<tr>
<td>TRCPIDR6</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>TRCPIDR7</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>TRCPIDR0</td>
<td>RO</td>
<td>C10.66 ETM Peripheral Identification Register 0 on page C10-584</td>
</tr>
<tr>
<td>TRCPIDR1</td>
<td>RO</td>
<td>C10.67 ETM Peripheral Identification Register 1 on page C10-585</td>
</tr>
<tr>
<td>TRCPIDR2</td>
<td>RO</td>
<td>C10.68 ETM Peripheral Identification Register 2 on page C10-586</td>
</tr>
<tr>
<td>TRCPIDR3</td>
<td>RO</td>
<td>C10.69 ETM Peripheral Identification Register 3 on page C10-587</td>
</tr>
<tr>
<td>TRCCIDR0</td>
<td>RO</td>
<td>C10.73 ETM Component Identification Register 0 on page C10-591</td>
</tr>
<tr>
<td>TRCCIDR1</td>
<td>RO</td>
<td>C10.74 ETM Component Identification Register 1 on page C10-592</td>
</tr>
<tr>
<td>TRCCIDR2</td>
<td>RO</td>
<td>C10.75 ETM Component Identification Register 2 on page C10-593</td>
</tr>
<tr>
<td>TRCCIDR3</td>
<td>RO</td>
<td>C10.76 ETM Component Identification Register 3 on page C10-594</td>
</tr>
</tbody>
</table>
C10.2 Programming Control Register

The TRCPRGCTLR characteristics are:

**Purpose**

Enables the ETM trace unit.

**Usage constraints**

See *C3.4 Programming and reading ETM trace unit registers* on page C3-391.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

![TRCPRGCTLR bit assignments](image)

Figure C10-1 TRCPRGCTLR bit assignments

[31:1]

Reserved, RES0.

**EN, [0]**

Trace program enable:

- 0 The ETM trace unit interface in the processor is disabled, and clocks are enabled only when necessary to process APB accesses, or drain any already generated trace. This is the reset value.
- 1 The ETM trace unit interface in the processor is enabled, and clocks are enabled. Writes to most trace registers are ignored.

The TRCPRGCTLR can be accessed through the external debug interface, offset 0x004.
C10.3 Status Register

The TRCSTATR characteristics are:

**Purpose**
Indicates the ETM trace unit status.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-2 TRCSTATR bit assignments](image)

**[31:2]**
Reserved, RES0.

**PMSTABLE, [1]**
Indicates whether the ETM trace unit registers are stable and can be read:

- 0 The programmers model is not stable.
- 1 The programmers model is stable.

**IDLE, [0]**
Idle status:

- 0 The ETM trace unit is not idle.
- 1 The ETM trace unit is idle.

The TRCSTATR can be accessed through the external debug interface, offset 0x00C.
The TRCCONFIGR characteristics are:

**Purpose**
Controls the tracing options.

**Usage constraints**
- This register must always be programmed as part of trace unit initialization.
- Only accepts writes when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
TRCCONFIGR is a 32-bit RW trace register.

See [C10.1 ETM register summary](#) on page C10-503.

![TRCCONFIGR bit assignments](image)

**[31:13]**
Reserved, RES0.

**RS, [12]**
Enables the return stack. The possible values are:

- 0  Disables the return stack.
- 1  Enables the return stack.

**TS, [11]**
Enables global timestamp tracing. The possible values are:

- 0  Disables global timestamp tracing.
- 1  Enables global timestamp tracing.

**[10:8]**
Reserved, RES0.

**VMID, [7]**
Enables VMID tracing. The possible values are:

- 0  Disables VMID tracing.
- 1  Enables VMID tracing.

**CID, [6]**
Enables context ID tracing. The possible values are:

- 0  Disables context ID tracing.
- 1  Enables context ID tracing.
Reserved, RES0.

CCI, [4]
Enables cycle counting instruction trace. The possible values are:
0  Disables cycle counting instruction trace.
1  Enables cycle counting instruction trace.

BB, [3]
Enables branch broadcast mode. The possible values are:
0  Disables branch broadcast mode.
1  Enables branch broadcast mode.

[2:1]
Reserved, RES0.

[0]
Reserved, RES1.

The TRCCONFIGR can be accessed through the external debug interface, offset 0x010.
C10.5 Branch Broadcast Control Register

The TRCBBCTRLR characteristics are:

**Purpose**
Controls how branch broadcasting behaves, and enables branch broadcasting to be enabled for certain memory regions.

**Usage constraints**
- Only accepts writes when the trace unit is disabled.
- Must be programmed if TRCCONFIGR.BB == 1.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-4 TRCBBCTRLR bit assignments](image)

[31:9]
Reserved, RES0.

**MODE**, [8]
Mode bit:
- 0 Exclude mode. Branch broadcasting is not enabled in the address range that RANGE defines.
  - If RANGE==0 then branch broadcasting is enabled for the entire memory map.
- 1 Include mode. Branch broadcasting is enabled in the address range that RANGE defines.
  - If RANGE==0 then the behavior of the trace unit is constrained UNPREDICTABLE. That is, the trace unit might or might not consider any instructions to be in a branch broadcast region.

**RANGE**, [7:0]
Address range field.
Selects which address range comparator pairs are in use with branch broadcasting. Each bit represents an address range comparator pair, so bit[n] controls the selection of address range comparator pair n. If bit[n] is:
- 0 The address range that address range comparator pair n defines, is not selected.
- 1 The address range that address range comparator pair n defines, is selected.

The TRCBBCTRLR can be accessed through the external debug interface, offset 0x03C.
C10.6 Auxiliary Control Register

The TRCAUXCTLR characteristics are:

**Purpose**
The function of this register is to provide IMPLEMENTATION DEFINED configuration and control options.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

![Figure C10-5 TRCAUXCTLR bit assignments](image)

**[31:8]**
Reserved, RES0.

**COREIFEN, [7]**
Keep core interface enabled regardless of trace enable register state. The possible values are:

- 0 Core interface enabled is set by trace enable register state.
- 1 Enable core interface, regardless of trace enable register state.

**[6]**
Reserved, RES0.

**AUTHNOFLUSH, [5]**
Do not flush trace on de-assertion of authentication inputs. The possible values are:

- 0 ETM trace unit FIFO is flushed and ETM trace unit enters idle state when DBGEN or NIDEN is LOW.
- 1 ETM trace unit FIFO is not flushed and ETM trace unit does not enter idle state when DBGEN or NIDEN is LOW.

When this bit is set to 1, the trace unit behavior deviates from architecturally-specified behavior.

**TSNODELAY, [4]**
Do not delay timestamp insertion based on FIFO depth. The possible values are:

- 0 Timestamp packets are inserted into FIFO only when trace activity is LOW.
- 1 Timestamp packets are inserted into FIFO irrespective of trace activity.

**SYNCDELAY, [3]**
Delay periodic synchronization if FIFO is more than half-full. The possible values are:

- 0 SYNC packets are inserted into FIFO only when trace activity is low.
- 1 SYNC packets are inserted into FIFO irrespective of trace activity.

**OVFLW, [2]**

Force overflow if synchronization is not completed when second synchronization becomes due. The possible values are:

- 0 No FIFO overflow when SYNC packets are delayed.
- 1 Forces FIFO overflow when SYNC packets are delayed.

When this bit is set to 1, the trace unit behavior deviates from architecturally-specified behavior.

**IDLEACK, [1]**

Force idle-drain acknowledge high, CPU does not wait for trace to drain before entering WFX state. The possible values are:

- 0 ETM trace unit idle acknowledge is asserted only when the ETM trace unit is in idle state.
- 1 ETM trace unit idle acknowledge is asserted irrespective of the ETM trace unit idle state.

When this bit is set to 1, trace unit behavior deviates from architecturally-specified behavior.

**AFREADY, [0]**

Always respond to AFREADY immediately. Does not have any interaction with FIFO draining, even in WFI state. The possible values are:

- 0 ETM trace unit AFREADY output is asserted only when the ETM trace unit is in idle state or when all the trace bytes in FIFO before a flush request are output.
- 1 ETM trace unit AFREADY output is always asserted HIGH. When this bit is set to 1, trace unit behavior deviates from architecturally-specified behavior.

The TRCAUXCTLR can be accessed through the external debug interface, offset 0x018.
C10.7 Event Control 0 Register

The TRCEVENTCTL0R characteristics are:

**Purpose**
Controls the tracing of events in the trace stream. The events also drive the external outputs from the ETM trace unit. The events are selected from the Resource Selectors.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See [C10.1 ETM register summary on page C10-503](#).

![Figure C10-6 TRCEVENTCTL0R bit assignments](#)

**TYPE3, [31]**
Selects the resource type for trace event 3:
- 0 Single selected resource.
- 1 Boolean combined resource pair.

**[30:28]**
Reserved, RES0.

**SEL3, [27:24]**
Selects the resource number, based on the value of TYPE3:
- When TYPE3 is 0, selects a single selected resource from 0-15 defined by bits[3:0].
- When TYPE3 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

**TYPE2, [23]**
Selects the resource type for trace event 2:
- 0 Single selected resource.
- 1 Boolean combined resource pair.

**[22:20]**
Reserved, RES0.

**SEL2, [19:16]**
Selects the resource number, based on the value of TYPE2:
- When TYPE2 is 0, selects a single selected resource from 0-15 defined by bits[3:0].
- When TYPE2 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

**TYPE1, [15]**
Selects the resource type for trace event 1:
- 0 Single selected resource.
Boolean combined resource pair.

[14:12]
Reserved, RES0.

SEL1, [11:8]
Selects the resource number, based on the value of TYPE1:
When TYPE1 is 0, selects a single selected resource from 0-15 defined by bits[3:0].
When TYPE1 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

TYPE0, [7]
Selects the resource type for trace event 0:
0 Single selected resource.
1 Boolean combined resource pair.

[6:4]
Reserved, RES0.

SEL0, [3:0]
Selects the resource number, based on the value of TYPE0:
When TYPE0 is 0, selects a single selected resource from 0-15 defined by bits[3:0].
When TYPE0 is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

The TRCEVENTCTL0R can be accessed through the external debug interface, offset 0x020.
C10.8 Event Control 1 Register

The TRCEVENTCTL1R characteristics are:

**Purpose**
Controls the behavior of the events that TRCEVENTCTL0R selects.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
TRCEVENTCTL1R is a 32-bit RW trace register.

See *C10.1 ETM register summary* on page C10-503.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Figure C10-7** TRCEVENTCL1R bit assignments

[31:13] Reserved, RES0.

**LPOVERRIDE, [12]**
Low-power state behavior override:
0 Low-power state behavior unaffected.
1 Low-power state behavior overridden. The resources and Event trace generation are unaffected by entry to a low-power state.

**ATB, [11]**
ATB trigger enable:
0 ATB trigger disabled.
1 ATB trigger enabled.

[10:4] Reserved, RES0.

**EN, [3:0]**
One bit per event, to enable generation of an event element in the instruction trace stream when the selected event occurs:
0 Event does not cause an event element.
1 Event causes an event element.

The TRCEVENTCTL1R can be accessed through the external debug interface, offset 0x024.
## C10.9 Stall Control Register

The TRCSTALLCTLR characteristics are:

**Purpose**
Enables the ETM trace unit to stall the Cortex-A32 processor if the ETM trace unit FIFO overflows.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-8 TRCSTALLCTLR bit assignments](image)

### Bit Assignments

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Description</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:9</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>ISTALL, Instruction stall bit</td>
<td>The trace unit does not stall the processor: 0</td>
</tr>
<tr>
<td>7:4</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>3:2</td>
<td>LEVEL, Threshold level field</td>
<td>0b00 Zero invasion. Greater risk of FIFO overflow.</td>
</tr>
<tr>
<td>1:0</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
</tbody>
</table>

The TRCSTALLCTLR can be accessed through the external debug interface, offset 0x02c.
C10.10 Global Timestamp Control Register

The TRCTSCTLR characteristics are:

**Purpose**
controls the insertion of global timestamps in the trace streams. When the selected event is triggered, the trace unit inserts a global timestamp into the trace streams. The event is selected from one of the Resource Selectors.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- Must be programmed if TRCCONFIGR.TS==1.

**Configurations**
Available in all configurations.

**Attributes**

TRCTSCTLR is a 32-bit RW trace register.

The register is set to an **UNKNOWN** value on a trace unit reset. See also *C10.1 ETM register summary* on page C10-503.

![Figure C10-9 TRCTSCTLR bit assignments](image)

<table>
<thead>
<tr>
<th>31:8</th>
<th>8:7</th>
<th>7:6</th>
<th>6:4</th>
<th>4:3</th>
<th>3:0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SEL, [3:1]</td>
<td>Identifies the resource selector to use.</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The TRCTSCTLR can be accessed through the external debug interface, offset 0x030.
C10.11 Synchronization Period Register

The TRCSYNCPR characteristics are:

**Purpose**
Controls how often periodic trace synchronization requests occur.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![TRCSYNCPR bit assignments](image)

---

**[31:5]**
Reserved, RES0.

**PERIOD, [4:0]**
Defines the number of bytes of trace between synchronization requests as a total of the number of bytes generated by both the instruction and data streams. The number of bytes is $2^N$ where $N$ is the value of this field:
- A value of zero disables these periodic synchronization requests, but does not disable other synchronization requests.
- The minimum value that can be programmed, other than zero, is 8, providing a minimum synchronization period of 256 bytes.
- The maximum value is 20, providing a maximum synchronization period of $2^{20}$ bytes.

The TRCSYNCPR can be accessed through the external debug interface, offset 0x034.
C10.12 Cycle Count Control Register

The TRCCCCTLR characteristics are:

**Purpose**
Sets the threshold value for cycle counting.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- Must be programmed if TRCCONFIGR.CCI==1.
- Minimum value that can be programmed is defined in TRCIDR3.CCITMIN.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>12</th>
<th>11</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>THRESHOLD</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure C10-11 TRCCCCTLR bit assignments

[31:12] Reserved, RES0.

**THRESHOLD, [11:0]**
Instruction trace cycle count threshold.

The TRCCCCTLR can be accessed through the external debug interface, offset 0x038.
C10.13 Trace ID Register

The TRCTRACEIDR characteristics are:

Purpose
Sets the trace ID for instruction trace.

Usage constraints
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

Configurations
Available in all configurations.

Attributes
TRCTRACEIDR is a 32-bit RW trace register.

See C10.1 ETM register summary on page C10-503.

| 31 | 30 | 29 | 28 | 27 | 26 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|---|---|---|---|---|---|---|---|---|
| RES0 | | | | | | | TRACEID |

[31:7] Reserved, RES0.

TRACEID, [6:0]
Trace ID value. When only instruction tracing is enabled, this provides the trace ID.

The TRCTRACEIDR can be accessed through the external debug interface, offset 0x040.
C10.14 ViewInst Main Control Register

The TRCVICTLR characteristics are:

**Purpose**
Controls instruction trace filtering.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- Returns stable data only when TRCSTATR.PMSTABLE==1.
- Must be programmed, particularly to set the value of the SSSTATUS bit, that sets the state of the start-stop logic.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

```
+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+
| 31             | 30             | 29             | 28             | 27             | 26             | 25             | 24             | 23             | 22             | 21             | 20             |
| RES0           | RES0           | RES0           | RES0           | SELEXLEVEL_S   | EXLEVEL_NS     | TYPE           | RES0           | SSSTATUS       | TRCRESET       | TRCERR         |
|                |                |                |                |                |                |                |                |                |                |                |                |
+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+-----------------+
```

**Figure C10-13** TRCVICTLR bit assignments

[31:24]
Reserved, RES0.

**EXLEVEL_NS, [23:20]**
In Non-secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level:

- **0** Trace unit generates instruction trace, in Non-secure state, for exception level \( n \).
- **1** Trace unit does not generate instruction trace, in Non-secure state, for exception level \( n \).

The exception levels are:

*Bit[20]* Exception level 0.

*Bit[21]* Exception level 1.

*Bit[22]* Exception level 2.

*Bit[23]* RAZ/WI. Instruction tracing is not implemented for exception level 3.

**EXLEVEL_S, [19:16]**
In Secure state, each bit controls whether instruction tracing is enabled for the corresponding exception level:

- **0** Trace unit generates instruction trace, in Secure state, for exception level \( n \).
- **1** Trace unit does not generate instruction trace, in Secure state, for exception level \( n \).

The exception levels are:

*Bit[16]* Exception level 0.
Bit[17] Exception level 1.
Bit[18] RAZ/WI. Instruction tracing is not implemented for exception level 2.

[15:12] Reserved, RES0.

Selects whether a system error exception must always be traced:
\( \begin{align*}
0 & \quad \text{System error exception is traced only if the instruction or exception immediately before the system error exception is traced.} \\
1 & \quad \text{System error exception is always traced regardless of the value of ViewInst.}
\end{align*} \)

TRCRESET, [10]
Selects whether a reset exception must always be traced:
\( \begin{align*}
0 & \quad \text{Reset exception is traced only if the instruction or exception immediately before the reset exception is traced.} \\
1 & \quad \text{Reset exception is always traced regardless of the value of ViewInst.}
\end{align*} \)

SSSTATUS, [9]
Indicates the current status of the start/stop logic:
\( \begin{align*}
0 & \quad \text{Start/stop logic is in the stopped state.} \\
1 & \quad \text{Start/stop logic is in the started state.}
\end{align*} \)

[8] Reserved, RES0.

TYPE, [7]
Selects the resource type for the viewinst event:
\( \begin{align*}
0 & \quad \text{Single selected resource.} \\
1 & \quad \text{Boolean combined resource pair.}
\end{align*} \)


SEL, [3:0]
Selects the resource number to use for the viewinst event, based on the value of TYPE:
When TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
When TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
The TRCVICTLR can be accessed through the external debug interface, offset 0x080.
C10.15 ViewInst Include-Exclude Control Register

The TRCVIIECTLR characteristics are:

**Purpose**
Defines the address range comparators that control the ViewInst Include/Exclude control.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-14 TRCVIIECTLR bit assignments](image)

**[31:20]**
Reserved, RES0.

**EXCLUDE, [19:16]**
Defines the address range comparators for ViewInst exclude control. One bit is provided for each implemented Address Range Comparator.

**[15:4]**
Reserved, RES0.

**INCLUDE, [3:0]**
Defines the address range comparators for ViewInst include control.

Selecting no include comparators indicates that all instructions must be included. The exclude control indicates which ranges must be excluded.

One bit is provided for each implemented Address Range Comparator.

The TRCVIIECTLR can be accessed through the external debug interface, offset 0x084.
C10.16 ViewInst Start-Stop Control Register

The TRCVISSCTLR characteristics are:

**Purpose**
Defines the single address comparators that control the ViewInst Start/Stop logic.

**Usage constraints**
- You must always program this register as part of trace unit initialization.
- Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

```
  | 31 | 24 | 23 | 16 | 15 | 8 | 7 | 0 |
  | RES0 | STOP | RES0 | START |
```

**Figure C10-15 TRCVISSCTLR bit assignments**

[31:24] Reserved, RES0.

**STOP, [23:16]**
Defines the single address comparators to stop trace with the ViewInst Start/Stop control.
One bit is provided for each implemented single address comparator.

[15:8] Reserved, RES0.

**START, [7:0]**
Defines the single address comparators to start trace with the ViewInst Start/Stop control.
One bit is provided for each implemented single address comparator.

The TRCVISSCTLR can be accessed through the external debug interface, offset 0x088.
C10.17 Sequencer State Transition Control Registers 0-2

The TRCSEQEVRn characteristics are:

**Purpose**
 Defines the sequencer transitions that progress to the next state or backwards to the previous state. The ETM trace unit implements a sequencer state machine with up to four states.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- Returns stable data only when TRCSTATR.PMSTABLE==1.
- Software must use this register to set the initial state of the sequencer before the sequencer is used.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-16 TRCSEQEVRn bit assignments](image)

[31:16] Reserved, RES0.

**B TYPE, [15]**
Selects the resource type to move backwards to this state from the next state:
- 0 Single selected resource.
- 1 Boolean combined resource pair.

[14:12] Reserved, RES0

**B SEL, [11:8]**
Selects the resource number, based on the value of B TYPE:
- When B TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
- When B TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

**F TYPE, [7]**
Selects the resource type to move forwards from this state to the next state:
- 0 Single selected resource.
- 1 Boolean combined resource pair.


**F SEL, [3:0]**
Selects the resource number, based on the value of F TYPE:
- When F TYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
- When F TYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].
The TRCSEQEVRn registers can be accessed through the external debug interface, offsets:

**TRCSEQEVR0**
\[ \text{offset} \times 100. \]

**TRCSEQEVR1**
\[ \text{offset} \times 104. \]

**TRCSEQEVR2**
\[ \text{offset} \times 108. \]
C10.18 Sequencer Reset Control Register

The TRCSEQRSTEVR characteristics are:

**Purpose**
- Resets the sequencer to state 0.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- If the sequencer is used, you must program all sequencer state transitions with a valid event.

**Configurations**
- Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

```plaintext
<p>| | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>4</td>
<td>3</td>
<td>0</td>
<td>RES0</td>
</tr>
</tbody>
</table>
```

**Figure C10-17 TRCSEQRSTEVR bit assignments**

[31:8]
- Reserved, RES0.

**RESETTYPE, [7]**
- Selects the resource type to move back to state 0:
  - 0 Single selected resource.
  - 1 Boolean combined resource pair.

[6:4]
- Reserved, RES0.

**RESETSEL, [3:0]**
- Selects the resource number, based on the value of RESETTYPE:
  - When RESETTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
  - When RESETTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

The TRCSEQRSTEVR can be accessed through the external debug interface, offset 0x118.
C10.19 Sequencer State Register

The TRCSEQSTR characteristics are:

**Purpose**

Holds the value of the current state of the sequencer.

**Usage constraints**

- Accepts writes only when the trace unit is disabled.
- Returns stable data only when TRCSTATR.PMSTABLE==1.
- Software must use this register to set the initial state of the sequencer before the sequencer is used.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

![Figure C10-18 TRCSEQSTR bit assignments](image)

<table>
<thead>
<tr>
<th>Bit position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:2]</td>
<td>Reserved, res0.</td>
</tr>
<tr>
<td>STATE [1:0]</td>
<td>Current sequencer state:</td>
</tr>
<tr>
<td>0b00</td>
<td>State 0.</td>
</tr>
<tr>
<td>0b01</td>
<td>State 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>State 2.</td>
</tr>
<tr>
<td>0b11</td>
<td>State 3.</td>
</tr>
</tbody>
</table>

The TRCSEQSTR can be accessed through the external debug interface, offset 0x11c.
C10.20 External Input Select Register

The TRCEXTINSELR characteristics are:

**Purpose**
Controls the selectors that choose an external input as a resource in the ETM trace unit. You can use the Resource Selectors to access these external input resources.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

<table>
<thead>
<tr>
<th>31</th>
<th>29</th>
<th>28</th>
<th>24</th>
<th>23</th>
<th>21</th>
<th>20</th>
<th>16</th>
<th>15</th>
<th>13</th>
<th>12</th>
<th>8</th>
<th>7</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>SEL3</td>
<td>RES0</td>
<td>SEL2</td>
<td>RES0</td>
<td>SEL1</td>
<td>RES0</td>
<td>SEL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure C10-19 TRCEXTINSELR bit assignments*

[31:29] Reserved, RES0.


[23:21] Reserved, RES0.

SEL2, [20:16] Selects an event from the external input bus for External Input Resource 2.

[15:13] Reserved, RES0.

SEL1, [12:8] Selects an event from the external input bus for External Input Resource 1.

[7:5] Reserved, RES0.

SEL0, [4:0] Selects an event from the external input bus for External Input Resource 0.

The TRCEXTINSELR can be accessed through the external debug interface, offset 0x120.
C10.21 Counter Reload Value Registers 0-1

The TRCCNTRLDVRn characteristics are:

**Purpose**
Defines the reload value for the counter.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-20 TRCCNTRLDVRn bit assignments](image)

[31:16] Reserved, RES0.

**VALUE, [15:0]**
Defines the reload value for the counter. This value is loaded into the counter each time the reload event occurs.

The TRCCNTRLDVRn registers can be accessed through the external debug interface, offsets:

**TRCCNTRLDVR0**
0x140.

**TRCCNTRLDVR1**
0x144.
C10.22 Counter Control Register 0

The TRCCNTCTRL0 characteristics are:

**Purpose**
- Controls the counter.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.

**Configurations**
- Available in all configurations.

**Attributes**
- See *C10.1 ETM register summary* on page C10-503.

![Figure C10-21 TRCCNTCTRL0 bit assignments](image)

- **[31:17]**
  - Reserved, RES0.

- **RLDSEL, [16]**
  - Defines whether the counter reloads when it reaches zero:
    - 0 The counter does not reload when it reaches zero. The counter only reloads based on RLDTYPE and RLDSEL.
    - 1 The counter reloads when it reaches zero and the resource selected by CNTTYPE and CNTSEL is also active. The counter also reloads based on RLDTYPE and RLDSEL.

- **RLDTYPE, [15]**
  - Selects the resource type for the reload:
    - 0 Single selected resource.
    - 1 Boolean combined resource pair.

- **[14:12]**
  - Reserved, RES0.

- **RLDSEL, [11:8]**
  - Selects the resource number, based on the value of RLDTYPE:
    - When RLDTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
    - When RLDTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

- **CNTTYPE, [7]**
  - Selects the resource type for the counter:
    - 0 Single selected resource.
    - 1 Boolean combined resource pair.

- **[6:4]**
  - Reserved, RES0.
CNTSEL, [3:0]

Selects the resource number, based on the value of CNTTYPE:

When CNTTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].

When CNTTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

The TRCCNTCTLR0 can be accessed through the external debug interface, offset 0x150.
### C10.23 Counter Control Register 1

The TRCCNTCTLR1 characteristics are:

**Purpose**
Controls the counter.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:18</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td>CNTCHAIN, defines whether the counter decrements when the counter reloads. This enables two counters to be used in combination to provide a larger counter: 0: The counter operates independently from the counter. The counter only decrements based on CNTTYPE and CNTSEL. 1: The counter decrements when the counter reloads. The counter also decrements when the resource selected by CNTTYPE and CNTSEL is active.</td>
</tr>
<tr>
<td>16</td>
<td>RLDSEL, defines whether the counter reloads when it reaches zero: 0: The counter does not reload when it reaches zero. The counter only reloads based on RLDTYPE and RLDSEL. 1: The counter reloads when it is zero and the resource selected by CNTTYPE and CNTSEL is also active. The counter also reloads based on RLDTYPE and RLDSEL.</td>
</tr>
<tr>
<td>15</td>
<td>RLDTYPE, selects the resource type for the reload: 0: Single selected resource. 1: Boolean combined resource pair.</td>
</tr>
<tr>
<td>8:6</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3:0</td>
<td>Selects the resource number, based on the value of RLDTYPE: When RLDTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0]. When RLDTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].</td>
</tr>
</tbody>
</table>

![Figure C10-22 TRCCNTCTLR1 bit assignments](image-url)

Figure C10-22 TRCCNTCTLR1 bit assignments
CNTTYPE, [7]

Selects the resource type for the counter:
0    Single selected resource.
1    Boolean combined resource pair.

[6:4]
Reserved, RES0.

CNTSEL, [3:0]

Selects the resource number, based on the value of CNTTYPE:
When CNTTYPE is 0, selects a single selected resource from 0-15 defined by bits[3:0].
When CNTTYPE is 1, selects a Boolean combined resource pair from 0-7 defined by bits[2:0].

The TRCCNTCTRL1 can be accessed through the external debug interface, offset 0x154.
C10.24 Counter Value Registers 0-1

The TRCCNTVRn characteristics are:

**Purpose**
Contains the current counter value.

**Usage constraints**
- Can be written only when the ETM trace unit is disabled.
- The count value is stable only when TRCSTATR.PMSTABLE==1.
- If software uses counter <n>, then it must write to this register to set the initial counter value.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

```
+-------------+-----+-----+-----+-----+
| 31          | 30  | 16  | 15  | 0   |
| RES0        |     | VALUE |     |     |
```

*Figure C10-23 TRCCNTVRn bit assignments*

[31:16]  
Reserved, RES0.

**VALUE, [15:0]**  
Contains the current counter value.

The TRCCNTVRn registers can be accessed through the external debug interface, offsets:

**TRCCNTVR0**  
0x160.

**TRCCNTVR1**  
0x164.
C10.25 ID Register 8

The TRCIDR8 characteristics are:

**Purpose**

Returns the maximum speculation depth of the instruction trace stream.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary on page C10-503.*

![Figure C10-24 TRCIDR8 bit assignments](image_url)

**MAXSPEC, [31:0]**

The maximum number of P0 elements in the trace stream that can be speculative at any time.

- Maximum speculation depth of the instruction trace stream.

The TRCIDR8 can be accessed through the external debug interface, offset 0x180.
C10.26  ID Register 9

The TRCIDR9 characteristics are:

**Purpose**

Returns the number of P0 right-hand keys that the trace unit can use.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NUMP0KEY |

The number of P0 right-hand keys that the trace unit can use.

- 0  Number of P0 right-hand keys.

The TRCIDR9 can be accessed through the external debug interface, offset 0x184.

![Figure C10-25 TRCID9 bit assignments](image-url)
C10.27 ID Register 10

The TRCIDR10 characteristics are:

Purpose
Returns the number of P1 right-hand keys that the trace unit can use.

Usage constraints
There are no usage constraints.

Configurations
Available in all configurations.

Attributes
See C10.1 ETM register summary on page C10-503.

<table>
<thead>
<tr>
<th>NUMP1KEY</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 0</td>
</tr>
</tbody>
</table>

Figure C10-26 TRCIDR10 bit assignments

NUMP1KEY, [31:0]
The number of P1 right-hand keys that the trace unit can use.

0 Number of P1 right-hand keys.

The TRCIDR10 can be accessed through the external debug interface, offset 0x188.
The TRCIDR11 characteristics are:

**Purpose**
Returns the number of special P1 right-hand keys that the trace unit can use.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-27 TRCIDR11 bit assignments](image-url)

**NUMP1SPC, [31:0]**
The number of special P1 right-hand keys that the trace unit can use.
0  Number of special P1 right-hand keys.

The TRCIDR11 can be accessed through the external debug interface, offset 0x18C.
C10.29 ID Register 12

The TRCIDR12 characteristics are:

Purpose
Returns the number of conditional instruction right-hand keys that the trace unit can use.

Usage constraints
There are no usage constraints.

Configurations
Available in all configurations.

Attributes
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-28 TRCIDR12 bit assignments](image)

NUMCONDKEY, [31:0]

The number of conditional instruction right-hand keys that the trace unit can use, including normal and special keys.

0 Number of conditional instruction right-hand keys.

The TRCIDR12 can be accessed through the external debug interface, offset 0x190.
C10.30 ID Register 13

The TRCIDR13 characteristics are:

**Purpose**
Returns the number of special conditional instruction right-hand keys that the trace unit can use.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-29 TRCIDR13 bit assignments](image)

**NUMCONDSPC, [31:0]**

The number of special conditional instruction right-hand keys that the trace unit can use, including normal and special keys.

0 Number of special conditional instruction right-hand keys.

The TRCIDR13 can be accessed through the external debug interface, offset 0x194.
C10.31 Implementation Specific Register 0

The TRCIMSPEC0 characteristics are:

**Purpose**
Shows the presence of any implementation specific features, and enables any features that are provided.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-30 TRCIMSPEC0 bit assignments](image)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>31</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SUPPORT</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[31:4]
Reserved, RES0.

**SUPPORT, [3:0]**

θ No implementation specific extensions are supported.

The TRCIMSPEC0 can be accessed through the external debug interface, offset 0x1C0.
C10.32 ID Register 0

The TRCIDR0 characteristics are:

**Purpose**

Returns the tracing capabilities of the ETM trace unit.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>24</th>
<th>23</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>TSIZE</td>
<td>RES0</td>
<td>QSUPP</td>
<td>QFILT</td>
<td>CONDTYPE</td>
<td>NUMEVENT</td>
<td>RETSTACK</td>
<td>RES0</td>
<td>RES1</td>
<td>INSTP0</td>
<td>TRCDATA</td>
<td>TRCBB</td>
<td>TRCOND</td>
<td>TRCCI</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure C10-31 TRCIDR0 bit assignments**

[31:30]

Reserved, RES0.

**COMMOPT, [29]**

Indicates the meaning of the commit field in some packets:

- 1 Commit mode 1.

**TSIZE, [28:24]**

Global timestamp size field:

- 0b01000 Implementation supports a maximum global timestamp of 64 bits.

[23:17]

Reserved, RES0.

**QSUPP, [16:15]**

Indicates Q element support:

- 0b0 Q elements not supported.

**QFILT, [14]**

Indicates Q element filtering support:

- 0b0 Q element filtering not supported.

**CONDTYPE, [13:12]**

Indicates how conditional results are traced:

- 0b0 Conditional trace not supported.

**NUMEVENT, [11:10]**
Number of events supported in the trace, minus 1:

0b11  Four events supported.

RETSTACK, [9]

Return stack support:
1  Return stack implemented.

[8]

Reserved, RES0.

TRCCCI, [7]

Support for cycle counting in the instruction trace:
1  Cycle counting in the instruction trace is implemented.

TRCCOND, [6]

Support for conditional instruction tracing:
0  Conditional instruction tracing is not supported.

TRCBB, [5]

Support for branch broadcast tracing:
1  Branch broadcast tracing is implemented.

TRCDATA, [4:3]

Conditional tracing field:
0b00  Tracing of data addresses and data values is not implemented.

INSTP0, [2:1]

P0 tracing support field:
0b00  Tracing of load and store instructions as P0 elements is not supported.

[0]

Reserved, RES1.

The TRCIDR0 can be accessed through the external debug interface, offset 0x1E0.
C10.33 ID Register 1

The TRCIDR1 characteristics are:

**Purpose**

Returns the base architecture of the trace unit.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary on page C10-503*.

![TRCIDR1 bit assignments](image)

**DESIGNER, [31:24]**

Indicates which company designed the trace unit:

0x41 Arm.

**[23:16]**

Reserved, RES0.

**[15:12]**

Reserved, RES1.

**TRCARCHMAJ, [11:8]**

Major trace unit architecture version number:

0b0100 ETMv4.

**TRCARCHMIN, [7:4]**

Minor trace unit architecture version number:

0b0000 Minor revision 0.

**REVISION, [3:0]**

Implementation revision number:

0x2 r1p0.

The TRCIDR1 can be accessed through the external debug interface, offset 0x1E4.
**C10.34 ID Register 2**

The TRCIDR2 characteristics are:

**Purpose**

Returns the maximum size of the following parameters in the trace unit:
- Cycle counter.
- Data value.
- Data address.
- VMID.
- Context ID.
- Instruction address.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>29</th>
<th>28</th>
<th>25</th>
<th>24</th>
<th>20</th>
<th>19</th>
<th>15</th>
<th>14</th>
<th>10</th>
<th>9</th>
<th>5</th>
<th>4</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>CCSIZE</td>
<td>DVSIZE</td>
<td>DASIZE</td>
<td>VMIDSIZE</td>
<td>CIDSIZE</td>
<td>IASIZE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure C10-33 TRCIDR2 bit assignments**

[31:29]

Reserved, RES0.

**CCSIZE, [28:25]**

Size of the cycle counter in bits minus 12:
- 0x0 The cycle counter is 12 bits in length.

**DVSIZE, [24:20]**

Data value size in bytes:
- 0x0 Data value tracing is not implemented.

**DASIZE, [19:15]**

Data address size in bytes:
- 0x0 Data address tracing is not implemented.

**VMIDSIZE, [14:10]**

Virtual Machine ID size:
- 0x1 Virtual Machine ID is 8 bits.

**CIDSIZE, [9:5]**

Context ID size in bytes:
- 0x4 Maximum of 32-bit Context ID size.

**IASIZE, [4:0]**

Instruction address size in bytes:
\(0x8\) Maximum of 64-bit address size.

The TRCIDR2 can be accessed through the external debug interface, offset \(0x1E8\).
The TRCIDR3 characteristics are:

**Purpose**
Indicates:
- Whether TRCVICTLR is supported.
- The number of cores available for tracing.
- If an exception level supports instruction tracing.
- The minimum threshold value for instruction trace cycle counting.
- Whether the synchronization period is fixed.
- Whether TRCSTALLCTLR is supported and if so whether it supports trace overflow prevention and supports stall control of the processor.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![TRCIDR3 bit assignments](image)

**NOOVERFLOW, [31]**
Indicates whether TRCSTALLCTLR.NOOVERFLOW is implemented:
- `0` TRCSTALLCTLR.NOOVERFLOW is not implemented.

**NUMPROC, [30:28]**
Indicates the number of cores available for tracing:
- `0b000` The trace unit can trace one processor, ETM trace unit sharing not supported.

**SYSSTALL, [27]**
Indicates whether stall control is implemented:
- `1` The system supports processor stall control.

**STALLCTL, [26]**
Indicates whether TRCSTALLCTLR is implemented:
- `1` TRCSTALLCTLR is implemented.

This field is used in conjunction with SYSSTALL.
SYNCPR, [25]
Indicates whether there is a fixed synchronization period:
0 TRCSYNCPR is read-write so software can change the synchronization period.

TRCERR, [24]
Indicates whether TRCVIDCTLR.TRCERR is implemented:
1 TRCVIDCTLR.TRCERR is implemented.

EXLEVEL NS, [23:20]
Each bit controls whether instruction tracing in Non-secure state is implemented for the corresponding exception level:
0b0111 Instruction tracing is implemented for Non-secure EL0, EL1 and EL2 exception levels.

EXLEVEL S, [19:16]
Each bit controls whether instruction tracing in Secure state is implemented for the corresponding exception level:
0b1011 Instruction tracing is implemented for Secure EL0, EL1 and EL3 exception levels.

[15:12]
Reserved, RES0.

CCITMIN, [11:0]
The minimum value that can be programmed in TRCCCTLR.THRESHOLD:
0x000 Instruction trace cycle counting minimum threshold is 4.

The TRCIDR3 can be accessed through the external debug interface, offset \texttt{0x1EC}. 
The TRCIDR4 characteristics are:

**Purpose**
Indicates the resources available in the ETM trace unit.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

![Figure C10-35 TRCIDR4 bit assignments](image)

**NUMVMIDC, [31:28]**
Indicates the number of VMID comparators available for tracing:
- 0x1 One VMID comparator is available.

**NUMCIDC, [27:24]**
Indicates the number of CID comparators available for tracing:
- 0x1 One Context ID comparator is available.

**NUMSSCC, [23:20]**
Indicates the number of single-shot comparator controls available for tracing:
- 0x1 One single-shot comparator control is available.

**NUMRSPAIR, [19:16]**
Indicates the number of resource selection pairs available for tracing:
- 0x7 Eight resource selection pairs are available.

**NUMPC, [15:12]**
Indicates the number of processor comparator inputs available for tracing:
- 0x0 Processor comparator inputs are not implemented.

**[11:9]**
Reserved, RES0.

**SUPPDAC, [8]**
Indicates whether the implementation supports data address comparisons: This value is:
- 0 Data address comparisons are not implemented.

**NUMDVC, [7:4]**
Indicates the number of data value comparators available for tracing:
0x0  Data value comparators not implemented.

**NUMACPPAIRS, [3:0]**

  Indicates the number of address comparator pairs available for tracing:

  0x4  Four address comparator pairs are implemented.

The TRCIDR4 can be accessed through the external debug interface, offset 0x1F0.
C10.37  ID Register 5

The TRCIDR5 characteristics are:

**Purpose**

Returns how many resources the trace unit supports.

**Usage constraints**

There are no usage constraints.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary on page C10-503.*

![Figure C10-36 TRCIDR5 bit assignments](image)

**REDFUNCNTR, [31]**

Reduced Function Counter implemented:

0 Reduced Function Counter not implemented.

**NUMCCNTR, [30:28]**

Number of counters implemented:

0b010 Two counters implemented.

**NUMSEQSTATE, [27:25]**

Number of sequencer states implemented:

0b100 Four sequencer states implemented.

[24]

Reserved, RES0.

**LPOVERRIDE, [23]**

Low-power state override support:

1 Low-power state override support implemented.

**ATBTRIG, [22]**

ATB trigger support:

1 ATB trigger support implemented.

**TRACEIDSIZE, [21:16]**

Number of bits of trace ID:
0x07  Seven-bit trace ID implemented.

[15:12]
Reserved, \texttt{RES0}.

\textbf{NUMEXTINSEL, [11:9]}
Number of external input selectors implemented:
\texttt{0b100}  Four external input selectors implemented.

\textbf{NUMEXTIN, [8:0]}
Number of external inputs implemented:
\texttt{0x1E}  30 external inputs implemented.

The TRCIDR5 can be accessed through the external debug interface, offset \texttt{0x1F4}. 
C10.38 Resource Selection Control Registers 2-16

The TRCRSCTLRn characteristics are:

**Purpose**
Controls the trace resources.

There are eight resource pairs, the first pair is predefined as \{0,1,pair=0\} and having reserved select registers. This leaves seven pairs to be implemented as programmable selectors.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>22 21 20 19 18 16 15</th>
<th>8 7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Group</td>
<td>RES0</td>
<td>Select</td>
</tr>
</tbody>
</table>

PAIRINV, [21]
Inverts the result of a combined pair of resources.
This bit is implemented only on the lower register for a pair of resource selectors.

INV, [20]
Inverts the selected resources:
0 Resource is not inverted.
1 Resource is inverted.

[19]
Reserved, RES0.

GROUP, [18:16]
Selects a group of resources. See the *Arm® ETM Architecture Specification, ETMv4* for more information.

[15:8]
Reserved, RES0.

SELECT, [7:0]
Selects one or more resources from the required group. One bit is provided for each resource from the group.

The TRCRSCTLRn can be accessed through the external debug interface, offset 0x208-023C.
C10.39 Single-Shot Comparator Control Register 0

The TRCSSCCR0 characteristics are:

**Purpose**
Controls the single-shot comparator.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-38 TRCSSCCR0 bit assignments](image)

- **[31:25]**
  Reserved, RES0.

- **RST, [24]**
  Enables the single-shot comparator resource to be reset when it occurs, to enable another comparator match to be detected:
  
  1. Reset enabled. Multiple matches can occur.

- **[23:20]**
  Reserved, RES0.

- **ARC, [19:16]**
  Selects one or more address range comparators for single-shot control.
  
  One bit is provided for each implemented address range comparator.

- **[15:8]**
  Reserved, RES0.

- **SAC, [7:0]**
  Selects one or more single address comparators for single-shot control.
  
  One bit is provided for each implemented single address comparator.

The TRCSSCCR0 can be accessed through the external debug interface, offset 0x280.
C10.40 Single-Shot Comparator Status Register 0

The TRCSSCSR0 characteristics are:

**Purpose**
Indicates the status of the single-shot comparator. TRCSSCSR0 is sensitive to instruction addresses.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- The STATUS bit value is stable only when TRCSTATR.PMSTABLE==1.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![TRCSSCSR0 bit assignments](image)

**STATUS, [31]**
Single-shot status. This indicates whether any of the selected comparators have matched:

0  Match has not occurred.
1  Match has occurred at least once.

When programming the ETM trace unit, if TRCSSCCRN.RST is b0, the STATUS bit must be explicitly written to 0 to enable this single-shot comparator control.

**[30:3]**
Reserved, RES0.

**DV, [2]**
Data value comparator support:

0  Single-shot data value comparisons not supported.

**DA, [1]**
Data address comparator support:

0  Single-shot data address comparisons not supported.

**INST, [0]**
Instruction address comparator support:

1  Single-shot instruction address comparisons supported.

The TRCSSCSR0 can be accessed through the external debug interface, offset 0x2A0.
C10.41 OS Lock Access Register

The TRCOSLAR characteristics are:

**Purpose**
Sets and clears the OS Lock, to lock out external debugger accesses to the ETM trace unit registers.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See [C10.1 ETM register summary on page C10-503](#).

![TRCOSLAR bit assignments](image)

**OSLK, [0]**
OS Lock key value:
- 0 Unlock the OS Lock.
- 1 Lock the OS Lock.

The TRCOSLAR can be accessed through the external debug interface, offset 0x300.
**C10.42 OS Lock Status Register**

The TRCOSLSR characteristics are:

**Purpose**
Returns the status of the OS Lock.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

\[
\begin{array}{cccccc}
31 & 30 & 29 & 28 & 4 & 3 & 2 & 1 & 0 \\
\hline
\text{RES0} & & & & & & & & \\
\hline
\text{OSLM}[1] & nTT & OSLK & OSLM[0] \\
\end{array}
\]

**Figure C10-41 TRCOSLSR bit assignments**

- **[31:4]** TRCOSCTLR
- **OSLM[1], [3]**
  - OS Lock model [1] bit. This bit is combined with OSLM[0] to form a two-bit field that indicates the OS Lock model is implemented.
  - The value of this field is always 0b10, indicating that the OS Lock is implemented.
- **nTT, [2]**
  - This bit is RAZ, that indicates that software must perform a 32-bit write to update the TRCOSLAR.
- **OSLK, [1]**
  - OS Lock status bit:
    - 0 OS Lock is unlocked.
    - 1 OS Lock is locked.
- **OSLM[0], [0]**
  - OS Lock model [0] bit. This bit is combined with OSLM[1] to form a two-bit field that indicates the OS Lock model is implemented.
  - The value of this field is always 0b10, indicating that the OS Lock is implemented.

The TRCOSLSR can be accessed through the external debug interface, offset 0x304.
C10.43 Power Down Control Register

The TRCPDCR characteristics are:

**Purpose**
Request to the system power controller to keep the ETM trace unit powered up.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See [C10.1 ETM register summary on page C10-503](#).

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:4]</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>PU, [3]</td>
<td>Powerup request, to request that power to the ETM trace unit and access to the trace registers is maintained:</td>
</tr>
<tr>
<td>0</td>
<td>Power not requested.</td>
</tr>
<tr>
<td>1</td>
<td>Power requested.</td>
</tr>
<tr>
<td>This bit is reset to 0 on a trace unit reset.</td>
<td></td>
</tr>
<tr>
<td>[2:0]</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

The TRCPDCR can be accessed through the external debug interface, offset 0x310.
C10.44 Power Down Status Register

The TRCPDSR characteristics are:

**Purpose**
Indicates the power down status of the ETM trace unit.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

```
[31:6]
Reserved, RES0.

OSLK, [5]
OS lock status.
0  The OS Lock is unlocked.
1  The OS Lock is locked.

[4:2]
Reserved, RES0.

STICKYPD, [1]
Sticky power down state.
0  Trace register power has not been removed since the TRCPDSR was last read.
1  Trace register power has been removed since the TRCPDSR was last read.

This bit is set to 1 when power to the ETM trace unit registers is removed, to indicate that programming state has been lost. It is cleared after a read of the TRCPDSR.

POWER, [0]
Indicates the ETM trace unit is powered:
0  ETM trace unit is not powered. The trace registers are not accessible and they all return an error response.
1  ETM trace unit is powered. All registers are accessible.

If a system implementation allows the ETM trace unit to be powered off independently of the debug power domain, the system must handle accesses to the ETM trace unit appropriately.

The TRCPDSR can be accessed through the external debug interface, offset 0x314.
C10.45  Address Comparator Value Registers 0-7

The TRCACVRn characteristics are:

**Purpose**
Indicates the address for the address comparators.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

ADDRESS, [63:0]
The address value to compare against.

The TRCACVRn can be accessed through the external debug interface, offset 0x400-0x43C.
C10.46 Address Comparator Access Type Registers 0-7

The TRCACATRn characteristics are:

**Purpose**
Controls the access for the corresponding address comparators.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- If software uses two single address comparators as an address range comparator then it must program the corresponding TRCACATR registers with identical values in the following fields:
  - TYPE
  - CONTEXTTYPE
  - EXLEVEL_S
  - EXLEVEL_NS

**Configurations**
Available in all configurations.

**Attributes**
See C10.1 ETM register summary on page C10-503.

![Figure C10-45 TRCACATRn bit assignments](image)

**[63:16]**
Reserved, RES0.

**EXLEVEL_NS, [15:12]**
Each bit controls whether a comparison can occur in Non-secure state for the corresponding exception level. The possible values are:

0  The trace unit can perform a comparison, in Non-secure state, for exception level $n$.
1  The trace unit does not perform a comparison, in Non-secure state, for exception level $n$.

The exception levels are:

**Bit[12]**  Exception level 0.
**Bit[13]**  Exception level 1.
**Bit[14]**  Exception level 2.
**Bit[15]**  Always RES0.

**EXLEVEL_S, [11:8]**
Each bit controls whether a comparison can occur in Secure state for the corresponding exception level. The possible values are:

0  The trace unit can perform a comparison, in Secure state, for exception level $n$.
1  The trace unit does not perform a comparison, in Secure state, for exception level $n$.

The exception levels are:
**Bit[8]** Exception level 0.

**Bit[9]** Exception level 1.

**Bit[10]** Always RES0.

**Bit[11]** Exception level 3.

[7:4]
Reserved, RES0.

**Context type, [3:2]**

Controls whether the trace unit performs a Context ID comparison, a VMID comparison, or both comparisons:

- 0b00 The trace unit does not perform a Context ID comparison.
- 0b01 The trace unit performs a Context ID comparison using the Context ID comparator that the CONTEXT field specifies, and signals a match if both the Context ID comparator matches and the address comparator match.
- 0b10 The trace unit performs a VMID comparison using the VMID comparator that the CONTEXT field specifies, and signals a match if both the VMID comparator and the address comparator match.
- 0b11 The trace unit performs a Context ID comparison and a VMID comparison using the comparators that the CONTEXT field specifies, and signals a match if the Context ID comparator matches, the VMID comparator matches, and the address comparator matches.

**Type, [1:0]**

The type of comparison:

- 0b00 Instruction address, RES0.

The TRCACATRn can be accessed through the external debug interface, offset 0x480-0x488.
C10.47 Context ID Comparator Value Register 0

The TRCCIDCVR0 characteristics are:

**Purpose**
Contains a Context ID value.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-46 TRCCIDCVR0 bit assignments](image)

**[63:32]**
Reserved, RES0.

**VALUE, [31:0]**
The data value to compare against.

The TRCCIDCVR0 can be accessed through the external debug interface, offset 0x600.
C10.48  VMID Comparator Value Register 0

The TRCVMIDCVR0 characteristics are:

**Purpose**
Contains a VMID value.

**Usage constraints**
Accepts writes only when the trace unit is disabled.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-47  TRCVMIDCVR0 bit assignments](image)

### Bit assignments

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7-0</td>
<td>VALUE, [7:0]</td>
</tr>
</tbody>
</table>

The VMID value.

The TRCVMIDCVR0 can be accessed through the external debug interface, offset 0x640.
C10.49 Context ID Comparator Control Register 0

The TRCCIDCCTLR0 characteristics are:

**Purpose**
Controls the mask value for the context ID comparators.

**Usage constraints**
- Accepts writes only when the trace unit is disabled.
- If software uses the TRCCIDCVR\textsubscript{n} registers, where \(n=0\) to \(3\), then it must program this register.
- If software sets a mask bit to 1 then it must program the relevant byte in TRCCIDCVR\textsubscript{n} to \(0x00\).

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | COMPO
    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0
```

**Figure C10-48 TRCCIDCCTLR0 bit assignments**

[31:4]
Reserved, RES0.

**COMP0, [3:0]**
Controls the mask value that the trace unit applies to TRCCIDCVR0. Each bit in this field corresponds to a byte in TRCCIDCVR0. When a bit is:

- 0 The trace unit includes the relevant byte in TRCCIDCVR0 when it performs the Context ID comparison.
- 1 The trace unit ignores the relevant byte in TRCCIDCVR0 when it performs the Context ID comparison.

The TRCCIDCCTLR0 can be accessed through the external debug interface, offset \(0x680\).
C10.50 Integration ATB Identification Register

The TRCITATBIDR characteristics are:

**Purpose**
Sets the state of output pins shown in the following table.

**Usage constraints**
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

![Figure C10-49 TRCITATBIDR bit assignments](image)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>7</th>
<th>6</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ID</td>
</tr>
</tbody>
</table>

[31:7]
Reserved. Read undefined.

ID, [6:0]
Drives the ATIDMn[6:0] output pins.
- When a bit is set to 0, the corresponding output pin is LOW.
- When a bit is set to 1, the corresponding output pin is HIGH.

The TRCITATBIDR bit values correspond to the physical state of the output pins.

The TRCITATBIDR can be accessed through the external debug interface, offset $0x$EE4.
C10.51 Integration Instruction ATB Data Register

The TRCITIDATAR characteristics are:

**Purpose**
Sets the state of the ATDATAMn output pins shown in the following table.

**Usage constraints**
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-50 TRCITIDATAR bit assignments](image)

For all non-reserved bits:
- When a bit is set to 0, the corresponding output pin is LOW.
- When a bit is set to 1, the corresponding output pin is HIGH.
- The TRCITDDATAR bit values correspond to the physical state of the output pins.

<table>
<thead>
<tr>
<th>[31:5]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

ATDATAM[31], [4]
Drives the ATDATAM[31] output.

ATDATAM[23], [3]
Drives the ATDATAM[23] output.

ATDATAM[15], [2]

ATDATAM[7], [1]

ATDATAM[0], [0]
Drives the ATDATAM[0] output.

The TRCITIDATAR can be accessed through the external debug interface, offset 0xEEC.
C10.52 Integration Instruction ATB In Register

The TRCITIATBINR characteristics are:

**Purpose**
Reads the state of the input pins shown in the following table.

**Usage constraints**
- Available when bit[0] of TRCITCTRL is set to 1.
- The values of the register bits depend on the signals on the input pins when the register is read.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-51 TRCITIATBINR bit assignments](image)

For all non-reserved bits:
- When an input pin is LOW, the corresponding register bit is 0.
- When an input pin is HIGH, the corresponding register bit is 1.
- The TRCITIATBINR bit values always correspond to the physical state of the input pins.

[31:2]
Reserved. Read undefined.

**AFVALIDM, [1]**
Returns the value of the AFVALIDMn input pin.

**ATREADYM, [0]**
Returns the value of the ATREADYMn input pin.

The TRCITIATBINR can be accessed through the external debug interface, offset 0xEF4.
C10.53 Integration Instruction ATB Out Register

The TRCITIATBOUTR characteristics are:

**Purpose**
Sets the state of the output pins shown in the following table.

**Usage constraints**
- Available when bit[0] of TRCITCTRL is set to 1.
- The value of the register sets the signals on the output pins when the register is written.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-52 TRCITIATBOUTR bit assignments](image)

For all non-reserved bits:
- When a bit is set to 0, the corresponding output pin is LOW.
- When a bit is set to 1, the corresponding output pin is HIGH.
- The TRCITIATBOUTR bit values always correspond to the physical state of the output pins.

[31:10]
Reserved. Read undefined.

BYTES, [9:8]
Drives the ATBYTESMn[1:0] output pins.

[7:2]
Reserved. Read undefined.

AFREADY, [1]
Drives the AFREADYMn output pin.

ATVALID, [0]
Drives the ATVALIDMn output pin.

The TRCITIATBOUTR can be accessed through the external debug interface, offset 0xEFC.
C10.54 Integration Mode Control Register

The TRCITCTRL characteristics are:

**Purpose**

Enables topology detection or integration testing, by putting the ETM trace unit into integration mode.

**Usage constraints**

Arm recommends that you perform a debug reset after using integration mode.

**Configurations**

Available in all configurations.

**Attributes**

See *C10.1 ETM register summary on page C10-503.*

![Figure C10-53 TRCITCTRL bit assignments](image)

- **[31:1]** Reserved, RES0.
- **IME, [0]**
  
  Integration mode enable bit. The possible values are:
  
  0  The trace unit is not in integration mode.
  1  The trace unit is in integration mode. This mode enables:
      • A debug agent to perform topology detection.
      • SoC test software to perform integration testing.

The TRCITCTRL can be accessed through the external debug interface, offset 0xF00.
**C10.55 Claim Tag Set Register**

The TRCCLAIMSET characteristics are:

**Purpose**
Sets bits in the claim tag and determines the number of claim tag bits implemented.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-54 TRCCLAIMSET bit assignments](image)

- **[31:4]** Reserved, RES0.
- **SET, [3:0]**
  - On reads, for each bit:
    - 0 Claim tag bit is not implemented.
    - 1 Claim tag bit is implemented.
  - On writes, for each bit:
    - 0 Has no effect.
    - 1 Sets the relevant bit of the claim tag.

The TRCCLAIMSET can be accessed through the external debug interface, offset 0xFA0.
C10.56 Claim Tag Clear Register

The TRCCLAIMCLR characteristics are:

**Purpose**
Cleans bits in the claim tag and determines the current value of the claim tag.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*.

![Figure C10-55 TRCCLAIMCLR bit assignments](image)

- [31:4] Reserved, RES0.
- **CLR, [3:0]**
  - On reads, for each bit:
    - 0 Claim tag bit is not set.
    - 1 Claim tag bit is set.
  - On writes, for each bit:
    - 0 Has no effect.
    - 1 Clears the relevant bit of the claim tag.

The TRCCLAIMCLR can be accessed through the external debug interface, offset 0xFA4.
C10.57 Device Affinity Register 0

The TRCDEVAFF0 characteristics are:

Purpose

Provides an additional core identification mechanism for scheduling purposes in a cluster.
TRCDEVAFF0 is a read-only copy of MPIDR accessible from the external debug interface.

Usage constraints

This register is accessible as follows:

<table>
<thead>
<tr>
<th>EL0 (NS)</th>
<th>EL0 (S)</th>
<th>EL1 (NS)</th>
<th>EL1 (S)</th>
<th>EL2 (SCR.NS = 1)</th>
<th>EL3 (SCR.NS = 0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

Configurations

The TRCDEVAFF0 is architecturally mapped to external TRCDEVAFF0 register.
There is one copy of this register that is used in both Secure and Non-secure states.

Attributes

TRCDEVAFF0 is a 32-bit register.

<table>
<thead>
<tr>
<th>31 30 29</th>
<th>25 24 23</th>
<th>16 15</th>
<th>8 7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>M U RES0</td>
<td>Aff2</td>
<td>Aff1</td>
<td>Aff0</td>
<td></td>
</tr>
</tbody>
</table>

Figure C10-56 TRCDEVAFF0 bit assignments

M, [31]

Reserved, RES1.

U, [30]

Indicates a single core system, as distinct from core 0 in a cluster. This value is:

0 Processor is part of a multiprocessor system. This is the value for implementations with more than one core, and for implementations with an ACE or CHI master interface.

1 Processor is part of a uniprocessor system. This is the value for single core implementations with an AXI master interface.

[29:25]

Reserved, RES0.

MT, [24]

Indicates whether the lowest level of affinity consists of logical cores that are implemented using a multi-threading type approach. This value is:

0 Performance of cores at the lowest affinity level is largely independent.

Aff2, [23:16]

Affinity level 2. Second highest level affinity field.
Indicates the value read in the CLUSTERIDAFF2 configuration signal.
**Aff1, [15:8]**

Affinity level 1. Third highest level affinity field.

Indicates the value read in the **CLUSTERIDAFF1** configuration signal.

**Aff0, [7:0]**

Affinity level 0. Lowest level affinity field.

Indicates the core number in the Cortex-A32 processor. The possible values are:

- 0x0       A processor with one core only.
- 0x0, 0x1   A cluster with two cores.
- 0x0, 0x1, 0x2  A cluster with three cores.
- 0x0, 0x1, 0x2, 0x3  A cluster with four cores.

To access the TRCDEV AFF0:

```
MRC p15,0,<Rt>,c0,c0,5 ; Read TRCDEVAFF0 into Rt
```

Register access is encoded as follows:

**Table C10-2  TRCDEVAFF0 access encoding**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1111</td>
<td>000</td>
<td>0000</td>
<td>0000</td>
<td>101</td>
</tr>
</tbody>
</table>

The TRCDEVAFF0 can be accessed through the external debug interface, offset 0xFA8.
C10.58 Device Affinity Register 1

The TRCDEVAFF1 characteristics are:

**Purpose**

The value is a read-only copy of MPIDR_EL1[63:32] as seen from EL3, unaffected by VMPIDR_EL2.

**Usage constraints**

Accessible only from the external debug interface.

**Configurations**

Available in all configurations.

**Attributes**

TRCDEVAFF1 is a 32-bit RO management register.

For the Cortex-A32 processor, MPIDR_EL1[63:32] is RES0.

See *C10.1 ETM register summary* on page C10-503.

The TRCDEVAFF1 can be accessed through the external debug interface, offset 0xFAC.
C10.59 Software Lock Access Register

The TRCLAR characteristics are:

**Purpose**

Controls access to registers using the memory-mapped interface, when PADDRDBG31 is LOW.

When the software lock is set, write accesses using the memory-mapped interface to all ETM trace unit registers are ignored, except for write accesses to the TRCLAR.

When the software lock is set, read accesses of TRCPDSR do not change the TRCPDSR.STICKYPD bit. Read accesses of all other registers are not affected.

**Usage constraints**

Accessible only from the memory-mapped interface.

**Configurations**

Available in all configurations.

**Attributes**

See [C10.1 ETM register summary on page C10-503](#).

![Figure C10-57 TRCLAR bit assignments](#)

**KEY, [31:0]**

Software lock key value:

0xC5ACCE55 Clear the software lock.

All other write values set the software lock.

The TRCLAR can be accessed through the external debug interface, offset 0xFB0.
**C10.60 Software Lock Status Register**

The TRCLSR characteristics are:

**Purpose**
Determines whether the software lock is implemented, and indicates the current status of the software lock.

**Usage constraints**
Accessible only from the external debug interface.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503*. 

![Figure C10-58 TRCLSR bit assignments](image)

**[31:3]**
Reserved, RES0.

**nTT, [2]**
Indicates size of TRCLAR:
- 0 TRCLAR is always 32 bits.

**SLK, [1]**
Software lock status:
- 0 Software lock is clear.
- 1 Software lock is set.

**SLI, [0]**
Indicates whether the software lock is implemented on this interface.
- 1 Software lock is implemented on this interface.

The TRCLSR can be accessed through the external debug interface, offset 0xFB4.
C10.61 Authentication Status Register

The TRAUTHSTATUS characteristics are:

**Purpose**
Indicates the current level of tracing permitted by the system.

**Usage constraints**
There are no usage constraints.

**Configurations**
Available in all configurations.

**Attributes**
See *C10.1 ETM register summary on page C10-503.*

![Figure C10-59 TRAUTHSTATUS bit assignments](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:8]</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>SNID, [7:6]</td>
<td>Secure Non-invasive Debug:</td>
</tr>
<tr>
<td></td>
<td>θb10 Secure Non-invasive Debug implemented but disabled.</td>
</tr>
<tr>
<td></td>
<td>θb11 Secure Non-invasive Debug implemented and enabled.</td>
</tr>
<tr>
<td>SID, [5:4]</td>
<td>Secure Invasive Debug:</td>
</tr>
<tr>
<td></td>
<td>θbθθ Secure Invasive Debug is not implemented.</td>
</tr>
<tr>
<td>NSNID, [3:2]</td>
<td>Non-secure Non-invasive Debug:</td>
</tr>
<tr>
<td></td>
<td>θb10 Non-secure Non-invasive Debug implemented but disabled, NIDEN=0.</td>
</tr>
<tr>
<td></td>
<td>θb11 Non-secure Non-invasive Debug implemented and enabled, NIDEN=1.</td>
</tr>
<tr>
<td>NSID, [1:0]</td>
<td>Non-secure Invasive Debug:</td>
</tr>
<tr>
<td></td>
<td>θbθθ Non-secure Invasive Debug is not implemented.</td>
</tr>
</tbody>
</table>

The TRAUTHSTATUS can be accessed through the external debug interface, offset 0xFB8.
C10.62 Device Architecture Register

The TRCDEVARCH characteristics are:

**Purpose**
- Identifies the ETM trace unit as an ETMv4 component.

**Usage constraints**
- There are no usage constraints.

**Configurations**
- Available in all configurations.

**Attributes**
- See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>21 20</th>
<th>16 15</th>
<th>14</th>
<th>13</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARCHITECT</td>
<td>REVISION</td>
<td>ARCHID</td>
<td>PRESENT</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ARCHITECT, [31:21]**
- Defines the architect of the component:
  - 0x4  Arm JEP continuation.
  - 0x3B  Arm JEP 106 code.

**PRESENT, [20]**
- Indicates the presence of this register:
  - 0b1  Register is present.

**REVISION, [19:16]**
- Architecture revision:
  - 0b0000  Architecture revision 0.

**ARCHID, [15:0]**
- Architecture ID:
  - 0x4A13  ETMv4 component.

The TRCDEVARCH can be accessed through the external debug interface, offset 0xFBC.
C10.63 Device ID Register

The TRCDEVID characteristics are:

**Purpose**
- Indicates the capabilities of the ETM trace unit.

**Usage constraints**
- There are no usage constraints.

**Configurations**
- Available in all configurations.

**Attributes**
- See [C10.1 ETM register summary on page C10-503](#).

![Figure C10-61 TRCDEVID bit assignments](image)

DEVID, [31:0]
- RAZ. There are no component-defined capabilities.

The TRCDEVID can be accessed through the external debug interface, offset 0xFC8.
C10.64 Device Type Register

The TRCDEVTYPE characteristics are:

**Purpose**
Indicates the type of the component.

**Usage constraints**
Accessible only from the external debug interface.

**Configurations**
Available in all configurations.

**Attributes**
*C10.1 ETM register summary on page C10-503.*

```
<table>
<thead>
<tr>
<th>31</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>SUB</td>
<td>MAJOR</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Figure C10-62 TRCDEVTYPE bit assignments**

[31:8]
Reserved, RES0.

**SUB, [7:4]**
The sub-type of the component:
0b0001 Processor trace.

**MAJOR, [3:0]**
The main type of the component:
0b0011 Trace source.

The TRCDEVTYPE can be accessed through the external debug interface, offset 0xFCC.
C10.65  ETM Peripheral Identification Registers

The ETM Peripheral Identification Registers provide standard information required for all CoreSight components.

The following table lists the Peripheral ID Registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peripheral ID4</td>
<td>0x04</td>
<td>0xFD0</td>
</tr>
<tr>
<td>Peripheral ID5</td>
<td>0x00</td>
<td>0xFD4</td>
</tr>
<tr>
<td>Peripheral ID6</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>Peripheral ID7</td>
<td>0x00</td>
<td>0xFDC</td>
</tr>
<tr>
<td>Peripheral ID0</td>
<td>0xDB</td>
<td>0xFE0</td>
</tr>
<tr>
<td>Peripheral ID1</td>
<td>0xB9</td>
<td>0xFE4</td>
</tr>
<tr>
<td>Peripheral ID2</td>
<td>0x2B</td>
<td>0xFE8</td>
</tr>
<tr>
<td>Peripheral ID3</td>
<td>0x00</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Only bits[7:0] of each Peripheral ID Register are used, with bits[31:8] reserved. Together, the eight Peripheral ID Registers define a single 64-bit Peripheral ID.
The TRCPIDR0 characteristics are:

**Purpose**

Provides information to identify a trace component.

**Usage constraints**

- Only bits[7:0] are valid.
- Accessible only from the external debugger interface, offset 0xFE0.

**Configurations**

Available in all implementations.

**Attributes**

TRCPIDR0 is a 32-bit RO management register.

See *C10.1 ETM register summary* on page C10-503.

```
<table>
<thead>
<tr>
<th>31</th>
<th>8</th>
<th>7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td>Part_0</td>
</tr>
</tbody>
</table>
```

**Figure C10-63 TRCPIDR0 bit assignments**

[31:8]

Reserved, RES0.

**Part_0, [7:0]**

\(0xDB\)  Least significant byte of the ETM trace unit part number.
C10.67 ETM Peripheral Identification Register 1

The TRCPIDR1 characteristics are:

Purpose
Provides information to identify a trace component.

Usage constraints
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFE4.

Configurations
Available in all implementations.

Attributes
TRCPIDR1 is a 32-bit RO management register.

See C10.1 ETM register summary on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>DES_0</td>
<td>Part_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[31:8]
Reserved, RES0.

DES_0, [7:4]
0xB Arm Limited. This is bits[3:0] of JEP106 ID code.

Part_1, [3:0]
0x9 Most significant four bits of the ETM trace unit part number.
C10.68 ETM Peripheral Identification Register 2

The TRCPIDR2 characteristics are:

**Purpose**
Provides information to identify a trace component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFE8.

**Configurations**
Available in all implementations.

**Attributes**
TRCPIDR2 is a 32-bit RO management register.

See *C10.1 ETM register summary* on page C10-503.

![Figure C10-65 TRCPIDR2 bit assignments](image)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7:4</td>
<td>Revision, ox2 r1p0.</td>
</tr>
<tr>
<td>3</td>
<td>JEDEC, 0b1 RES1. Indicates a JEP106 identity code is used.</td>
</tr>
<tr>
<td>2:0</td>
<td>DES_1, 0b011 Arm Limited. This is bits[6:4] of JEP106 ID code.</td>
</tr>
</tbody>
</table>
ETM Peripheral Identification Register 3

The TRCPIDR3 characteristics are:

**Purpose**
Provides information to identify a trace component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFEC.

**Configurations**
Available in all implementations.

**Attributes**
TRCPIDR3 is a 32-bit RO management register.

See *C10.1 ETM register summary* on page C10-503.

![Figure C10-66 TRCPIDR3 bit assignments](image)

[31:8]
Reserved, RES0.

**REVAND, [7:4]**

0x0 Part minor revision.

**CMOD, [3:0]**

0x0 Not customer modified.
The TRCPIDR4 characteristics are:

**Purpose**
Provides information to identify a trace component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset \(0xFD0\).

**Configurations**
Available in all implementations.

**Attributes**
TRCPIDR4 is a 32-bit RO management register.

See *C10.1 ETM register summary* on page C10-503.

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td>Size</td>
<td></td>
<td></td>
<td></td>
<td>DES_2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

![Figure C10-67 TRCPIDR4 bit assignments](image-url)

**[31:8]**
Reserved, `RES0`.

**Size, [7:4]**
\(0x0\) Size of the component. \(\log_2\) the number of 4KB pages from the start of the component to the end of the component ID registers.

**DES_2, [3:0]**
\(0x4\) Arm Limited. This is bits[3:0] of the JEP106 continuation code.
C10.71  ETM Peripheral Identification Register 5-7

No information is held in the Peripheral ID5, Peripheral ID6, and Peripheral ID7 Registers. They are reserved for future use and are RES0.
C10.72 ETM Component Identification Registers

There are four read-only ETM Component Identification Registers, Component ID0 to Component ID3.

Table C10-4 Summary of the ETM Component Identification Registers

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component ID0</td>
<td>0x0D</td>
<td>0xFF0</td>
</tr>
<tr>
<td>Component ID1</td>
<td>0x90</td>
<td>0xFF4</td>
</tr>
<tr>
<td>Component ID2</td>
<td>0x05</td>
<td>0xFF8</td>
</tr>
<tr>
<td>Component ID3</td>
<td>0xB1</td>
<td>0xFFC</td>
</tr>
</tbody>
</table>

The ETM Component Identification Registers identify ETM trace unit as a CoreSight component.
C10.73  ETM Component Identification Register 0

The TRCCIDR0 characteristics are:

**Purpose**

Provides information to identify a trace component.

**Usage constraints**

- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFF0.

**Configurations**

Available in all implementations.

**Attributes**

See *C10.1 ETM register summary* on page C10-503.

![Figure C10-68  TRCCIDR0 bit assignments](image)

[31:8]

Reserved, RES0.

PRMBL_0, [7:0]

0x0D  Preamble byte 0.
C10.74  ETM Component Identification Register 1

The TRCCIDR1 characteristics are:

**Purpose**
Provides information to identify a trace component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFF4.

**Configurations**
Available in all implementations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-69  TRCCIDR1 bit assignments](image)

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>8</th>
<th>7</th>
<th>4</th>
<th>3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CLASS</td>
<td>PRMBL_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>[31:8]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLASS, [7:4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x9</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PRMBL_1, [3:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
</tr>
</tbody>
</table>
The TRCCIDR2 characteristics are:

**Purpose**
Provides information to identify a CTI component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFF8.

**Configurations**
Available in all implementations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![TRCCIDR2 bit assignments](image-url)

**[31:8]**
Reserved, RESO.

**PRMBL_2, [7:0]**

| 0x05 | Preamble byte 2. |
The TRCCIDR3 characteristics are:

**Purpose**
Provides information to identify a trace component.

**Usage constraints**
- Only bits[7:0] are valid.
- Accessible only from the external debug interface, offset 0xFFC.

**Configurations**
Available in all implementations.

**Attributes**
See *C10.1 ETM register summary* on page C10-503.

![Figure C10-71 TRCCIDR3 bit assignments](image-url)

[31:8]
- Reserved, RES0.

**PRMBL_3, [7:0]**
- 0xB1  Preamble byte 3.
Chapter C11
CTI registers

This chapter describes the CTI registers.

It contains the following sections:

• C11.1 Cross trigger register summary on page C11-596.
• C11.2 External register access permissions to the CTI registers on page C11-598.
• C11.3 CTI Device Identification Register on page C11-599.
• C11.4 CTI Integration Mode Control Register on page C11-601.
• C11.5 CTI Peripheral Identification Registers on page C11-602.
• C11.6 CTI Peripheral Identification Register 0 on page C11-603.
• C11.7 CTI Peripheral Identification Register 1 on page C11-604.
• C11.8 CTI Peripheral Identification Register 2 on page C11-605.
• C11.9 CTI Peripheral Identification Register 3 on page C11-606.
• C11.10 CTI Peripheral Identification Register 4 on page C11-607.
• C11.11 CTI Peripheral Identification Register 5-7 on page C11-608.
• C11.12 CTI Component Identification Registers on page C11-609.
• C11.13 CTI Component Identification Register 0 on page C11-610.
• C11.14 CTI Component Identification Register 1 on page C11-611.
• C11.15 CTI Component Identification Register 2 on page C11-612.
• C11.16 CTI Component Identification Register 3 on page C11-613.
C11.1 Cross trigger register summary

This section describes the cross trigger registers in the Cortex-A32 processor. These registers are accessed through the external debug interface.

The following table gives a summary of the Cortex-A32 cross trigger registers. For those registers not described in this chapter, see the Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>CTICONTROL</td>
<td>RW</td>
<td>CTI Control Register</td>
</tr>
<tr>
<td>0x000-0x00C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x010</td>
<td>CTIINTACK</td>
<td>WO</td>
<td>CTI Output Trigger Acknowledge Register</td>
</tr>
<tr>
<td>0x014</td>
<td>CTIAPPSET</td>
<td>RW</td>
<td>CTI Application Trigger Set Register</td>
</tr>
<tr>
<td>0x018</td>
<td>CTIAPPCLEAR</td>
<td>WO</td>
<td>CTI Application Trigger Clear Register</td>
</tr>
<tr>
<td>0x01C</td>
<td>CTIAPPPULSE</td>
<td>WO</td>
<td>CTI Application Pulse Register</td>
</tr>
<tr>
<td>0x020</td>
<td>CTIINEN0</td>
<td>RW</td>
<td>CTI Input Trigger to Output Channel Enable Registers</td>
</tr>
<tr>
<td>0x024</td>
<td>CTIINEN1</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x028</td>
<td>CTIINEN2</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x02C</td>
<td>CTIINEN3</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x030</td>
<td>CTIINEN4</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x034</td>
<td>CTIINEN5</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x038</td>
<td>CTIINEN6</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x03C</td>
<td>CTIINEN7</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x040-0x09C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x0A0</td>
<td>CTIOUTEN0</td>
<td>RW</td>
<td>CTI Input Channel to Output Trigger Enable Registers</td>
</tr>
<tr>
<td>0x0A4</td>
<td>CTIOUTEN1</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0A8</td>
<td>CTIOUTEN2</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0AC</td>
<td>CTIOUTEN3</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0B0</td>
<td>CTIOUTEN4</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0B4</td>
<td>CTIOUTEN5</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0B8</td>
<td>CTIOUTEN6</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0BC</td>
<td>CTIOUTEN7</td>
<td>RW</td>
<td></td>
</tr>
<tr>
<td>0x0C0-0x12C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0x130</td>
<td>CTITRIGINSTATUS</td>
<td>RO</td>
<td>CTI Trigger In Status Register</td>
</tr>
<tr>
<td>0x134</td>
<td>CTITRIGOUTSTATUS</td>
<td>RO</td>
<td>CTI Trigger Out Status Register</td>
</tr>
<tr>
<td>0x138</td>
<td>CTICHINSTATUS</td>
<td>RO</td>
<td>CTI Channel In Status Register</td>
</tr>
<tr>
<td>0x13C</td>
<td>CTICHOUTSTATUS</td>
<td>RO</td>
<td>CTI Channel Out Status Register</td>
</tr>
<tr>
<td>0x140</td>
<td>CTIGATE</td>
<td>RW</td>
<td>CTI Channel Gate Enable Register</td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Type</td>
<td>Description</td>
</tr>
<tr>
<td>----------</td>
<td>-------------------</td>
<td>------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>0x144</td>
<td>ASICCTL</td>
<td>RW</td>
<td>CTI External Multiplexer Control Register</td>
</tr>
<tr>
<td>0x148-0xF7C</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xF00</td>
<td>CTIITCTRL</td>
<td>RW</td>
<td>C11.4 CTI Integration Mode Control Register on page C11-601</td>
</tr>
<tr>
<td>0xF04-0xFA4</td>
<td>-</td>
<td>-</td>
<td>Reserved</td>
</tr>
<tr>
<td>0xFA0</td>
<td>CTICLAIMSET</td>
<td>RW</td>
<td>CTI Claim Tag Set Register</td>
</tr>
<tr>
<td>0xFA4</td>
<td>CTICLAIMCLR</td>
<td>RW</td>
<td>CTI Claim Tag Clear Register</td>
</tr>
<tr>
<td>0xFA8</td>
<td>CTIDEVAFF0</td>
<td>RO</td>
<td>CTI Device Affinity Register 0</td>
</tr>
<tr>
<td>0xFAC</td>
<td>CTIDEVAFF1</td>
<td>RO</td>
<td>CTI Device Affinity Register 1</td>
</tr>
<tr>
<td>0xFB0</td>
<td>CTILAR</td>
<td>WO</td>
<td>CTI Lock Access Register</td>
</tr>
<tr>
<td>0xFB4</td>
<td>CTILSR</td>
<td>RO</td>
<td>CTI Lock Status Register</td>
</tr>
<tr>
<td>0xFB8</td>
<td>CTIAUTHSTATUS</td>
<td>RO</td>
<td>CTI Authentication Status Register</td>
</tr>
<tr>
<td>0xFC0</td>
<td>CTIDEVARCH</td>
<td>RO</td>
<td>CTI Device Architecture Register</td>
</tr>
<tr>
<td>0xFC4</td>
<td>CTIDEVID2</td>
<td>RO</td>
<td>CTI Device ID Register 2</td>
</tr>
<tr>
<td>0xFC8</td>
<td>CTIDEVID1</td>
<td>RO</td>
<td>CTI Device ID Register 1</td>
</tr>
<tr>
<td>0xFCC</td>
<td>CTIDEVTYPE</td>
<td>RO</td>
<td>CTI Device Type Register</td>
</tr>
<tr>
<td>0xFD0</td>
<td>CTIPIDR4</td>
<td>RO</td>
<td>C11.10 CTI Peripheral Identification Register 4 on page C11-607</td>
</tr>
<tr>
<td>0xFD4</td>
<td>CTIPIDR5</td>
<td>RO</td>
<td>C11.11 CTI Peripheral Identification Register 5-7 on page C11-608</td>
</tr>
<tr>
<td>0xFD8</td>
<td>CTIPIDR6</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFD0</td>
<td>CTIPIDR7</td>
<td>RO</td>
<td></td>
</tr>
<tr>
<td>0xFE0</td>
<td>CTIPIDR0</td>
<td>RO</td>
<td>C11.6 CTI Peripheral Identification Register 0 on page C11-603</td>
</tr>
<tr>
<td>0xFE4</td>
<td>CTIPIDR1</td>
<td>RO</td>
<td>C11.7 CTI Peripheral Identification Register 1 on page C11-604</td>
</tr>
<tr>
<td>0xFE8</td>
<td>CTIPIDR2</td>
<td>RO</td>
<td>C11.8 CTI Peripheral Identification Register 2 on page C11-605</td>
</tr>
<tr>
<td>0xFEC</td>
<td>CTIPIDR3</td>
<td>RO</td>
<td>C11.9 CTI Peripheral Identification Register 3 on page C11-606</td>
</tr>
<tr>
<td>0xFF0</td>
<td>CTICIDR0</td>
<td>RO</td>
<td>C11.13 CTI Component Identification Register 0 on page C11-610</td>
</tr>
<tr>
<td>0xFF4</td>
<td>CTICIDR1</td>
<td>RO</td>
<td>C11.14 CTI Component Identification Register 1 on page C11-611</td>
</tr>
<tr>
<td>0xFFF</td>
<td>CTICIDR2</td>
<td>RO</td>
<td>C11.15 CTI Component Identification Register 2 on page C11-612</td>
</tr>
<tr>
<td>0xFFC</td>
<td>CTICIDR3</td>
<td>RO</td>
<td>C11.16 CTI Component Identification Register 3 on page C11-613</td>
</tr>
</tbody>
</table>
C11.2 External register access permissions to the CTI registers

External access permission to the cross trigger registers is subject to the conditions at the time of the access.

The following table describes the processor response to accesses through the external debug and memory-mapped interfaces.

<table>
<thead>
<tr>
<th>Name</th>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>EDPRSR.PU is 0</td>
<td>Processor power domain is completely off, or in a low-power state where the processor power domain registers cannot be accessed.</td>
</tr>
<tr>
<td>DLK</td>
<td>EDPRSR.DLK is 1</td>
<td>OS Double Lock is locked.</td>
</tr>
<tr>
<td>OSLK</td>
<td>OSLSR_EL1.OSLK is 1</td>
<td>OS Lock is locked.</td>
</tr>
<tr>
<td>EDAD</td>
<td>AllowExternalDebugAccess() ==FALSE</td>
<td>External debug access is disabled. When an error is returned because of an EDAD condition code, and this is the highest priority error condition, EDPRSR.SDAD is set to 1. Otherwise EDPRSR.SDAD is unchanged.</td>
</tr>
<tr>
<td>SLK</td>
<td>Memory-mapped interface only</td>
<td>Software lock is locked. For the external debug interface, ignore this row.</td>
</tr>
<tr>
<td>Default</td>
<td>-</td>
<td>None of the conditions apply, normal access.</td>
</tr>
</tbody>
</table>

The following table shows an example of external register condition codes for access to a cross trigger register. To determine the access permission for the register, scan the columns from left to right. Stop at the first column a condition is true, the entry gives the access permission of the register and scanning stops.

<table>
<thead>
<tr>
<th>Name</th>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>-</td>
<td>RO/WI</td>
</tr>
<tr>
<td>DLK</td>
<td>-</td>
<td>RO</td>
</tr>
<tr>
<td>OSLK</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>EDAD</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>SLK</td>
<td>Memory-mapped interface only</td>
<td>RO</td>
</tr>
<tr>
<td>Default</td>
<td>-</td>
<td>RO</td>
</tr>
</tbody>
</table>
### C11.3 CTI Device Identification Register

The CTIDEVID characteristics are:

**Purpose**

Describes the CTI component to the debugger.

**Usage constraints**

The accessibility of CTIDEVID by condition code is:

<table>
<thead>
<tr>
<th></th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*Note: The table above is not included in the text.*

**Configurations**

CTIDEVID is in the Debug power domain.

**Attributes**

See the register summary in *C11.1 Cross trigger register summary* on page C11-596.

---

**INOUT, [25:24]**

Input and output options. Indicates the presence of an input gate. The possible values are:

- **0b00**: CTIGATE does not mask propagation of input events from external channels.
- **0b01**: CTIGATE masks propagation of input events from external channels.

**NUMCHAN, [21:16]**

Number of channels implemented. This value is:

- **0b00100**: Four channels implemented.

**NUMTRIG, [13:8]**

Number of triggers implemented. This value is:

- **0b01000**: Eight triggers implemented.

---

### Figure C11-1 CTIDEVID bit assignments

---

**Reserved, RES0**

---

**RES0**

---

**NUMCHAN, RES0**

---

**NUMTRIG, RES0**

---

**EXTMAXNUM**

---
Maximum number of external triggers implemented. This value is:

\[0b00000\]  No external triggers implemented.

CTIDEVID can be accessed through the external debug interface, offset \[\text{0xFC8}\].
C11.4 CTI Integration Mode Control Register

The CTIITCTRL characteristics are:

**Purpose**

The CTIITCTRL shows that the Cortex-A32 processor does not implement an integration mode.

**Usage constraints**

The accessibility of CTIITCTRL by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EDAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO/WI</td>
</tr>
<tr>
<td>RW</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

_C11.2 External register access permissions to the CTI registers on page C11-598_ describes the condition codes.

**Configurations**

CTIITCTRL is in the Debug power domain.

**Attributes**

See the register summary in _C11.1 Cross trigger register summary on page C11-596_.

![Figure C11-2 CTIITCTRL bit assignments](image)

[31:1]

Reserved, RES0.

IME, [0]

Integration mode enable. The possible value is:

0  Normal operation.

CTIITCTRL can be accessed through the external debug interface, offset 0xF00.
C11.5 CTI Peripheral Identification Registers

The CTI Peripheral Identification Registers provide standard information required for all components that conform to the Arm CoreSight architecture.

The following table lists the CTI Peripheral Identification Registers.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peripheral ID4</td>
<td>0x04</td>
<td>0xFD0</td>
</tr>
<tr>
<td>Peripheral ID5</td>
<td>0x00</td>
<td>0xFD4</td>
</tr>
<tr>
<td>Peripheral ID6</td>
<td>0x00</td>
<td>0xFD8</td>
</tr>
<tr>
<td>Peripheral ID7</td>
<td>0x00</td>
<td>0xFDC</td>
</tr>
<tr>
<td>Peripheral ID0</td>
<td>0xDB</td>
<td>0xFE0</td>
</tr>
<tr>
<td>Peripheral ID1</td>
<td>0xB9</td>
<td>0xFE4</td>
</tr>
<tr>
<td>Peripheral ID2</td>
<td>0x2B</td>
<td>0xFE8</td>
</tr>
<tr>
<td>Peripheral ID3</td>
<td>0x00</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Only bits[7:0] of each Peripheral ID Register are used, with bits[31:8] reserved. Together, the eight Peripheral ID Registers define a single 64-bit Peripheral ID.
C11.6 CTI Peripheral Identification Register 0

The CTIPIDR0 characteristics are:

**Purpose**
Provides information to identify a CTI component.

**Usage constraints**
The accessibility of CTIPIDR0 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

_C11.2 External register access permissions to the CTI registers on page C11-598 describes the condition codes._

**Configurations**
CTIPIDR0 is in the Debug power domain.
CTIPIDR0 is optional to implement in the external register interface.

**Attributes**
See the register summary in _C11.1 Cross trigger register summary on page C11-596._

![Figure C11-3 CTIPIDR0 bit assignments](image)

<table>
<thead>
<tr>
<th>31</th>
<th>8-7</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Part_0</td>
<td></td>
</tr>
</tbody>
</table>

**[31:8]**
Reserved, RES0.

**Part_0, [7:0]**
0x08  Least significant byte of the cross trigger part number.

CTIPIDR0 can be accessed through the external debug interface, offset 0xFE0.
C11.7 CTI Peripheral Identification Register 1

The CTIPIDR1 characteristics are:

**Purpose**

Provides information to identify a CTI component.

**Usage constraints**

The accessibility of CTIPIDR1 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**

CTIPIDR1 is in the Debug power domain.

CTIPIDR1 is optional to implement in the external register interface.

**Attributes**

See the register summary in *C11.1 Cross trigger register summary on page C11-596*.

![Figure C11-4 CTIPIDR1 bit assignments](image)

[31:8]

Reserved, RES0.

**DES_0, [7:4]**

0x8  Arm Limited. This is the least significant nibble of JEP106 ID code.

**Part_1, [3:0]**

0x9  Most significant nibble of the CTI part number.

CTIPIDR1 can be accessed through the external debug interface, offset 0xFE4.
C11.8 CTI Peripheral Identification Register 2

The CTIPIDR2 characteristics are:

**Purpose**

Provides information to identify a CTI component.

**Usage constraints**

The accessibility of CTIPIDR2 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**

CTIPIDR2 is in the Debug power domain.

CTIPIDR2 is optional to implement in the external register interface.

**Attributes**

See the register summary in *C11.1 Cross trigger register summary on page C11-596.*

![Figure C11-5 CTIPIDR2 bit assignments](image)

- **[31:8]**
  - Reserved, RES0.

- **Revision, [7:4]**
  - 0x2  r1p0.

- **JEDEC, [3]**
  - 0b1  RES1. Indicates a JEP106 identity code is used.

- **DES_1, [2:0]**
  - 0b11  Arm Limited. This is the most significant nibble of JEP106 ID code.

CTIPIDR2 can be accessed through the external debug interface, offset 0xFE8.
C11.9 CTI Peripheral Identification Register 3

The CTIPIDR3 characteristics are:

**Purpose**
Provides information to identify a CTI component.

**Usage constraints**
The accessibility of CTIPIDR3 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**
CTIPIDR3 is in the Debug power domain.
CTIPIDR3 is optional to implement in the external register interface.

**Attributes**
See the register summary in *C11.1 Cross trigger register summary* on page C11-596.

![Figure C11-6 CTIPIDR3 bit assignments](image)

[31:8]
Reserved, RES0.

**REVAND, [7:4]**
0x0 Part minor revision.

**CMOD, [3:0]**
0x0 Customer modified.

CTIPIDR3 can be accessed through the external debug interface, offset 0xFEC.
C11.10 CTI Peripheral Identification Register 4

The CTIPIDR4 characteristics are:

**Purpose**

Provides information to identify a CTI component.

**Usage constraints**

The accessibility of CTIPIDR4 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**

CTIPIDR4 is in the Debug power domain.

CTIPIDR4 is optional to implement in the external register interface.

**Attributes**

See the register summary in *C11.1 Cross trigger register summary on page C11-596*.

![Figure C11-7 CTIPIDR4 bit assignments](image)

<table>
<thead>
<tr>
<th>31:8</th>
<th>8:7</th>
<th>4:3</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Size</td>
<td>DES_2</td>
<td></td>
</tr>
</tbody>
</table>

[31:8]

Reserved, RES0.

**Size, [7:4]**

0x0  Size of the component. Log2 the number of 4KB pages from the start of the component to the end of the component ID registers.

**DES_2, [3:0]**

0x4  Arm Limited. This is the least significant nibble JEP106 continuation code.

CTIPIDR4 can be accessed through the external debug interface, offset 0xFD0.
C11.11 CTI Peripheral Identification Register 5-7

No information is held in the Peripheral ID5, Peripheral ID6, and Peripheral ID7 Registers. They are reserved for future use and are RES0.
C11.12 CTI Component Identification Registers

There are four read-only CTI Component Identification Registers, Component ID0 through Component ID3.

<table>
<thead>
<tr>
<th>Register</th>
<th>Value</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component ID0</td>
<td>(0x0D)</td>
<td>(0xFF0)</td>
</tr>
<tr>
<td>Component ID1</td>
<td>(0x90)</td>
<td>(0xFF4)</td>
</tr>
<tr>
<td>Component ID2</td>
<td>(0x05)</td>
<td>(0xFF8)</td>
</tr>
<tr>
<td>Component ID3</td>
<td>(0xB1)</td>
<td>(0xFFC)</td>
</tr>
</tbody>
</table>
C11.13 CTI Component Identification Register 0

The CTICIDR0 characteristics are:

**Purpose**

Provides information to identify a CTI component.

**Usage constraints**

The accessibility of CTICIDR0 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**

CTICIDR0 is in the Debug power domain.

CTICIDR0 is optional to implement in the external register interface.

**Attributes**

See the register summary in *C11.1 Cross trigger register summary on page C11-596*.

![Figure C11-8 CTICIDR0 bit assignments](image)

[31:8]

Reserved, RES0.

**PRMBL_0, [7:0]**

0x0D  Preamble byte 0.

CTICIDR0 can be accessed through the external debug interface, offset 0xFF0.
C11.14 CTI Component Identification Register 1

The CTICIDR1 characteristics are:

**Purpose**

Provides information to identify a CTI component.

**Usage constraints**

The accessibility of CTICIDR1 by condition code is:

<table>
<thead>
<tr>
<th>Condition Code</th>
<th>Accessibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off</td>
<td>RO</td>
</tr>
<tr>
<td>DLK</td>
<td>RO</td>
</tr>
<tr>
<td>OSLK</td>
<td>RO</td>
</tr>
<tr>
<td>EPMAD</td>
<td>RO</td>
</tr>
<tr>
<td>SLK</td>
<td>RO</td>
</tr>
<tr>
<td>Default</td>
<td>RO</td>
</tr>
</tbody>
</table>

*Figure C11-9 CTICIDR1 bit assignments*

[31:8]

Reserved, RES0.

**CLASS, [7:4]**

0x9  Debug component.

**PRMBL_1, [3:0]**

0x0  Preamble byte 1.

CTICIDR1 can be accessed through the external debug interface, offset 0xFF4.
C11.15 CTI Component Identification Register 2

The CTICIDR2 characteristics are:

Purpose
Provides information to identify a CTI component.

Usage constraints
The accessibility of CTICIDR2 by condition code is:

<table>
<thead>
<tr>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

C11.2 External register access permissions to the CTI registers on page C11-598 describes the condition codes.

Configurations
CTICIDR2 is in the Debug power domain.

CTICIDR2 is optional to implement in the external register interface.

Attributes
See the register summary in C11.1 Cross trigger register summary on page C11-596.

Figure C11-10 CTICIDR2 bit assignments

[31:8]
Reserved, RES0.

PRMBL_2, [7:0]

0x05  Preamble byte 2.

CTICIDR2 can be accessed through the external debug interface, offset 0xFFF8.
C11.16 CTI Component Identification Register 3

The CTICIDR3 characteristics are:

**Purpose**
Provides information to identify a CTI component.

**Usage constraints**
The accessibility of CTICIDR3 by condition code is:

<table>
<thead>
<tr>
<th>Condition Code</th>
<th>Off</th>
<th>DLK</th>
<th>OSLK</th>
<th>EPMAD</th>
<th>SLK</th>
<th>Default</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>RO</td>
<td>RO</td>
</tr>
</tbody>
</table>

*C11.2 External register access permissions to the CTI registers on page C11-598* describes the condition codes.

**Configurations**
CTICIDR3 is in the Debug power domain.
CTICIDR3 is optional to implement in the external register interface.

**Attributes**
See the register summary in *C11.1 Cross trigger register summary* on page C11-596.

![Figure C11-11 CTICIDR3 bit assignments](image)

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:8]</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td></td>
<td><strong>PRMBL_3</strong></td>
</tr>
</tbody>
</table>

*Reserved, RES0.*

**PRMBL_3, [7:0]**

- 0x81 Preamble byte 3.

CTICIDR3 can be accessed through the external debug interface, offset 0xFFC.
C11 CTI registers

C11.16 CTI Component Identification Register 3
Part D
Appendices
Appendix A
Signal Descriptions

This appendix describes the signals at the external interfaces of the processor.

It contains the following sections:

- A.1 About the signal descriptions on page Appx-A-618.
A.1 About the signal descriptions

The tables in this appendix provide direction information and high-level descriptions about the signals at the external interfaces of the processor.

Some of the buses include a configurable width field, <Signal>[CN:0], where CN = 0, 1, 2, or 3, to encode up to four cores. For example:

- nIRQ[0] represents a core 0 interrupt request.
- nIRQ[2] represents a core 2 interrupt request.

Some signals are specified in the form <signal>x where x = 0, 1, 2 or 3 to reference core 0, core 1, core 2, core 3. If a core is not present, the corresponding pin is removed. For example:

- PMUEVENT0[29:0] represents the core 0 PMU event bus.
- PMUEVENT3[29:0] represents the core 3 PMU event bus.

The number of signals changes depending on the configuration. For example, the CHI interface signals are not present when the processor is configured to have an ACE memory interface.
### A.2 Processor configuration signals

The processor samples configuration signals only during cluster reset.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CFGEND[CN:0]</td>
<td>Input</td>
<td>Endianness configuration at reset. It sets the initial value of SCTLR_EL3.EE and SCTR_S.EE: 0 LOW. 1 HIGH.</td>
</tr>
<tr>
<td>CFGTE[CN:0]</td>
<td>Input</td>
<td>Enabling T32 exceptions. It sets the initial value of SCTLR.TE: 0 LOW. 1 HIGH.</td>
</tr>
<tr>
<td>CLUSTERIDAFF1[7:0]</td>
<td>Input</td>
<td>Value read in MPIDR.Aff1. This signal is sampled only during processor reset.</td>
</tr>
<tr>
<td>CLUSTERIDAFF2[7:0]</td>
<td>Input</td>
<td>Value read in MPIDR.Aff2. This signal is sampled only during processor reset.</td>
</tr>
<tr>
<td>CP15SDISABLE2[CN:0]</td>
<td>Input</td>
<td>Disables write access to some Secure CP15 registers.</td>
</tr>
<tr>
<td>CRYPTODISABLE[CN:0]</td>
<td>Input</td>
<td>Disables the Cryptographic Extensions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>If a subset of cores in the processor is configured to include the Cryptographic Extensions, then CRYPTODISABLE[CN:0] is replaced with separate CRYPTOxDISABLE signals, where x indicates the core that each signal relates to.</td>
</tr>
<tr>
<td>VINITHI[CN:0]</td>
<td>Input</td>
<td>Location of the exception vectors at reset. It sets the initial value of SCTLR.V: 0 Exception vectors start at address 0x00000000. 1 Exception vectors start at address 0xFFFF0000.</td>
</tr>
</tbody>
</table>

**Related information**

*B1.97 Multiprocessor Affinity Register* on page B1-309

*B1.105 System Control Register* on page B1-324
A.3 Clock signals

The processor uses a single standard clock signal.

Table A-2 Clock signal

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLKin</td>
<td>Input</td>
<td>Global clock</td>
</tr>
</tbody>
</table>

Related information
A3.1 Clocks on page A3-46
A.4 Reset signals

The processor uses a set of reset signals.

### Table A-3  Reset and reset control signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
</table>
| nCPUPORESET[CN:0] | Input     | Processor powerup reset:  
0  Apply reset to all processor logic.  
1  Do not apply reset to all processor logic.  
Processor logic includes Advanced SIMD and floating-point, debug, ETM trace unit, breakpoint and watchpoint logic. |
| nCORERESET[CN:0]  | Input     | Individual core resets excluding debug and ETM trace unit:  
0  Apply reset to processor logic.  
1  Do not apply reset to processor logic. |
| nL2RESET          | Input     | L2 memory system reset:  
0  Apply reset to the shared L2 memory system controller.  
1  Do not apply reset to the shared L2 memory system controller. |
| L2RSTDISABLE      | Input     | Disable the automatic invalidation of the L2 cache at reset:  
0  Hardware resets the L2 cache.  
1  Hardware does not reset the L2 cache.  
This signal is sampled only during processor reset. |
| WARMRSTREQ[CN:0]  | Output    | Request for a processor warm reset:  
0  Do not apply warm reset.  
1  Apply warm reset. |
| DBG_RSTREQ[CN:0]  | Output    | Warm reset request.                                                                                                                         |
| DBG_L1RSTDISABLE  | Input     | Disable the automatic invalidation of the L1 data cache at processor reset:  
0  Enable automatic invalidation of L1 data cache on reset.  
1  Disable automatic invalidation of L1 data cache on reset.  
This signal is sampled only during processor reset. |

**Related information**

A3.3 Resets on page A3-48
A.5 GIC signals

The processor uses a range of signals for global disable, base address definition, interrupt types, and Distributor messaging.

This interface exists only if the processor is configured to use the GIC CPU interface. However, the first seven signals in the following table are present even when the processor is configured without a GIC CPU interface.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nFIQ[CN:0]</td>
<td>Input</td>
<td>FIQ request. Active-LOW, level sensitive, asynchronous FIQ interrupt request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate FIQ interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate FIQ interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats the nFIQ input as level-sensitive. The nFIQ input must be asserted until the processor acknowledges the interrupt.</td>
</tr>
<tr>
<td>nIRQ[CN:0]</td>
<td>Input</td>
<td>IRQ request input lines. Active-LOW, level sensitive, asynchronous interrupt request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats the nIRQ input as level-sensitive. The nIRQ input must be asserted until the processor acknowledges the interrupt.</td>
</tr>
<tr>
<td>nSEI[CN:0]</td>
<td>Input</td>
<td>System Error Interrupt request. Active-LOW, edge sensitive:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate SEI request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate SEI request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats nSEI as edge-sensitive. The nSEI signal must be sent as a pulse to the processor.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Asserting the nSEI input causes an Asynchronous Data Abort. The DFSR.FS field is set to indicate an Asynchronous External Abort.</td>
</tr>
<tr>
<td>nVFIQ[CN:0]</td>
<td>Input</td>
<td>Virtual FIQ request. Active-LOW, level sensitive, asynchronous FIQ interrupt request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate FIQ interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate FIQ interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats the nVFIQ input as level-sensitive. The nVFIQ input must be asserted until the processor acknowledges the interrupt. If the GIC is enabled by tying GICCDISABLE LOW, nVFIQ must be tied off to HIGH. If the GIC is disabled by tying GICCDISABLE HIGH, nVFIQ can be driven by an external GIC in the SoC.</td>
</tr>
<tr>
<td>nVIRQ[CN:0]</td>
<td>Input</td>
<td>Virtual IRQ request. Active-LOW, level sensitive, asynchronous interrupt request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate interrupt.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats nVIRQ as level-sensitive. nVIRQ must be asserted until the processor acknowledges the interrupt. If the GIC is enabled by tying GICCDISABLE LOW, nVIRQ must be tied off to HIGH. If the GIC is disabled by tying GICCDISABLE HIGH, nVIRQ can be driven by an external GIC in the SoC.</td>
</tr>
</tbody>
</table>
### Table A-4  GIC signals (continued)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nVSEI[CN:0]</td>
<td>Input</td>
<td>Virtual System Error Interrupt request. Active-LOW, edge sensitive:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate virtual SEI request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate virtual SEI request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats nVSEI as edge-sensitive. The nVSEI signal must be sent as a pulse to the processor. Asserting nVSEI causes an asynchronous Data Abort. The DFSR.FS field is set to indicate an Asynchronous External Abort.</td>
</tr>
<tr>
<td>nREI[CN:0]</td>
<td>Input</td>
<td>RAM Error Interrupt request. Active-LOW, edge sensitive:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Activate REI request. Reports an asynchronous RAM error in the system.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Do not activate REI request.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>The processor treats nREI as edge-sensitive. The nREI signal must be sent as a pulse to the processor. Asserting the nREI input causes an asynchronous Data Abort. The DFSR.FS field is set to indicate an Asynchronous parity error on memory access.</td>
</tr>
<tr>
<td>nVCPUMNTIRQ[CN:0]</td>
<td>Output</td>
<td>Virtual CPU interface maintenance interrupt PPI output.</td>
</tr>
<tr>
<td>PERIPHBASE[39:18]</td>
<td>Input</td>
<td>Specifies the base address for the GIC registers. This value is sampled into CBAR at reset.</td>
</tr>
<tr>
<td>GICCDISABLE</td>
<td>Input</td>
<td>Globally disables the GIC CPU interface logic and routes the external signals directly to the processor:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Enable the GIC CPU interface logic.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Disable the GIC CPU interface logic and route the legacy nIRQ, nFIQ, nVIRQ, and nVFIQ signals directly to the processor. Drive this signal HIGH when you are using a legacy interrupt controller such as the GIC-400 which does not support GICv3 or GICv4.</td>
</tr>
</tbody>
</table>

### Table A-5  AXI4 Stream Protocol signals for messages from the Distributor to the GIC CPU Interface

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICDTVVALID</td>
<td>Input</td>
<td>Indicates that the master is driving a valid transfer.</td>
</tr>
<tr>
<td>ICDTREADY</td>
<td>Output</td>
<td>Indicates that the slave can accept a transfer in the current cycle.</td>
</tr>
<tr>
<td>ICDTDATA[15:0]</td>
<td>Input</td>
<td>Primary payload for the data that is passing across the interface.</td>
</tr>
<tr>
<td>ICDTLAST</td>
<td>Input</td>
<td>Indicates the boundary of a packet.</td>
</tr>
<tr>
<td>ICDTDEST[1:0]</td>
<td>Input</td>
<td>Routing information for the data stream.</td>
</tr>
</tbody>
</table>

### Table A-6  AXI4 Stream Protocol signals for messages from the GIC CPU Interface to the Distributor

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCTVALID</td>
<td>Output</td>
<td>Indicates that the master is driving a valid transfer.</td>
</tr>
<tr>
<td>ICCTREADY</td>
<td>Input</td>
<td>Indicates that the slave can accept a transfer in the current cycle.</td>
</tr>
<tr>
<td>ICCTDATA[15:0]</td>
<td>Output</td>
<td>Primary payload for the data that is passing across the interface.</td>
</tr>
</tbody>
</table>
Table A-6  AXI4 Stream Protocol signals for messages from the GIC CPU Interface to the Distributor (continued)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCTLAST</td>
<td>Output</td>
<td>Indicates the boundary of a packet.</td>
</tr>
<tr>
<td>ICCTID[1:0]</td>
<td>Output</td>
<td>Data stream identifier.</td>
</tr>
</tbody>
</table>

Related information

B1.49 Data Fault Status Register on page B1-217
B1.38 Configuration Base Address Register on page B1-194
Chapter A12 GIC CPU Interface on page A12-135
A.6 Generic Timer signals

The processor uses a standard set of signals for the Generic Timer.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nCNTHPIRQ[CN:0]</td>
<td>Output</td>
<td>Hypervisor physical timer event.</td>
</tr>
<tr>
<td>nCNTPNSIRQ[CN:0]</td>
<td>Output</td>
<td>Non-secure physical timer event.</td>
</tr>
<tr>
<td>nCNTPSIRQ[CN:0]</td>
<td>Output</td>
<td>Secure physical timer event.</td>
</tr>
<tr>
<td>nCNTVIRQ[CN:0]</td>
<td>Output</td>
<td>Virtual physical timer event.</td>
</tr>
<tr>
<td>CNTCLKEN</td>
<td>Input</td>
<td>Counter clock enable.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This clock enable must be asserted one cycle before the CNTVALUEB bus.</td>
</tr>
<tr>
<td>CNTVALUEB[63:0]</td>
<td>Input</td>
<td>Global system counter value in binary format.</td>
</tr>
</tbody>
</table>

Related information

A2.4 About the Generic Timer on page A2-43
### A.7 Power management signals

The processor has retention and non-retention signals for power management.

#### Table A-8 Non-Retention power management signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLREXMONREQ</td>
<td>Input</td>
<td>Clearing of the external global exclusive monitor request. When this signal is asserted, it acts as a WFE wake-up event to all the cores in the processor device.</td>
</tr>
<tr>
<td>CLREXMONACK</td>
<td>Output</td>
<td>Clearing of the external global exclusive monitor acknowledge.</td>
</tr>
<tr>
<td>EVENTI</td>
<td>Input</td>
<td>Event input for processor wake-up from WFE state.</td>
</tr>
<tr>
<td>EVENTO</td>
<td>Output</td>
<td>Event output. Active when a SEV instruction is executed.</td>
</tr>
<tr>
<td>STANDBYWFI[CN:0]</td>
<td>Output</td>
<td>Indicates whether a core is in WFI low-power state:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Core not in WFI low-power state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Core in WFI low-power state. This is the reset condition.</td>
</tr>
<tr>
<td>STANDBYWFE[CN:0]</td>
<td>Output</td>
<td>Indicates whether a core is in WFE low-power state:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Core not in WFE low-power state.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Core in WFE low-power state.</td>
</tr>
<tr>
<td>STANDBYWFIL2</td>
<td>Output</td>
<td>Indicates whether the L2 memory system is in WFI low-power state. This signal is active when the following conditions are met:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• All cores are in WFI low-power state, held in reset, or nL2RESET is asserted LOW.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In an ACE configuration, ACINACTM is asserted HIGH.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In a CHI configuration, SINACT is asserted HIGH.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• If ACP has been configured, AINACTS is asserted HIGH.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• L2 memory system is idle.</td>
</tr>
<tr>
<td>L2FLUSHREQ</td>
<td>Input</td>
<td>L2 hardware flush request.</td>
</tr>
<tr>
<td>L2FLUSHDONE</td>
<td>Output</td>
<td>L2 hardware flush complete.</td>
</tr>
<tr>
<td>SMPEN[CN:0]</td>
<td>Output</td>
<td>Indicates whether a core is taking part in coherency.</td>
</tr>
<tr>
<td>DBGNOPWRDWN[CN:0]</td>
<td>Output</td>
<td>Request not to power down the core:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Do not request that the core stays powered-up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Request that the core stays powered-up.</td>
</tr>
<tr>
<td>DBGPWRUPREQ[CN:0]</td>
<td>Output</td>
<td>Core power-up request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Do not request that the core powered up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Request that the core is powered up.</td>
</tr>
<tr>
<td>DBGPWRDUP[CN:0]</td>
<td>Input</td>
<td>Core powered up</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Core is powered down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Core is powered up.</td>
</tr>
</tbody>
</table>
## Table A-9 Retention power management signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPUQACTIVE[CN:0]</td>
<td>Output</td>
<td>Indicates whether the referenced core is active</td>
</tr>
<tr>
<td>CPUQREQn[CN:0]</td>
<td>Input</td>
<td>Indicates that the power controller is ready to enter or exit retention for the referenced core</td>
</tr>
<tr>
<td>CPUQDENY[CN:0]</td>
<td>Output</td>
<td>Indicates that the referenced core denies the power controller retention request</td>
</tr>
<tr>
<td>CPUQACCEPTn[CN:0]</td>
<td>Output</td>
<td>Indicates that the referenced core accepts the power controller retention request</td>
</tr>
<tr>
<td>NEONQACTIVE[CN:0]</td>
<td>Output</td>
<td>Indicates whether the referenced Advanced SIMD and Floating-point block is active</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note</strong> If a subset of cores in the processor is configured with Advanced SIMD and floating-point functionality, then NEONQACTIVE[CN:0] is replaced with separate NEONxQACTIVE signals, where x indicates the core that each signal relates to.</td>
</tr>
<tr>
<td>NEONQREQn[CN:0]</td>
<td>Input</td>
<td>Indicates that the power controller is ready to enter or exit retention for the referenced Advanced SIMD and Floating-point block</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note</strong> If a subset of cores in the processor is configured with Advanced SIMD and floating-point functionality, then NEONQREQn[CN:0] is replaced with separate NEONxQREQn signals, where x indicates the core that each signal relates to.</td>
</tr>
<tr>
<td>NEONQDENY[CN:0]</td>
<td>Output</td>
<td>Indicates that the referenced Advanced SIMD and Floating-point block denies the power controller retention request</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note</strong> If a subset of cores in the processor is configured with Advanced SIMD and floating-point functionality, then NEONQDENY[CN:0] is replaced with separate NEONxQDENY signals, where x indicates the core that each signal relates to.</td>
</tr>
<tr>
<td>NEONQACCEPTn[CN:0]</td>
<td>Output</td>
<td>Indicates that the referenced Advanced SIMD and Floating-point block accepts the power controller retention request</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note</strong> If a subset of cores in the processor is configured with Advanced SIMD and floating-point functionality, then NEONQACCEPTn[CN:0] is replaced with separate NEONxQACCEPTn signals, where x indicates the core that each signal relates to.</td>
</tr>
<tr>
<td>L2QACTIVE</td>
<td>Output</td>
<td>Indicates whether the L2 data RAMs are active</td>
</tr>
<tr>
<td>L2QREQn</td>
<td>Input</td>
<td>Indicates that the power controller is ready to enter or exit retention for the L2 data RAMs</td>
</tr>
<tr>
<td>L2QDENY</td>
<td>Output</td>
<td>Indicates that the L2 data RAMs deny the power controller retention request</td>
</tr>
<tr>
<td>L2QACCEPTn</td>
<td>Output</td>
<td>Indicates that the L2 data RAMs accept the power controller retention request</td>
</tr>
</tbody>
</table>

**Related information**

*Chapter A4 Power Management* on page A4-53
A.8 L2 error signals

The processor has signals for errors in the Level 2 cache.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nEXERRIRQ</td>
<td>Output</td>
<td>Error indicator for memory transactions with a write response error condition.</td>
</tr>
<tr>
<td>nINTERRIRQ</td>
<td>Output</td>
<td>Error indicator for L2 RAM double-bit ECC error.</td>
</tr>
</tbody>
</table>

Related information
A7.5 Handling of external aborts on page A7-97
A.9 ACP interface signals

The AXI protocol supports clock, configuration, and data handling signals if the processor implements the ACP slave interface to an external master to make coherent request to the shared L2 cache of the cluster.

This interface exists only if the processor is configured to have the ACP interface.

All ACP channels must be balanced with respect to CLKIN and timed relative to ACLKENS.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACLKENS</td>
<td>Input</td>
<td>AXI slave bus clock enable.</td>
</tr>
<tr>
<td>AINACTS</td>
<td>Input</td>
<td>ACP master is inactive and is not participating in coherency. There must be no outstanding transactions when the master asserts this signal, and while it is asserted the master must not send any new transactions: 0 ACP Master is active. 1 ACP Master is inactive. This signal must be asserted before the processor enters the low-power L2 WFI state.</td>
</tr>
</tbody>
</table>

Table A-11 ACP clock and Configuration signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWREADYS</td>
<td>Output</td>
<td>Write address ready</td>
</tr>
<tr>
<td>AWVALIDS</td>
<td>Input</td>
<td>Write address valid</td>
</tr>
<tr>
<td>AWIDS[4:0]</td>
<td>Input</td>
<td>Write address ID</td>
</tr>
<tr>
<td>AWADDRS[39:0]</td>
<td>Input</td>
<td>Write address</td>
</tr>
<tr>
<td>AWLENS[7:0]</td>
<td>Input</td>
<td>Write burst length</td>
</tr>
<tr>
<td>AWCACHE[3:0]</td>
<td>Input</td>
<td>Write cache type</td>
</tr>
<tr>
<td>AWUSERS[1:0]</td>
<td>Input</td>
<td>Write attributes: [0] Inner Shareable. [1] Outer Shareable.</td>
</tr>
<tr>
<td>AWPROTS[2:0]</td>
<td>Input</td>
<td>Write protection type</td>
</tr>
</tbody>
</table>

Table A-12 ACP write address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WREADYS</td>
<td>Output</td>
<td>Write data ready</td>
</tr>
<tr>
<td>WVALIDS</td>
<td>Input</td>
<td>Write data valid</td>
</tr>
<tr>
<td>WDATAS[127:0]</td>
<td>Input</td>
<td>Write data</td>
</tr>
<tr>
<td>WSTRBS[15:0]</td>
<td>Input</td>
<td>Write byte-lane strobes</td>
</tr>
<tr>
<td>WLASTS</td>
<td>Input</td>
<td>Write data last transfer indication</td>
</tr>
</tbody>
</table>

Table A-13 ACP write data channel signals
### Table A-14  ACP write response channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BREADYS</td>
<td>Input</td>
<td>Write response ready</td>
</tr>
<tr>
<td>BVALIDS</td>
<td>Output</td>
<td>Write response valid</td>
</tr>
<tr>
<td>BIDS[4:0]</td>
<td>Output</td>
<td>Write response ID</td>
</tr>
<tr>
<td>BRESPS[1:0]</td>
<td>Output</td>
<td>Write response</td>
</tr>
</tbody>
</table>

### Table A-15  ACP read address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARREADYS</td>
<td>Output</td>
<td>Read address ready</td>
</tr>
<tr>
<td>ARVALIDS</td>
<td>Input</td>
<td>Read address valid</td>
</tr>
<tr>
<td>ARIDS[4:0]</td>
<td>Input</td>
<td>Read address ID</td>
</tr>
<tr>
<td>ARADDRS[39:0]</td>
<td>Input</td>
<td>Read address</td>
</tr>
<tr>
<td>ARLENS[7:0]</td>
<td>Input</td>
<td>Read burst length</td>
</tr>
<tr>
<td>ARCACHES[3:0]</td>
<td>Input</td>
<td>Read cache type</td>
</tr>
<tr>
<td>ARUSERS[1:0]</td>
<td>Input</td>
<td>Read attributes:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[0] Inner Shareable.</td>
</tr>
<tr>
<td>ARPROTS[2:0]</td>
<td>Input</td>
<td>Read protection type</td>
</tr>
</tbody>
</table>

### Table A-16  ACP read data channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RREADYS</td>
<td>Input</td>
<td>Read data ready</td>
</tr>
<tr>
<td>RVALIDS</td>
<td>Output</td>
<td>Read data valid</td>
</tr>
<tr>
<td>RIDS[4:0]</td>
<td>Output</td>
<td>Read data ID</td>
</tr>
<tr>
<td>RDATAS[127:0]</td>
<td>Output</td>
<td>Read data</td>
</tr>
<tr>
<td>RRESPS[1:0]</td>
<td>Output</td>
<td>Read response</td>
</tr>
<tr>
<td>RLASTS</td>
<td>Output</td>
<td>Read data last transfer indication</td>
</tr>
</tbody>
</table>
A.10 Broadcast signals for the memory interface

The processor has broadcast signals for the memory interface. These signals are only sampled at processor reset.

The signals in the following table only exist if the processor is configured to have an ACE or CHI memory interface.

Table A-17 Broadcast signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BROADCASTCACHEMAINT</td>
<td>Input</td>
<td>Enable broadcasting of cache maintenance operations to downstream caches:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ Cache maintenance operations are not broadcast to downstream caches.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Cache maintenance operations are broadcast to downstream caches.</td>
</tr>
<tr>
<td>BROADCASTINNER</td>
<td>Input</td>
<td>Enable broadcasting of Inner Shareable transactions:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ Inner Shareable transactions are not broadcast externally.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Inner Shareable transactions are broadcast externally.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>If BROADCASTINNER is tied HIGH, you must also tie BROADCASTOUTER HIGH.</td>
</tr>
<tr>
<td>BROADCASTOUTER</td>
<td>Input</td>
<td>Enable broadcasting of outer shareable transactions:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>θ Outer Shareable transactions are not broadcast externally.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Outer Shareable transactions are broadcast externally.</td>
</tr>
</tbody>
</table>
A.11 AXI interface signals

The AXI protocol supports clock, configuration, and data handling signals when the processor uses this protocol for the master memory interface.

This interface exists only if the processor is configured to have the AXI interface.

All AXI channels must be balanced with respect to CLkin and timed relative to ACLKNM.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACLKENM</td>
<td>Input</td>
<td>AXI Master bus clock enable. See A3.1 Clocks on page A3-46 for more information.</td>
</tr>
<tr>
<td>RDMEMATTR[7:0]</td>
<td>Output</td>
<td>Read request memory attributes.</td>
</tr>
<tr>
<td>WRMEMATTR[7:0]</td>
<td>Output</td>
<td>Write request memory attributes.</td>
</tr>
</tbody>
</table>

Table A-19 AXI write address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWADDRM[39:0]</td>
<td>Output</td>
<td>Write address.</td>
</tr>
<tr>
<td>AWBURSTM[1:0]</td>
<td>Output</td>
<td>Write burst type.</td>
</tr>
<tr>
<td>AWCACHEM[3:0]</td>
<td>Output</td>
<td>Write cache type.</td>
</tr>
<tr>
<td>AWIDM[4:0]</td>
<td>Output</td>
<td>Write address ID.</td>
</tr>
<tr>
<td>AWLENM[7:0]</td>
<td>Output</td>
<td>Write burst length.</td>
</tr>
<tr>
<td>AWLOCKM</td>
<td>Output</td>
<td>Write lock type.</td>
</tr>
<tr>
<td>AWPROTM[2:0]</td>
<td>Output</td>
<td>Write protection type.</td>
</tr>
<tr>
<td>AWREADYM</td>
<td>Input</td>
<td>Write address ready.</td>
</tr>
<tr>
<td>AWSIZEM[2:0]</td>
<td>Output</td>
<td>Write burst size.</td>
</tr>
<tr>
<td>AWVALIDM</td>
<td>Output</td>
<td>Write address valid.</td>
</tr>
</tbody>
</table>

Table A-20 AXI write data channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDATAM[127:0]</td>
<td>Output</td>
<td>Write data</td>
</tr>
<tr>
<td>WIDM[4:0]</td>
<td>Output</td>
<td>Write data ID</td>
</tr>
<tr>
<td>WLASTM</td>
<td>Output</td>
<td>Write data last transfer indication</td>
</tr>
<tr>
<td>WREADYM</td>
<td>Input</td>
<td>Write data ready</td>
</tr>
<tr>
<td>WSTRBM[15:0]</td>
<td>Output</td>
<td>Write byte-lane strobes</td>
</tr>
<tr>
<td>WVALIDM</td>
<td>Output</td>
<td>Write data valid</td>
</tr>
</tbody>
</table>
Table A-21  AXI write data response channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIDM[4:0]</td>
<td>Input</td>
<td>Write response ID</td>
</tr>
<tr>
<td>BREADYM</td>
<td>Output</td>
<td>Write response ready</td>
</tr>
<tr>
<td>BRESPM[1:0]</td>
<td>Input</td>
<td>Write response</td>
</tr>
<tr>
<td>BVALIDM</td>
<td>Input</td>
<td>Write response valid</td>
</tr>
</tbody>
</table>

Table A-22  AXI read address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARADDRM[39:0]</td>
<td>Output</td>
<td>Read address.</td>
</tr>
<tr>
<td>ARBURSTM[1:0]</td>
<td>Output</td>
<td>Read burst type.</td>
</tr>
<tr>
<td>ARCACHEM[3:0]</td>
<td>Output</td>
<td>Read cache type</td>
</tr>
<tr>
<td>ARIDM[5:0]</td>
<td>Output</td>
<td>Read address ID</td>
</tr>
<tr>
<td>ARLENM[7:0]</td>
<td>Output</td>
<td>Read burst length</td>
</tr>
<tr>
<td>ARLOCKM</td>
<td>Output</td>
<td>Read lock type</td>
</tr>
<tr>
<td>ARPROTM[2:0]</td>
<td>Output</td>
<td>Read protection type</td>
</tr>
<tr>
<td>ARREADYM</td>
<td>Input</td>
<td>Read address ready</td>
</tr>
<tr>
<td>ARSIZEM[2:0]</td>
<td>Output</td>
<td>Read burst size</td>
</tr>
<tr>
<td>ARVALIDM</td>
<td>Output</td>
<td>Read address valid</td>
</tr>
</tbody>
</table>

Table A-23  AXI read data channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDATAM[127:0]</td>
<td>Input</td>
<td>Read data</td>
</tr>
<tr>
<td>RIDM[5:0]</td>
<td>Input</td>
<td>Read data ID</td>
</tr>
<tr>
<td>RLASTM</td>
<td>Input</td>
<td>Read data last transfer indication</td>
</tr>
<tr>
<td>RREADYM</td>
<td>Output</td>
<td>Read data ready</td>
</tr>
<tr>
<td>RRESPM[1:0]</td>
<td>Input</td>
<td>Read data response</td>
</tr>
<tr>
<td>RVALIDM</td>
<td>Input</td>
<td>Read data valid</td>
</tr>
</tbody>
</table>

Related information

Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, and ACE and ACE-Lite
A.12 ACE interface signals

The ACE protocol supports clock, configuration, and data handling signals when the processor uses this protocol for the master memory interface.

This interface exists only if the Cortex-A32 processor is configured to have the ACE interface.

All ACE channels must be balanced with respect to CLKin and timed relative to ACLKENM.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACLKENM</td>
<td>Input</td>
<td>ACE Master bus clock enable.</td>
</tr>
<tr>
<td>ACINACTM</td>
<td>Input</td>
<td>Snoop interface is inactive and not participating in coherency:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Snoop interface is active.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Snoop interface is inactive.</td>
</tr>
<tr>
<td>RDMEMATTR[7:0]</td>
<td>Output</td>
<td>Read request memory attributes.</td>
</tr>
<tr>
<td>WRMEMATTR[7:0]</td>
<td>Output</td>
<td>Write request memory attributes.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AWADDRM[43:0]</td>
<td>Output</td>
<td>Write address.</td>
</tr>
<tr>
<td>AWBARM[1:0]</td>
<td>Output</td>
<td>Write barrier type.</td>
</tr>
<tr>
<td>AWBURSTM[1:0]</td>
<td>Output</td>
<td>Write burst type.</td>
</tr>
<tr>
<td>AWCACHEM[3:0]</td>
<td>Output</td>
<td>Write cache type.</td>
</tr>
<tr>
<td>AWDOMAINM[1:0]</td>
<td>Output</td>
<td>Write shareability domain type.</td>
</tr>
<tr>
<td>AWIDM[4:0]</td>
<td>Output</td>
<td>Write address ID.</td>
</tr>
<tr>
<td>AWLENM[7:0]</td>
<td>Output</td>
<td>Write burst length.</td>
</tr>
<tr>
<td>AWLOCKM</td>
<td>Output</td>
<td>Write lock type.</td>
</tr>
<tr>
<td>AWPROTM[2:0]</td>
<td>Output</td>
<td>Write protection type.</td>
</tr>
<tr>
<td>AWREADYM</td>
<td>Input</td>
<td>Write address ready.</td>
</tr>
<tr>
<td>AWSIZEM[2:0]</td>
<td>Output</td>
<td>Write burst size.</td>
</tr>
<tr>
<td>AWSNOOPM[2:0]</td>
<td>Output</td>
<td>Write snoop request type.</td>
</tr>
<tr>
<td>AWUNIQUEM</td>
<td>Output</td>
<td>For WriteBack, WriteClean and WriteEvict transactions.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Indicates that the write is:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0 Shared.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1 Unique.</td>
</tr>
<tr>
<td>AWVALIDM</td>
<td>Output</td>
<td>Write address valid.</td>
</tr>
</tbody>
</table>
### Table A-26  ACE write data channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDATAM[127:0]</td>
<td>Output</td>
<td>Write data</td>
</tr>
<tr>
<td>WIDM[4:0]</td>
<td>Output</td>
<td>Write data ID</td>
</tr>
<tr>
<td>WLASTM</td>
<td>Output</td>
<td>Write data last transfer indication</td>
</tr>
<tr>
<td>WREADYM</td>
<td>Input</td>
<td>Write data ready</td>
</tr>
<tr>
<td>WSTRBM[15:0]</td>
<td>Output</td>
<td>Write byte-lane strobes</td>
</tr>
<tr>
<td>WVALIDM</td>
<td>Output</td>
<td>Write data valid</td>
</tr>
</tbody>
</table>

### Table A-27  ACE write data response channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BIDM[4:0]</td>
<td>Input</td>
<td>Write response ID</td>
</tr>
<tr>
<td>BREADYM</td>
<td>Output</td>
<td>Write response ready</td>
</tr>
<tr>
<td>BRESPM[1:0]</td>
<td>Input</td>
<td>Write response</td>
</tr>
<tr>
<td>BVALIDM</td>
<td>Input</td>
<td>Write response valid</td>
</tr>
</tbody>
</table>

### Table A-28  ACE read address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARADDRM[43:0]</td>
<td>Output</td>
<td>Read address. The top 4 bits communicate only the ACE virtual address for DVM messages. The top 4 bits are Read-as-Zero if a DVM message is not being broadcast.</td>
</tr>
<tr>
<td>ARBARM[1:0]</td>
<td>Output</td>
<td>Read barrier type.</td>
</tr>
<tr>
<td>ARBURSTM[1:0]</td>
<td>Output</td>
<td>Read burst type.</td>
</tr>
<tr>
<td>ARCACHEM[3:0]</td>
<td>Output</td>
<td>Read cache type.</td>
</tr>
<tr>
<td>ARDOMAINM[1:0]</td>
<td>Output</td>
<td>Read shareability domain type.</td>
</tr>
<tr>
<td>ARIDM[5:0]</td>
<td>Output</td>
<td>Read address ID.</td>
</tr>
<tr>
<td>ARLENM[7:0]</td>
<td>Output</td>
<td>Read burst length.</td>
</tr>
<tr>
<td>ARLOCKM</td>
<td>Output</td>
<td>Read lock type.</td>
</tr>
<tr>
<td>ARPROTM[2:0]</td>
<td>Output</td>
<td>Read protection type.</td>
</tr>
<tr>
<td>ARREAYDM</td>
<td>Input</td>
<td>Read address ready.</td>
</tr>
<tr>
<td>ARSIZEM[2:0]</td>
<td>Output</td>
<td>Read burst size.</td>
</tr>
<tr>
<td>ARSNOOPM[3:0]</td>
<td>Output</td>
<td>Read snoop request type.</td>
</tr>
<tr>
<td>ARVALIDM</td>
<td>Output</td>
<td>Read address valid.</td>
</tr>
</tbody>
</table>
Table A-29  ACE read data channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDATAM[127:0]</td>
<td>Input</td>
<td>Read data</td>
</tr>
<tr>
<td>RIDM[5:0]</td>
<td>Input</td>
<td>Read data ID</td>
</tr>
<tr>
<td>RLASTM</td>
<td>Input</td>
<td>Read data last transfer indication</td>
</tr>
<tr>
<td>RREADYM</td>
<td>Output</td>
<td>Read data ready</td>
</tr>
<tr>
<td>RRESPM[3:0]</td>
<td>Input</td>
<td>Read data response</td>
</tr>
<tr>
<td>RVALIDM</td>
<td>Input</td>
<td>Read data valid</td>
</tr>
</tbody>
</table>

Table A-30  ACE coherency address channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACADDRM[43:0]</td>
<td>Input</td>
<td>Snoop address. The top 4 bits communicate only the ACE virtual address for DVM messages.</td>
</tr>
<tr>
<td>ACPROMT[2:0]</td>
<td>Input</td>
<td>Snoop protection type.</td>
</tr>
<tr>
<td>ACREADY</td>
<td>Output</td>
<td>Master ready to accept snoop address.</td>
</tr>
<tr>
<td>ACSNOOPM[3:0]</td>
<td>Input</td>
<td>Snoop request type.</td>
</tr>
<tr>
<td>AVALIDM</td>
<td>Input</td>
<td>Snoop address valid.</td>
</tr>
</tbody>
</table>

Table A-31  ACE coherency response channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CRREADYM</td>
<td>Input</td>
<td>Slave ready to accept snoop response</td>
</tr>
<tr>
<td>CRVALIDM</td>
<td>Output</td>
<td>Snoop response</td>
</tr>
<tr>
<td>CRRESPM[4:0]</td>
<td>Output</td>
<td>Snoop response valid</td>
</tr>
</tbody>
</table>

Table A-32  ACE coherency data channel handshake signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CDDATAM[127:0]</td>
<td>Output</td>
<td>Snoop data</td>
</tr>
<tr>
<td>CDLASTM</td>
<td>Output</td>
<td>Snoop data last transform</td>
</tr>
<tr>
<td>CDREADYM</td>
<td>Input</td>
<td>Slave ready to accept snoop data</td>
</tr>
<tr>
<td>CVALIDM</td>
<td>Output</td>
<td>Snoop data valid</td>
</tr>
</tbody>
</table>

Table A-33  ACE read and write acknowledge signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RACKM</td>
<td>Output</td>
<td>Read acknowledge</td>
</tr>
<tr>
<td>WACKM</td>
<td>Output</td>
<td>Write acknowledge</td>
</tr>
</tbody>
</table>
Related information

A3.1 Clocks on page A3–46

Arm® AMBA® AXI and ACE Protocol Specification AXI3, AXI4, and AXI4-Lite, and ACE and ACE-Lite
A.13 CHI interface signals

The CHI protocol supports clock, configuration, data handling, and address map signals when the processor uses this protocol for the master memory interface.

This interface exists only if the processor is configured to have the CHI interface.

Table A-34 CHI clock and configuration signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCLKEN</td>
<td>Input</td>
<td>CHI interface bus clock enable</td>
</tr>
<tr>
<td>SINACT</td>
<td>Input</td>
<td>CHI snoop active</td>
</tr>
<tr>
<td>NODEID[6:0]</td>
<td>Input</td>
<td>Cortex-A32 CHI Node Identifier</td>
</tr>
<tr>
<td>RXSACTIVE</td>
<td>Input</td>
<td>Receive pending activity indicator</td>
</tr>
<tr>
<td>TXSACTIVE</td>
<td>Output</td>
<td>Transmit pending activity indicator</td>
</tr>
<tr>
<td>RXLINKACTIVEREQ</td>
<td>Input</td>
<td>Receive link active request</td>
</tr>
<tr>
<td>RXLINKACTIVEACK</td>
<td>Output</td>
<td>Receive link active acknowledge</td>
</tr>
<tr>
<td>TXLINKACTIVEREQ</td>
<td>Output</td>
<td>Transmit link active request</td>
</tr>
<tr>
<td>TXLINKACTIVEACK</td>
<td>Input</td>
<td>Transmit link active acknowledge</td>
</tr>
<tr>
<td>REQMEMATTR[7:0]</td>
<td>Output</td>
<td>Request memory attributes</td>
</tr>
</tbody>
</table>

Table A-35 CHI transmit request virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXREQFLITPEND</td>
<td>Output</td>
<td>Transmit request flit pending</td>
</tr>
<tr>
<td>TXREQFLITV</td>
<td>Output</td>
<td>Transmit request flit valid</td>
</tr>
<tr>
<td>TXREQFLIT[99:0]</td>
<td>Output</td>
<td>Transmit request flit payload</td>
</tr>
<tr>
<td>TXREQLCRDV</td>
<td>Input</td>
<td>Transmit request link-layer credit valid</td>
</tr>
</tbody>
</table>

Table A-36 CHI transmit response virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXRSPFLITPEND</td>
<td>Output</td>
<td>Transmit response flit pending</td>
</tr>
<tr>
<td>TXRSPFLITV</td>
<td>Output</td>
<td>Transmit response flit valid</td>
</tr>
<tr>
<td>TXRSPFLIT[44:0]</td>
<td>Output</td>
<td>Transmit response flit</td>
</tr>
<tr>
<td>TXRSPLCRDV</td>
<td>Input</td>
<td>Transmit response link-layer credit valid</td>
</tr>
</tbody>
</table>

Table A-37 CHI transmit data virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TXDATFLITPEND</td>
<td>Output</td>
<td>Transmit data flit pending</td>
</tr>
<tr>
<td>TXDATFLITV</td>
<td>Output</td>
<td>Transmit data flit valid</td>
</tr>
<tr>
<td>TXDATFLIT[193:0]</td>
<td>Output</td>
<td>Transmit data flit</td>
</tr>
<tr>
<td>TXDATLCRDV</td>
<td>Input</td>
<td>Transmit data link-layer credit valid</td>
</tr>
</tbody>
</table>
### Table A-38  CHI receive snoop virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXSNPFLITPEND</td>
<td>Input</td>
<td>Receive snoop flit pending</td>
</tr>
<tr>
<td>RXSNPFLITV</td>
<td>Input</td>
<td>Receive snoop flit valid</td>
</tr>
<tr>
<td>RXSNPFLIT[64:0]</td>
<td>Input</td>
<td>Receive snoop flit</td>
</tr>
<tr>
<td>RXSNPLCRDV</td>
<td>Output</td>
<td>Receive snoop link-layer credit valid</td>
</tr>
</tbody>
</table>

### Table A-39  CHI receive response virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXRSPFLITPEND</td>
<td>Input</td>
<td>Receive response flit pending</td>
</tr>
<tr>
<td>RXRSPFLITV</td>
<td>Input</td>
<td>Receive response flit valid</td>
</tr>
<tr>
<td>RXRSPFLIT[44:0]</td>
<td>Input</td>
<td>Receive response flit</td>
</tr>
<tr>
<td>RXRSPPLCRDV</td>
<td>Output</td>
<td>Receive response link-layer credit valid</td>
</tr>
</tbody>
</table>

### Table A-40  CHI receive Data virtual channel signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RXDATFLITPEND</td>
<td>Input</td>
<td>Receive data flit pending</td>
</tr>
<tr>
<td>RXDATFLITV</td>
<td>Input</td>
<td>Receive data flit valid</td>
</tr>
<tr>
<td>RXDATFLIT[193:0]</td>
<td>Input</td>
<td>Receive data flit</td>
</tr>
<tr>
<td>RXDATLCRDV</td>
<td>Output</td>
<td>Receive data link-layer credit valid</td>
</tr>
</tbody>
</table>

### Table A-41  CHI system address map signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SAMADDRMAP0[1:0]</td>
<td>Input</td>
<td>Region mapping, 0 – 512MB</td>
</tr>
<tr>
<td>SAMADDRMAP1[1:0]</td>
<td>Input</td>
<td>Region mapping, 512MB – 1GB</td>
</tr>
<tr>
<td>SAMADDRMAP2[1:0]</td>
<td>Input</td>
<td>Region mapping, 1GB – 1.5GB</td>
</tr>
<tr>
<td>SAMADDRMAP3[1:0]</td>
<td>Input</td>
<td>Region mapping, 1.5GB – 2GB</td>
</tr>
<tr>
<td>SAMADDRMAP4[1:0]</td>
<td>Input</td>
<td>Region mapping, 2GB – 2.5GB</td>
</tr>
<tr>
<td>SAMADDRMAP5[1:0]</td>
<td>Input</td>
<td>Region mapping, 2.5GB – 3GB</td>
</tr>
<tr>
<td>SAMADDRMAP6[1:0]</td>
<td>Input</td>
<td>Region mapping, 3GB – 3.5GB</td>
</tr>
<tr>
<td>SAMADDRMAP7[1:0]</td>
<td>Input</td>
<td>Region mapping, 3.5GB – 4GB</td>
</tr>
<tr>
<td>SAMADDRMAP8[1:0]</td>
<td>Input</td>
<td>Region mapping, 4GB – 8GB</td>
</tr>
<tr>
<td>SAMADDRMAP9[1:0]</td>
<td>Input</td>
<td>Region mapping, 8GB – 16GB</td>
</tr>
<tr>
<td>SAMADDRMAP10[1:0]</td>
<td>Input</td>
<td>Region mapping, 16GB – 32GB</td>
</tr>
<tr>
<td>SAMADDRMAP11[1:0]</td>
<td>Input</td>
<td>Region mapping, 32GB – 64GB</td>
</tr>
<tr>
<td>SAMADDRMAP12[1:0]</td>
<td>Input</td>
<td>Region mapping, 64GB – 128GB</td>
</tr>
<tr>
<td>SAMADDRMAP13[1:0]</td>
<td>Input</td>
<td>Region mapping, 128GB – 256GB</td>
</tr>
<tr>
<td>Signal</td>
<td>Direction</td>
<td>Description</td>
</tr>
<tr>
<td>------------------------</td>
<td>-----------</td>
<td>-----------------------------------------------------</td>
</tr>
<tr>
<td>SAMADDRMAP14[1:0]</td>
<td>Input</td>
<td>Region mapping, 256GB – 512GB</td>
</tr>
<tr>
<td>SAMADDRMAP15[1:0]</td>
<td>Input</td>
<td>Region mapping, 512GB – 1TB</td>
</tr>
<tr>
<td>SAMMNBASE[39:24]</td>
<td>Input</td>
<td>MN base address</td>
</tr>
<tr>
<td></td>
<td></td>
<td>SAMMNBASE must reside in a SAMADDRMAPx[1:0] that corresponds to the HN-I.</td>
</tr>
<tr>
<td>SAMMNNODEID[6:0]</td>
<td>Input</td>
<td>MN node ID</td>
</tr>
<tr>
<td>SAMHNI0NODEID[6:0]</td>
<td>Input</td>
<td>HN-I 0 node ID</td>
</tr>
<tr>
<td>SAMHNI1NODEID[6:0]</td>
<td>Input</td>
<td>HN-I 1 node ID</td>
</tr>
<tr>
<td>SAMHNF0NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 0 node ID</td>
</tr>
<tr>
<td>SAMHNF1NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 1 node ID</td>
</tr>
<tr>
<td>SAMHNF2NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 2 node ID</td>
</tr>
<tr>
<td>SAMHNF3NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 3 node ID</td>
</tr>
<tr>
<td>SAMHNF4NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 4 node ID</td>
</tr>
<tr>
<td>SAMHNF5NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 5 node ID</td>
</tr>
<tr>
<td>SAMHNF6NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 6 node ID</td>
</tr>
<tr>
<td>SAMHNF7NODEID[6:0]</td>
<td>Input</td>
<td>HN-F 7 node ID</td>
</tr>
<tr>
<td>SAMHNFMODE[2:0]</td>
<td>Input</td>
<td>HN-F interleaving module</td>
</tr>
</tbody>
</table>
A.14 Debug signals

The processor has the following debug signals.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
</table>
| DBGROMADDR[39:12] | Input     | Debug ROM base address.  
  Specifies bits[39:12] of the ROM table physical address.  
  If the address cannot be determined, tie this signal LOW.  
  This signal is sampled only during processor reset. |
| DBGROMADDRV    | Input     | Debug ROM base address valid.  
  If the debug ROM address cannot be determined, tie this signal LOW.  
  This signal is sampled only during processor reset. |
| DBGACK[CN:0]   | Output    | Debug acknowledge:  
  0 External debug request not acknowledged.  
  1 External debug request acknowledged. |
| nCOMMIRQ[CN:0] | Output    | Communications channel receive or transmit interrupt request  
  0 Request interrupt.  
  1 No interrupt request. |
| COMMRX[CN:0]   | Output    | Communications channel receive. Receive portion of Data Transfer Register full flag:  
  0 Empty.  
  1 Full. |
| COMMTX[CN:0]   | Output    | Communication transmit channel. Transmit portion of Data Transfer Register empty flag:  
  0 Full.  
  1 Empty. |
| EDBGRQ[CN:0]   | Input     | External debug request:  
  0 No external debug request.  
  1 External debug request.  
  The processor treats the EDBGRQ input as level-sensitive. The EDBGRQ input must be asserted until the processor asserts DBGACK. |
| DBGEN[CN:0]    | Input     | Invasive debug enable:  
  0 Not enabled.  
  1 Enabled. |
| NIDEN[CN:0]    | Input     | Non-invasive debug enable:  
  0 Not enabled.  
  1 Enabled. |
### Table A-42  Debug signals (continued)

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPIDEN[CN:0]</td>
<td>Input</td>
<td>Secure privileged invasive debug enable:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Not enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Enabled.</td>
</tr>
<tr>
<td>SPNIDEN[CN:0]</td>
<td>Input</td>
<td>Secure privileged non-invasive debug enable:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Not enabled.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Enabled.</td>
</tr>
<tr>
<td>DBGRSTREQ[CN:0]</td>
<td>Output</td>
<td>Warm reset request.</td>
</tr>
<tr>
<td>DBGNOPWRDWN[CN:0]</td>
<td>Output</td>
<td>Request not to power down the core:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Do not request that the core stays powered up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Request that the core stays powered up.</td>
</tr>
<tr>
<td>DBGPWRUPREQ[CN:0]</td>
<td>Output</td>
<td>Core power-up request:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Do not request that the core is powered up.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Request that the core is powered up.</td>
</tr>
<tr>
<td>DBGPWRDUP[CN:0]</td>
<td>Input</td>
<td>Core powered up:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Core is powered down.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Core is powered up.</td>
</tr>
<tr>
<td>DBGL1RSTD disable</td>
<td>Input</td>
<td>Disable the automatic invalidation of the L1 data cache at processor reset:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0  Enable automatic invalidation of L1 data cache on reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1  Disable automatic invalidation of L1 data cache on reset.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This signal is sampled only during processor reset.</td>
</tr>
</tbody>
</table>

**Related information**

- *Chapter C1 Debug* on page C1-365
- *Chapter C6 AArch32 debug registers* on page C6-409
- *Chapter C7 Memory-mapped debug registers* on page C7-423
- Debug memory mapped registers
- ROM table
A.15 APB interface signals

The debug APB bus supports clock, reset, addressing, and data handling signals when the processor includes an APB interface to provide access to the debug and performance monitoring registers.

You must balance all APB interface signals with respect to CLKin and time them relative to PCLKENDBG.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>nPRESETDBG</td>
<td>Input</td>
<td>APB reset, active-LOW: 0 Apply reset to APB interface. 1 Do not apply reset to APB interface.</td>
</tr>
<tr>
<td>PADDRDBG[21:2]</td>
<td>Input</td>
<td>APB address bus.</td>
</tr>
<tr>
<td>PADDRDBG31</td>
<td>Input</td>
<td>APB address bus bit[31]: 0 Not an external debugger access. 1 External debugger access.</td>
</tr>
<tr>
<td>PCLKENDBG</td>
<td>Input</td>
<td>APB clock enable.</td>
</tr>
<tr>
<td>PENABLEDBG</td>
<td>Input</td>
<td>Indicates the second and subsequent cycles of an APB transfer.</td>
</tr>
<tr>
<td>PRDATADBG[31:0]</td>
<td>Output</td>
<td>APB read data.</td>
</tr>
<tr>
<td>PREADYDBG</td>
<td>Output</td>
<td>APB slave ready.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>An APB slave can deassert PREADYDBG to extend a transfer by inserting wait states.</td>
</tr>
<tr>
<td>PSELDDBG</td>
<td>Input</td>
<td>Debug bus access.</td>
</tr>
<tr>
<td>PSLVERRDBG</td>
<td>Output</td>
<td>APB slave transfer error: 0 No transfer error. 1 Transfer error.</td>
</tr>
<tr>
<td>PWDATA[31:0]</td>
<td>Input</td>
<td>APB write data.</td>
</tr>
<tr>
<td>PWRITEDBG</td>
<td>Input</td>
<td>APB read or write signal: 0 Reads from APB. 1 Writes to APB.</td>
</tr>
</tbody>
</table>

Table A-43 APB interface signals
A.16 ATB interface signals

The ATB bus supports clock and data handling signals when the processor includes an ATB interface for each core to output trace information for debugging.

This interface exists only if the processor is configured to have one or more ETMs.

You must balance all ATB interface signals with respect to CLIN and time them relative to ATCLKEN.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ATCLKEN</td>
<td>Input</td>
<td>ATB clock enable</td>
</tr>
<tr>
<td>ATREADYMx</td>
<td>Input</td>
<td>ATB device ready</td>
</tr>
<tr>
<td>AFVALIDMx</td>
<td>Input</td>
<td>FIFO flush request</td>
</tr>
<tr>
<td>ATDATAMx[31:0]</td>
<td>Output</td>
<td>Data</td>
</tr>
<tr>
<td>ATVALIDMx</td>
<td>Output</td>
<td>Data valid</td>
</tr>
<tr>
<td>ATBYTESMx[1:0]</td>
<td>Output</td>
<td>Data size</td>
</tr>
<tr>
<td>AFREADYMx</td>
<td>Output</td>
<td>FIFO flush finished</td>
</tr>
<tr>
<td>ATIDMx[6:0]</td>
<td>Output</td>
<td>Trace source ID</td>
</tr>
<tr>
<td>SYNCREQMx</td>
<td>Input</td>
<td>Synchronization request from the trace sink</td>
</tr>
</tbody>
</table>
A.17 ETM signals

The processor has signals to receive information from an external trace device. This interface exists only if the processor is configured to have one or more ETMs.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSVALUEB[63:0]</td>
<td>Input</td>
<td>Timestamp in binary encoding</td>
</tr>
</tbody>
</table>
A.18 PMU interface signals

The processor uses the PMU signals to communicate with the external performance monitoring device.

Table A-46  PMU interface signals

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMUEVENTx[29:0]</td>
<td>Output</td>
<td>PMU event bus</td>
</tr>
<tr>
<td>nPMUIRQ[CN:0]</td>
<td>Output</td>
<td>PMU interrupt request</td>
</tr>
</tbody>
</table>


A.19 CTI interface signals

The processor supports various cross-trigger signals when it implements the CTI.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTICHIN[3:0]</td>
<td>Input</td>
<td>Channel In</td>
</tr>
<tr>
<td>CTICHOUTACK[3:0]</td>
<td>Input</td>
<td>Channel Out acknowledge</td>
</tr>
<tr>
<td>CTICHOUT[3:0]</td>
<td>Output</td>
<td>Channel Out</td>
</tr>
<tr>
<td>CTICHINACK[3:0]</td>
<td>Output</td>
<td>Channel In acknowledge</td>
</tr>
<tr>
<td>CISBYPASS</td>
<td>Input</td>
<td>Channel interface sync bypass</td>
</tr>
<tr>
<td>CIHSBYPASS[3:0]</td>
<td>Input</td>
<td>Channel interface H/S bypass</td>
</tr>
<tr>
<td>CTIRQ[CN:0]</td>
<td>Output</td>
<td>CTI interrupt, active-HIGH</td>
</tr>
<tr>
<td>CTIRQACK[CN:0]</td>
<td>Input</td>
<td>CTI interrupt acknowledge</td>
</tr>
</tbody>
</table>
A.20 DFT interface signals

The processor uses the DFT signals to communicate with the external test device.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFTRAMHOLD</td>
<td>Input</td>
<td>Disable the RAM chip select during scan testing</td>
</tr>
<tr>
<td>DFTRSTDISABLE</td>
<td>Input</td>
<td>Disable internal synchronized reset during scan shift</td>
</tr>
<tr>
<td>DFTCGEN</td>
<td>Input</td>
<td>Clock gate enable, forces on the clock grids during scan shift</td>
</tr>
<tr>
<td>DFTMCPHOLD</td>
<td>Input</td>
<td>Disable Multicycle Paths on RAM interfaces</td>
</tr>
</tbody>
</table>
A.21 MBIST interface signals

The processor does not include an external MBIST address and data interface port. The MBIST address and data interface ports are internally tied-off in the design, and you can insert MBIST into the design before synthesis. The process of adding MBIST into the design can be done automatically by an EDA MBIST tool.

<table>
<thead>
<tr>
<th>Signal</th>
<th>Direction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>MBISTREQ</td>
<td>Input</td>
<td>MBIST test request</td>
</tr>
<tr>
<td>nMBISTRESET</td>
<td>Input</td>
<td>MBIST reset</td>
</tr>
</tbody>
</table>
A Signal Descriptions

A.21 MBIST interface signals
Appendix B
AArch32 UNPREDICTABLE Behaviors

The cases in which the Cortex-A32 processor implementation diverges from the preferred behavior described in Armv8 AArch32 UNPREDICTABLE behaviors.

It contains the following sections:

• **B.1 Use of R15 by Instruction** on page Appx-B-652.
• **B.2 UNPREDICTABLE instructions within an IT Block** on page Appx-B-653.
• **B.3 Load/Store accesses crossing page boundaries** on page Appx-B-654.
• **B.4 Armv8 Debug UNPREDICTABLE behaviors** on page Appx-B-655.
• **B.5 Other UNPREDICTABLE behaviors** on page Appx-B-659.
B.1 Use of R15 by Instruction

If the use of R15 as a base register for a load or store is UNPREDICTABLE, the value used by the load or store using R15 as a base register is the Program Counter (PC) with its usual offset and, in the case of T32 instructions, with the forced word alignment. In this case, if the instruction specifies Writeback, then the load or store is performed without Writeback.

The Cortex-A32 core does not implement a Read 0 or Ignore Write policy on UNPREDICTABLE use of R15 by instruction. Instead, the Cortex-A32 core takes an UNDEFINED exception trap.
**B.2 UNPREDICTABLE instructions within an IT Block**

Conditional instructions within an IT Block, described as being unpredictable in the *Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile* pseudo-code, are executed unconditionally.

The Cortex-A32 core does not implement an unconditional execution policy for the following instructions. Instead all execute conditionally:

- NEON instructions new to Armv8.
- All instructions in the Armv8 Cryptographic Extensions.
- CRC32.
B.3 Load/Store accesses crossing page boundaries

The Cortex-A32 processor implements a set of behaviors for load or store accesses that cross page boundaries.

Crossing a page boundary with different memory types or shareability attributes

The Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile, states that a memory access from a load or store instruction that crosses a page boundary to a memory location that has a different memory type or shareability attribute results in constrained unpredictable behavior.

Crossing a 4KB boundary with a Device access

The Arm® Architecture Reference Manual Armv8, for Armv8-A architecture profile, states that a memory access from a load or store instruction to Device memory that crosses a 4KB boundary results in constrained unpredictable behavior.

Implementation (for both page boundary specifications)

For an access that crosses a page boundary, the Cortex-A32 processor implements the following behaviors:

- Store crossing a page boundary:
  - No alignment fault.
  - The access is split into two stores.
  - Each store uses the memory type and shareability attributes associated with its own address.

- Load crossing a page boundary (Device to Device and Normal to Normal):
  - No alignment fault.
  - The access is split into two loads.
  - Each load uses the memory type and shareability attributes associated with its own address.

- Load crossing a page boundary (Device to Normal and Normal to Device):
  - The instruction might generate an alignment fault.
  - If no fault is generated, the access is split into two loads.
  - Each load uses the memory type and shareability attributes associated with its own address.
### B.4 Armv8 Debug UNPREDICTABLE behaviors

This section describes the behavior that the Cortex-A32 processor implements when:

- A topic has multiple options.
- The behavior differs from either or both of the Options and Preferences behaviors.

**Note**

This section does not describe the behavior when a topic only has a single option and the processor implements the preferred behavior.

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>A32 BKPT instruction with condition code not AL</td>
<td>The processor implements the following preferred option: <strong>Executed unconditionally.</strong></td>
</tr>
<tr>
<td>Address match breakpoint match only on second halfword of an instruction</td>
<td>The processor generates a breakpoint on the instruction, unless it is a breakpoint on the second half of the first 32-bit instruction. In this case the breakpoint is taken on the following instruction.</td>
</tr>
<tr>
<td>Address matching breakpoint on A32 instruction with DBGBCRn.BAS=1100</td>
<td>The processor implements the following option: <strong>Does match.</strong></td>
</tr>
<tr>
<td>Address match breakpoint match on T32 instruction at DBGBCRn+2 with</td>
<td>The processor implements the following option: <strong>Does match.</strong></td>
</tr>
<tr>
<td>DBGBCRn.BAS=1111</td>
<td></td>
</tr>
<tr>
<td>Address mismatch breakpoint match on T32 instruction at DBGBCRn +2 with</td>
<td>The processor implements the following option: <strong>Does match.</strong></td>
</tr>
<tr>
<td>DBGBCRn.BAS=1111</td>
<td></td>
</tr>
<tr>
<td>Other mismatch breakpoint matches any address in current mode and state</td>
<td>The processor implements the following option: <strong>Immediate breakpoint debug event.</strong></td>
</tr>
<tr>
<td>Mismatch breakpoint on branch to self</td>
<td>The processor implements the following option: **Instruction is stepped an <strong>UNKNOWN</strong> number of times, while it continues to branch to itself.</td>
</tr>
<tr>
<td>Link to non-existent breakpoint or breakpoint that is not context-aware</td>
<td>The processor implements the following option: **No Breakpoint or Watchpoint debug event is generated, and the LBN field of the linker reads <strong>UNKNOWN.</strong></td>
</tr>
<tr>
<td>DBGWCRn_EL1.MASK!=00000 and DBGWCRn_EL1.BAS!=11111111</td>
<td>The processor behaves as indicated in the sole Preference: <strong>DBGWCRn_EL1.BAS is ignored and treated as if 0x11111111.</strong></td>
</tr>
<tr>
<td>Address-matching Vector catch on 32-bit T32 instruction at (vector-2)</td>
<td>The processor implements the following option: <strong>Does match.</strong></td>
</tr>
<tr>
<td>Address-matching Vector catch on 32-bit T32 instruction at (vector+2)</td>
<td>The processor implements the following option: <strong>Does match.</strong></td>
</tr>
<tr>
<td>Address-matching Vector catch and Breakpoint on same instruction</td>
<td>The processor implements the following option: <strong>Report Breakpoint.</strong></td>
</tr>
<tr>
<td>Scenario</td>
<td>Behavior</td>
</tr>
<tr>
<td>-------------------------------------------------------------------------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Address match breakpoint with DBGBCRn_EL1.BAS=0000</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• As if disabled.</td>
</tr>
<tr>
<td>DBGWCRn_EL1.BAS specifies a non-contiguous set of bytes within a double-word</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• A Watchpoint debug event is generated for each byte.</td>
</tr>
<tr>
<td>A32 HLT instruction with condition code not AL</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• Executed unconditionally.</td>
</tr>
<tr>
<td>Execute instruction at a given EL when the corresponding EDECCR bit is 1 and Halting is allowed</td>
<td>The processor behaves as follows:</td>
</tr>
<tr>
<td></td>
<td>• Generates debug event and Halt no later than the instruction following the next Context Synchronization operation (CSO) excluding ISB instruction.</td>
</tr>
<tr>
<td>Unlinked Context matching and Address mismatch breakpoints taken to Abort mode</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• A Prefetch Abort debug exception is generated. Because the breakpoint is configured to generate a breakpoint at PL1, the instruction at the Prefetch Abort vector generates a Vector catch debug event.</td>
</tr>
<tr>
<td></td>
<td>———— Note ————</td>
</tr>
<tr>
<td></td>
<td>The debug event is subject to the same CONSTRAINED UNPREDICTABLE behavior, therefore the Breakpoint debug event is repeatedly generated an UNKNOWN number of times.</td>
</tr>
<tr>
<td>Vector catch on Data or Prefetch abort, and taken to Abort mode</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• A Prefetch Abort debug exception is generated. If Vector catch is enabled on the Prefetch Abort vector, this generates a Vector catch debug event.</td>
</tr>
<tr>
<td></td>
<td>———— Note ————</td>
</tr>
<tr>
<td></td>
<td>The debug event is subject to the same CONSTRAINED UNPREDICTABLE behavior, therefore the Breakpoint debug event is repeatedly generated an UNKNOWN number of times.</td>
</tr>
<tr>
<td>H &gt; N or H = 0 at Non-secure EL1 and EL0, including value read from PMCR_EL0.N</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• A simple implementation where all of HPMN[4:0] are implemented, and In Non-secure EL1 and EL0:</td>
</tr>
<tr>
<td></td>
<td>— If H &gt; N then M = N.</td>
</tr>
<tr>
<td></td>
<td>— If H = 0 then M = 0.</td>
</tr>
<tr>
<td>H &gt; N or H = 0: value read back in MDCR_EL2.HPMN</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• A simple implementation where all of HPMN[4:0] are implemented and for reads of MDCR_EL2.HPMN, return H.</td>
</tr>
<tr>
<td>P ≥ M and P ≠ 31: reads and writes of PMXEVTYPER_EL0 and PMXEVCNTR_EL0</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• A simple implementation where all of SEL[4:0] are implemented, and if P ≥ M and P ≠ 31 then the register is RES0.</td>
</tr>
<tr>
<td>P ≥ M and P ≠ 31: value read in PMSELR_EL0.SEL</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• A simple implementation where all of SEL[4:0] are implemented, and if P ≥ M and P ≠ 31 then the register is RES0.</td>
</tr>
</tbody>
</table>
Table B-1  Armv8 Debug UNPREDICTABLE behaviors (continued)

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>$P = 31$: reads and writes of PMXEVCNTR_EL0</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• RES0.</td>
</tr>
<tr>
<td>$n \geq M$: Direct access to PMEVCNTRn_EL0 and PMEVTYPEPer_EL0</td>
<td>The processor implements:</td>
</tr>
<tr>
<td></td>
<td>• If $n \geq N$, then the instruction is UNALLOCATED.</td>
</tr>
<tr>
<td></td>
<td>• Otherwise if $n \geq M$, then the register is RES0.</td>
</tr>
<tr>
<td>Exiting Debug state while instruction issued through EDITR is in flight</td>
<td>The processor implements the following option:</td>
</tr>
<tr>
<td></td>
<td>• The instruction completes in Debug state before executing the restart.</td>
</tr>
<tr>
<td>Using memory-access mode with a non-word-aligned address</td>
<td>The processor behaves as indicated in the sole Preference:</td>
</tr>
<tr>
<td></td>
<td>• Does unaligned accesses, faulting if these are not permitted for the memory type.</td>
</tr>
<tr>
<td>Access to memory-mapped registers mapped to Normal memory</td>
<td>The processor behaves as indicated in the sole Preference:</td>
</tr>
<tr>
<td></td>
<td>• The access is generated, and accesses might be repeated, gathered, split or resized, in accordance with the rules for Normal memory, meaning the effect is UNPREDICTABLE.</td>
</tr>
<tr>
<td>Not word-sized accesses</td>
<td>The processor behaves as indicated in the sole Preference:</td>
</tr>
<tr>
<td></td>
<td>• Reads occur and return UNKNOWN data.</td>
</tr>
<tr>
<td></td>
<td>• Writes set the accessed register(s) to UNKNOWN.</td>
</tr>
<tr>
<td>External debug write to register that is being reset</td>
<td>The processor behaves as indicated in the sole Preference:</td>
</tr>
<tr>
<td></td>
<td>• Takes reset value.</td>
</tr>
<tr>
<td>Scenario</td>
<td>Behavior</td>
</tr>
<tr>
<td>-------------------------------------------------------------------------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Accessing reserved debug registers</td>
<td>The processor deviates from Preferred behavior because the hardware cost to decode some of these addresses in debug power domain is significantly high:</td>
</tr>
<tr>
<td></td>
<td><strong>Actual behavior:</strong></td>
</tr>
<tr>
<td></td>
<td>1. For reserved debug and Performance Monitors registers the response is <strong>CONSTRAINED UNPREDICTABLE Error</strong> or <strong>RES0</strong>, when any of the following error instead of preferred <strong>RES0</strong> for reserved debug registers 0x000-0xCFC and reserved PMU registers 0x000-0xF00:</td>
</tr>
<tr>
<td></td>
<td><strong>Off</strong></td>
</tr>
<tr>
<td></td>
<td>Core power domain is either completely off, or in a low-power state where the Core power domain registers cannot be accessed.</td>
</tr>
<tr>
<td></td>
<td><strong>DLK</strong></td>
</tr>
<tr>
<td></td>
<td>DoubleLockStatus() is TRUE, OS double-lock is locked, that is, EDPRSR.DLK is 1.</td>
</tr>
<tr>
<td></td>
<td><strong>OSLK</strong></td>
</tr>
<tr>
<td></td>
<td>OSLR_EL1.OSLK is1, OS lock is locked.</td>
</tr>
<tr>
<td></td>
<td>2. In addition, for reserved debug registers in the address ranges 0x400 to 0x4FC and 0x800 to 0x8FC, the response is <strong>CONSTRAINED UNPREDICTABLE Error</strong> or <strong>RES0</strong> when the conditions in 1 do not apply and:</td>
</tr>
<tr>
<td></td>
<td><strong>EDAD</strong></td>
</tr>
<tr>
<td></td>
<td>AllowExternalDebugAccess() is FALSE, external debug access is disabled.</td>
</tr>
<tr>
<td></td>
<td>3. For reserved Performance Monitor registers in the address ranges 0x000 to 0x8FC and 0x400 to 0x47F, the response is <strong>CONSTRAINED UNPREDICTABLE Error</strong>, or <strong>RES0</strong> when the conditions in 1 and 2 do not apply, and the following errors instead of preferred res0 for the these registers:</td>
</tr>
<tr>
<td></td>
<td><strong>EPMAD</strong></td>
</tr>
<tr>
<td></td>
<td>AllowExternalPMUAccess() is FALSE (external Performance Monitors access is disabled).</td>
</tr>
<tr>
<td>Clearing the <strong>clear-after-read</strong> EDPRSR bits when Core power domain is on, and DoubleLockStatus() is TRUE</td>
<td>The processor behaves as indicated in the sole Preference:</td>
</tr>
<tr>
<td></td>
<td>• Bits are not cleared to zero.</td>
</tr>
</tbody>
</table>
### B.5 Other UNPREDICTABLE behaviors

This section describes other UNPREDICTABLE behaviors.

<table>
<thead>
<tr>
<th>Scenario</th>
<th>Description</th>
</tr>
</thead>
</table>
| CSSEL.R indicates a cache that is not implemented. | If CSSEL.R indicates a cache that is not implemented, then on a read of the CCSIDR the behavior is CONSTRAINED UNPREDICTABLE, and can be one of the following:  
  - The CCSIDR read is treated as NOP.  
  - The CCSIDR read is UNDEFINED.  
  - The CCSIDR read returns an UNKNOWN value (preferred). |
| HDCR.HPMN is set to 0, or to a value larger than PMCR.N. | If HDCR.HPMN is set to 0, or to a value larger than PMCR.N, then the behavior in Non-secure EL0 and EL1 is CONSTRAINED UNPREDICTABLE, and one of the following must happen:  
  - The number of counters accessible is an UNKNOWN non-zero value less than PMCR.N.  
  - There is no access to any counters.  

For reads of HDCR.HPMN by EL2 or higher, if this field is set to 0 or to a value larger than PMCR.N, the core must return a CONSTRAINED UNPREDICTABLE value that is one of:  
  - PMCR.N.  
  - The value that was written to HDCR.HPMN.  
  - (The value that was written to HDCR.HPMN) modulo 2^h, where h is the smallest number of bits required for a value in the range 0 to PMCR.N. |
Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:

• C.1 Revisions on page Appx-C-662.
C.1 Revisions

This section describes the technical changes between released issues of this document.

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<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
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<td>First release for r0p0.</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>First release for r0p1.</td>
<td>On front page and in document history table.</td>
<td>r0p1</td>
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<td>B1.96 Main ID Register on page B1-307.</td>
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<td>B2.3 CPU Interface Identification Register on page B2-354.</td>
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<tr>
<td>B2.8 VM CPU Interface Identification Register on page B2-359.</td>
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<tr>
<td>C7.11 External Debug Peripheral Identification Register 1 on page C7-440.</td>
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<tr>
<td>C8.8 ROM Table Peripheral Identification Register 2 on page C8-462.</td>
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<td>C10.13 Trace ID Register on page C10-520.</td>
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<tr>
<td>C10.68 ETM Peripheral Identification Register 2 on page C10-586.</td>
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<td></td>
</tr>
<tr>
<td>C11.8 CTI Peripheral Identification Register 2 on page C11-605.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>References to internal memory-mapped removed.</td>
<td>B1.96 Main ID Register on page B1-307.</td>
<td>All versions</td>
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<tr>
<td>B1.97 Multiprocessor Affinity Register on page B1-309.</td>
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</tr>
<tr>
<td>C7.1 Memory-mapped debug register summary on page C7-424.</td>
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<tr>
<td>C9.1 AArch32 PMU register summary on page C9-472.</td>
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<td></td>
</tr>
<tr>
<td>C9.5 Memory-mapped PMU register summary on page C9-483.</td>
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<tr>
<td>C11.1 Cross trigger register summary on page C11-596.</td>
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<td></td>
</tr>
<tr>
<td>nSEI, nREI, and nVSEI clarified in GIC signals table.</td>
<td>A.5 GIC signals on page Appx-A-622.</td>
<td>All versions</td>
</tr>
<tr>
<td>Change</td>
<td>Location</td>
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<tr>
<td>First release for r1p0</td>
<td>Revision history table</td>
<td>r1p0</td>
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<tr>
<td>B1.96 Main ID Register on page B1-307</td>
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<tr>
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<td>B2.8 VM CPU Interface Identification Register on page B2-359.</td>
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<tr>
<td>C8.8 ROM Table Peripheral Identification Register 2 on page C8-462.</td>
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<tr>
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<td></td>
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<tr>
<td>C11.8 CTI Peripheral Identification Register 2 on page C11-605.</td>
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<tr>
<td>MIDR and VPIDR reset values in B1.2 c0 registers on page B1-146, B1.20 AArch32 Identification registers on page B1-170 and B1.28 AArch32 Virtualization registers on page B1-180.</td>
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</tr>
<tr>
<td>GICV_IIDR reset value in B2.6 Virtual CPU interface register summary on page B2-357.</td>
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<tr>
<td>Updated company name from Arm to Arm</td>
<td>Entire manual</td>
<td>All versions</td>
</tr>
<tr>
<td>Updated all sections affected by the addition of a new asymmetric floating-point/NEON feature</td>
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<td>r1p0</td>
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<tr>
<td>• A1.3 Implementation options on page A1-28</td>
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<td>• A2.1 Components on page A2-36</td>
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<td>• A.7 Power management signals on page Appx-A-626</td>
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</tr>
<tr>
<td>Updated all sections affected by the additional of the CP15SDISABLE2 signal</td>
<td></td>
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<td>• B1.47 Domain Access Control Register on page B1-215</td>
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<td>• B1.107 Secure Debug Enable Register on page B1-330</td>
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<td>• B1.110 Translation Table Base Control Register on page B1-333</td>
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<td>• B1.116 Translation Table Base Register 1 on page B1-342</td>
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</tr>
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<td>• B1.119 Vector Base Address Register on page B1-346</td>
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<td></td>
</tr>
<tr>
<td>Fixed incorrect MRC/MCR encodings</td>
<td>C9.2 Performance Monitors Control Register on page C9-474</td>
<td>All versions</td>
</tr>
<tr>
<td>Clarified the L2 cache behavior when disabled</td>
<td>A5.4 Disabling a cache on page A5-77</td>
<td>All versions</td>
</tr>
<tr>
<td>Added warm reset information</td>
<td>A3.3 Resets on page A3-48</td>
<td>All versions</td>
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</table>