Arm® Versatile™ Express Beetle IoT Evaluation Board

V2M-Beetle Technical Reference Manual

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Arm® Versatile™ Express Beetle IoT Evaluation Board

V2M-Beetle Technical Reference Manual

Release Information

Document History

Issue	Date	Confidentiality	Change
0000-00	01 June 2016	Non-Confidential	First issue of Technical Reference Manual

Non-Confidential Proprietary Notice

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Product Status

The information in this document is Final, that is for a developed product.

Web Address

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Conformance Notices

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling Versatile™ *Express* boards.

The motherboard generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the target board
- Reorient the receiving antenna
- Increase the distance between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables are used.

Contents
Arm® Versatile™ Express Beetle IoT Evaluation Board V2M-Beetle Technical Reference Manual

Preface

This preface introduces the *Arm® Versatile™ Express Beetle IoT Evaluation Board V2M-Beetle Technical Reference Manual*.

It contains the following:

About this book

This book describes the Arm® Versatile™ *Express* (V2M-Beetle) Internet of Things (IoT) evaluation board.

Product revision status

The r*m*p*n* identifier indicates the revision status of the product described in this book, for example, r*1*p*2*, where:

r*m* Identifies the major revision of the product, for example, r1.

p*n* Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced software developers to aid IoT endpoint development using the V2M-Beetle evaluation board.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter introduces the V2M-Beetle evaluation board.

Chapter 2 Hardware Description
This chapter describes the Versatile™ *Express* Internet of Things evaluation board hardware.

Chapter 3 Board Configuration and operating modes
This chapter describes board configuration during powerup, loading boot code and test chip programming, CMSIS-DAP programming, and board operating modes.

Chapter 4 Programmers Model
This chapter describes the programmers model of the V2M-Beetle evaluation board.

Appendix A.1 Signal Descriptions
This appendix describes the signals present at the interface connectors of the V2M-Beetle evaluation board.

Appendix B.2 Specifications
This specification contains the electrical specifications of the V2M-Beetle evaluation board.

Appendix C.3 Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Glossary is a list of terms used in documentation, together with definitions for those terms. The Glossary does not contain terms that are industry standard unless the meaning differs from the generally accepted meaning.

See the *Arm® Glossary* for more information.

Typographic conventions

italic
Introduces special terminology, denotes cross-references, and citations.

bold
Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

`monospace`
: Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

`monospace`
: Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

`monospace italic`
: Denotes arguments to monospace text where the argument is to be replaced by a specific value.

`monospace bold`
: Denotes language keywords when used outside example code.

`<and>`
: Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

SMALL CAPITALS
: Used in body text for a few terms that have specific technical meanings, that are defined in the *Glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

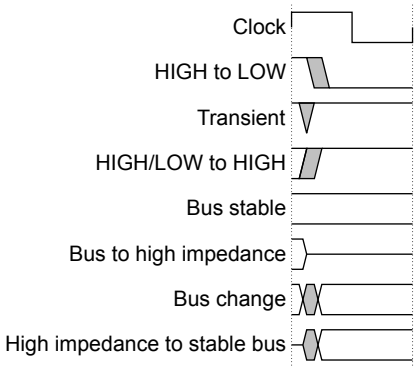

Figure 1 Key to timing diagram conventions

Signals

The signal conventions are:

Signal level
: The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n
: At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This book contains information that is specific to this product. See the following documents for other relevant information.

Arm publications

- *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* (ARM DDI 0551)
- *ARM® Cordio® BT4 Radio IP Integration Manual* (ARM DII 0299)
- *Cortex-M™ System Design Kit Technical Reference Manual* (ARM DDI 0479)
- *ARM® PrimeCell Technical Reference Manual Real Time Clock (PL031)* (ARM DDI 0224)

Other publications

- See the Arduino website *https://www.arduino.cc/* for information about Arduino and Arduino-compatible shields.

Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to *errata@arm.com*. Give:

- The title *Arm Versatile Express Beetle IoT Evaluation Board V2M-Beetle Technical Reference Manual*.
- The number 100417_0000_00_en.
- If applicable, the page number(s) to which your comments refer.
- A concise explanation of your comments.

also welcomes general suggestions for additions and improvements.

Note

tests the PDF only in Adobe Acrobat and Acrobat Reader, and cannot guarantee the quality of the represented document when used with any other PDF reader.

Chapter 1
Introduction

This chapter introduces the V2M-Beetle evaluation board.

It contains the following sections:

1.1 Precautions

You can take certain precautions to ensure safety and to prevent damage to your V2M-Beetle evaluation board.

This section contains the following subsections:

1.1.1 Ensuring safety

There are two alternative power sources for the V2M-Beetle evaluation board, the USB host 5V supply, or two 1.5V AAA batteries.

——— Warning ———

Do not use the V2M-Beetle evaluation board near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.

———————————

1.1.2 Preventing damage

The V2M-Beetle evaluation board is intended for use within a laboratory or engineering development environment.

——— Caution ———

To avoid damage to the V2M-Beetle evaluation board, observe the following precautions:

- Connect the external power supply to the board before powerup.
- Never subject the board to high electrostatic potentials. Observe Electrostatic discharge (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not use the board near a source of electromagnetic emissions other than Bluetooth radios.
- Do not fit an expansion shield while power, either 5V USB or AAA batteries, is applied to the V2M-Beetle evaluation board.

———————————

1.2 About the V2M-Beetle evaluation board

The V2M-Beetle evaluation board provides access to the Beetle test chip to enable hardware and software development for Internet of Things (IoT) applications.

V2M-Beetle evaluation board and Beetle test chip

The Beetle test chip is based on the IoT Subsystem for Cortex®-M.

The V2M-Beetle board provides:

- One Beetle test chip:
  - One IoT Subsystem for Cortex-M that incorporates a Cortex-M3.
  - One Arm Cordio BT4, a Bluetooth Low-Energy radio block.

  Note

  The Beetle test chip is designed as a test vehicle. ARM does not guarantee that all test chip functionality has been tested or validated.

- Headers that enable fitting of an Arduino-compatible R3 expansion shield:
  - 16 GPIO signals.
  - Power to the expansion shield.
  - I^2C interface.
  - SPI interface.
  - UART interface.
  - Six Analog signals from the expansion shield to an ADC on V2M-Beetle evaluation board. The output of the ADC is input to the Beetle test chip.

  Note

  The board might not be compatible with all available Arduino-compatible R3 expansion shields. Check the shield requirements against the Beetle board specification. For example, some shields require the analog pins A0-A5 to be digital output capable, which this board does not support. Also, check the shield power requirements. Beetle 3V3 and 5V can each provide a maximum of 200mA.

- A 50Ω on-board antenna.
- One motion sensor:
  - 3-axis orientation and motion sensing.
- One temperature sensor.

Internet of Things (IoT) development

The V2M-Beetle evaluation board, incorporating the Beetle test chip, enables IoT endpoint development with expansion by fitting an Arduino-compatible R3 expansion shield.

1.3 Layout of the V2M-Beetle evaluation board

The following figures show the physical layout of the V2M-Beetle evaluation board.

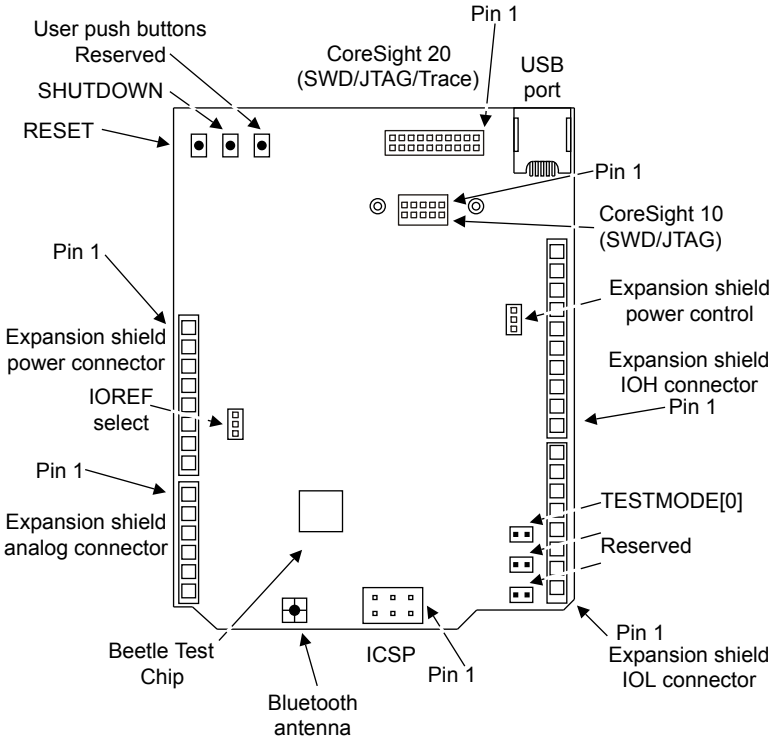

Figure 1-1 V2M-Beetle evaluation board upper face

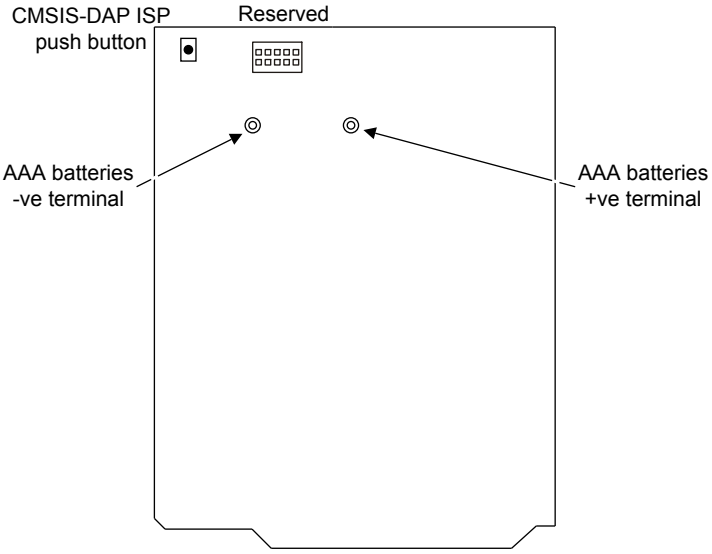

Figure 1-2 V2M-Beetle evaluation board lower face

Chapter 2
Hardware Description

This chapter describes the Versatile™ *Express* Internet of Things evaluation board hardware.

It contains the following sections:

2.1 Overview of the V2M-Beetle evaluation board

The hardware infrastructure of the V2M-Beetle evaluation board supports IoT endpoint development by providing access to the Beetle test chip.

The following figure shows the hardware infrastructure of the V2M-Beetle board.

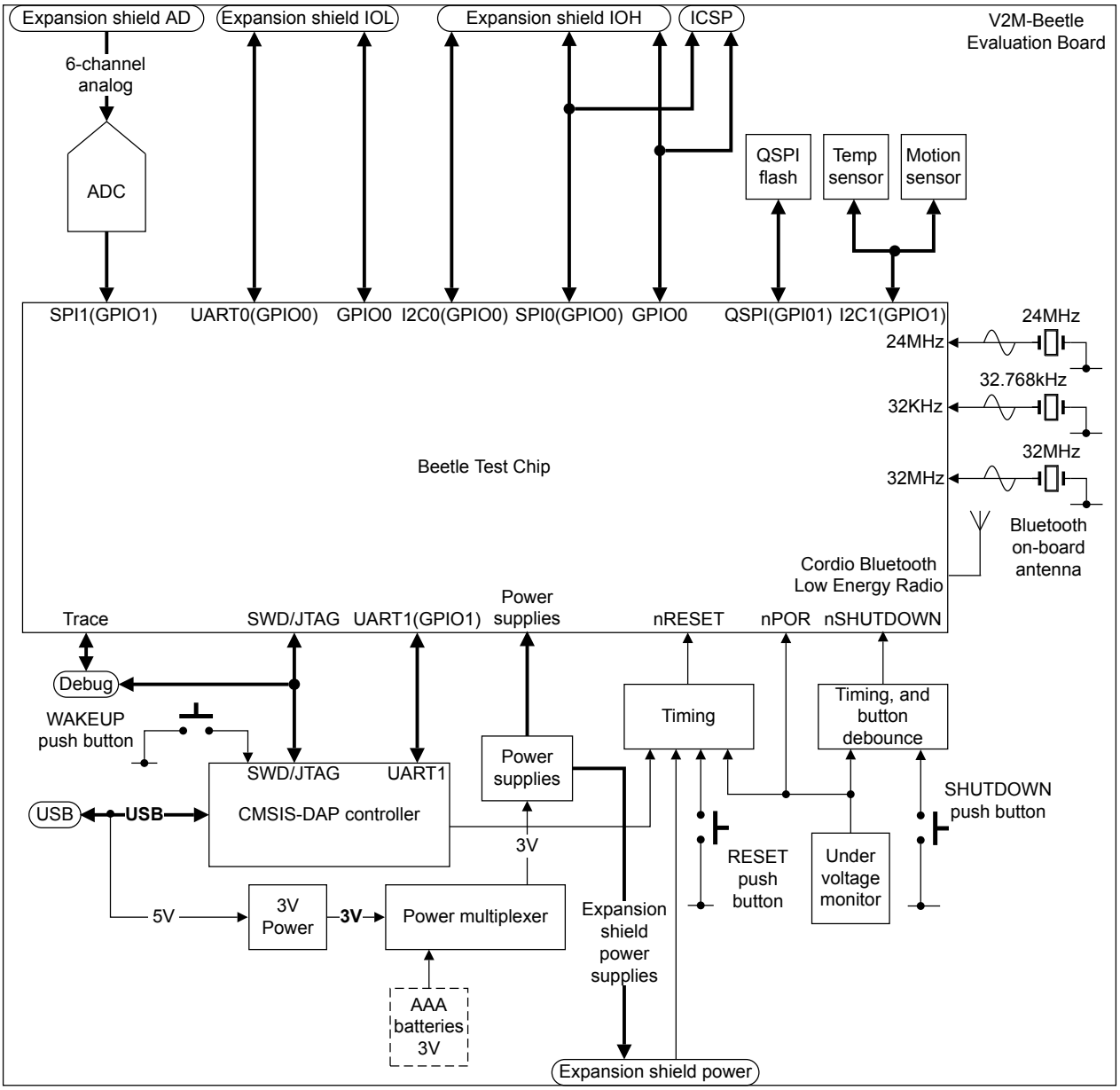

Figure 2-1 V2M-Beetle board system architecture with fitted Arduino-compatible R3 expansion shield

The V2M-Beetle board contains the following components and interfaces:

- Beetle test chip:
  - IoT Subsystem for Cortex-M.
  - RF port that connects to the 50Ω on-board antenna on the V2M-Beetle board.
  - Cortex-M3, part of the IoT Subsystem for Cortex-M
- USB port and CMSIS-DAP controller that provides programming and debug access:

  - Drag-and-drop system software image programming.
  - CMSIS-DAP software debug.
  - Virtual UART access over USB.
  - Reset over USB and from external debugger.
- Debug port:
  - Serial Wire Debug (SWD).
  - 4-bit trace.
  - P-JTAG debug.
  - Beetle test chip debug when the CMSIS-DAP controller is powered down.
- QSPI flash:
  - 256K alternative bootup memory for the Cortex-M3, an alternative to the embedded flash (eFlash) in the Beetle test chip.
- 32kHz crystal oscillator:
  - Drives the Cordio BT4 Bluetooth RF block in the Beetle test chip.
  - Available as an input to the test chip clock prescaler circuitry.
- 32MHz oscillator:
  - Drives the Cordio BT4 Bluetooth RF block in the Beetle test chip.
- 24MHz oscillator:
  - Drives the clock PLL in the Beetle test chip.
- Analog to Digital Converter (ADC):
  - 6-channel analog input from the expansion shield.
  - Analog reference voltage from the expansion shield.
  - SPI output to the SPI1 interface in the Beetle test chip.

  Note

  The ADC is only available when the expansion shield power is enabled. When the expansion shield power is not enabled, configure the ADC pins on the Beetle test chip as GPIO pins to save power.

- Temperature and motion sensors:
  - One motion sensor with 3-axis orientation and motion sensing.
  - One temperature sensor.
  - The sensors send data to the I2C1 interface in the Beetle test chip.
- Two power sources:
  - External 5V power through the USB port.
  - Two AAA batteries (optional).

  Note

  The choice of power source determines which operating and power modes are available to the board.

- Board shutdown system that resets the Cortex-M3 and causes the system to enter the shutdown sequence. The shutdown sources are:
  - User shutdown push button.
  - On-board under-voltage monitor.
- Board reset system that resets all hardware on the board except the eFlash power controller. The reset sources are:
  - Power on RC delay.
  - User reset push button.
  - CMSIS-DAP reset over USB.
  - Reset signal from expansion shield power connector.
  - Reset signal from external debugger.
- Expansion shield AD connector that carries six analog signals to the ADC.
- Expansion shield I/O Low (IOL) connector that carries:
  - Six GPIO signals from the Beetle test chip.
  - Two multiplexed UART0-GPIO0 signals from the Beetle test chip.

- Expansion shield I/O High (IOH) connector that carries:
  - Two GPIO signals from the Beetle test chip.
  - Four multiplexed SPI0-GPIO0 signals from the Beetle test chip.
  - Two multiplexed I2C0-GPIO0 signals from the Beetle test chip.
  - ADC analog reference voltage from the expansion shield.
- Expansion shield power connector that carries:
  - 5V and 3V power to the fitted expansion shield.
  - 3V3 reference for the I/O digital pins.
  - Reset signal to the CMSIS-DAP controller on the V2M-Beetle board.
  - Raw reference voltage for local voltage regulator on the expansion shield.

Note

The V2M-Beetle board:
- Accepts Arduino-compatible R3 expansion shields.
- Outputs signals at 3V.

- ICSP connector:
  - Enables In-Circuit Serial Programming.

See the *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* for more information about the IoT Subsystem for Cortex-M.

2.2 Architecture of the Beetle test chip

The test chip provides facilities to aid IoT endpoint development.

The following figure shows the architecture of the Beetle test chip.

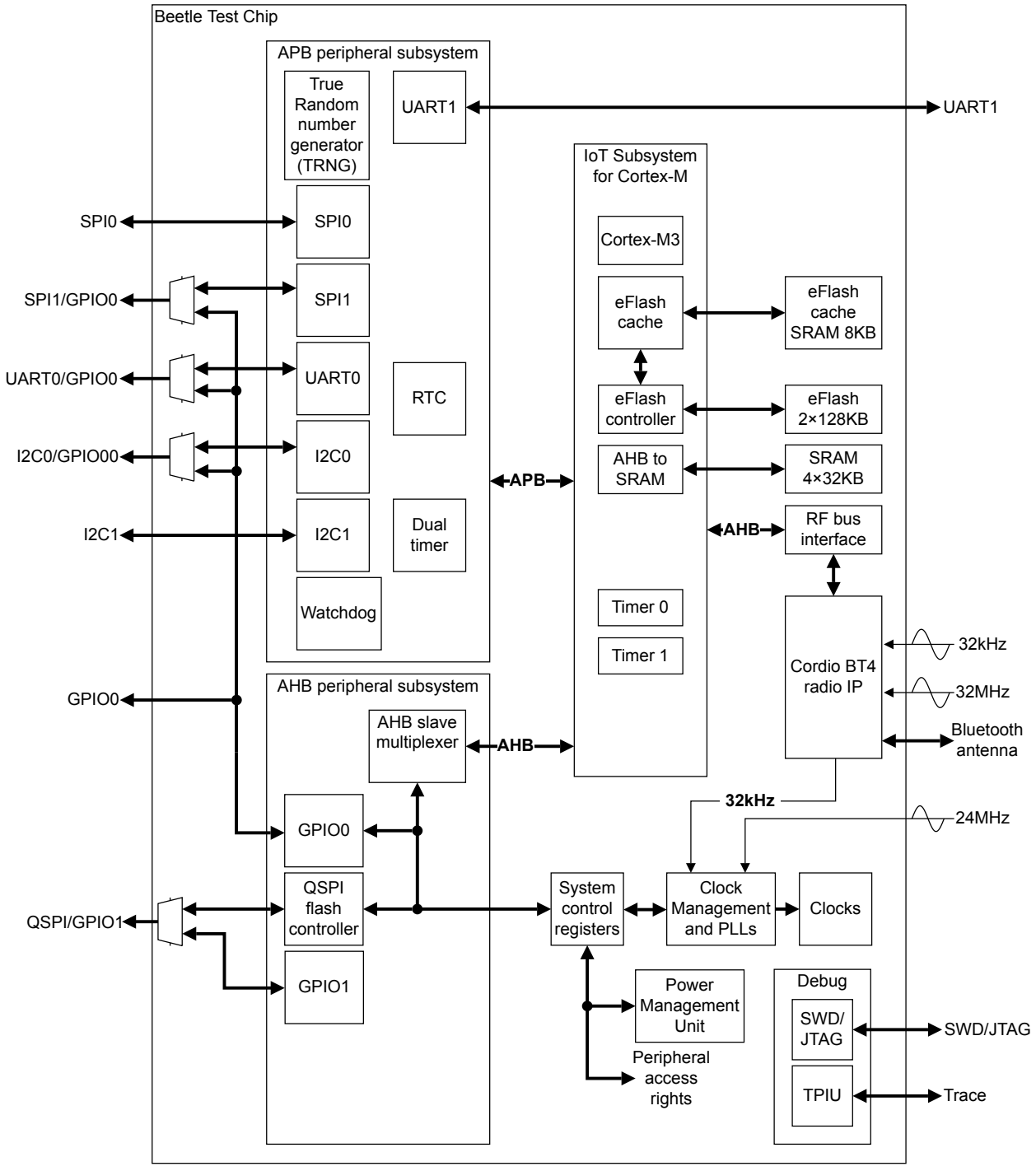

Figure 2-2 Architecture of the test chip

The Beetle test chip contains the following components and interfaces:

- IoT Subsystem for Cortex-M:

  - Cortex-M3 processor.
  - Two independent timers.
  - SRAM controller, part of the SRAM memory subsystem.
- eFlash memory subsystem:
  - eFlash controller, in the IoT Compute subsystem.
  - eFlash cache, in the IoT Compute subsystem. It caches instructions and data that are stored in the eFlash.
  - 2×128KB eFlash memory.
- SRAM memory subsystem:
  - 4×32KB.
- APB peripheral subsystem:
  - SPI interface, *SPI1*, that connects to the output of the ADC on the V2M-Beetle board.
  - SPI interface, *SPI0*, that connects to the expansion shield IOH connector.
  - UART interface, *UART0*, that connects to the expansion shield IOL connector.
  - UART interface, *UART1*, that connects to the CMSIS-DAP virtual UART port on the V2M-Beetle board.
  - I^2C interface, *I2C0*, that connects to the IOH connector on the V2M-Beetle board.
  - Watchdog timer.
  - Dual-timer.
  - *Real-time clock* (RTC).
  - True Random number generator (TRNG).

    Note

    The SPI interfaces natively support only 8-bit mode.

- AHB peripheral subsystem:
  - GPIO interface *GPIO0* that connects to the expansion shield IOL and IOH connectors.
  - I^2C interface, *I2C1*, that connects to the temperature and motion sensors on the V2M-Beetle board.
  - QuadSPI flash controller that connects to the *QuadSPI* flash memory on the V2M-Beetle board.

    Note

    The *SPI1*, *UART0*, *I2C0* and, QuadSPI flash controller interface signals are multiplexed outputs. The multiplexers can select either the interface functions, or GPIO, as output.

    Normal test chip operation occurs when the interface functions are selected. See *2.3 Beetle test chip GPIO interface* on page 2-22 for a description of the GPIO multiplexing scheme.

- System control:
  - The system control registers provide clock configuration and control, and peripheral access permission configuration.
- Bluetooth radio:
  - ARM Cordio BT4 radio, a Bluetooth Low Energy (BLE) RF block.
  - Host Controller Interface (HCI) to the Cortex-M3.
  - Imports a 32MHz signal and a 32kHz signal from crystal oscillators on the V2M-Beetle evaluation board. It exports the 32kHz clock signal to other systems in the Beetle test chip.
- Debug:
  - 4-bit trace port from the *Trace Port Interface Unit* (TPIU) in the Beetle test chip.
  - SWD/JTAG port.

See *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* for information on the IoT Subsystem for Cortex-M and the following blocks:

- Timers.
- eFlash memory system.
- SRAM memory system.

See *Cortex-M™ System Design Kit Technical Reference Manual* for information about the following blocks:

- GPIO interfaces.
- Watchdog.
- UARTs.
- Dual timer.

See *ARM® Cordio® BT4 Radio IP Integration Manual* for information about the Cordio BT4 Bluetooth Low Energy RF block.

2.3 Beetle test chip GPIO interface

The Beetle test chip multiplexes general-purpose I/O (GPIO) with SPI, UART, I^2C, and QSPI signals.

The GPIO registers, GPIO0ALTFUNCSET, GPIO1ALTFUNCSET, GPIO0ALTFUNCCLR, and GPIO1ALTFUNCCLR, select the multiplexed signals. The following table shows the GPIO multiplexing scheme including the connectivity of the multiplexed signals. You must select the alternative functions for normal and full operation of the test chip.

Table 2-1 Beetle test chip multiplexed GPIO signals

GPIO default function (AHB peripheral subsystem)	Alternative function	Connectivity	Source of alternative function on test chip
GPIO0[0]	UART0 RxD (In)	Expansion shield IOL connector pin 1	APB peripheral subsystem
GPIO0[1]	UART0 TxD (Out)	Expansion shield IOL connector pin 2	
GPIO0[2]	-	Expansion shield IOL connector pin 3	-
GPIO0[3]		Expansion shield IOL connector pin 4	
GPIO0[4]		Expansion shield IOL connector pin 5	
GPIO0[5]		Expansion shield IOL connector pin 6	
GPIO0[6]		Expansion shield IOL connector pin 7	
GPIO0[7]		Expansion shield IOL connector pin 8	
GPIO0[8]		Expansion shield IOH connector pin 1	
GPIO0[9]		Expansion shield IOH connector pin 2	

Table 2-1 Beetle test chip multiplexed GPIO signals (continued)

GPIO default function (AHB peripheral subsystem)	Alternative function	Connectivity	Source of alternative function on test chip
GPIO0[10]	SPI0 nSS[0]	Expansion shield IOH connector pin 3	APB peripheral subsystem
GPIO0[11]	SPI0 MOSI (Out)	Expansion shield IOH connector pin 4	
GPIO0[12]	SPI0 MISO (In)	Expansion shield IOH connector pin 5	
GPIO0[13]	SPI0 SCK (Out)	Expansion shield IOH connector pin 6	
GPIO0[14]	I2C0 Data (SDA)	Expansion shield IOH connector pin 9	
GPIO0[15]	I2C0 Clock (SCL)	Expansion shield IOH connector pin 10	
GPIO1[0]	UART1 RxD (In)	CMSIS-DAP controller	
GPIO1[1]	UART1 TxD (Out)		
GPIO1[2]	SPI1 nSS[0]	ADC	
GPIO1[3]	SPI1 MOSI (Out)		
GPIO1[4]	SPI1 MISO (In)		
GPIO1[5]	SPI1 SCK (Out)		
GPIO1[6]	I2C1 Data (SDA)	Temperature and motion sensors	
GPIO1[7]	I2C1 Clock (SCL)		
GPIO1[8]	I2C1 Interrupt		
GPIO1[9]	QSPI CS1	QSPI flash	AHB peripheral subsystem
GPIO1[10]	QSPI IOF0		
GPIO1[11]	QSPI IOF1		
GPIO1[12]	QSPI IOF2		
GPIO1[13]	QSPI IOF3		
GPIO1[14]	QSPI IOF4		
GPIO1[15]	-	Expansion shield power enable system on V2M-Beetle evaluation board.	APB peripheral subsystem

Related concepts

4.6 GPIO registers on page 4-57

Related reference

Expansion shield IOL connector on page Appx-A-0

Expansion shield IOH connector on page Appx-A-0

2.4 Clocks

The V2M-Beetle evaluation board contains 24MHz and 32kHz crystal oscillators which drive the systems on the board and in the Beetle test chip.

Overview of clocks

The following figure shows the V2M-Beetle evaluation board and test chip system clocks.

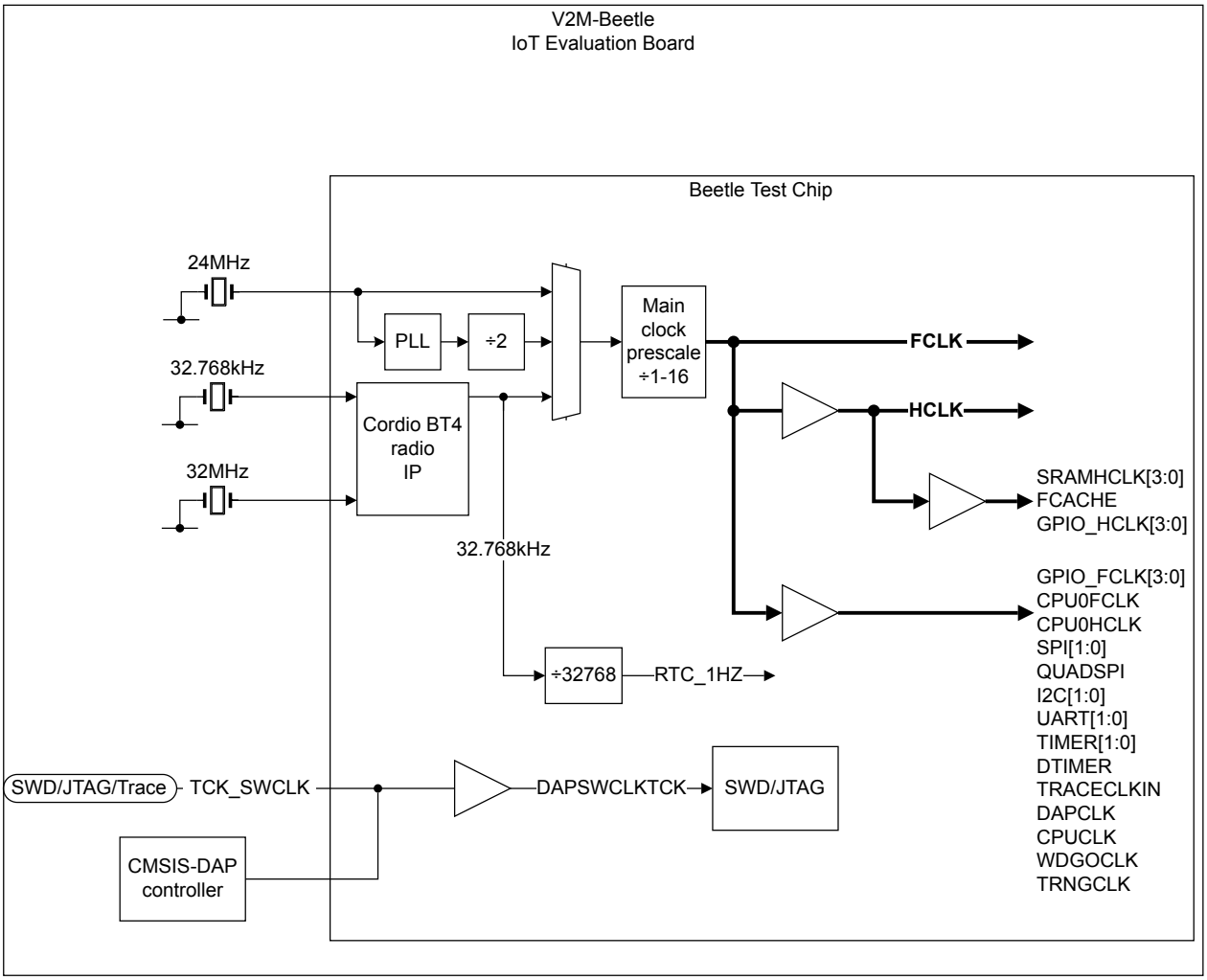

Figure 2-3 Beetle test chip clocks

System control register MAINCLK controls the input clock multiplexer and the output prescaler. The input is **CLK24MHZ** and the default prescaler setting is *bypass prescaler*, that is, no frequency division. The DAPlink chip provides the debug clock **TCK_SWCLK**.

The debug clock, **TCK_SWCLK**, has two sources. It can come from the debug connector or from the CMSIS-DAP controller.

Related reference

4.7.9 MAINCLK on page 4-74

2.5 Resets

The reset system on the V2M-Beetle evaluation board provides one reset push button, one shutdown push button, and two reset signals to the Beetle test chip.

The following figure shows the reset system.

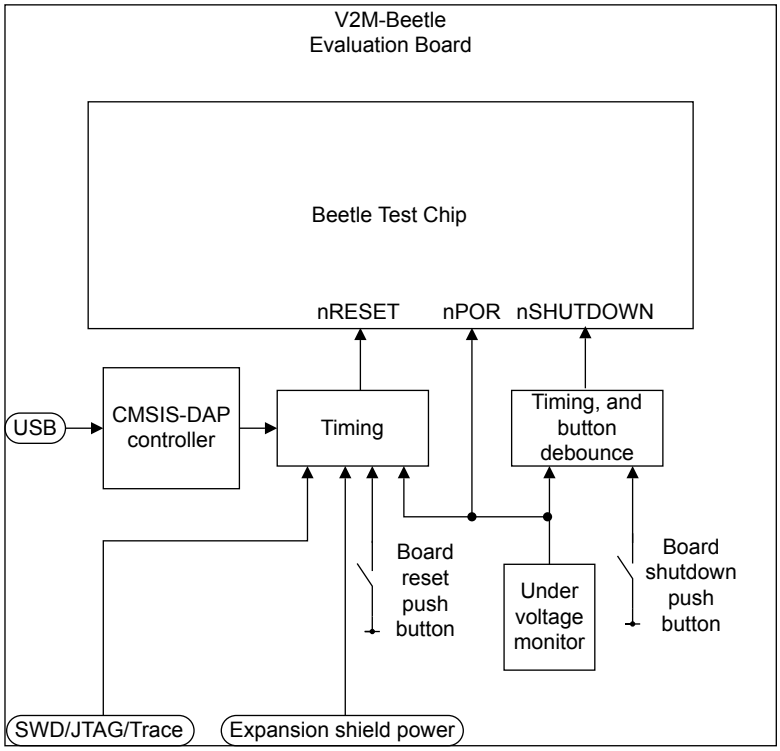

Figure 2-4 V2M-Beetle evaluation board resets

The test chip reset and shutdown signals are:

nPOR

This reset operates during the powerup process when the board voltage rises above 2V7.

nRESET

Performs a hardware reset of the test chip. It has the following sources:

- *RESET* push button.
- CMSIS-DAP reset over USB.
- Reset from external debugger.
- Expansion shield.
- The under-voltage monitor, when the board voltage rises above 2V7 during the powerup process. Timing circuitry synchronizes this signal with **nPOR**.

nSHUTDOWN

Powers down the test chip. It has the following sources:

- Under-voltage monitor, when the board voltage falls below 2V7.
- *SHUTDOWN* push button.

Caution

ARM recommends pressing the *SHUTDOWN* push button before disconnecting the power source to avoid the possibility of damaging the eFlash memory in the test chip.

The following figure shows the powerup and powerdown timing sequences.

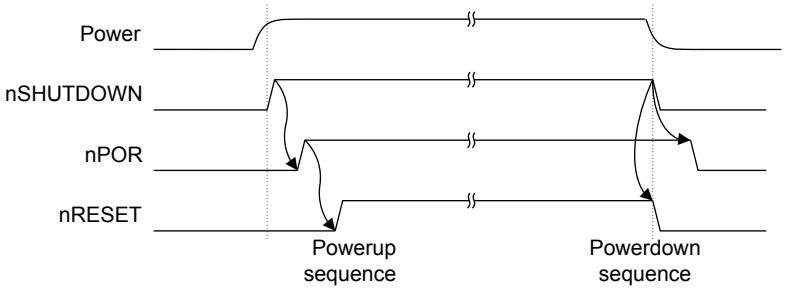

Figure 2-5 Powerup and powerdown timing sequences

The following figure shows the reset sequence where one of the reset sources generates signal **nRESET** to the test chip.

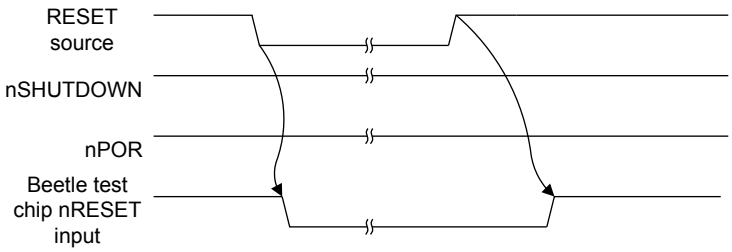

Figure 2-6 Reset sequence

Note

- Signal **RESET source** represents the active reset source generating the reset sequence.
- For resets generated by the *RESET* button, the diagram shows the debounced push button signal.

2.6 USB interface

The V2M-Beetle evaluation board provides one USB port for configuration and debug.

The following figure shows the V2M-Beetle board USB interface.

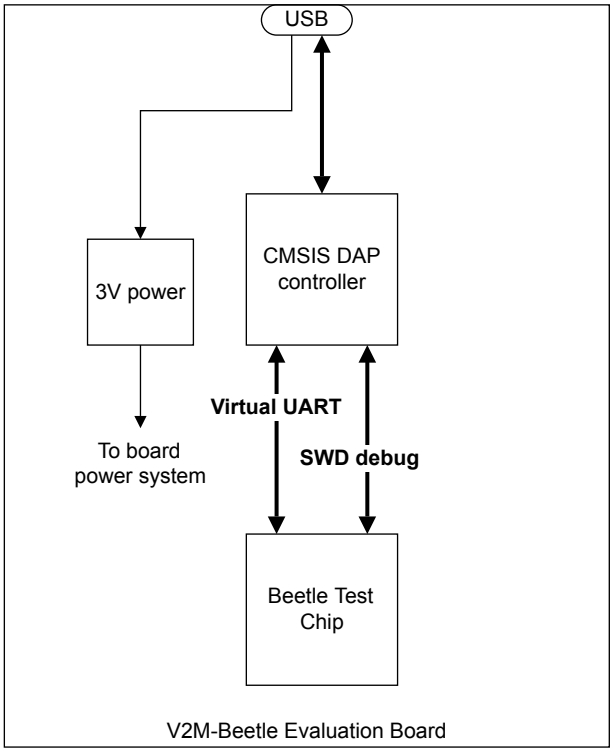

Figure 2-7 USB interface

The USB port enables:

- Virtual UART over USB.
- External 5V power.
- CMSIS-DAP reset and debug.
- Drag-and-drop software image programming.

Updating the CMSIS-DAP image

The following procedure updates the CMSIS-DAP image using a host computer running Microsoft Windows.

1. Remove the USB host cable from the V2M-Beetle board.
2. Press and hold the ISP button while reinserting the USB host cable.
3. The host computer mounts a new drive, labeled *CRP DISABLD*.
4. Drag and drop the CMSIS-DAP binary file onto the new drive.
5. When copying of the new file is complete, remove and then reinsert the USB host cable.

Note

The eFlash in the test chip and QSPI Flash on the V2M-Beetle board require different firmware. See *http://www.arm.com/beetle* for more information.

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14
A.1.3 USB connector on page Appx-A-0

2.7 SPI ADC interface

The V2M-Beetle evaluation board expansion shield AD connector carries six Analog signals to the Analog to Digital Converter (ADC). The ADC digital output connects to the SPI1 interface on the Beetle test chip.

The following figure shows the V2M-Beetle board SPI ADC interface.

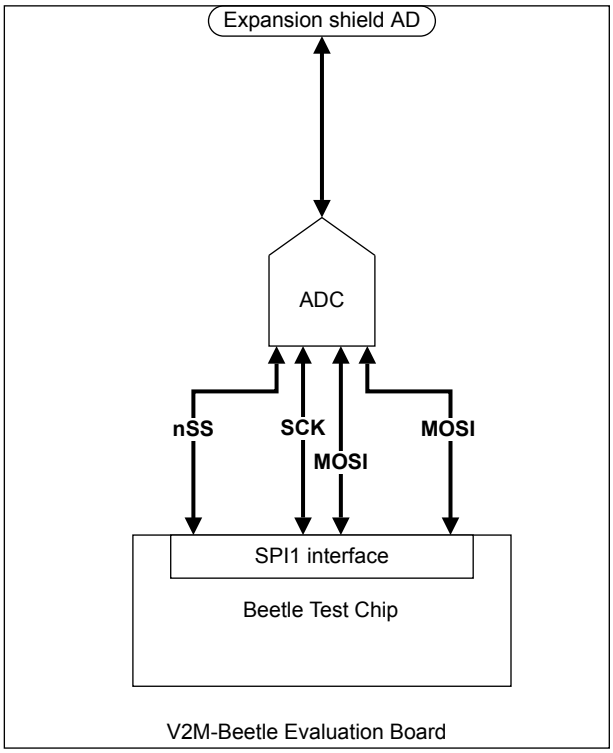

Figure 2-8 SPI ADC interface

The characteristics of the ADC are:

- Part number: Texas Instruments ADC128S052.
- Resolution: 12-bit.
- Sample rate: 200-500 kSPS.
- Input range: 0-5V.
- Type: Successive-Approximation Register (SAR).

Note

The expansion shield must be enabled to enable the ADC. When the expansion shield power supply enable signal, GPIO1[15], is not enabled, that is, set HIGH, the ADC is not available on the SPI1 interface.

Related concepts

2.3 Beetle test chip GPIO interface on page 2-22

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14

Expansion shield IOH connector on page Appx-A-0

2.8 Interrupts

The IoT Compute subsystem controller implements a nested vector interrupt controller.

The following table shows the mapping of the interrupt signals from the test chip.

Table 2-2 Beetle test chip interrupts and their sources on the V2M-Beetle board

Interrupt	Source
NMI	Watchdog
IRQ0	UART0
IRQ1	Reserved
IRQ2	UART1
IRQ3	I2C0
IRQ4	I2C1
IRQ5	RTC
IRQ6	GPIO0 combined interrupt
IRQ7	GPIO1 combined interrupt
IRQ8	Timer 0
IRQ9	Timer 1
IRQ10	Dual-timer
IRQ11	SPI0
IRQ12	UART overflow
IRQ13	SPI1
IRQ14	QSPI
IRQ15	Reserved
IRQ16	GPIO 0/1 pin 0
IRQ17	GPIO 0/1 pin 1
IRQ18	GPIO 0/1 pin 2
IRQ19	GPIO 0/1 pin 3
IRQ20	GPIO 0/1 pin 4
IRQ21	GPIO 0/1 pin 5
IRQ22	GPIO 0/1 pin 6
IRQ23	GPIO 0/1 pin 7
IRQ24	GPIO 0/1 pin 8
IRQ25	GPIO 0/1 pin 9
IRQ26	GPIO 0/1 pin 10
IRQ27	GPIO 0/1 pin 11
IRQ28	GPIO 0/1 pin 12
IRQ29	GPIO 0/1 pin 13
IRQ30	GPIO 0/1 pin 14
IRQ31	GPIO 0/1 pin 15

Table 2-2 Beetle test chip interrupts and their sources on the V2M-Beetle board (continued)

Interrupt	Source
IRQ32	System error (eFlash cache)
IRQ33	eFlash
IRQ34	LLC_TXCMDIRQ (Cordio)
IRQ35	LLC_TXEVTIRQ (Cordio)
IRQ36	LLC_TXDMA0IRQ (Cordio)
IRQ37	LLC_TXDMA1IRQ (Cordio)
IRQ38	LLC_RXCMDIRQ (Cordio)
IRQ39	LLC_RXEVTIRQ (Cordio)
IRQ40	LLC_RXDMA0IRQ (Cordio)
IRQ41	LLC_RXDMA1IRQ (Cordio)
IRQ42	GPIO2 (Cordio)
IRQ43	GPIO3 (Cordio)
IRQ44	True Random Number Generator (TRNG)

See *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* for information on the interrupt controller in the Beetle test chip.

2.9 Cordio® BT4 Bluetooth Low-Energy radio and antenna

The V2M-Beetle evaluation board provides an on-board antenna that connects to the Bluetooth Low-Energy (BLE) RF block in the test chip.

The following figure shows the V2M-Beetle evaluation board Cordio BT4 Bluetooth low energy radio and antenna system.

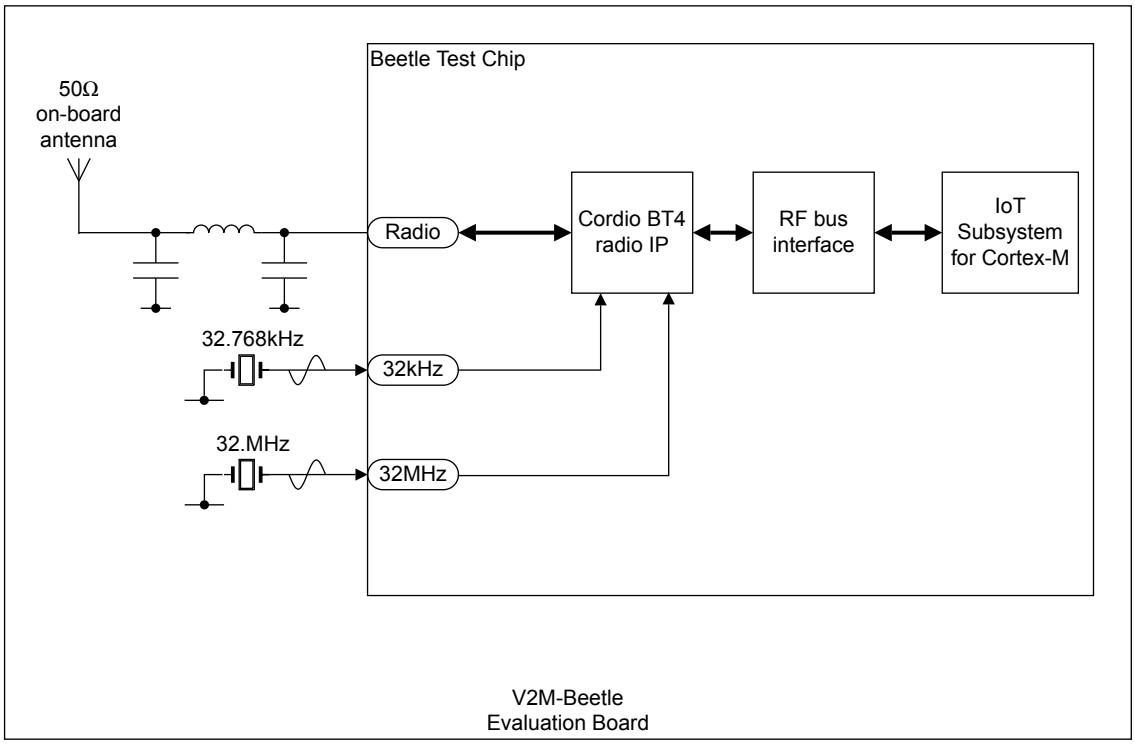

Figure 2-9 Cordio BT4 Bluetooth low energy radio and antenna system

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14

2.10 V2M-Beetle board and expansion shield power

The V2M-Beetle evaluation board has two alternative power sources, an external 5V USB supply, and on-board AAA batteries. A jumper connector on the V2M-Beetle board selects the input voltage for the expansion shield **IOREF** voltage.

V2M-Beetle board power

The following figure shows the V2M-Beetle board power scheme.

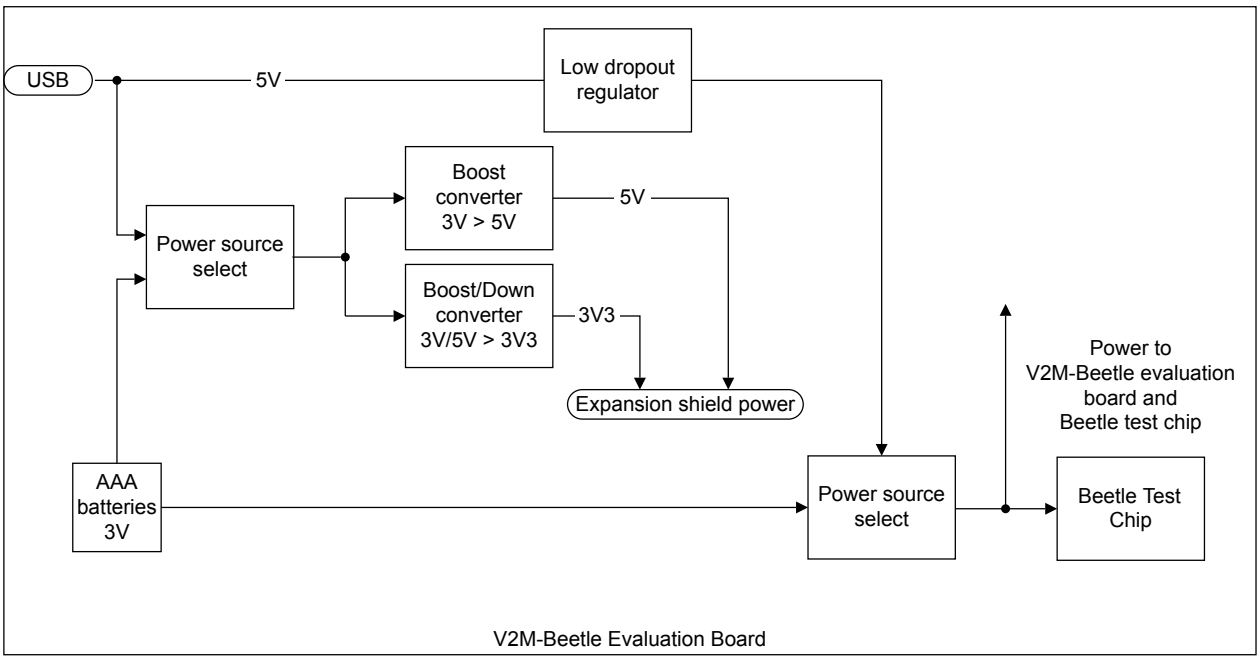

Figure 2-10 Board power scheme

.

USB 5V

When the 5V USB power is connected, the switch automatically selects this power supply and overrides the AAA batteries.

Two AAA batteries (3V)

For use when extended battery operation is required, or if battery operation is required during expansion shield usage. See *1.3 Layout of the V2M-Beetle evaluation board* on page 1-14 for the location of the AAA battery terminals.

Note

The choice of power source determines the possible operating modes of the board. See *3.2 Operating modes* on page 3-42

Selection of expansion shield power supply voltage

The IOREF jumper connector selects either 3V3 or 5V to connect to the **IOREF** pin of the expansion shield power connector. The expansion shield uses this signal to select the appropriate power supply voltage from the V2M-Beetle board. See *1.3 Layout of the V2M-Beetle evaluation board* on page 1-14 for the location of this jumper connector.

The following figure is a close-up of the V2M-Beetle board showing the IOREF select jumper connections.

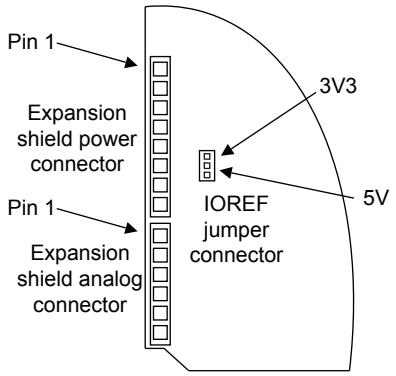

Figure 2-11 Expansion shield IOREF voltage selection

Control of expansion shield power supply

The expansion shield power control jumper controls whether the expansion shield power supply is always on, or under software control. See *1.3 Layout of the V2M-Beetle evaluation board* on page 1-14 for the location of this jumper connector.

The following figure is a close-up of the V2M-Beetle board showing the expansion shield power control jumper connections.

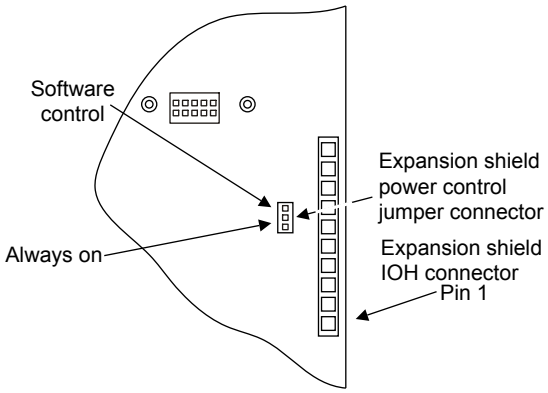

Figure 2-12 Control of expansion shield power supply

Note

Each expansion shield supply, 3V3 and 5V, can supply up to 200mA. The battery life of the board depends on the total amount of current drawn by the test chip and any attached shield. Review the AAA battery datasheet discharge curve data.

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14

2.11 Beetle test chip power management

The test chip provides sleep states of different levels of power consumption to support power management.

This section contains the following subsections:

2.11.1 Active state

The active state is the fully operational mode of the Beetle test chip.

The characteristics of the active state of the test chip are:

- Processor clocks **HCLK** and **FCLK** are on.
- System AHB clock **HCLK** is on.
- Peripheral clock (APB) operates during transfers.

System control registers configure the peripheral clocks in the active state.

AHBCLKCFG0SET
This register enables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

AHBCLKCFG0CLR
This register disables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

APBCLKCFG0SET
This register enables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors, and to components on the V2M-Beetle evaluation board.

APBCLKCFG0CLR
This register disables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors and, to components on the V2M-Beetle evaluation board.

2.11.2 Sleep state

The sleep state is one of the states that provides power-saving in the Beetle test chip.

The characteristics of the sleep state of the test chip are:

- Processor clock **FCLK** is on.
- Processor clock **HCLK** is off.
- System bus clock **HCLK** is off except when the Cordio BT4 Bluetooth RF block requests transfers.
- Peripheral clock (APB) operates during transfers.

System control registers configure the peripheral clocks in the sleep state:

AHBCLKCFG1SET
This register enables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

AHBCLKCFG1CLR
This register disables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

APBCLKCFG1SET
This register enables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors, and to components on the V2M-Beetle evaluation board.

APBCLKCFG1CLR
This register disables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors and, to components on the V2M-Beetle evaluation board.

2.11.3 Deep sleep state

The deep sleep state is one of the states that provides power-saving in the Beetle test chip.

System control register SLEEPCFG configures the deep sleep state of the test chip. The characteristics of the deep sleep state are:

- Processor clocks **FCLK** and **HCLK** are both off.
- System bus clock **HCLK** is off except when the Cordio BT4 Bluetooth RF block requests transfers.
- SRAM can be put into state retention mode.

System control registers configure the deep sleep state:

MAINCLK
This register can enable the main clocks, **FCLK** and **HCLK**, in the deep sleep state.

SLEEPCFG
This register controls power modes, retention modes, and other settings for eFlash, eFlash cache SRAM, SRAM, and Cordio.

AHBCLKCFG2SET
This register enables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

AHBCLKCFG2CLR
This register disables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

APBCLKCFG2SET
This register enables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors, and to components on the V2M-Beetle evaluation board.

APBCLKCFG2CLR
This register disables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors and, to components on the V2M-Beetle evaluation board.

2.11.4 Powerdown sleep state

The powerdown sleep state provides the maximum available power-saving in the Beetle test chip.

The characteristics of the deep sleep state are:

- Processor clocks **FCLK** and **HCLK** are both off.
- System bus clock **HCLK** is off except when the Cordio Bluetooth RF block requests transfers.
- SRAM is powered down. It can be put into state retention mode.
- Peripherals, except GPIO, can be powered or powered down. If not powered down, the peripherals retain their state during test chip powerdown sleep state.
- Debug not operational.
- Wake up with interrupts or reset.

System control registers configure the powerdown sleep state:

AHBCLKCFG2SET
This register enables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

AHBCLKCFG2CLR
This register disables AHB peripheral clocks **FCLK** and **HCLK** to GPIO1 and GPIO0 interfaces that connect to the expansion shield IOH and IOL connectors.

APBCLKCFG2SET

This register enables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors, and to components on the V2M-Beetle evaluation board.

APBCLKCFG2CLR

This register disables the APB peripheral clocks that connect to the expansion shield IOH and IOL connectors and, to components on the V2M-Beetle evaluation board.

2.12 Board peripherals

The V2M-Beetle evaluation board provides a motion sensor, and temperature sensor, to enable simple demonstration applications without the need for an expansion shield.

The following figure shows the board peripherals, the motion sensor, and the temperature sensor, that connect to the I2C interface, *I2C1*, in the Beetle test chip.

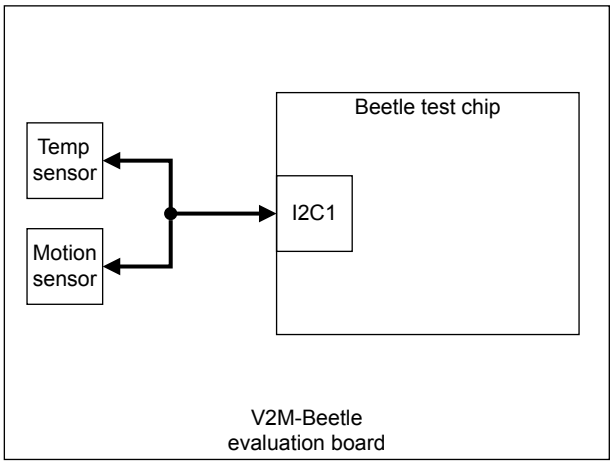

Figure 2-13 V2M-Beetle evaluation board peripherals

Motion sensor

- MMA7660FC 3-axis orientation and motion sensor.
- Slave address: `0x90`

Temperature sensor

- TMP102 temperature sensor.
- Slave address: `0x98`

Data signals, **SDA** from the motion sensor, and **SDA** from the temperature sensor, connect to **I2C1 Data**, that is, **GPIO1[6]**.

Clock signals, **SCL** from the motion sensor, and **SCL** from the temperature sensor, connect to **I2C1 Clock**, that is, **GPIO1[7]**.

Interrupt signals, **nINT** from the motion sensor, and **nALERT** from the temperature sensor, connect to **I2C1 Interrupt**, that is, **GPIO1[8]**.

2.13 Debug and trace

The V2M-Beetle evaluation board provides debug and trace access to the Beetle test chip.

The following figure shows the V2M-Beetle board debug and trace system.

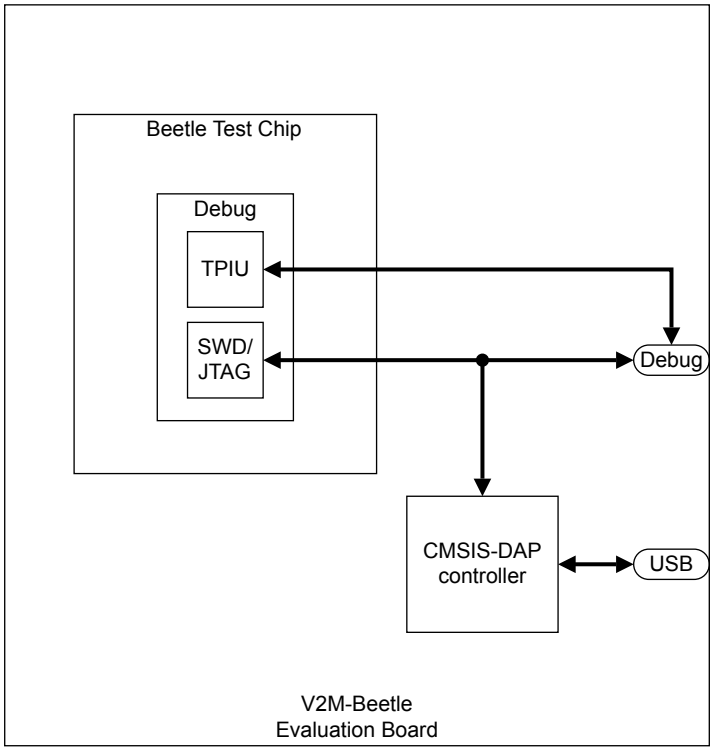

Figure 2-14 V2M-Beetle evaluation board debug and trace system

The V2M-Beetle board provides:

- SWD debug with external hardware debugger such as ULINK2™.
- 4-bit trace using an external debugger, such as ULINKpro™
- P-JTAG debug.
- CMSIS-DAP debug over USB.

Caution

The external USB 5V supply must be connected for CMSIS-DAP debug over USB. Do not attempt to wake up the CMSIS-DAP controller without the external USB 5V supply being connected because the batteries cannot supply enough current.

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14

A.1.4 CoreSight™ 20 debug connector on page Appx-A-0

A.1.5 CoreSight™ 10 debug connector on page Appx-A-0

Chapter 3
Board Configuration and operating modes

This chapter describes board configuration during powerup, loading boot code and test chip programming, CMSIS-DAP programming, and board operating modes.

It contains the following sections:

3.1 Board configuration and programming

Configuration of the V2M-Beetle evaluation board proceeds automatically when power is applied to the board.

Overview of V2M-Beetle board configuration and programming

The following figure shows the configuration system.

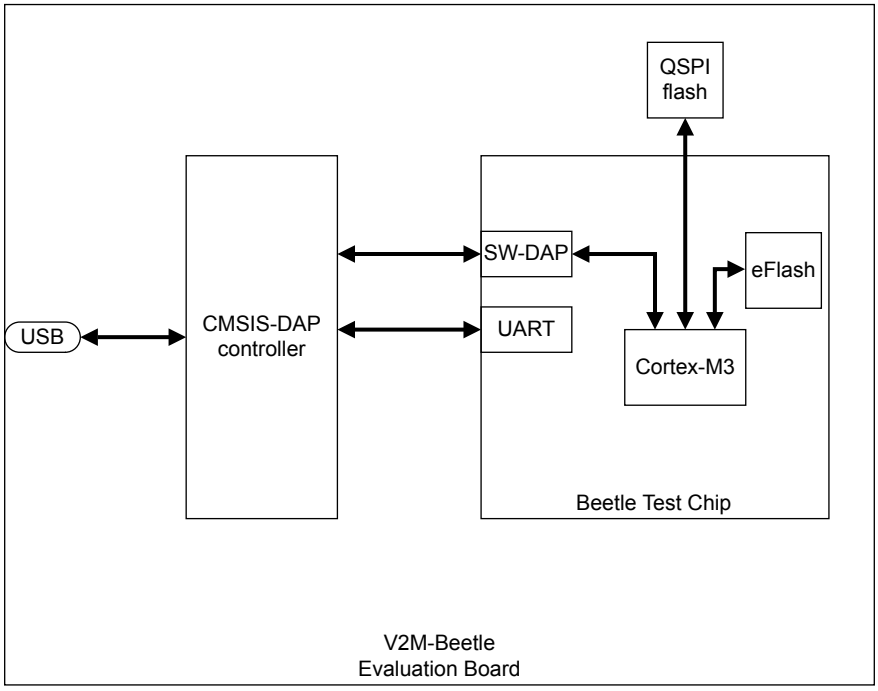

Figure 3-1 V2M-Beetle evaluation board configuration system

The USB port and CMSIS-DAP controller enables drag-and-drop loading of Cortex-M3 boot code and software images. The Cortex-M3 can boot and run code from two possible sources:

- eFlash in the Beetle test chip:
  - eFlash is the default boot option.
- External QSPI flash on the V2M-Beetle board:
  - The external QSPI flash is the alternative boot option.

3.2 Operating modes

The V2M-Beetle evaluation board has three operating modes.

Board operating modes

The power source that you select for the V2M-Beetle evaluation board defines the operating mode of the board. The operating modes of the V2M-Beetle evaluation board are:

***Always on* mode**

- Operates when the external 5V USB power source is connected.
- The V2M-Beetle board and Beetle test chip are fully operational.
- Expansion shield support and virtual UART are available.
- The CMSIS-DAP controller is in operational mode. USB debug is available.
- If AAA batteries are fitted, the external 5V USB power source automatically overrides them.

***Battery Shield* mode**

- Operates from the 2×AAA batteries (3V).
- The V2M-Beetle board and Beetle test chip are fully operational.
- Expansion shield support is available.
- The CMSIS-DAP controller is automatically put into *Deep Powerdown* mode. USB debug and USB virtual UART are not available because the external USB 5V power is not connected.

***Long Duration* mode**

- Operates from 2×AAA batteries (3V).
- The V2M-Beetle board and Beetle test chip are fully operational.
- Expansion shield support is not available.
- The CMSIS-DAP controller is automatically put into *Deep Powerdown* mode. USB debug and USB virtual UART are not available because the external USB 5V power is not connected.

——— **Note** ———

The external 5V USB power source must not be connected in *Battery Shield* and *Long Duration* modes, otherwise it overrides the AAA batteries.

———————————

Transitions between V2M-Beetle evaluation board and CMSIS-DAP controller operating modes

Applying power

1. Apply power by either:
   - Fitting 2×AAA batteries:
     - The board powers up in either *Battery Shield* mode or *Long Duration* mode.
     - The CMSIS-DAP automatically goes into *Deep Powerdown* mode to save power:
       - All CMSIS-DAP I/O are set to their default states.
       - CMSIS-DAP internal clocks are turned off except the low- frequency RC clock.
     - USB debug is unavailable.
   - Connecting a USB host cable to the USB port:
     - The board powers up in *Always on* mode.
     - The CMSIS-DAP controller automatically goes into *Operational* mode.
     - USB debug is available.

Bringing CMSIS-DAP controller out of *Deep Powerdown* mode

When the board is in *Battery Shield* or *Long Duration* mode, connecting a USB host cable to the USB port:

- Brings the board to *Always on* mode.
- Wakes up the CMSIS-DAP controller, that is, brings it from *Deep Powerdown* mode to *operational* mode.
- Makes USB debug available.

Transition from *Always on* mode to *Battery Shield* or *Long Duration* mode

When the board is in *Always on* mode:

1. Remove the USB host cable. The CMSIS-DAP controller is still operational but USB debug is unavailable.

   Caution

   - If the batteries are fitted, do not leave the board in this state. Because the USB host cable is absent, USB debug is unavailable. However, the CMSIS-DAP controller remains in *Operational* mode and draws battery current which is wasted.

2. Depending on whether batteries are present or not present:
   - If batteries are not present, fit 2×AAA batteries.
   - If batteries are present, remove and then refit the AAA batteries.
3. The board powers up in either *Battery Shield* or *Long Duration* mode.

Powering down the board

1. Briefly press the board *SHUTDOWN* push button.
2. Remove all power from the board, that is, both the 5V USB power source and the 2×AAA batteries.

Chapter 4
Programmers Model

This chapter describes the programmers model of the V2M-Beetle evaluation board.

It contains the following sections:

4.1 About this programmers model

The following information applies to the registers in the test chip.

- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or powerup reset.
  - *4.7.1 System control register summary* on page 4-63 describes register access type as follows:

    RW Read and write.

    RO Read-only.

    WO Write-only.

4.2 Memory map

The Cortex-M3 in the test chip sees a 32-bit memory map.

The following figure shows the memory map.

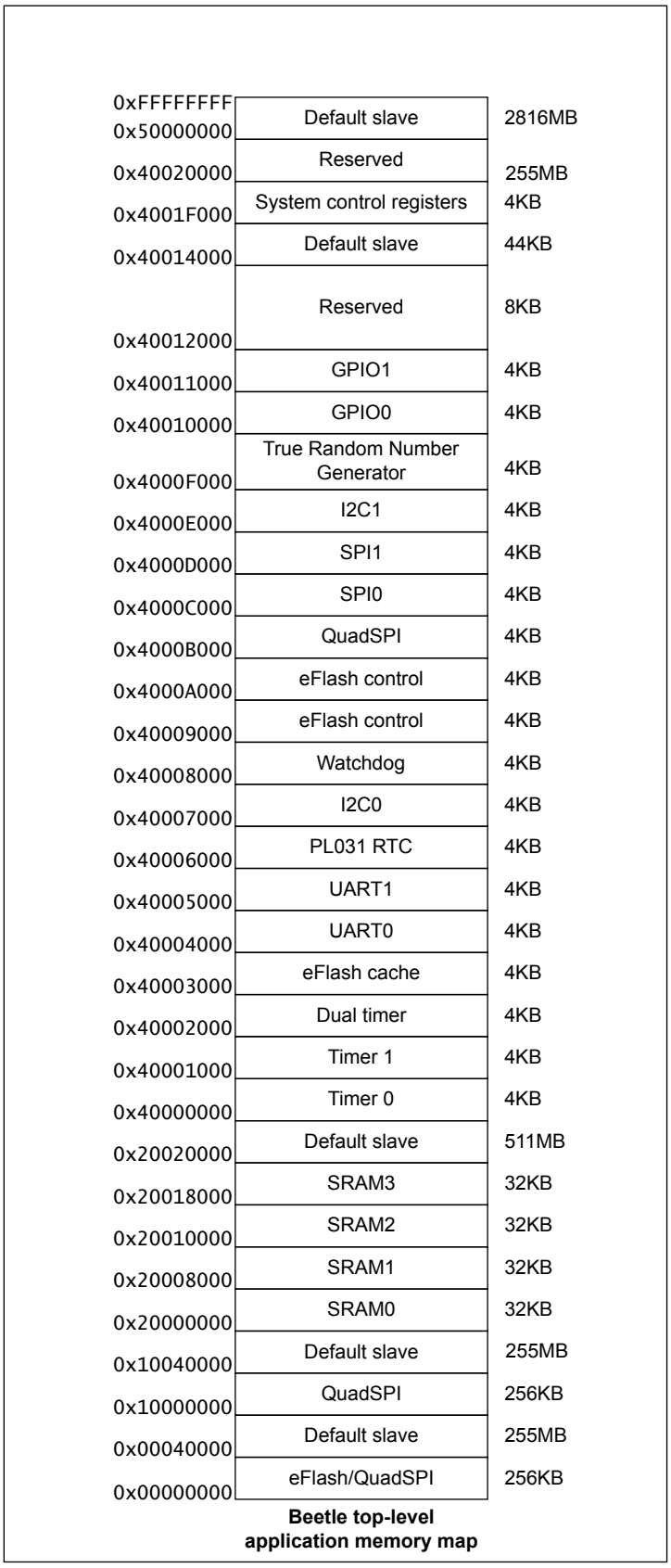

Figure 4-1 Beetle test chip memory map

The following table shows the memory map.

Table 4-1 Beetle test chip memory map

Address range	Size	Description:
0x00000000-0x0003FFFF	256KB	eFlash/QuadSPI (Cadence Flash QSPI Controller IP6514E).
0x00040000-0x0FFFFFFF	255MB	Default slave.
0x10000000-0x1003FFFF	256MB	QuadSPI (Cadence Flash QSPI Controller IP6514E).
0x10040000-0x1FFFFFFF	255MB	Default slave.
0x20000000-0x20007FFF	32KB	SRAM0.
0x20008000-0x2000FFFF	32KB	SRAM1.
0x20010000-0x20017FFF	32KB	SRAM2.
0x20018000-0x2001FFFF	32KB	SRAM3.
0x20020000-0x3FFFFFFF	511MB	Default slave.
0x40000000-0x40000FFF	4KB	Timer 0.
0x40001000-0x40001FFF	4KB	Timer 1.
0x40002000-0x40002FFF	4KB	Dual timer.
0x40003000-0x40003FFF	4KB	eFlash cache.
0x40004000-0x40004FFF	4KB	UART0.
0x40005000-0x40005FFF	4KB	UART1.
0x40006000-0x40006FFF	4KB	PL031 RTC.
0x40007000-0x40007FFF	4KB	I2C0 (Cadence 1^2C Controller IP6510).
0x40008000-0x40008FFF	4KB	Watchdog.
0x40009000-0x40009FFF	4KB	eFlash controller.
0x4000A000-0x4000AFFF	4KB	eFlash controller.
0x4000B000-0x4000BFFF	4KB	QuadSPI (Cadence Flash QSPI Controller IP6514E).
0x4000C000-0x4000CFFF	4KB	SPI0 (Cadence Peripheral Interface IP6524).
0x4000D000-0x4000DFFF	4KB	SPI1 (Cadence Peripheral Interface IP6524).
0x4000E000-0x4000EFFF	4KB	I2C1 (Cadence 1^2C Controller IP6510).
0x4000F000-0x4000FFFF	4KB	True Random Number Generator (TRNG).
0x40010000-0x40010FFF	4KB	GPIO0.
0x40011000-0x40011FFF	4KB	GPIO1.
0x40012000-0x40013FFF	8KB	Reserved. Do not write or read from these addresses.
0x40014000-0x4001EFFF	44KB	Default slave.
0x4001F000-0x4001FFFF	4KB	System control registers.
0x40020000-0x4FFFFFFF	255MB	Reserved. Do not write to or read from these addresses.
0x50000000-0xFFFFFFFF	2816MB	Default slave.

The TESTMODE [0] jumper connector on the board controls the remap function at `0x00000000`:

- No jumper:
  — eFlash.
- Jumper:
  — QSPI.

Note

- When the remap option at `0x00000000` is set to eFlash, QSPI remains available at `0x10000000`.
- See *1.3 Layout of the V2M-Beetle evaluation board* on page 1-14 for the location of the TESTMODE [0] jumper connector on the V2M-Beetle board.

See the *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* for more information about the Beetle test chip memory map.

Contact your local Cadence representative for information about the I^2C, SPI, and QSPI IP blocks.

Related reference

1.3 Layout of the V2M-Beetle evaluation board on page 1-14

4.3 Dual timer registers

The Beetle test chip contains registers that control the functions of the dual timers. The base memory address of the dual timers control registers is `0x40002000`.

Undefined registers are reserved. Software must not attempt to write to or read from these registers.

See the *Dual-input timers* section of the *Cortex-M™ System Design Kit Technical Reference Manual* for descriptions of these registers.

The following table shows the dual timer control registers in the test chip in address offset order from the base memory address.

Table 4-2 Beetle test chip dual timers control registers summary

Offset	Name	Type	Reset	Width	Function
`0x0000`	DTIMER1LOAD	RW	`0x00000000`	32	Dual Timer 1 load register.
`0x0004`	DTIMER1VALUE	RO	`0xFFFFFFFF`	32	Dual Timer 1 current value register.
`0x0008`	DTIMER1CONTROL	RW	`0x00000020`	32	Dual Timer 1 control register. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x000C`	DTIMER1INTCLR	WO	-	32	Dual Timer 1 interrupt clear register.
`0x0010`	DTIMER1RIS	RO	`0x00000000`	32	Dual Timer 1 raw interrupt status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.
`0x0014`	DTIMER1MIS	RO	`0x00000000`	32	Dual Timer 1 interrupt status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.
`0x0018`	DTIMER1BGLOAD	RW	`0x00000000`	32	Dual Timer 1 background load register.
`0x0020`	DTIMER2LOAD	RW	`0x00000000`	32	Dual timer 2 load register.
`0x0024`	DTIMER2VALUE	RO	`0xFFFFFFFF`	32	Dual timer 2 current value register.
`0x0028`	DTIMER2CONTROL	RW	`0x00000020`	32	Dual timer 2 control register. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x002C`	DTIMER2INTCLR	WO	-	32	Dual timer 2 interrupt clear register.
`0x0030`	DTIMER2RIS	RO	`0x00000000`	32	Dual timer 2 raw interrupt status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.
`0x0034`	DTIMER2MIS	RO	`0x00000000`	32	Dual timer 2 interrupt status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.

Table 4-2 Beetle test chip dual timers control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x0038	DTIMER2BGLOAD	RW	0x00000000	32	Dual timer 2 background load register.
0x0F00	DTIMERITCR	RW	0x00000000	32	Integration test control register.
0x0F04	DTIMERITOP	WO	0x00000000	32	Integration test output set register. Bits [31:2] are reserved. Software that writes to this register must write all zeros to these bits.
0x0FD0	DTIMERPERIPHID4	RO	0x00000004	32	Peripheral ID Register 4. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FE0	DTIMERPERIPHID0	RO	0x00000023	32	Peripheral ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FE4	DTIMERPERIPHID1	RO	0x000000B8	32	Peripheral ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FE8	DTIMERPERIPHID2	RO	0x0000000B	32	Peripheral ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FEC	DTIMERPERIPHID3	RO	0x00000000	32	Peripheral ID Register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF0	DTIMERPCELLID0	RO	0x0000000D	32	Component ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF4	DTIMERPCELLID1	RO	0x000000F0	32	Component ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF8	DTIMERPCELLID2	RO	0x00000005	32	Component ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FFC	DTIMERPCELLID3	RO	0x000000B1	32	Component ID Register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.

4.4 UART registers

The Beetle test chip contains registers that control the functions of the two UARTs, UART0 and UART1. The base memory address of the UART control registers is `0x40004000`.

Undefined registers are reserved. Software must not attempt to write to or read from these registers.

See the *UART* section of the *Cortex-M™ System Design Kit Technical Reference Manual* for full descriptions of these registers.

The following table shows the UART control registers in the test chip in address offset order from the base memory address.

Table 4-3 UART control registers summary

Offset	Name	Type	Reset	Width	Function
`0x0000`	UART0_DATA	RW	-	32	UART0 data value register.
`0x0004`	UART0_STATE	RW	`0x00000000`	32	UART0 state register. Bits [31:4] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0008`	UART0_CTRL	RW	`0x00000000`	32	UART0 control register. Bits [31:7] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x000C`	UART0_INTSTATUS UART0_INTCLEAR	RW	`0x00000000`	32	UART0 interrupt status and clear register. Bits [31:4] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0010`	UART0_BAUDDIV	RW	`0x00000000`	32	UART0 baud rate divisor register. Bits [31:20] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0FD0`	UART0_PID4	RO	`0x00000004`	32	UART0 peripheral ID Register 4. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
`0x0FE0`	UART0_PID0	RO	`0x00000021`	32	UART0 peripheral ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
`0x0FE4`	UART0_PID1	RO	`0x000000B8`	32	UART0 peripheral ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.

Table 4-3 UART control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x0FE8	UART0_PID2	RO	0x0000000B	32	UART0 peripheral ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FEC	UART0_PID3	RO	0x00000000	32	UART0 peripheral ID3 register. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF0	UART0_CID0	RO	0x0000000D	32	UART0 component ID0 register. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF4	UART0_CID1	RO	0x000000F0	32	UART0 component ID1 register. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF8	UART0_CID2	RO	0x00000005	32	UART0 component ID2 register. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FFC	UART0_CID3	RO	0x000000B1	32	UART0 component ID3 register. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1000	UART1_DATA	RW	-	32	UART1 data value register.
0x1004	UART1_STATE	RW	0x00000000	32	UART1 state register. Bits [31:4] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1008	UART1_CTRL	RW	0x00000000	32	UART1 control register. Bits [31:7] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x100C	UART1_INTSTATUS UART1_INTCLEAR	RW	0x00000000	32	UART1 interrupt status and clear register. Bits [31:4] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1010	UART1_BAUDDIV	RW	0x00000000	32	UART1 baud rate divisor register. Bits [31:20] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-3 UART control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x1FD0	UART1_PID4	RO	0x00000004	32	UART1 peripheral ID Register 4. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FE0	UART1_PID0	RO	0x00000021	32	UART1 peripheral ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FE4	UART1_PID1	RO	0x000000B8	32	UART1 peripheral ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FE8	UART1_PID2	RO	0x0000000B	32	UART1 peripheral ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FEC	UART1_PID3	RO	0x00000000	32	UART1 peripheral ID Register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FF0	UART1_CID0	RO	0x0000000D	32	UART1 component ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FF4	UART1_CID1	RO	0x000000F0	32	UART1 component ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FF8	UART1_CID2	RO	0x00000005	32	UART1 component ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x1FFC	UART1_CID3	RO	0x000000B1	32	UART1 component ID Register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.

4.5 Watchdog registers

The Beetle test chip contains registers that control the functions of the watchdog module. The base memory address of the watchdog registers is `0x40008000`.

Undefined registers are reserved. Software must not attempt to write to or read from these registers.

See the *Watchdog* section of the *Cortex-M™ System Design Kit Technical Reference Manual* for descriptions of these registers.

The following table shows the watchdog module control registers in the test chip in address offset order from the base memory address.

Table 4-4 Watchdog control registers summary

Offset	Name	Type	Reset	Width	Function
`0x0000`	WDOGLOAD	RW	`0xFFFFFFFF`	32	Watchdog load register.
`0x0004`	WDOGVALUE	RO	`0xFFFFFFFF`	32	Current value of watchdog counter register.
`0x0008`	WDOGCONTROL	RW	`0x00000000`	8	Timer 1 control register. Bits [31:2] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x000C`	WDOGINTCLR	WO	-	32	Watchdog interrupt clear register.
`0x0010`	WDOGRIS	RO	`0x00000000`	1	Watchdog interrupt status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.
`0x0014`	WDOGMIS	RO	`0x00000000`	1	Watchdog status register. Bits [31:1] are reserved. Software that reads these bits must ignore these bits.
`0x0C00`	WDOGLOCK	RW	`0x00000000`	32	Watchdog lock register.
`0x0F00`	WDOGITCR	RW	`0x00000000`	32	Watchdog integration test control register. Bits [31:1] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0F04`	WDOGITOP	WO	`0x00000000`	32	Watchdog integration test output set register.
`0x0FD0`	WDOGPERIPHID4	RO	`0x00000004`	8	Peripheral ID register 4. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
`0x0FE0`	WDOGPERIPHID0	RO	`0x00000024`	32	Peripheral ID register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.

Table 4-4 Watchdog control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x0FE4	WDOGPERIPHID1	RO	0x000000B8	1	Peripheral ID register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FE8	WDOGPERIPHID2	RO	0x0000000B	1	Peripheral ID register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FEC	WDOGPERIPHID3	RO	0x00000000	32	Peripheral ID register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF0	WDOGPCELLID0	RO	0x0000000D	8	Component ID Register 0. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF4	WDOGCELLID1	RO	0x000000F0	8	Component ID Register 1. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FF8	WDOGPCELLID2	RO	0x00000005	8	Component ID Register 2. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.
0x0FFC	WDOGPCELLID3	RO	0x000000B1	8	Component ID Register 3. Bits [31:8] are reserved. Software that reads these bits must ignore these bits.

4.6 GPIO registers

The Beetle test chip contains registers that control the functions of the GPIO pins. The base memory address of the GPIO control registers is `0x40010000`.

Undefined registers are reserved. You must not attempt to write to or read from these registers.

See the *AHB GPIO* section of the *Cortex-M™ System Design Kit Technical Reference Manual* for descriptions of these registers.

Note

Prefixes GPIO0 and GPIO1 are added to the register names to distinguish between the GPIO0 and GPIO1 interfaces on the test chip.

The following table shows the GPIO control registers in the test chip in address offset order from the base memory address.

Table 4-5 GPIO control registers summary

Offset	Name	Type	Reset	Width	Function
`0x0000`	GPIO0DATA	RW	`0x00000000`	32	Data value. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0004`	GPIO0DATAOUT	RW	`0x00000000`	32	Data output value. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0010`	GPIO0OUTENSET	RW	`0x00000000`	32	Output enable set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0014`	GPIO0OUTENCLR	RW	`0x00000000`	32	Output enable clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x0018`	GPIO0ALTFUNCSET	RW	`0x00000000`	32	Alternative function set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
`0x001C`	GPIO0ALTFUNCCLR	RW	`0x00000000`	32	Alternative function clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-5 GPIO control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x0020	GPIO0INTENSET	RW	0x00000000	32	Interrupt enable set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0024	GPIO0INTENCLR	RW	0x00000000	32	Interrupt enable clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0028	GPIO0INTTYPESET	RW	0x00000000	32	Interrupt type set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x002C	GPIO0INTTYPECLR	RW	0x00000000	32	Interrupt type clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0030	GPIO0INTPOLSET	RW	0x00000000	32	Polarity-level, edge IRQ configuration. Set interrupt polarity bit. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0034	GPIO0INTPOLCLR	RW	0x00000000	32	Polarity-level, edge IRQ configuration. Clear interrupt polarity bit. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0038	GPIO0INTSTATUS INTCLEAR	RW	0x00000000	32	Clear interrupt request. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FD0	GPIO0PID4	RW	0x00000000	32	Peripheral ID Register 4. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-5 GPIO control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x0FE0	GPIO0PID0	RW	0x00000000	32	Peripheral ID Register 0. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FE4	GPIO0PID1	RW	0x00000000	32	Peripheral ID Register 1. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FE8	GPIO0PID2	RW	0x00000000	32	Peripheral ID Register 2. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FEC	GPIO0PID3	RW	0x00000000	32	Peripheral ID Register 3. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FF0	GPIO0CID0	RW	0x00000000	32	Component ID Register 0. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FF4	GPIO0CID1	RW	0x00000000	32	Component ID Register 1. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FF8	GPIO0CID2	RW	0x00000000	32	Component ID Register 2. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x0FFC	GPIO0CID3	RW	0x00000000	32	Component ID Register 3. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1000	GPIO1DATA	RW	0x00000000	32	Data value. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-5 GPIO control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x1004	GPIO1DATAOUT	RW	0x00000000	32	Data output value. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1010	GPIO1OUTENSET	RW	0x00000000	32	Output enable set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1014	GPIO1OUTENCLR	RW	0x00000000	32	Output enable clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1018	GPIO1ALTFUNCSET	RW	0x00000000	32	Alternative function set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x101C	GPIO1ALTFUNCCLR	RW	0x00000000	32	Alternative function clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1020	GPIO1INTENSET	RW	0x00000000	32	Interrupt enable set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1024	GPIO1INTENCLR	RW	0x00000000	32	Interrupt enable clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1028	GPIO1INTTYPESET	RW	0x00000000	32	Interrupt type set. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x102C	GPIO1INTTYPECLR	RW	0x00000000	32	Interrupt type clear. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-5 GPIO control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x1030	GPIO1INTPOLSET	RW	0x00000000	32	Polarity-level, edge IRQ configuration. Set interrupt polarity bit. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1034	GPIO1INTPOLCLR	RW	0x00000000	32	Polarity-level, edge IRQ configuration. Clear interrupt polarity bit. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1038	GPIO1INTSTATUS INTCLEAR	RW	0x00000000	32	Clear interrupt request. Bits [31:16] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FD0	GPIO1PID4	RO	0x00000000	32	Peripheral ID Register 4. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FE0	GPIO1PID0	RO	0x00000000	32	Peripheral ID Register 0. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FE4	GPIO1PID1	RO	0x00000000	32	Peripheral ID Register 1. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FE8	GPIO1PID2	RO	0x00000000	32	Peripheral ID Register 2. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FEC	GPIO1PID3	RO	0x00000000	32	Peripheral ID Register 3. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-5 GPIO control registers summary (continued)

Offset	Name	Type	Reset	Width	Function
0x1FF0	GPIO1CID0	RO	0x00000000	32	Component ID Register 0. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FF4	GPIO1CID1	RO	0x00000000	32	Component ID Register 1. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FF8	GPIO1CID2	RO	0x00000000	32	Component ID Register 2. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
0x1FFC	GPIO1CID3	RO	0x00000000	32	Component ID Register 3. Bits [31:8] are reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Related concepts

2.3 Beetle test chip GPIO interface on page 2-22

Related reference

Expansion shield IOL connector on page Appx-A-0

Expansion shield IOH connector on page Appx-A-0

4.7 System controller registers

The Beetle test chip contains the system control registers.

This section contains the following subsections:

4.7.1 System control register summary

The base memory address of the system control registers is `0x4001F000`.

Undefined registers are reserved. You must not attempt to write to or read from these registers.

See *ARM® IoT Subsystem for Cortex-M® Technical Reference Manual* for information about other registers that control systems in the IoT Compute subsystem.

The following table shows the system control registers in address offset order from the base memory address.

Table 4-6 V2M-Beetle evaluation board APB system registers summary

Offset	Name	Type	Reset	Width	Description
0x0004	CMSDKPMUCTRL	RO	0x00000001	32	See *4.7.2 PMUCTRL* on page 4-65.
0x0008	RESETOP	RW	0x00000000	32	See *4.7.3 RESETOP* on page 4-66.
0x0010	RSTINFO	W1C	0x00000000	32	See *4.7.4 RSTINFO* on page 4-67.
0x0020	AHBPER0SET	RW	0x00000000	32	See *4.7.5 AHBPER0SET* on page 4-68.
0x0024	AHBPER0CLR	RW	0x00000000	32	See *4.7.6 AHBPER0CLR* on page 4-69
0x0030	APBPER0SET	RW	0x00008608	32	See *4.7.7 APBPER0SET* on page 4-70.
0x0034	APBPER0CLR	RW	0x00000000	32	See *4.7.8 APBPER0CLR* on page 4-72.
0x0040	MAINCLK	RW	0x00000000	32	See *4.7.9 MAINCLK* on page 4-74.
0x0044	AUXCLK	RW	0x00000080	32	See *4.7.10 AUXCLK* on page 4-75.
0x0080	AHBCLKCFG0SET	RW	0x00000000	32	See *4.7.11 AHBCLKCFG0SET* on page 4-76.
0x0084	AHBCLKCFG0CLR	RW	0x00000000	32	See *4.7.12 AHBCLKCFG0CLR* on page 4-77.
0x0088	AHBCLKCFG1SET	RW	0x00000000	32	See *4.7.13 AHBCLKCFG1SET* on page 4-78.
0x008C	AHBCLKCFG1CLR	RW	0x00000000	32	See *4.7.14 AHBCLKCFG1CLR* on page 4-79.
0x0090	AHBCLKCFG2SET	RW	0x00000000	32	See *4.7.15 AHBCLKCFG2SET* on page 4-80.
0x0094	AHBCLKCFG2CLR	RW	0x00000000	32	See *4.7.16 AHBCLKCFG2CLR* on page 4-81.
0x00A0	APBCLKCFG0SET	RW	0x00000000	32	See *4.7.17 APBCLKCFG0SET* on page 4-82.
0x00A4	APBCLKCFG0CLR	RW	0x00000000	32	See *4.7.18 APBCLKCFG0CLR* on page 4-84.
0x00A8	APBCLKCFG1SET	RW	0x00000000	32	See *4.7.19 APBCLKCFG1SET* on page 4-86
0x00AC	APBCLKCFG1CLR	RW	0x00000000	32	See *4.7.20 APBCLKCFG1CLR* on page 4-88.

Table 4-6 V2M-Beetle evaluation board APB system registers summary (continued)

Offset	Name	Type	Reset	Width	Description
0x00B0	APBCLKCFG2SET	RW	0x00000000	32	See *4.7.21 APBCLKCFG2SET* on page 4-91.
0x00B4	APBCLKCFG2CLR	RW	0x00000000	32	See *4.7.22 APBCLKCFG2CLR* on page 4-93.
0x00C0	AHBPRST0SET	RW	0x00000000	32	See *4.7.23 AHBPRST0SET* on page 4-95.
0x00C4	AHBPRST0CLR	RW	0x00000000	32	See *4.7.24 AHBPRST0CLR* on page 4-96.
0x00C8	APBPRST0SET	RW	0x00000600	32	See *4.7.25 APBPRST0SET* on page 4-97.
0x00CC	APBPRST0CLR	RW	0x00000000	32	See *4.7.26 APBPRST0CLR* on page 4-99.
0x00D0	PWRDNCFG0SET	RW	0x00000000	32	See *4.7.27 PWRDNCFG0SET* on page 4-101.
0x00D4	PWRDNCFG0CLR	RW	0x00000000	32	See *4.7.28 PWRDNCFG0CLR* on page 4-102.
0x00D8	PWRDNCFG1SET	RW	0x00000000	32	See *4.7.29 PWRDNCFG1SET* on page 4-103.
0x00DC	PWRDNCFG1CLR	RW	0x00000000	32	See *4.7.30 PWRDNCFG1CLR* on page 4-105.
0x00E0	RTCRESET	WO	0x00000000	32	See *4.7.31 RTCRESET* on page 4-106.
0x00E4	EVENTCFG	RW	0x00000000	32	See *4.7.32 EVENTCFG* on page 4-107.
0x0FD0	PID4	RO	0x00000004	32	See *4.7.33 PID4* on page 4-108.
0x0FE0	PID0	RO	0x00000042	32	See *4.7.37 PID0* on page 4-110.
0x0FE4	PID1	RO	0x000000B7	32	See *4.7.38 PID1* on page 4-111.
0x0FE8	PID2	RO	0x000000rB	32	See *4.7.39 PID2* on page 4-111.
0x0FEC	PID3	RO	0x00000000	32	See *4.7.40 PID3* on page 4-112.
0x0FF0	CID0	RO	0x0000000D	32	See *4.7.41 CID0* on page 4-112.
0x0FF4	CID1	RO	0x00000010	32	See *4.7.42 CID1* on page 4-113.
0x0FF8	CID2	RO	0x00000005	32	See *4.7.43 CID2* on page 4-114.
0x0FFC	CID3	RO	0x000000B1	32	See *4.7.44 CID3* on page 4-114.

4.7.2 PMUCTRL

The PMUCTRL Register characteristics are:

Purpose

This register is the PMU control register.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

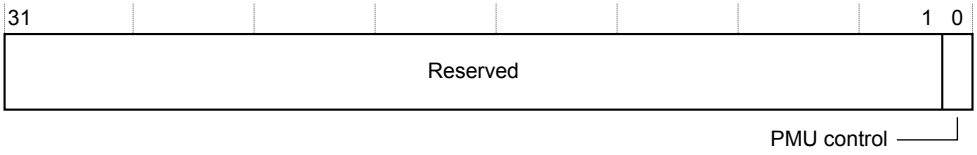

Figure 4-2 PMUCTRL Register bit assignments

The following table shows the bit assignments.

Table 4-7 PMUCTRL Register bit assignments

Bits	Name	Function
[31:1]	-	Reserved. Software that reads this register must ignore these bits.
[0]	PMU control	`0b0` PMU not enabled. `0b1` PMU enabled. **Note** This bit is always `0b1`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.3 RESETOP

The RESETOP Register characteristics are:

Purpose

Initiates Warm reset if Cortex-M3 locks up.

Usage constraints

Bits [31:1] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

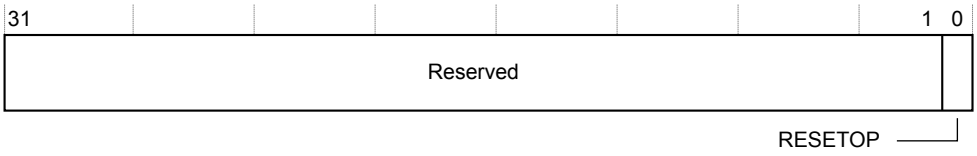

Figure 4-3 RESETOP Register bit assignments

The following table shows the bit assignments.

Table 4-8 RESETOP Register bit assignments

Bits	Name	Function
[31:1]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[0]	RESETOP	`0b0` No Warm reset if Cortex-M3 locks up. `0b1` Warm reset if Cortex-M3 locks up.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.4 RSTINFO

The RSTINFO Register characteristics are:

Purpose

Stores the condition that caused the last reset to enable application software to act accordingly. This register is writable to enable software to clear it after reading, because the reset process does not clear the register before writing.

Usage constraints

Bits [31:4] are reserved. Bits [3:0] are W1C access, that is, software writes `0b1` to a bit position to clear that bit. Other bits are left unchanged.

Configurations

Available in all V2M-Beetle evaluation board configuration.

The following figure shows the bit assignments.

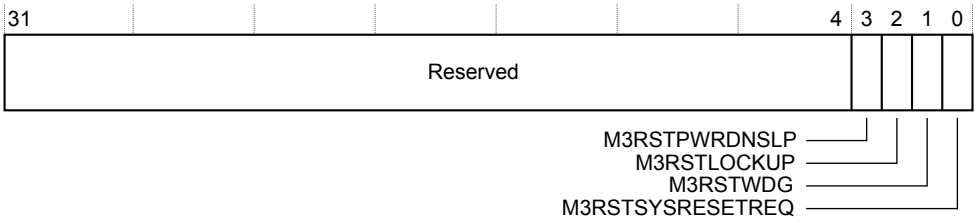

Figure 4-4 RSTINFO Register bit assignments

The following table shows the bit assignments.

Table 4-9 RSTINFO Register bit assignments

Bits	Name	Function
[31:4]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[3]	M3RSTPWRDNSLP	`0b0` No Warm reset if Cortex-M3 is reset from powerdown sleep. `0b1` Warm reset if Cortex-M3 is reset from powerdown sleep.
[2]	M3RSTLOCKUP	`0b0` No Warm reset if Cortex-M3 is reset from lockup. `0b1` Warm reset if Cortex-M3 is reset from lockup.
[1]	M3RSTWDG	`0b0` Cortex-M3 Warm reset from watchdog is not enabled. `0b1` Cortex-M3 Warm reset from watchdog is enabled.
[0]	M3RSTSYSRESETREQ	`0b0` Cortex-M3 Warm reset from **SYSRESETREQ** is not enabled. `0b1` Cortex-M3 Warm reset from **SYSRESETREQ** is enabled.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.5 AHBPER0SET

The AHBPER0SET Register characteristics are:

Purpose

Sets AHB peripheral access privilege. This register has the same read value as register AHBPER0CLR.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

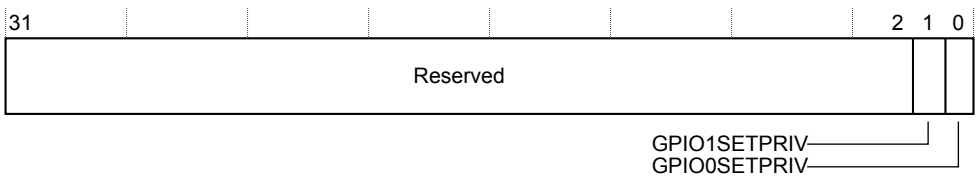

Figure 4-5 AHBPER0SET Register bit assignments

The following table shows the bit assignments.

Table 4-10 AHBPER0SET Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1SETPRIV	`0b0` No effect. `0b1` Sets GPIO1 privileged access.
[0]	GPIO0SETPRIV	`0b0` No effect. `0b1` Sets GPIO0 privileged access.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.6 AHBPER0CLR

The AHBPER0CLR Register characteristics are:

Purpose

Clears AHB peripheral access privilege. This register has the same read value as register AHBPER0SET.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

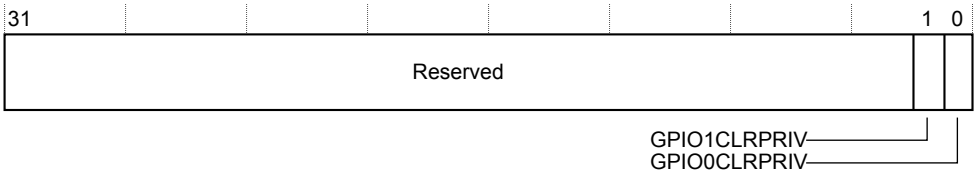

Figure 4-6 AHBPER0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-11 AHBPER0CLR Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLRPRIV	`0b0` No effect. `0b1` Clears GPIO1 privileged access.
[0]	GPIO0CLRPRIV	`0b0` No effect. `0b1` Clears GPIO0 privileged access.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.7 APBPER0SET

The APBPER0SET Register characteristics are:

Purpose

Sets APB peripheral access privilege. This register has the same read value as register APBPER0CLR.

Usage constraints

Bits [31:16], bits [10:9], and bit [3], are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

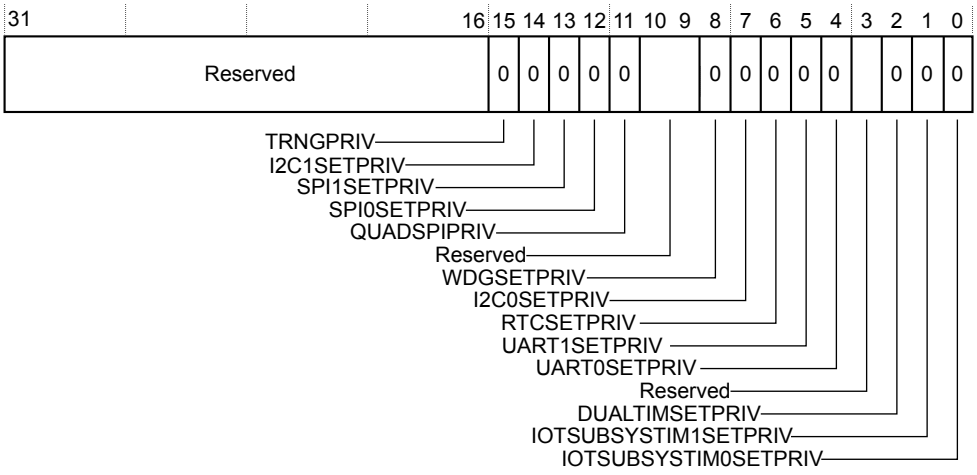

Figure 4-7 APBPER0SET Register bit assignments

The following table shows the bit assignments.

Table 4-12 APBPER0SET Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGPRIV	This bit is permanently `0b1`. True Random Number Generator has permanent privileged access.
[14]	I2C1SETPRIV	`0b0` No effect. `0b1` Sets I2C1 privileged access.
[13]	SPI1SETPRIV	`0b0` No effect. `0b1` Sets SPI1 privileged access.
[12]	SPI0SETPRIV	`0b0` No effect. `0b1` Sets SPI0 privileged access.
[11]	QUADSPIPRIV	`0b0` No effect. `0b1` Sets QuadSPI privileged access.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGSETPRIV	`0b0` No effect. `0b1` Sets watchdog privileged access.
[7]	I2C0SETPRIV	`0b0` No effect. `0b1` Sets I2C0 privileged access.
[6]	RTCSETPRIV	`0b0` No effect. `0b1` Sets RTC privileged access.
[5]	UART1SETPRIV	`0b0` No effect. `0b1` Sets UART1 privileged access.
[4]	UART0SETPRIV	`0b0` No effect. `0b1` Sets UART0 privileged access.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMSETPRIV	`0b0` No effect. `0b1` Sets dual-timer privileged access.

Table 4-12 APBPER0SET Register bit assignments (continued)

Bits	Name	Function
[1]	IOTSUBSYSTIM1SETPRIV	`0b0` No effect. `0b1` Sets IoT Compute subsystem Timer 1 privileged access.
[0]	IOTSUBSYSTIM0SETPRIV	`0b0` No effect. `0b1` Sets IoT Compute subsystem Timer 0 privileged access.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.8 APBPER0CLR

The APBPER0CLR Register characteristics are:

Purpose

Clears APB peripheral access privilege. This register has the same read value as register APBPER0SET.

Usage constraints

Bits [31:16], bits [10:9], and bit [3], are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

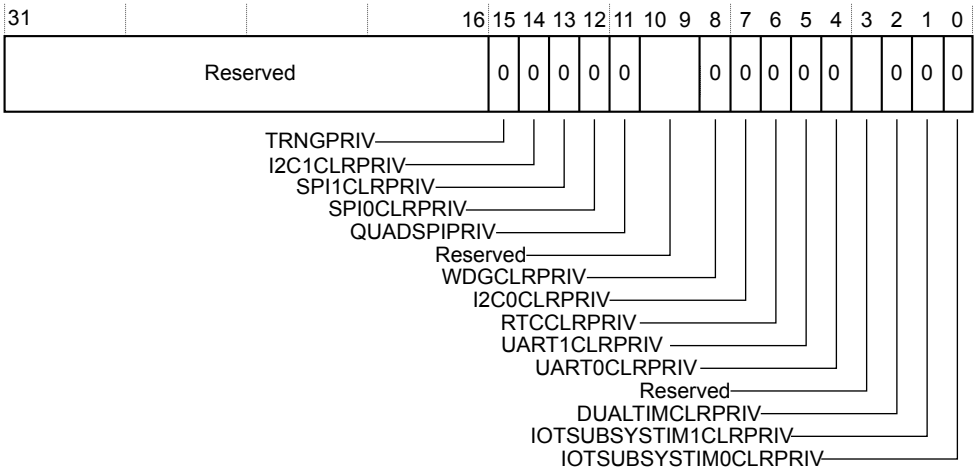

Figure 4-8 APBPER0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-13 APBPER0CLR Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGPRIV	This bit is permanently `0b1`. True Random Number Generator has permanent privileged access.
[14]	I2C1CLRPRIV	`0b0` No effect. `0b1` Clears I2C1 privileged access.
[13]	SPI1CLRPRIV	`0b0` No effect. `0b1` Clears SPI1 privileged access.
[12]	SPI0CLRPRIV	`0b0` No effect. `0b1` Clears SPI0 privileged access.
[11]	QUADSPIPRIV	`0b0` No effect. `0b1` Clears QuadSPI privileged access.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLRPRIV	`0b0` No effect. `0b1` Clears watchdog privileged access.
[7]	I2C0CLRPRIV	`0b0` No effect. `0b1` Clears I2C0 privileged access.
[6]	RTCCLRPRIV	`0b0` No effect. `0b1` Clears RTC privileged access.
[5]	UART1CLRPRIV	`0b0` No effect. `0b1` Clears UART1 privileged access.
[4]	UART0CLRPRIV	`0b0` No effect. `0b1` Clears UART0 privileged access.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMCLRPRIV	`0b0` No effect. `0b1` Clears dual-timer privileged access.

Table 4-13 APBPER0CLR Register bit assignments (continued)

Bits	Name	Function
[1]	IOTSUBSYSTIM1CLRPRIV	`0b0` No effect. `0b1` Clears IoT Compute subsystem Timer 1 privileged access.
[0]	IOTSUBSYSTIM0CLRPRIV	`0b0` No effect. `0b1` Clears IoT Compute subsystem Timer 0 privileged access.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.9 MAINCLK

The MAINCLK Register characteristics are:

Purpose

Configures the main clock control circuitry.

Usage constraints

Bits [31:8] and bits [3:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

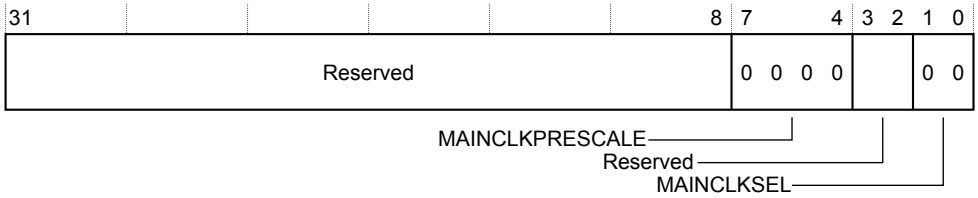

Figure 4-9 MAINCLK Register bit assignments

The following table shows the bit assignments.

Table 4-14 MAINCLK Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[7:4]	MAINCLKPRESCALE[3:0]	Prescales main clock frequency: `0b0000` Bypass prescaler. No frequency division. `0b0001-0b1111` Frequency division factor is (MAINCLKPRESCALE[3:0] + 1).

Table 4-14 MAINCLK Register bit assignments (continued)

Bits	Name	Function
[3:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1:0]	MAINCLKSEL[1:0]	Selects source for main clock: `0b00` 24MHz clock. 24MHz is the default input. `0b01` PLL output. `0b10` 32kHz. `0b11` Invalid. Do not use.

Related concepts

4.7.1 System control register summary on page 4-63
2.4 Clocks on page 2-25

4.7.10 AUXCLK

The AUXCLK Register characteristics are:

Purpose

Configures the auxiliary clock and RTC clock control circuitry.

Usage constraints

Bits [31:8], bits [6:5], and bits [3:0] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

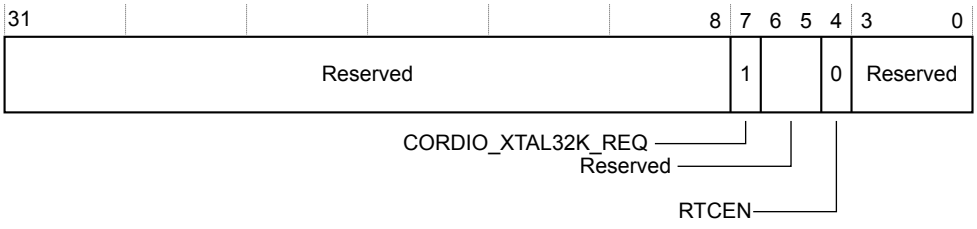

Figure 4-10 AUXCLK Register bit assignments

The following table shows the bit assignments.

Table 4-15 AUXCLK Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[7]	CORDIO_XTAL32K_REQ	Request 32kHz crystal frequency from Cordio BT4 radio interface: `0b0` No request. `0b1` Request. The request is enabled by default.
[6:5]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[4]	RTCEN	RTC clock gate and divider enable: `0b0` Not enabled. `0b1` Enabled.
[3:0]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.11 AHBCLKCFG0SET

The AHBCLKCFG0SET Register characteristics are:

Purpose

Enables AHB peripheral clocks. This register operates when the test chip is in the Active state. This register has the same read value as the AHBCLKCFG0CLR register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

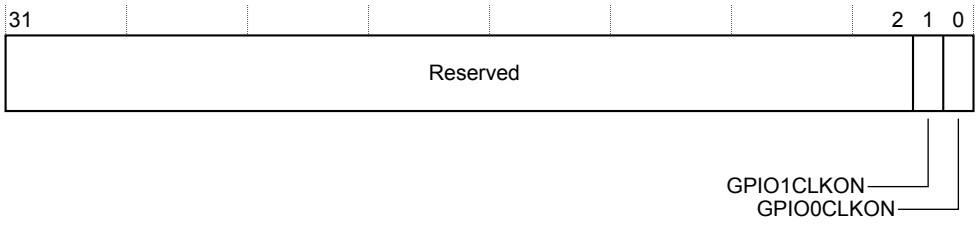

Figure 4-11 AHBCLKCFG0SET Register bit assignments

The following table shows the bit assignments.

Table 4-16 AHBCLKCFG0SET Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKON	Enables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.
[0]	GPIO0CLKON	Enables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.12 AHBCLKCFG0CLR

The AHBCLKCFG0CLR Register characteristics are:

Purpose

Disables AHB peripheral clocks. This register operates when the test chip is in the Active state. This register has the same read value as the AHBCLKCFG1SET register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

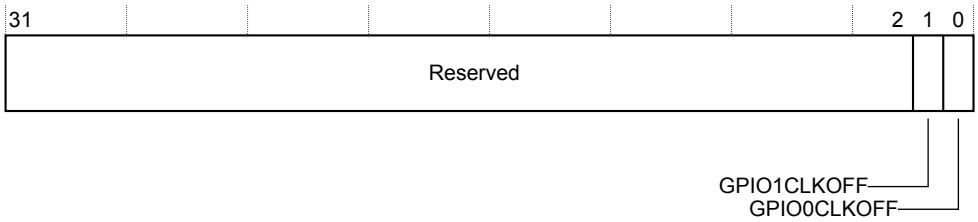

Figure 4-12 AHBCLKCFG0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-17 AHBCLKCFG0CLR Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKOFF	Disables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.
[0]	GPIO0CLKOFF	Disables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.13 AHBCLKCFG1SET

The AHBCLKCFG1SET Register characteristics are:

Purpose

Enables AHB peripheral clocks. This register operates when the test chip is in the Sleep state. This register has the same read value as the AHBCLKCFG1CLR register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

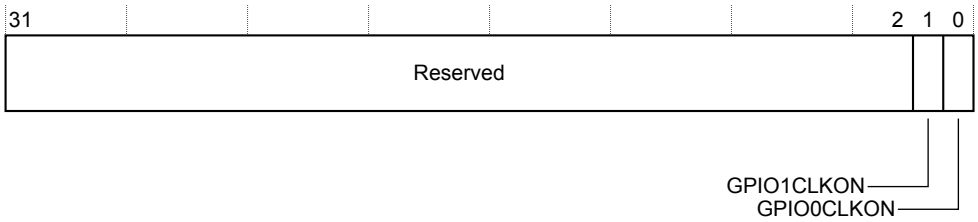

Figure 4-13 AHBCLKCFG1SET Register bit assignments

The following table shows the bit assignments.

Table 4-18 AHBCLKCFG1SET Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKON	Enables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.
[0]	GPIO0CLKON	Enables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.14 AHBCLKCFG1CLR

The AHBCLKCFG1CLR Register characteristics are:

Purpose

Disables AHB peripheral clocks. This register operates when the test chip is in the Sleep state. This register has the same read value as the AHBCLKCFG1SET register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

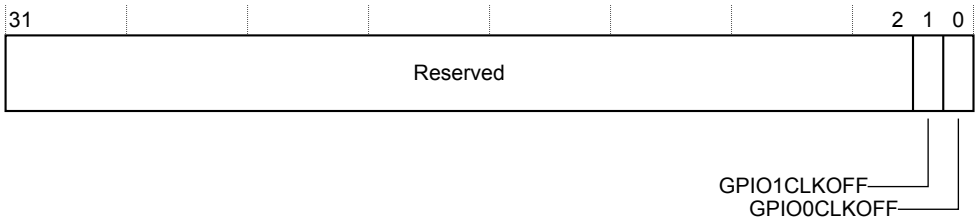

Figure 4-14 AHBCLKCFG1CLR Register bit assignments

The following table shows the bit assignments.

Table 4-19 AHBCLKCFG1CLR Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKOFF	Disables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.
[0]	GPIO0CLKOFF	Disables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.15 AHBCLKCFG2SET

The AHBCLKCFG2SET Register characteristics are:

Purpose

Enables AHB peripheral clocks. This register operates when the test chip is in the deep sleep state, or the powerdown state. This register has the same read value as the AHBCLKCFG2CLR register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

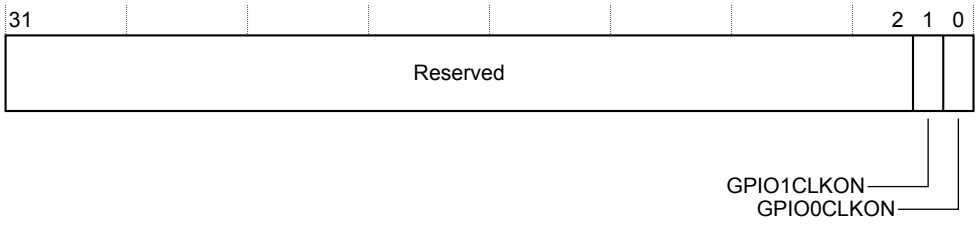

Figure 4-15 AHBCLKCFG2SET Register bit assignments

The following table shows the bit assignments.

Table 4-20 AHBCLKCFG2SET Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKON	Enables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.
[0]	GPIO0CLKON	Enables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.16 AHBCLKCFG2CLR

The AHBCLKCFG2CLR Register characteristics are:

Purpose

Disables AHB peripheral clocks. This register operates when the test chip is in the deep sleep state, or the powerdown state. This register has the same read value as the AHBCLKCFG2SET register.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

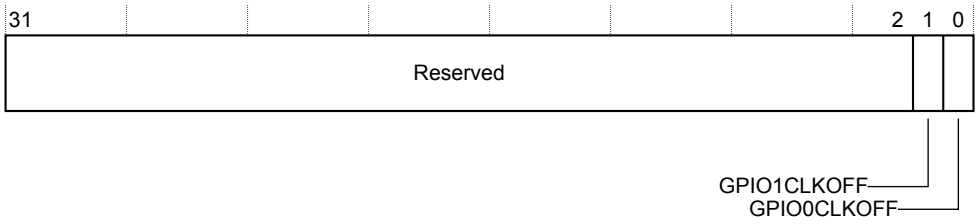

Figure 4-16 AHBCLKCFG2CLR Register bit assignments

The following table shows the bit assignments.

Table 4-21 AHBCLKCFG2CLR Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1CLKOFF	Disables GPIO1 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.
[0]	GPIO0CLKOFF	Disables GPIO0 AHB peripheral clocks: `0b0` No effect. `0b1` FCLK and HCLK are both off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.17 APBCLKCFG0SET

The APBCLKCFG0SET Register characteristics are:

Purpose

Enables APB peripheral clocks. This register operates when the test chip is in the Active state. This register has the same read value as the APBCLKCFG0CLR register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

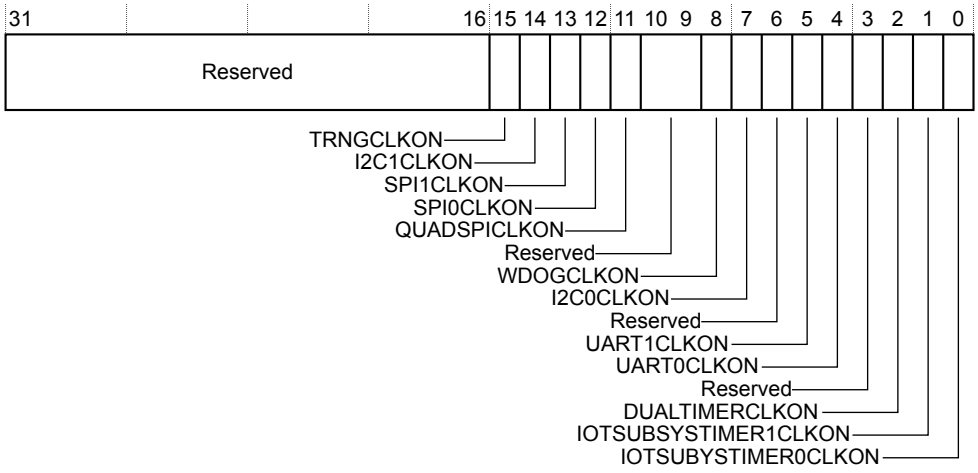

Figure 4-17 APBCLKCFG0SET Register bit assignments

The following table shows the bit assignments.

Table 4-22 APBCLKCFG0SET Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKON	Enables True Random Number Generator (TRNG) clock: 0b0 No effect. 0b1 TRNG clock is on.
[14]	I2C1CLKON	Enables I2C1 clock: 0b0 No effect. 0b1 I2C1 clock is on.
[13]	SPI1CLKON	Enables SPI1 clock: 0b0 No effect. 0b1 SPI1 clock is on.
[12]	SPI0CLKON	Enables SPI0 clock: 0b0 No effect. 0b1 SPI0 clock is on.
[11]	QUADSPICCLKON	Enables QUADSPI clock: 0b0 No effect. 0b1 QUADSPI clock is on.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLKON	Enables Watchdog clock: 0b0 No effect. 0b1 Watchdog clock is on.
[7]	I2C0CLKON	Enables I2C0 clock: 0b0 No effect. 0b1 I2C0 clock is on.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKON	Enables UART1 clock: 0b0 No effect. 0b1 UART1 clock is on.
[4]	UART0CLKON	Enables UART0 clock: 0b0 No effect. 0b1 UART0 clock is on.

Table 4-22 APBCLKCFG0SET Register bit assignments (continued)

Bits	Name	Function
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKON	Enables dual-timer clock: `0b0` No effect. `0b1` Dual-timer clock is on.
[1]	IOTSUBSYSTIMER1CLKON	Enables IoT Compute subsystem Timer 1 clock: `0b0` No effect. `0b1` IoT Compute subsystem Timer 1 clock is on.
[0]	IOTSUBSYSTIMER0CLKON	Enables IoT Compute subsystem Timer 0 clock: `0b0` No effect. `0b1` IoT Compute subsystem Timer 0 clock is on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.18 APBCLKCFG0CLR

The APBCLKCFG0CLR Register characteristics are:

Purpose

Disables APB peripheral clocks. This register operates when the test chip is in the Active state. This register has the same read value as the APBCLKCFG0SET register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

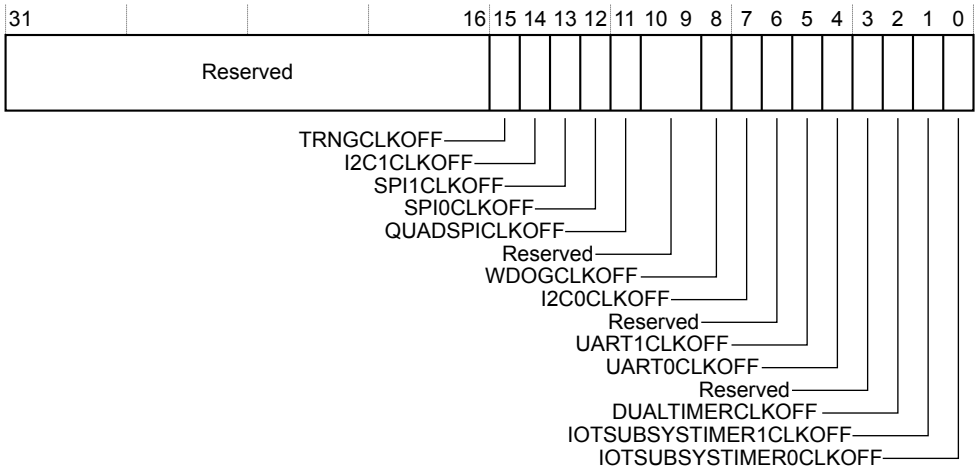

Figure 4-18 APBCLKCFG0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-23 APBCLKCFG0CLR Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKOFF	Disables True Random Number Generator (TRNG) clock: `0b0` No effect. `0b1` TRNG clock is off.
[14]	I2C1CLKOFF	Disables I2C1 clock: `0b0` No effect. `0b1` I2C1 clock is off.
[13]	SPI1CLKOFF	Disables SPI1 clock: `0b0` No effect. `0b1` SPI1 clock is off.
[12]	SPI0CLKOFF	Disables SPI0 clock: `0b0` No effect. `0b1` SPI0 clock is off.
[11]	QUADSPICCLKOFF	Disables QUADSPI clock: `0b0` No effect. `0b1` QUADSPI clock is off.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.

Table 4-23 APBCLKCFG0CLR Register bit assignments (continued)

Bits	Name	Function
[8]	WDOGCLKOFF	Disables Watchdog clock: 0b0 No effect. 0b1 Watchdog clock is off.
[7]	I2C0CLKOFF	Disables I2C0 clock: 0b0 No effect. 0b1 I2C0 clock is off.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKOFF	Disables UART1 clock: 0b0 No effect. 0b1 UART1 clock is off.
[4]	UART0CLKOFF	Disables UART0 clock: 0b0 No effect. 0b1 UART0 clock is off.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKOFF	Disables dual-timer clock: 0b0 No effect. 0b1 Dual-timer clock is off.
[1]	IOTSUBSYSTIMER1CLKOFF	Disables IoT Compute subsystem Timer 1 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 1 clock is off.
[0]	IOTSUBSYSTIMER0CLKOFF	Disables IoT Compute subsystem Timer 0 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 0 clock is off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.19 APBCLKCFG1SET

The APBCLKCFG1SET Register characteristics are:

Purpose

Enables APB peripheral clocks. This register operates when the test chip is in the Sleep state. This register has the same read value as the APBCLKCFG1CLR register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

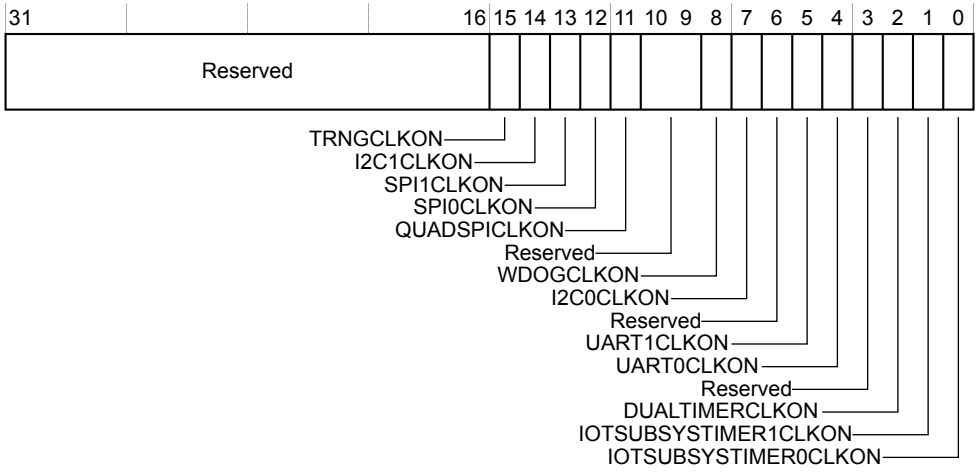

Figure 4-19 APBCLKCFG1SET Register bit assignments

The following table shows the bit assignments.

Table 4-24 APBCLKCFG1SET Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKON	Enables True Random Number Generator (TRNG) clock: `0b0` No effect. `0b1` TRNG clock is on.
[14]	I2C1CLKON	Enables I2C1 clock: `0b0` No effect. `0b1` I2C1 clock is on.
[13]	SPI1CLKON	Enables SPI1 clock: `0b0` No effect. `0b1` SPI1 clock is on.
[12]	SPI0CLKON	Enables SPI0 clock: `0b0` No effect. `0b1` SPI0 clock is on.
[11]	QUADSPICCLKON	Enables QUADSPI clock: `0b0` No effect. `0b1` QUADSPI clock is on.

Table 4-24 APBCLKCFG1SET Register bit assignments (continued)

Bits	Name	Function
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLKON	Enables Watchdog clock: `0b0` No effect. `0b1` Watchdog clock is on.
[7]	I2C0CLKON	Enables I2C0 clock: `0b0` No effect. `0b1` I2C0 clock is on.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKON	Enables UART1 clock: `0b0` No effect. `0b1` UART1 clock is on.
[4]	UART0CLKON	Enables UART0 clock: `0b0` No effect. `0b1` UART0 clock is on.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKON	Enables dual-timer clock: `0b0` No effect. `0b1` Dual-timer clock is on.
[1]	IOTSUBSYSTIMER1CLKON	Enables IoT Compute subsystem Timer 1 clock: `0b0` No effect. `0b1` IoT Compute subsystem Timer 1 clock is on.
[0]	IOTSUBSYSTIMER0CLKON	Enables IoT Compute subsystem Timer 0 clock is on: `0b0` No effect. `0b1` IoT Compute subsystem Timer 0 clock is on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.20 APBCLKCFG1CLR

The APBCLKCFG1CLR Register characteristics are:

Purpose

Disables APB peripheral clocks. This register operates when the test chip is in the Sleep state. This register has the same read value as the APBCLKCFG1SET register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

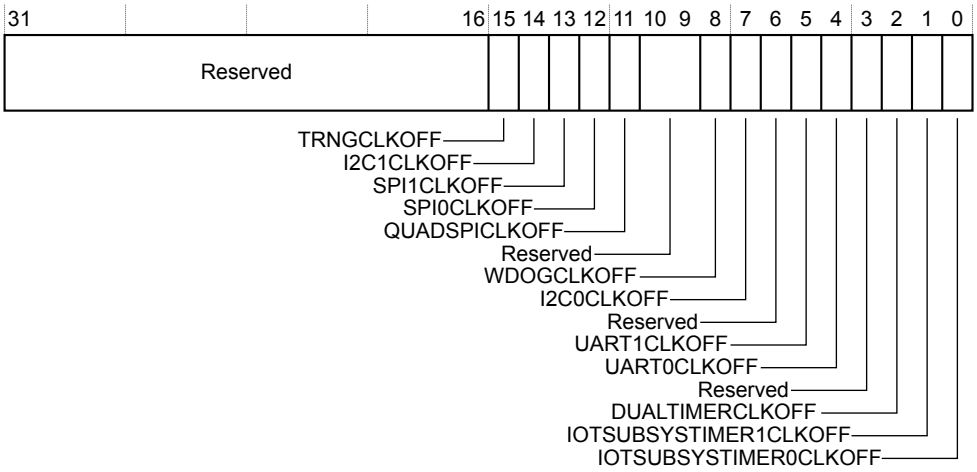

Figure 4-20 APBCLKCFG1CLR Register bit assignments

The following table shows the bit assignments.

Table 4-25 APBCLKCFG1CLR Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKOFF	Disables True Random Number Generator (TRNG) clock: `0b0` No effect. `0b1` TRNG clock is off.
[14]	I2C1CLKOFF	Disables I2C1 clock: `0b0` No effect. `0b1` I2C1 clock is off.
[13]	SPI1CLKOFF	Disables SPI1 clock: `0b0` No effect. `0b1` SPI1 clock is off.
[12]	SPI0CLKOFF	Disables SPI0 clock: `0b0` No effect. `0b1` SPI0 clock is off.

Table 4-25 APBCLKCFG1CLR Register bit assignments (continued)

Bits	Name	Function
[11]	QUADSPICCLKOFF	Disables QUADSPI clock: 0b0 No effect. 0b1 QUADSPI clock is off.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLKOFF	Disables Watchdog clock: 0b0 No effect. 0b1 Watchdog clock is off.
[7]	I2C0CLKOFF	Disables I2C0 clock: 0b0 No effect. 0b1 I2C0 clock is off.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKOFF	Disables UART1 clock: 0b0 No effect. 0b1 UART1 clock is off.
[4]	UART0CLKOFF	Disables UART0 clock: 0b0 No effect. 0b1 UART0 clock is off.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKOFF	Disables dual-timer clock: 0b0 No effect. 0b1 Dual-timer clock is off.
[1]	IOTSUBSYSTIMER1CLKOFF	Disables IoT Compute subsystem Timer 1 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 1 clock is off.
[0]	IOTSUBSYSTIMER0CLKOFF	Disables IoT Compute subsystem Timer 0 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 0 clock is off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.21 APBCLKCFG2SET

The APBCLKCFG2SET Register characteristics are:

Purpose

Enables APB peripheral clocks. This register operates when the test chip is in the deep sleep state, or the powerdown state. This register has the same read value as the APBCLKCFG2CLR register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

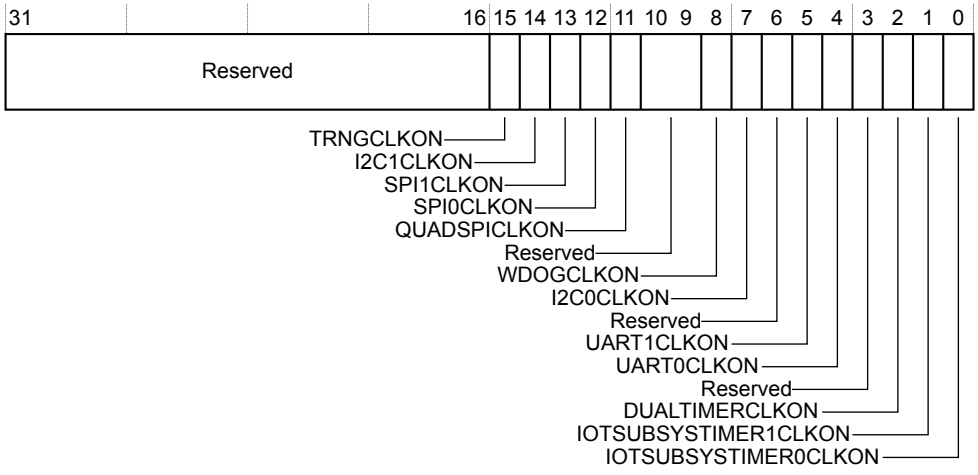

Figure 4-21 APBCLKCFG2SET Register bit assignments

The following table shows the bit assignments.

Table 4-26 APBCLKCFG2SET Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKON	Enables True Random Number Generator (TRNG) clock: `0b0` No effect. `0b1` TRNG clock is on.
[14]	I2C1CLKON	Enables I2C1 clock: `0b0` No effect. `0b1` I2C1 clock is on.

Table 4-26 APBCLKCFG2SET Register bit assignments (continued)

Bits	Name	Function
[13]	SPI1CLKON	Enables SPI1 clock: 0b0 No effect. 0b1 SPI1 clock is on.
[12]	SPI0CLKON	Enables SPI0 clock: 0b0 No effect. 0b1 SPI0 clock is on.
[11]	QUADSPICCLKON	Enables QUADSPI clock: 0b0 No effect. 0b1 QUADSPI clock is on.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLKON	Enables Watchdog clock: 0b0 No effect. 0b1 Watchdog clock is on.
[7]	I2C0CLKON	Enables I2C0 clock: 0b0 No effect. 0b1 I2C0 clock is on.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKON	Enables UART1 clock: 0b0 No effect. 0b1 UART1 clock is on.
[4]	UART0CLKON	Enables UART0 clock: 0b0 No effect. 0b1 UART0 clock is on.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKON	Enables dual-timer clock: 0b0 No effect. 0b1 Dual-timer clock is on.

Table 4-26 APBCLKCFG2SET Register bit assignments (continued)

Bits	Name	Function
[1]	IOTSUBSYSTIMER1CLKON	Enables IoT Compute subsystem Timer 1 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 1 clock is on.
[0]	IOTSUBSYSTIMER0CLKON	Enables IoT Compute subsystem Timer 0 clock: 0b0 No effect. 0b1 IoT Compute subsystem Timer 0 clock is on.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.22 APBCLKCFG2CLR

The APBCLKCFG2CLR Register characteristics are:

Purpose

Disables APB peripheral clocks. This register operates when the test chip is in the deep sleep state, or the powerdown state. This register has the same read value as the APBCLKCFG2CLR register.

Usage constraints

Bits [31:16], bits [10:9], bit [6], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

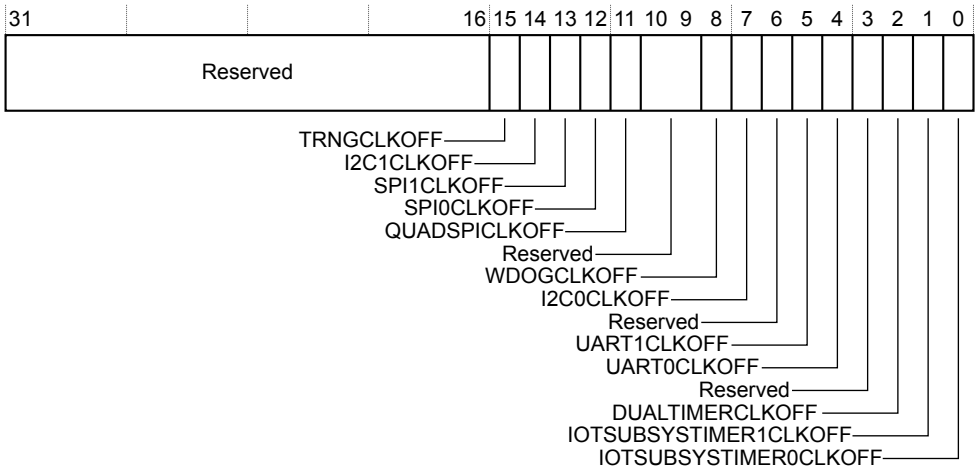

Figure 4-22 APBCLKCFG2CLR Register bit assignments

The following table shows the bit assignments.

Table 4-27 APBCLKCFG2CLR Register bit assignments

Bits	Name	Function
[31:16]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[15]	TRNGCLKOFF	Disables True Random Number Generator (TRNG) clock: 0b0 No effect. 0b1 TRNG clock is off.
[14]	I2C1CLKOFF	Disables I2C1 clock: 0b0 No effect. 0b1 I2C1 clock is off.
[13]	SPI1CLKOFF	Disables SPI1 clock: 0b0 No effect. 0b1 SPI1 clock is off.
[12]	SPI0CLKOFF	Disables SPI0 clock: 0b0 No effect. 0b1 SPI0 clock is off.
[11]	QUADSPICCLKOFF	Disables QUADSPI clock: 0b0 No effect. 0b1 QUADSPI clock is off.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGCLKOFF	Disables Watchdog clock: 0b0 No effect. 0b1 Watchdog clock is off.
[7]	I2C0CLKOFF	Disables I2C0 clock: 0b0 No effect. 0b1 I2C0 clock is off.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1CLKOFF	Disables UART1 clock: 0b0 No effect. 0b1 UART1 clock is off.
[4]	UART0CLKOFF	Disables UART0 clock: 0b0 No effect. 0b1 UART0 clock is off.

Table 4-27 APBCLKCFG2CLR Register bit assignments (continued)

Bits	Name	Function
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERCLKOFF	Disables dual-timer clock: `0b0` No effect. `0b1` Dual-timer clock is off.
[1]	IOTSUBSYSTIMER1CLKOFF	Disables IoT Compute subsystem Timer 1 clock: `0b0` No effect. `0b1` IoT Compute subsystem Timer 1 clock is off.
[0]	IOTSUBSYSTIMER0CLKOFF	Disables IoT Compute subsystem Timer 0 clock: `0b0` No effect. `0b1` IoT Compute subsystem Timer 0 clock is off.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.23 AHBPRST0SET

The AHBPRST0SET Register characteristics are:

Purpose

Enables **nPOR** as the reset signal for the AHB peripherals. When set, the system-wide software reset does not reset the peripheral which is necessary if the peripheral needs to wake the system. This register has the same read value as the AHBPRST0CLR register.

Usage constraints

Bits [31:4] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

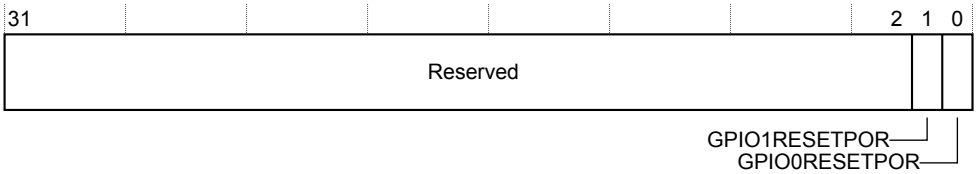

Figure 4-23 AHBPRST0SET Register bit assignments

The following table shows the bit assignments.

Table 4-28 AHBPRST0SET Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1RESETPOR	`0b0` No effect. `0b1` Enables **nPOR** as the reset signal for the GPIO1 AHB peripherals.
[0]	GPIO0RESETPOR	`0b0` No effect. `0b1` Enables **nPOR** as the reset signal for the GPIO0 AHB peripherals.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.24 AHBPRST0CLR

The AHBPRST0CLR Register characteristics are:

Purpose

Disables **nPOR** as the reset signal for the AHB peripherals. This register has the same read value as the AHBPRST0SET register.

Usage constraints

Bits [31:4] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

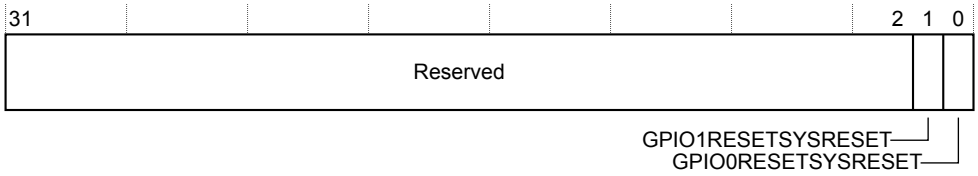

Figure 4-24 AHBPRST0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-29 AHBPRST0CLR Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1RESETSYSRESET	`0b0` No effect. `0b1` Selects system reset as the reset signal for the GPIO1 AHB peripherals.
[0]	GPIO0ESETSYSRESET	`0b0` No effect. `0b1` Selects system reset as the reset signal for the GPIO0 AHB peripherals.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.25 APBPRST0SET

The APBPRST0SET Register characteristics are:

Purpose

Enables **nPOR** as the reset signal for the APB peripherals. When set, the system-wide software reset does not reset the peripheral which is necessary if the peripheral needs to wake the system. This register has the same read value as the APBPRST0CLR register.

Usage constraints

Bits [31:15], bits [10:8], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

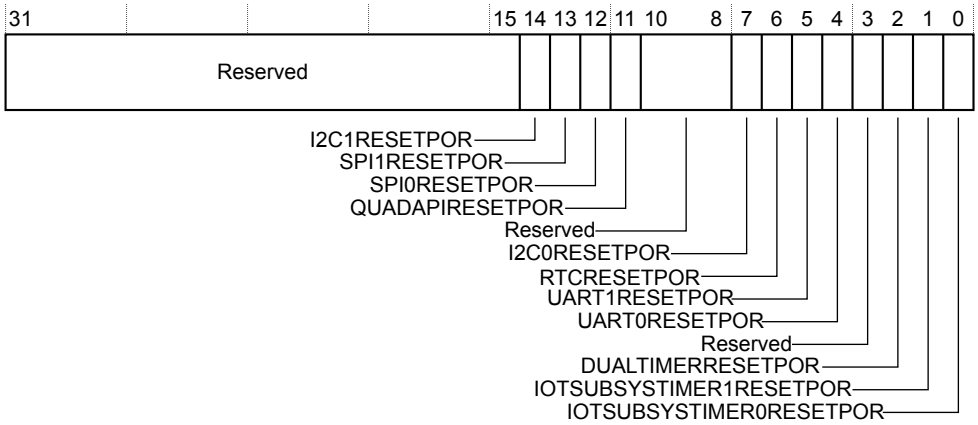

Figure 4-25 APBPRST0SET Register bit assignments

The following table shows the bit assignments.

Table 4-30 APBPRST0SET Register bit assignments

Bits	Name	Function
[31:15]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[14]	I2C1RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the I2C1 peripheral.
[13]	SPI1RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the SPI1 peripheral.
[12]	SPI0RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the SPI0 peripheral.
[11]	QUADSPICRESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the QUADSPI.
[10:8]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[7]	I2C0RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the I2C0 peripheral.
[6]	RTCRESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the real-time clock.
[5]	UART1RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for UART1.
[4]	UART0RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for UART0.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERRESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the dual-timer.

Table 4-30 APBPRST0SET Register bit assignments (continued)

Bits	Name	Function
[1]	IOTSUBSYSTIMER1RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the IoT Compute subsystem Timer 1.
[0]	IOTSUBSYSTIMER0RESETPOR	`0b0` No effect. `0b1` Selects **nPOR** as the reset signal for the IoT Compute subsystem Timer 0.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.26 APBPRST0CLR

The APBPRST0CLR Register characteristics are:

Purpose

Disables **nPOR** as the reset signal for the APB peripherals. This register has the same read value as the APBPRST0SET register.

Usage constraints

Bits [31:15], bits [10:8], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

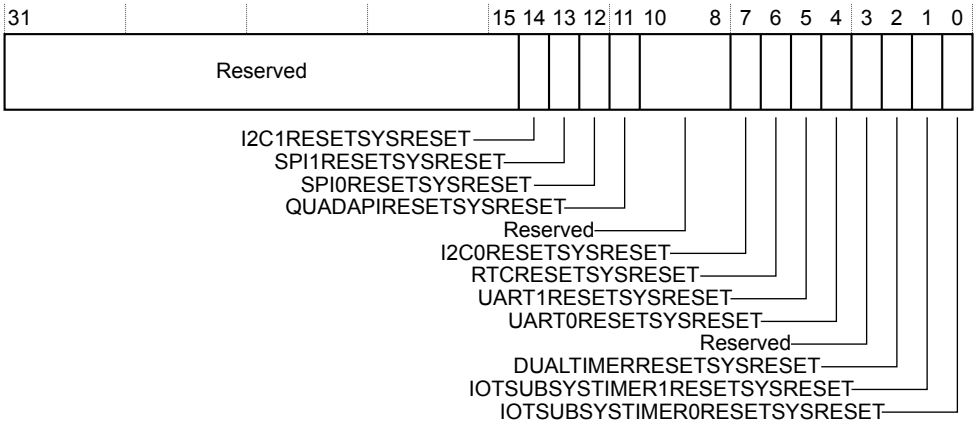

Figure 4-26 APBPRST0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-31 APBPRST0CLR Register bit assignments

Bits	Name	Function
[31:15]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[14]	I2C1RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the I2C1 peripheral.
[13]	SPI1RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the SPI1 peripheral.
[12]	SPI0RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the SPI0 peripheral.
[11]	QUADSPICRESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the QUADSPI.
[10:8]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[7]	I2C0RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the I2C0 peripheral.
[6]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[5]	UART1RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for UART1.
[4]	UART0RESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for UART0.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERRESETSYSRESET	0b0 No effect. 0b1 Selects system reset as the reset signal for the dual-timer.

Table 4-31 APBPRST0CLR Register bit assignments (continued)

Bits	Name	Function
[1]	IOTSUBSYSTIMER1RESETSYSRESET	`0b0` No effect. `0b1` Selects system reset as the reset signal for the IoT Compute subsystem Timer 1.
[0]	IOTSUBSYSTIMER0RESETSYSRESET	`0b0` No effect. `0b1` Selects system reset as the reset signal for the IoT Compute subsystem Timer 0.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.27 PWRDNCFG0SET

The PWRDNCFG0SET Register characteristics are:

Purpose

Enables sleep state wakeup signals for the AHB peripherals. This register has the same read value as PWRDNCFG0CLR.

Usage constraints

Bits [31:17], and bits [15:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

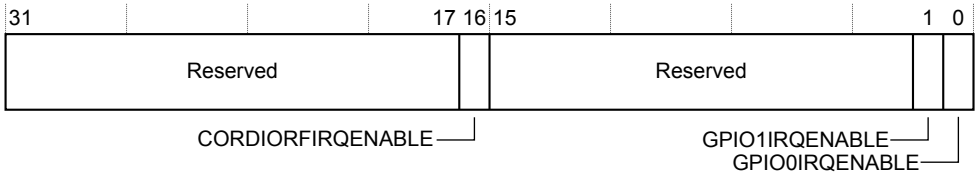

Figure 4-27 PWRDNCFG0SET Register bit assignments

The following table shows the bit assignments.

Table 4-32 PWRDNCFG0SET Register bit assignments

Bits	Name	Function
[31:17]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[16]	CORDIORFIRQENABLE	`0b0` No effect. `0b1` Enables Cordio BT4 RF block IRQ as wakeup source.

Table 4-32 PWRDNCFG0SET Register bit assignments (continued)

Bits	Name	Function
[15:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1IRQENABLE	`0b0` No effect. `0b1` Enables GPIO1 IRQ as wakeup source.
[0]	GPIO0IRQENABLE	`0b0` No effect. `0b1` Enables GPIO0 IRQ as wakeup source.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.28 PWRDNCFG0CLR

The PWRDNCFG0CLR Register characteristics are:

Purpose

Disables sleep state wakeup signals for the AHB peripherals. This register has the same read value as PWRDNCFG0SET.

Usage constraints

Bits [31:17], and bits [15:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

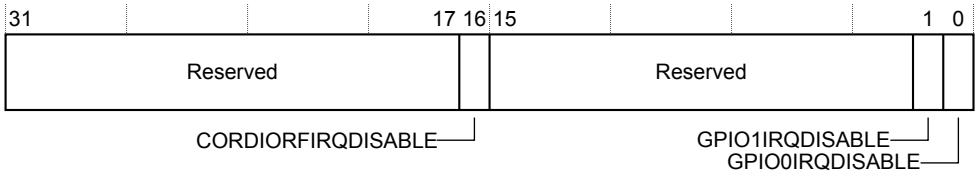

Figure 4-28 PWRDNCFG0CLR Register bit assignments

The following table shows the bit assignments.

Table 4-33 PWRDNCFG0CLR Register bit assignments

Bits	Name	Function
[31:17]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[16]	CORDIORFIRQDISABLE	`0b0` No effect. `0b1` Disables Cordio BT4 RF block IRQ as wakeup source.

Table 4-33 PWRDNCFG0CLR Register bit assignments (continued)

Bits	Name	Function
[15:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO1IRQDISABLE	`0b0` No effect. `0b1` Disables GPIO1 IRQ as wakeup source.
[0]	GPIO0IRQDISABLE	`0b0` No effect. `0b1` Disables GPIO0 IRQ as wakeup source.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.29 PWRDNCFG1SET

The PWRDNCFG1SET Register characteristics are:

Purpose

Enables sleep state wakeup signals for the APB peripherals. This register has the same read value as PWRDNCFG1CLR.

Usage constraints

Bits [31:15], bits [10:9], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

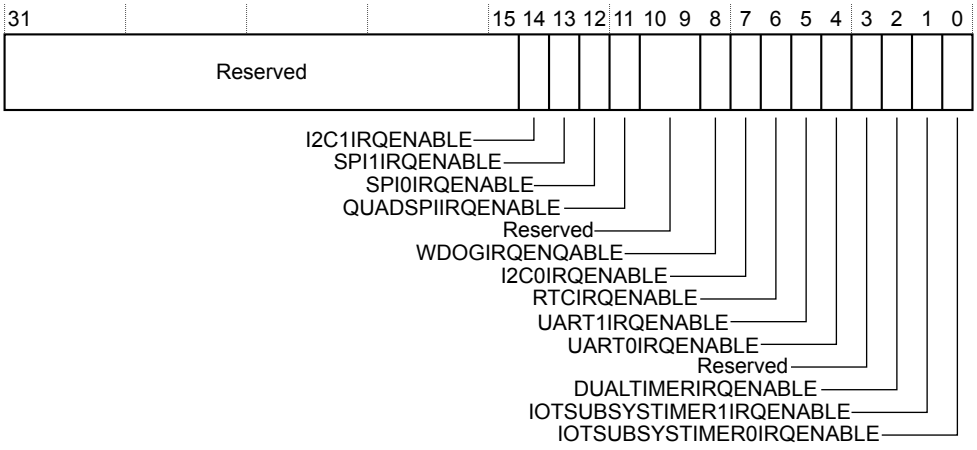

Figure 4-29 PWRDNCFG1SET Register bit assignments

The following table shows the bit assignments.

Table 4-34 PWRDNCFG1SET Register bit assignments

Bits	Name	Function
[31:15]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[14]	I2C1IRQENABLE	0b0 No effect. 0b1 Enables I2C1 IRQ as wakeup source.
[13]	SPI1IRQENABLE	0b0 No effect. 0b1 Enables SPI1 IRQ as wakeup source.
[12]	SPI0IRQENABLE	0b0 No effect. 0b1 Enables SPI0 IRQ as wakeup source.
[11]	QUADSPICIRQENABLE	0b0 No effect. 0b1 Enables QUADSPI IRQ as wakeup source.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGIRQENABLE	0b0 No effect. 0b1 Enables Watchdog IRQ as wakeup source.
[7]	I2C0IRQENABLE	0b0 No effect. 0b1 Enables I2C0 IRQ as wakeup source.
[6]	RTCIRQENABLE	0b0 No effect. 0b1 Enables RTC IRQ as wakeup source.
[5]	UART1IRQENABLE	0b0 No effect. 0b1 Enables UART1 IRQ as wakeup source.
[4]	UART0IRQENABLE	0b0 No effect. 0b1 Enables UART0 IRQ as wakeup source.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERIRQENABLE	0b0 No effect. 0b1 Enables dual-timer IRQ as wakeup source.
[1]	IOTSUBSYSTIMER1IRQENABLE	0b0 No effect. 0b1 Enables IoT Compute subsystem time1 IRQ as wakeup source.
[0]	IOTSUBSYSTIMER0IRQENABLE	0b0 No effect. 0b1 Enables IoT Compute subsystem Timer 0 IRQ as wakeup source.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.30 PWRDNCFG1CLR

The PWRDNCFG1CLR Register characteristics are:

Purpose

Disables sleep state wakeup signals for the APB peripherals. This register has the same read value as PWRDNCFG1SET.

Usage constraints

Bits [31:15], bits [10:9], and bit [3] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

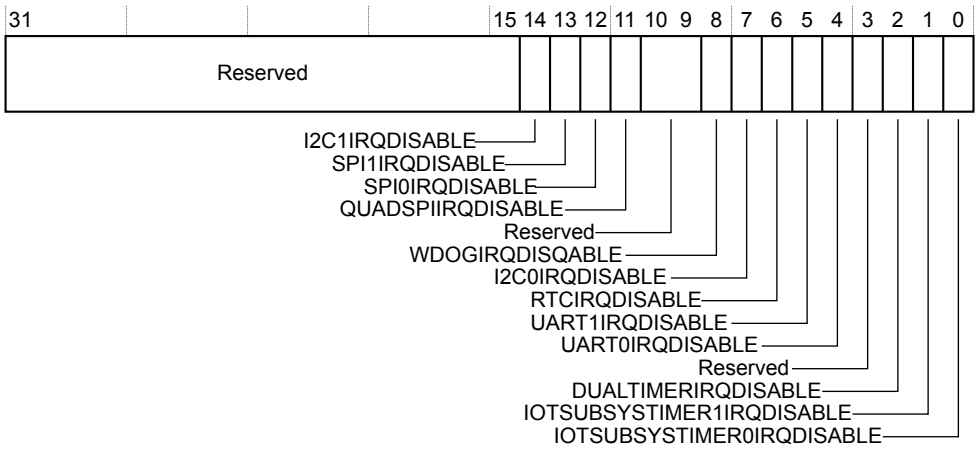

Figure 4-30 PWRDNCFG1CLR Register bit assignments

The following table shows the bit assignments.

Table 4-35 PWRDNCFG1CLR Register bit assignments

Bits	Name	Function
[31:15]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[14]	I2C1IRQDISABLE	`0b0` No effect. `0b1` Disables I2C1 IRQ as wakeup source.
[13]	SPI1IRQDISABLE	`0b0` No effect. `0b1` Disables SPI1 IRQ as wakeup source.
[12]	SPI0IRQDISABLE	`0b0` No effect. `0b1` Disables SPI0 IRQ as wakeup source.

Table 4-35 PWRDNCFG1CLR Register bit assignments (continued)

Bits	Name	Function
[11]	QUADSPICIRQDISABLE	`0b0` No effect. `0b1` Disables QUADSPI IRQ as wakeup source.
[10:9]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[8]	WDOGIRQDISABLE	`0b0` No effect. `0b1` Disables Watchdog IRQ as wakeup source.
[7]	I2C0IRQDISABLE	`0b0` No effect. `0b1` Disables I2C0 IRQ as wakeup source.
[6]	RTCIRQDISABLE	`0b0` No effect. `0b1` Disables RTC IRQ as wakeup source.
[5]	UART1IRQDISABLE	`0b0` No effect. `0b1` Disables UART1 IRQ as wakeup source.
[4]	UART0IRQDISABLE	`0b0` No effect. `0b1` Disables UART0 IRQ as wakeup source.
[3]	-	Reserved. Software that writes to this register must write zero to this bit. Software that reads this register must ignore this bit.
[2]	DUALTIMERIRQDISABLE	`0b0` No effect. `0b1` Disables dual-timer IRQ as wakeup source.
[1]	IOTSUBSYSTIMER1IRQDISABLE	`0b0` No effect. `0b1` Disables IoT Compute subsystem time1 IRQ as wakeup source.
[0]	IOTSUBSYSTIMER0IRQDISABLE	`0b0` No effect. `0b1` Disables IoT Compute subsystem Timer 0 IRQ as wakeup source.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.31 RTCRESET

The RTCRESET Register characteristics are:

Purpose

Resets the real-time clock.

Usage constraints

Bits [31:1] are reserved. Bit [0] is write-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

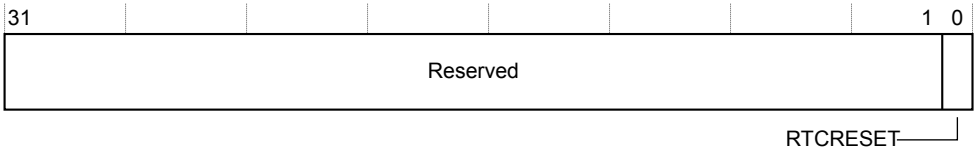

Figure 4-31 RTCRESET Register bit assignments

The following table shows the bit assignments.

Table 4-36 RTCRESET Register bit assignments

Bits	Name	Function
[31:1]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[0]	RTCRESET	Resets the real-time clock, 1Hz domain, to zero.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.32 EVENTCFG

The EVENTCFG Register characteristics are:

Purpose

Controls the event interface.

Usage constraints

Bits [31:2] are reserved.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

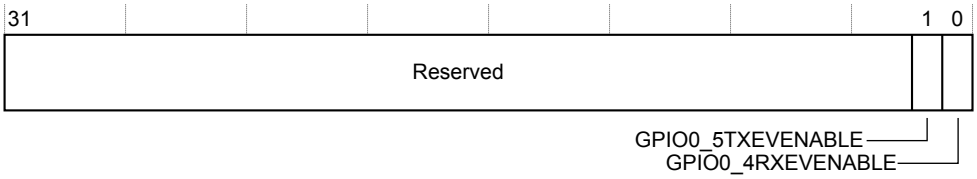

Figure 4-32 EVENTCFG Register bit assignments

The following table shows the bit assignments.

Table 4-37 EVENTCFG Register bit assignments

Bits	Name	Function
[31:2]	-	Reserved. Software that writes to this register must write all zeros to these bits. Software that reads this register must ignore these bits.
[1]	GPIO0_5TXEVENABLE	`0b0` No effect. `0b1` Enables GPIO0[5] TXEV.
[0]	GPIO0_4RXEVENABLE	`0b0` No effect. `0b1` Enables GPIO0[4] RXEV.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.33 PID4

The PID4 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

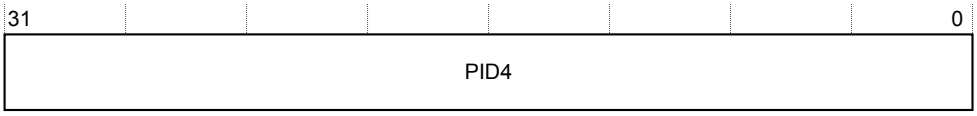

Figure 4-33 PID4 Register bit assignments

The following table shows the bit assignments.

Table 4-38 PID4 Register bit assignments

Bits	Name	Function
[31:0]	PID4	Peripheral ID 4 identification. The value in the Beetle test chip r0p0 is `0x0004`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.34 PID5

The PID5 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

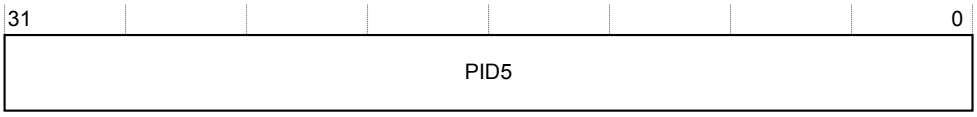

Figure 4-34 PID5 Register bit assignments

The following table shows the bit assignments.

Table 4-39 PID5 Register bit assignments

Bits	Name	Function
[31:0]	PID5	Peripheral ID 5 identification. The value in the Beetle test chip r0p0 is `0x0000`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.35 PID6

The PID6 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

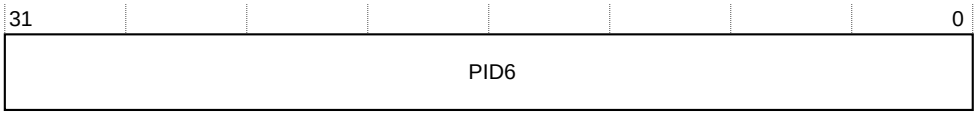

Figure 4-35 PID6 Register bit assignments

The following table shows the bit assignments.

Table 4-40 PID6 Register bit assignments

Bits	Name	Function
[31:0]	PID6	Peripheral ID 6 identification. The value in the Beetle test chip r0p0 is `0x0000`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.36 PID7

The PID7 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

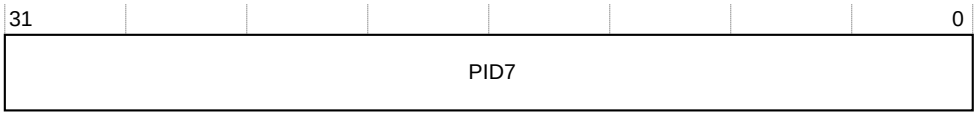

Figure 4-36 PID7 Register bit assignments

The following table shows the bit assignments.

Table 4-41 PID7 Register bit assignments

Bits	Name	Function
[31:0]	PID7	Peripheral ID 7 identification. The value in the Beetle test chip r0p0 is `0x0000`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.37 PID0

The PID0 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

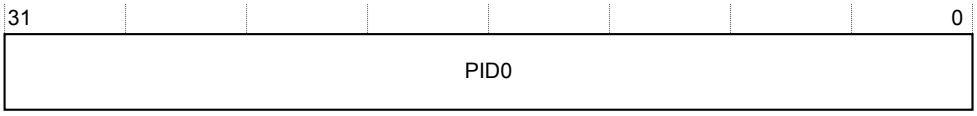

Figure 4-37 PID0 Register bit assignments

The following table shows the bit assignments.

Table 4-42 PID0 Register bit assignments

Bits	Name	Function
[31:0]	PID0	Peripheral ID 0 identification. The value in the Beetle test chip r0p0 is `0x0042`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.38 PID1

The PID1 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

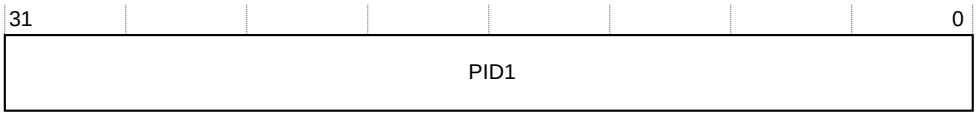

Figure 4-38 PID1 Register bit assignments

The following table shows the bit assignments.

Table 4-43 PID1 Register bit assignments

Bits	Name	Function
[31:0]	PID1	Peripheral ID 1 identification. The value in the Beetle test chip r0p0 is `0x00B7`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.39 PID2

The PID2 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

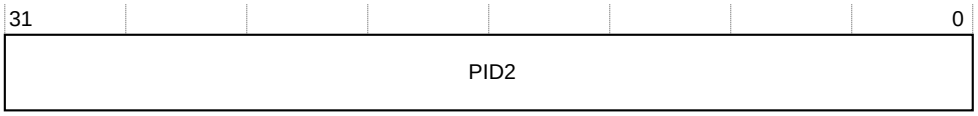

Figure 4-39 PID2 Register bit assignments

The following table shows the bit assignments.

Table 4-44 PID2 Register bit assignments

Bits	Name	Function
[31:0]	PID2	Peripheral ID 2 identification. The value in the Beetle test chip is `0x00rB` where r is the revision number.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.40 PID3

The PID3 Register characteristics are:

Purpose

Stores peripheral identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

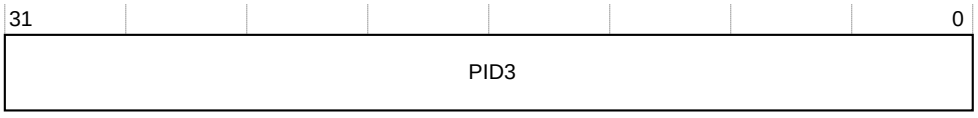

Figure 4-40 PID3 Register bit assignments

The following table shows the bit assignments.

Table 4-45 PID3 Register bit assignments

Bits	Name	Function
[31:0]	PID3	Peripheral ID 3 identification. The value in the Beetle test chip r0p0 is `0x0000`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.41 CID0

The CID0 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

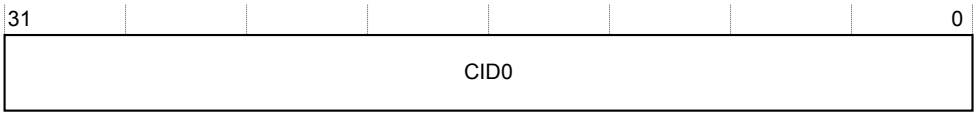

Figure 4-41 CID0 Register bit assignments

The following table shows the bit assignments.

Table 4-46 CID0 Register bit assignments

Bits	Name	Function
[31:0]	CID0	Component ID 0 identification. The value in the Beetle test chip r0p0 is `0x000D`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.42 CID1

The CID1 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

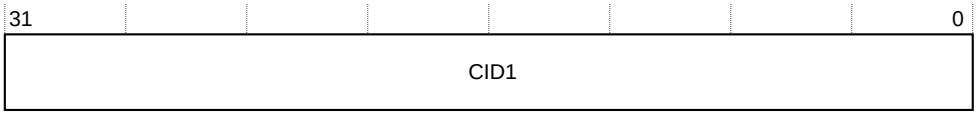

Figure 4-42 CID1 Register bit assignments

The following table shows the bit assignments.

Table 4-47 CID1 Register bit assignments

Bits	Name	Function
[31:0]	CID1	Component ID 1 identification. The value in the Beetle test chip r0p0 is `0x0010`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.43 CID2

The CID2 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

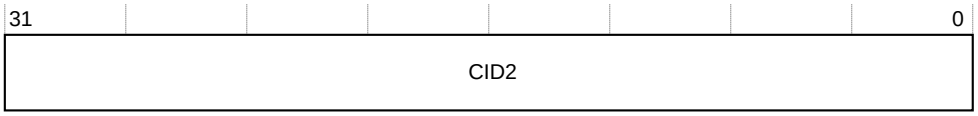

Figure 4-43 CID2 Register bit assignments

The following table shows the bit assignments.

Table 4-48 CID1 Register bit assignments

Bits	Name	Function
[31:0]	CID2	Component ID 2 identification. The value in the Beetle test chip r0p0 is `0x0005`.

Related concepts

4.7.1 System control register summary on page 4-63

4.7.44 CID3

The CID3 Register characteristics are:

Purpose

Stores component identification information.

Usage constraints

This register is read-only.

Configurations

Available in all V2M-Beetle evaluation board configurations.

The following figure shows the bit assignments.

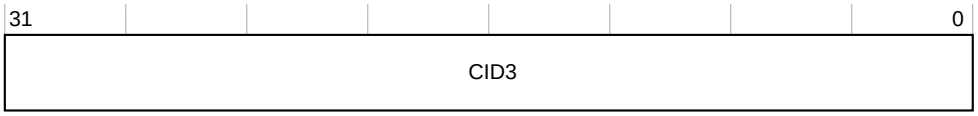

Figure 4-44 CID3 Register bit assignments

The following table shows the bit assignments.

Table 4-49 CID1 Register bit assignments

Bits	Name	Function
[31:0]	CID3	Component ID 3 identification. The value in the Beetle test chip r0p0 is `0x00B1`.

Related concepts

4.7.1 System control register summary on page 4-63