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Product status
The information in this document is Final, that is for a developed product.

Web address
http://www.arm.com
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Preface

This preface introduces the Arm® CoreLink™ DMC-620 Dynamic Memory Controller Technical Reference Manual.

It contains the following:

About this book

This book is for the Arm® CoreLink™ DMC-620 Dynamic Memory Controller.

Product revision status

The rmponder identifies the revision status of the product described in this book, for example, r1p2, where:

r  Identifies the major revision of the product, for example, r1.
p  Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced hardware engineers who want to integrate the delivered ARM System on Chip (SoC) product in a SoC design.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter describes the DMC-620.

Chapter 2 Functional description
This chapter describes how the DMC-620 operates.

Chapter 3 Programmers model
This chapter describes the programmers model of the DMC-620.

Appendix A Signal descriptions
This appendix describes the DMC-620 signals.

Appendix B Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm® Glossary for more information.

Typographic conventions

*italic*  Introduces special terminology, denotes cross-references, and citations.

**bold** Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

*monospace* Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

*monospace* **italic** Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

*monospace italic* Denotes arguments to monospace text where the argument is to be replaced by a specific value.

*monospace bold* Denotes language keywords when used outside example code.
Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <Crn>, <Crn>, <Opcode_2>
```

**Small caps**

Used in body text for a few terms that have specific technical meanings, that are defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

**Timing diagrams**

The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

![Figure 1 Key to timing diagram conventions](image)

**Signals**

The signal conventions are:

**Signal level**

The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW.

Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

**Lowercase n**

At the start or end of a signal name denotes an active-LOW signal.

**Additional reading**

This book contains information that is specific to this product. See the following documents for other relevant information.
Arm publications

- AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces (Arm IHI 0068).
- Arm®v8.2 RAS Architecture Extension Specification.

The following confidential books are only available to licensees:

- Arm® CoreLink™ DMC-620 Dynamic Memory Controller Configuration and Integration Manual (Arm 100569).
- Arm® CoreLink™ DMC-620 Dynamic Memory Controller Design Manual (Arm 100567).
- Arm® AMBA® 5 CHI Architecture Specification (Arm IHI 0050).

Other publications


Note

See the Arm® CoreLink™ DMC-620 Dynamic Memory Controller Release Note for the actual versions of the specifications that Arm used when designing the device.
Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:
- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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If you have comments on content then send an e-mail to errata@arm.com. Give:
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Chapter 1
Introduction

This chapter describes the DMC-620.

It contains the following sections:

• 1.1 About the product on page 1-12.
• 1.2 DMC-620 compliance on page 1-13.
• 1.3 Features on page 1-14.
• 1.4 Interfaces on page 1-15.
• 1.5 Configurable options on page 1-16.
• 1.6 Test features on page 1-17.
• 1.7 Product documentation and design flow on page 1-18.
• 1.8 Product revisions on page 1-20.
1.1 About the product

About the product is a high-level overview of the DMC-620.

The DMC-620 is an Arm AMBA 5 CHI SoC peripheral, developed, tested, and licensed by Arm. It is a high-performance, area-optimized memory controller that is compatible with the AMBA 5 CHI protocol.

It supports the following memory devices:
- *Double Data Rate 3* (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- *Double Data Rate 4* (DDR4) SDRAM.

The following figure shows an example system:

![Example system diagram](image)

**Figure 1-1 Example system**

The DMC-620 enables data transfer between the SoC and the SDRAM devices external to the chip. It connects to the on-chip system through a single CHI interface, and to a processor through the programmers APB3 interface to program the DMC-620. It connects to the SDRAM devices through its memory interface block and the *DDR PHY Interface* (DFI).
1.2 DMC-620 compliance

The DMC-620 is compatible with the following protocol specifications and standards:

- AMBA 5 CHI-A/CHI-B/CHI-C protocol.
- AMBA 3 APB protocol.
- JEDEC DDR4 JESD79-4 standard.
- JEDEC DDR3 JESD79-3 standard.
- JEDEC DDR3L JESD79-3-1 standard.
- JEDEC JESD82-29 standard.
- JEDEC LRDIMM DDR4 Data Buffer Specification.
- DDR4 RCD02 Specification.
- DDR4 SDRAM Registered DIMM Design Specification.
- DDR4 SDRAM Load Reduced DIMM Design Specification.
- DFI 3.1.
- DFI 4.0.
1.3 Features

The DMC-620 supports DDR3 and DDR4 SDRAMs. It also supports error checking, reliability, availability, and serviceability features. In addition, Quality of Service (QoS) features and Arm TrustZone® architecture security extensions are built in throughout the controller.

The DMC-620 has the following features:

- Profiling signals that enable performance profiling to be performed in the system.
- TrustZone architecture security extensions.
- Buffering to optimize read and write turnaround, and to maximize bandwidth.
- A System Interface (SI) that provides:
  - A CHI interface to connect to a CoreLink Cache Coherent Network (CCN) or a CoreLink Coherent Mesh Network (CMN).
  - An AMBA5 CHI interface supporting the CHI-A, CHI-B, and CHI-C architecture.
  - An APB interface for configuration and initialization.
  - An external performance event interface for connecting to CoreSight™ on-chip debug and trace technology.
  - A 128-bit or 256-bit CHI interface.
- A Memory Interface (MI) that provides:
  - A DFI 3.1 and 4.0 interface to a PHY that supports DDR3, DDR3L, and DDR4.
  - Support for 1:2 DFI frequency ratio mode.
  - Support for either a 32-bit wide data SDRAM interface or a 64-bit wide data SDRAM interface.
- Low-power operation through programmable SDRAM power modes.
- ARMv8.2 compatible Reliability, Availability, Serviceability (RAS):
  - Single Error Correcting, Double Error Detecting (SECDED) Error-Correcting Code (ECC) for off-chip DRAM.
  - Symbol-based ECC, to correct memory chip and data-lane failures.
  - SECDED ECC for on-chip RAM protection.
  - Supports ARMv8.2 end-to-end RAS protection, data poisoning, and deferment.
  - Hardware Read-Modify-Write (RMW) for systems supporting sparse writes.
  - Command-Address (CA) parity checks for DDR3 and DDR4 link faults.
  - CRC write-data protection for DDR4 devices.
- A programmable mechanism for automated SDRAM scrubbing.
- Error handling and automated recovery.
- Power Control Logic (PCL) that generates powerdown requests to the SDRAM, and manages power enablers for the PHY logic.
- 3DS support for 8H, 4H, and 2H devices.
- DDR4 Registered Dual In-line Memory Module (RDIMM) and Load-Reduced Dual In-line Memory Module (LRDIMM) support.
- Flexible Dual In-line Memory Module (DIMM) topology support:
  - Signal multiplexing that allows a single board layout to support different RDIMM device types (3DS or planer), and a different number of devices.
  - Support for RDIMM Encoded or Direct CS.
- Core to DMC Prefetch Hint direct path allowing the core to directly initiate a DMC prefetch.
- Configurable out-of-order request queue depth and symbol ECC logic.
1.4 Interfaces

This section lists the interfaces in the DMC-620.

The DMC-620 has the following external interfaces:

- A System interface to provide read and write access to or from a master that supports either the CHI-A, CHI-B, or CHI-C protocol.
- An APB3 programmers interface to program and control the DMC-620.
- A DFI-compatible PHY interface to transfer data to and from the external memory.
- A Profile and Debug interface.
- A Low-power clock control interface that uses the Q-Channel protocol. See Q-Channel interface on page 2-26.
- An Abort interface that is a four-phase request and acknowledge handshake. The Abort interface can be used to recover from a livelock when DRAM or PHY fails.
- User I/O ports.
- A set of interrupts that are used to report operational events and detected faults.
1.5 Configurable options

The DMC-620 has the following configurable options:

Table 1-1 Configurable options

<table>
<thead>
<tr>
<th>Option</th>
<th>Parameter</th>
<th>Default</th>
<th>Default value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHI-A, CHI-B, or CHI-C</td>
<td>DMC_CHIB, DMC_CHIC</td>
<td>CHIC</td>
<td>1</td>
<td>Configures an AMBA 5 CHI Protocol Specification CHI Issue A, CHI Issue B, or CHI Issue C.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note For CHI-C, both parameters CHI-B and CHI-C must be 1.</td>
</tr>
<tr>
<td>128-bit or 256-bit CHI-B interface</td>
<td>DMC_SYS_DATA_WIDTH</td>
<td>128</td>
<td>256</td>
<td>Valid in CHI-B only. Configures a 128-bit or 256-bit CHI interface.</td>
</tr>
<tr>
<td>Include Symbol ECC</td>
<td>DMC_SYM_ECC</td>
<td>Yes</td>
<td>1</td>
<td>Includes logic for Symbol ECC. Symbol ECC is only supported with a x64 DRAM interface.</td>
</tr>
<tr>
<td>Queue depth</td>
<td>DMC_QUEUE_DEPTH</td>
<td>128</td>
<td>128</td>
<td>Can select a depth of 64 or 128.</td>
</tr>
</tbody>
</table>

Note

- If Symbol ECC is excluded from the configuration, you must ensure the err0ctlr_ecc field is never set to 2.
- If the DMC is configured for a CHI-A interconnect, you must ensure the err0ctlr_cpi and err0ctlr_cdi fields are set to ignore the CHI-B Data Byte Parity (DBP) and poison bits.
1.6 Test features

The DMC-620 provides the following test features:

• Integration test logic for integration testing.
• A debug and profile interface to enable you to monitor transaction events.
1.7 Product documentation and design flow

This section describes the DMC-620 books and how they relate to the design flow.

Documentation

The DMC-620 documentation is as follows:


The Technical Reference Manual (TRM) summarizes the functionality of the DMC, and describes its signals.

The TRM is a non-confidential book available to the public.

Design Manual

The Design Manual (DM) describes the functionality and the effects of functional options on the behavior of the DMC. It is required at all stages of the design flow. The choices that are made in the design flow mean that some behavior that is described in the DM is not relevant. If you are programming the DMC, then contact:

• The implementer to determine what integration, if any, was performed before implementing the DMC.
• The integrator to determine the pin configuration of the device that you are using.

The DM is a confidential book that is only available to licensees.

Configuration and Integration Manual

The Configuration and Integration Manual (CIM) describes how to integrate the DMC into a SoC. The CIM includes a description of the signals that the integrator must tie off to connect the DMC into an SoC design or to other IP.

The CIM describes:

• How to synthesize the Register Transfer Level (RTL).
• How to integrate RAM arrays.
• How to run test patterns.
• The processes to sign off the configured design.

The Arm product deliverables include reference scripts and information about using them to implement your design. Contact your EDA vendor for EDA tool support.

The CIM is a confidential book that is only available to licensees.

Design flow

The DMC-620 is delivered as synthesizable RTL. Before it can be used in a product, it must go through the following processes:

Implementation

The implementer synthesizes the RTL to produce a hard macrocell. This stage includes integrating RAMs into the design.

Integration

The integrator connects the implemented design into a SoC. This stage includes connecting it to a memory system.

Programming

The system programmer develops the software that is required to initialize the DMC, and tests the required application software.

Each process:

• Can be performed by a different party.
• Can include implementation and integration choices that affect the behavior and features of the DMC.
The operation of the final device depends on:

**Configuration inputs**

The integrator configures some features of the DMC by tying inputs to specific values. These configurations affect the start-up behavior before any software configuration is made. They can also limit the options available to the software.

**Software programming**

The programmer configures the DMC by programming particular values into registers. This stage affects the behavior of the DMC.

---

**Note**

This manual refers to implementation-defined features. Reference to a feature that is included means that the appropriate signal configuration options are selected. Reference to an enabled feature means one that has also been configured by software.
1.8 Product revisions

This section describes the differences in functionality between product revisions of the DMC-620.

- **r0p0** First release.
- **r0p0-r1p0** The functional changes are:
  - Incorrect VREF DQ training behavior fixed.
  - CHI-C support added.
Chapter 2

Functional description

This chapter describes how the DMC-620 operates.

It contains the following sections:

- 2.1 About the functions on page 2-22.
- 2.2 Clocking and resets on page 2-24.
- 2.3 Interfaces on page 2-25.
- 2.4 Constraints and limitations of use on page 2-28.
2.1 About the functions

This section gives a brief description of all the functions of the DMC-620.

The following figure shows a block diagram of the functions of the DMC-620. The colors show the different categories of functions:

- Blue indicates the blocks that are associated with data flow. The System interface is an example.
- Green indicates the blocks that are associated with programming. The Programming interface is an example.
- Orange indicates the blocks that are associated with the quality and efficiency of the communication to external memory. The QoS engine is an example.

![DMC functional block diagram](image)

**System Interface**

The DMC-620 interfaces to the rest of the SoC through the System interface. This interface connects to a CHI Slave Node (SN-F) interface. For any attempted accesses that the system makes outside of the programmed address range, the System interface responds with a *Non-data Error* (NDERR) response. Depending on how you program the DMC-620, it converts the system access information to the correct rank, bank, column, and row access of the external SDRAM. The System interface supports TrustZone features to regulate Secure and Non-secure accesses to both Secure and Non-secure regions of memory.

The DMC monitors queue occupancies and dictates whether system requests of any given QoS are accepted. Prefetched and Dynamic P-Credit requests are allocated based on a threshold setting, which is derived from register settings.

**Note**

There is no support for exclusive access in the DMC because the CoreLink CCN-5xx and CMN-6xx products support exclusive access requests in the *Home Node* (HN-F).
Memory channel
Through this interface, the DMC-620 conducts data transactions with the SDRAM and regulates the power consumption of the SDRAM. The DMC-620 uses the ECC information that it receives from the SDRAM to maximize the reliability from these devices.

Programming interface
Through this interface, a master in the system programs the DMC-620. You can define the Secure and Non-secure regions of external memory. You can also define how the DMC-620 addresses the external memory from the address that the system provides on its System interface. You can also make direct accesses to the SDRAM, for example to initialize it.

QoS engine
The DMC-620 provides controls to enable you to adjust its arbitration scheme for your system to maximize the availability of your external memory devices. It provides buffers to reorder system transaction requests. It uses an advanced scheduling algorithm to ensure that traffic going to one memory bank causes minimal disruption to traffic going to a different memory bank. It also schedules transaction requests according to the availability of the destination memory bank. For system access requests to different available memory banks, the DMC-620 arbitrates these requests using the QoS priority initially, and then the temporal priority. The memory access requests all compete for control of the external SDRAM bus and SDRAM bank.

RAS
RAS features include support for the following:
• V8.2 RAS Extension compliant.
• Supports end-to-end RAS protection, data poisoning, and deferment.
• SECDED ECC and symbol-based ECC for external DRAM. The symbol-based ECC performs quad-symbol correct and multi-symbol detect.
• SECDED ECC of on-chip SRAM buffers within the DMC-620.
• An automated retry of failed read transactions.
• Write-back of corrected errors.
• To improve containment of faults, the DMC-620 supports:
  — Link error protection for the memory interface, including automated hardware recovery for system memory access, training, and other hardware operations.
  — Programmable data scrubbing. The DMC-620 periodically detects and corrects data errors in the memory autonomously.
2.2 Clocking and resets

The DMC-620 normally operates as one synchronous clock domain between the interconnect and the external DDR interface. However, the Programming interface can operate asynchronously to this.

This section shows the clock and reset signals that the DMC-620 requires.

Clocks

The DMC-620 has three clock inputs:

- *clk*  
  *clk* is the main DMC clock that runs at SDRAM clock frequency. It must run synchronous to, and at the same frequency, as the CHI interface. If the CHI interconnect is not running at SDRAM clock frequency, then an asynchronous bridge such as the CCN Device Source Synchronous Bridge (DSSB) must be used.

- *clkdiv2*  
  This clock runs the DFI interface and connects to both the DMC and the PHY. It must be edge synchronous to *clk* and run at half the *clk* frequency.

- *pclk*  
  *pclk* can run asynchronously to *clk* and *clkdiv2*.

Reset

Resets must be applied for a minimum duration of 16 clock cycles for each clock domain.

There are two reset inputs. *RESETn* resets both *clk* and the *clkdiv2* registers and *PRESETn* resets the *pclk* registers. The *pclk* domain must be out of reset before the *clk* and *clkdiv2* domains.

——— Note ———

- To assert any DMC-620 reset signal, you must set it LOW.
- To perform a DMC-620 reset, you must assert both reset signals.
2.3 Interfaces

This section describes the interfaces of the DMC-620, as the following figure shows.

![Interface Diagram](image)

This section contains the following subsections:

- **2.3.1 System interface** on page 2-25.
- **2.3.2 Programming interface** on page 2-25.
- **2.3.3 PHY interface** on page 2-25.
- **2.3.4 Low-power clock control interface** on page 2-26.
- **2.3.5 Abort interface** on page 2-26.

### 2.3.1 System interface

This section describes the function of the System interface.

The System interface provides protocol conversion between CHI and internal read/write requests. Because CHI is packet-based, and a slave node only supports read and write semantics, this translation is straightforward at a transaction level because no transformation function is performed.

### 2.3.2 Programming interface

This section describes the APB3 interface, which is used for programming the DMC-620.

The AMBA APB3 slave interface allows software to configure the controller and to initialize the memory devices. The APB3 programming interface also provides a means of performing architectural state transitions in addition to querying certain debug and profile information. The APB3 interface is a memory-mapped register interface.

### 2.3.3 PHY interface

The PHY interface provides command scheduling and arbitration, including the generation of any required SDRAM prepare commands, for example, ACTIVATE and PRECHARGE.

The PHY interface is compatible with the DDR standards for DDR4 and DDR3 (including DDR3L). It provides:
- Command scheduling and arbitration.
- Automated AUTOREFRESH command generation.
- SDRAM interface link protection including automated retries for failed commands to ensure the correct ordering of those retried commands to SDRAM.
• Automated SDRAM and PHY logic power control.
• Profile and debug information.
• Support for 1:2 frequency ratio mode.

2.3.4 Low-power clock control interface

This section describes the clock requirements for the DMC-620.

The DMC-620 provides a Low-power control interface using the Q-Channel protocol. The Low-power control interface is used to place the DMC into its low-power state, where the clock can be removed. The system can use the APB interface to put the DMC into its low-power state, and take it out of its low-power state.

Q-Channel interface

The DMC has a Q-Channel interface that allows an external power controller to place the DMC into a low-power state.

It is a standard Q-Channel interface as defined in the AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces using the following signals:

• qactive.
• qreqn.
• qacceptn.
• qdeny.

When the DMC receives a request, it puts the DRAM into self_refresh before asserting qacceptn to accept the request that indicates the clk can be stopped.

The DMC denies requests to power down using the Q-Channel when geardown_mode is enabled. In this case, low-power mode can still be entered using the APB interface.

There is a separate Q-Channel interface for the pclk using the following signals:

• qactive_apb.
• qreqn_apb.
• qacceptn_apb.
• qdeny_apb.

The DMC never denies a request to power down the APB clock although it might be delayed based on APB activity.

Note

These two interfaces are interrelated and a change on one can cause qactive on the other to be asserted. If this occurs, then the powerup request must be responded to in a timely fashion to allow the request to be serviced.

See the AMBA® Low Power Interface Specification, Arm® Q-Channel and P-Channel Interfaces.

2.3.5 Abort interface

When a fault is detected on the DFI interface, it causes repeated retries of commands on the memory interface. The Abort interface is a 4-phase request and acknowledge handshake. The DMC can use this interface to recover from a livelock that is caused by a DRAM failure or a PHY failure.

The following diagram shows the request, acknowledge handshake:
The system can issue an abort at any time, which puts the DMC into the ABORT architectural state. Software must then restore the memory state. All current system transactions are retried after software restores the memory state and puts the DMC back into the READY state.

The Abort interface has the payload signal `abort_err_type` as an input to the DMC, which the DMC outputs as `dfi_disconnect_error` on the DFI interface during an abort sequence. Any PHY training that is in progress gets aborted and the DMC indicates to the PHY the error type through `dfi_disconnect_error`.

Figure 2-4  Abort interface timing diagram
2.4 Constraints and limitations of use

The constraints and limitations of the DMC-620 depend on the SDRAMs used, and the interoperability within the PHYs. Which in turn, depends on the DDR Physical Interface (DFI) parameters.

The SDRAMs supported by the DMC-620 are:

- Double Data Rate 3 (DDR3) SDRAM.
- Low-voltage DDR3 SDRAM.
- Double Data Rate 4 (DDR4) SDRAM.

Note

These devices are described in the JEDEC specifications that are global standards for the microelectronics industry.

The DIMMs supported by the DMC-620 are:

- DDR3 UDIMM.
- DDR4 UDIMM.
- DDR4 RDIMM.
- DDR4 LRDIMM.
- DDR4 3DS. DIMMs utilizing 3DS parts are supported.

The JEDEC specification implies the following constraints and must be met:

1. **t_xp < t_xsr** - Exiting power down timing must be less than self-refresh exit.
2. **t_mrw_cs < t_mrw** - The delay after a Mode Register Write command and before any other command is issued to a different rank. This delay must be less than the delay applied after a Mode Register Write command and before any other command is issued to the same rank.
Chapter 3
Programmers model

This chapter describes the programmers model of the DMC-620.

It contains the following sections:
• 3.1 About this programmers model on page 3-30.
• 3.2 Register descriptions on page 3-31.
• 3.3 Register summary on page 3-32.
3.1 About this programmers model

The following information applies to the dmc620 registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to the reset value specified in the 3.3 Register summary on page 3-32
- Access type is described as follows:
  - RW     Read and write.
  - RO     Read only.
  - WO     Write only.
3.2 Register descriptions

This section describes the dmc620 registers.

3.3 Register summary on page 3-32 provides cross references to individual registers.
### 3.3 Register summary

The following table shows the registers in offset order from the base memory address.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x000</td>
<td>memc_status</td>
<td>RO</td>
<td>0x00000000</td>
<td>32</td>
<td>3.3.1 memc_status on page 3-51</td>
</tr>
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<td>memc_config</td>
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<td>memc_cmd</td>
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<td>RW</td>
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<td>decode_control_next</td>
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<td>format_control</td>
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<td>Name</td>
<td>Type</td>
<td>Reset</td>
<td>Width</td>
<td>Description</td>
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<td>Type</td>
<td>Reset</td>
<td>Width</td>
<td>Description</td>
</tr>
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<td>32</td>
<td>3.3.488 phymstr_control_now on page 3-205</td>
</tr>
</tbody>
</table>
### Table 3-1 Register summary (continued)

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1FD</td>
<td>periph_id_4</td>
<td>RO</td>
<td>0x00000014</td>
<td>32</td>
<td>3.3.489 periph_id_4 on page 3-205</td>
</tr>
<tr>
<td>0x1FE</td>
<td>periph_id_0</td>
<td>RO</td>
<td>0x000000054</td>
<td>32</td>
<td>3.3.490 periph_id_0 on page 3-205</td>
</tr>
<tr>
<td>0x1FE</td>
<td>periph_id_1</td>
<td>RO</td>
<td>0x00000084</td>
<td>32</td>
<td>3.3.491 periph_id_1 on page 3-206</td>
</tr>
<tr>
<td>0x1FE</td>
<td>periph_id_2</td>
<td>RO</td>
<td>0x00000008</td>
<td>32</td>
<td>3.3.492 periph_id_2 on page 3-206</td>
</tr>
<tr>
<td>0x1FE</td>
<td>periph_id_3</td>
<td>RO</td>
<td>0x00000000</td>
<td>32</td>
<td>3.3.493 periph_id_3 on page 3-206</td>
</tr>
<tr>
<td>0x1F0</td>
<td>component_id_0</td>
<td>RO</td>
<td>0x00000000</td>
<td>32</td>
<td>3.3.494 component_id_0 on page 3-206</td>
</tr>
<tr>
<td>0x1F4</td>
<td>component_id_1</td>
<td>RO</td>
<td>0x000000F0</td>
<td>32</td>
<td>3.3.495 component_id_1 on page 3-207</td>
</tr>
<tr>
<td>0x1F8</td>
<td>component_id_2</td>
<td>RO</td>
<td>0x00000005</td>
<td>32</td>
<td>3.3.496 component_id_2 on page 3-207</td>
</tr>
<tr>
<td>0x1FC</td>
<td>component_id_3</td>
<td>RO</td>
<td>0x00000081</td>
<td>32</td>
<td>3.3.497 component_id_3 on page 3-207</td>
</tr>
</tbody>
</table>

#### 3.3.1 memc_status

Holds the architectural status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc_status register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x000
  - Type: Read-only
  - Reset: 0x00000000
  - Width: 32

#### 3.3.2 memc_config

Holds the configuration data for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The memc_config register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x004
3.3.3  memc_cmd

Used to change the architectural state of the DMC, or execute queued manager operations. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The memc_cmd register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x008
- Type Write-only
- Reset 0x00000000
- Width 32

3.3.4  address_control_next

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x010
- Type Read-write
- Reset 0x0030202
- Width 32

3.3.5  decode_control_next

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, ie. row_order != bank_order != rank_order. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The decode_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x014
- Type Read-write
- Reset 0x001A3000
3.3.6 format_control

Configures the memory burst access parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The format_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x018
- Type: Read-write
- Reset: 0x12000113
- Width: 32

3.3.7 address_map_next

Configures the system address mapping options. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_map_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x01C
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.8 low_power_control_next

Configures the low-power features of the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The low_power_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x020
- Type: Read-write
- Reset: 0x00000020
- Width: 32

3.3.9 turnaround_control_next

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The turnaround_control_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset** 0x028
- **Type** Read-write
- **Reset** 0xF0F0F0F0
- **Width** 32

### 3.3.10 hit_turnaround_control_next

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The hit_turnaround_control_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset** 0x02C
- **Type** Read-write
- **Reset** 0x08909FBF
- **Width** 32

### 3.3.11 qos_class_control_next

Configures the priority class for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The qos_class_control_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset** 0x030
- **Type** Read-write
- **Reset** 0x00000FC8
- **Width** 32

### 3.3.12 escalation_control_next

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The escalation_control_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.
Attributes
    Offset  0x034
    Type    Read-write
    Reset   0x00000000
    Width   32

3.3.13  qv_control_31_00_next
Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The qv_control_31_00_next register characteristics are:
Usage constraints
    There are no usage constraints.
Configurations
    There is only one DMC configuration.
Attributes
    Offset  0x038
    Type    Read-write
    Reset   0x76543210
    Width   32

3.3.14  qv_control_63_32_next
Configures the priority settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The qv_control_63_32_next register characteristics are:
Usage constraints
    There are no usage constraints.
Configurations
    There is only one DMC configuration.
Attributes
    Offset  0x03C
    Type    Read-write
    Reset   0xFEDCBA98
    Width   32

3.3.15  rt_control_31_00_next
Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The rt_control_31_00_next register characteristics are:
Usage constraints
    There are no usage constraints.
Configurations
    There is only one DMC configuration.
Attributes
    Offset  0x040
    Type    Read-write
    Reset   0x00000000
### 3.3.16 rt_control_63_32_next

Configures the timeout settings for each QoS encoding. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rt_control_63_32_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x044
- Type: Read-write
- Reset: 0x00000000
- Width: 32

### 3.3.17 timeout_control_next

Configures the prescaler applied to timeout values. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The timeout_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x048
- Type: Read-write
- Reset: 0x00000001
- Width: 32

### 3.3.18 credit_control_next

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The credit_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x04C
- Type: Read-write
- Reset: 0x00000F03
- Width: 32

### 3.3.19 write_priority_control_31_00_next

Configures the priority settings for write requests within the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The write_priority_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x050</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.20 write_priority_control_63_32_next

Configures the priority settings for write requests within the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The write_priority_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x054</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.21 queue_threshold_control_31_00_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue_threshold_control_31_00_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x058</td>
<td>Read-write</td>
<td>0x00000008</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.22 queue_threshold_control_63_32_next

Configures the threshold settings for requests in the DMC Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The queue_threshold_control_63_32_next register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.
Attributes
  Offset  0x05C
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.23  address_shutter_31_00_next
 Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
 Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_31_00_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x060
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.24  address_shutter_63_32_next
 Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
 Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_63_32_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x064
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.25  address_shutter_95_64_next
 Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW
 Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_95_64_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x068
  Type    Read-write
  Reset   0x00000000
3.3.26 address_shutter_127_96_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_127_96_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x06C
Type Read-write
Reset 0x00000000
Width 32

3.3.27 address_shutter_159_128_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_159_128_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x070
Type Read-write
Reset 0x00000000
Width 32

3.3.28 address_shutter_191_160_next

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The address_shutter_191_160_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x074
Type Read-write
Reset 0x00000000
Width 32

3.3.29 memory_address_max_31_00_next

Configures the address space control for the DMC default region. Applies post address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The memory_address_max_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x078
- Type Read-write
- Reset 0x00000010
- Width 32

3.3.30 memory_address_max_47_32_next

Configures the address space control for the DMC default region. Applies post address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory_address_max_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x07C
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.31 access_address_min0_31_00_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min0_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x080
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.32 access_address_min0_47_32_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min0_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
Attributes

Offset   0x084
Type     Read-write
Reset    0x00000000
Width    32

3.3.33    access_address_max0_31_00_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max0_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset   0x088
Type     Read-write
Reset    0x00000000
Width    32

3.3.34    access_address_max0_47_32_next

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max0_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset   0x08C
Type     Read-write
Reset    0x00000000
Width    32

3.3.35    access_address_min1_31_00_next

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min1_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset   0x090
Type     Read-write
Reset    0x00000000
3.3.36 **access_address_min1_47_32_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min1_47_32_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x094
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.37 **access_address_max1_31_00_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max1_31_00_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x098
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.38 **access_address_max1_47_32_next**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max1_47_32_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x09C
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.39 **access_address_min2_31_00_next**

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The access_address_min2_31_00_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0A0
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.40 access_address_min2_47_32_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min2_47_32_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0A4
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.41 access_address_max2_31_00_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max2_31_00_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0A8
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.42 access_address_max2_47_32_next

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max2_47_32_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.
Attributes
Offset  0x0AC
Type    Read-write
Reset   0x00000000
Width   32

3.3.43 access_address_min3_31_00_next
Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min3_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x0B0
Type    Read-write
Reset   0x00000000
Width   32

3.3.44 access_address_min3_47_32_next
Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min3_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x0B4
Type    Read-write
Reset   0x00000000
Width   32

3.3.45 access_address_max3_31_00_next
Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max3_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x088
Type    Read-write
Reset   0x00000000
3.3.46 access_address_max3_47_32_next

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max3_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0BC
Type Read-write
Reset 0x00000000
Width 32

3.3.47 access_address_min4_31_00_next

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min4_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0C0
Type Read-write
Reset 0x00000000
Width 32

3.3.48 access_address_min4_47_32_next

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min4_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0C4
Type Read-write
Reset 0x00000000
Width 32

3.3.49 access_address_max4_31_00_next

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The access_address_max4_31_00_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0C8
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.50 access_address_max4_47_32_next

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max4_47_32_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0CC
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.51 access_address_min5_31_00_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min5_31_00_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x0D0
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.52 access_address_min5_47_32_next

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min5_47_32_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.
Attributes
  Offset  0x004
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.53  access_address_max5_31_00_next
This register configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max5_31_00_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x008
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.54  access_address_max5_47_32_next
This register configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max5_47_32_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x0C
  Type    Read-write
  Reset   0x00000000
  Width   32

3.3.55  access_address_min6_31_00_next
This register configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min6_31_00_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x0E0
  Type    Read-write
  Reset   0x00000000
Width 32

3.3.56 access_address_min6_47_32_next

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min6_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0E4
Type Read-write
Reset 0x00000000
Width 32

3.3.57 access_address_max6_31_00_next

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max6_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0E8
Type Read-write
Reset 0x00000000
Width 32

3.3.58 access_address_max6_47_32_next

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max6_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0EC
Type Read-write
Reset 0x00000000
Width 32

3.3.59 access_address_min7_31_00_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The access_address_min7_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0F0
Type Read-write
Reset 0x00000000
Width 32

3.3.60 access_address_min7_47_32_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_min7_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0F4
Type Read-write
Reset 0x00000000
Width 32

3.3.61 access_address_max7_31_00_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max7_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x0F8
Type Read-write
Reset 0x00000000
Width 32

3.3.62 access_address_max7_47_32_next

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The access_address_max7_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
Attributes

Offset 0x0FC
Type Read-write
Reset 0x00000000
Width 32

3.3.63 channel_status

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel_status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x100
Type Read-only
Reset 0x00000003
Width 32

3.3.64 channel_status_63_32

Holds the current status of the memory channel. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The channel_status_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x104
Type Read-only
Reset 0x00000000
Width 32

3.3.65 direct_addr

Sets the direct command address field for direct commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The direct_addr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x108
Type Read-write
Reset 0x00000000
3.3.66  **direct_cmd**

Generates direct commands from the manager. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG, PAUSED or READY states.

The direct_cmd register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x10C
- Type: Write-only
- Reset: 0x00000000
- Width: 32

3.3.67  **dci_replay_type_next**

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dci_replay_type_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x110
- Type: Read-write
- Reset: 0x00000002
- Width: 32

3.3.68  **direct_control_next**

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The direct_control_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x114
- Type: Read-write
- Reset: 0x0003FFFF
- Width: 32
3.3.69  **dci_strb**

Configures the write data strobe values used during direct_cmd WRITE operations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG, PAUSED or READY states.

The dci_strb register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

- Offset: 0x118
- Type: Read-write
- Reset: 0x0000000F
- Width: 32

3.3.70  **dci_data**

Reading from this register location returns read data received a result of a READ command. Writing to this register location sets the data to be used for direct_cmd WRITE commands. You must read or write once for each 32-bit data word of a DRAM burst. Access restrictions: RW Can be read from when in CONFIG, PAUSED or READY states. Can be written to when in CONFIG, PAUSED or READY states.

The dci_data register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

- Offset: 0x11C
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.71  **refresh_control_next**

Configures the type of refresh commands issued by the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The refresh_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

- Offset: 0x120
- Type: Read-write
- Reset: 0x00000000
- Width: 32
3.3.72 memory_type_next

Configures the DMC for the attached memory type. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The memory_type_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x128
- Type Read-write
- Reset 0x00000101
- Width 32

3.3.73 feature_config

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The feature_config register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x130
- Type Read-write
- Reset 0x000018E0
- Width 32

3.3.74 nibble_failed_031_000

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_031_000 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x138
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.75 nibble_failed_063_032

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_063_032 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x13C
Type Read-write
Reset 0x00000000
Width 32

3.3.76  nibble_failed_095_064

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_095_064 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x140
Type Read-write
Reset 0x00000000
Width 32

3.3.77  nibble_failed_127_096

Used to inform the DMC that a particular nibble has failed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The nibble_failed_127_096 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x144
Type Read-write
Reset 0x00000000
Width 32

3.3.78  queue_allocate_control_031_000

Used to inform the DMC that a particular queue (RAM) entry has failed, where 0 means failed and not included for allocation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_031_000 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.79  queue_allocate_control_063_032

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_063_032 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x148
Type Read-write
Reset 0xFFFFFFFF
Width 32

3.3.80  queue_allocate_control_095_064

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_095_064 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x14C
Type Read-write
Reset 0xFFFFFFFF
Width 32

3.3.81  queue_allocate_control_127_096

Configures the DMC to not allocate particular queue entries (one bit per entry), for example to avoid using faulty internal RAM locations. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The queue_allocate_control_127_096 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x150
Type Read-write
Reset 0xFFFFFFFF
Width 32
### 3.3.82 link_err_count

Counter register for link errors. The counter increments on detection of a new link error (dfi_alert_n or dfi_err). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The link_err_count register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x16C
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.83 scrub_control0_next

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_control0_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x170
- **Type**: Read-write
- **Reset**: 0xFFFFF00
- **Width**: 32

### 3.3.84 scrub_address_min0_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_min0_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x174
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32
3.3.85  **scrub_address_max0_next**

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_max0_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x178</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.86  **scrub_address_current0**

Current scrub address for scrub 0. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub_address_current0 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x17C</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.87  **scrub_control1_next**

Scrub engine channel control register. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_control1_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x180</td>
<td>Read-write</td>
<td>0x0FFFFF00</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.88  **scrub_address_min1_next**

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_min1_next register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x184
Type Read-write
Reset 0x00000000
Width 32

3.3.89 scrub_address_max1_next

Configures the address space control for the scrub engine channel. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The scrub_address_max1_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x188
Type Read-write
Reset 0x00000000
Width 32

3.3.90 scrub_address_current1

Current scrub address for scrub 1. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The scrub_address_current1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x18C
Type Read-only
Reset 0x00000000
Width 32

3.3.91 cs_remap_control_31_00_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.92 cs_remap_control_63_32_next
Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_63_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1A0
Type Read-write
Reset 0x00020001
Width 32

3.3.93 cs_remap_control_95_64_next
Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_95_64_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1A4
Type Read-write
Reset 0x00080004
Width 32

3.3.94 cs_remap_control_127_96_next
Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cs_remap_control_127_96_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1A8
Type Read-write
Reset 0x00200010
Width 32
3.3.95 **cid_remap_control_31_00_next**

Control register for dfi_CID remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid_remap_control_31_00_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1B0
- **Type**: Read-write
- **Reset**: 0x20001000
- **Width**: 32

3.3.96 **cid_remap_control_63_32_next**

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cid_remap_control_63_32_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1B4
- **Type**: Read-write
- **Reset**: 0x00004000
- **Width**: 32

3.3.97 **cke_remap_control_next**

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The cke_remap_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1C0
- **Type**: Read-write
- **Reset**: 0x76543210
- **Width**: 32

3.3.98 **rst_remap_control_next**

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rst_remap_control_next register characteristics are:
Usage constraints
    There are no usage constraints.

Configurations
    There is only one DMC configuration.

Attributes
    Offset  0x1C4
    Type    Read-write
    Reset   0x76543210
    Width   32

3.3.99  ck_remap_control_next

Control register for CKE remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The ck_remap_control_next register characteristics are:

Usage constraints
    There are no usage constraints.

Configurations
    There is only one DMC configuration.

Attributes
    Offset  0x1C8
    Type    Read-write
    Reset   0x76543210
    Width   32

3.3.100  power_group_control_31_00_next

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke_remap_control register should belong to the same power-group Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_31_00_next register characteristics are:

Usage constraints
    There are no usage constraints.

Configurations
    There is only one DMC configuration.

Attributes
    Offset  0x1D0
    Type    Read-write
    Reset   0x00020001
    Width   32

3.3.101  power_group_control_63_32_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_63_32_next register characteristics are:

Usage constraints
    There are no usage constraints.

Configurations
    There is only one DMC configuration.

Attributes
3.3.102 power_group_control_95_64_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_95_64_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1D8
Type Read-write
Reset 0x00000010
Width 32

3.3.103 power_group_control_127_96_next

Control register for CS remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The power_group_control_127_96_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1DC
Type Read-write
Reset 0x00000040
Width 32

3.3.104 phy_rdwrdata_cs_mask_31_00

Maps a logical rank to the physical rank phy_rdwrdata_cs output pins. Using this register it is possible to map a logical rank to multiple phy_rdwrdata_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_rdwrdata_cs_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1E0
Type Read-write
Reset 0xF7FBFDFF
3.3.105 phy_rdwrdata_cs_mask_63_32

Maps a logical rank to the physical rank phy_rdwrdata_cs output pins. Using this register it is possible to map a logical rank to multiple phy_rdwrdata_cs output pins. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_rdwrdata_cs_mask_63_32 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1E4
- Type: Read-write
- Reset: 0x7FBFDFEF
- Width: 32

3.3.106 phy_request_cs_remap

Maps PHY training request from a physical chip select to DMC internal logical chip select. Requests which are mapped using this register are dfi_rdlvl_cs, dfi_rdlvl_gate_cs, dfi_wrlvl_cs, dfi_phylvl_req_cs_n and dfi_phymstr_cs_state. The default settings are a 1:1 logical to physical rank mapping. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_request_cs_remap register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1E8
- Type: Read-write
- Reset: 0x76543210
- Width: 32

3.3.107 feature_control_next

Control register for DMC features. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The feature_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1F0
- Type: Read-write
- Reset: 0x0AA00000
- Width: 32
3.3.108  mux_control_next

Control muxing options for the DMC. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The mux_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1F4
Type Read-write
Reset 0x00000000
Width 32

3.3.109  rank_remap_control_next

Control register for rank remap. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rank_remap_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1F8
Type Read-write
Reset 0x76543210
Width 32

3.3.110  t_refi_next

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_refi_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x200
Type Read-write
Reset 0x00090100
Width 32

3.3.111  t_rfc_next

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The \texttt{t_rfc_next} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}
\begin{itemize}
  \item \textbf{Offset} \quad \texttt{0x204}
  \item \textbf{Type} \quad \text{Read-write}
  \item \textbf{Reset} \quad \texttt{0x00008C23}
  \item \textbf{Width} \quad 32
\end{itemize}

\textbf{3.3.112 \texttt{t_mrr_next}}
Configures the \texttt{tMRR} timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{t_mrr_next} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}
\begin{itemize}
  \item \textbf{Offset} \quad \texttt{0x208}
  \item \textbf{Type} \quad \text{Read-write}
  \item \textbf{Reset} \quad \texttt{0x00000002}
  \item \textbf{Width} \quad 32
\end{itemize}

\textbf{3.3.113 \texttt{t_mrw_next}}
Configures the \texttt{tMRW} timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{t_mrw_next} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}
\begin{itemize}
  \item \textbf{Offset} \quad \texttt{0x20C}
  \item \textbf{Type} \quad \text{Read-write}
  \item \textbf{Reset} \quad \texttt{0x0000000C}
  \item \textbf{Width} \quad 32
\end{itemize}

\textbf{3.3.114 \texttt{refresh_enable_next}}
Configures refresh counters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{refresh_enable_next} register characteristics are:
Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x210
  Type    Read-write
  Reset   0x00000001
  Width   32

3.3.115  t_rcd_next

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rcd_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x218
  Type    Read-write
  Reset   0x00000005
  Width   32

3.3.116  t_ras_next

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ras_next register characteristics are:

Usage constraints
  There are no usage constraints.

Configurations
  There is only one DMC configuration.

Attributes
  Offset  0x21C
  Type    Read-write
  Reset   0x0000000E
  Width   32

3.3.117  t_rp_next

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rp_next register characteristics are:

Usage constraints
  There are no usage constraints.
3.3.118  t_rpall_next

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rpall_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x220
- Type: Read-write
- Reset: 0x00000005
- Width: 32

3.3.119  t_rrd_next

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rrd_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x224
- Type: Read-write
- Reset: 0x00000005
- Width: 32

3.3.120  t_act_window_next

Configures the tFAW and tMAWi timing parameters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_act_window_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
3.3.121 t_rtr_next
Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), different chip-selects (t_rtr_cs), and same chip, different logical rank(t_rtr_dlr). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtr_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x22C
Type Read-write
Reset 0x03561414
Width 32

3.3.122 t_rtw_next
Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtw_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x234
Type Read-write
Reset 0x10060404
Width 32

3.3.123 t_rtp_next
Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rtp_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.124 t_wr_next

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank. Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: \( t_{wr}(dmc) = CWL +4+tWR(\text{from dram data sheet}) \). CWL should account for write CRC if enabled. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wr_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000005</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.125 t_wtr_next

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs). Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: \( t_{wtr}(dmc) = CWL+WBL/2+tWR(\text{DRAM}) \). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wtr_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>0x248</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x0000005</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.126 t_wtw_next

Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes, same chip, different logical rank(t_wtw_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wtw_next register characteristics are:
3.3.127 t_clock_control_next

Configures the enter DRAM clock disable timing parameter. This parameter is applied between stopping the clock when idle, or when in a power-down state, and any subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_clock_control_next register characteristics are:

Usage constraints
- There are no usage constraints.

Configurations
- There is only one DMC configuration.

Attributes
- Offset: 0x24C
- Type: Read-write
- Reset: 0x10060404
- Width: 32

3.3.128 t_xmpd_next

Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xmpd_next register characteristics are:

Usage constraints
- There are no usage constraints.

Configurations
- There is only one DMC configuration.

Attributes
- Offset: 0x250
- Type: Read-write
- Reset: 0x00000505
- Width: 32

3.3.129 t_ep_next

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ep_next register characteristics are:

Usage constraints
- There are no usage constraints.
3.3.130  **t\_xp\_next**

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t_xpdll must be greater than or equal to tRCD and tCKE, and t_xp must be greater than or equal to tMPX\_S. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xp_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x258
- Type: Read-write
- Reset: 0x00000002
- Width: 32

3.3.131  **t\_esr\_next**

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_esr_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x25C
- Type: Read-write
- Reset: 0x00000002
- Width: 32

3.3.132  **t\_xsr\_next**

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_xsr_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.
Attributes
Offset  0x264
Type    Read-write
Reset   0x05120100
Width   32

3.3.133  t_esrck_next

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_esrck_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x268
Type    Read-write
Reset   0x00000005
Width   32

3.3.134  t_ckxsr_next

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_ckxsr_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x26C
Type    Read-write
Reset   0x00000001
Width   32

3.3.135  t_cmd_next

Configures command signaling timing. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_cmd_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x270
Type    Read-write
3.3.136  **t_parity_next**

Parity latencies \( t_{\text{parinlat}} \) and \( t_{\text{completion}} \). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \( t_{\text{parity}\_next} \) register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x274
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.137  **t_zqcs_next**

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \( t_{\text{zqcs}\_next} \) register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x278
- Type: Read-write
- Reset: 0x00000040
- Width: 32

3.3.138  **t_rw_odt_clr_next**

This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as t_poll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to \( t_{\text{odt}\_off\_rd/wr}(\text{max setting}) + \text{DODTOff}(\text{from DDR4 spec}) \) Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \( t_{\text{rw}\_odt\_clr}\_next \) register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x27C
- Type: Read-write
3.3.139  \textit{t\_rddata\_en\_next}

Determines the time between a READ command commencing on the DFI interface, and the assertion of the \textit{dfi\_read\_en} signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \textit{t\_rddata\_en\_next} register characteristics are:

\textbf{Usage constraints}

There are no usage constraints.

\textbf{Configurations}

There is only one DMC configuration.

\textbf{Attributes}

\begin{itemize}
  \item Offset \(0x300\)
  \item Type Read-write
  \item Reset \(0x00000001\)
  \item Width 32
\end{itemize}

3.3.140  \textit{t\_phyrdlat\_next}

Determines the maximum possible time between the assertion of the \textit{dfi\_read\_en} signal, and the assertion of the \textit{dfi\_rddata\_valid} signal by the PHY. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \textit{t\_phyrdlat\_next} register characteristics are:

\textbf{Usage constraints}

There are no usage constraints.

\textbf{Configurations}

There is only one DMC configuration.

\textbf{Attributes}

\begin{itemize}
  \item Offset \(0x304\)
  \item Type Read-write
  \item Reset \(0x00000000\)
  \item Width 32
\end{itemize}

3.3.141  \textit{t\_phywrlat\_next}

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of the \textit{dfi\_wrdata\_en}, \textit{dfi\_wrdata\_cs} and \textit{dfi\_wrdata} signals. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \textit{t\_phywrlat\_next} register characteristics are:

\textbf{Usage constraints}

There are no usage constraints.

\textbf{Configurations}

There is only one DMC configuration.

\textbf{Attributes}

\begin{itemize}
  \item Offset \(0x308\)
  \item Type Read-write
  \item Reset \(0x00000001\)
  \item Width 32
\end{itemize}
### 3.3.142 rdlvl_control_next

Determines the DMC behavior during read training operations. See the PHY training interface section of the Integration Manual for more details on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl_control_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x310
- Type: Read-write
- Reset: 0x00001080
- Width: 32

### 3.3.143 rdlvl_mrs_next

Determines the Mode Register command to use to place the DRAM into a training mode for read training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The rdlvl_mrs_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x314
- Type: Read-write
- Reset: 0x00000004
- Width: 32

### 3.3.144 t_rdlvl_en_next

Configures the t_rdlvl_en timing parameter. This specifies the cycle delay between asserting dfi_rdlvl_en and the first training command, and also the cycle delay between deasserting dfi_rdlvl_en and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rdlvl_en_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x318
- Type: Read-write
- Reset: 0x00000000
- Width: 32
3.3.145  t_rdlvl_rr_next
Configures the t_rdlvl_rr timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting dfi_rdlvl_en after observing dfi_rdlvl.resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_rdlvl_rr_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x31C
Type Read-write
Reset 0x00000000
Width 32

3.3.146  wrlvl_control_next
Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x320
Type Read-write
Reset 0x00101000
Width 32

3.3.147  wrlvl_mrs_next
Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wrlvl_mrs_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x324
Type Read-write
Reset 0x00000086
Width 32
3.3.148 t_wrlvl_en_next

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wrlvl_en_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
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<tr>
<th>Offset</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
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</tr>
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<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.149 t_wrlvl_ww_next

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvl_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wrlvl_ww_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
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<tbody>
<tr>
<td>Type</td>
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<td>Reset</td>
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</tr>
<tr>
<td>Width</td>
<td>32</td>
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</tbody>
</table>

3.3.150 training_wrlvl_slice_status

Shows slice information relating to the wrlvl training request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_wrlvl_slice_status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
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<tbody>
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<td>Type</td>
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<td>Reset</td>
<td>0x00000000</td>
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<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>
3.3.151  **training_rdlvl_slice_status**

Shows slice information relating to the rdlvl training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_slice_status register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x338
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.152  **training_rdlvl_gate_slice_status**

Shows slice information relating to the rdlvl gate training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_gate_slice_status register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x33C
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.153  **training_wdqlvl_slice_status**

Shows slice information relating to the WrDQ training request status of the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_status register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x340
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.154  **training_wdqlvl_slice_result**

Shows per slice result from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO
Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_result register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x344
Type Read-only
Reset 0x00000000
Width 32

3.3.155 phy_power_control_next

Configures the low-power requests made to the PHY for the different channel states. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_power_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x348
Type Read-write
Reset 0x00000000
Width 32

3.3.156 t_lpresp_next

Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_lpresp_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x34C
Type Read-write
Reset 0x00000000
Width 32

3.3.157 phy_update_control_next

Configures the update mechanism to use in response to PHY training requests. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phy_update_control_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.158  t_odth_next

Configures the ODTH8 timing parameter as timed from Write command registered with ODT high
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_odth_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x350
Type    Read-write
Reset   0x2FE00000
Width   32

3.3.159  odt_timing_next

Configures the ODT on and off timing. Access restrictions: RW Can be read from when in ALL states.
Can be written to when in ALL states.

The odt_timing_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x354
Type    Read-write
Reset   0x00000006
Width   32

3.3.160  odt_wr_control_31_00_next

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions:
RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_wr_control_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x360
Type    Read-write
Reset   0x08040201
Width   32
3.3.161  odt_wr_control_63_32_next
Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions:
RW Can be read from when in ALL states. Can be written to when in ALL states.
The odt_wr_control_63_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x364
- Type Read-write
- Reset 0x80402010
- Width 32

3.3.162  odt_rd_control_31_00_next
Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions:
RW Can be read from when in ALL states. Can be written to when in ALL states.
The odt_rd_control_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x368
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.163  odt_rd_control_63_32_next
Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions:
RW Can be read from when in ALL states. Can be written to when in ALL states.
The odt_rd_control_63_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x36c
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.164  temperature_readout
Holds the status of the temperature information. Reading the register returns the current temperature
from the most recent automated temperature poll. Access restrictions: RO Can be read from when in
ALL states. Cannot be changed.
The temperature_readout register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

3.3.165 training_status

Shows information relating to the training request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

3.3.166 training_status_63_32

Shows information relating to the update request status of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_status_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

3.3.167 dq_map_control_15_00_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_15_00_next register characteristics are:

Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0x380
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.168 dq_map_control_31_16_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_31_16_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0x384
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.169 dq_map_control_47_32_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_47_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0x388
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.170 dq_map_control_63_48_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The dq_map_control_63_48_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x38C
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.171 dq_map_control_71_64_next

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The dq_map_control_71_64_next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x390
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.172 rank_status

Shows the current status of geardown, MPD and CAL. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The rank_status register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x398
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.173 mode_change_status

Shows the current status of the sequence that is currently being processed. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The mode_change_status register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x39C
Type Read-only
Reset 0x00000000
Width 32

3.3.174 odt_cp_control_31_00_next
Determines which of the 8 dfi_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_cp_control_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x3B0
Type Read-write
Reset 0x08040201
Width 32

3.3.175 odt_cp_control_63_32_next
Determines which of the 8 dfi_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The odt_cp_control_63_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x3B4
Type Read-write
Reset 0x80402010
Width 32

3.3.176 user_status
Shows the value of the input user_status signals. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The user_status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.177 user_config0_next

Drives the output user_config0 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user_config0_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x400
Type Read-only
Reset 0x00000000
Width 32

3.3.178 user_config1_next

Drives the output user_config1 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user_config1_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x40C
Type Read-write
Reset 0x00000000
Width 32

3.3.179 user_config2

Drives the output user_config2 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user_config2 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x410
Type Read-write
Reset 0x00000000
Width 32
3.3.180 user_config3

Drives the output user_config3 signal. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The user_config3 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x414
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.181 interrupt_control

Configures interrupt behavior. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The interrupt_control register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x500
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.182 interrupt_clr

Clear register for interrupts. Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The interrupt_clr register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x508
- Type: Write-only
- Reset: 0x00000000
- Width: 32

3.3.183 interrupt_status

Status register for interrupts (pre-mask). Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The interrupt_status register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x510
Type Read-only
Reset 0x00000000
Width 32

3.3.184 failed_access_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_access_int_info_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x538
Type Read-only
Reset 0x00000000
Width 32

3.3.185 failed_access_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_access_int_info_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x53C
Type Read-only
Reset 0x00000000
Width 32

3.3.186 failed_prog_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_prog_int_info_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.187 failed_prog_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The failed_prog_int_info_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x540
Type Read-only
Reset 0x00000000
Width 32

3.3.188 link_err_int_info_31_00

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link_err_int_info_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x544
Type Read-only
Reset 0x00000000
Width 32

3.3.189 link_err_int_info_63_32

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The link_err_int_info_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x548
Type Read-only
Reset 0x00000000
Width 32
3.3.190  **arch fsm int info 31 00**

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch fsm int info 31 00 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset 0x550
- Type Read-only
- Reset 0x00000000
- Width 32

3.3.191  **arch fsm int info 63 32**

Shows information relating to the interrupt Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The arch fsm int info 63 32 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset 0x554
- Type Read-only
- Reset 0x00000000
- Width 32

3.3.192  **t db train resp next**

Configures the t db train resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi db train resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi rddata_valid) to define the delay between DFI read command and when the response is valid on the dfi rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t db train resp next register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset 0x610
- Type Read-write
- Reset 0x00000000
- Width 32
3.3.193  \texttt{t_lvl_disconnect\_next}

Configures the t\_lvl\_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t*lvl\_disconnect and t*lvl\_disconnect\_error timing parameters from the PHY. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{t_lvl_disconnect\_next} register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x614
  - Type: Read-write
  - Reset: 0x0000000F
  - Width: 32

3.3.194  \texttt{wdqlvl\_control\_next}

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{wdqlvl\_control\_next} register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x620
  - Type: Read-write
  - Reset: 0x00000094
  - Width: 32

3.3.195  \texttt{wdqlvl\_vrefdq\_train\_mrs\_next}

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the \texttt{wdqlvl\_control\_register}. You enable this function with the \texttt{wdqlvl\_control\_Register}. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{wdqlvl\_vrefdq\_train\_mrs\_next} register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x624
  - Type: Read-write
  - Reset: 0x00000000
  - Width: 32
3.3.196  wdqlvl_address_31_00_next

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_address_31_00_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x628
 Type Read-write
 Reset 0x00000000
 Width 32

3.3.197  wdqlvl_address_63_32_next

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The wdqlvl_address_63_32_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x62C
 Type Read-write
 Reset 0x00000000
 Width 32

3.3.198  t_wdqlvl_en_next

Configures the t_wdqlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wdqlvl_en, the delay between asserting dfi_wdqlvl_en and the first training command, the delay between de-asserting dfi_wdqlvl_en and de-asserting ODT, and de-asserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_en_next register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x630
 Type Read-write
 Reset 0x00000000
 Width 32
3.3.199  t_wdqlvl_ww_next

Configures the t_wdqlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wdqlvl_resp. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_ww_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x634
- **Type**: Read-write
- **Reset**: 0xffffffff
- **Width**: 32

3.3.200  t_wdqlvl_rw_next

Configures the t_wdqlvl_rw timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The t_wdqlvl_rw_next register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x638
- **Type**: Read-write
- **Reset**: 0xffffffff
- **Width**: 32

3.3.201  training_wdqlvl_slice_resp

Shows per slice response from the PHY in response to the WrDQ training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_wdqlvl_slice_resp register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x63C
- **Type**: Read-only
- **Reset**: 0xffffffff
- **Width**: 32
### 3.3.202 training_rdlvl_slice_resp

Shows per slice response from the PHY in response to the rdlvl training request to the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The training_rdlvl_slice_resp register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**:
  - **Offset**: 0x640
  - **Type**: Read-only
  - **Reset**: 0x00000000
  - **Width**: 32

### 3.3.203 phymstr_control_next

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The phymstr_control_next register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**:
  - **Offset**: 0x654
  - **Type**: Read-write
  - **Reset**: 0x00000000
  - **Width**: 32

### 3.3.204 err0fr

This record defines features which are common to all RAS error records in this section. Each field defines which of the architecturally-defined common features are implemented and, of the implemented features, which are software programmable. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0fr register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**:
  - **Offset**: 0x700
  - **Type**: Read-only
  - **Reset**: 0x000009AA
  - **Width**: 32
3.3.205 err0ctlr0

This register is the global control register for the DMC RAS functions. This register control features such as ECC type and enable, error reporting and interrupt enable, error deferment, etc. The setting of a Global control record bit affects all records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctlr0 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x708
Type Read-write
Reset 0x00000010
Width 32

3.3.206 err0ctlr1

This register is the global control register for the DMC RAS functions. The registers in this record affect all DMC RAS records. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The err0ctlr1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x70C
Type Read-write
Reset 0x000000C0
Width 32

3.3.207 err0status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err0status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x710
Type Read-only
Reset 0x00000000
Width 32
3.3.208  err1fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1fr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x740
- Type Read-only
- Reset 0x000009AA
- Width 32

3.3.209  err1ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err1ctlr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x748
- Type Read-only
- Reset 0x00000000
- Width 32

3.3.210  err1status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x750
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.211  err1addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. If an error has an associated physical address, this must be written to the
address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr0 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

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<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x758</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.212 err1addr1

Contains the physical CID and Rank broken out in the following way: [31:6] = Reserved, [5:3] = CID, [2:0] = Rank. If an error has an associated physical address, this must be written to the address register when the error is recorded. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1addr1 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x75C</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.213 err1misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc0 register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x760</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.214 err1misc1

This register gives the bank, logical rank, and failed nibble location of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The.err1misc1.register.characteristics.are:

Usage.constraints
There.are.no.usage.constraints.

Configurations
There.is.only.one.DMC.configuration.

Attributes
Offset 0x764
Type Read-write
Reset 0x00000000
Width 32

3.3.215 err1misc2

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The.err1misc2.register.characteristics.are:

Usage.constraints
There.are.no.usage.constraints.

Configurations
There.is.only.one.DMC.configuration.

Attributes
Offset 0x768
Type Read-write
Reset 0x00000000
Width 32

3.3.216 err1misc3

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The.err1misc3.register.characteristics.are:

Usage.constraints
There.are.no.usage.constraints.

Configurations
There.is.only.one.DMC.configuration.

Attributes
Offset 0x76C
Type Read-write
Reset 0x00000000
Width 32

3.3.217 err1misc4

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The.err1misc4.register.characteristics.are:

Usage.constraints
There.are.no.usage.constraints.

Configurations
There.is.only.one.DMC.configuration.
Attributes
Offset 0x770
Type Read-write
Reset 0x00000000
Width 32

3.3.218 err1misc5

DRAM Correctable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err1misc5 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x774
Type Read-write
Reset 0x00000000
Width 32

3.3.219 err2fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2fr register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x780
Type Read-only
Reset 0x000009AA
Width 32

3.3.220 err2ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTL0. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err2ctlr register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x788
Type Read-only
3.3.221 err2status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x790
Type Read-write
Reset 0x00000000
Width 32

3.3.222 err2addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2addr0 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x798
Type Read-write
Reset 0x00000000
Width 32

3.3.223 err2addr1


The err2addr1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x79C
Type Read-write
Reset 0x00000000
Width 32
3.3.224  err2misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc0 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x7A0</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.225  err2misc1

This register gives the bank and logical rank of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x7A4</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.226  err2misc2

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc2 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x7A8</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.227  err2misc3

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc3 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x7AC
Type Read-write
Reset 0x00000000
Width 32

3.3.228 err2misc4

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc4 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x7B0
Type Read-write
Reset 0x00000000
Width 32

3.3.229 err2misc5

DRAM Uncorrectable Error Counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err2misc5 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x7B4
Type Read-write
Reset 0x00000000
Width 32

3.3.230 err3fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3fr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.231  **err3ctlr**

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The **err3ctlr** register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset 0x7C0
- Type Read-only
- Reset 0x000009AA
- Width 32

3.3.232  **err3status**

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The **err3status** register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset 0x7D0
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.233  **err3addr0**

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The **err3addr0** register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset 0x7D8
- Type Read-write
- Reset 0x00000000
- Width 32
### 3.3.234 err3addr1

Contains the physical CID and Rank broken out in the following way: 

\[
\]

Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err3addr1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

- **Offset**: 0x7DC
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.235 err3misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last created.

Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3misc0 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

- **Offset**: 0x7E0
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

### 3.3.236 err3misc1

This register gives the bank and logical rank of the first error detected since last created. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err3misc1 register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

- **Offset**: 0x7E4
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32
3.3.237 err4fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4fr register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x800
- Type: Read-only
- Reset: 0x000009AA
- Width: 32

3.3.238 err4ctrlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTRL. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err4ctrlr register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x808
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.239 err4status

This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4status register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x810
- Type: Read-write
- Reset: 0x00000000
- Width: 32
3.3.240 err4addr0

Contains the physical Bank, Row, and Column broken out in the following way \{[31:28] = Bank, [27:10] = Row, [9:0] = Column\}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4addr0 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x818
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.241 err4addr1


The err4addr1 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x81C
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.242 err4misc0

This register gives the Physical Rank, Row, and Column of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc0 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x820
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32
3.3.243 err4misc1

This register gives the bank and logical rank, and DBID of the last error detected before an interrupt is asserted. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x824
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.244 err4misc2

Ram Correctable Error Counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err4misc2 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x828
- Type Read-write
- Reset 0x00000000
- Width 32

3.3.245 err5fr

Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5fr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x840
- Type Read-only
- Reset 0x000009AA
- Width 32
3.3.246 err5ctlr

This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTL. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err5ctlr register characteristics are:

Usage constraints
   There are no usage constraints.
Configurations
   There is only one DMC configuration.
Attributes
   Offset 0x848
   Type Read-only
   Reset 0x00000000
   Width 32

3.3.247 err5status

This status register reports error type, status, and contains valid bits for extra syndrome registers Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5status register characteristics are:

Usage constraints
   There are no usage constraints.
Configurations
   There is only one DMC configuration.
Attributes
   Offset 0x850
   Type Read-write
   Reset 0x000000
   Width 32

3.3.248 err5addr0

Contains the physical Bank, Row, and Column broken out in the following way {[31:28] = Bank, [27:10] = Row, [9:0] = Column}. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr0 register characteristics are:

Usage constraints
   There are no usage constraints.
Configurations
   There is only one DMC configuration.
Attributes
   Offset 0x858
   Type Read-write
   Reset 0x00000000
   Width 32
### err5addr1

Contains the physical CID and Rank broken out in the following way: \([31:6] = \text{Reserved}, [5:3] = \text{CID}, [2:0] = \text{Rank}\) Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5addr1 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x85C
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### err5misc0

This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc0 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x860
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### err5misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc1 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x864
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

### err5misc2

RAM Uncorrectable error counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err5misc2 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x868
Type Read-write
Reset 0x00000000
Width 32

3.3.253 err6fr
Reading this register returns the same value programmed in the ERR0FR Global Control Record Feature Register. See the ERR0FR description for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6fr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x880
Type Read-only
Reset 0x000009AA
Width 32

3.3.254 err6ctlr
This register is reserved. Control of this register is achieved through the Global Control Record Register - ERR0CTLR. Reading this register returns all zeros. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The err6ctlr register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x888
Type Read-only
Reset 0x00000000
Width 32

3.3.255 err6status
This status register reports error type, status, and contains valid bits for extra syndrome registers. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6status register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
Attributes
Offset 0x890
Type Read-write
Reset 0x000000
Width 32

3.3.256 err6addr0
Contains the physical Bank, Row, and Column broken out in the following way \([31:28] = \text{Bank}, [27:10] = \text{Row}, [9:0] = \text{Column}\). Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr0 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.

Attributes
Offset 0x898
Type Read-write
Reset 0x00000000
Width 32

3.3.257 err6addr1
Contains the physical CID and Rank broken out in the following way \([31:6] = \text{Reserved}, [5:3] = \text{CID}, [2:0] = \text{Rank}\) Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6addr1 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.

Attributes
Offset 0x89C
Type Read-write
Reset 0x00000000
Width 32

3.3.258 err6misc0
This register gives the Physical Rank, Row, and Column of the first error detected since last cleared. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc0 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.

Attributes
Offset 0x8A0
Type Read-write
3.3.259  err6misc1

This register gives the bank and logical rank, and DBID of the first error detected since the last clear. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The err6misc1 register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x8A4
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.260  errgsr

This register shows the status of all the DMC error records. When a CFH, FH, or ER interrupt occurs software may check this register to tell which error record(s) caused the interrupt. Each field in this register is a copy of each individual records ERRnSTATUS.V bit. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The errgsr register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x920
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.261  pmu_snapshot_req

Generates PMU snapshot request Access restrictions: WO Cannot be read from. Can be written to when in ALL states.

The pmu_snapshot_req register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0xA00
- Type: Write-only
- Reset: 0x00000000
- Width: 32
3.3.262 pmu_snapshot_ack

Indicates PMU snapshot acknowledge Access restrictions: RO Can be read from when in ALL states.
Cannot be changed.

The pmu_snapshot_ack register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xA04
Type Read-only
Reset 0x00000000
Width 32

3.3.263 pmu_overflow_status_clkdiv2

Indicates which clkdiv2 counters have overflowed Access restrictions: RW Can be read from when in
ALL states. Can be written to when in ALL states.

The pmu_overflow_status_clkdiv2 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xA08
Type Read-write
Reset 0x00000000
Width 32

3.3.264 pmu_overflow_status_clk

Indicates which clk domain counters have overflowed Access restrictions: RW Can be read from when in
ALL states. Can be written to when in ALL states.

The pmu_overflow_status_clk register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xA0C
Type Read-write
Reset 0x00000000
Width 32

3.3.265 pmu_clkdiv2_counter_0_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be
written to when in ALL states.

The pmu_clkdiv2_counter_0_mask_31_00 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset $0xA10$
Type Read-write
Reset $0x00000000$
Width 32

3.3.266 pmu_clkdiv2_counter_0_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_mask_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset $0xA14$
Type Read-write
Reset $0x00000000$
Width 32

3.3.267 pmu_clkdiv2_counter_0_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset $0xA18$
Type Read-write
Reset $0x00000000$
Width 32

3.3.268 pmu_clkdiv2_counter_0_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_0_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.269 **pmu_clkdiv2_counter_0_control**

Controls muxes, enables and other control bits for the PMU counters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `pmu_clkdiv2_counter_0_control` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>0xA1C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.270 **pmu_clkdiv2_counter_0_snapshot_value_31_00**

Value of the PMU snapshot registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The `pmu_clkdiv2_counter_0_snapshot_value_31_00` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>0xA20</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
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<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.271 **pmu_clkdiv2_counter_0_value_31_00**

Value of the PMU counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The `pmu_clkdiv2_counter_0_value_31_00` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>
3.3.272  pmu_clkdiv2_counter_1_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xA38
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.273  pmu_clkdiv2_counter_1_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_mask_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xA3C
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.274  pmu_clkdiv2_counter_1_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xA40
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.275  pmu_clkdiv2_counter_1_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_match_63_32 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0xA4
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.276 pmu_clkdiv2_counter_1_control
Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0xA8
- **Type**: Read-write
- **Reset**: 0x00000000
- **Width**: 32

3.3.277 pmu_clkdiv2_counter_1_snapshot_value_31_00
value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_1_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- **Offset**: 0xA5
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

3.3.278 pmu_clkdiv2_counter_1_value_31_00
value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_1_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.279 pmu_clkdiv2_counter_2_mask_31_00
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_2_mask_31_00 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes

3.3.280 pmu_clkdiv2_counter_2_mask_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_2_mask_63_32 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes

3.3.281 pmu_clkdiv2_counter_2_match_31_00
Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_2_match_31_00 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
3.3.282 pmu_clkdiv2_counter_2_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA6C</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.283 pmu_clkdiv2_counter_2_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA70</td>
<td>Read-write</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.284 pmu_clkdiv2_counter_2_snapshot_value_31_00

Value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_2_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA78</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.285 pmu_clkdiv2_counter_2_value_31_00

Value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_2_value_31_00 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>0xA80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.286 pmu_clkdiv2_counter_3_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>0xA80</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.287 pmu_clkdiv2_counter_3_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_mask_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>0xA8C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.288 pmu_clkdiv2_counter_3_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.289  pmu_clkdiv2_counter_3_match_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xA90
Type   Read-write
Reset  0x00000000
Width  32

3.3.290  pmu_clkdiv2_counter_3_control
Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_3_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xA94
Type   Read-write
Reset  0x00000000
Width  32

3.3.291  pmu_clkdiv2_counter_3_snapshot_value_31_00
value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_3_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xAA0
Type   Read-only
Reset  0x00000000
Width  32
3.3.292  \texttt{pmu\_clkdiv2\_counter\_3\_value\_31\_00}

- Value of the PMU counter
- Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{pmu\_clkdiv2\_counter\_3\_value\_31\_00} register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**
  - Offset: 0xAA8
  - Type: Read-write
  - Reset: 0x00000000
  - Width: 32

3.3.293  \texttt{pmu\_clkdiv2\_counter\_4\_mask\_31\_00}

- Masks PMU payload information
- Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{pmu\_clkdiv2\_counter\_4\_mask\_31\_00} register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**
  - Offset: 0xAB0
  - Type: Read-write
  - Reset: 0x00000000
  - Width: 32

3.3.294  \texttt{pmu\_clkdiv2\_counter\_4\_mask\_63\_32}

- Masks PMU payload information
- Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{pmu\_clkdiv2\_counter\_4\_mask\_63\_32} register characteristics are:

- **Usage constraints**: There are no usage constraints.
- **Configurations**: There is only one DMC configuration.
- **Attributes**
  - Offset: 0xAB4
  - Type: Read-write
  - Reset: 0x00000000
  - Width: 32

3.3.295  \texttt{pmu\_clkdiv2\_counter\_4\_match\_31\_00}

- Compares against the masked PMU payload to determine whether or not to increment the counter.
- Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The \texttt{pmu\_clkdiv2\_counter\_4\_match\_31\_00} register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xAB8
Type Read-write
Reset 0x00000000
Width 32

3.3.296 pmu_clkdiv2_counter_4_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xABC
Type Read-write
Reset 0x00000000
Width 32

3.3.297 pmu_clkdiv2_counter_4_control

Controls muxes, enables and other control bits for the PMU counters. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_4_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xAC0
Type Read-write
Reset 0x00000000
Width 32

3.3.298 pmu_clkdiv2_counter_4_snapshot_value_31_00

Value of the pmu snapshot registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_4_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.299 pmu_clkdiv2_counter_4_value_31_00
value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written
to when in ALL states.
The pmu_clkdiv2_counter_4_value_31_00 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xAC8
Type Read-only
Reset 0x00000000
Width 32

3.3.300 pmu_clkdiv2_counter_5_mask_31_00
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be
written to when in ALL states.
The pmu_clkdiv2_counter_5_mask_31_00 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xAD0
Type Read-write
Reset 0x00000000
Width 32

3.3.301 pmu_clkdiv2_counter_5_mask_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be
written to when in ALL states.
The pmu_clkdiv2_counter_5_mask_63_32 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xAD8
Type Read-write
Reset 0x00000000
Width 32
3.3.302  pmu_clkdiv2_counter_5_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xAE0
Type    Read-write
Reset   0x00000000
Width   32

3.3.303  pmu_clkdiv2_counter_5_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xAE4
Type    Read-write
Reset   0x00000000
Width   32

3.3.304  pmu_clkdiv2_counter_5_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_5_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0xAE8
Type    Read-write
Reset   0x00000000
Width   32

3.3.305  pmu_clkdiv2_counter_5_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_5_snapshot_value_31_00 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xAF8
Type Read-only
Reset 0x00000000
Width 32

3.3.306 pmu_clkdiv2_counter_5_value_31_00
value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_5_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xAF8
Type Read-write
Reset 0x00000000
Width 32

3.3.307 pmu_clkdiv2_counter_6_mask_31_00
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_6_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB00
Type Read-write
Reset 0x00000000
Width 32

3.3.308 pmu_clkdiv2_counter_6_mask_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clkdiv2_counter_6_mask_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.309 pmu_clkdiv2_counter_6_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB04
Type Read-write
Reset 0x00000000
Width 32

3.3.310 pmu_clkdiv2_counter_6_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB08
Type Read-write
Reset 0x00000000
Width 32

3.3.311 pmu_clkdiv2_counter_6_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_6_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB10
Type Read-write
Reset 0x00000000
Width 32
3.3.312  pmu_clkdiv2_counter_6_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states.
Cannot be changed.

The pmu_clkdiv2_counter_6_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset       0xB18
  Type         Read-only
  Reset        0x00000000
  Width        32

3.3.313  pmu_clkdiv2_counter_6_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written
to when in ALL states.

The pmu_clkdiv2_counter_6_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset       0xB20
  Type         Read-write
  Reset        0x00000000
  Width        32

3.3.314  pmu_clkdiv2_counter_7_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written
to when in ALL states.

The pmu_clkdiv2_counter_7_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset       0xB28
  Type         Read-write
  Reset        0x00000000
  Width        32

3.3.315  pmu_clkdiv2_counter_7_mask_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written
to when in ALL states.

The pmu_clkdiv2_counter_7_mask_63_32 register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xB2C
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.316 pmu_clkdiv2_counter_7_match_31_00

Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xB30
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.317 pmu_clkdiv2_counter_7_match_63_32

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0xB34
- Type: Read-write
- Reset: 0x00000000
- Width: 32

3.3.318 pmu_clkdiv2_counter_7_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.319 pmu_clkdiv2_counter_7_snapshot_value_31_00

Value of the pmu snapshot registers. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clkdiv2_counter_7_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x840
Type Read-only
Reset 0x00000000
Width 32

3.3.320 pmu_clkdiv2_counter_7_value_31_00

Value of the PMU counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clkdiv2_counter_7_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x848
Type Read-write
Reset 0x00000000
Width 32

3.3.321 pmu_clk_counter_0_mask_31_00

Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x850
Type Read-write
Reset 0x00000000
Width 32
3.3.32 pmu_clk_counter_0_mask_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clk_counter_0_mask_63_32 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xB54
Type Read-write
Reset 0x00000000
Width 32

3.3.323 pmu_clk_counter_0_match_31_00
Compares against the masked PMU payload to determine whether or not to increment the counter. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clk_counter_0_match_31_00 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xB58
Type Read-write
Reset 0x00000000
Width 32

3.3.324 pmu_clk_counter_0_match_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clk_counter_0_match_63_32 register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0xB5C
Type Read-write
Reset 0x00000000
Width 32

3.3.325 pmu_clk_counter_0_control
Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.
The pmu_clk_counter_0_control register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB60
Type Read-write
Reset 0x00000000
Width 32

3.3.326 pmu_clk_counter_0_snapshot_value_31_00
value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clk_counter_0_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB60
Type Read-only
Reset 0x00000000
Width 32

3.3.327 pmu_clk_counter_0_value_31_00
value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_0_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB70
Type Read-write
Reset 0x00000000
Width 32

3.3.328 pmu_clk_counter_1_mask_31_00
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_mask_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB78
Type Read-write
Reset 0x00000000
Width 32

3.3.329 pmu_clk_counter_1_mask_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_mask_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB7C
Type Read-write
Reset 0x00000000
Width 32

3.3.330 pmu_clk_counter_1_match_31_00
Compares against the masked PMU payload to determine whether or not to increment the counter.
Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_match_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB80
Type Read-write
Reset 0x00000000
Width 32

3.3.331 pmu_clk_counter_1_match_63_32
Masks PMU payload information. Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_match_63_32 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xB84
Type Read-write
Reset 0x00000000
Width 32
3.3.332 pmu_clk_counter_1_control

Controls muxes, enables and other control bits for the PMU counters Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_control register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
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<td>Reset</td>
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</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.333 pmu_clk_counter_1_snapshot_value_31_00

value of the pmu snapshot registers Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The pmu_clk_counter_1_snapshot_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
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<tbody>
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<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.334 pmu_clk_counter_1_value_31_00

value of the PMU counter Access restrictions: RW Can be read from when in ALL states. Can be written to when in ALL states.

The pmu_clk_counter_1_value_31_00 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>0x898</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-write</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000000</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.335 integ_cfg

Integration test register to enable integration test mode. Access restrictions: RW Can be read from when in ALL states. Can be written to when in CONFIG or LOW-POWER states.

The integ_cfg register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xE00
Type Read-write
Reset 0x00000000
Width 32

3.3.336  integ_outputs

Drives the value of outputs when in integration test mode. Access restrictions: WO Cannot be read from. Can be written to when in CONFIG or LOW-POWER states.

The integ_outputs register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0xE08
Type Write-only
Reset 0x00000000
Width 32

3.3.337  address_control_now

Configures the DRAM address parameters. Use the DRAM device data sheet or Serial Presence Detect (SPD)-derived values to assist in programming these values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1010
Type Read-only
Reset 0x00030202
Width 32

3.3.338  decode_control_now

Configures how the DRAM address is decoded from the system address. The DRAM address consists of the rank, cid, bank, row, and the column address. Note: Order fields must be unique, i.e. row_order != bank_order != rank_order. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The decode_control_now register characteristics are:

Usage constraints
There are no usage constraints.
Configurations

There is only one DMC configuration.

Attributes

Offset  0x1014
Type    Read-only
Reset   0x001A3000
Width   32

3.3.339  address_map_now

Configures the system address mapping options. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The address_map_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset  0x101C
Type    Read-only
Reset   0x00000000
Width   32

3.3.340  low_power_control_now

Configures the low-power features of the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The low_power_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset  0x1020
Type    Read-only
Reset   0x00000020
Width   32

3.3.341  turnaround_control_now

Configures the settings for arbitration between read and write and rank to rank traffic on the DRAM bus. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The turnaround_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset  0x1028
Type  Read-only
Reset  0x0F0F0F0F
Width  32

3.3.342  **hit_turnaround_control_now**

Configures the settings for preventing starvation of non-hits in the presence of in-row hit streams. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The hit_turnaround_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset  0x102C
  Type    Read-only
  Reset   0x08909FBF
  Width   32

3.3.343  **qos_class_control_now**

Configures the priority class for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qos_class_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset  0x1030
  Type    Read-only
  Reset   0x00000FC8
  Width   32

3.3.344  **escalation_control_now**

Configures the settings for escalating the priority of entries in the queue. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The escalation_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
  Offset  0x1034
  Type    Read-only
  Reset   0x00080F03
  Width   32
3.3.345  qv_control_31_00_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x1038
- Type Read-only
- Reset 0x76543210
- Width 32

3.3.346  qv_control_63_32_now

Configures the priority settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The qv_control_63_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x103C
- Type Read-only
- Reset 0xFEDCBA98
- Width 32

3.3.347  rt_control_31_00_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x1040
- Type Read-only
- Reset 0x00000000
- Width 32
### 3.3.348 rt_control_63_32_now

Configures the timeout settings for each QoS encoding. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rt_control_63_32_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1044
- Type: Read-only
- Reset: 0x00000000
- Width: 32

### 3.3.349 timeout_control_now

Configures the prescaler applied to timeout values. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The timeout_control_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1048
- Type: Read-only
- Reset: 0x00000001
- Width: 32

### 3.3.350 credit_control_now

Configures the settings for preventing starvation of CHI protocol retries. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The credit_control_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x104C
- Type: Read-only
- Reset: 0x0000F03
- Width: 32
3.3.351  write_priority_control_31_00_now

Configures the priority settings for write requests within the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write_priority_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1050
Type Read-only
Reset 0x00000000
Width 32

3.3.352  write_priority_control_63_32_now

Configures the priority settings for write requests within the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The write_priority_control_63_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1054
Type Read-only
Reset 0x00000000
Width 32

3.3.353  queue_threshold_control_31_00_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue_threshold_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1058
Type Read-only
Reset 0x00000008
Width 32
3.3.354 queue_threshold_control_63_32_now

Configures the threshold settings for requests in the DMC Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The queue_threshold_control_63_32_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x105C
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

3.3.355 address_shutter_31_00_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_31_00_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1060
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

3.3.356 address_shutter_63_32_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_63_32_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1064
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32
3.3.357 address_shutter_95_64_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
PAUSED or READY states.

The address_shutter_95_64_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1068
Type Read-only
Reset 0x00000000
Width 32

3.3.358 address_shutter_127_96_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
PAUSED or READY states.

The address_shutter_127_96_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x106C
Type Read-only
Reset 0x00000000
Width 32

3.3.359 address_shutter_159_128_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
PAUSED or READY states.

The address_shutter_159_128_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1070
Type Read-only
Reset 0x00000000
Width 32
3.3.360  address_shutter_191_160_now

Configures the address shuttering due to channel striping in the interconnect. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The address_shutter_191_160_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1074
Type Read-only
Reset 0x00000000
Width 32

3.3.361  memory_address_max_31_00_now

Configures the address space control for the DMC default region. Applies post address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory_address_max_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1078
Type Read-only
Reset 0x00000010
Width 32

3.3.362  memory_address_max_47_32_now

Configures the address space control for the DMC default region. Applies post address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The memory_address_max_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x107C
Type Read-only
Reset 0x00000000
Width 32
3.3.363 access_address_min0_31_00_now
Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_min0_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1080
Type Read-only
Reset 0x00000000
Width 32

3.3.364 access_address_min0_47_32_now
Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_min0_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1084
Type Read-only
Reset 0x00000000
Width 32

3.3.365 access_address_max0_31_00_now
Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_max0_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1088
Type Read-only
Reset 0x00000000
Width 32
3.3.366 access_address_max0_47_32_now

Configures the address space control for address region 0. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max0_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

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<tr>
<th>Offset</th>
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<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.367 access_address_min1_31_00_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min1_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
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</tr>
</thead>
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<td>32</td>
</tr>
</tbody>
</table>

3.3.368 access_address_min1_47_32_now

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min1_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
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</thead>
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<td>0x1094</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>
3.3.369 **access_address_max1_31_00_now**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max1_31_00_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x1098
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

3.3.370 **access_address_max1_47_32_now**

Configures the address space control for address region 1. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max1_47_32_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x109C
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32

3.3.371 **access_address_min2_31_00_now**

Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min2_31_00_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset**: 0x10A0
- **Type**: Read-only
- **Reset**: 0x00000000
- **Width**: 32
3.3.372  access_address_min2_47_32_now
Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min2_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x10A4
Type Read-only
Reset 0x00000000
Width 32

3.3.373  access_address_max2_31_00_now
Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max2_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x10A8
Type Read-only
Reset 0x00000000
Width 32

3.3.374  access_address_max2_47_32_now
Configures the address space control for address region 2. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max2_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x10AC
Type Read-only
Reset 0x00000000
Width 32
3.3.375 access_address_min3_31_00_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min3_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10B0
Type Read-only
Reset 0x00000000
Width 32

3.3.376 access_address_min3_47_32_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min3_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10B4
Type Read-only
Reset 0x00000000
Width 32

3.3.377 access_address_max3_31_00_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max3_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10B8
Type Read-only
Reset 0x00000000
Width 32
3.3.378 access_address_max3_47_32_now

Configures the address space control for address region 3. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max3_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x108C
Type Read-only
Reset 0x00000000
Width 32

3.3.379 access_address_min4_31_00_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min4_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10C0
Type Read-only
Reset 0x00000000
Width 32

3.3.380 access_address_min4_47_32_now

Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min4_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10C4
Type Read-only
Reset 0x00000000
Width 32
3.3.381 access_address_max4_31_00_now
Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_max4_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10C8
Type Read-only
Reset 0x00000000
Width 32

3.3.382 access_address_max4_47_32_now
Configures the address space control for address region 4. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_max4_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10CC
Type Read-only
Reset 0x00000000
Width 32

3.3.383 access_address_min5_31_00_now
Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.
The access_address_min5_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10D0
Type Read-only
Reset 0x00000000
Width 32
3.3.384 access_address_min5_47_32_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min5_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10D4
Type Read-only
Reset 0x00000000
Width 32

3.3.385 access_address_max5_31_00_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max5_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10D8
Type Read-only
Reset 0x00000000
Width 32

3.3.386 access_address_max5_47_32_now

Configures the address space control for address region 5. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max5_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x10DC
Type Read-only
Reset 0x00000000
Width 32
3.3.387 **access_address_min6_31_00_now**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min6_31_00_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset** 0x10E0
- **Type** Read-only
- **Reset** 0x00000000
- **Width** 32

3.3.388 **access_address_min6_47_32_now**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min6_47_32_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset** 0x10E4
- **Type** Read-only
- **Reset** 0x00000000
- **Width** 32

3.3.389 **access_address_max6_31_00_now**

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max6_31_00_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- **Offset** 0x10E8
- **Type** Read-only
- **Reset** 0x00000000
- **Width** 32
3.3.390  access_address_max6_47_32_now

Configures the address space control for address region 6. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max6_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x10EC
 Type Read-only
 Reset 0x00000000
 Width 32

3.3.391  access_address_min7_31_00_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min7_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x10F0
 Type Read-only
 Reset 0x00000000
 Width 32

3.3.392  access_address_min7_47_32_now

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_min7_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
 Offset 0x10F4
 Type Read-only
 Reset 0x00000000
 Width 32
3.3.393  **access_address_max7_31_00_now**

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max7_31_00_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x10F8
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.394  **access_address_max7_47_32_now**

Configures the address space control for address region 7. Applies prior to address translation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The access_address_max7_47_32_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x10FC
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.395  **dci_replay_type_now**

Configures the behavior of the DMC if a DRAM or PHY error is received when executing a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The dci_replay_type_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1110
- Type: Read-only
- Reset: 0x00000002
- Width: 32
3.3.396  **direct_control_now**

Represents the training configuration of the DMC executed by a direct command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, PAUSED or READY states.

The direct_control_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x1114
- Type: Read-only
- Reset: 0x0003FFFF
- Width: 32

3.3.397  **refresh_control_now**

Configures the type of refresh commands issued by the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or PAUSED states.

The refresh_control_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x1120
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.398  **memory_type_now**

Configures the DMC for the attached memory type. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The memory_type_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- Offset: 0x1128
- Type: Read-only
- Reset: 0x00000101
- Width: 32

3.3.399  **scrub_control0_now**

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub_control0_now register characteristics are:
3.3.400 scrub_address_min0_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_min0_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1170
Type Read-only
Reset 0xFFFFF00
Width 32

3.3.401 scrub_address_max0_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_max0_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1174
Type Read-only
Reset 0x00000000
Width 32

3.3.402 scrub_control1_now

Scrub engine channel control register. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The scrub_control1_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
Attributes

Offset 0x1180
Type Read-only
Reset 0xFFFFF00
Width 32

3.3.403 scrub_address_min1_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_min1_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1184
Type Read-only
Reset 0x00000000
Width 32

3.3.404 scrub_address_max1_now

Configures the address space control for the scrub engine channel. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG or LOW-POWER states.

The scrub_address_max1_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x1188
Type Read-only
Reset 0x00000000
Width 32

3.3.405 cs_remap_control_31_00_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset 0x11A0
Type Read-only
3.3.406 cs_remap_control_63_32_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_63_32_now register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x11A4
  - Type: Read-only
  - Reset: 0x00000004
  - Width: 32

3.3.407 cs_remap_control_95_64_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_95_64_now register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x11A8
  - Type: Read-only
  - Reset: 0x00200010
  - Width: 32

3.3.408 cs_remap_control_127_96_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cs_remap_control_127_96_now register characteristics are:

- **Usage constraints**
  - There are no usage constraints.

- **Configurations**
  - There is only one DMC configuration.

- **Attributes**
  - Offset: 0x11AC
  - Type: Read-only
  - Reset: 0x00800040
  - Width: 32
3.3.409 **cid_remap_control_31_00_now**

Control register for dfi_CID remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid_remap_control_31_00_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x11B0
- **Type**: Read-only
- **Reset**: 0x20001000
- **Width**: 32

3.3.410 **cid_remap_control_63_32_now**

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cid_remap_control_63_32_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x11B4
- **Type**: Read-only
- **Reset**: 0x00004000
- **Width**: 32

3.3.411 **cke_remap_control_now**

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The cke_remap_control_now register characteristics are:

**Usage constraints**
There are no usage constraints.

**Configurations**
There is only one DMC configuration.

**Attributes**
- **Offset**: 0x11C0
- **Type**: Read-only
- **Reset**: 0x76543210
- **Width**: 32

3.3.412 **rst_remap_control_now**

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rst_remap_control_now register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x11C4
Type Read-only
Reset 0x76543210
Width 32

3.3.413 ck_remap_control_now

Control register for CKE remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The ck_remap_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x11C8
Type Read-only
Reset 0x76543210
Width 32

3.3.414 power_group_control_31_00_now

Power Group Control register for power managing ranks together. The ranks that are CKE-tied together as represented in cke_remap_control register should belong to the same power-group Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x11D0
Type Read-only
Reset 0x00020001
Width 32

3.3.415 power_group_control_63_32_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_63_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
3.3.416 power_group_control_95_64_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_95_64_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

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<td>Width</td>
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3.3.417 power_group_control_127_96_now

Control register for CS remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The power_group_control_127_96_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

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<tr>
<td>Width</td>
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3.3.418 feature_control_now

Control register for DMC features. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The feature_control_now register characteristics are:

**Usage constraints**

There are no usage constraints.

**Configurations**

There is only one DMC configuration.

**Attributes**

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</tr>
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<td>Width</td>
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</tr>
</tbody>
</table>
3.3.419 mux_control_now

Control muxing options for the DMC. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The mux_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x11F4
Type Read-only
Reset 0x00000000
Width 32

3.3.420 rank_remap_control_now

Control register for rank remap. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rank_remap_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x11F8
Type Read-only
Reset 0x76543210
Width 32

3.3.421 t_refi_now

Configures the refresh interval timing parameter. It must be programmed to the device average all-bank AUTOREFRESH interval, divided by 8. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_refi_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1200
Type Read-only
Reset 0x00000100
Width 32
### 3.3.422 t_rfc_now

Configures the tRFC timing parameter. This determines the delay applied after an AUTOREFRESH command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rfc_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1204
- Type: Read-only
- Reset: 0x00008C23
- Width: 32

### 3.3.423 t_mrr_now

Configures the tMRR timing parameter. This determines the Mode Register Read (including Multi-Purpose Register Reads) command delay before any other command is issued to the same rank. Note: this value is used to determine the data cycles returned as a result of an MRR command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_mrr_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1208
- Type: Read-only
- Reset: 0x00000002
- Width: 32

### 3.3.424 t_mrw_now

Configures the tMRW timing parameter. This determines the delay applied after a Mode Register Write (including Multi-Purpose Register Writes) command before any other command is issued to the same rank. Note: this value is used for all delays associated with mode register write and set commands, so the largest of these delays must be programmed. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_mrw_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x120C
- Type: Read-only
- Reset: 0x0000000C
3.3.425 refresh_enable_now

Configures refresh counters. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The refresh_enable_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1210
Type Read-only
Reset 0x00000001
Width 32

3.3.426 t_rcd_now

Configures the tRCD timing parameter. This determines the delay applied after an ACTIVATE command before a READ or WRITE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rcd_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1218
Type Read-only
Reset 0x00000005
Width 32

3.3.427 t_ras_now

Configures the tRAS timing parameter. This determines the delay applied after an ACTIVATE command before a PRECHARGE command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ras_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x121C
Type Read-only
Reset 0x0000000E
Width 32
3.3.428 t_rp_now

Configures the tRP timing parameter. This determines the delay applied after a PRECHARGE command before any other command is issued to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rp_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1220
Type Read-only
Reset 0x00000005
Width 32

3.3.429 t_rpall_now

Configures the tRPALL timing parameter. This determines the delay applied after a PRECHARGEALL command before any other command is issued to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rpall_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1224
Type Read-only
Reset 0x00000005
Width 32

3.3.430 t_rrd_now

Configures the tRRD timing parameter. This determines the delay applied after an ACTIVATE command before another ACTIVATE command is issued to the same rank. The _l and _s fields apply to the same bank group, a different bank group, and different logical rank, respectively, as described in the DDR4 specification. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rrd_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1228
Type Read-only
Reset 0x04000404
Width 32
3.3.431 t_act_window_now

Configures the tFAW and tMAWi timing parameters. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER, or PAUSED states.

The t_act_window_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

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3.3.432 t_rtr_now

Configures the read-to-read timing parameter. This determines the READ to READ command delay applied between reads to the same chip, other bank group (t_rtr_s), same chip, same bank group (t_rtr_l), different chip-selects (t_rtr_cs), and same chip, different logical rank(t_rtr_dlr). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

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</tr>
</tbody>
</table>

3.3.433 t_rtw_now

Configures the read-to-write timing parameter. This determines the READ to WRITE command delay applied between issued commands to the same chip, other bank group (t_rtw_s), same chip, same bank group (t_trw_l), and other chip-selects (t_rtw_cs). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtw_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
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</tr>
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<tbody>
<tr>
<td>Type</td>
<td>Read-only</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00060606</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
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</tbody>
</table>
3.3.434  t_rtp_now

Configures the read-to-precharge timing parameter. This determines the READ to PRECHARGE command delay applied between issued commands to the same bank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rtp_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x123C
Type Read-only
Reset 0x00000004
Width 32

3.3.435  t_wr_now

Configures the tWR timing parameter. This determines the write recovery time and is used as the delay applied between the issue of a WRITE command and subsequent commands, other than WRITEs, to the same bank. Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: \( t_{wr(dmc)} = CWL + 4 + tWR(\text{from dram data sheet}) \). CWL should account for write CRC if enabled. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1244
Type Read-only
Reset 0x00000005
Width 32

3.3.436  t_wtr_now

Configures the write-to-read timing parameter, for both same chip, other bank group (tWTR_s), same chip, same bank group (t_WTR_l), and alternate chip (tWTR_cs). Note: This timing parameter is derived differently than indicated in the DRAM timing specification: It is derived from the start of the WRITE command as opposed to the end of the data burst. To program this parameter correctly the following formula should be used: \( t_{wtr(dmc)} = CWL + WBL/2 + tWR(\text{DRAM}) \). Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wtr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
### Attributes
- **Offset**: 0x1248
- **Type**: Read-only
- **Reset**: 0x00040505
- **Width**: 32

### 3.3.437 t_wtw_now
Configures the write-to-write timing parameter for same chip, other bank group (t_wtw_s), same chip, same bank group (t_wtw_l), alternate chip (t_wtw_cs) writes, same chip, different logical rank(t_wtw_dlr). Note: these must take into account CRC timing requirements. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wtw_now register characteristics are:

#### Usage constraints
There are no usage constraints.

#### Configurations
There is only one DMC configuration.

### Attributes
- **Offset**: 0x124C
- **Type**: Read-only
- **Reset**: 0x10060404
- **Width**: 32

### 3.3.438 t_clock_control_now
Configures the enter DRAM clock disable timing parameter. This parameter is applied between stopping the clock when idle, or when in a power-down state, and any subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_clock_control_now register characteristics are:

#### Usage constraints
There are no usage constraints.

#### Configurations
There is only one DMC configuration.

### Attributes
- **Offset**: 0x1250
- **Type**: Read-only
- **Reset**: 0x00000505
- **Width**: 32

### 3.3.439 t_xmpd_now
Configures the command delay between exiting Maximum Power Down and a subsequent command to that rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xmpd_now register characteristics are:

#### Usage constraints
There are no usage constraints.

#### Configurations
There is only one DMC configuration.
Attributes

Offset  0x1254
Type    Read-only
Reset   0x000003FF
Width   32

3.3.440  t_ep_now

Configures the enter power-down timing parameter. This parameter is applied between the issue of an active or precharge power down request and subsequent commands to the same rank. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ep_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset  0x1258
Type    Read-only
Reset   0x00000002
Width   32

3.3.441  t_xp_now

Configures the exit power-down timing parameter for operations that do not require a DLL (tXP), and those that do (tXPDLL). Note: t_xpdl must be greater than or equal to tRCD and tCKE, and t_xp must be greater than or equal to tMPX_S. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xp_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

Offset  0x125C
Type    Read-only
Reset   0x00000002
Width   32

3.3.442  t_esr_now

Configures the enter self-refresh timing parameter. This parameter is applied between issue of an enter self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_esr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
3.3.443 t_xsr_now

Configures the exit self-refresh timing parameter. This parameter is applied between the issue of an exit self-refresh request and subsequent commands to the same rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_xsr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1260
Type Read-only
Reset 0x0000000E
Width 32

3.3.444 t_esrck_now

Configures the delay between entering self-refresh and disabling the DRAM clock. This parameter is applied when stopping the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_esrck_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1264
Type Read-only
Reset 0x05120100
Width 32

3.3.445 t_ckxsr_now

Configures the delay between DRAM clock enable and exiting self-refresh. This parameter is applied when re-instating the clock when in self-refresh and when in a maximum power-down state. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_ckxsr_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.
Attributes
Offset 0x126C
Type Read-only
Reset 0x00000001
Width 32

3.3.446 t_cmd_now

Configures command signaling timing. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_cmd_now register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x1270
Type Read-only
Reset 0x00000000
Width 32

3.3.447 t_parity_now

Parity latencies t_parinlat and t_completion. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_parity_now register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x1274
Type Read-only
Reset 0x00000000
Width 32

3.3.448 t_zqcs_now

Configures the delay to apply following a ZQC-Short calibration command. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_zqcs_now register characteristics are:
Usage constraints
There are no usage constraints.
Configurations
There is only one DMC configuration.
Attributes
Offset 0x1278
Type Read-only
Reset 0x00000040
This timing parameter applies extra guard-band between the last issued rd/wr command and potential ZQC, SREF, and MRS commands which are issued automatically by hardware such as tpoll. This may be necessary to prevent overlap of these automated commands with ranks actively participating in non-target rank ODT (while other ranks are streaming data). ZQC, MRS, and SREF commands are typically not allowed on non-target ranks in this case as these commands could change ODT settings. In general, if non-target rank termination is used this parameter should be programmed to t_odt_off_rd/wr(max setting) + DODTLoff(from DDR4 spec) Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rw_odt_clr_now register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

- Offset: 0x127C
- Type: Read-only
- Reset: 0x00000000
- Width: 32

Determines the time between a READ command commencing on the DFI interface, and the assertion of the dfi_read_en signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_rddata_en_now register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

- Offset: 0x1300
- Type: Read-only
- Reset: 0x00000001
- Width: 32

Determines the maximum possible time between the assertion of the dfi_read_en signal, and the assertion of the dfi_rddata_valid signal by the PHY. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_phyrdlat_now register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

- Offset: 0x1304
3.3.452 t_phywrlat_now

Determines the time between a WRITE command commencing on the DFI interface, and the assertion of
the dfi_wrddata_en, dfi_wrddata_cs and dfi_wrddata signals. Access restrictions: RO Can be read from
when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or
PAUSED states.

The t_phywrlat_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1308
Type Read-only
Reset 0x00000000
Width 32

3.3.453 rdlvl_control_now

Determines the DMC behavior during read training operations. See the PHY training interface section of
the Integration Manual for more details on PHY training. Access restrictions: RO Can be read from when
in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1310
Type Read-only
Reset 0x00001080
Width 32

3.3.454 rdlvl_mrs_now

Determines the Mode Register command to use to place the DRAM into a training mode for read
training, when enabled by the rdlvl_control register. See the PHY interface section of the Integration
Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The rdlvl_mrs_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1314
3.3.455 \textbf{t_rdlvl_en now}

Configures the \textit{t_rdlvl_en} timing parameter. This specifies the cycle delay between asserting \texttt{dfi\_rdlvl\_en} and the first training command, and also the cycle delay between deasserting \texttt{dfi\_rdlvl\_en} and performing any subsequent command. It also specifies the minimum delay between training commands and refreshes during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The \textit{t_rdlvl_en_now} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}

\begin{itemize}
    \item \textbf{Offset} \hspace{1cm} 0x1318
    \item \textbf{Type} \hspace{1cm} Read-only
    \item \textbf{Reset} \hspace{1cm} 0x00000000
    \item \textbf{Width} \hspace{1cm} 32
\end{itemize}

3.3.456 \textbf{t_rdlvl_rr_now}

Configures the \textit{t_rdlvl_rr} timing parameter. This specifies the cycle delay between training commands. It also specifies the minimum delay between the last training command and deasserting \texttt{dfi\_rdlvl\_en} after observing \texttt{dfi\_rdlvl\_resp}. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The \textit{t_rdlvl_rr_now} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}

\begin{itemize}
    \item \textbf{Offset} \hspace{1cm} 0x131C
    \item \textbf{Type} \hspace{1cm} Read-only
    \item \textbf{Reset} \hspace{1cm} 0x00000000
    \item \textbf{Width} \hspace{1cm} 32
\end{itemize}

3.3.457 \textbf{wrlvl_control_now}

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The \textit{wrlvl\_control\_now} register characteristics are:

\textbf{Usage constraints}
There are no usage constraints.

\textbf{Configurations}
There is only one DMC configuration.

\textbf{Attributes}
### 3.3.458 wrlvl_mrs_now

Determines the Mode Register command that the DMC must use to put the DRAM into a training mode for write leveling. You enable this function with the wrlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wrlvl_mrs_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1320
- Type: Read-only
- Reset: 0x00101000
- Width: 32

### 3.3.459 t_wrlvl_en_now

Configures the t_wrlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wrlvl_en, the delay between asserting dfi_wrlvl_en and the first training command, the delay between deasserting dfi_wrlvl_en and de-asserting ODT, and deasserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wrlvl_en_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1324
- Type: Read-only
- Reset: 0x00000086
- Width: 32

### 3.3.460 t_wrlvl_ww_now

Configures the t_wrlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrlvl_en on observing dfi_wrlvlResp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wrlvl_ww_now register characteristics are:

**Usage constraints**
- There are no usage constraints.
Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x132C
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.461 phy_power_control_now
Configures the low-power requests made to the PHY for the different channel states. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
LOW-POWER or PAUSED states.

The phy_power_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x1348
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.462 t_lpresp_now
Configures the minimum cycle delay to apply for PHY low-power handshakes. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
LOW-POWER or PAUSED states.

The t_lpresp_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x134C
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.463 phy_update_control_now
Configures the update mechanism to use in response to PHY training requests. Access restrictions: RO
Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
LOW-POWER or PAUSED states.

The phy_update_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
3.3.464  t_odth_now

Configures the ODTH8 timing parameter as timed from Write command registered with ODT high
Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated
when in CONFIG, LOW-POWER or PAUSED states.

The t_odth_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x1350
Type    Read-only
Reset   0x2FE00000
Width   32

3.3.465  odt_timing_now

Configures the ODT on and off timing. Access restrictions: RO Can be read from when in ALL states.
Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_timing_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x1354
Type    Read-only
Reset   0x00000006
Width   32

3.3.466  odt_wr_control_31_00_now

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG,
LOW-POWER or PAUSED states.

The odt_wr_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset  0x1360
Type    Read-only
Reset   0x88840201
3.3.467  
**odt_wr_control_63_32_now**

Configures the ODT on and off settings for active and inactive ranks during writes. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The `odt_wr_control_63_32_now` register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

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</tr>
</tbody>
</table>

3.3.468  
**odt_rd_control_31_00_now**

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The `odt_rd_control_31_00_now` register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
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<th>Width</th>
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<tbody>
<tr>
<td>0x1368</td>
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<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.469  
**odt_rd_control_63_32_now**

Configures the ODT on and off settings for active and inactive ranks during reads. Access restrictions:
RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The `odt_rd_control_63_32_now` register characteristics are:

**Usage constraints**  
There are no usage constraints.

**Configurations**  
There is only one DMC configuration.

**Attributes**

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x136C</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>
3.3.470 dq_map_control_15_00_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_15_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1380
Type Read-only
Reset 0x00000000
Width 32

3.3.471 dq_map_control_31_16_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_31_16_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1384
Type Read-only
Reset 0x00000000
Width 32

3.3.472 dq_map_control_47_32_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_47_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1388
Type Read-only
3.3.473 dq_map_control_63_48_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for each nibble into the corresponding register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_63_48_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x138C
- Type Read-only
- Reset 0x00000000
- Width 32

3.3.474 dq_map_control_71_64_now

Controls the DQ mapping compensation applied for CRC calculation. For each nibble of the DQ bus, the DIMM SPD defines a DQ Map Index to define the bit connectivity to each rank. Program the DQ Map Index retrieved from the SPD for DIMM Check Bits bus into this register in the DMC for correct CRC operation. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The dq_map_control_71_64_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x1390
- Type Read-only
- Reset 0x00000000
- Width 32

3.3.475 odt_cp_control_31_00_now

Determines which of the 8 dfi_odt[7:0] output signals are connected to a logically addressed rank. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_cp_control_31_00_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset 0x13B0

3.3.476 odt_cp_control_63_32_now

Determines which of the 8 dfi_odt[7:0] output signals are driven during a write to DRAM. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The odt_cp_control_63_32_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
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<td>32</td>
</tr>
</tbody>
</table>

3.3.477 user_config0_now

Drives the output user_config0 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user_config0_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1408</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.478 user_config1_now

Drives the output user_config1 signal. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in ALL states.

The user_config1_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x140C</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>
3.3.479  **t_db_train_resp_now**

Configures the t_db_train_resp timing parameter for DB-DRAM Training. With DFI4.0 PHY this register is specified to define the cycle delay between DFI read command and when the response is valid on the dfi_db_train_resp. However this register can also be configured in DFI3.1 mode (optional: in absence of dfi_rddata_valid) to define the delay between DFI read command and when the response is valid on the dfi_rddata. This must include the whole round trip time including the board delays, take a look at DFI4.0 spec for details. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_db_train_resp_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1610
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.480  **t_lvl_disconnect_now**

Configures the t_lvl_disconnect timing parameter for all DFI training interfaces. This value should be programmed to be max of all t*lvl_disconnect and t*lvl_disconnect_error timing parameters from the PHY. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_lvl_disconnect_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1614
- Type: Read-only
- Reset: 0x0000000F
- Width: 32

3.3.481  **wdqlvl_control_now**

Determines the DMC behavior during write-DQ training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_control_now register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1620
- Type: Read-only
3.3.482 wdqlvl_vrefdq_train_mrs_now

Determines the Mode Register command to use to place the DRAM into a VrefDQ training mode as part of WrDQ training, when enabled by the wdqlvl_control register. You enable this function with the wdqlvl_control Register. See the PHY training interface section of the Integration Manual for more information. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_vrefdq_train_mrs_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1624
Type Read-only
Reset 0x00000000
Width 32

3.3.483 wdqlvl_address_31_00_now

Programs the row and column address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_address_31_00_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x1628
Type Read-only
Reset 0x00000000
Width 32

3.3.484 wdqlvl_address_63_32_now

Programs the address that is used in WrDQ training. This address is used for all ranks undergoing training Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The wdqlvl_address_63_32_now register characteristics are:

Usage constraints

There are no usage constraints.

Configurations

There is only one DMC configuration.

Attributes

Offset 0x162C
Type Read-only
Reset 0x00000000
Width 32

3.3.485 t_wdqlvl_en_now
Configures the t_wdqlvl_en timing parameter. Specifies the cycle delay between asserting ODT for training and asserting dfi_wdqlvl_en, the delay between asserting dfi_wdqlvl_en and the first training command, the delay between de-asserting dfi_wdqlvl_en and de-asserting ODT, and de-asserting ODT to any subsequent command. It is also used between ODT transitions and refreshes generated during training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_en_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1630</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.486 t_wdqlvl_ww_now
Configures the t_wdqlvl_ww timing parameter. Specifies the cycle delay between training commands. Also specifies the minimum delay between the last training command and de-asserting dfi_wrvlvl_en on observing dfi_wdqlvl_resp. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_ww_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Reset</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1634</td>
<td>Read-only</td>
<td>0x00000000</td>
<td>32</td>
</tr>
</tbody>
</table>

3.3.487 t_wdqlvl_rw_now
Configures the t_wdqlvl_rw timing parameter. Specifies the minimum numbers of clock cycles from the last read in a calibration sequence to the first write in the next set of calibration commands. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The t_wdqlvl_rw_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x1638</td>
<td></td>
</tr>
</tbody>
</table>
3.3.488  phymstr_control_now

Determines the DMC behavior during write training operations. See the PHY training interface section of the Integration Manual for more information on PHY training. Access restrictions: RO Can be read from when in ALL states. Cannot be written to and only updated when in CONFIG, LOW-POWER or PAUSED states.

The phymstr_control_now register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x1654
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.489  periph_id_4

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_4 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x1FD0
- Type: Read-only
- Reset: 0x00000014
- Width: 32

3.3.490  periph_id_0

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The periph_id_0 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
- Offset: 0x1FE0
- Type: Read-only
- Reset: 0x00000054
- Width: 32
3.3.491  **periph_id_1**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The `periph_id_1` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1FE4
- Type: Read-only
- Reset: 0x000000B4
- Width: 32

3.3.492  **periph_id_2**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The `periph_id_2` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1FE8
- Type: Read-only
- Reset: 0x0000000B
- Width: 32

3.3.493  **periph_id_3**

Peripheral ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The `periph_id_3` register characteristics are:

**Usage constraints**
- There are no usage constraints.

**Configurations**
- There is only one DMC configuration.

**Attributes**
- Offset: 0x1FEC
- Type: Read-only
- Reset: 0x00000000
- Width: 32

3.3.494  **component_id_0**

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The `component_id_0` register characteristics are:
Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1FF0
Type Read-only
Reset 0x0000000D
Width 32

3.3.495 component_id_1

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_1 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1FF4
Type Read-only
Reset 0x000000F0
Width 32

3.3.496 component_id_2

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_2 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
Offset 0x1FF8
Type Read-only
Reset 0x00000005
Width 32

3.3.497 component_id_3

Component ID register. Access restrictions: RO Can be read from when in ALL states. Cannot be changed.

The component_id_3 register characteristics are:

Usage constraints
There are no usage constraints.

Configurations
There is only one DMC configuration.

Attributes
<table>
<thead>
<tr>
<th>Offset</th>
<th>0x1FFC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>Read-only</td>
</tr>
<tr>
<td>Reset</td>
<td>0x00000081</td>
</tr>
<tr>
<td>Width</td>
<td>32</td>
</tr>
</tbody>
</table>
Appendix A

Signal descriptions

This appendix describes the DMC-620 signals.

It contains the following section:

• *A.1 Signals list on page Appx-A-210.*
A.1  Signals list

DMC signals list that excludes bus interface signals. The bus interface signals are defined by their own bus protocol standard.

The following table shows the Primary clock and reset signals bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk</td>
<td></td>
<td>Primary DMC clock</td>
</tr>
<tr>
<td>resetn</td>
<td></td>
<td>Primary DMC reset</td>
</tr>
</tbody>
</table>

The following table shows the Divided Primary DMC clock. Edge Synchronous, half the frequency of clk bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>clkdiv2</td>
<td></td>
<td>Primary DMC clock. Edge Synchronous, half the frequency of clk</td>
</tr>
<tr>
<td>resetn</td>
<td></td>
<td>Primary DMC reset</td>
</tr>
</tbody>
</table>

The following table shows the APB clock and reset signals bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>pclk</td>
<td></td>
<td>APB clock</td>
</tr>
<tr>
<td>presetn</td>
<td></td>
<td>APB reset</td>
</tr>
</tbody>
</table>

The following table shows the APB Interface bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>paddr</td>
<td>32</td>
<td>APB address</td>
</tr>
<tr>
<td>psel</td>
<td></td>
<td>APB select</td>
</tr>
<tr>
<td>penable</td>
<td></td>
<td>APB enable</td>
</tr>
<tr>
<td>pwrite</td>
<td></td>
<td>APB write</td>
</tr>
<tr>
<td>pwddata</td>
<td>32</td>
<td>APB write data</td>
</tr>
<tr>
<td>pready</td>
<td></td>
<td>APB ready</td>
</tr>
<tr>
<td>prdata</td>
<td>32</td>
<td>APB read data</td>
</tr>
<tr>
<td>pslverr</td>
<td></td>
<td>APB error signal</td>
</tr>
</tbody>
</table>

The following table shows the DFI Interface bus list of the DMC.
## Table A-5  DMC DFI Interface list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_address_p0</td>
<td>18</td>
<td>Address to DDR3 PHY</td>
</tr>
<tr>
<td>dfi_address_p1</td>
<td>18</td>
<td>Address to DDR3 PHY</td>
</tr>
<tr>
<td>dfi_bank_p0</td>
<td>3</td>
<td>Bank Address to PHY</td>
</tr>
<tr>
<td>dfi_bank_p1</td>
<td>3</td>
<td>Bank Address to PHY</td>
</tr>
<tr>
<td>dfi_ras_n_p0</td>
<td>1</td>
<td>Row address strobe to PHY</td>
</tr>
<tr>
<td>dfi_ras_n_p1</td>
<td>1</td>
<td>Row address strobe to PHY</td>
</tr>
<tr>
<td>dfi_cas_n_p0</td>
<td>1</td>
<td>Column address strobe to PHY</td>
</tr>
<tr>
<td>dfi_cas_n_p1</td>
<td>1</td>
<td>Column address strobe to PHY</td>
</tr>
<tr>
<td>dfi_we_n_p0</td>
<td>1</td>
<td>Write enable to PHY</td>
</tr>
<tr>
<td>dfi_we_n_p1</td>
<td>1</td>
<td>Write enable to PHY</td>
</tr>
<tr>
<td>dfi_cs_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_cs_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_act_n_p0</td>
<td>1</td>
<td>Activate to PHY</td>
</tr>
<tr>
<td>dfi_act_n_p1</td>
<td>1</td>
<td>Activate to PHY</td>
</tr>
<tr>
<td>dfi_bg_p0</td>
<td>2</td>
<td>Bank group address to PHY</td>
</tr>
<tr>
<td>dfi_bg_p1</td>
<td>2</td>
<td>Bank group address to PHY</td>
</tr>
<tr>
<td>dfi_cid_p0</td>
<td>3</td>
<td>Chip ID to PHY</td>
</tr>
<tr>
<td>dfi_cid_p1</td>
<td>3</td>
<td>Chip ID to PHY</td>
</tr>
<tr>
<td>dficke_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Clock enable to PHY</td>
</tr>
<tr>
<td>dficke_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Clock enable to PHY</td>
</tr>
<tr>
<td>dfi_odt_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>On Die Termination to PHY</td>
</tr>
<tr>
<td>dfi_odt_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>On Die Termination to PHY</td>
</tr>
<tr>
<td>dfi_reset_n_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Reset to PHY</td>
</tr>
<tr>
<td>dfi_reset_n_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Reset to PHY</td>
</tr>
<tr>
<td>dfi_parity_in_p0</td>
<td>1</td>
<td>Command parity to PHY</td>
</tr>
<tr>
<td>dfi_parity_in_p1</td>
<td>1</td>
<td>Command parity to PHY</td>
</tr>
<tr>
<td>dfi_wrdata_en_p0</td>
<td>(DFI_DATA_SLICES)</td>
<td>Write data enable PHY</td>
</tr>
<tr>
<td>dfi_wrdata_en_p1</td>
<td>(DFI_DATA_SLICES)</td>
<td>Write data enable PHY</td>
</tr>
<tr>
<td>dfi_wrdata_p0</td>
<td>(DFI_DATA_BITS/2)</td>
<td>Write data to PHY</td>
</tr>
<tr>
<td>dfi_wrdata_p1</td>
<td>(DFI_DATA_BITS/2)</td>
<td>Write data to PHY</td>
</tr>
<tr>
<td>dfi_wrdata_cs_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Write Data Path Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_wrdata_cs_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Write Data Path Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_wrdata_mask_p0</td>
<td>(DFI_DATA_BYTES/2)</td>
<td>Write data mask PHY</td>
</tr>
<tr>
<td>dfi_wrdata_mask_p1</td>
<td>(DFI_DATA_BYTES/2)</td>
<td>Write data mask PHY</td>
</tr>
<tr>
<td>dfi_rddata_en_p0</td>
<td>(DFI_DATA_SLICES)</td>
<td>Enable for read data</td>
</tr>
<tr>
<td>Name</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>----------------------</td>
<td>------------------------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td>dfi_rddata_en_p1</td>
<td>(DFI_DATA_SLICES)</td>
<td>Enable for read data</td>
</tr>
<tr>
<td>dfi_rddata_p0</td>
<td>(DFI_DATA_BITS/2)</td>
<td>Read data input from PHY</td>
</tr>
<tr>
<td>dfi_rddata_p1</td>
<td>(DFI_DATA_BITS/2)</td>
<td>Read data input from PHY</td>
</tr>
<tr>
<td>dfi_rddata_dbp_p0</td>
<td>(DFI_DATA_SLICES*2)</td>
<td>Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.</td>
</tr>
<tr>
<td>dfi_rddata_dbp_p1</td>
<td>(DFI_DATA_SLICES*2)</td>
<td>Read Data DBI. This signal is sent with dfi_rddata bus indicating DBI functionality. If not used this signal must be tied to 'b1.</td>
</tr>
<tr>
<td>dfi_rddata_valid_p0</td>
<td>(DFI_DATA_SLICES)</td>
<td>Indicates read data valid</td>
</tr>
<tr>
<td>dfi_rddata_valid_p1</td>
<td>(DFI_DATA_SLICES)</td>
<td>Indicates read data valid</td>
</tr>
<tr>
<td>dfi_rddata_cs_p0</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Read Data Path Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_rddata_cs_p1</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>Read Data Path Chip-select to PHY</td>
</tr>
<tr>
<td>dfi_ctrlupd_req</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_ctrlupd_ack</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phyupd_req</td>
<td>1</td>
<td>DFI PHY-initiated update request</td>
</tr>
<tr>
<td>dfi_phyupd_ack</td>
<td>1</td>
<td>DFI PHY-initiated update acknowledge</td>
</tr>
<tr>
<td>dfi_phyupd_type</td>
<td>2</td>
<td>DFI PHY-initiated update type</td>
</tr>
<tr>
<td>dfi_data_byte_disable</td>
<td>(DFI_DATA_BYTES/2)</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_dram_clk_disable</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>DRAM clock disable to PHY</td>
</tr>
<tr>
<td>dfi_init_start</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_init_complete</td>
<td>1</td>
<td>Indicates PHY initialization complete</td>
</tr>
<tr>
<td>dfi_alert_n_p0</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see JEDEC specification for details.</td>
</tr>
<tr>
<td>dfi_alert_n_p1</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see JEDEC specification for details.</td>
</tr>
<tr>
<td>dfi_frequency</td>
<td>5</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_geardown_en</td>
<td>1</td>
<td>This signal is part of DFI 4.0 Geardown Interface.</td>
</tr>
<tr>
<td>dfi_err</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_err_info</td>
<td>4</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_disconnect_error</td>
<td>1</td>
<td>Provides Disconnect type if a disconnect occurs on training, update, or PHY-master interface. This signal is part of DFI 4.0 Disconnect Interface.</td>
</tr>
<tr>
<td>dfi_phymstr_req</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phymstr_cs_state</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phymstr_state_sel</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phymstr_type</td>
<td>2</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>Name</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>----------------------</td>
<td>-------------------------------</td>
<td>--------------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>dfi_phymstr_ack</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phylvl_req_cs_n</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>This signal is part of DFI 3.1, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_phylvl_ack_cs_n</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>This signal is part of DFI 3.1, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_rdlvl_req</td>
<td>DFI_DATA_SLICES</td>
<td>DFI read data training request</td>
</tr>
<tr>
<td>dfi_rdlvl_cs</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>DFI read data training request chip-select</td>
</tr>
<tr>
<td>dfi_rdlvl_en</td>
<td>DFI_DATA_SLICES</td>
<td>DFI read data training enable</td>
</tr>
<tr>
<td>dfi_rdlvl_resp</td>
<td>(DFI_DATA_SLICES*2)</td>
<td>DFI read data training response</td>
</tr>
<tr>
<td>dfi_rdlvl_done</td>
<td>DFI_DATA_SLICES</td>
<td>DFI Read data training done</td>
</tr>
<tr>
<td>dfi_rdlvl_gate_req</td>
<td>DFI_DATA_SLICES</td>
<td>DFI read gate training request</td>
</tr>
<tr>
<td>dfi_rdlvl_gate_cs</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>DFI read gate training request chip-select</td>
</tr>
<tr>
<td>dfi_rdlvl_gate_en</td>
<td>DFI_DATA_SLICES</td>
<td>DFI read gate training enable</td>
</tr>
<tr>
<td>dfi_wrlvl_req</td>
<td>DFI_DATA_SLICES</td>
<td>DFI write leveling training request</td>
</tr>
<tr>
<td>dfi_wrlvl_cs</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>DFI write leveling training request chip-select</td>
</tr>
<tr>
<td>dfi_wrlvl_en</td>
<td>DFI_DATA_SLICES</td>
<td>DFI write leveling training enable</td>
</tr>
<tr>
<td>dfi_wrlvl_strobe_p0</td>
<td>DFI_DATA_SLICES</td>
<td>DFI write leveling training strobe</td>
</tr>
<tr>
<td>dfi_wrlvl_strobe_p1</td>
<td>DFI_DATA_SLICES</td>
<td>DFI write leveling training strobe</td>
</tr>
<tr>
<td>dfi_wrlvl_resp</td>
<td>DFI_DATA_SLICES</td>
<td>DFI write leveling training response</td>
</tr>
<tr>
<td>dfi_wdqlvl_req</td>
<td>DFI_DATA_SLICES</td>
<td>DFI Write-DQ leveling training request</td>
</tr>
<tr>
<td>dfi_wdqlvl_cs</td>
<td>MEMORY_CHIP_SELECTS</td>
<td>DFI Write-DQ leveling training request chip-select</td>
</tr>
<tr>
<td>dfi_wdqlvl_en</td>
<td>DFI_DATA_SLICES</td>
<td>DFI Write-DQ leveling training enable</td>
</tr>
<tr>
<td>dfi_wdqlvl_result</td>
<td>DFI_DATA_SLICES</td>
<td>DFI Write-DQ leveling training result</td>
</tr>
<tr>
<td>dfi_wdqlvl_done</td>
<td>DFI_DATA_SLICES</td>
<td>DFI Write-DQ leveling training done</td>
</tr>
<tr>
<td>dfi_wdqlvl_resp</td>
<td>(DFI_DATA_SLICES*2)</td>
<td>DFI Write-DQ leveling training response</td>
</tr>
<tr>
<td>dfi_lvl_pattern</td>
<td>4</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_lvl_periodic</td>
<td>1</td>
<td>This signal is part of DFI 4.0, see DFI specification for details.</td>
</tr>
<tr>
<td>dfi_db_train_en</td>
<td>DFI_DATA_SLICES</td>
<td>Enable for DB-DRAM Training. This signal is part of DFI 4.0 DB-DRAM Training.</td>
</tr>
<tr>
<td>dfi_db_train_resp_w0</td>
<td>(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)</td>
<td>Response data for DB-DRAM Training. This signal is part of DFI 4.0.</td>
</tr>
<tr>
<td>dfi_db_train_resp_w1</td>
<td>(DFI_DATA_SLICES*DFI_SLICE_WIDTH/4)</td>
<td>Response data for DB-DRAM Training. This signal is part of DFI 4.0.</td>
</tr>
<tr>
<td>dfi_lp_ctrl_req</td>
<td>1</td>
<td>DFI command low-power request</td>
</tr>
<tr>
<td>dfi_lp_data_req</td>
<td>1</td>
<td>DFI data low-power request</td>
</tr>
<tr>
<td>dfi_lp_wakeup</td>
<td>4</td>
<td>DFI command low-power PHY wakeup allowance</td>
</tr>
<tr>
<td>dfi_lp_ack</td>
<td>1</td>
<td>DFI command low-power acknowledge</td>
</tr>
</tbody>
</table>
The following table shows the Q-Channel Interface for DMC bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>qreqn</td>
<td>1</td>
<td>Request from the external clock controller to prepare to stop the clock</td>
</tr>
<tr>
<td>qacceptn</td>
<td>1</td>
<td>Positive acknowledgement after receiving QREQn assertion indicating that the DMC has completed preparation to stop the clocks and that the external clock controller can stop the clock</td>
</tr>
<tr>
<td>qdeny</td>
<td>1</td>
<td>Negative acknowledgement after receiving QREQn assertion indicating that the DMC has refused the request from the external clock controller to prepare to stop the clock</td>
</tr>
<tr>
<td>qactive</td>
<td>1</td>
<td>Indication that the DMC is active</td>
</tr>
</tbody>
</table>

The following table shows the Q-Channel Interface for APB interface bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>qreqn_apb</td>
<td>1</td>
<td>Request from the external clock controller to prepare to stop the clock</td>
</tr>
<tr>
<td>qacceptn_apb</td>
<td>1</td>
<td>Positive acknowledgement after receiving QREQn assertion indicating that the APB interface has completed preparation to stop the clocks and that the external clock controller can stop the clock</td>
</tr>
<tr>
<td>qdeny_apb</td>
<td>1</td>
<td>Negative acknowledgement after receiving QREQn assertion indicating that the APB interface has refused the request from the external clock controller to prepare to stop the clock</td>
</tr>
<tr>
<td>qactive_apb</td>
<td>1</td>
<td>Indication that the APB interface is active</td>
</tr>
</tbody>
</table>

The following table shows the Clock Frequency Change Interface bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>cc_frequency</td>
<td>5</td>
<td>Used to indicate new frequency as part of frequency change protocol</td>
</tr>
<tr>
<td>cc_freq_change_req</td>
<td>1</td>
<td>Signals to an external clock control that the clock frequency can be updated</td>
</tr>
<tr>
<td>cc_freq_change_ack</td>
<td>1</td>
<td>Signals to the DMC from an external clock control that the clock frequency has been updated</td>
</tr>
</tbody>
</table>

The following table shows the Abort Interface bus list of the DMC.

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_frequency</td>
<td>5</td>
<td>Used to indicate new frequency as part of frequency change protocol</td>
</tr>
<tr>
<td>dfi_freq_change_req</td>
<td>1</td>
<td>Signals to an external clock control that the clock frequency can be updated</td>
</tr>
<tr>
<td>dfi_freq_change_ack</td>
<td>1</td>
<td>Signals to the DMC from an external clock control that the clock frequency has been updated</td>
</tr>
</tbody>
</table>
### Table A-10  DMC Abort Interface list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>abort_req</td>
<td>1</td>
<td>An input to abort retries in the face of DFI link errors.</td>
</tr>
<tr>
<td>abort_err_type</td>
<td>1</td>
<td>Abort Error Type as a payload to abort_req.</td>
</tr>
<tr>
<td>abort_ack</td>
<td>1</td>
<td>An output to acknowledge that the DMC has completed outstanding transactions as a result of an abort.</td>
</tr>
</tbody>
</table>

The following table shows the Memory BIST interface bus list of the DMC.

### Table A-11  DMC Memory BIST interface list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>mbistresetn</td>
<td>1</td>
<td>MBIST reset. Active low.</td>
</tr>
<tr>
<td>mbistreq</td>
<td>1</td>
<td>MBIST request</td>
</tr>
<tr>
<td>mbistack</td>
<td>1</td>
<td>MBIST acknowledge</td>
</tr>
<tr>
<td>mbistwriteen</td>
<td>1</td>
<td>MBIST write enable</td>
</tr>
<tr>
<td>mbistreaden</td>
<td>1</td>
<td>MBIST read enable</td>
</tr>
<tr>
<td>mbistaddr</td>
<td>MAX_TID_BITS</td>
<td>MBIST address</td>
</tr>
<tr>
<td>mbistarray</td>
<td>4</td>
<td>MBIST array selection</td>
</tr>
<tr>
<td>mbistcfg</td>
<td>1</td>
<td>MBIST Configuration</td>
</tr>
<tr>
<td>mbistindata</td>
<td>154</td>
<td>MBIST write data</td>
</tr>
<tr>
<td>mbistoutdata</td>
<td>154</td>
<td>MBIST read data</td>
</tr>
</tbody>
</table>

The following table shows the DFT interface bus list of the DMC.

### Table A-12  DMC DFT interface list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DFTCLKCGEN</td>
<td>1</td>
<td>DFT clock gate override</td>
</tr>
<tr>
<td>DFTRSTDISABLE</td>
<td>2</td>
<td>DFT reset synchronizer disable</td>
</tr>
<tr>
<td>DFTRAMHOLD</td>
<td>1</td>
<td>DFT on-chip RAM hold</td>
</tr>
<tr>
<td>DFTMCPSHOLD</td>
<td>1</td>
<td>DFT multicycle path hold</td>
</tr>
</tbody>
</table>

The following table shows the user-defined inputs bus list of the DMC.

### Table A-13  DMC user-defined inputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_status</td>
<td>32</td>
<td>User-defined inputs</td>
</tr>
</tbody>
</table>

The following table shows the user-defined outputs bus list of the DMC.

### Table A-14  DMC user-defined outputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config0</td>
<td>32</td>
<td>User-defined outputs</td>
</tr>
</tbody>
</table>
The following table shows the user-defined outputs bus list of the DMC.

Table A-15  DMC user-defined outputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config1</td>
<td>32</td>
<td>User-defined outputs</td>
</tr>
</tbody>
</table>

The following table shows the user-defined outputs bus list of the DMC.

Table A-16  DMC user-defined outputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config2</td>
<td>32</td>
<td>User-defined outputs</td>
</tr>
</tbody>
</table>

The following table shows the user-defined outputs bus list of the DMC.

Table A-17  DMC user-defined outputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config3</td>
<td>32</td>
<td>User-defined outputs</td>
</tr>
</tbody>
</table>

The following table shows the Direct command event trigger inputs bus list of the DMC.

Table A-18  DMC Direct command event trigger inputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>direct_cmd_event_in</td>
<td>4</td>
<td>Direct command event trigger inputs</td>
</tr>
</tbody>
</table>

The following table shows the Direct command event triggered outputs bus list of the DMC.

Table A-19  DMC Direct command event triggered outputs list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>direct_cmd_event_out</td>
<td>4</td>
<td>Direct command event triggered outputs</td>
</tr>
</tbody>
</table>

The following table shows the memory_type bus list of the DMC.

Table A-20  DMC memory_type list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>memory_type</td>
<td>3</td>
<td>An external output of the value of the memory_type register bitfield.</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the value of CMOD in the periph_id_3 bitfield bus list of the DMC.

Table A-21  DMC Tie-off value to set the value of CMOD in the periph_id_3 bitfield list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_periph_id_3</td>
<td>8</td>
<td>Tie-off value to set the value of CMOD in the periph_id_3 bitfield</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_rddata_en_diff bus list of the DMC.
Table A-22  DMC Tie-off value for reset of register bitfield t_rddata_en_diff list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_rddata_en_diff_tie_off</td>
<td>6</td>
<td>Tie-off value for reset of register bitfield t_rddata_en_diff</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_phyrdsclat bus list of the DMC.

Table A-23  DMC Tie-off value for reset of register bitfield t_phyrdsclat list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_phyrdsclat_tie_off</td>
<td>5</td>
<td>Tie-off value for reset of register bitfield t_phyrdsclat</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_phyrdlat bus list of the DMC.

Table A-24  DMC Tie-off value for reset of register bitfield t_phyrdlat list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_phyrdlat_tie_off</td>
<td>7</td>
<td>Tie-off value for reset of register bitfield t_phyrdlat</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_phywrlat_diff bus list of the DMC.

Table A-25  DMC Tie-off value for reset of register bitfield t_phywrlat_diff list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_phywrlat_diff_tie_off</td>
<td>5</td>
<td>Tie-off value for reset of register bitfield t_phywrlat_diff</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_phywrclat bus list of the DMC.

Table A-26  DMC Tie-off value for reset of register bitfield t_phywrclat list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_phywrclat_tie_off</td>
<td>5</td>
<td>Tie-off value for reset of register bitfield t_phywrclat</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_phywrdata bus list of the DMC.

Table A-27  DMC Tie-off value for reset of register bitfield t_phywrdata list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_phywrdata_tie_off</td>
<td>1</td>
<td>Tie-off value for reset of register bitfield t_phywrdata</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield refresh_dur_rdlvl bus list of the DMC.

Table A-28  DMC Tie-off value for reset of register bitfield refresh_dur_rdlvl list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>refresh_dur_rdlvl_tie_off</td>
<td>1</td>
<td>Tie-off value for reset of register bitfield refresh_dur_rdlvl</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_rdlvl_en bus list of the DMC.
Table A-29  DMC Tie-off value for reset of register bitfield t_rdlvl_en list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_rdlvl_en_tie_off</td>
<td>6</td>
<td>Tie-off value for reset of register bitfield t_rdlvl_en</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_rdlvl_rr bus list of the DMC.

Table A-30  DMC Tie-off value for reset of register bitfield t_rdlvl_rr list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_rdlvl_rr_tie_off</td>
<td>10</td>
<td>Tie-off value for reset of register bitfield t_rdlvl_rr</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield refresh_dur_wrlvl bus list of the DMC.

Table A-31  DMC Tie-off value for reset of register bitfield refresh_dur_wrlvl list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>refresh_dur_wrlvl_tie_off</td>
<td>1</td>
<td>Tie-off value for reset of register bitfield refresh_dur_wrlvl</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_wrlvl_en bus list of the DMC.

Table A-32  DMC Tie-off value for reset of register bitfield t_wrlvl_en list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_wrlvl_en_tie_off</td>
<td>6</td>
<td>Tie-off value for reset of register bitfield t_wrlvl_en</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_wrlvl_ww bus list of the DMC.

Table A-33  DMC Tie-off value for reset of register bitfield t_wrlvl_ww list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_wrlvl_ww_tie_off</td>
<td>10</td>
<td>Tie-off value for reset of register bitfield t_wrlvl_ww</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield refresh_dur_wrlvl bus list of the DMC.

Table A-34  DMC Tie-off value for reset of register bitfield refresh_dur_wrlvl list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>refresh_dur_wdqlvl_tie_off</td>
<td>1</td>
<td>Tie-off value for reset of register bitfield refresh_dur_wrlvl</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_ww bus list of the DMC.

Table A-35  DMC Tie-off value for reset of register bitfield t_wdqlvl_ww list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_wdqlvl_ww_tie_off</td>
<td>10</td>
<td>Tie-off value for reset of register bitfield t_wdqlvl_ww</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_rw bus list of the DMC.
Table A-36  DMC Tie-off value for reset of register bitfield t_wdqlvl_rw list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_wdqlvl_rw_tie_off</td>
<td>10</td>
<td>Tie-off value for reset of register bitfield t_wdqlvl_rw</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_wdqlvl_en bus list of the DMC.

Table A-37  DMC Tie-off value for reset of register bitfield t_wdqlvl_en list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_wdqlvl_en_tie_off</td>
<td>6</td>
<td>Tie-off value for reset of register bitfield t_wdqlvl_en</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield refresh_dur_phymstr bus list of the DMC.

Table A-38  DMC Tie-off value for reset of register bitfield refresh_dur_phymstr list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>refresh_dur_phymstr_tie_off</td>
<td>1</td>
<td>Tie-off value for reset of register bitfield refresh_dur_phymstr</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_db_train_resp bus list of the DMC.

Table A-39  DMC Tie-off value for reset of register bitfield t_db_train_resp list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_db_train_resp_tie_off</td>
<td>7</td>
<td>Tie-off value for reset of register bitfield t_db_train_resp</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield t_lpresp bus list of the DMC.

Table A-40  DMC Tie-off value for reset of register bitfield t_lpresp list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>t_lpresp_tie_off</td>
<td>6</td>
<td>Tie-off value for reset of register bitfield t_lpresp</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield user_config0 bus list of the DMC.

Table A-41  DMC Tie-off value for reset of register bitfield user_config0 list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config0_tie_off</td>
<td>32</td>
<td>Tie-off value for reset of register bitfield user_config0</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield user_config1 bus list of the DMC.

Table A-42  DMC Tie-off value for reset of register bitfield user_config1 list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config1_tie_off</td>
<td>32</td>
<td>Tie-off value for reset of register bitfield user_config1</td>
</tr>
</tbody>
</table>
The following table shows the Tie-off value for reset of register bitfield user_config2 bus list of the DMC.

**Table A-43  DMC Tie-off value for reset of register bitfield user_config2 list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config2_tie_off</td>
<td>32</td>
<td>Tie-off value for reset of register bitfield user_config2</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value for reset of register bitfield user_config3 bus list of the DMC.

**Table A-44  DMC Tie-off value for reset of register bitfield user_config3 list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>user_config3_tie_off</td>
<td>32</td>
<td>Tie-off value for reset of register bitfield user_config3</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the physical node ID of the DMC bus list of the DMC.

**Table A-45  DMC Tie-off value to set the physical node ID of the DMC list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>system_id</td>
<td>CHI_RSP_FLIT_SRCID_WIDTH</td>
<td>Tie-off value to set the physical node ID of the DMC</td>
</tr>
</tbody>
</table>

The following table shows the Tie off value to specify the concatenated physical node IDs of up to SYSTEM_REQUESTORS Home Nodes that are permitted to access the DMC. SYSTEM_REQUESTORS is 8 when configured as DMC_CHIB==0, and is 32 when configured as DMC_CHIB==1. Bus list of the DMC.

**Table A-46  DMC Tie off value to specify the concatenated physical node IDs list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>home_node_id</td>
<td>(CHI_REQ_FLIT_SRCID_WIDTH*SYSTEM_REQUESTORS)</td>
<td>Tie off value to specify the concatenated physical node IDs of the requestors that are permitted to access the DMC</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring bus list of the DMC.

**Table A-47  DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_rdlvl_periodic</td>
<td>1</td>
<td>Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_req is occurring</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring bus list of the DMC.

**Table A-48  DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring list**

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_rdlvl_gate_periodic</td>
<td>1</td>
<td>Tie-off value to set the value for dfi_lvl_periodic when a dfi_rdlvl_gate_req is occurring</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring bus list of the DMC.
**Table A-49** DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_wrlvl_periodic</td>
<td>1</td>
<td>Tie-off value to set the value for dfi_lvl_periodic when a dfi_wrlvl_req is occurring</td>
</tr>
</tbody>
</table>

The following table shows the Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring bus list of the DMC.

**Table A-50** DMC Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>dfi_wdqlvl_periodic</td>
<td>1</td>
<td>Tie-off value to set the value for dfi_lvl_periodic when a dfi_wdqlvl_req is occurring</td>
</tr>
</tbody>
</table>

The following table shows the interrupt signal list of the DMC.

**Table A-51** DMC interrupts list

<table>
<thead>
<tr>
<th>Name</th>
<th>Width</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>er_int</td>
<td>1</td>
<td>The DMC has detected an uncorrectable error or previously poisoned data that cannot be deferred</td>
</tr>
<tr>
<td>cfb_int</td>
<td>1</td>
<td>The number of correctable errors detected by the DMC has overflowed an error counter</td>
</tr>
<tr>
<td>fh_int</td>
<td>1</td>
<td>The DMC has detected a new (non-poisoned) data failure that cannot be corrected, but might be able to be deferred</td>
</tr>
<tr>
<td>failed_access_int</td>
<td>1</td>
<td>The DMC has detected a system request that has failed a permissions check</td>
</tr>
<tr>
<td>failed_prog_int</td>
<td>1</td>
<td>The DMC has detected a programming request that is not permitted</td>
</tr>
<tr>
<td>link_err_int</td>
<td>1</td>
<td>The DRAM interface has suffered from a link failure and a recovery attempt has begun</td>
</tr>
<tr>
<td>temperature_event_int</td>
<td>1</td>
<td>The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor</td>
</tr>
<tr>
<td>arch_fsm_int</td>
<td>1</td>
<td>The DMC has detected a change in the architectural state</td>
</tr>
<tr>
<td>scrub_engine0_complete_int</td>
<td>1</td>
<td>The DMC scrub engine 0 has completed a scrub</td>
</tr>
<tr>
<td>scrub_engine1_complete_int</td>
<td>1</td>
<td>The DMC scrub engine 1 has completed a scrub</td>
</tr>
<tr>
<td>scrub_engine_behind_schedule_int</td>
<td>1</td>
<td>A DMC scrub engine is behind schedule</td>
</tr>
<tr>
<td>phy_request_int</td>
<td>1</td>
<td>The DMC has detected a PHY request</td>
</tr>
<tr>
<td>combined_int</td>
<td>1</td>
<td>A combined interrupt that is the logical OR of the other interrupts</td>
</tr>
<tr>
<td>failed_access_oflow</td>
<td>1</td>
<td>The DMC has detected a system request that has failed a permissions check and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td>failed_prog_oflow</td>
<td>1</td>
<td>The DMC has detected a programming request that is not permitted and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td>link_err_oflow</td>
<td>1</td>
<td>The DRAM interface has suffered from a link failure and a recovery attempt has begun and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td>temperature_event_oflow</td>
<td>1</td>
<td>The DMC has detected a temperature event signaled by the DRAM, either directly, or if a temperature delta has been observed through automated polling of the temperature sensor and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td>Name</td>
<td>Width</td>
<td>Description</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-------</td>
<td>-----------------------------------------------------------------------------</td>
</tr>
<tr>
<td><code>arch fsm oflow</code></td>
<td>1</td>
<td>The DMC has detected a change in the architectural state and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td><code>scrub_engine0_complete oflow</code></td>
<td>1</td>
<td>The DMC scrub engine 0 has completed a scrub and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td><code>scrub_engine1_complete oflow</code></td>
<td>1</td>
<td>The DMC scrub engine 1 has completed a scrub and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td><code>scrub_engine_behind_schedule oflow</code></td>
<td>1</td>
<td>A DMC scrub engine is behind schedule and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td><code>phy_request oflow</code></td>
<td>1</td>
<td>The DMC has detected a PHY request and a previously detected assertion was not cleared</td>
</tr>
<tr>
<td><code>combined oflow</code></td>
<td>1</td>
<td>A combined interrupt that is the logical OR of the other interrupt overflows.</td>
</tr>
<tr>
<td><code>pmu_counter oflow</code></td>
<td>1</td>
<td>An interrupt that indicates at least one PMU counter has overflowed</td>
</tr>
</tbody>
</table>
Appendix B
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:
• *B.1 Revisions* on page Appx-B-224.
B.1 Revisions

This appendix describes the technical changes between released issues of this book.

Table B-1  Issue 0000-00

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>First release</td>
<td>-</td>
<td>All revisions.</td>
</tr>
</tbody>
</table>

Table B-2  Differences between issue 0000-00 and issue 0000-01

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>No technical changes.</td>
<td>-</td>
<td>All revisions.</td>
</tr>
</tbody>
</table>

Table B-3  Differences between issue 0000-01 and issue 0000-02

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>No technical changes.</td>
<td>-</td>
<td>All revisions.</td>
</tr>
</tbody>
</table>

Table B-4  Differences between issue 0000-02 and issue 0100-00

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Updated Configurable options.</td>
<td>1.5 Configurable options on page 1-16</td>
<td>r1p0.</td>
</tr>
<tr>
<td>Product revisions have been updated for r1p0.</td>
<td>1.8 Product revisions on page 1-20</td>
<td>r1p0.</td>
</tr>
<tr>
<td>References to CHI-C support have been added.</td>
<td>• 1.2 DMC-620 compliance on page 1-13</td>
<td>r1p0.</td>
</tr>
<tr>
<td></td>
<td>• 1.3 Features on page 1-14</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• 1.4 Interfaces on page 1-15</td>
<td></td>
</tr>
</tbody>
</table>