Arm® Versatile™ Express Cortex® Prototyping System (MPS3)

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This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

The system should be powered down when not in use.

It is recommended that ESD precautions be taken when handling Versatile™ Express boards.

The motherboard generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. There is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the target board
- Reorient the receiving antenna
- Increase the distance between the equipment and the receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

Note
It is recommended that wherever possible shielded interface cables be used.
Contents


Preface

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>About this book</td>
<td>7</td>
</tr>
<tr>
<td>Feedback</td>
<td>10</td>
</tr>
</tbody>
</table>

Chapter 1 Introduction

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 Precautions</td>
<td>1-12</td>
</tr>
<tr>
<td>1.2 About the MPS3 motherboard</td>
<td>1-13</td>
</tr>
<tr>
<td>1.3 Location of components on the MPS3 motherboard</td>
<td>1-15</td>
</tr>
</tbody>
</table>

Chapter 2 Hardware description

<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 Overview of the board hardware</td>
<td>2-17</td>
</tr>
<tr>
<td>2.2 Example Cortex®-M33 IoT Kit subsystem design</td>
<td>2-21</td>
</tr>
<tr>
<td>2.3 Clocks</td>
<td>2-23</td>
</tr>
<tr>
<td>2.4 Reset, powerup, and configuration</td>
<td>2-25</td>
</tr>
<tr>
<td>2.5 Power</td>
<td>2-27</td>
</tr>
<tr>
<td>2.6 Serial Configuration Controller interface</td>
<td>2-28</td>
</tr>
<tr>
<td>2.7 MCC-SMC interface</td>
<td>2-30</td>
</tr>
<tr>
<td>2.8 USB 2.0 and Ethernet static memory interface</td>
<td>2-35</td>
</tr>
<tr>
<td>2.9 Video HDLCD interface</td>
<td>2-36</td>
</tr>
<tr>
<td>2.10 Audio codec interface</td>
<td>2-37</td>
</tr>
<tr>
<td>2.11 QVGA video CLCD display</td>
<td>2-38</td>
</tr>
<tr>
<td>2.12 On-board user components</td>
<td>2-39</td>
</tr>
</tbody>
</table>
2.13 Interrupts ............................................................................................................. 2-40
2.14 FPGA DDR4 memory interface ........................................................................ 2-41
2.15 User non-volatile memory ............................................................................. 2-42
2.16 Arduino Shield and Pmod interfaces ............................................................ 2-43
2.17 FMC-HPC interface ...................................................................................... 2-46
2.18 System debug .................................................................................................. 2-49
2.19 Design settings for correct board operation with a minimal design .......... 2-52

**Chapter 3**

**Configuration**

3.1 Overview of the configuration system .......................................................... 3-54
3.2 Powerup and configuration sequence ............................................................ 3-56
3.3 Reset push buttons ....................................................................................... 3-59
3.4 Configuration files ........................................................................................ 3-61

**Appendix A**

**Signal descriptions**

A.1 Debug connectors .......................................................................................... Appx-A-66
A.2 Arduino Shield connectors ........................................................................... Appx-A-71
A.3 Peripheral Module (Pmod) connectors ...................................................... Appx-A-75
A.4 FMC-HPC connector ................................................................................. Appx-A-77
A.5 FMC configuration connector ................................................................... Appx-A-78
A.6 Combined Ethernet and dual USB-A connector ........................................ Appx-A-79
A.7 HDMI Type A female connector ................................................................. Appx-A-80
A.8 Audio connectors, stacked stereo jacks ...................................................... Appx-A-81
A.9 12V power connector .................................................................................. Appx-A-82

**Appendix B**

**Specifications**

B.1 Available power for expansion boards ....................................................... Appx-B-84

**Appendix C**

**Revisions**

C.1 Revisions ...................................................................................................... Appx-C-86
Preface

This preface introduces the Arm® Versatile™ Express Cortex® Prototyping System (MPS3) Technical Reference Manual.

It contains the following:
- About this book on page 7.
- Feedback on page 10.
About this book

This book describes the Arm® Versatile™ Express Cortex® Prototyping Systems, that is, the MPS3 FPGA motherboard.

Product revision status

The rm:p identifier indicates the revision status of the product described in this book, for example, r1p2, where:

r  Identifies the major revision of the product, for example, r1.
p  Identifies the minor revision or modification status of the product, for example, p2.

Intended audience

This book is written for experienced hardware and software developers to enable them to perform FPGA development using the MPS3 motherboard.

Using this book

This book is organized into the following chapters:

Chapter 1 Introduction
This chapter introduces the MPS3 motherboard.

Chapter 2 Hardware description
This chapter describes the MPS3 motherboard hardware.

Chapter 3 Configuration
This chapter describes the powerup and configuration processes of the MPS3 motherboard.

Appendix A Signal descriptions
This appendix lists the signals at the interface connectors of the MPS3 motherboard.

Appendix B Specifications
This appendix contains electrical specifications of the MPS3 motherboard.

Appendix C Revisions
This appendix describes the technical changes between released issues of this book.

Glossary

The Arm® Glossary is a list of terms used in Arm documentation, together with definitions for those terms. The Arm Glossary does not contain terms that are industry standard unless the Arm meaning differs from the generally accepted meaning.

See the Arm® Glossary for more information.

Typographic conventions

*italic*  Introduces special terminology, denotes cross-references, and citations.

*bold*  Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

*monospace*  Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

*monospace*  Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
Denotes arguments to monospace text where the argument is to be replaced by a specific value.

Monospace bold
Denotes language keywords when used outside example code.

<and>
Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example:

```
MRC p15, 0, <Rd>, <CRn>, <CRm>, <Opcode_2>
```

Small capitals
Used in body text for a few terms that have specific technical meanings, that are defined in the Arm® Glossary. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams
The following figure explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are undefined, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.

![Timing diagram conventions](image)

**Figure 1** Key to timing diagram conventions

Signals
The signal conventions are:

Signal level
The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:

- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lowercase n
At the start or end of a signal name denotes an active-LOW signal.

Additional reading
This book contains information that is specific to this product. See the following documents for other relevant information.
Arm publications

- Application Note AN522 Example IoT Kit Subsystem design for MPS3 (DAI 0522).
- Arm® CoreLink™ SSE-200 Subsystem Technical Overview (Arm DTO 0051).
- Arm® CoreLink™ SSE-100 Subsystem Technical Reference Manual (Arm DDI 0551).
- Arm® DS-5 Setting up the Arm DSTREAM Hardware (Arm DUI 0481).
- Arm® DS-5 Using the Debug Hardware Configuration Utilities (Arm DUI 0498).

Other publications

- See the Xilinx website https://www.xilinx.com for information about the Xilinx Kintex Ultrascale XCKU115-1FLVB1760C FPGA.
Feedback

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:
• The product name.
• The product revision or version.
• An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

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• If applicable, the page number(s) to which your comments refer.
• A concise explanation of your comments.

Arm also welcomes general suggestions for additions and improvements.

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Chapter 1
Introduction

This chapter introduces the MPS3 motherboard.

It contains the following sections:
- 1.1 Precautions on page 1-12.
- 1.2 About the MPS3 motherboard on page 1-13.
- 1.3 Location of components on the MPS3 motherboard on page 1-15.
1.1 Precautions

You can take certain precautions to ensure safety and to prevent damage to your MPS3 motherboard.

This section contains the following subsections:

- 1.1.1 Ensuring safety on page 1-12.
- 1.1.2 Operating temperature on page 1-12.
- 1.1.3 Preventing damage on page 1-12.

1.1.1 Ensuring safety

An on-board connector supplies 12V DC to the MPS3 motherboard.

--- Warning ---

Do not use the MPS3 motherboard near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.

1.1.2 Operating temperature

The MPS3 motherboard has been tested in the temperature range 0°C to 40°C.

1.1.3 Preventing damage

The MPS3 motherboard is intended for use within a laboratory or engineering development environment.

--- Caution ---

To avoid damage to the MPS3 motherboard, observe the following precautions:

- Connect the external power supply to the board before starting the powerup process.
- Never subject the board to high electrostatic potentials. Observe ElectroStatic Discharge (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not fit an Arduino Shield, or a Pmod expansion shield, while the MPS3 motherboard is powered.
1.2 **About the MPS3 motherboard**

The MPS3 motherboard is an FPGA *Internet of Things* (IoT) development platform. The board is designed to support Arm Cortex-M class and small to medium Arm Cortex-A and Cortex-R class processors, or dedicated custom designs.

**Major features of the MPS3 motherboard**

The MPS3 motherboard contains a Xilinx Kintex Ultrascale XCKU115-1FLVB1760C FPGA, support logic, and peripheral interfaces that provide access to the FPGA and I/O interfaces.

The feature-rich set of user peripherals connects directly to the FPGA and provides flexibility for the user. The peripherals can be included in a custom design as required.

Two Arduino expansion Shield slots enable connection of sensors, motors, and other design-specific peripherals. The MPS3 motherboard also provides expansion through four Peripheral Module (Pmod) expansion ports, and an **FPGA Mezzanine Card High Pin Count** (FMC-HPC) expansion port.

An on-board *Motherboard Configuration Controller* (MCC) controls the motherboard and configures the FPGA in a way similar to other boards in the Arm Versatile™ Express range.

**Uses of the MPS3 motherboard**

The MPS3 motherboard enables FPGA prototyping of complex designs:

- **Software development:**
  - Linux development on Cortex-A or Cortex-R class processors.
  - Bare metal development.

- **Tool development.**

**Major components and systems of the MPS3 motherboard**

The MPS3 motherboard provides:

- **One Kintex XCKU115 FPGA.**

- **Board interfaces:**
  - Ethernet 10/100.
  - AC97 audio.
  - HDMI video up to 1080p.
  - Dual USB-A port.

- **Expansion connectivity:**
  - Two Arduino Shield interfaces for custom peripherals.
  - FMC-HPC expansion for up to 160 I/O, 10 multi-*GigaBit Transceivers* (GBT), and clocks.
  - Four Pmod interfaces.

- **Quarter Video Graphics Array** (QVGA) CLCD with touchscreen.

- **Memory:**
  - 4GB DDR4 with capacity for up to 8GB.
  - 8MB user *Quad Serial Peripheral Interface* (QSPI) flash for boot.
  - Up to 8MB of FPGA *Block RAM* (BRAM).
  - 16GB eMMC.
  - microSD card interface.

- **Clocks:**
  - *Real-Time Clock* (RTC).
  - Five programmable clocks.
  - One fixed 24MHz clock.

- **User board components:**
  - Ten user LEDs.
  - Eight user switches.
  - Two user push buttons.
• Reset push buttons and power indicator LEDs.
• Debug support:
  — P-JTAG processor debug.
  — F-JTAG (FPGA) debug.
  — *Serial Wire Debug* (SWD).
  — 16-bit trace.
  — 4-bit trace.
  — On-board CMSIS-DAP.
  — Four serial ports over USB.
1.3 Location of components on the MPS3 motherboard

The following figure shows the physical layout of the MPS3 motherboard.

See 2.12 On-board user components on page 2-39 for a description of the use of the Shield and Pmod power and I/O reference voltage user links.

--- Note ---

The configuration switches are reserved. For correct operation, you must ensure that both switches are in the OFF position, that is, pointing away from the board.
Chapter 2
Hardware description

This chapter describes the MPS3 motherboard hardware.

It contains the following sections:

- 2.1 Overview of the board hardware on page 2-17.
- 2.2 Example Cortex®-M33 IoT Kit subsystem design on page 2-21.
- 2.3 Clocks on page 2-23.
- 2.4 Reset, powerup, and configuration on page 2-25.
- 2.5 Power on page 2-27.
- 2.6 Serial Configuration Controller interface on page 2-28.
- 2.7 MCC-SMC interface on page 2-30.
- 2.8 USB 2.0 and Ethernet static memory interface on page 2-35.
- 2.9 Video HDLCD interface on page 2-36.
- 2.10 Audio codec interface on page 2-37.
- 2.11 QVGA video CLCD display on page 2-38.
- 2.12 On-board user components on page 2-39.
- 2.13 Interrupts on page 2-40.
- 2.14 FPGA DDR4 memory interface on page 2-41.
- 2.15 User non-volatile memory on page 2-42.
- 2.16 Arduino Shield and Pmod interfaces on page 2-43.
- 2.17 FMC-HPC interface on page 2-46.
- 2.18 System debug on page 2-49.
- 2.19 Design settings for correct board operation with a minimal design on page 2-52.
2.1 Overview of the board hardware

The MPS3 motherboard provides access to the Kintex XCKU115 FPGA and peripherals to enable FPGA prototyping and software development.

The following figure shows the hardware infrastructure of the MPS3 motherboard.
The MPS3 motherboard contains the following components:

- One Xilinx Kintex Ultrascale XCKU115-1FLVB1760C FPGA:
— 1451k logic cells.
— Four UARTs (connected to a USB to serial hub for connection to the host computer).
— Support for encrypted FPGA images and Partial Reconfiguration.

• User memory system:
  — Up to 8MB internal BRAM.
  — microSD card interface.
  — 8MB external QSPI flash.
  — 4GB, 64-bit external DDR4 SODIMM.
  — 16GB, 8-bit external eMMC.

• Motherboard Configuration Controller (MCC) that controls the MPS3 motherboard, and supports board configuration at powerup or reset:
  — FPGA configuration.
  — Board configuration.
  — Supervises user update of the board configuration files in the configuration microSD card.
  — Two hardware reset buttons, both labeled PBRST, and two On/Off soft reset buttons, both labeled PBON.

• Ethernet 10/100 port and Ethernet controller that connects to the Static Memory Controller (SMC) interface in the FPGA.

• HDMI port and HDMI controller:
  — Inputs 24-bit RGB data from the HDLCD controller in the FPGA.
  — Configured over I²C directly from FPGA.
  — Supports an I²S audio connection to the FPGA.
  — Drives the HDMI connector.

• Audio codec:
  — Provides stereo Line In, stereo Line Out, and stereo Microphone Input In to the stacked stereo jack audio interface.
  — Configured over I²C from the I²C controller in the FPGA.
  — I²S audio connection to the I²S in the FPGA.

• Shield expansion:
  — Two Arduino expansion interfaces for Shields for custom peripherals or off-the-shelf sensor interfaces such as WiFi, Bluetooth, Proximity detectors, or Gyro sensors.
  — Each interface connects: 16 × digital 3V3 I/O or 16 × digital 5V I/O, voltage references, and six analog inputs from each Shield.

• Peripheral Module (Pmod) interface expansion:
  — Four Pmod expansion connectors that use the same I/O on an interface shared with the Shield connectors, Type 2A/3/4 support.
  — Requires Pmod adapters that provide 8 × analog 3V3 I/O, or 8 × analog 5V I/O.

• FMC-HPC expansion:
  — Connector to enable fitting of an FPGA Mezzanine Card (FMC) High Pin Count (HPC) expansion card to the MPS3 motherboard.
  — A 14-pin FMC configuration connector and configuration EEPROM to enable configuration of Arm FMC boards.

• User switches, LEDs, and push buttons that connect directly to GPIO in the FPGA:
  — One 8-way user DIP switch.
  — Ten user LEDs.
  — Two user push buttons.

• System LEDs:
  — Green 12V OK LED.
  — Orange 3V3 OK LED.
  — Green PWR ON LED.
  — Green FPGA configuration LED.
  — Green MCC active LED.
  — Orange Debug USB active LED.
— Green LED. Ethernet speed indicator-incorporated into combined Ethernet and dual-USB connector.
— Yellow LED. Ethernet link and activity indicator-incorporated into combined Ethernet and dual-USB connector.

Related references
1.3 Location of components on the MPS3 motherboard on page 1-15.
2.2 Example Cortex®-M33 IoT Kit subsystem design

The MPS3 motherboard is an FPGA motherboard Internet of Things (IoT) development platform. The board is designed to support Arm Cortex-M class and small to medium Arm Cortex-A and Cortex-R class processors, or dedicated customs designs.

The following figure shows an example Cortex-M33 IoT Kit subsystem design for the MPS3 motherboard. You can implement this example design in MPS3. See Application Note AN522 Example IoT Kit Subsystem design for MPS3.
Figure 2-2  Example IoT Kit subsystem design for MPS3
2.3 Clocks

The MPS3 motherboard provides fixed and programmable clocks to drive the FPGA and motherboard interfaces.

The following figure shows a functional overview of the clock systems of the MPS3 motherboard. In this figure, the image implements OSCLK4 as the audio clock and OSCLK5 as the HDLCD clock.

![Figure 2-3  Overview of MPS3 motherboard clocks](image)

The Motherboard Configuration Controller (MCC) configures the programmable OSCCLKs at powerup using the default values, which are defined in the MPS3 motherboard configuration application note .txt
file in the configuration microSD card. The system register interface can implement runtime control of the OSCCLKs.

PLLS within the FPGA can use the reference 24MHz to generate other fixed internal frequencies.

The following table lists the MPS3 motherboard clocks and their characteristics.

<table>
<thead>
<tr>
<th>Clock name: Source</th>
<th>Programmable frequency range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>OSCLK0</td>
<td>24MHz, fixed</td>
<td>-</td>
</tr>
<tr>
<td>OSCLK1</td>
<td>2-230MHz</td>
<td>-</td>
</tr>
<tr>
<td>OSCLK2</td>
<td>2-230MHz</td>
<td>-</td>
</tr>
<tr>
<td>OSCLK3</td>
<td>2-230MHz</td>
<td>-</td>
</tr>
<tr>
<td>OSCLK3A</td>
<td>12MHz, fixed</td>
<td>USB 2.0 controller.</td>
</tr>
<tr>
<td>OSCLK4</td>
<td>2-230MHz</td>
<td>The preferred use for this clock is as the clock for the audio codec and FPGA audio interface. In this case, this clock is the source clock for: • AACI_MCLK. • AACI_SCLK. • AACI_LRCLK.</td>
</tr>
<tr>
<td>OSCLK0A</td>
<td>25MHz, fixed</td>
<td>Ethernet controller.</td>
</tr>
<tr>
<td>OSCLK5</td>
<td>2-230MHz</td>
<td>The preferred use for this clock is for the HDMI controller and HDLCD interface in FPGA.</td>
</tr>
<tr>
<td>OSCLK6</td>
<td>100MHz, fixed</td>
<td>DDR.</td>
</tr>
<tr>
<td>OSC8MHz</td>
<td>8MHz, fixed</td>
<td>MCC main input clock.</td>
</tr>
<tr>
<td>OSC32K</td>
<td>32.768kHz, fixed</td>
<td>Input for <em>Real Time Clock</em> (RTC) in MCC.</td>
</tr>
<tr>
<td>TCK: JTAG</td>
<td>-</td>
<td>Source clock for JTAG debug system. Frequency depends on the debugger setting.</td>
</tr>
<tr>
<td>CFGCLK: MCC</td>
<td>25MHz (fixed)</td>
<td>Configuration clock for FPGA.</td>
</tr>
</tbody>
</table>

**Related references**

*1.3 Location of components on the MPS3 motherboard* on page 1-15.
2.4 Reset, powerup, and configuration

The MPS3 motherboard provides five external resets to the FPGA.

**Overview of reset system**

The MPS3 motherboard provides a hardware reset, and a software reset.

There are two hardware reset buttons. They perform the same function and both are labeled *PBRST*. Pressing one of them puts the system into the standby state.

There are two On/Off soft reset buttons. Both are labeled *PBON*. Pressing one of them performs a software reset, or if the board is already in the standby state, powers up the system.

The following figure shows the MPS3 motherboard reset system, where the FPGA contains a user image.

![MPS3 motherboard reset system diagram](image_url)

**FPGA resets**

**FPGA_nRST**

Board and FPGA reset including FPGA PLLs.

**CB_nPOR**

The main powerup reset for the FPGA image logic. If a System Control Processor (SCP) is present in the design, releasing this reset might also trigger the powerup reset sequencing.

**nTRST**

Resets the CoreSight DAP.

**CB_nRST, nSRST**

*CB_nRST* is the core reset. These inputs are ANDed together in the FPGA. They initiate operation of the processors and enable the debug tools to debug the processors before they leave reset.

**CB_CFGnRST**

The reset signal for the serial interface of the Serial Configuration Controller (SCC).
CPUWAIT

Core register used to release processor core or cores from reset.

Reset sequence

The following figure shows the MPS3 motherboard reset and powerup timing cycle including board configuration.

Figure 2-5  MPS3 motherboard reset and configuration timing

Related references

1.3 Location of components on the MPS3 motherboard on page 1-15.
2.5 Power

You supply power to the motherboard from the mains supply using the on-board power jack and the connector cable that Arm supplies with the board.

Arm supplies an external power supply unit that converts mains power to 12V 5A DC and connects to the 12V jack on the board. The unit accepts mains power in the range 110V AC to 240V AC.

________ Caution ________
If you supply your own external mains adapter, it must be a Low-Power Source (LPS). Some adapters are marked LPS on their rating label. Otherwise it might be necessary to consult you adapter supplier to ensure that it meets this criterion.

Alternatively, you can connect an external 12V DC supply, +/- 10%, directly to the 12V connector.

________ Caution ________
Any external 12V DC +/- 10% power supply that is used must be a limited power source, maximum 5amps.

__________
On-board regulators supply power to the motherboard power domains and to the FPGA power domains.

__________ Note _________
The following on-board LEDs illuminate when power is applied:
• 12V OK. External 12V DC connected.
• SB_3V3 OK. On-board 3V3 supply asserted.
• PWR ON. On-board 5V supply asserted.

Related references
A.9 12V power connector on page Appx-A-82.
1.3 Location of components on the MPS3 motherboard on page 1-15.
2.6 Serial Configuration Controller interface

The design can include a Serial Configuration Controller (SCC) interface, using a block of registers in the FPGA.

After FPGA configuration, the Motherboard Configuration Controller (MCC) sets default values in the SCC registers, using values from the board configuration file in the configuration microSD card. The Motherboard Configuration Controller (MCC) configures the SCC through the serial interface on the MCC.

The following figure shows the SCC interface.

![Serial Configuration Controller interface diagram](image)

**Figure 2-6 Serial Configuration Controller interface**

--- **Note** ---

If the design does not implement the SCC, you must set the variable FPGA_SCC to FALSE in the board config.txt file. See 3.4.2 config.txt generic motherboard configuration file on page 3-62.

The following figures show the read and write cycle timing of the SCC interface.
2.6 Serial Configuration Controller interface

Figure 2-7 Serial Configuration Controller interface read cycle timing

Figure 2-8 Serial Configuration Controller interface write cycle timing
2.7 MCC-SMC interface

The SMC interface in the MCC supports read and write transactions that enable communication with the internal system bus of the FPGA. The FPGA design must convert these transactions to the type of transactions that are used in the FPGA design, usually AHB-type transactions.

Overview of MCC-SMC interface

The following figure shows the FPGA-MCC SMC interface.

![MCC-SMC interface diagram]

--- Note ---

SMBM\_nBL[1:0] is not used.

The MCC-SMC interface enables the MCC to access the peripheral space of the FPGA system. Typical uses are:

- Preloading boot images.
- Reading and writing to system registers.
- Preconfiguring peripherals.

Implementing the MCC-SMC interface

Chip-Select

SMBM\_nE[4:1] functions as a Chip-Select, providing four active-low Chip-Selects:

- 0xF: No Chip Select.
- 0xE: Chip-Select 0.
- 0xD: Chip-Select 1.
- 0xB: Chip-Select 2.
- 0x7: Chip-Select 3.
Address and data transfer out of the MCC-SMC interface
The MCC provides 25 of the 32 bits that the FPGA design uses for AHB-type transactions. The FPGA design generates the other 7 bits.

During the address phase, the 25 address bits are shared between SMBM_D[15:0] and SMBM_A[24:16].
- SMBM_D[15:0] carries the 16 least significant address bits of the interface.
- SMBM_A[24:16] carries the 9 most significant address bits of the interface.

--- Note ---
SMBM_A[25] is not used.

---
During the data transfer phase, SMBM_D[15:0] carries the four data bytes in two stages. It carries the two least significant bytes, and then the two most significant data bytes.

The following figure shows an MCC-SMC interface address and data transfer.

---

--- Note ---
- The MCC-SMC interface supports only 32-bit data read and write transfers.
- To meet the timing requirements for address and data transfer, Arm recommends that you use the MCC-SMC interface decoder in the file microToAhb.v, provided by Arm.
Forming the 32-bit address in the FPGA

The FPGA design must form the 32-bit address, for AHB-type transfers inside the FPGA, from the following:

- The least significant bit (LSB), generated by the FPGA design.

  **Note**

  The MCC-SMC interface supports only four-byte address mode transactions. To support four-byte address mode, the LSB generated by the FPGA design must be 0b0 and the LSB of the MCC-SMC interface is always 0b0.

- 25 address bits from the MCC.
- Six user bits, generated by the FPGA design.

The MCC can access 64MB of user memory for each Chip-Select, that is, a total memory space of 256MB. Each Chip-Select can point to non-contiguous areas in the user design but the total amount of user memory accessed by each Chip-Select cannot exceed 64MB.

The six address bits generated by the design, and if necessary, the Chip-Select bits, define which parts of the user memory space are accessed.

The following figure shows the formation of the AHB 32-bit address in the FPGA.
Example user memory map

The following figure shows an example user memory map.

![Example user memory map diagram]

**Figure 2-12 Example user memory map**

The example memory map shows the mapping when the six user bits have the following values for each Chip-Select:

- **CS0**: The image in the FPGA generates internal AHB address bits[31:26] = 0b000000 which gives a base address of 0x00000000.
- **CS1**: The image in the FPGA generates internal AHB address bits[31:26] = 0b000011 which gives a base address of 0x0C000000.
- **CS2**: The image in the FPGA generates internal AHB address bits[31:26] = 0b001100 which gives a base address of 0x30000000.
- **CS3**: The image in the FPGA generates internal AHB address bits[31:26] = 0b110000 which gives a base address of 0xC0000000.

The variable IMAGE0ADDRESS in the images.txt configuration file defines the base address in the MCC memory. In this example, setting IMAGE0ADDRESS to 0x05000000 selects a base address of 0x0D000000 in the FPGA user memory. The firmware sets SMBM_nE[4:1] to 0xD to select Chip-Select 1 which maps to the correct area of user memory.

See 3.4.3 Contents of the MB directory on page 3-62 for information on the images.txt file.
MCC-SMC interface not implemented

If the design does not implement the MCC-SMC interface, you must set the variable FPGA_SMB to FALSE in the board config.txt file. See 3.4.2 config.txt generic motherboard configuration file on page 3-62.
2.8 USB 2.0 and Ethernet static memory interface

The FPGA incorporates a simple Static Memory Controller (SMC) that interfaces to the USB 2.0 and Ethernet controllers on the MPS3 motherboard.

The following figure shows the USB 2.0 and Ethernet SMC interface.

![Diagram of USB 2.0 and Ethernet static memory interface]

**Figure 2-13 MPS3 motherboard USB 2.0 and Ethernet static memory interface**

Related references

- *1.3 Location of components on the MPS3 motherboard on page 1-15.*
2.9 **Video HDLCD interface**

The HDMI controller and HDMI connector on the MPS3 motherboard enable you to implement an HDLCD interface.

The external controller is a frame buffer device that can display up to $1920 \times 1080p$ resolution at 60fps.

--- **Note** ---
Support for higher resolutions up to 1080p depends on the timing performance of your FPGA image.

The HDMI controller also supports I²S audio from the FPGA.

The following figure shows a video HDLCD interface example design.

![MPS3 motherboard video HDLCD interface example design](image)

--- **Figure 2-14** MPS3 motherboard video HDLCD interface example design ---

**Related references**

*A.7 HDMI Type A female connector on page Appx-A-80.*

*1.3 Location of components on the MPS3 motherboard on page 1-15.*
### 2.10 Audio codec interface

An AACI audio codec on the MPS3 motherboard provides a stereo audio interface with Line In, Line Out, and Microphone In.

The AACI audio codec and the stereo audio interface enable you to implement an audio codec interface. The FPGA configures the codec over I²C and has an I²S audio interface. The I²S controller is a dedicated controller that consists of a data buffer and serializer.

The interface supports the standard audio data rate of 48kHz, up to a maximum of 96kHz. The codec contains audio power amplifiers that can drive up to 500mW, 8Ω stereo speakers.

The audio codec drives the stacked stereo jack on the MPS3 motherboard. When using an electret type of microphones, use jumpers J58 (L) and J59 (R) to enable microphone bias current.

The following figure shows a audio codec interface example design.

![Audio codec interface diagram](image)

**Figure 2-15  MPS3 motherboard audio codec interface example design**

**Related references**

- 1.3 Location of components on the MPS3 motherboard on page 1-15.
2.11 QVGA video CLCD display

The MPS3 motherboard provides QVGA, 320 × 240, CLCD video display.

The CLCD video display system provides an on-board CLCD display panel that includes:
- An 8-bit parallel bus between the FPGA and the display panel.
- A 4-wire resistive touch screen.
- A Touch Screen Controller (TSC) that connects to the FPGA over an I²C bus.

The interrupt signal from the touch screen controller, LCD_TSINT, and the backlight control signal, LCD_BLC, connect to the GPIO interface in the FPGA.

The interface supports a screen update rate of 20fps.

The following figure shows a functional overview of the CLCD display system.

![Figure 2-16 MPS3 motherboard CLCD display system](image-url)
2.12 On-board user components

The MPS3 motherboard provides ten user LEDs, eight user switches, and two user push buttons. The LEDs, switches, and push buttons connect directly to the FPGA, and this means they can be used for debug.

The following figure shows the user components on the MPS3 motherboard.

![Diagram of MPS3 motherboard user components]

**Figure 2-17 MPS3 motherboard user components**

Related references

1.3 Location of components on the MPS3 motherboard on page 1-15.
2.13 Interrupts

Interrupt signals from peripherals on the MPS3 motherboard connect to external pins on the FPGA. The image that you implement connects the peripheral interrupts to systems in the FPGA.

The following table shows the peripheral interrupt signals that connect to external pins on the FPGA.

<table>
<thead>
<tr>
<th>Interrupt</th>
<th>Interrupt source</th>
</tr>
</thead>
<tbody>
<tr>
<td>IOFPGA_SYSWDT</td>
<td>RTCC/SYS_CFG (OUT)</td>
</tr>
<tr>
<td>PB_IRQ</td>
<td>Push button</td>
</tr>
<tr>
<td>WDOG_RREQ</td>
<td>Watchdog reset (OUT)</td>
</tr>
<tr>
<td>DVI_INT</td>
<td>HDMI interrupt</td>
</tr>
<tr>
<td>USB_INT</td>
<td>USB 2.0</td>
</tr>
<tr>
<td>ETH_INT</td>
<td>Ethernet</td>
</tr>
<tr>
<td>CLCD_TINT</td>
<td>CLCD touchscreen</td>
</tr>
</tbody>
</table>
2.14 FPGA DDR4 memory interface

The MPS3 motherboard provides 4GB of DDR4 SODIMM and a DDR4 interface to the FPGA. The DDR4 controller and PHY interface uses the Xilinx Memory Interface Generator (MIG). The interface is 64-bit and uses 10 byte lanes.

The interface supports up to 900MHz, 1800MT/s, with the supplied SODIMM (MTA4ATF51264HZ-2GB31).

The following figure shows the FPGA DDR4 memory interface.
2.15 User non-volatile memory

The MPS3 motherboard provides on-board user non-volatile memory, 8MB QSPI flash (SST26VF064B), 16GB eMMC16G_M525, and a microSD card interface.

A typical use of the QSPI flash is as boot memory. The microSD card or eMMC memory can be used for storing the Linux file system.

The following figure shows a non-volatile memory system example design. For completeness, the figure includes the DDR4 volatile memory.

---

Note

The simplest boot method is to use block RAM in the FPGA which can be pre-loaded by the MCC before resets are released. The use of block RAM requires the FPGA design to implement the MCC-SMC interface. See 2.7 MCC-SMC interface on page 2-30.
2.16 Arduino Shield and Pmod interfaces

The MPS3 motherboard supports peripheral development by providing two Arduino Shield interfaces and, as an alternative, four Peripheral Module (Pmod) interfaces (Type 2A/3/4 support).

Overview of Shield and Pmod interfaces

The following figure shows the two Shield interfaces, and the four Pmod interfaces, of the MPS3 motherboard, where the FPGA design implements an SPI controller that drives the 12-bit ADC.

![Diagram of shield and pmod interfaces](image)

The Arduino Shield and Pmod interfaces share pins on the FPGA.
The Shield and Pmod interfaces share signals, including the digital I/O. Each Shield interface has 16 digital I/O, and the four Pmod interfaces each have 8 digital I/O. See the following sections for information on how the Shield and Pmod interfaces share the digital I/O signals:


The interfaces enable the use of off-the-shelf sensor interfaces, for example, WiFi, Bluetooth, proximity sensors, and gyro sensors, to suit custom design requirements. The interfaces also enable you to add full-custom sensor modules to the system.

**Shield interfaces**

Each Shield interface has 16 I/O and supports the choice of 3V3 or 5V I/O, independently selectable for each Shield using two user-links.

The outputs from the digital I/O user-links also act as the digital I/O voltage references for the Shields.

Other links, one for each Shield, select 5V or 12V for the power inputs, VIN0 and VIN1.

Note

The links also select I/O references and power inputs to the Pmod interfaces.

See Shield and Pmod power and I/O reference voltage user-links on page 2-44 for more information on the use of the user-links.

A 12-bit ADC supports six analog channels on each Shield.

**Pmod interfaces**

The Pmod interfaces are an alternative to the Shield interfaces. Each Pmod expansion header has 8 digital I/O and supports the choice of 3V3 or 5V digital I/O. You can select the digital I/O using two user-links on the board. One user-link selects 3V3 or 5V digital I/O operation for Pmod 0 and Pmod 1. The other user-link selects 3V3 or 5V operation for Pmod 2 and Pmod 3.

The outputs from the digital I/O user-links also act as the digital I/O voltage references for the Pmod expansion boards.

Two other links select 5V or 12V for the power inputs, VIN0 and VIN1.

Note

The links also select digital I/O references and power inputs to the Shield interfaces.

See Shield and Pmod power and I/O reference voltage user-links on page 2-44 for more information on the use of the user-links.

The locations of the Pmod connectors support the use of a dual-connector board, if required.

The Pmod interfaces do not support analog I/O.

**Shield and Pmod power and I/O reference voltage user-links**

The following figure shows the user-links that select I/O voltage level and power inputs to the Shield and Pmod interfaces. The figure shows the user-links that select 12V or 5V power, and 5V or 3V3 I/O references, for the Shields.
One user-link selects 3V3 or 5V I/O operations for the Shield 0, Pmod 0, and Pmod 1 interfaces.

One user-link selects 3V3 or 5V I/O operations for the Shield 1, Pmod 2, and Pmod 3 interfaces.

One user-link selects 5V or 12V power for the Shield 0 interface.

One user-link selects 5V or 12V power for the Shield 1 interface.

--- Caution ---

The maximum currents available at the power and reference pins are:

- **3V3/IOREF**: 1A maximum available for both Shields and all four Pmod interfaces.
- **5V/IOREF**: 1A maximum available for both Shields and all four Pmod interfaces.
- **12V**: 0.5A maximum available for both Shields.

---

See **1.3 Location of components on the MPS3 motherboard** on page 1-15 for the location of the user-links.

**Related references**

- **A.3 Peripheral Module (Pmod) connectors** on page Appx-A-75.
- **1.3 Location of components on the MPS3 motherboard** on page 1-15.
2.17 FMC-HPC interface

The MPS3 motherboard supports high speed, high pin count expansion using the FPGA Mezzanine Card (FMC) standard.

Overview of the FMC-HPC interface

The MPS3 motherboard uses the FMC-High Pin Count (FMC-HPC) variant and provides:

- One 400-way Samtec SEARAY connector.
- 160 I/O.
- 10 × high-speed differential transceivers, Multi-Gigabit Transceivers (MGTs).
- 2 × high-speed differential clocks, MGT clocks.
- Four differential clocks.
- Power.

The following figure shows the MPS3 motherboard FMC-HPC interface.

![Figure 2-22 MPS3 motherboard FMC-HPC interface](image)

**Note**

The FMC board configuration EEPROM is part of the FMC standard. The Arm daughterboard configuration EEPROM and Daughterboard Configuration Controller (DCC) are not part of the FMC standard but are supplied with Arm FMC daughterboards.

**FPGA-FMC pin connectivity**

See the following documents for the FPGA-FMC pin connectivity:

- FMC: `V2M_MPS3_fmc_pinout.xlsx`
- FPGA: `V2M_MPS3_fpga_pinout.xlsx`

**Example FMC board layout**

The following figure shows an MPS3 motherboard with an FMC board that is fitted to the FMC-HPC expansion connector.
Figure 2-23  FMC-HPC board fitted to the MPS3 motherboard FMC-HPC expansion connector

The figure shows a single-width FMC board, 69mm × 76.5mm, fitted. The maximum component height in the shaded area in the figures is 6mm to enable fitting of wider FMC boards.

Configuration of Arm FMC expansion boards

The MPS3 motherboard provides a custom 14-pin connector to enable configuration of Arm FMC boards using I²C, SPI, and reset signals. The configuration process is similar to the configuration process used on other Versatile Express boards that use the signals on the HDRY headers.

Arm FMC expansion boards provide a daughterboard EEPROM and a Daughterboard Configuration Controller (DCC). The DCC and the MCC on the MPS3 motherboard configure the Arm FMC expansion board using the configuration information in the daughterboard EEPROM.
Examples of available third-party FMC expansion boards

The following are examples of FMC third-party expansion boards that are available to support various interfaces:

ADC board
AD9467-FMC.

Loopback board
WHZ-FMC XM-107.

Related references
A.5 FMC configuration connector on page Appx-A-78.
1.3 Location of components on the MPS3 motherboard on page 1-15.
2.18 System debug

The MPS3 motherboard provides several methods of performing debug.

**CoreSight™ debug**
The following figure shows the MPS3 motherboard debug and trace system.

![Figure 2-24 MPS3 motherboard CoreSight debug and trace](image)

- **P-JTAG processor debug on:**
  - 20-pin IDC connector.
  - 10-pin IDC connector.
  - 20-pin Cortex debug and ETM connector.
  - 38-pin MICTOR connector.
- **Serial Wire Debug (SWD) on:**
  - 20-pin IDC connector.
  - 10-pin IDC connector.
  - 20-pin Cortex debug and ETM connector.
  - 38-pin MICTOR connector.
  - CMSIS-DAP debug over USB on a USB 2.0 type B connector.
- 16-bit trace on a 38-pin MICTOR connector.
- 4-bit trace on a 20-pin Cortex debug and ETM connector.
- FPGA debug on 14-pin ILA connector for FPGA debug.
The availability of P-JTAG, SWD, 16-bit trace, and 4-bit trace depends on the design that you implement in the FPGA.

**Debug over USB**

Debug over USB supports:

- Four UARTs.
- MCC debug.
- CMSIS-DAP.

The following figure shows the architecture of the debug over USB system.

---

**Serial ports**

The four user serial ports on the Kintex XCKU115 FPGA indicate the status of the system during boot time. After the system has booted, they are used for debug or status information. The four serial ports are concentrated into a USB-serial interface that connects to a four port hub, that is connected to the USB connector. The hub enables the four FPGA serial ports, the MCC USBDBG port, and the CMSIS-DAP controller to share the USB debug connector.

**CMSIS-DAP debug**

The CMSIS-DAP interface in the FPGA enables debug over USB to the FPGA CoreSight components using the dedicated Arm CMSIS-DAP controller.

**Setting up host software for the hub and serial ports**

The MPS3 motherboard does not require software drivers for Windows 7 or later versions of Windows.

The following figure shows the USB devices that the MPS3 motherboard adds when you connect a workstation into the USB debug connector.
Related references

A.1.4 38-pin MICTOR connector on page Appx-A-68.
A.1.6 Debug USB 2.0 connector on page Appx-A-70.
1.3 Location of components on the MPS3 motherboard on page 1-15.
2.19 Design settings for correct board operation with a minimal design

For correct operation with a minimal design, the MPS3 motherboard requires a minimum amount of RTL in the FPGA, and certain variable settings in the `config.txt` file.

**Minimum RTL**

The following table shows the signals that you must tie off in the FPGA to generate the minimum RTL for correct operation of the MPS3 motherboard.

<table>
<thead>
<tr>
<th>FPGA signal</th>
<th>Minimum RTL</th>
</tr>
</thead>
<tbody>
<tr>
<td>MMB_IDCLK</td>
<td>Tie LOW</td>
</tr>
<tr>
<td>EMMC_CLK</td>
<td>Tie LOW</td>
</tr>
<tr>
<td>QSPI_nCS</td>
<td>Tie HIGH</td>
</tr>
<tr>
<td>QSPI_SCLK</td>
<td>Tie LOW</td>
</tr>
<tr>
<td>IOFPGA_SYSWDT</td>
<td>Tie LOW</td>
</tr>
<tr>
<td>WDOG_RREQ</td>
<td>Tie LOW</td>
</tr>
<tr>
<td>SMBM_nWAIT</td>
<td>Tie HIGH</td>
</tr>
<tr>
<td>CFG_DATAOUT</td>
<td>Tie LOW</td>
</tr>
</tbody>
</table>

**Configuration file settings**

If the design does not implement the *Serial Configuration Controller* (SCC), you must set the variable FPGA_SCC to FALSE in the board `config.txt` file.

If the design does not implement the MCC-SMC interface, you must set the variable FPGA_SMB to FALSE in the board `config.txt` file.

See 3.4.2 `config.txt generic motherboard configuration file` on page 3-62.
Chapter 3
Configuration

This chapter describes the powerup and configuration processes of the MPS3 motherboard.

It contains the following sections:

• 3.1 Overview of the configuration system on page 3-54.
• 3.2 Powerup and configuration sequence on page 3-56.
• 3.3 Reset push buttons on page 3-59.
• 3.4 Configuration files on page 3-61.
3.1 Overview of the configuration system

The Motherboard Configuration Controller (MCC) controls the configuration process of the MPS3 motherboard during powerup or reset. After application of power, and a press of one of the On/Off soft reset buttons, PBON, the configuration process begins and completes without further user intervention.

Overview of configuration system

The following figure shows the motherboard configuration system.

![MPS3 motherboard configuration system diagram](image)

The microSD card stores the board configuration files, including the `board.txt` and `config.txt` files. You can access the configuration microSD card as a Universal Serial Bus Mass Storage Device (USBMSD).

The MCC:
- Reads the FPGA image from the configuration microSD card and loads it into the FPGA.
- Sets the board oscillator frequencies using values from the MPS3 motherboard configuration application note .txt file.
- If enabled, configures the FPGA Serial Configuration Control (SCC) registers using values from the `board.txt` file.
- If enabled, loads the boot memory, QSPI, DDR4, or BRAM, with the boot image that the `images.txt` file defines.

At the start of the configuration process, the MCC reads the contents of the configuration EEPROM. The EEPROM contains the following information:
- Board HBI number.
- Board revision.
- Board variant.
- Number of FPGAs.
- The names of the current images in 8.3 format and the file creation dates.
The HBI number is a unique code that identifies the board. The root directories in the EEPROM and the microSD card contain subdirectories in the form HBIBoardNumberBoardrevision, for example HBI0309.

There are two stages in programming and configuring the images in the FPGA:

1. The MCC reads the configuration files in the microSD card to determine which image to load.

   **Note**
   
   The debug USB port supports MSD class enabling Drag-and-Drop for transferring new images to the configuration microSD card. The microSD card appears in the file system as a device with removable storage.

2. The MCC loads the FPGA image into the FPGA.

**Configuration port connected to an external workstation**

If you connect an external workstation to the MCC debug port, you can access the configuration microSD card. You can then edit and copy configuration and software images to the SD card.

**Related references**

- 3.4.1 Overview of configuration files and microSD card directory structure on page 3-61.
- 3.4.2 config.txt generic motherboard configuration file on page 3-62.
- 3.4.3 Contents of the MB directory on page 3-62.
- 3.4.4 Contents of the SOFTWARE directory on page 3-64.
3.2 Powerup and configuration sequence

The power push buttons and configuration files control the sequence of events of the motherboard powerup and configuration process.

The following figure shows the powerup and configuration sequence.
3 Configuration

3.2 Powerup and configuration sequence

Figure 3-2 MPS3 motherboard powerup and configuration sequence
The powerup and configuration sequence is:

1. The board applies power to the system.
2. The MCC powers the EEPROM and reads it to determine the HBI identification code for the board.
3. The system enters standby mode.
4. The system enables the microSD memory card. You can connect a workstation to the debug USB port to edit existing configuration files or Drag-and-Drop new configuration files.

--- Caution ---

File names and directory names are in 8.3 format:

- File names that you generate must be in lowercase.
- Directory names must be in uppercase.
- All configuration files must use DOS line endings (0x0D/0x0A).

5. The system stays in standby state until you press the On/Off soft reset button, PBO\text{N}.

6. The system loads the board configuration file:
   - The MCC reads the generic config.txt file.
   - The MCC searches the microSD card MB directory for the HBI0309x subdirectory that matches the HBI code in the board EEPROM.

7. The next steps depend on the configuration files:
   - If the MCC finds configuration subdirectories that match the HBI code of the motherboard, configuration continues and the MCC reads the board.txt file.
   - If the MCC does not find the correct configuration files, it records the failure in a log file on the microSD card. Configuration stops and the system re-enters the standby state.

8. The MCC measures the board power supplies.
9. The MCC configures the board clocks and FPGA SCC registers.
10. If the MCC finds new software images, it loads them into the QSPI flash, BRAM, or DDR4 memory through the FPGA.
11. The MCC releases the system resets, CB\text{_nPOR}, CB\text{_nRST}, and CB\text{_RUN}. The system enters the RUN state.
12. Normal operation continues until a new event occurs.

Related references

3.4.1 Overview of configuration files and microSD card directory structure on page 3-61.
3.4.2 config.txt generic motherboard configuration file on page 3-62.
3.4.3 Contents of the MB directory on page 3-62.
3.4.4 Contents of the SOFTWARE directory on page 3-64.
3.3 Reset push buttons

The MPS3 motherboard provides push buttons that initiate reset and configuration. You can initiate a software reset, or a hardware reset, of the system.

Software reset push buttons

The MPS3 motherboard provides two On/Off soft reset buttons, both labeled PBON. Pressing either one initiates a software reset of the system because the two buttons perform the same function:

White On/Off soft reset button
Located near to the configuration microSD card.

Red On/Off soft reset button
Located near the debug USB 2.0 port.

See 1.3 Location of components on the MPS3 motherboard on page 1-15 for the location of the On/Off soft reset push buttons on the MPS3 motherboard.

Initiate a software reset by briefly pressing the button during runtime. The MCC performs a software reset of the FPGA and resets the devices on the board.

The software reset sequence is as follows:
1. Briefly press one of the two PBON buttons.

   ________ Caution _________
   Pressing and holding one of the software reset buttons for more than two seconds performs a hardware reset and the system enters the standby state. Pressing one of the software reset buttons for more than two seconds is similar to pressing the hardware reset button PBRST.

   ________________________________

2. The MCC asserts the CB_nRST signal. The MCC might also assert CB_nPOR depending on the variable ASSERTNPOR in the configuration file config.txt.
3. The MCC releases CB_nPOR if it is active depending on the setting of the variable ASSERTNPOR in the configuration file config.txt.
4. The MCC releases CB_nRST.
5. The motherboard enters the run state.

   ________ Note _________
   The MCC does not perform the following actions as a result of a software reset:
   • Read the configuration files.
   • Perform a board reconfiguration.
   • Perform a full reconfiguration of the FPGA.

Hardware reset buttons

The MPS3 motherboard provides two hardware reset buttons, both labeled PBRST. Pressing either one initiates a hardware reset of the system because the two buttons perform the same function.

White hardware reset button
Located near to the configuration microSD card.

Red hardware reset button
Located near the debug USB 2.0 port.

See 1.3 Location of components on the MPS3 motherboard on page 1-15 for the location of the hardware reset push buttons on the MPS3 motherboard.

You can change the operation of the board from ON to standby by briefly pressing one of the hardware reset buttons. Briefly pressing the button switches off the power to the board and resets the system to the default values.
If you then press one of the software reset buttons, the system performs a full configuration and enters the run state.

**Related references**

1.3 *Location of components on the MPS3 motherboard* on page 1-15.
3.4 Configuration files

This section describes the MPS3 motherboard configuration files on the configuration microSD card that control the board powerup and configuration process.

This section contains the following subsections:
- 3.4.1 Overview of configuration files and microSD card directory structure on page 3-61.
- 3.4.2 config.txt generic motherboard configuration file on page 3-62.
- 3.4.3 Contents of the MB directory on page 3-62.
- 3.4.4 Contents of the SOFTWARE directory on page 3-64.

3.4.1 Overview of configuration files and microSD card directory structure

The configuration microSD card on the MPS3 motherboard contains configuration files that control the board powerup and configuration process.

Because the motherboard microSD card is non-volatile memory, it is only necessary to load new configuration files if you change the system configuration. The microSD card that is supplied with the MPS3 motherboard contains default configuration files.

If you connect a workstation to the debug USB port, the microSD card appears as a USB Mass Storage Device (USBMSD). You can then add, edit, or delete files.

You can use a standard text editor that produces DOS line endings to read and edit the board configuration files.

The following figure shows a typical example of the directory structure on the microSD card memory.

```plaintext
V2MMPS3(F:)
  -- config.txt
  -- LOG.TXT
  -- MB/
    -- HBI0309B/
    -- mbb_v????.ebf
    -- board.txt
    -- AN???
      -- an???.v?.bit
      -- an???.v?.txt
    -- images.txt
  -- SOFTWARE/
    -- dm_v????.axf
    -- st_v????.axf
```

Figure 3-3 Example USBMSD directory structure

—— Caution ——

File names and directory names are in 8.3 format:
- File names that you generate must be in lowercase.
- Directory names must be in uppercase.
- All configuration files must use DOS line endings (0x0D/0x0A).

The directory structure and file name format ensure that each image is matched to the correct target device defined in the board configuration EEPROM:

config.txt file  Generic configuration file for all motherboards. This file applies to all Versatile Express motherboards including the MPS3 motherboard. Some settings are specific to the MPS3 motherboard.
MB directory
Contains subdirectories for any motherboard variants that might be present in the system. The subdirectory names match the HBI codes for the specific motherboard variants. The files in this directory contain clock, register, and other settings for the motherboard.

SOFTWARE directory
Can contain user application files that the MCC can load into the QSPI, BRAM, or DDR4 on the board. The memory that is loaded depends on the image that you implement in the FPGA. The images.txt file defines the file that the MCC loads.

Related references
3.1 Overview of the configuration system on page 3-54.
3.2 Powerup and configuration sequence on page 3-56.

3.4.2 config.txt generic motherboard configuration file
You can connect a workstation to the USB debug port to update the generic Versatile Express configuration file, config.txt, on the configuration microSD card.
The following example shows a configuration file that you can load into the configuration microSD card.

Note
• Colons (:) indicate the end of commands and must be separated by a space character (0x20) from the value fields.
• Semicolons (;) indicate comments.

TITLE: Versatile Express V2M- MPS3 configuration file
[CONFIGURATION]
AUTORUN: FALSE ;Auto Run from power on
AUTORUNDELAY: 3 ;Delay in seconds to wait for key press to stop bootup
RTC: FALSE ;TRUE = Enable RTC, FALSE = Disable RTC
UARTMODE: 2 ;0-MCC:FPGA0, 1-MCC:FPGA1, 2-MCC/FPGA0:FPGA1
REMAP: BRAM ;Boot device BRAM/DDR/QSPI
FPGA_SMB: TRUE ;FPGA image supports the MCC SMB interface
FPGA_SCC: TRUE ;FPGA image supports the MCC SCC interface
FMC_FORCE: FALSE ;Force FMC power ON
FMC_EEMODE: 0 ;FMC EEPROM mode, 0-default/1-two byte address
DVIMODE: VGA ;VGA/SVGA/XGA/SXGA/UXGA or HD1080 (MCC sets OSCLK5)
USERSWITCH: 00000000 ;Userswitch[7:0] in binary
CONFSWITCH: 00000000 ;Configuration Switch[7:0] in binary
ASSERTNPOR: TRUE ;External resets assert nPOR
CPU0WAIT: 0x00000000 ;CPU0WAIT value set to 0xFFFFFFFF when using CB_nRST
WDTRESET: NONE ;Watchdog reset options NONE/RESETMB/RESETDB
USB_REMOTE: FALSE ;Selects remote command via USB
MACADDRESS: 0xFFFFFFFFFFFF ;MAC Address

Related references
3.1 Overview of the configuration system on page 3-54.
3.2 Powerup and configuration sequence on page 3-56.

3.4.3 Contents of the MB directory
The MPS3 motherboard MB directory contains a configuration HBI subdirectory that matches the HBI code of the board.
The HBI subdirectory contains:
• A file of the form mbb_vxxx.ebf. This file is an MCC BIOS image.
• A board.txt file that defines the MCC BIOS image.
• An application-specific subdirectory that contains the following board configuration files:
  — Image files for the FPGA, that have .bit extensions, and for the MCC, that have .rbe extensions.
• An images.txt file that defines the .axf files that the MCC loads into external memory during
  configuration:
• An application note .txt file that defines:
  — The number of FPGAs on the board.
  — The number of oscillators and their frequencies.
  — FPGA image file.
  — Details of the SCC registers.

The following example shows a typical MPS3 motherboard configuration board.txt file.

```plaintext
BOARD: HBI0309
TITLE: Motherboard configuration file

[MCC]
MBIOS mbb_v020.ebf ;MB BIOS IMAGE

[APPLICATION NOTE]
;Please select the required processor
;APPFILE: AN522\an522_v1.txt ;MPS3 test image
```

The following example shows a typical MPS3 motherboard configuration application note .txt file.

```plaintext
BOARD: HBI0309
TITLE: AN??? application note configuration file

[FPGAS]
TOTALFPGAS: 1 ;Total Number of FPGAS (Max : 1)
F0FILE: an522_v1.bit ;FPGA0 Filename
F0MODE: FPGA ;FPGA0 Programming Mode

[OSCCLKS]
TOTALOSCCLKS: 7
OSC0: 24.0 ;OSC0 - REFCLK24MHz
OSC1: 32.0 ;OSC1 - ACLK
OSC2: 50.0 ;OSC2 - MCLK
OSC3: 50.0 ;OSC3 - GPCLK
OSC4: 24.576 ;OSC4 - AUDCLK
OSC5: 23.75 ;OSC5 - HDLCD (MCC overrides this value)
OSC6: 100.0 ;OSC6 - GTX clock (DDR)

[SCC REGISTERS]
TOTALSYSCONS: 1 ;Total Number of SYSCON registers defined
SYSCON: 0x000 0x00000001

[PERIPHERALS]
LANBASE: 0x64000000 ;LAN peripheral base address
RTCBASE: 0x64000000 ;RTC peripheral base address
FPGAREG: 0x64300000 ;FPGA peripheral base address
SCCREG: 0x64300000 ;SCC peripheral base address
QSPIBASE: 0x64000000 ;QSPI peripheral base address
QSPIDATA: 0x62000000 ;QSPI peripheral data address
XIPBASE: 0x64000000 ;QSPI/XIP peripheral base address
```

If a particular base address is not defined in the PERIPHERALS section, the Motherboard Configuration
Controller (MCC) uses the address in Application Note AN522 Example IoT Kit Subsystem design for
MPS3. If you use another image which does not implement a particular peripheral, you must set the base
address to 0x0. The 0x0 base address prevents the MCC from attempting to configure that peripheral.

The following example shows a typical MPS3 motherboard images.txt file.

```plaintext
TITLE: Versatile Express Images Configuration File

[IMAGES]
TOTALIMAGES: 1 ;Number of Images (Max : 32)
IMAGE0ADDRESS: 0x85000000 ;Please select the required executable program
IMAGE0UPDATE: AUTO ;Image Update:NONE/AUTO/FORCE
IMAGE0FILE: \SOFTWARE\st_viot.axf ; - selftest uSD
;IMAGE0FILE: \SOFTWARE\st_emmc.axf ; - selftest emmc, also supports QSPI boot
;IMAGE0FILE: \SOFTWARE\demo_IoT.axf ; - V2M-MSP3 demo
;IMAGE0FILE: \SOFTWARE\shield.axf ; - Shield demo
```
See 2.7 MCC-SMC interface on page 2-30 for information on the IMAGE0ADDRESS variable.

.axf and .elf files are treated as elf files. All other files are treated as binary.

**Related references**

3.1 Overview of the configuration system on page 3-54.
3.2 Powerup and configuration sequence on page 3-56.

### 3.4.4 Contents of the SOFTWARE directory

The SOFTWARE directory can contain applications that you can load into the QSPI flash, BRAM, or DDR4 memory. The memory that is loaded depends on the image that you implement in the FPGA.

You can create applications and load them into the memory on the motherboard. Application images are typically boot images or demo programs and have a .axf extension.

Typical applications in this directory are:
- demo_IoT.axf board demonstration software.
- st_viot.axf board test software.

**Related references**

3.1 Overview of the configuration system on page 3-54.
3.2 Powerup and configuration sequence on page 3-56.
Appendix A
Signal descriptions

This appendix lists the signals at the interface connectors of the MPS3 motherboard.

It contains the following sections:

• *A.1 Debug connectors* on page Appx-A-66.
• *A.3 Peripheral Module (Pmod) connectors* on page Appx-A-75.
• *A.4 FMC-HPC connector* on page Appx-A-77.
• *A.5 FMC configuration connector* on page Appx-A-78.
• *A.6 Combined Ethernet and dual USB-A connector* on page Appx-A-79.
• *A.7 HDMI Type A female connector* on page Appx-A-80.
• *A.8 Audio connectors, stacked stereo jacks* on page Appx-A-81.
• *A.9 12V power connector* on page Appx-A-82.
A.1 Debug connectors

The MPS3 motherboard provides connectors that support P-JTAG processor debug, F-JTAG FPGA debug, 16-bit and 4-bit trace, and SWD.

This section contains the following subsections:
- A.1.6 Debug USB 2.0 connector on page Appx-A-70.

A.1.1 20-pin IDC connector

The MPS3 motherboard provides one 1V8 20-pin IDC connector that supports P-JTAG processor debug to enable connection of DSTREAM, or a compatible third-party debugger. The connector also supports Serial Wire Debug (SWD).

The 20-pin IDC connector connects to general-purpose pins on the FPGA. The availability of P-JTAG or SWD depends on the design that you implement in the FPGA.

The following figure shows the 20-pin IDC connector, J14.

![Figure A-1 20-pin IDC connector](image)

The following table shows the pin mapping for each P-JTAG and SWD signal on the 20-pin IDC connector.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1V8_REF</td>
<td>2</td>
<td>1V8</td>
</tr>
<tr>
<td>3</td>
<td>nTRST</td>
<td>4</td>
<td>GND</td>
</tr>
<tr>
<td>5</td>
<td>TDI</td>
<td>6</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>SWDIO/TMS</td>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>SWDCLK/TCK</td>
<td>10</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>GND/RTCK</td>
<td>12</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>SWO/TDO</td>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>nSRST</td>
<td>16</td>
<td>GND</td>
</tr>
<tr>
<td>17</td>
<td>NC/DBGQ</td>
<td>18</td>
<td>GNDDETECT</td>
</tr>
<tr>
<td>19</td>
<td>NC/DBACK</td>
<td>20</td>
<td>GND</td>
</tr>
</tbody>
</table>

Note

- Pins 1, 3, 5, 7, 13, 15, and 19 have pullup resistors to 1V8.
- Pins 9, 11, and 17 have pulldown resistors to GND.
A.1.2 10-pin IDC connector

The MPS3 motherboard provides one 1V8 10-pin IDC connector that supports P-JTAG processor debug to enable connection of DSTREAM or a compatible third-party debugger. The connector also supports Serial Wire Debug (SWD).

The 10-pin IDC connector connects to general-purpose pins on the FPGA. The availability of P-JTAG or SWD depends on the design that you implement in the FPGA.

The following figure shows the 10-pin IDC connector, J15.

![Figure A-2 10-pin IDC connector](image)

The following table shows the pin mapping for each P-JTAG and SWD signal on the 10-pin IDC connector.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1V8</td>
<td>2</td>
<td>SWDIO/TMS</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>4</td>
<td>SWDCLK/TCK</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>SWO/TDO</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>8</td>
<td>NC/TDI</td>
</tr>
<tr>
<td>9</td>
<td>GNDDETECT</td>
<td>10</td>
<td>nSRST</td>
</tr>
</tbody>
</table>

---

**Note**

- Pins 2, 6, 8, and 10 have pullup resistors to 1V8.
- Pin 4 has a pulldown resistor to GND.

A.1.3 20-pin Cortex debug and ETM connector

The MPS3 motherboard provides one 1V8 20-pin Cortex debug and Embedded Trace Macrocell (ETM) connector. The connector supports P-JTAG processor debug to enable connection of DSTREAM, or a compatible third-party debugger. The connector also supports Serial Wire Debug (SWD) and 4-bit trace.

The 20-pin Cortex debug and ETM connector connects to general-purpose pins on the FPGA. The availability of P-JTAG, SWD, or 4-bit trace depends on the design that you implement in the FPGA.

The following figure shows the 20-pin Cortex debug and ETM connector, J12.
The following table shows the pin mapping for each P-JTAG, SWD, and 4-bit trace signal on the 20-pin Cortex debug and ETM connector.

### Table A-3 20-pin Cortex debug and ETM connector, J12, pin mapping

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1V8</td>
<td>2</td>
<td>SWDIOTMS</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>4</td>
<td>SWDCLKTCK</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>SWOTDOEXTa</td>
</tr>
<tr>
<td>7</td>
<td>NC</td>
<td>8</td>
<td>NC/TDIEXTb</td>
</tr>
<tr>
<td>9</td>
<td>GNDDETECT</td>
<td>10</td>
<td>nSRST</td>
</tr>
<tr>
<td>11</td>
<td>3V0_OUT</td>
<td>12</td>
<td>TRACECLK</td>
</tr>
<tr>
<td>13</td>
<td>3V0_OUT</td>
<td>14</td>
<td>TRACEDATA[0]</td>
</tr>
<tr>
<td>15</td>
<td>GND</td>
<td>16</td>
<td>TRACEDATA[1]</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>18</td>
<td>TRACEDATA[2]</td>
</tr>
<tr>
<td>19</td>
<td>GND</td>
<td>20</td>
<td>TRACEDATA[3]</td>
</tr>
</tbody>
</table>

#### Note
- Pins 2, 6, 8, 9, 10, 11, and 13 have pullup resistors to 1V8.
- Pin 4 has a pulldown resistor to GND.

### Related references

- 2.18 System debug on page 2-49.
- 1.3 Location of components on the MPS3 motherboard on page 1-15.

### A.1.4 38-pin MICTOR connector

The MPS3 motherboard provides one 1V8 38-pin MICTOR connector. The connector supports P-JTAG processor debug to enable connection of DSTREAM, or a compatible third-party debugger. The connector also supports Serial Wire Debug (SWD) and 16-bit trace.

The 38-pin MICTOR connector connects to general-purpose pins on the FPGA. The availability of P-JTAG, SWD, or 16-bit trace depends on the design that you implement in the FPGA.

The following figure shows the 38-pin MICTOR connector, J13.
The following table shows the pin mapping for each P-JTAG, SWD, and 16-bit trace signal on the 20-pin Cortex debug and ETM connector.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NC</td>
<td>2</td>
<td>NC</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>4</td>
<td>NC</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>TRACECLK</td>
</tr>
<tr>
<td>7</td>
<td>DBGRQ</td>
<td>8</td>
<td>DBGACK</td>
</tr>
<tr>
<td>9</td>
<td>NC/nSRST</td>
<td>10</td>
<td>EXTTRIG</td>
</tr>
<tr>
<td>11</td>
<td>TDO/SWO</td>
<td>12</td>
<td>1V8 reference</td>
</tr>
<tr>
<td>13</td>
<td>RTCK</td>
<td>14</td>
<td>1V8_OUT</td>
</tr>
<tr>
<td>15</td>
<td>TCK/SWCLK</td>
<td>16</td>
<td>TRACEDATA[7]</td>
</tr>
<tr>
<td>17</td>
<td>TMS/SWDIO</td>
<td>18</td>
<td>TRACEDATA[6]</td>
</tr>
<tr>
<td>19</td>
<td>TDI</td>
<td>20</td>
<td>TRACEDATA[5]</td>
</tr>
<tr>
<td>21</td>
<td>nTRST</td>
<td>22</td>
<td>TRACEDATA[4]</td>
</tr>
<tr>
<td>29</td>
<td>TRACEDATA[12]</td>
<td>30</td>
<td>GND</td>
</tr>
<tr>
<td>33</td>
<td>TRACEDATA[10]</td>
<td>34</td>
<td>1V8 reference</td>
</tr>
<tr>
<td>35</td>
<td>TRACEDATA[9]</td>
<td>36</td>
<td>TRACECTL</td>
</tr>
<tr>
<td>37</td>
<td>TRACEDATA[8]</td>
<td>38</td>
<td>TRACEDATA[0]</td>
</tr>
</tbody>
</table>

--- Note ---

- Pins 9, 11, 17, 19, and 21 have pullup resistors to 1V8.
- Pins 13 and 15 have pulldown resistors to GND.

---

**Related references**

2.18 System debug on page 2-49.
1.3 Location of components on the MPS3 motherboard on page 1-15.

**A.1.5 14-pin F-JTAG ILA connector**

The MPS3 motherboard provides one 3V3 14-pin F-JTAG ILA connector that supports FPGA debug. It enables you to connect an ILA device, such as SignalTap II, to a hard FPGA JTAG chain in the FPGA and debug your design.

The following figure shows the 14-pin F-JTAG ILA connector, J17.
The following table shows the pin mapping for each P-JTAG and SWD signal on the 14-pin F-JTAG ILA connector.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>2</td>
<td>3V3_OUT</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>4</td>
<td>FPGA_TMS</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>FPGA_TCK</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>8</td>
<td>FPGA_TDO</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>10</td>
<td>FPGA_TDI</td>
</tr>
<tr>
<td>11</td>
<td>NC</td>
<td>12</td>
<td>NC</td>
</tr>
<tr>
<td>13</td>
<td>NC</td>
<td>14</td>
<td>NC</td>
</tr>
</tbody>
</table>

**Note**
- Pins 4, 8, and 10 have pullup resistors to 3V3.
- Pin 6 has a pulldown resistor to GND.

**Related references**

1.3 *Location of components on the MPS3 motherboard* on page 1-15.
2.18 *System debug* on page 2-49.

### A.1.6 Debug USB 2.0 connector

The MPS3 motherboard provides one USB 2.0 connector that supports configuration file editing in the microSD, UART access to the FPGA, and CMSIS-DAP FPGA debug using SWD only.

The following figure shows the USB type B connector, J8.

**Related references**

1.3 *Location of components on the MPS3 motherboard* on page 1-15.
2.18 *System debug* on page 2-49.
A.2 Arduino Shield connectors

Connectors on the MPS3 motherboard provide two Shield expansion interfaces. Each interface provides 16 digital I/O and six analog I/O.

The Peripheral Module interface (Pmod) connectors share some of the Shield connectors and are wired in parallel with them. Interface Pmod0/1 shares some signals with Shield 0 interface, and Pmod2/3 shares some signals with Shield 1 interface.

--- Caution ---
The MPS3 motherboard supports simultaneous use of Pmod and Shield expansion but you must take care when driving the shared signals.

Shield 0 and Shield 1 interface connectors

The following figure shows a combined diagram of the Arduino Shield 0 and Arduino Shield 1 interfaces on the MPS3 motherboard.

---Figure A-7 Shield 0 and Shield 1 interface connectors on the MPS3 motherboard---

Connectors J25, J26, J27, J29, and J30 form the Shield 0 interface.

Connectors J33, J35, J36, J37, and J39 form the Shield 1 interface.
See 1.3 Location of components on the MPS3 motherboard on page 1-15 for the location of the Arduino Shield interface connectors on the MPS3 motherboard.

Note
User-links select digital I/O operating voltages and power inputs. The power inputs and IOREF voltages have maximum current limits available at the board interface pins. See 2.16 Arduino Shield and Pmod interfaces on page 2-43 for information on the user-links, and the maximum available IOREF currents.

Digital I/O connectors: Connectors J25, J33, J30, and J39
Connector J25 provides Shield 0 I/O[15:8], and connector J33 provides Shield 1 I/O[15:8]. The connectors also provide the analog I/O reference voltages. The following table shows the pin mapping for connectors J25 and J33.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0/SH1_IO8</td>
</tr>
<tr>
<td>2</td>
<td>SH0/SH1_IO9</td>
</tr>
<tr>
<td>3</td>
<td>SH0/SH1_IO10</td>
</tr>
<tr>
<td>4</td>
<td>SH0/SH1_IO11</td>
</tr>
<tr>
<td>5</td>
<td>SH0/SH1_IO12</td>
</tr>
<tr>
<td>6</td>
<td>SH0/SH1_IO13</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>SH0/SH1_AREF</td>
</tr>
<tr>
<td>9</td>
<td>SH0/SH1_IO14</td>
</tr>
<tr>
<td>10</td>
<td>SH0/SH1_IO15</td>
</tr>
</tbody>
</table>

Connector J30 provides Shield 0 I/O[7:0] and connector J36 provides Shield 1 I/O[7:0]. The following table shows the pin mapping for connectors J30 and J36.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0/SH1_IO0</td>
</tr>
<tr>
<td>2</td>
<td>SH0/SH1_IO1</td>
</tr>
<tr>
<td>3</td>
<td>SH0/SH1_IO2</td>
</tr>
<tr>
<td>4</td>
<td>SH0/SH1_IO3</td>
</tr>
<tr>
<td>5</td>
<td>SH0/SH1_IO4</td>
</tr>
<tr>
<td>6</td>
<td>SH0/SH1_IO5</td>
</tr>
<tr>
<td>7</td>
<td>SH0/SH1_IO6</td>
</tr>
<tr>
<td>8</td>
<td>SH0/SH1_IO7</td>
</tr>
</tbody>
</table>

Analog I/O connectors: Connectors J29 and J39
Connector J29 provides six analog I/O for Shield 0 and connector J36 provides six analog I/O for Shield 1. The following table shows the pin mapping for connectors J29 and J39.
Table A-8 Connectors J29 (Shield 0) and J39 (Shield 1) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SHO/SH1_AD0</td>
</tr>
<tr>
<td>2</td>
<td>SHO/SH1_AD1</td>
</tr>
<tr>
<td>3</td>
<td>SHO/SH1_AD2</td>
</tr>
<tr>
<td>4</td>
<td>SHO/SH1_AD3</td>
</tr>
<tr>
<td>5</td>
<td>SHO/SH1_AD4</td>
</tr>
<tr>
<td>6</td>
<td>SHO/SH1_AD5</td>
</tr>
</tbody>
</table>

Power and voltage references: Connectors J26 and J35

Connector J26 provides power and voltage references for Shield 0 digital I/O. Connector J35 provides power and voltage references for Shield 1 digital I/O. The following table shows the pin mapping for Shield connectors J26 and J35.

Table A-9 Connectors J26 (Shield 0) and J35 (Shield 1) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>N/C</td>
</tr>
<tr>
<td>2</td>
<td>SHO/SH1_IOREF</td>
</tr>
<tr>
<td>3</td>
<td>SHO/SH1_nRST</td>
</tr>
<tr>
<td>4</td>
<td>3V3</td>
</tr>
<tr>
<td>5</td>
<td>5V</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
</tr>
<tr>
<td>8</td>
<td>SHO/SH1_VIN</td>
</tr>
</tbody>
</table>

Supplementary connectors J27 and J37

The supplementary connectors, J27 and J37, provide subsets of the signals on the main Shield connectors. Connector J27 provides a subset of the Shield 0 signals and connector J37 provides a subset of the Shield 1 signals. The following table shows the pin mapping for connectors J27 and J37.

Table A-10 Connectors J27 (Shield 0) and J37 (Shield 1) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SHO/SH1_IO12</td>
</tr>
<tr>
<td>2</td>
<td>5V</td>
</tr>
<tr>
<td>3</td>
<td>SHO/SH1_IO13</td>
</tr>
<tr>
<td>4</td>
<td>SHO/SH1_IO11</td>
</tr>
<tr>
<td>5</td>
<td>SHO/SH1_nRST</td>
</tr>
<tr>
<td>6</td>
<td>GND</td>
</tr>
</tbody>
</table>
Related references

2.16 Arduino Shield and Pmod interfaces on page 2-43.
1.3 Location of components on the MPS3 motherboard on page 1-15.
A.3 Peripheral Module (Pmod) connectors

The Pmod connectors on the MPS3 motherboard provide digital I/O expansion capability, an alternative to the Shield interfaces.

The four Pmod connectors enable fitting of TYPE 2A (J24/J34) and TYPE 1 (J28/J38) boards. Connectors J24 and J28 form interface Pmod0/1 and connectors J34 and J38 form interface Pmod2/3. The Pmod connectors carry a subset of the signals on the Arduino connectors and are wired in parallel with them. Interface Pmod0/1 shares signals with Shield 0 interface, and Pmod2/3 shares signals with Shield 1 interface.

**Note**

User-links select 3V3 or 5V digital I/O operating voltages, and the digital IOREF voltages. The IOREF voltages have maximum current limits available at the board interface pins. See 2.16 Arduino Shield and Pmod interfaces on page 2-43 for information on the user-links, and the maximum available IOREF current.

**Caution**

The MPS3 motherboard supports simultaneous use of Pmod and Shield expansion but you must exercise caution when driving the shared signals.

The following figure shows the Pmod connectors.

![Figure A-8 Pmod connectors J24, J28, J34, and J38](image)

The following table shows the pin mapping for the Pmod0/1 interface connector, J24.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0_5V_IO10</td>
<td>7</td>
<td>SH0_5V_IO5</td>
</tr>
<tr>
<td>2</td>
<td>SH0_5V_IO11</td>
<td>8</td>
<td>SH0_5V_IO6</td>
</tr>
<tr>
<td>3</td>
<td>SH0_5V_IO12</td>
<td>9</td>
<td>SH0_5V_IO7</td>
</tr>
<tr>
<td>4</td>
<td>SH0_5V_IO13</td>
<td>10</td>
<td>SH0_5V_IO8</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>11</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>SH0_REF</td>
<td>12</td>
<td>SH0_REF</td>
</tr>
</tbody>
</table>

The following table shows the pin mapping for the Pmod0/1 interface connector, J28.
Table A-12  Connector J28 (Pmod0/1 interface) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0_5V_IO3</td>
<td>7</td>
<td>SH0_5V_IO4</td>
</tr>
<tr>
<td>2</td>
<td>SH0_5V_IO1</td>
<td>8</td>
<td>SH0_5V_IO2</td>
</tr>
<tr>
<td>3</td>
<td>SH0_5V_IO0</td>
<td>9</td>
<td>SH0_5V_IO15</td>
</tr>
<tr>
<td>4</td>
<td>SH0_5V_IO9</td>
<td>10</td>
<td>SH0_5V_IO14</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>11</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>SH0_REF</td>
<td>12</td>
<td>SH0_REF</td>
</tr>
</tbody>
</table>

The following table shows the pin mapping for the Pmod2/3 interface connector, J34.

Table A-13  Connectors J34 (Pmod2/3 interface) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0_5V_IO10</td>
<td>7</td>
<td>SH1_5V_IO5</td>
</tr>
<tr>
<td>2</td>
<td>SH0_5V_IO11</td>
<td>8</td>
<td>SH1_5V_IO6</td>
</tr>
<tr>
<td>3</td>
<td>SH0_5V_IO12</td>
<td>9</td>
<td>SH1_5V_IO7</td>
</tr>
<tr>
<td>4</td>
<td>SH0_5V_IO13</td>
<td>10</td>
<td>SH1_5V_IO8</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>11</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>SH1_REF</td>
<td>12</td>
<td>SH1_REF</td>
</tr>
</tbody>
</table>

The following table shows the pin mapping for the Pmod2/3 interface connector, J38.

Table A-14  Connectors J38 (Pmod2/3 interface) signal list

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SH0_5V_IO3</td>
<td>7</td>
<td>SH1_5V_IO4</td>
</tr>
<tr>
<td>2</td>
<td>SH0_5V_IO9</td>
<td>8</td>
<td>SH1_5V_IO2</td>
</tr>
<tr>
<td>3</td>
<td>SH0_5V_IO0</td>
<td>9</td>
<td>SH1_5V_IO15</td>
</tr>
<tr>
<td>4</td>
<td>SH0_5V_IO1</td>
<td>10</td>
<td>SH1_5V_IO14</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>11</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>SH1_REF</td>
<td>12</td>
<td>SH1_REF</td>
</tr>
</tbody>
</table>

Related references

2.16 Arduino Shield and Pmod interfaces on page 2-43.
1.3 Location of components on the MPS3 motherboard on page 1-15.
A.4 FMC-HPC connector

The MPS3 motherboard provides a 400-way Samtec SEARAY connector to support the FPGA Mezzanine Card standard, high pin count variant, FMC-HPC.

The following figure shows the FMC-HPC connector, J9.

![FMC-HPC connector](image_url)

**Figure A-9  FMC-HPC connector**


**Related references**

2.17 FMC-HPC interface on page 2-46.

1.3 Location of components on the MPS3 motherboard on page 1-15.
A.5 FMC configuration connector

The MPS3 motherboard provides a custom 14-pin connector to enable configuration of Arm FMC boards.

The FMC configuration connector is reserved for Arm FMC boards only.

The following figure shows the FMC-HPC configuration connector, J61.

![FMC-HPC configuration connector](image)

**Figure A-10  FMC-HPC configuration connector**

**Related references**

2.17 FMC-HPC interface on page 2-46.

1.3 Location of components on the MPS3 motherboard on page 1-15.
A.6 Combined Ethernet and dual USB-A connector

The MPS3 motherboard provides a combined Ethernet and dual USB-A connector that connects to the Ethernet 10/100 controller and to the USB 2.0 controller.

The following figure shows the combined Ethernet and dual USB-A connector, J2.

![Combined Ethernet and dual USB-A connector](image)

Figure A-11 Combined Ethernet and dual USB-A connector

Related references

2.8 USB 2.0 and Ethernet static memory interface on page 2-35.
1.3 Location of components on the MPS3 motherboard on page 1-15.
A.7 HDMI Type A female connector

The female HDMI connector on the MPS3 motherboard provides digital video and digital audio to external displays.

The following figure shows the HDMI connector, J3.

![HDMI connector](image)

The following table shows the pin mapping for the HDMI connector, J3, including encoded I2S digital audio.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Signal</th>
<th>Pin</th>
<th>Signal</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DVI_TX2P</td>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>DVI_TX2N</td>
<td>4</td>
<td>DVI_TX1P</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>6</td>
<td>DVI_TX1N</td>
</tr>
<tr>
<td>7</td>
<td>DVI_TX0P</td>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>DVI_TX0N</td>
<td>10</td>
<td>DVI_TXCP</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td>12</td>
<td>DVI_TXCN</td>
</tr>
<tr>
<td>13</td>
<td>DVI_CECAO</td>
<td>14</td>
<td>No connection</td>
</tr>
<tr>
<td>15</td>
<td>DVI_DSCLO</td>
<td>16</td>
<td>DVI_DSDAO</td>
</tr>
<tr>
<td>17</td>
<td>GND</td>
<td>18</td>
<td>DVI_5V0</td>
</tr>
<tr>
<td>19</td>
<td>DVI_HPDO</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

Related references

2.9 Video HDLCD interface on page 2-36.
1.3 Location of components on the MPS3 motherboard on page 1-15.
A.8 Audio connectors, stacked stereo jacks

The MPS3 motherboard provides three stacked 3.5mm stereo jack connectors that connect to a stereo audio codec. The connectors provide line-level stereo input, line-level stereo output, and microphone-level stereo input.

The top, blue, jack is the line-in connector. The middle, green, jack is the line-out connector. The bottom, pink, jack is the microphone-in connector.

When using electret microphones, use jumpers J58 (L) and J59 (R) to enable microphone bias current.

The following figure shows the three stereo jack connectors, J4.

![Figure A-13 Stacked stereo jack connectors](image)

Related references

2.10 Audio codec interface on page 2-37.
1.3 Location of components on the MPS3 motherboard on page 1-15.
A.9 12V power connector

The MPS3 motherboard provides a Thru-hole DC power jack for connecting external power to the board.

Connect the external mains power supply unit, that Arm supplies with the MPS3 motherboard, to the power jack.

Alternatively, you can connect an external 12V 5A, +/-10%, power supply to the power jack.

Note
The center pin is the positive side of the power supply.

Related references
2.5 Power on page 2-27.
1.3 Location of components on the MPS3 motherboard on page 1-15.
Appendix B
Specifications

This appendix contains electrical specifications of the MPS3 motherboard.

It contains the following section:
• B.1 Available power for expansion boards on page Appx-B-84.
B.1 Available power for expansion boards

The MPS3 motherboard supplies power to the expansion boards through the expansion connectors.

**FMC-HPC power**

The MPS3 motherboard supplies power, through the FMC-HPC connector, to a fitted FMC-HPC board. The following table shows the maximum current that the board can supply from each power rail.

<table>
<thead>
<tr>
<th>Power rail</th>
<th>Voltage</th>
<th>Max load</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>12P0V</td>
<td>12V</td>
<td>1A</td>
<td>-</td>
</tr>
<tr>
<td>3P3VAUX</td>
<td>3V3 standby</td>
<td>20mA</td>
<td>For FMC EEPROM only</td>
</tr>
<tr>
<td>3P3V</td>
<td>3V3</td>
<td>2.5A</td>
<td>-</td>
</tr>
<tr>
<td>FMCVADJ</td>
<td>1V2/1V5/1V8</td>
<td>4A</td>
<td>Other voltages are not supported</td>
</tr>
</tbody>
</table>

**Shield expansion and Pmod expansion power**

The MPS3 motherboard supplies power to expansion Shields or Pmod expansion boards, depending on what expansion boards are fitted. The following table shows the maximum current that the board can supply from each power rail.

<table>
<thead>
<tr>
<th>Power rail</th>
<th>Max load</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>3V3</td>
<td>1A</td>
<td>Maximum current available for both Shields, or all four Pmod expansion boards. Includes digital I/O reference IOREF.</td>
</tr>
<tr>
<td>5V</td>
<td>1A</td>
<td>Maximum current available for both Shields, or all four Pmod expansion boards. Includes digital I/O reference IOREF.</td>
</tr>
<tr>
<td>12V</td>
<td>0.5A</td>
<td>Maximum current available for both Shields, or all four Pmod expansion boards. Includes digital I/O reference IOREF.</td>
</tr>
</tbody>
</table>

**Note**

User-links on the board select 3V3 or 5V digital I/O operation. See *2.16 Arduino Shield and Pmod interfaces on page 2-43* for information on the digital I/O user-links.
Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

It contains the following section:
• C.1 Revisions on page Appx-C-86.
### C.1 Revisions

The following table lists the technical changes between released issues of this book.

#### Table C-1  Issue 100765_0000_00

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>No changes, first release.</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

#### Table C-2  Difference between issue 100765_0000_00 and issue 100765_0000_01

<table>
<thead>
<tr>
<th>Change</th>
<th>Location</th>
<th>Affects</th>
</tr>
</thead>
<tbody>
<tr>
<td>Remove mention of JTAG mode from description of MPS3 DAP-Link interface.</td>
<td>2.18 System debug on page 2-49. A.1.6 Debug USB 2.0 connector on page Appx-A-70.</td>
<td>All versions.</td>
</tr>
<tr>
<td>Remove statement that availability of P-JTAG or SWD depends on the design that the user implements in the FPGA.</td>
<td>A.1.5 14-pin F-JTAG ILA connector on page Appx-A-69.</td>
<td>All versions.</td>
</tr>
</tbody>
</table>