AMBA Decoder
Data Sheet
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Release Information

The following changes have been made to this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Issue</th>
<th>Confidentiality</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

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Chapter 1

AMBA Decoder

The following sections describe the function of the AMBA decoder.

- *Overview* on page 1-2
- *Signal description* on page 1-4
- *Memory map* on page 1-6
- *Decoder function* on page 1-7.
1.1 Overview

The decoder performs three functions:

- It generates the slave select signals (DSELx) for each of the bus slaves, indicating that a transfer to that slave is required.
- It generates the slave response signals (BWAIT, BLAST and BERROR) during Address-only transfers, when no slave is selected.
- It can act as a simple protection unit which prevents attempts to access an illegal or protected area of the memory map.

Two implementations of the decoder are provided:

- Decoder with decode cycles. This is the default model. This implementation automatically inserts a decode cycle:
  - at the start of a non-sequential transfer
  - on a sequential transfer when BLAST has been asserted
  - when 1KB memory boundaries are reached

  This decoder is used in fast systems where the decoder might not have enough time to decode the address and assert the corresponding DSEL signal in a single clock HIGH phase.

- Decoder without decode cycles. This implementation attempts to decode the address bus on every cycle, and therefore will only be suitable for slow systems where this can be safely achieved.

Every system must have a default bus master which is granted use of the bus during reset, when no other bus master requires the bus.

A block diagram of the decoder is shown below:
* only used by the decoder with decode cycles

Figure 1-1 Decoder block diagram
1.2 Signal description

This section describes the signals that interface to the decoder.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BA[31:0]</td>
<td>In</td>
<td>This is the system address bus, which is driven by the bus master. The addresses change during the HIGH phase before the transfer to which they refer, and remain valid until the last HIGH phase of the transfer.</td>
</tr>
<tr>
<td>BCLK</td>
<td>In</td>
<td>System (bus) clock. This clock times all bus transfers. The clock has two distinct phases: phase 1 in which BCLK is LOW, and phase 2 in which BCLK is HIGH.</td>
</tr>
<tr>
<td>BERROR</td>
<td>InOut</td>
<td>A transfer error is indicated by the selected bus slave or decoder using the BERROR signal. When BERROR is HIGH, a transfer error has occurred. When BERROR is LOW, the transfer is successful. This signal is also used in combination with the BLAST signal to indicate a bus retract operation. When no bus transfer is taking place, this signal is driven by the decoder. This signal is driven in the LOW phase of BCLK and is valid before the rising edge of BCLK.</td>
</tr>
<tr>
<td>BLAST</td>
<td>InOut</td>
<td>This signal is driven by the selected bus slave or decoder to indicate whether the current transfer should be the last of a burst sequence. When BLAST is HIGH, the next bus transfer must allow sufficient time for address decoding. When BLAST is LOW, the next transfer may continue a burst sequence. This signal is also used in combination with the BERROR signal to indicate a bus retract operation. When no bus transfer is taking place, this signal is driven by the decoder. This signal is driven in the LOW phase of BCLK and is valid before the rising edge of BCLK.</td>
</tr>
<tr>
<td>BnRES</td>
<td>In</td>
<td>This active LOW signal indicates the reset status of the bus and is driven by the reset controller.</td>
</tr>
<tr>
<td>BTRAN[1:0]</td>
<td>In</td>
<td>These signals indicate the type of the next transaction, which may be address-only, nonsequential or sequential. These signals are valid during the phase HIGH before the transfer to which they refer.</td>
</tr>
<tr>
<td>BWAIT</td>
<td>InOut</td>
<td>This signal is driven by the selected bus slave or decoder to indicate whether the current transfer may complete. If BWAIT is HIGH, a further bus cycle is required. If BWAIT is LOW, the transfer may complete in the current bus cycle. When no bus transfer is taking place, this signal is driven by the bus decoder (this block). This signal is driven in the LOW phase of BCLK and is valid before the rising edge of BCLK.</td>
</tr>
</tbody>
</table>
DSELx
Slave Select
This signal indicates that a slave device is selected and a data transfer is required. There is a DSELx signal for each bus slave. This signal becomes valid during the phase HIGH before the data transfer is required, and remains active until the last phase HIGH of the transfer.

BSIZE[1:0]
Transfer Size
These signals indicate the size of the transfer which may be byte, halfword or word. They are only needed by the decoder with decode cycles implementation. They have the same timing as the system address bus.

ReMap
In
When LOW, this forces the internal memory to be replaced by the external memory. The external memory should contain the system’s start-up program (boot ROM/BIOS). In normal operation this signal is HIGH.

<table>
<thead>
<tr>
<th>Name</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSELx</td>
<td>Out</td>
<td>This signal indicates that a slave device is selected and a data transfer is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>required. There is a DSELx signal for each bus slave.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>This signal becomes valid during the phase HIGH before the data transfer is</td>
</tr>
<tr>
<td></td>
<td></td>
<td>required, and remains active until the last phase HIGH of the transfer.</td>
</tr>
<tr>
<td>BSIZE[1:0]</td>
<td>In</td>
<td>These signals indicate the size of the transfer which may be byte, halfword</td>
</tr>
<tr>
<td></td>
<td></td>
<td>or word. They are only needed by the decoder with decode cycles implementation.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>They have the same timing as the system address bus.</td>
</tr>
<tr>
<td>ReMap</td>
<td>In</td>
<td>When LOW, this forces the internal memory to be replaced by the external</td>
</tr>
<tr>
<td></td>
<td></td>
<td>memory. The external memory should contain the system’s start-up program</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(boot ROM/BIOS). In normal operation this signal is HIGH.</td>
</tr>
</tbody>
</table>
1.3 Memory map

The decoder controls the memory map of the system, and generates a slave select signal for each memory region.

The ReMap signal is used to provide a different memory map at reset, when ROM is required at address 0, and during normal operation, when RAM may be used at address 0.

The ReMap signal is typically provided by a remap and pause peripheral, which drives ReMap LOW at reset. The signal is only driven HIGH after a particular address in the remap and pause peripheral is accessed.

Figure 1-2 shows both the Normal and Reset memory maps.

![Figure 1-2 Memory map](image-url)
1.4 Decoder function

At the start of every transfer on the bus the decoder can perform a number of actions. The decoder is able to determine when a transfer is about to start by examining the BWAIT signal, which will be LOW when the previous transfer is completing.

The actions the decoder may take depend on the type of transfer:

- **Nonsequential transfer**
  The decoder inserts a single decode cycle to allow the address bus to stabilize and the new address to be decoded. For the first cycle, the decoder drives BWAIT HIGH and negates all DSELx signals. In the second cycle, the decoder asserts the appropriate DSELx, and the selected slave becomes responsible for driving the slave transfer response. This is the case for a decoder that implements decode cycles, otherwise the decoder asserts the DSELx signal during the first cycle (see Figure 1-4 on page 1-8).

- **Sequential transfer with BLAST LOW**
  The decoder drives the appropriate DSELx signal, and the selected slave is responsible for driving the slave transfer response.

- **Sequential transfer with BLAST HIGH**
  The decoder treats this case in the same way as a nonsequential transfer.

- **Address-only transfer**
  The decoder does not generate any DSELx signals and drives a slave transfer response of BWAIT LOW.

Figure 1-3 on page 1-8 illustrates a decode cycle.
1.4.1 Slave response

The decoder control block monitors bus activity, and determines when a transfer is required to a slave device. When a transfer is required, a signal is asserted to the address decoder block, which in turn generates a slave select signal depending on the address on the bus.
When no slave is selected, the decoder must provide the slave response signals (BWAIT, BLAST and BERROR) in order for the bus to remain synchronised. The decoder will drive these signals during the address-only cycle (as indicated by the BTRAN[1:0] signals which are driven by the bus master), and the decode cycle, which occurs at the start of every nonsequential transfer and may also be requested by a slave device using the BLAST signal.

The decoder with decode cycles will provide the following responses:

<table>
<thead>
<tr>
<th>Condition</th>
<th>BWAIT</th>
<th>BLAST</th>
<th>BERROR</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address-only cycle</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Error</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Decode cycle</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

The decoder without decode cycles does not provide the decode cycle response.

When a slave is selected it must provide a response on the BWAIT, BERROR and BLAST signals.

### 1.4.2 Implementation of DecError and DecLast

These two internal decoder signals are required by the state machine. DecError is used by both state machines, with and without decode cycles. It is asserted when an access is made to the undefined region.

DecLast is only needed by the state machine with decode cycles. It is asserted when the last address in a 1KB boundary is accessed, and is dependent on the size of the transfer.

### 1.4.3 Decode control state machine

There are two possible implementations of the decoder, depending on the performance requirements of the system design. One implementation inserts decode cycles, and the other does not. The state machine for the decoder with decode cycles has an extra state, DECODE.

The decoder state machine is clocked off the falling edge of the bus clock, BCLK. Therefore it is necessary for the decoder to use latched versions of the BWAIT and BLAST signals. WAIT + RETNEXT is equivalent to LBWAIT.
The decoder will drive an address-only cycle response when in the ADDRONLY state, a Decode cycle response when in the DECODE state, and an Error transfer response when in the ERROR state. The decoder will not drive the slave response signals in the SLAVESEL state; this is the responsibility of the selected slave.

Figure 1-5 on page 1-11 shows the state machine of the decoder control block.
Figure 1-5 Decoder state machine with decode cycles
State descriptions

**DECODE**  Decode cycle. The DECODE state is only entered for a single cycle. Assuming that there is no reset condition and that **DecError** is not asserted, the next state is SLAVESEL.

**SLAVESEL**  Slave transfer. The SLAVESEL state may be entered either from the DECODE or the ADDRONLY state.

Unless there is a reset condition, the state machine will remain in the SLAVESEL state when **BWAIT** is HIGH. When **BWAIT** is LOW, the next state is ADDRONLY if the transfer type is address-only, DECODE if the transfer type is nonsequential, or if **BLAST** or **DecLast** have been asserted. However, if the transfer type is sequential and **BLAST** or **DecLast** have not been asserted, the next state remains as SLAVESEL.

**Error**  Error transfer. The ERROR state is entered when **DecError** is asserted.

Unless there is a reset condition, the state machine remains in the ERROR state when the transfer type is sequential and DecLast is not asserted. The next state is ADDRONLY if the transfer type is address-only, or DECODE if the transfer type is nonsequential, or if it is sequential and **DecLast** is asserted.

Figure 1-6 on page 1-13 shows the state machine of the decoder control block.
Figure 1-6 Decoder state machine without decode cycles

!WAIT = DONE + LAST + ERROR + RETRACT
State descriptions

**ADDRONLY** No transfer. This state is entered when no data transfer is occurring on the bus. This state is also entered during a reset condition.

The ADDRONLY state is only exited when a transfer is about to occur, as indicated by the BTRAN signals. If DecError is asserted, the next state is ERROR; if it is not asserted, the next state is SLAVESEL.

**SLAVESEL** Slave transfer. The SLAVESEL state may be entered from either the ERROR or the ADDRONLY state.

Unless there is a reset condition, the state machine will remain in the SLAVESEL state when BWAIT is HIGH. When BWAIT is LOW, the next state is ADDRONLY if the transfer type is address-only, or ERROR if DecError has been asserted. However, if DecError has not been asserted, the next state remains as SLAVESEL.

**Error** Error transfer. The ERROR state is entered when DecError is asserted.

Unless there is a reset condition, the state machine remains in the ERROR state when the transfer type is sequential or nonsequential, and DecError is asserted. The next state is ADDRONLY if the transfer type is address-only, or SLAVESEL if the transfer type is sequential or nonsequential and DecError is not asserted.

### 1.4.4 Address decoder

When the decoder control section indicates that a slave transfer is required, the address decoder generates a slave select signal, depending on the address on the bus.

The address decoder section must be changed to implement a different memory map.

Signals, other than the address bus, may be used to affect the address map; ReMap is an example of such a signal.

### 1.4.5 Reset operation

During a reset condition, when BnRES is LOW, the decoder control block asynchronously removes all slave select signals.