AMBA Remap and Pause

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Technical Reference Manual

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AMBA Remap and Pause
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change History

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Proprietary Notice

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AMBA Remap and Pause Technical Reference Manual

Chapter 1
AMBA Remap and Pause

This document provides information on the Remap and Pause module, which is connected to the Advanced Peripheral Bus (APB). It contains the following sections:

1.1 About AMBA Remap and Pause

The Reset and Pause module provides:

- defined boot behavior with power on reset detection
- wait for interrupt Pause mode
- an identification register.

Figure 1-1 shows the remap and pause block diagram.

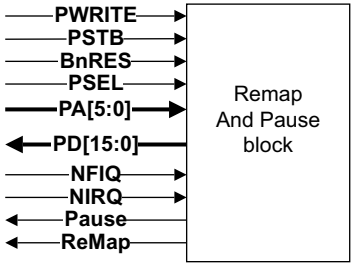

Figure 1-1 Remap and Pause block diagram

1.2 Hardware Interface and Signal Description

The Remap and Pause module is connected to the APB bus. Table 1-1 describes the APB signals used and produced.

Table 1-1 APB signal descriptions

Name	Type	Source/ Destination	Description
PA	In	APB Bridge	This is the peripheral address bus, which is used by individual peripherals for decoding register accesses to that peripheral. The addresses become valid before **PSTB** goes HIGH and remain valid after **PSTB** goes LOW.
PD	InOut	APB Peripherals, BD bus	This is the bidirectional peripheral data bus. The data bus is driven by this block during read cycles (when **PWRITE** is LOW).
PSTB	In	APB Bridge	This strobe signal is used to time all accesses on the peripheral bus. The falling edge of **PSTB** is coincident with the falling edge of **BCLK**.
PWRITE	In	APB Bridge	This signal indicates a write to a peripheral when HIGH and a read from a peripheral when LOW. It has the same timing as the peripheral address bus. It becomes valid before **PSTB** goes HIGH and remains valid after **PSTB** goes LOW.
PSEL	In	APB Bridge	When HIGH, this signal indicates that this module has been selected by the APB bridge. This selection is a decode of the system address bus. See the *AMBA Peripheral Bus Controller* for more details.
Pause	Out	APB peripherals/external world	Pause signal. Module has entered Pause mode.
ReMap	Out	Memory Controller	Remap. Output that indicates that the reset memory map is in operation.
NFIQ	In	Interrupt Controller	NFIQ interrupt input from the interrupt controller.
NIRQ	In	Interrupt Controller	NIRQ interrupt input from the interrupt controller.
BnRES	In	Reset Controller	The active LOW bus reset signal.

1.2.1 APB write cycle

Writes to the Reset and Pause module are generated from the Peripheral Bus Controller Module. Figure 1-2 shows the Reset and Pause module APB write cycle.

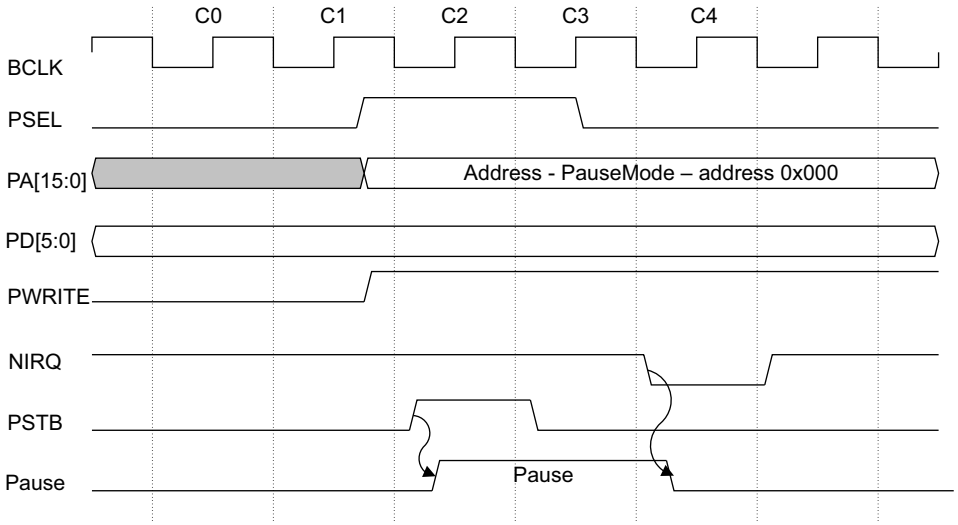

Figure 1-2 Reset and Pause module APB write cycle

The access lasts for two cycles, starting in C1 and completing in C2. Pause can be reset by the **BnRES**, **NFIQ,** or **NIRQ** signals.

1.3 Remap and Pause

The remap and pause control is the combination of the following functions:

Pause

Defines a method of allowing the processor system to enter a low-power, wait for interrupt state, when the system does not require the processor to be active.

Identification

Provides an indication of the system configuration. *Identification* describes the minimum case, a single bit identification register.

Reset status

Provides an indication of the cause of the most recent reset condition. A minimum implementation is defined.

Reset memory map

Provides a method of overlaying the system base memory at reset.

1.3.1 Pause

Pause register Write-only. Writing to the Pause location causes the system to enter a wait for interrupt state.

The exact effect of writing to this location is not defined, but typically this would prevent the processor from fetching further instructions until the receipt of an interrupt or a power on reset. Further registers may be added to provide more sophisticated power-saving modes.

1.3.2 Identification

ID register Read-only. The ID register provides identification information about the system. Only a single-bit implementation (bit 0) is required, which is used to indicate if there is further ID information.

ID Bit 0 flag Identification bit.

0 no further ID information

1 further ID information is available

If the bottom bit of the ID register is set, further bits are required to provide more detailed system identification information.

1.3.3 Reset status

Reset Status register

Read-only. The Reset Status register provides the reset status. Only one bit of this register is defined in this specification and this is bit 0, which provides the power on reset status. Further bits in the reset status register may be implemented to provide more detailed reset information.

The status register has a dual mechanism for setting and clearing bits, allowing independent bits to be altered with no knowledge of the other bits in the register.

The single bit defined in this specification is the power on reset bit, which may be used to determine if the most recent reset was caused by initial power on, or if a warm reset has occurred.

POR Bit 0 flag

Power on reset bit.

0 no POR since flag was last cleared

1 POR

Reset Status Clear register

Write-only. This location is used to clear Reset Status flags. When writing to this register each data bit which is HIGH causes the corresponding bit in the Reset Status register to be cleared. Data bits which are LOW have no effect on the corresponding bit in the Reset Status register.

Reset Status Set register

Write-only. This location is used to set Reset Status flags.When writing to this register each data bit which is HIGH causes the corresponding bit in the Reset Status register to be set. Data bits which are LOW have no effect on the corresponding bit in the Reset Status register.

This register has no function in the minimal reference microcontroller specification, because the power on reset status bit cannot be set by software. This register is included in the specification to ensure expandability of the reset status functionality.

1.3.4 Reset Memory Map

Clear Reset Map register

Write-only. Writing to the clear reset memory map location causes the system memory map to change from that required after reset, to that required during normal operation.

When the reset memory map has been cleared and the normal memory map is in use, there is no method of resuming the reset memory map, other than undergoing a power on reset condition.

A typical system implementation is to map the system ROM to location 0 at reset, but to change the memory map after reset, such that RAM is located at location 0 for normal operation. In a system where such remapping does not occur, writing to this register has no effect.

1.4 Remap and Pause Memory Map

The base address of the Remap and Pause controller memory is not fixed and can be different for any particular system implementation. However, the offset of any particular register from the base address is fixed. Table 1-2 shows the memory map of the remap and pause controller APB peripheral.

Table 1-2 Memory map of the remap and pause controller APB peripheral

Address	Read location	Write location
RemapBase	-	Pause
RemapBase + `0x10`	Identification	-
RemapBase + `0x20`	-	ClearResetMap
RemapBase + `0x30`	ResetStatus	ResetStatusSet
RemapBase + `0x34`	-	ResetStatusClear