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Cortex™-A8 Technical Reference Manual – ARM DDI 0344H **Errata 01**

This errata is applicable to the Cortex-A8 Technical Reference Manual issues A-H for product revisions r1p0-r3p0. It contains the following section:

1 CTI CoreSight defined registers

The *Cortex-A8 Technical Reference Manual* contains an incorrect description of the *Cross Trigger Interface* (CTI) Device ID Register. The CoreSight CTI, as described in the *CoreSight Components Technical Reference Manual*, uses bits [4:0] of this register to specify an implementation defined number of multiplexing levels on the trigger inputs and outputs. The Cortex-A8 processor implementation has no multiplexing on its trigger inputs or outputs, and therefore bits [4:0] must be zero.

The following section replaces section 15.8.2 in the *Cortex-A8 Technical Reference Manual*.

1.1 Device ID Register, 0xFC8

The Device ID Register reports the configuration of the CTI. For the Cortex-A8 processor, the CTI Device ID is `0x40900`. Table 15-28 shows how the bit values correspond with the Device ID Register functions.

Table 15-28 Device ID Register bit functions

Bits	Value	Function
[31:20]	`0x000`	Reserved, RAZ
[19:16]	`0x4`	Number of CTI channels available
[15:8]	`0x09`	Number of CTI triggers available
[7:5]	b000	Reserved, RAZ
[4:0]	b00000	Number of multiplexing levels on CTI inputs and outputs