ARM® LogicTile Express 20MG

V2F-1XV7

Technical Reference Manual

ARM®

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ARM LogicTile Express 20MG
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
12 October 2012	A	Non-Confidential	First release
31 March 2013	B	Non-Confidential	Second release
14 August 2013	C	Non-Confidential	Third release
26 May 2014	D	Non-Confidential	Fourth release

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

The LogicTile Express 20MG generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the card.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

Contents
ARM LogicTile Express 20MG Technical Reference Manual

Preface

This is the *Technical Reference Manual* (TRM) for the LogicTile Express 20MG daughterboard. It contains the following sections:

- *About this book* on page vii.
- *Feedback* on page x.

About this book

This book is for the LogicTile Express 20MG, V2F-1XV7, daughterboard.

Intended audience

This book is written for experienced hardware and software engineers who are developing ARM-based products using the daughterboard as part of a Versatile Express development platform.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the LogicTile Express 20MG daughterboard.

Appendix A *Signal Descriptions*

Read this for a description of the signals present at the external interface connectors of the daughterboard.

Appendix B *Specifications*

Read this for the electrical specifications of the daughterboard.

Appendix C *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

ARM Glossary, `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page viii.
- *Timing diagrams* on page viii.
- *Signals* on page ix.

Typographical conventions

The following table describes the typographical conventions:

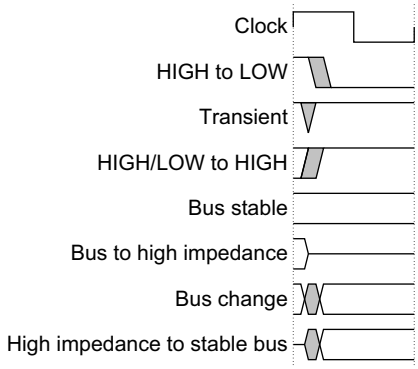
Typographical conventions

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are UNDEFINED, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals.
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

- *ARM Information Center*, http://infocenter.arm.com/help/index.jsp for access to ARM documentation.
- *ARM Technical Support Knowledge Articles*, http://infocenter.arm.com/help/topic/com.arm.doc.faqs/index.html for additional technical support.

ARM publications

This book contains information that is specific to this product. the following documents for other relevant information:

- *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4* (ARM DAI 0306)
- *ARM® Motherboard Express µATX (V2M-P1) Technical Reference Manual* (ARM DUI 0447).
- *ARM® Versatile™ Express Configuration Technical Reference Manual* (ARM DDI 0496).
- *ARM® CoreTile Express A5x2 Cortex™-A5 MPCore (V2P-CA5s) Technical Reference Manual* (ARM DUI 0541).
- *ARM® CoreTile Express A15x2 Cortex®-A15 MPCore Technical Reference Manual* (ARM DUI 0604).
- *ARM® CoreTile Express A9x4 Cortex™-A9 MPCore Technical Reference Manual* (ARM DUI 0448).
- *ARM® LogicTile Express 3MG (V2F-1XV5) Technical Reference Manual* (ARM DUI 0449).
- *ARM ®LogicTile Express 13MG Technical Reference Manual* (ARM DUI 0556).
- *ARM® Versatile™ Express Boot Monitor Reference Manual* (ARM DUI 0465).

Other publications

This section lists relevant documents published by third parties:

- the JEDEC Solid State Technology Association web site, www.jedec.org for information on *Small Outline Dual In-line Memory Modules* (SO-DIMMs).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, DDI 0498D.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter provides an introduction to the LogicTile Express 20MG, V2F-1XV7, daughterboard. It contains the following sections:

1.1 Precautions

This section contains advice about how to prevent damage to your daughterboard.

1.1.1 Ensuring safety

The daughterboard is powered from 12V DC through a 6 pin PCIe connector, J6. 5VDC and a *Variable IO* (VIO) voltage is supplied to the board through header connector HDRYL, J5, on the lower side of the board.

Warning

Do not use the daughterboard near equipment that is sensitive to electromagnetic emissions, for example, medical equipment.

1.1.2 Preventing damage

The daughterboard is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure that leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the board, observe the following precautions:

- You must connect the PCIe power cable to the daughterboard before powerup to prevent damage.
- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Ensure that the voltage on the pins of the FPGA and interface circuitry on the daughterboard is at the correct level. Some of the daughterboard FPGA signals are connected directly to the Versatile Express µATX Motherboard.
- You must not configure FPGA pins connected to an external signal source as outputs.
- Do not use the board near a transmitter of electromagnetic emissions.

1.2 About the LogicTile Express 20MG daughterboard

The daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA®) that use the *Advanced eXtensible Interface* (AXI™) or custom logic for use with ARM cores or clusters.

Note

The daughterboard is designed to be used with a Versatile Express µATX Motherboard.

The daughterboard contains the following devices:

- One Xilinx Virtex-7 FPGA, XC7V2000T-1:
  - Speed grade -1.
- NAND Flash memory for high speed FPGA programming and configuration.
- Daughterboard Configuration Controller to configure the FPGA.
- 4GB of DDR3 64-bit memory using a *Small Outline Dual In-line Memory Module* (SO-DIMM).
- HDRXL header on the bottom side of the board with two *High-Speed Buses* (HSBs), one master, one slave, that connect to the other daughterboard site.
- HDRYL header on the bottom side of the board with five buses to the motherboard.
- HDRXU and HDRYU headers on the top side of the board for expansion:
  - The HDRYU header is only partly populated. the `an306_revb.xdc` file in the `docs` directory of the DVD supplied with the V2F-1XV7 daughterboard.
- Two *Serial Advanced Technology Attachment* (SATA) Host, H, and two SATA Device, D, connectors.
- JTAG and Trace debug interfaces.
- Eight green user LEDs, S0-S7, connected to the Daughterboard Configuration Controller.
- One green user LED, FPGA_LED, connected to the FPGA.
- One green FPGA DONE_LED.
- One green 3V3 power supply LED.
- One red OverTemp LED.
- Eight red FPGA power supply fault LEDs.
- Eight general-purpose *Dual In-line Package* (DIP) switches.

You must supply external 12V to the board through the 6-pin PCIE connector. The power supply must be able to supply 6.25A.

The V2F-1XV7 daughterboard supports board stacking. *Clock domains* on page 2-16. Each board in a stacked system must have its own external 12V supply.

Figure 1-1 on page 1-4 and Figure 1-2 on page 1-5 show the physical layout of the daughterboard.

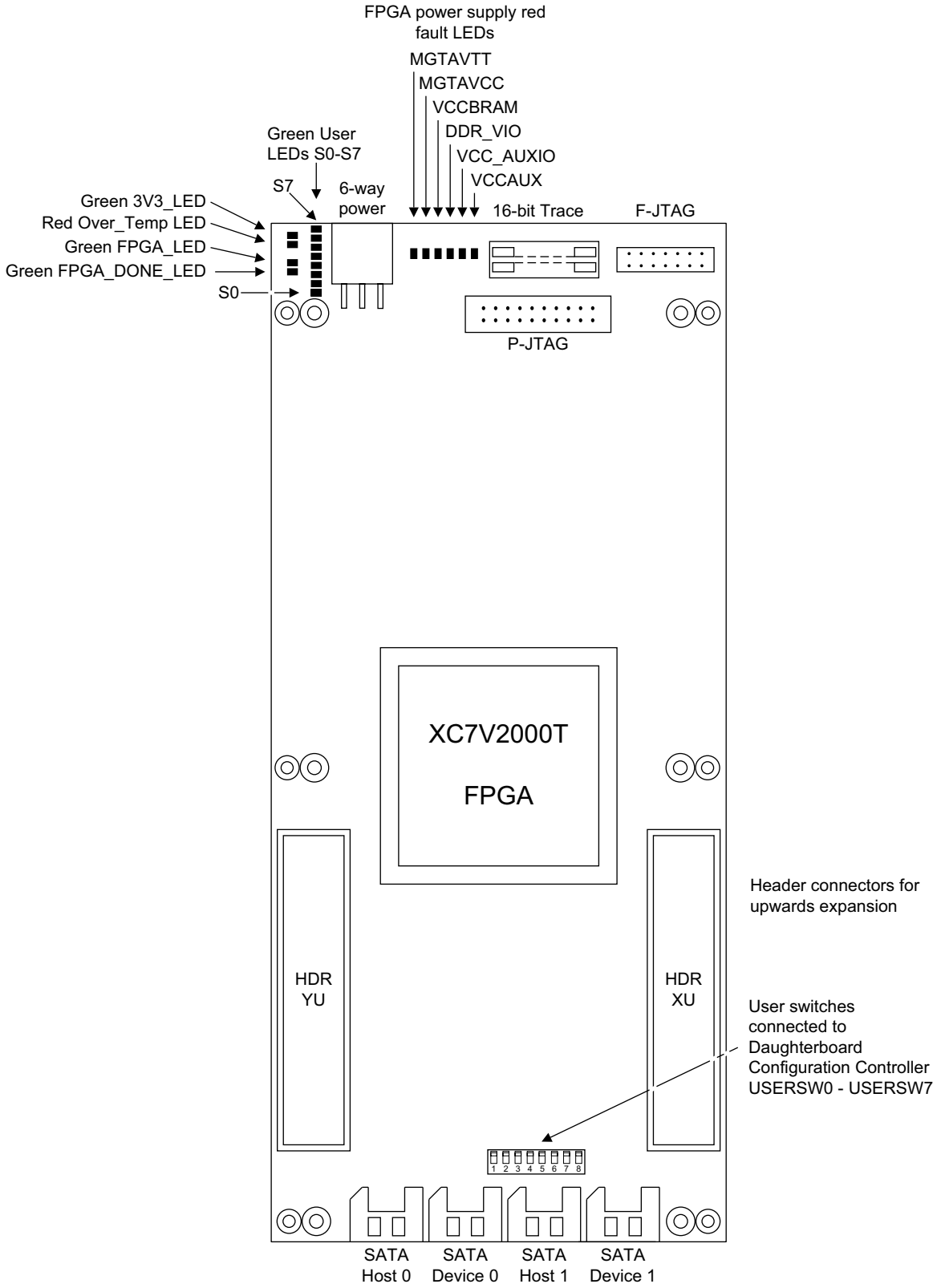


Figure 1-1 Daughterboard layout, upper side

Note

When the daughterboard is fitted to the motherboard, the upper side of the board faces away from the motherboard.

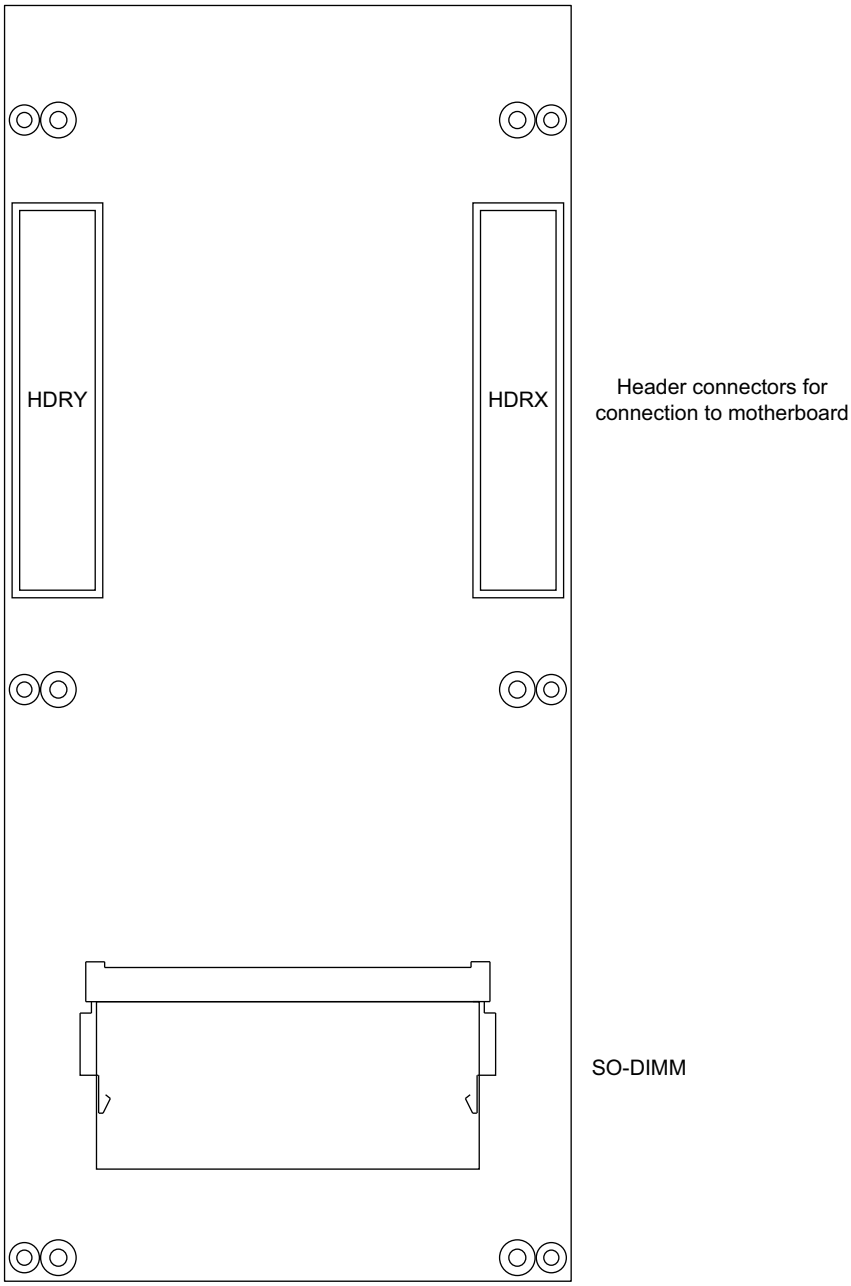


Figure 1-2 Daughterboard layout, lower

Note

The lower side of the daughterboard is the side that connects to the motherboard.

Chapter 2
Hardware Description

This chapter describes the LogicTile Express 20MG, V2F-1XV7, daughterboard hardware. It contains the following sections:

2.1 Overview of the daughterboard hardware

The hardware infrastructure supports system expansion and a number of debug interfaces. Figure 2-1 shows the high-level hardware infrastructure. For information on the connector signals to these additional interfaces, see Appendix A *Signal Descriptions*.

Note

The configuration image loaded into the FPGA at power-up defines the functionality of the daughterboard. *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, provided by ARM, implements an example AMBA 3.0 system using the daughterboard.

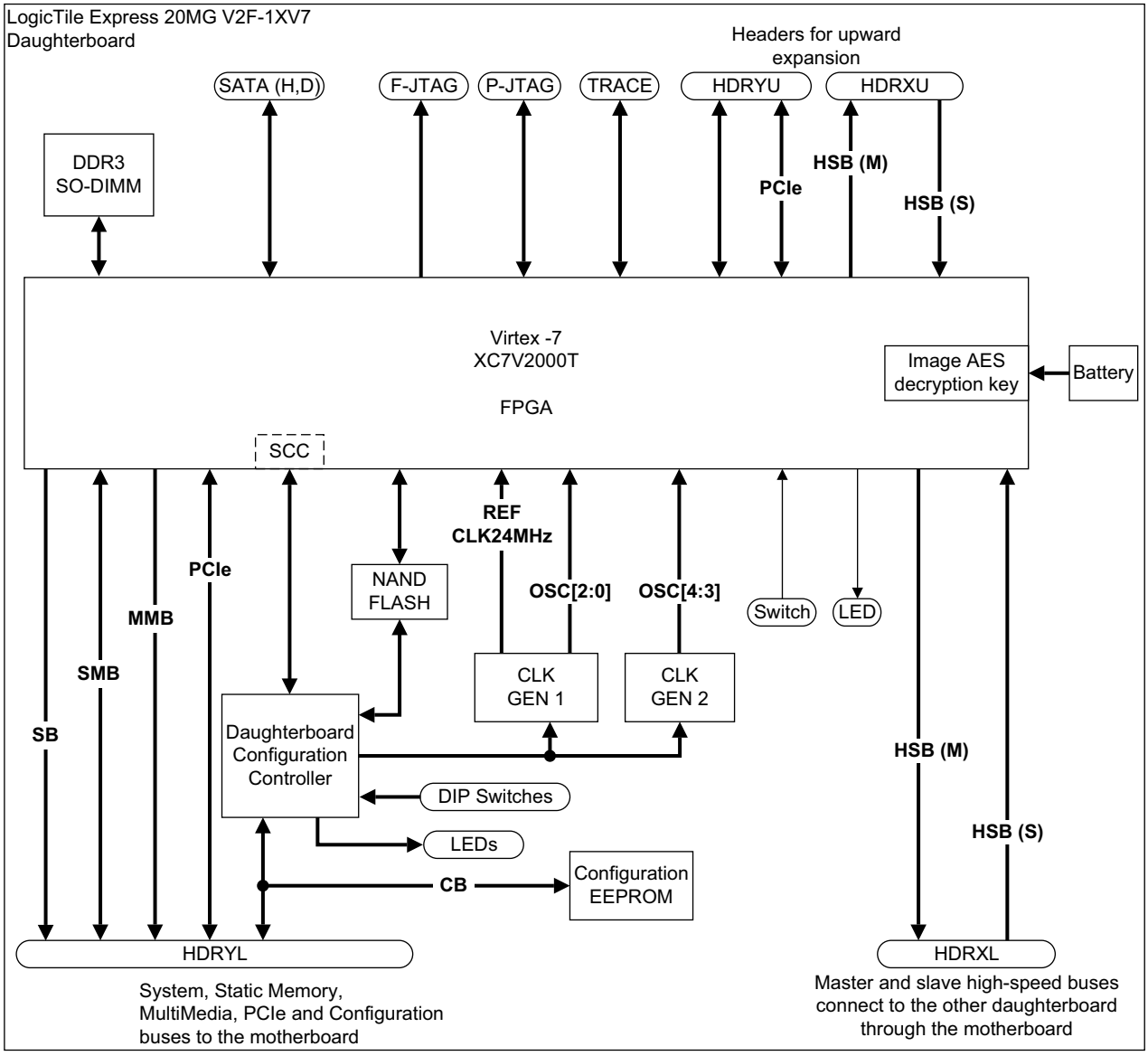


Figure 2-1 Hardware infrastructure

The hardware infrastructure of the daughterboard comprises:

- One Xilinx Virtex-7 FPGA:
  - XC7V2000T-1 FPGA
  - 20 million gates.
  - Speed grade -1.
  - Gigabit transceiver connection to SATA connectors and to HDRYL and HDRYU headers.
- One NAND Flash memory, used to store FPGA images.
- A configuration EEPROM to store the board *Hardware Board International* (HBI) number and names of the current FPGA images.
- One local Daughterboard Configuration Controller whose purpose is to:
  - Set the oscillator frequencies.
  - Set and monitor the power supply voltages.
  - Load the FPGA image.
  - Transfer SCC register values.
- SO-DIMM memory connector:
  - 4GB of external DDR3 RAM fitted in the SO-DIMM connector that the FPGA drives.
- One header connector, HDRXL, on the bottom side of the board for routing *High-Speed Buses* (HSBs) from the FPGA to the other daughterboard site on the motherboard:
  - One HSB Master, M, interface implemented on the FPGA.
  - One HSB Slave, S, interface implemented on the FPGA.
  - *Low Voltage Differential Signaling* (LVDS) support, 160 pairs.
  - 20 single-ended signals.
- One header connector, HDRYL, for routing buses to the motherboard:
  - *MultiMedia Bus* (MMB).
  - *PCI-Express Bus* (PCIe).
  - *System Bus* (SB).
  - *Static Memory Bus* (SMB).
  - *Configuration Bus* (CB).
  - Gigabit transceiver connection.
- Two header connectors, HDRXU and HDRYU, on the top side of the board to support upward expansion. The HDRYU header is only partly populated. See the `an306_revb.xdc` file in the `docs` directory of the DVD supplied with the V2F-1XV7 daughterboard:
  - 320 single-ended IO pins that you can configure as up to 160 pairs, LVDS, and 20 single-ended only IO pins available on the FPGA that connect to HDRXU.
  - 100 general, single-ended, IO pins available on the FPGA that connect to HDRYU.
- *Serial Advanced Technology Attachment* (SATA) connectors:
  - Two Host, H, connector.
  - Two Device, D, connector.
  - Each connector has one transmit lane and one receive lane.

- PCI-Express Bus (PCIe):
  - Configurable PCIe capability with a maximum capacity of 4 lanes upwards and 4 lanes downwards. See *PCI Express Bus (PCIe)* on page 2-8.
- Debug interfaces:
  - P-JTAG port for DSTREAM™ or other compatible third-party debuggers.
  - *Integrated Logic Analyzer* (ILA) F-JTAG port for *ChipScope*, for example.
  - One trace port supporting 16-bit trace.
- Eight green general-purpose user LEDs, S0-S7, connected to the Daughterboard Configuration Controller.
- One green user LED, FPGA_LED, connected to the FPGA.
- One green FPGA DONE_LED, connected to the Daughterboard Configuration Controller.
  - Indicates *FPGA configured*.
- One green power 3V3 power supply LED, 3V3_LED:
  - Indicates *onboard 3V3 power supply operating inside its specified limits*.
- One red OverTemp LED, connected to the Daughterboard Configuration Controller:
  - Indicates *FPGA over temperature*.
  - This LED flashes briefly at daughterboard powerup.
- Eight red FPGA power supply fault LEDs:
  - Each LED indicates *FPGA power supply operating outside its specified limits*.
  - These LEDs flash briefly at daughterboard powerup.
- Eight general-purpose *Dual In-Line Package* (DIP) switches connected to the Daughterboard Configuration Controller.
- One user switch connected to the FPGA.
- A battery to provide power to the FPGA to store the FPGA image AES decryption key.
- Five on-board programmable oscillators, all input to the FPGA.

For more information see *System interconnect* on page 2-5.

2.2 System interconnect

Figure 2-2 shows a typical system interconnect.

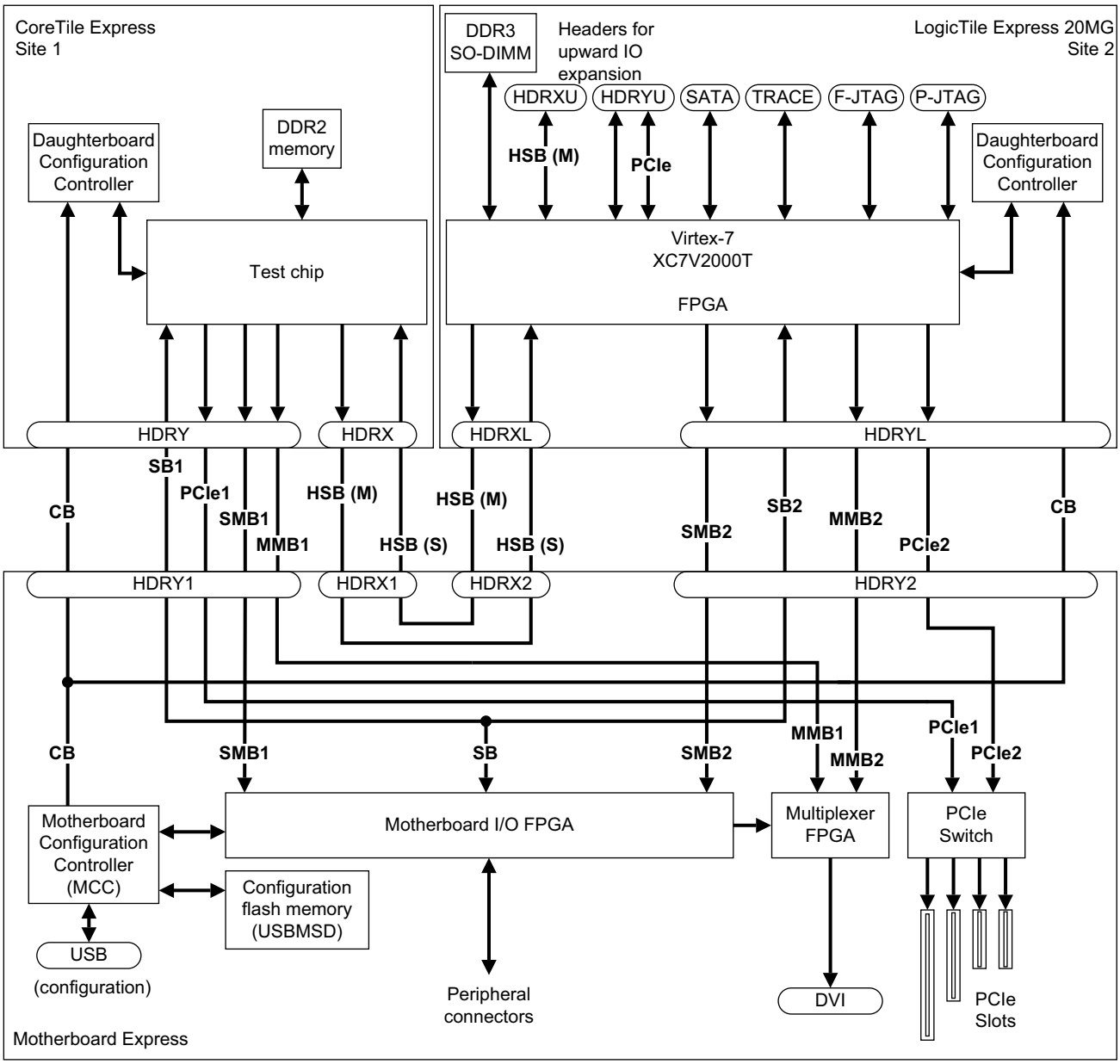


Figure 2-2 System interconnect

The signals on the daughterboard are routed to the motherboard over two header connectors, HDRXL and HDRYL, on the lower side of the board. See Figure 1-2 on page 1-5.

The HDRXU and HDRYU header connectors on the upper side of the board support stacking of three V2F-1XV7 daughterboards. See *Global clocks* on page 2-17.

For more information on the motherboard signals, see Chapter 2 *Hardware Description* of the *ARM® Motherboard Express µATX (V2M-P1) Technical Reference Manual* and the media supplied with the LogicTile Express 20MG, V2F-1XV7, daughterboard.

Note

The V2M-P1 motherboard can support a *root complex* either on the daughterboard in Site 1 or on the daughterboard in Site 2. You select which site contains the *root complex* by editing the `config.txt` file.

Note

ARM recommends that you fit LogicTile Express daughterboards, including the LogicTile Express 20MG, V2F-1XV7, daughterboard, on site 2, and that you fit CoreTile Express daughterboards on site 1.

2.2.1 FPGA bus widths

Figure 2-3 shows the number of signals available to implement the FPGA buses.

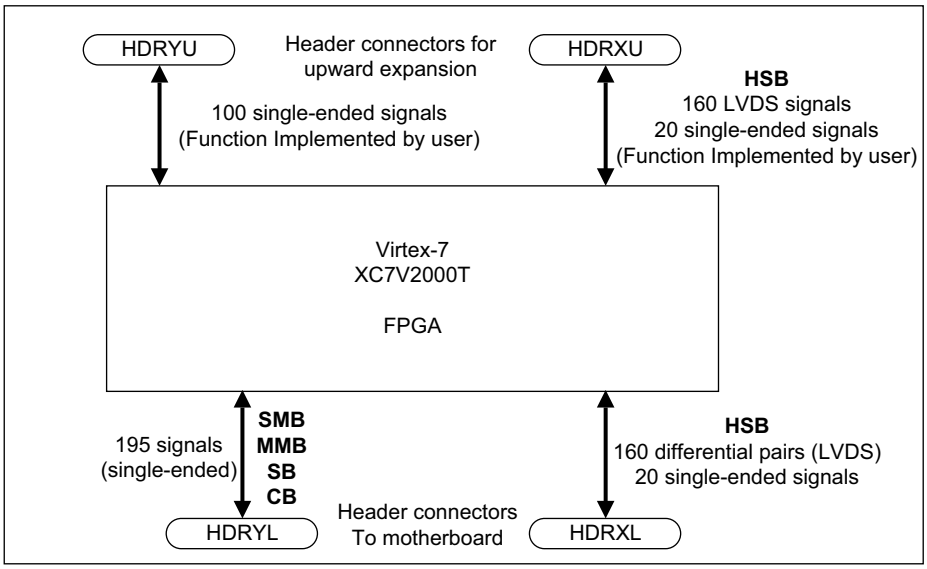


Figure 2-3 Available FPGA Bus widths

Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4 implements the following buses:

- HSB link to the other daughterboard site on the motherboard. See the `an306_revb.xdc` constraints file in application note AN306 for a listing of the 160 LVDS pairs, XP-XN, and the 20 single-ended signals available between the FPGA and header HDRXL.
- The *Static Memory Bus*.
- The *MultiMedia Bus*.
- The *System Bus*.
- The *Configuration Bus*.

Application note AN306 does not implement the following buses:

- HSB link upwards to the expansion board. You can implement this yourself by using the 160 LVDS pairs, XP_UP/XN_UP, and 20 single-ended signals available between the FPGA and header HDRXU. See the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for a listing of these signals.
- Other buses upwards to an expansion board. You can implement these buses yourself by using the 100 single-ended signals available between the FPGA and header HDRYU. See the `an306_revb.xdc` constraints file, available in *Application Note 306* for a listing of these signals.

2.2.2 High-Speed Buses to other daughterboard

The HDRXL header connects one Master, M, and one Slave, S, HSB, one full duplex bus lane, from the FPGA to the other daughterboard through dedicated headers on the motherboard. The most common use of this bus lane is to implement multiplexed AXI master and slave interfaces between the daughterboards.

Note

Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4 provides an example AXI design implementing external multiplexed AXI master and slave buses at the HDRXL header. See *FPGA bus widths* on page 2-6.

2.2.3 Buses for upward expansion

The daughterboard can support bus links from the FPGA through upper headers HDRXU and HDRYU to another LogicTile Express 20MG daughterboard or user IO expansion board.

340 single-ended IO signals are available between the FPGA and upper header HDRXU. You can configure up to 320 of these signals as 160 LVDS pairs. You can only use the other 20 signals as single-ended IO. You can use these signals to implement an HSB bus, for example AXI, to the upper LogicTile 20MG daughterboard or user IO expansion board.

100 single-ended signals are available between the FPGA and upper header HDRYU. You can use these signals to implement other buses to the upper LogicTile 20MG daughterboard or user IO expansion board.

Note

- Application note AN306 does not implement these links but you can implement them yourself using the 160 LVDS pairs and 20 IO signals available between the FPGA and header HDRXU and the 100 single-ended signals available between the FPGA and header HDRYU. See *FPGA bus widths* on page 2-6.
- If you stack the LogicTile daughterboard an external 12V, 6.25A ATX power supply is required for each daughterboard.
- ARM does not support stacking of LogicTile Express 3MG, V2F-1XV5, or LogicTile Express 13MG, V2F-2XV6, daughterboards on the LogicTile Express 20MG, V2F-1XV7, daughterboard.
- ARM recommends a maximum stack of three LogicTile Express 20MG on each motherboard site, to enable the use of a common synchronous clock. See *Global clocks* on page 2-17.

2.2.4 *Static Memory Bus* (SMB)

The daughterboard uses the Static Memory Bus (SMB) for peripheral and memory accesses to the motherboard. This is the minimum bus implementation required to enable the daughterboards to boot and run applications.

2.2.5 *MultiMedia Bus* (MMB)

The optional *MultiMedia Bus* (MMB) is implemented to enable the daughterboard to drive audio and video data. The MMB consists of a video bus and I2S and S/PDIF audio buses. This enables the daughterboard to drive up to 1080p or UXGA video and audio formats from stereo to 8-channel surround sound.

2.2.6 *System Bus* (SB)

The *System Bus* (SB) carries interrupt and DMA signals between the daughterboards and motherboard.

2.2.7 *Configuration Bus* (CB)

This connects the Daughterboard Configuration Controller to the motherboard MCC. The *Configuration Bus* (CB) is used to control the power and reset sequence of the daughterboard and to load or update the image in the FPGA. The CB also enables SCC register transfers at power-up and during run time. See *FPGA configuration and initialization* on page 2-12.

2.2.8 *PCI Express Bus* (PCIe)

The daughterboard can implement a *root complex* to connect,through the motherboard PCIe switch, to the PCI Express Gen1 Card slots on the motherboard. The daughterboard supports a maximum of four lanes downwards to header HDRYL.

The daughterboard can implement an *endpoint* which supports a maximum of four lanes upwards to header HDRYU.

Figure 2-4 on page 2-9 shows the PCI-Express signals to the headers. Table 2-1 on page 2-9 shows the connectivity between the *Gigabit Transceiver* (GTX) locations in the FPGA and the PCI Express lanes.

Note

Xilinx supplies the PCIe *endpoint* and the PCIe root port in the Virtex-7 FPGA as a hardblock. You can implement it using the Xilinx tool flow. You can implement a PCIe *root complex* using a third-party IP softblock.

Note

The V2M-P1 motherboard can support a *root complex* either on the daughterboard in Site 1 or on the daughterboard in Site 2, but not both. You select which site contains the *root complex* by editing the `config.txt` file. By default, the daughterboard in Site 1 is the *root complex*.

The V2M-P1 motherboard tile sites do not support *endpoints* in the daughterboards connected to the switch.

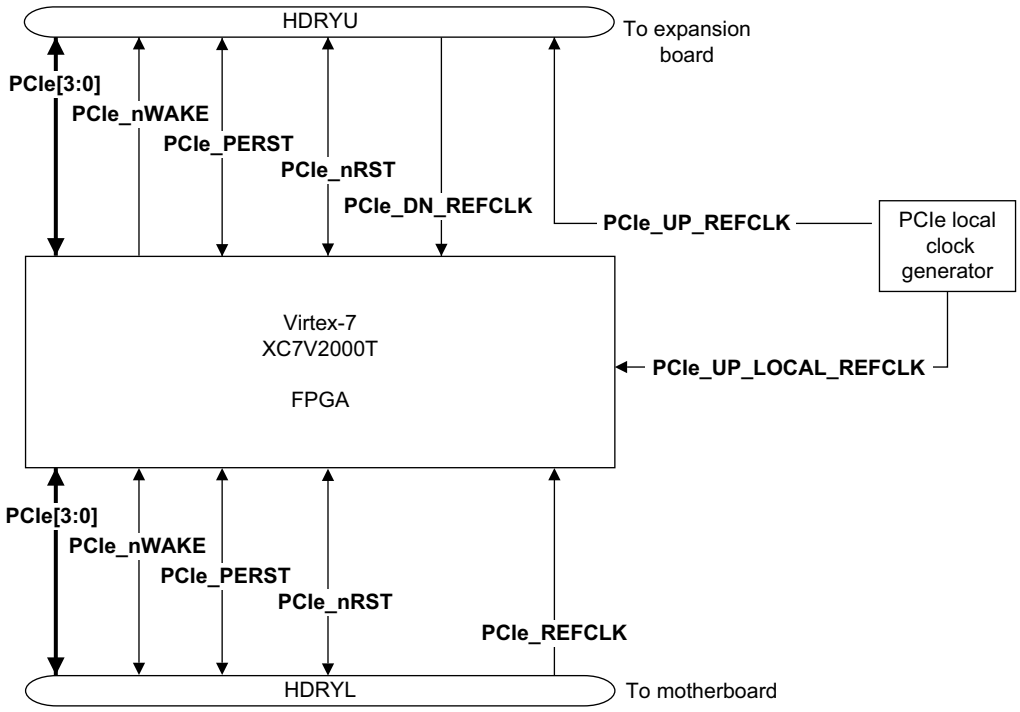


Figure 2-4 PCI express bus connections

Caution

You can configure the **PCIe_nWAKE**, **PCIe_PERST**, and **PCIe_nRST** sideband signals as either inputs or outputs. If you configure them as outputs, you must set them to be open-collector.

Note

- When the daughterboard is fitted to site 1 of the motherboard, HDRYU is on the upper side of the board facing away from the motherboard and HDRYL is on the lower side of the board facing towards the motherboard.
- The **PCIe_UP_REFCLK** and **PCIe_UP_LOCAL_REFCLK** clocks are synchronous.

Table 2-1 shows the connectivity between the GTX locations in the FPGA and the PCI-Express lanes for the upper header.

Table 2-1 Upper header PCI-Express Lanes. FPGA -GTX connectivity

PCIe lane	GTX location
PCIE_DN_REFCLK MGTREFCLK1_113	X0Y2
PCIE_UP_LOCAL_REFCLK MGTREFCLK0_113	X0Y2
Lane 0	X0Y11

Table 2-1 Upper header PCI-Express Lanes. FPGA -GTX connectivity (continued)

PCIe lane	GTX location
Lane 1	X0Y10
Lane 2	X0Y9
Lane 3	X0Y8

Table 2-2 shows the connectivity between the GTX locations in the FPGA and the PCI-Express lanes for the lower header.

Table 2-2 Lower header PCI-Express Lanes. FPGA -GTX connectivity

PCIe lane	GTX location
Lane 0	X0Y19
Lane 1	X0Y18
Lane 2	X0Y17
Lane 3	X0Y16
PCIE_REFCLK MGTREFCLK0_115	X0Y4

2.2.9 DDR3 memory interface (SO-DIMM)

The SO-DIMM connector supports up to 4GB of 64-bit DDR3 memory expansion. Figure 2-5 shows the generic FPGA to DDR3 memory interconnect.

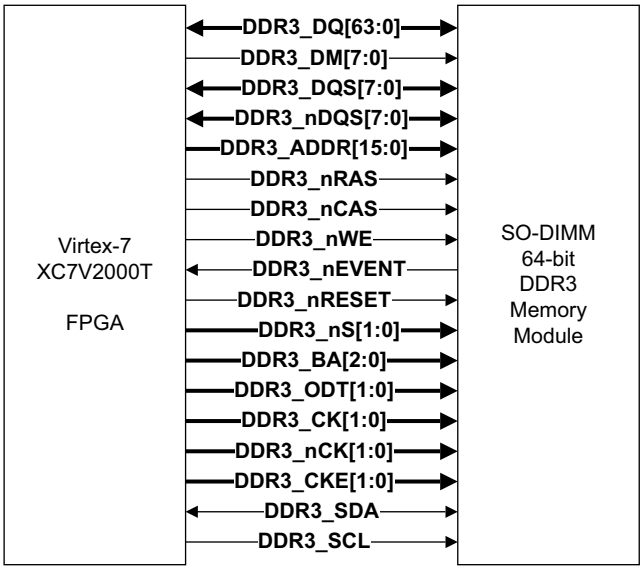


Figure 2-5 DDR3 memory interface

2.2.10 FPGA configuration Flash memory interface

The V2F-1XV7 daughterboard contains one NAND Flash memory. The Flash memory stores one FPGA image. The Daughterboard Configuration Controller loads data into the Flash memory and initializes the data transfer from the Flash memory to the FPGA.

2.2.11 SATA connectors

Eight SATA lanes, four transmit and four receive, from the FPGA connect to four SATA connectors. See *SATA connector, J13, J14, J15, and J16* on page A-7.

ARM does not provide an example SATA controller.

2.3 FPGA configuration and initialization

Configuration is performed during power-up or reset by the *Motherboard Configuration Controller* (MCC) on the motherboard, and the Daughterboard Configuration Controllers with its associated NAND Flash memory.

The Daughterboard Configuration Controllers and the NAND Flash memory configure the Virtex-7 XC7V2000T FPGA. The Daughterboard Configuration Controllers also sets all the daughterboard oscillator frequencies and FPGA SCC registers using information from the motherboard microSD card, that is a *Universal Serial Bus Mass Storage Device* (USBMSD) card.

See the *ARM® Versatile™ Express Configuration Technical Reference Manual* and *ARM® Motherboard Express µATX (V2M-P1) Technical Reference Manual* or *ARM® Programmer Module (V2M-CP1) Technical Reference Manual* for information on how to configure the V2F-1XV7 daughterboard using the configuration files on the motherboard.

The V2F-1XV7 provides a DONE_LED for the FPGA to indicate when configuration is complete.

Caution

ARM recommends that you use the configuration files for all system configuration. *SCC register descriptions* on page 3-5, however, describes registers that directly modify the FPGA configuration.

Note

When external power is not present, a battery supplies power to part of the FPGA that is used to store an AES decryption key. This key is used to enable loading of encrypted images.

2.4 Voltage, temperature, oscillator, and SCC register monitoring

The Daughterboard Configuration Controller on the daughterboard transmits voltage and temperature measurements and information about the oscillators and SCC registers supported in the two FPGA designs. The Daughterboard Configuration Controllers transmits the information to the motherboard where it can be read from the SYS_CFGCTRL interface.

See the *ARM® Motherboard Express µATX (V2M-P1) Technical Reference Manual* for more information on the SYS_CFGCTRL registers.

2.4.1 Information transmitted by Daughterboard Configuration Controller to the motherboard

The Daughterboard Configuration Controller transmits voltage measurements, information about the daughterboard oscillators, temperature measurements of the FPGA and information about the SCC registers supported in the FPGA design.

Table 2-3 shows the device numbers for the voltage supplies.

Table 2-3 Device numbers for the voltage supplies

Device	Voltage supply	Default voltage	Description
0	VIO_UP	0.8 +/- 5%	VIO to expansion board above. You can set VIO_UP to any of the voltages shown.
		1.0 +/- 5%	
		1.2 +/- 5%	
		1.5 +/- 5%	
		1.8 +/- 5%	
1	12	12 +/- 5%	12V from power connector J6.

Table 2-4 shows the device numbers for the daughterboard oscillators.

Table 2-4 Device numbers for oscillator frequencies

Device	Oscillator	Description
0	OSC0	These oscillators connect to the Virtex-7 XC7V2000T FPGA.
1	OSC1	
2	OSC2	
3	OSC3	
4	OSC4	

Table 2-5 shows the device numbers for the FPGA temperature measurements.

Table 2-5 Device numbers for FPGA temperature measurements

Device	Description
0	Virtex-7 XC7V2000T FPGA temperature in degrees C, max 80°C

Table 2-6 shows the device numbers for the SCC registers supported in the FPGA 1, 550T, design.

Table 2-6 Device numbers for the SCC registers supported in the Virtex-7 FPGA design

Device	Virtex-7 XC7V2000T FPGA SCC Registers	Description
0x000 to 0xFFC	SCC0 to SCC1023	32-bit RW registers, if supported by design.

2.4.2 Daughterboard shutdown because of excessive temperature

Both FPGAs have an associated red LED that signifies excessive FPGA temperature, D20 for FPGA 1, and D21 for FPGA 2. See Figure 1-1 on page 1-4 for the location of these LEDs on the daughterboard. Each LED illuminates when the internal FPGA temperature exceeds approximately 70°C.

If the internal temperature of the FPGA exceeds 80°C, the MCC powers down the daughterboard to prevent damage.

2.5 Clocks

This section describes the V2F-1XV7 daughterboard clocks. It contains the following subsections:

- *Overview of clocks*.
- *Clock domains* on page 2-16.
- *Global clocks* on page 2-17.

2.5.1 Overview of clocks

Clock generators on the daughterboard, and inside the FPGA, generate the majority of the clocks that the daughterboard uses. Figure 2-6 on page 2-16 shows the clock domains of the daughterboard.

The MCC transfers clock settings to the Daughterboard Configuration Controller during power-up sequencing using values that the daughterboard configuration files define. The Daughterboard Configuration Controller then configures the programmable clock generators.

The daughterboard has four on-board clock generators. You configure the frequencies of clock generators 1, 2 and 4 by editing the *OSCCLKS* section of configuration file `an306r0p0.txt`. See *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4* for an example `an306r0p0.txt` file.

Table 2-7 shows the daughterboard clocks.

Table 2-7 Daughterboard clocks

Daughterboard clocks	Source	Frequency range	Comment
OSC[2:0]	CLK GEN 1	2MHz-230MHz 1% resolution	Variables OSC0, OSC1, and OSC2 in file `an306r0p0.txt` configure these daughterboard clocks
OSC[4:3]	CLK GEN 2	2MHz-230MHz 1% resolution	Variables OSC3, and OSC4 in file `an306r0p0.txt` configure these daughterboard clocks
OSC[5]	-	-	`an306r0p0.txt` contains variable OSC5 but the daughterboard does not use this clock
SATACLK0	CLK GEN 3	Fixed 150MHz	-
SATACLK1	CLK GEN 4	Fixed 100MHz	-
PCIE_UP_REFCLK(P|N)			-
PCIE_UP_LOCAL_REFCLK(P|N)			-
DDR3REFCLK		See `an306r0p0.txt` for a list of available frequencies.	Variables OSC6 in file `an306r0p0.txt` configures this daughterboard clock

See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for information on how to edit daughterboard configuration files.

You can read and write to the daughterboard while the system is running using the motherboard SYS_CFG register interface.

See Figure 2-6.

2.5.2 Clock domains

Figure 2-6 shows the clock domains of the daughterboard.

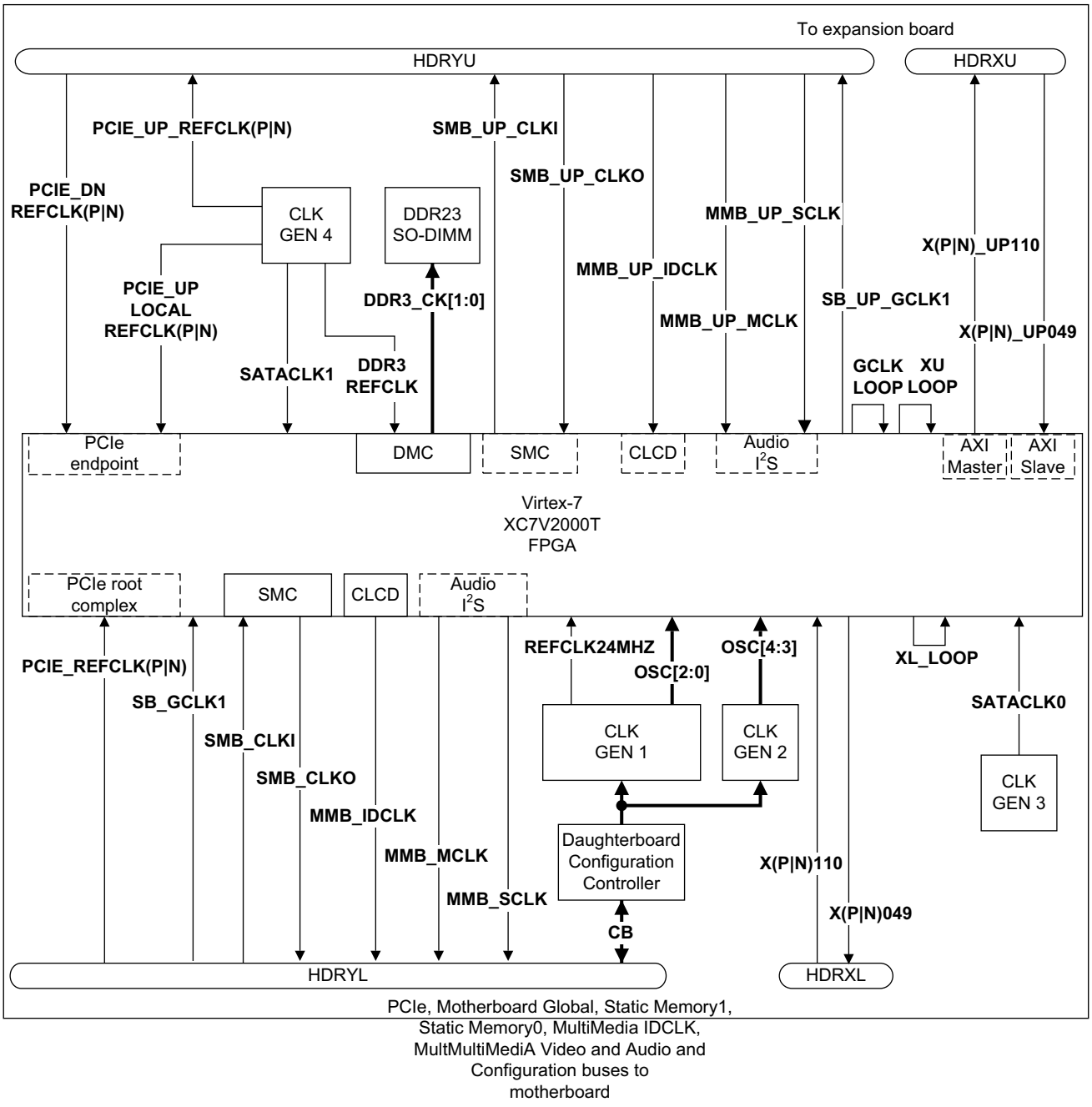


Figure 2-6 FPGA clock domains

The GCLK_LOOP, XU_LOOP, and XL_LOOP clock loops enable you to use phase-shifted clocks internally in your design while transmitting the non phase-shifted clock externally. *Application Note Example LogicTile Express 20MG Design for a CoreTile Express A9x4* contains an example use of phase-shifted clocks.

Note

Figure 2-6 on page 2-16 shows the clocks available to implement the functions shown as blocks inside the FPGA. See the `an306_revb.xdc` constraints files, supplied in application note *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*. The application note implements the functions shown as solid blocks and does not supply the functions shown as dashed blocks.

2.5.3 Global clocks

The **SB_GCLK1** and **SMB_CLKO** clocks, that connect to header HDRYL, and the **SB_UP_GCLK1** and **SMB_UP_CLK0** clocks, that connect to header HDRYU, are delay-matched global clocks. They connect between daughterboards in a stacked daughterboard system, and remain synchronous when received by FPGAs on the receiving daughterboards.

Figure 2-7 shows the global clocks on the V2F-1XV7 daughterboard.

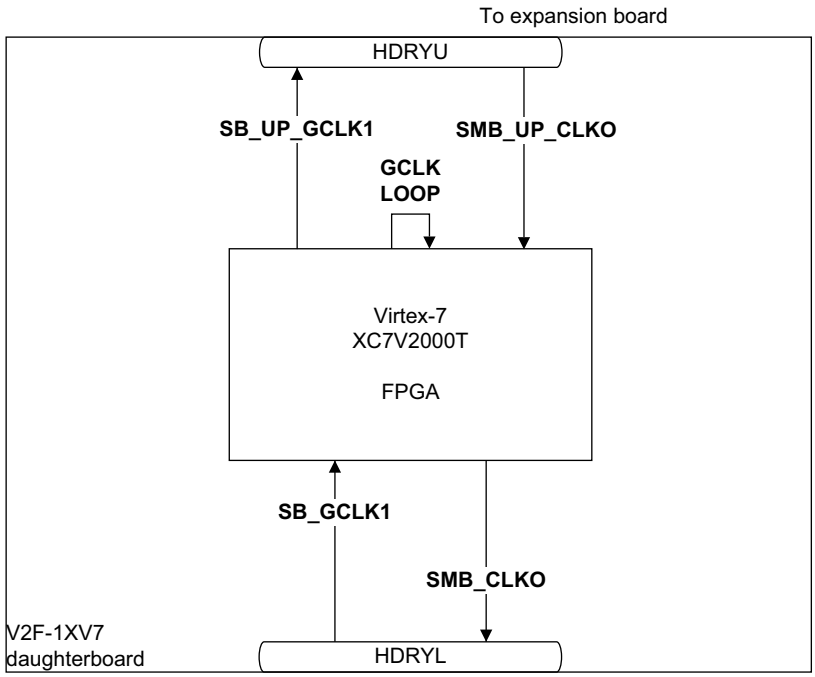


Figure 2-7 V2F-1XV7 daughterboard global clocks

Delay-matching to enable vertical stacking of daughterboards

The track lengths of global clocks on the V2F-1XV7 daughterboard are delay-matched to length L. The track lengths of the **GCLK_LOOP** clock loop is matched to length 2L. This enables two LogicTile Express 20MG, V2F-1XV7, daughterboards that are fitted on site 1 and site 2 of the motherboard to receive the **MB_GCLK1** synchronous motherboard global clock.

Delay-matching enables vertical stacking of V2F-1XV7 daughterboards or custom design daughterboards that also have clock track matching of length L. This enables the **GCLK_UP1** and **SMB_CLK0** clocks to propagate up and down the stack synchronously. See Figure 2-8 on page 2-18.

Distribution of global clocks to stacked daughterboards

Figure 2-8 shows the recommended clocking scheme to distribute the global clocks to two stacked daughterboards.

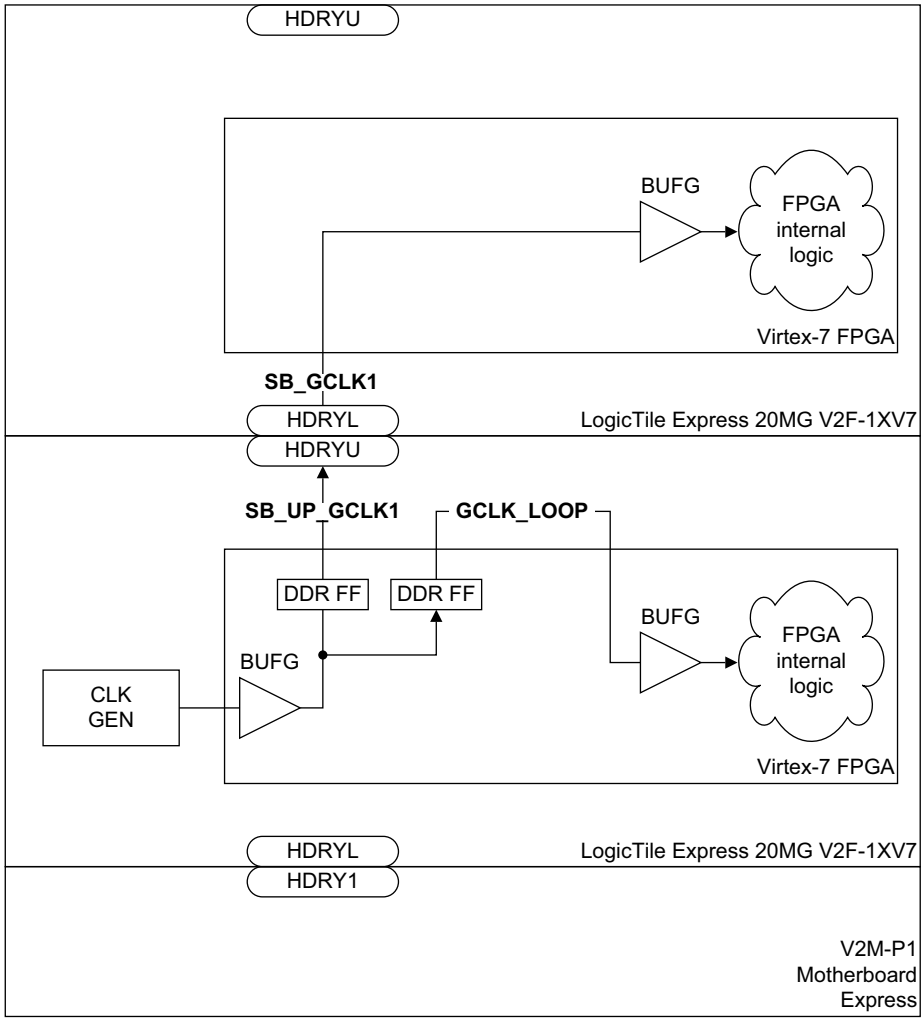


Figure 2-8 Distribution of global clocks to two stacked daughterboards

Figure 2-9 on page 2-19 shows the recommended clocking scheme to distribute the global clocks to three stacked daughterboards.

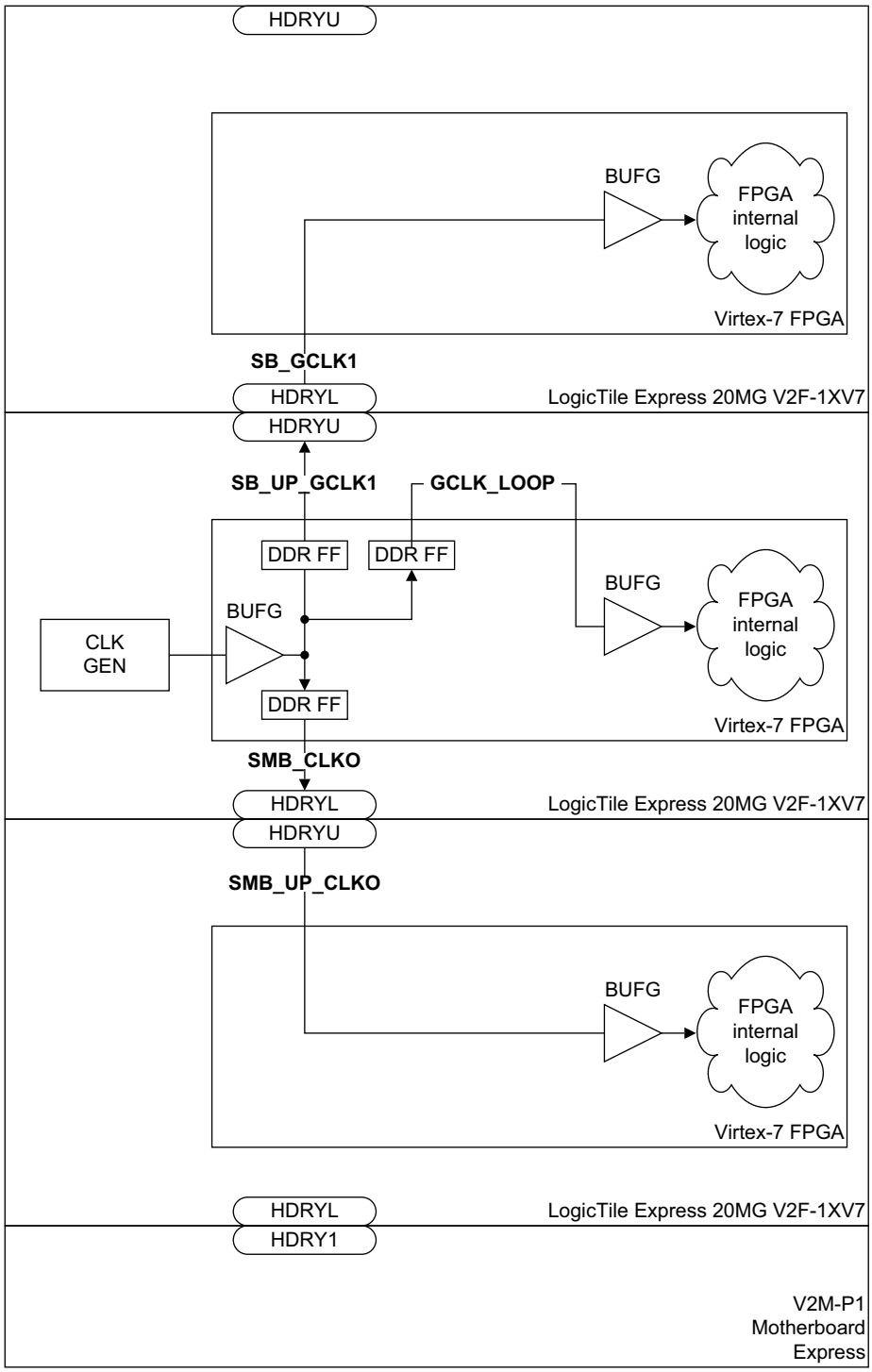


Figure 2-9 Distribution of global clocks to three stacked daughterboards

Note

- ARM recommends a maximum stack of three LogicTile Express 20MG on each motherboard site.

- DDR FF are logic cells, and BUFG are buffers provided by Xilinx within the Virtex-7 FPGAs. This clocking scheme uses them to propagate the clocks with identical delays. See the *Virtex-7 FPGA SelectIO Resources User Guide* at the Xilinx web site, http://www.xilinx.com for more information.

2.6 Resets

The MCC on the motherboard controls the daughterboard reset signals. Figure 2-10 shows the reset request signals from the daughterboard, and the reset signals from the motherboard.

Reset requests from the daughterboard can originate in the FPGA or from the P-JTAG connector. A reset request from the P-JTAG connector connects to **CB_RSTREQ** through the FPGA and the Daughterboard Configuration Controller. A reset request from the FPGA connects to **CB_RSTREQ** through the Daughterboard Configuration Controller.

The reset request from the daughterboard results in the motherboard asserting **CB_nRST**. **CB_nPOR** can optionally be asserted by the setting **ASSERTNPOR**, that can be TRUE or FALSE in the `config.txt` motherboard configuration file. See the *ARM® Versatile™ Express Configuration Technical Reference Manual* for an example `config.txt` file.

Note

Only the **CB_nPOR** and **CB_nRST** signals are driven to the daughterboard FPGA and Daughterboard Configuration Controller. **CB_RSTREQ** can be driven from the FPGA through the Daughterboard Configuration Controller to request a cold or warm reset, depending on the motherboard configuration file settings.

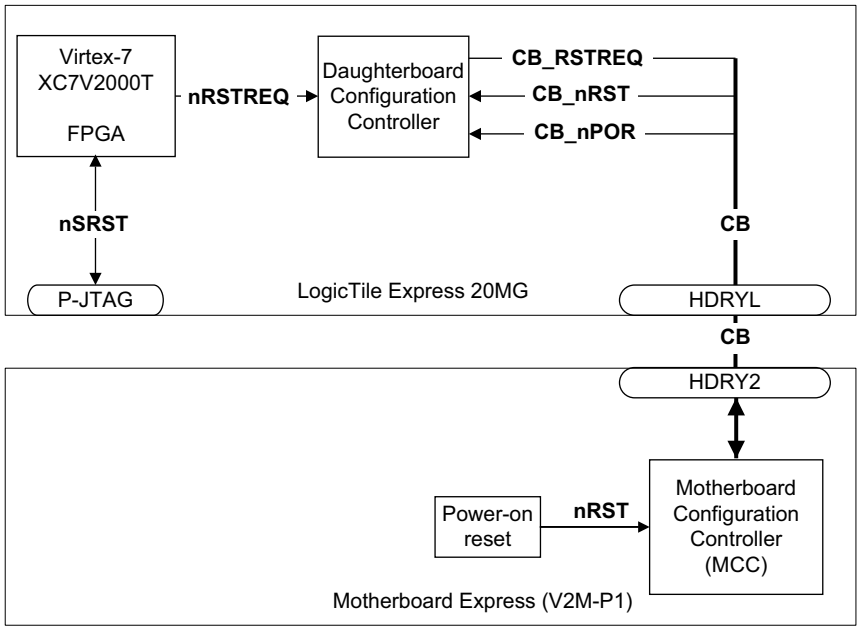


Figure 2-10 Daughterboard resets

Figure 2-11 on page 2-22 shows the basic power-up reset cycle.

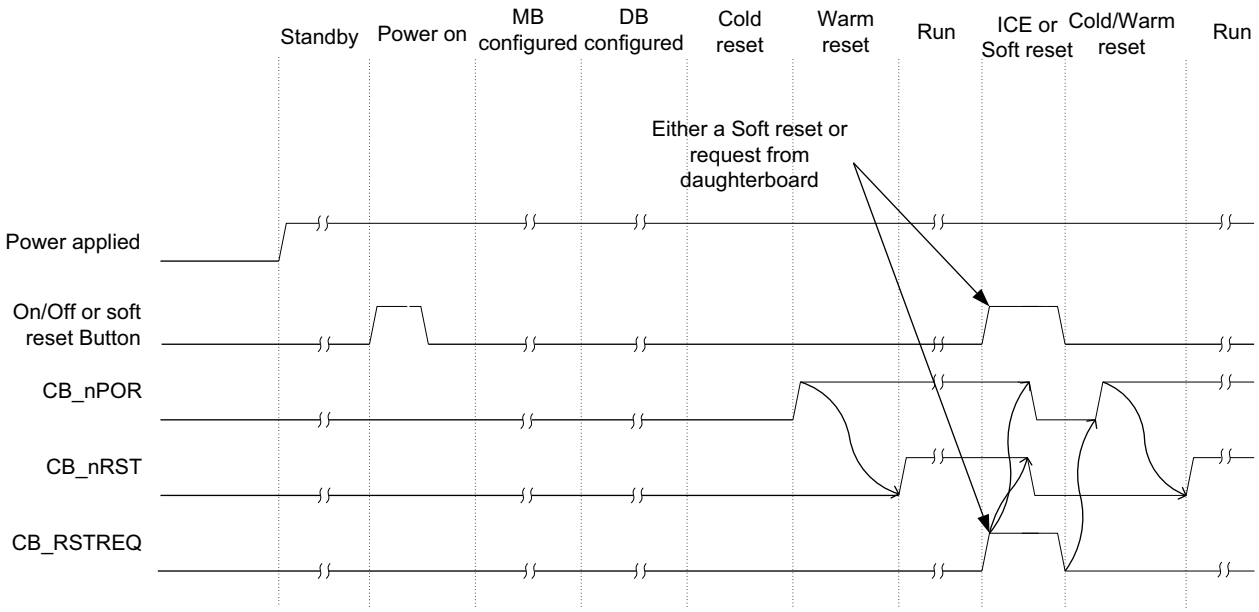


Figure 2-11 Reset timing cycle

2.7 Daughterboard Configuration Controller-FPGA serial interface

The Daughterboard Configuration Controller uses a serial communication channel to receive and transmit information to the FPGA on the daughterboard. The FPGA must implement a *Serial Configuration Controller* (SCC) to support these accesses. See Chapter 3 *Programmers Model*. See also *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4* for an example SCC implementation.

The MCC configures the daughterboard SCC registers on power-up with the values that the daughterboard configuration board file defines. You can also read and write to the SCC registers while the system is running using the motherboard SYS_CFG register interface.

2.7.1 SCC Serial Configuration Controller

The SCC serial interface operates at 0.5MHz. The serial interface is similar to a memory-mapped peripheral because it has an address and a data phase. Figure 2-12 and Figure 2-13 on page 2-24 show the timing diagrams for write and read operations. The SCC operates a 12-bit address and 32-bit data phase.

The **nCFGRST** output from the Daughterboard Configuration Controller loads the default configuration settings into the FPGA. **CFGLOAD** determines when WRITE DATA is completed, or when READ DATA is expected to be ready. The Daughterboard Configuration Controller provides **CFGCLK** to the FPGA. **CFGWnR** changes depending on the access type.

WRITE DATA is sent *Most Significant Bit* (MSB) first.

READ DATA is received *Least Significant Bit* (LSB) first.

The SCC also has an *Advanced Peripheral Bus* (APB) interface that you can use to access the internal registers.

Note

If the SCC serial interface is not implemented in the FPGA design, ARM recommends that you tie off the **CFGDATAOUT** and **nRSTREQ** signals as follows:

- You must tie the **CFGDATAOUT** signal from the FPGA LOW. This is the **NAND_D[5]** pin on the FPGA.
- You must tie the **nRSTREQ** signal from the FPGA HIGH. This is the **NAND_D[7]** pin on the FPGA.

Figure 2-12 shows the timing diagrams for the write operation.

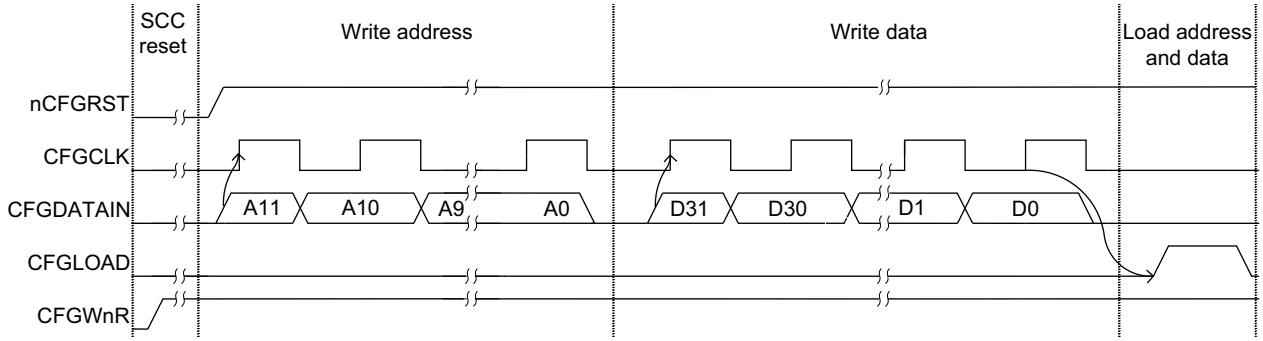


Figure 2-12 Daughterboard Configuration Controller write to SCC

Figure 2-13 on page 2-24 show the timing diagram for the read operation.

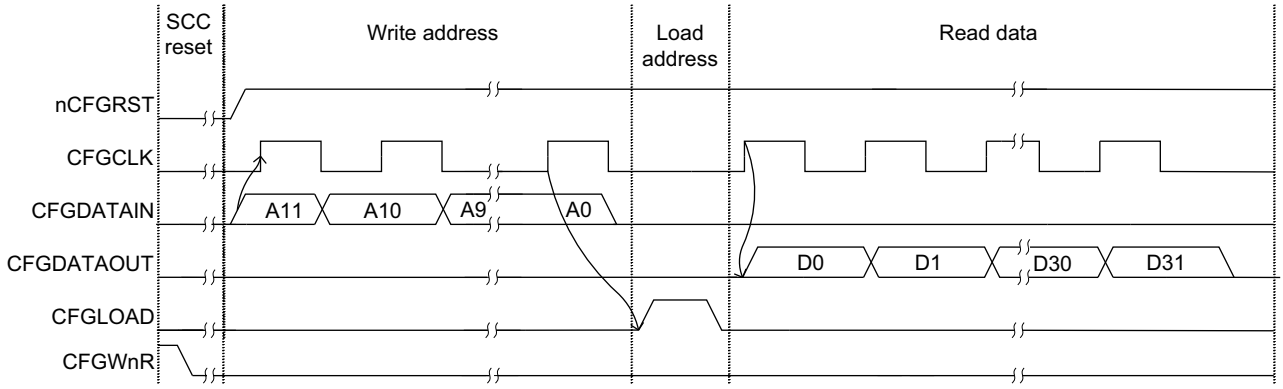


Figure 2-13 Daughterboard Configuration Controller read from SCC

Table 2-8 shows the Daughterboard Configuration Controller AC timing requirements.

Table 2-8 Daughterboard Configuration Controller AC timing requirements for SCC interface

Variable	Time
Daughterboard Configuration Controller output valid time, DCCTov	1µs
Daughterboard Configuration Controller output hold time, DCCToh	1µs
Daughterboard Configuration Controller input setup time, DCCTis	1µs
Daughterboard Configuration Controller input hold time, DCCTih	1µs

2.8 Power

The following sources supply power to the V2F-1XV7 daughterboard:

- HDRY:
  - Supplies: 5V, VIO, CB_SPWR, and CB_3V3 from the motherboard.
- One 1.5V button cell battery that provides power for the Virtex-7 FPGA encryption key.
- One PCIE 6-pin power connector:
  - External supply at 12V at up to 6.25A.

5V, CB_SPWR, and CB_3V3 from the motherboard supply power to devices on the daughterboard, the configuration bus IO, and the parts of the FPGA that communicate with the motherboard. The maximum value of VIO is 1.8V.

If you stack the daughterboards, the external 12V supplies power to the VIO_UP domain, VIO on the upper board, that enables communication to the upper board.

The external 12V supplies power to the FPGA power domains. See Appendix B *Specifications* for information on the power that is available to each of the FPGA power domains.

Figure 2-14 on page 2-26 shows the main power domains of the V2F-1XV7 daughterboard.

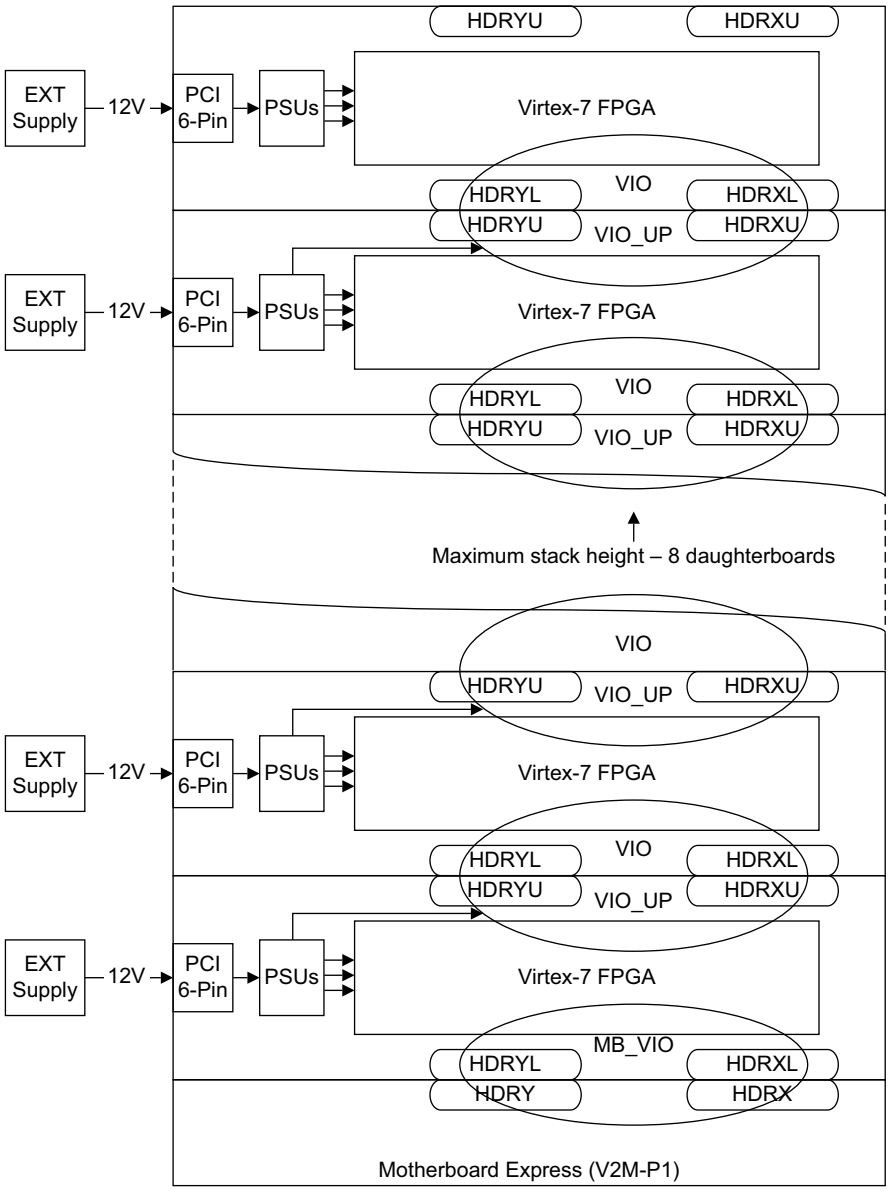


Figure 2-14 Daughterboard power domains

2.9 Temperature monitoring

The Daughterboard Configuration Controller monitors the temperature of the FPGA. The Daughterboard Configuration Controller controls a *Pulse-Width Modulation* (PWM) fan that cools the FPGA.

2.9.1 Daughterboard shutdown because of excessive temperature

The FPGA has an associated red LED, D22, that signifies excessive FPGA temperature. See Figure 1-1 on page 1-4 for the location of this LED on the daughterboard. The LED illuminates when the internal FPGA temperature exceeds approximately 70°C.

If the internal temperature of the FPGA exceeds 80°C, the MCC powers-down the daughterboard to prevent damage.

2.10 FPGA debug and trace

This section describes the debug and trace interfaces provided on the daughterboard. Figure 2-15 shows a simplified view of the F-JTAG, P-JTAG, and Trace connections with an external In-Circuit Analyzer (ILA) and *Processor debug* equipment.

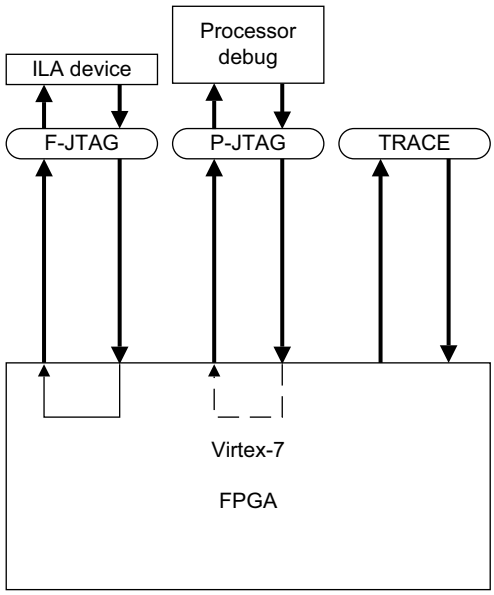


Figure 2-15 Simple JTAG and trace overview

Note

- The ILA device can be any compatible device, for example *XChecker* or *ChipScope*.
- The *Processor debug* device can be any compatible debugger, for example *RealView ICE* (RVI) or *DSTREAM*.

See also Figure 2-1 on page 2-2 and Figure A-2 on page A-3.

2.10.1 F-JTAG

The F-JTAG, ILA, connector supports FPGA debug. See *F-JTAG (ILA) connector* on page A-5. The F-JTAG chain connects to the hard TAP controllers in the FPGA. See the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

2.10.2 P-JTAG

The P-JTAG connector supports P-JTAG, *Processor debug*. The use of the P-JTAG chain requires you to connect the P-JTAG signals to a module within the FPGA that has a TAP interface, and to loop these signals back to form a JTAG chain. See *P-JTAG connector* on page A-6. See also the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

2.10.3 Trace

The Trace connector, connected to the FPGA, supports 16-bit parallel Trace. See *Trace connector* on page A-4. See also the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

2.11 Minimum design settings for daughterboard operation

The minimum RTL in the LogicTile Express FPGA to operate correctly involves:

- Setting the **SMB_CLKO** output to the inactive LOW state.
- Setting the SMB chip select to the inactive HIGH state.
- Setting **CFGDATAOUT** to the inactive LOW state.
- Setting **nRSTREQ** to the inactive HIGH state.

1. Set the **SMB_CLKO** signal to the inactive LOW state as follows:

   Tie **SMB_CLKO** to `b0`.

   Note

   This stops data being clocked to the IOFPGA on the motherboard.

2. Set the SMB chip select to the inactive HIGH state as follows:

   Tie the chip selects **SMB_nCS** to `b11111111`.

   Note

   This stops static memory access to the motherboard.

3. Set the **CFGATAOUT** signal to the inactive LOW state as follows:

   Tie **NAND_D[5]** to `b0`, as the note in *SCC Serial Configuration Controller* on page 2-23 describes.

   Note

   This informs the Daughterboard Configuration Controller that the V2F-1XV7 daughterboard does not implement any of its features.

4. Set the **nRSTREQ** signal to the inactive HIGH state as follows:

   Tie **NAND_D[7]** to `b1`.

   Note

   This prevents **nRSTREQ** from generating a reset. **nRSTREQ** is usually a system-wide master soft reset signal that is both generated and observed by the JTAG debug box.

Note

ARM recommends that you tie all unused pins to their inactive states.

Chapter 3
Programmers Model

This chapter describes the programmers model of the LogicTile Express 20MG, V2F-1XV7, daughterboard. It contains the following sections:

3.1 About this programmers model

The following information applies to the SCC:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in Unpredictable behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or power-on reset.
  - Access type in Table 3-1 on page 3-3 is described as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

3.2 Register summary

Table 3-1 shows the registers in offset order from the base memory address.

Table 3-1 Register summary

Offset	Name	Type	Reset	Width	Description
0x000-0x0FC	DCC_CFGx	RW	0xXXXXXXXX[a]	32	*DCC_CFGx registers* on page 3-5
0x100	DCC_LOCK	RO	0xFFXX000X[b]	32	*DCC_LOCK Register* on page 3-5
0x104	DCC_LED	RO	0x0000000F	32	*DCC_LED Register* on page 3-6
0x108	DCC_SW	RO	0x00000000	32	*DCC_SW Register* on page 3-7
0xFF8	DCC_AID	RO	0xXXXXXXXX[a]	32	*DCC_AID Register* on page 3-7
0xFFC	DCC_ID	RO	0xXXXXXXXX[a]	32	*DCC_ID Register* on page 3-8

a. Where X = unknown at reset.

b. Last X = b000X, either b0000 or b0001.

3.3 Memory map

The images that are loaded into the FPGAs determine the LogicTile Express 20MG memory map. *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4* for an example image.

3.4 SCC register descriptions

The Daughterboard Configuration Controller writes to the SCC registers at powerup with the values that the configuration board file defines. The Daughterboard Configuration Controller also reads the LOCK and ID registers to determine whether the PLLs in the FPGA are locked, and to determine the FPGA image that has been loaded. During run-time, the Daughterboard Configuration Controller polls the LED and switch values to ensure that they match the SCC register values. The SCC registers are also available during run-time from the motherboard SYG_CFG register interface.

3.4.1 DCC_CFGx registers

The DCC_CFGx registers characteristics are:

Purpose These registers write the USER configuration value. You can define up to 64 write registers. The register address must be in increments of `0x004`, and the data must be 32-bits wide. The MCC reads the daughterboard configuration file during board configuration and writes the register values to the FPGA SCC registers. You must implement the appropriate decoder and logic in the FPGA for these to have any effect.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-1 shows the bit assignments.

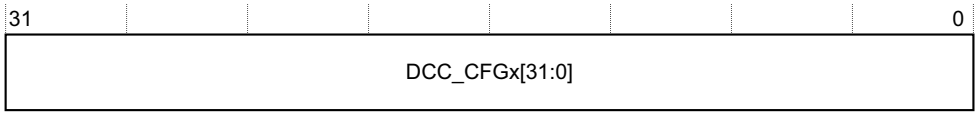


Figure 3-1 DCC_CFGx Registers bit assignments

Table 3-2 shows the bit assignments.

Table 3-2 DCC_CFGx Registers bit assignments

Bits	Name	Function
[31:0]	DCC_CFGx[31:0]	User registers configured during board initialization up from configuration file

Note

You can also update the DCC_CFGx registers during run-time through the motherboard SYS_CFG register interface, or motherboard serial port command line interface or SCC APB interface.

3.4.2 DCC_LOCK Register

The DCC_LOCK Register characteristics are:

Purpose PLL lock status bits from the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-2 shows the bit assignments.

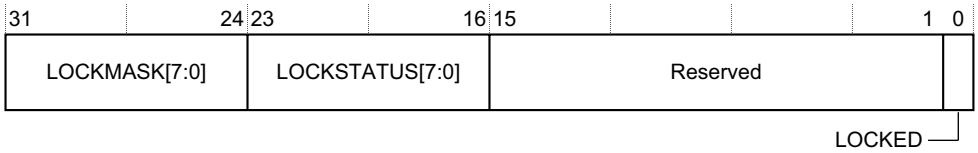


Figure 3-2 DCC_LOCK Register bit assignments

Table 3-3 shows the bit assignments.

Table 3-3 DCC_LOCK Register bit assignments

Bits	Name	Function
[31:24]	LOCK_MASK[7:0]	These bits indicate whether the individual lock bits are masked.
[23:16]	LOCK_STATUS[7:0]	These bits indicate the individual lock status: `b0` Unlocked. `b1` Locked.
[15:1]	-	Reserved.
[0]	LOCKED	This bit indicates whether all unmasked lock bits are locked: `b0` Unlocked. `b1` Locked.

3.4.3 DCC_LED Register

The DCC_LED Register characteristics are:

Purpose Controls the USER LEDs on the daughterboard. The Daughterboard Configuration Controller polls this SCC register from the FPGA and updates the appropriate LEDs.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-3 shows the bit assignments.

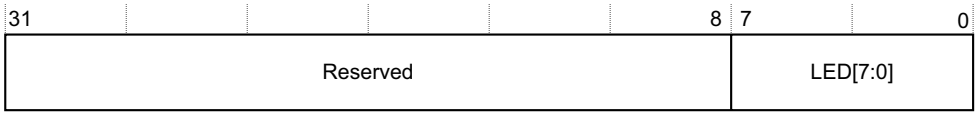


Figure 3-3 DCC_LED Register bit assignments

Table 3-4 shows the bit assignments.

Table 3-4 DCC_LED Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	LED[7:0]	These bits control the individual USER LEDs

3.4.4 DCC_SW Register

The DCC_SW Register characteristics are:

Purpose Determines the state of the eight user switches on the daughterboard. The Daughterboard Configuration Controller polls the switches and updates this SCC register in the FPGA.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-4 shows the register bit assignments.

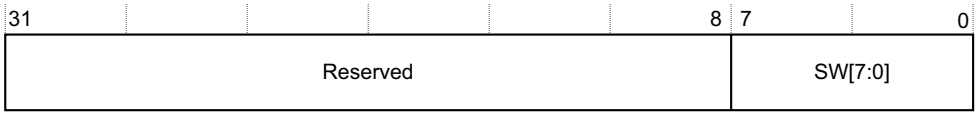


Figure 3-4 DCC_SW Register bit assignments

Table 3-5 shows the bit assignments.

Table 3-5 DCC_SW Register bit assignments

Bits	Name	Function
[31:8]	-	Reserved
[7:0]	SW[7:0]	These bits indicate state of user switches

3.4.5 DCC_AID Register

The DCC_AID Register characteristics are:

Purpose The Daughterboard Configuration Controller reads this information and uses it to determine the number of DCC_CFGx registers, and the registers that are supported that can be read from the motherboard SYS-CFG register interface. If this register is not implemented, the Daughterboard Configuration Controller does not support user switches or LEDs, lock, or `user config` commands.

If a SCC interface is not implemented in the FPGAs, the FPGA **CFGDATAOUT** signal must be pulled to a logic LOW to signal to the Daughterboard Configuration Controller that no data is transferred.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-5 shows the bit assignments.

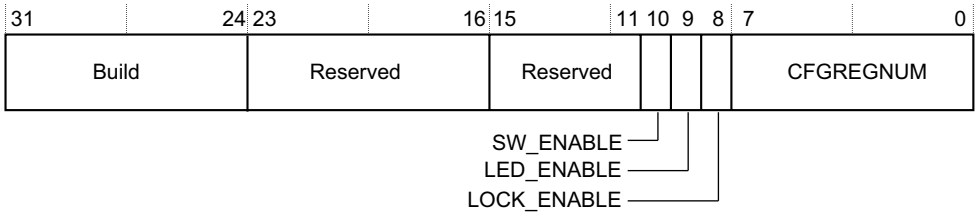


Figure 3-5 DCC_AID Register bit assignments

Table 3-6 shows the bit assignments.

Table 3-6 DCC_AID Register bit assignments

Bits	Name	Function
[31:24]	Build	FPGA build number.
[23:16]	-	Reserved.
[15:11]	-	Reserved.
[10]	SW_ENABLE	This bit indicates whether the DCC_SW_READ command is supported.
[9]	LED_ENABLE	This bit indicates whether the DCC_LED_READ command is supported.
[8]	LOCK_ENABLE	This bit indicates whether the DCC_LOCK_READ command is supported.
[7:0]	CFGREGNUM	These bits indicate the number of user config commands. The maximum number supported is 64.

3.4.6 DCC_ID Register

The DCC_ID Register characteristics are:

Purpose The Daughterboard Configuration Controller reads this register and uses it to determine information about the design in the FPGA that can be read through the motherboard SYS_CFG register interface.

Usage constraints There are no usage constraints.

Configurations Available in all LogicTile Express 20MG configurations.

Attributes Table 3-1 on page 3-3.

Figure 3-6 shows the bit assignments.

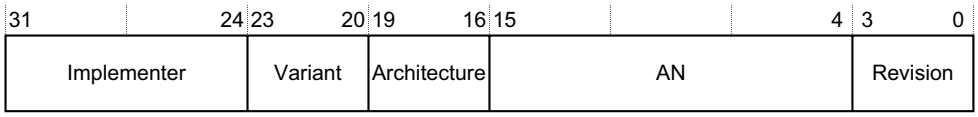


Figure 3-6 DCC_ID Register bit assignments

Table 3-7 shows the bit assignments.

Table 3-7 DCC_ID Register bit assignments

Bits	Name	Function
[31:24]	Implementer	Implementer ID.
[23:20]	Variant	Variant number.
[19:16]	Architecture	Architecture. `0x00` for Application Notes.
[15:4]	AN	Application Note number.
[3:0]	Revision	Revision number.

Appendix A
Signal Descriptions

This appendix describes the signals present at the interface connectors. The on-board connectors are:

A.1 Daughterboard connectors

Figure A-1 shows the connectors fitted to the lower side of the daughterboard.

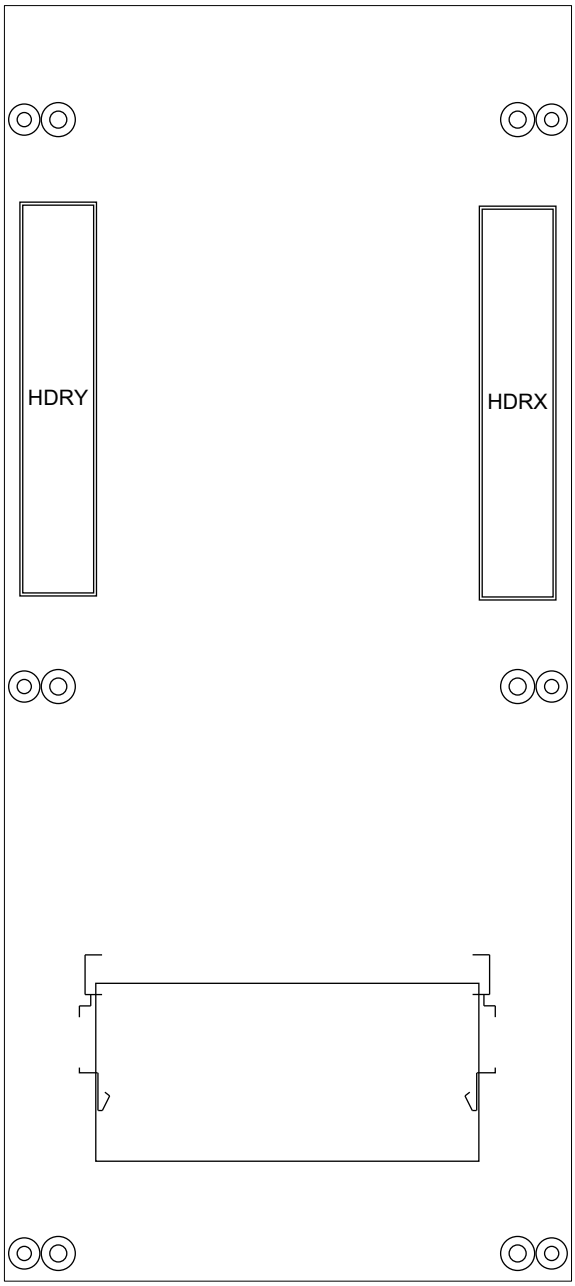


Figure A-1 Connectors on lower side of daughterboard

Figure A-2 on page A-3 shows the connectors fitted to the upper side of the daughterboard.

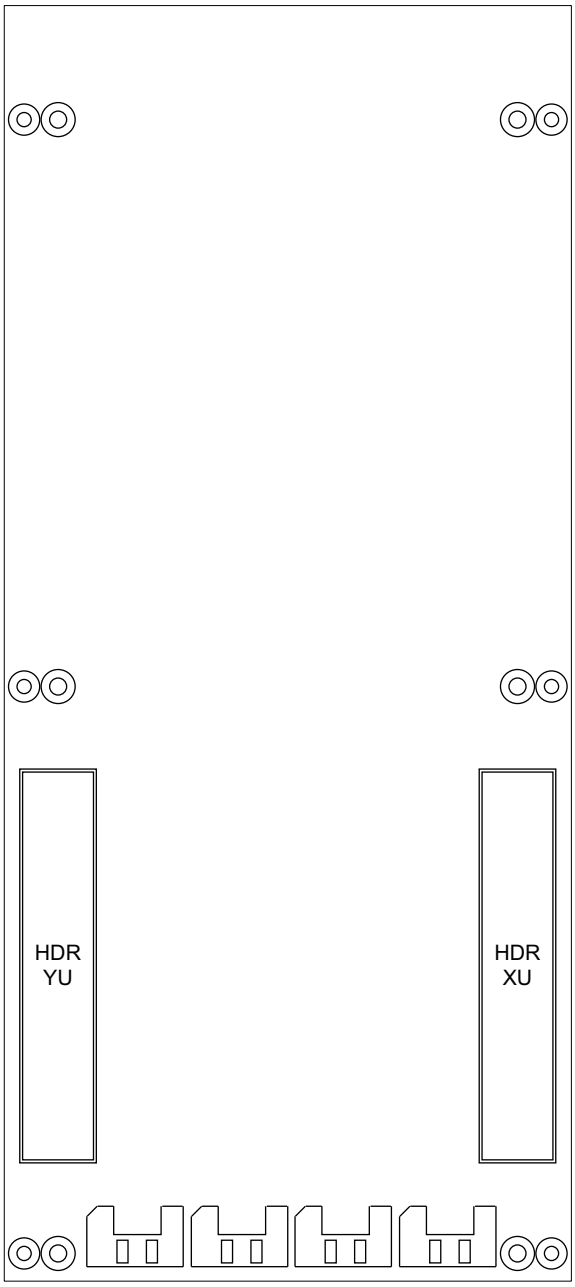


Figure A-2 Connectors on upper side of daughterboard

A.1.1 Header connectors on lower side of board

Two high-density headers on the underside of the daughterboard route signal and power interconnects to the motherboard and to the other daughterboard site:

- HDRYL routes signal and power interconnects to the motherboard.
- HDRXL routes high-speed buses to the other daughterboard site.

the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*.

A.1.2 Header connectors on upper side of board

Two high density headers, HDRXU and HDRYU, on the upper side of the board, route signal and power interconnects to support upward expansion:

- HDRYU routes signal and power interconnects to the expansion board.
- HDRXL routes high-speed buses to the expansion board.

You must implement these buses yourself. *FPGA bus widths* on page 2-6.

The Versatile Express PCIe connector daughterboard, V2C-002, is an example of a board that can be used for upward expansion. the DVD supplied with the V2F-1XV7 daughterboard for mechanical information.

A.1.3 SO-DIMM connector

The SO-DIMM connector is on the lower side of the board and enables up to 8GB of 64-bit DDR3 memory expansion. You can download the signal list and connector information from the JEDEC web site. *Other publications* on page ix.

A.1.4 Trace connector

The V2F-1XV7 daughterboard provides one MICTOR trace connector, J17, labeled *Trace*. The connector supports 16-bit trace and provides access to a *Trace Port Interface Unit* (TPIU) that can be implemented in the FPGA.

Note

Examples of trace modules that can be used are RealView ICE and RealView Trace 2.

Figure A-3 shows the MICTOR connector, part number AMP 2-5767004-2.

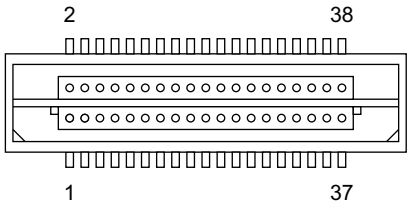


Figure A-3 Trace Connector, J17

Table A-1 shows the trace pin mapping for each *Trace* signal. the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-1 Trace dual connector, J17, signal list

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKA**
7	**TRACEDBGRQ**	8	**TRACEDBGACK**
9	**nSRST**	10	**TRACEEXTTRIGX**
11	**TDO**	12	**VTREFA, 1V5**

Table A-1 Trace dual connector, J17, signal list (continued)

Pin	Signal	Pin	Signal
13	**RTCK**	14	**VSUPPYLYA**
15	**TCK**	16	**TRACEDATA7**
17	**TMS**	18	**TRACEDATA6**
19	**TDI**	20	**TRACEDATA5**
21	**nTRST**	22	**TRACEDATA4**
23	**TRACEDATA15**	24	**TRACEDATA3**
25	**TRACEDATA14**	26	**TRACEDATA2**
27	**TRACEDATA13**	28	**TRACEDATA1**
29	**TRACEDATA12**	30	**GND**
31	**TRACEDATA11**	32	**GND**
33	**TRACEDATA10**	34	**VTREFA**, 1V5
35	**TRACEDATA9**	36	**TRACECTL**
37	**TRACEDATA8**	38	**TRACEDATA0**

Note

The V2F-1XV7 daughterboard does not support adaptive clocking. The **RTCK** signal is tied LOW on the trace connector.

A.1.5 F-JTAG (ILA) connector

The V2F-1XV7 daughterboard provides an F-JTAG (ILA) connector, J4, to enable you to connect an ILA device, such as *ChipScope*, to debug designs in the FPGA. Figure A-4 shows the F-JTAG (ILA) connector.

Note

Pins 2, 4, 6, 8, and 10 on the F-JTAG (ILA) connector have pull-up resistors to 1V5.

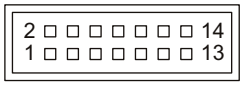


Figure A-4 F-JTAG, ILA, connector, J4

Table A-2 shows the F-JTAG (ILA) pin mapping for each ILA signal. the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-2 F-JTAG, ILA, connector, J4, signal list

Pin	Signal	Pin	Signal
1	**GND**	2	**ILA_1V5**
3	**GND**	4	**ILA_TMS**
5	**GND**	6	**ILA_TCK**
7	**GND**	8	**ILA_TDO**
9	**GND**	10	**ILA_TDI**
11	**GND**	12	Not connected
13	**GND**	14	Not connected

A.1.6 P-JTAG connector

The V2F-1XV7 daughterboard provides a P-JTAG connector to enable connection of RealView ICE, DSTREAM, or a compatible third-party debugger. Figure A-5 shows the P-JTAG connector, J18.

Note

DBGRQ has a pull-down resistor to 0V. **DBGACK** has no pull-up or pull-down resistor. All other signal connections on the P-JTAG connector have pull-up resistors to 1V5.

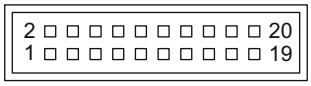


Figure A-5 P-JTAG connector, J18

Table A-3 shows the P-JTAG pin mapping for each P-JTAG signal. the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-3 P-JTAG connector, J5, signal list

Pin	Signal	Pin	Signal
1	**VIREF**	2	**VSUPPLYA**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**TMS**	8	**GND**
9	**TCK**	10	**GND**
11	**RTCK**	12	**GND**
13	**TDO**	14	**GND**

Table A-3 P-JTAG connector, J5, signal list (continued)

Pin	Signal	Pin	Signal
15	**nSRST**	16	**GND**
17	**DBGRQ**	18	**GND**
19	**DBGACK**	20	**GND**

A.1.7 SATA connectors

There are four SATA connectors, J13, J14, J15, and J16, on the daughterboard that provide connectivity for four SATA Host, H, and four SATA Device, D, interfaces. Figure A-2 on page A-3 shows the location of these connectors.

Figure A-6 shows the SATA connector.

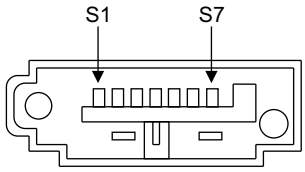


Figure A-6 SATA connector, J13, J14, J15, and J16

Table A-4 and Table A-5 on page A-8 show the SATA Host pin mappings and GTX locations for the Host 0 and Host 1 SATA signals.

Note

the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-4 shows the SATA Host pin mappings and GTX Transceiver Quad locations for the Host 0 SATA signals.

Table A-4 SATA Host Device 0, J13, signal list

Pin	Signal	FPGA pin	GTX Transceiver Quad location
S1	**GND**	-	-
S2	**SATAH_A_P0**	AY2	X0Y7
S3	**SATAH_A_N0**	AY1	X0Y7
S4	**GND**	-	-
S5	**SATAH_B_N0**	AW3	X0Y7
S6	**SATAH_B_P0**	AW4	X0Y7
S7	**GND**	-	-

Table A-5 shows the SATA Host pin mappings and GTX Transceiver Quad locations for the Host 1 SATA signals.

Table A-5 SATA Host Device 1, J15, signal list

Pin	Signal	FPGA pin	GTX Transceiver Quad location
S1	**GND**	-	-
S2	**SATAH_A_P1**	BA4	X0Y6
S3	**SATAH_A_N1**	BA3	X0Y6
S4	**GND**	-	-
S5	**SATAH_B_N1**	AY5	X0Y6
S6	**SATAH_B_P1**	AY6	X0Y6
S7	**GND**	-	-

Note

the `an306_revb.xdc` constraints file, available in *Application Note 306 Example LogicTile Express 20MG Design for a CoreTile Express A9x4*, for FPGA mapping.

Table A-6 shows the SATA Device pin mappings and GTX Transceiver Quad locations for the Device 0, J14, SATA signals.

Table A-6 SATA Device 0, J14, signal list

Pin	Signal	FPGA pin	GTX Transceiver Quad location
S1	**GND**	-	-
S2	**SATAD_A_P0**	BB6	X0Y5
S3	**SATAD_A_N0**	BB5	X0Y5
S4	**GND**	-	-
S5	**SATAD_B_N0**	BB1	X0Y5
S6	**SATAD_B_P0**	BB2	X0Y5
S7	**GND**	-	-

Table A-7 shows the SATA Device pin mappings and GTX Transceiver Quad locations for the Device 1, J16, SATA signals.

Table A-7 SATA Device 1, J16, signal list

Pin	Signal	FPGA pin	GTX Transceiver Quad location
S1	**GND**	-	-
S2	**SATAD_A_P1**	BD6	X0Y4
S3	**SATAD_A_N1**	BD5	X0Y4

Table A-7 SATA Device 1, J16, signal list (continued)

Pin	Signal	FPGA pin	GTX Transceiver Quad location
S4	**GND**	-	-
S5	**SATAD_B_N1**	BC3	X0Y4
S6	**SATAD_B_P1**	BC4	X0Y4
S7	**GND**	-	-

Appendix B
Specifications

This appendix contains the electrical specification of the daughterboard. It contains the following section:

- *Electrical specification* on page B-2.

B.1 Electrical specification

This section provides information on the current characteristics of the daughterboard.

B.1.1 FPGA current requirements

the Xilinx web site, http://www.xilinx.com, for software to help you calculate the current requirements for your particular application.

Table B-1 shows the power available for each power domain of the Virtex-7 FPGA on the daughterboard and the IO pins on any expansion board supplied through the headers.

Table B-1 Available FPGA current

Power domain	Voltage	Maximum available current	Power	Comment
VCCINT	1.0V	20A	20W	FPGA cores.
VCCBRAM	1.0V	0.4A	0.4W	FPGA block RAMs.
VCCAUX_IO	2.0V	4.5A	9W	Intermediate logic between FPGA cores and IO pads.
VCCAUX	1.8V	5A	9W	FPGA auxiliary supply voltage.
MGTVCCAUX	1.8	400mA	720mW	Auxiliary analog Quad PLL voltage supply for the transceivers.
MGTAVCC	1.0V	3A	3W	Internal analog circuits of the GTX transceiver on the FPGA.
MGTAVTT	1.2V	3A	3.6W	Analog supply for the transmitter and receiver termination circuits of the GTX transceiver on the FPGA.
VIO_UP	1.2-1.8V	10A	12-18W	Current shared between the IO pins that communicate between the FPGA and any expansion board supplied through the upper header connectors, HDRXU and HDRYU.
VIO	1.2-1.8V	5.5A	12-18W	Current shared between the IO pins that communicate between the FPGA on an expansion board supplied through the lower header connectors, HDRYL and HDRU. The board beneath can be another V2F-1XV7 daughterboard or the V2M-P1 motherboard.
DDR3	1.5V	5.5A	8.25W	FPGA DDR3 IO pins and DDR3 module.

Caution

- Some FPGA designs might exceed the current and temperature rating of the board. Therefore, you must estimate the power requirements of such designs, using tools such as Xilinx XPE, before implementation.
- The heatsinks supplied on the FPGA have a thermal resistance of 1.6°C per Watt. The recommended maximum FPGA temperature is 80°C.

Appendix C
Revisions

This appendix describes the technical changes between released issues of this book.

Table C-1 Issue A

Change	Location	Affects
No changes, first release	-	-

Table C-2 Differences between Issue A and Issue B

Change	Locations	Affects
Clarified SATA pin and SATA FPGA mappings.	*SATA connectors* on page A-7	All versions
Removed reference to Application Note AN306 because it does not include an example DDR3 controller netlist.	*DDR3 memory interface (SO-DIMM)* on page 2-10	All versions
SO-DIMM connector supports up to a maximum 4GB of external DDR3 RAM.	*Overview of the daughterboard hardware* on page 2-2 *DDR3 memory interface (SO-DIMM)* on page 2-10	Rev C

Table C-3 Differences between Issue B and Issue C

Change	Locations	Affects
Added section on information transmitted by the DCC to the motherboard	*Voltage, temperature, oscillator, and SCC register monitoring* on page 2-13	All versions
Clarified description of daughterboard clocks.	Table 2-7 on page 2-15	All versions

Table C-4 Differences between Issue C and Issue D

Change	Locations	Affects
Corrected description of PCI Express system.	*System interconnect* on page 2-5 *PCI Express Bus (PCIe)* on page 2-8 Figure 2-6 on page 2-16	All versions