Arm® Architecture Registers
Armv8, for Armv8-A architecture profile
Arm Architecture Registers
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Release Information

For information on the change history and known issues for this release, see the Release Notes in the System Register XML for Armv8.7 (2020-09).

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(LES-PRE-20349 version 21.0)

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The information in this document covers multiple versions of the architecture. The content relating to different versions is given different quality ratings.

The information in this document relating to v8.7 of the architecture and the features introduced in this release is at Alpha quality. Alpha quality means that most major features of the specification are included, features and details might be missing.

The information in this document relating to versions of the architecture before v8.7 and features introduced in previous releases is at Beta quality. Beta quality means that all major features of the specification are included, some details might be missing.
Web Address

http://www.arm.com
AArch64 System Registers

**ACCDATA_EL1**: Accelerator Data

**ACTLR_EL1**: Auxiliary Control Register (EL1)

**ACTLR_EL2**: Auxiliary Control Register (EL2)

**ACTLR_EL3**: Auxiliary Control Register (EL3)

**AFSR0_EL1**: Auxiliary Fault Status Register 0 (EL1)

**AFSR0_EL2**: Auxiliary Fault Status Register 0 (EL2)

**AFSR0_EL3**: Auxiliary Fault Status Register 0 (EL3)

**AFSR1_EL1**: Auxiliary Fault Status Register 1 (EL1)

**AFSR1_EL2**: Auxiliary Fault Status Register 1 (EL2)

**AFSR1_EL3**: Auxiliary Fault Status Register 1 (EL3)

**AIDR_EL1**: Auxiliary ID Register

**AMAIR_EL1**: Auxiliary Memory Attribute Indirection Register (EL1)

**AMAIR_EL2**: Auxiliary Memory Attribute Indirection Register (EL2)

**AMAIR_EL3**: Auxiliary Memory Attribute Indirection Register (EL3)

**AMCFGR_EL0**: Activity Monitors Configuration Register

**AMCG1IDR_EL0**: Activity Monitors Counter Group 1 Identification Register

**AMCGCR_EL0**: Activity Monitors Counter Group Configuration Register

**AMCNTENCLR0_EL0**: Activity Monitors Count Enable Clear Register 0

**AMCNTENCLR1_EL0**: Activity Monitors Count Enable Clear Register 1

**AMCNTENSET0_EL0**: Activity Monitors Count Enable Set Register 0

**AMCNTENSET1_EL0**: Activity Monitors Count Enable Set Register 1

**AMCR_EL0**: Activity Monitors Control Register

**AMEVCNTR0<n>_EL0**: Activity Monitors Event Counter Registers 0

**AMEVCNTR1<n>_EL0**: Activity Monitors Event Counter Registers 1

**AMEVCNTVOFF0<n>_EL2**: Activity Monitors Event Counter Virtual Offset Registers 0

**AMEVCNTVOFF1<n>_EL2**: Activity Monitors Event Counter Virtual Offset Registers 1

**AMEVTYPER0<n>_EL0**: Activity Monitors Event Type Registers 0

**AMEVTYPER1<n>_EL0**: Activity Monitors Event Type Registers 1

**AMUSERENR_EL0**: Activity Monitors User Enable Register

**APDAKeyHi_EL1**: Pointer Authentication Key A for Data (bits[127:64])

**APDAKeyLo_EL1**: Pointer Authentication Key A for Data (bits[63:0])

**APDBKeyHi_EL1**: Pointer Authentication Key B for Data (bits[127:64])

**APDBKeyLo_EL1**: Pointer Authentication Key B for Data (bits[63:0])

**APGAKeyHi_EL1**: Pointer Authentication Key A for Code (bits[127:64])
APGAKeyLo_EL1: Pointer Authentication Key A for Code (bits[63:0])
APGAKeyHi_EL1: Pointer Authentication Key A for Instruction (bits[127:64])
APGAKeyLo_EL1: Pointer Authentication Key A for Instruction (bits[63:0])
APGAKeyHi_EL1: Pointer Authentication Key B for Instruction (bits[127:64])
APGAKeyLo_EL1: Pointer Authentication Key B for Instruction (bits[63:0])
CCSIDR2_EL1: Current Cache Size ID Register 2
CCSIDR_EL1: Current Cache Size ID Register
CLIDR_EL1: Cache Level ID Register
CNTFRO_EL0: Counter-timer Frequency register
CNTHCTL_EL2: Counter-timer Hypervisor Control register
CNTHPS_CTL_EL2: Counter-timer Secure Physical Timer Control register (EL2)
CNTHPS_CVAL_EL2: Counter-timer Secure Physical Timer CompareValue register (EL2)
CNTHPS_TVAL_EL2: Counter-timer Secure Physical Timer TimerValue register (EL2)
CNTHP_CTL_EL2: Counter-timer Hypervisor Physical Timer Control register
CNTHP_CVAL_EL2: Counter-timer Physical Timer CompareValue register (EL2)
CNTHP_TVAL_EL2: Counter-timer Physical Timer TimerValue register (EL2)
CNTHVS_CTL_EL2: Counter-timer Secure Virtual Timer Control register (EL2)
CNTHVS_CVAL_EL2: Counter-timer Secure Virtual Timer CompareValue register (EL2)
CNTHVS_TVAL_EL2: Counter-timer Secure Virtual Timer TimerValue register (EL2)
CNTHV_CTL_EL2: Counter-timer Virtual Timer Control register (EL2)
CNTHV_CVAL_EL2: Counter-timer Virtual Timer CompareValue register (EL2)
CNTHV_TVAL_EL2: Counter-timer Virtual Timer TimerValue Register (EL2)
CNTKCTL_EL1: Counter-timer Kernel Control register
CNTPCTSS_EL0: Counter-timer Self-Synchronized Physical Count register
CNTPCT_EL0: Counter-timer Physical Count register
CNTPOFF_EL2: Counter-timer Physical Offset register
CNTPS_CTL_EL1: Counter-timer Physical Secure Timer Control register
CNTPS_CVAL_EL1: Counter-timer Physical Secure Timer CompareValue register
CNTPS_TVAL_EL1: Counter-timer Physical Secure Timer TimerValue register
CNTP_CTL_EL0: Counter-timer Physical Timer Control register
CNTP_CVAL_EL0: Counter-timer Physical Timer CompareValue register
CNTP_TVAL_EL0: Counter-timer Physical Timer TimerValue register
CNTVCTSS_EL0: Counter-timer Self-Synchronized Virtual Count register
CNTVCT_EL0: Counter-timer Virtual Count register
CNTVOFF_EL2: Counter-timer Virtual Offset register
CNTV_CTL_EL0: Counter-timer Virtual Timer Control register
CNTV_CV р: Counter-timer Virtual Timer CompareValue register
CNTV_TV р: Counter-timer Virtual Timer TimerValue register
CONTEXTIDR_EL1: Context ID Register (EL1)
CONTEXTIDR_EL2: Context ID Register (EL2)
CPACR_EL1: Architectural Feature Access Control Register
CPTR_EL2: Architectural Feature Trap Register (EL2)
CPTR_EL3: Architectural Feature Trap Register (EL3)
CSSELR_EL1: Cache Size Selection Register
CTR_EL0: Cache Type Register
CurrentEL: Current Exception Level
DACR32_EL2: Domain Access Control Register
DAIF: Interrupt Mask Bits
DBGAUTHSTATUS_EL1: Debug Authentication Status register
DBGBCР<n>_EL1: Debug Breakpoint Control Registers
DBGВVR<n>_EL1: Debug Breakpoint Value Registers
DBGCLAIMCLR_EL1: Debug CLAIM Tag Clear register
DBGCLAIMSET_EL1: Debug CLAIM Tag Set register
DBGDTRRX_EL0: Debug Data Transfer Register, Receive
DBGDTRTX_EL0: Debug Data Transfer Register, Transmit
DBGDT_EL0: Debug Data Transfer Register, half-duplex
DBGPRCР_EL1: Debug Power Control Register
DBGVCР32_EL2: Debug Vector Catch Register
DBGWCR<n>_EL1: Debug Watchpoint Control Registers
DBGWVR<n>_EL1: Debug Watchpoint Value Registers
DCZID_EL0: Data Cache Zero ID register
DISR_EL1: Deferred Interrupt Status Register
DIT: Data Independent Timing
DLR_EL0: Debug Link Register
DSPSR_EL0: Debug Saved Program Status Register
ELR_EL1: Exception Link Register (EL1)
ELR_EL2: Exception Link Register (EL2)
ELR_EL3: Exception Link Register (EL3)
ERRIDR_EL1: Error Record ID Register
ERRSELР_EL1: Error Record Select Register
ERRADDR_EL1: Selected Error Record Address Register
ERXCTRL_EL1: Selected Error Record Control Register
ERXFR_EL1: Selected Error Record Feature Register
ERXMISC0_EL1: Selected Error Record Miscellaneous Register 0
ERXMISC1_EL1: Selected Error Record Miscellaneous Register 1
ERXMISC2_EL1: Selected Error Record Miscellaneous Register 2
ERXMISC3_EL1: Selected Error Record Miscellaneous Register 3
ERXPFGCDN_EL1: Selected Pseudo-fault Generation Countdown register
ERXPFGCTL_EL1: Selected Pseudo-fault Generation Control register
ERXPFGF_EL1: Selected Pseudo-fault Generation Feature register
ERXSTATUS_EL1: Selected Error Record Primary Status Register
ESR_EL1: Exception Syndrome Register (EL1)
ESR_EL2: Exception Syndrome Register (EL2)
ESR_EL3: Exception Syndrome Register (EL3)
FAR_EL1: Fault Address Register (EL1)
FAR_EL2: Fault Address Register (EL2)
FAR_EL3: Fault Address Register (EL3)
FPCR: Floating-point Control Register
FPEXC32_EL2: Floating-Point Exception Control register
FPSR: Floating-point Status Register
GCR_EL1: Tag Control Register.
GMID_EL1: Multiple tag transfer ID register
HACR_EL2: Hypervisor Auxiliary Control Register
HAFGRTR_EL2: Hypervisor Activity Monitors Fine-Grained Read Trap Register
HCRX_EL2: Extended Hypervisor Configuration Register
HCR_EL2: Hypervisor Configuration Register
HDFGRTR_EL2: Hypervisor Debug Fine-Grained Read Trap Register
HDFGWTR_EL2: Hypervisor Debug Fine-Grained Write Trap Register
HFGITR_EL2: Hypervisor Fine-Grained Instruction Trap Register
HFGRTR_EL2: Hypervisor Fine-Grained Read Trap Register
HFGWTR_EL2: Hypervisor Fine-Grained Write Trap Register
HPFAR_EL2: Hypervisor IPA Fault Address Register
HSTR_EL2: Hypervisor System Trap Register
ICC_AP0R<n>_EL1: Interrupt Controller Active Priorities Group 0 Registers
ICC_AP1R<n>_EL1: Interrupt Controller Active Priorities Group 1 Registers
ICC_ASGI1R_EL1: Interrupt Controller Alias Software Generated Interrupt Group 1 Register
ICC_BPR0_EL1: Interrupt Controller Binary Point Register 0
ICC_BPR1_EL1: Interrupt Controller Binary Point Register 1
ICC_CTLR_EL1: Interrupt Controller Control Register (EL1)
ICC_CTLR_EL3: Interrupt Controller Control Register (EL3)
ICC_DIR_EL1: Interrupt Controller Deactivate Interrupt Register
ICC_EOIR0_EL1: Interrupt Controller End Of Interrupt Register 0
ICC_EOIR1_EL1: Interrupt Controller End Of Interrupt Register 1
ICC_HPPIR0_EL1: Interrupt Controller Highest Priority Pending Interrupt Register 0
ICC_HPPIR1_EL1: Interrupt Controller Highest Priority Pending Interrupt Register 1
ICC_IAR0_EL1: Interrupt Controller Interrupt Acknowledge Register 0
ICC_IAR1_EL1: Interrupt Controller Interrupt Acknowledge Register 1
ICC_IGRPEN0_EL1: Interrupt Controller Interrupt Group 0 Enable register
ICC_IGRPEN1_EL1: Interrupt Controller Interrupt Group 1 Enable register
ICC_IGRPEN1_EL3: Interrupt Controller Interrupt Group 1 Enable register (EL3)
ICC_PMR_EL1: Interrupt Controller Interrupt Priority Mask Register
ICC_RPR_EL1: Interrupt Controller Running Priority Register
ICC_SGI0R_EL1: Interrupt Controller Software Generated Interrupt Group 0 Register
ICC_SGI1R_EL1: Interrupt Controller Software Generated Interrupt Group 1 Register
ICC_SRE_EL1: Interrupt Controller System Register Enable register (EL1)
ICC_SRE_EL2: Interrupt Controller System Register Enable register (EL2)
ICC_SRE_EL3: Interrupt Controller System Register Enable register (EL3)
ICH_AP0R<n>_EL2: Interrupt Controller Hyp Active Priorities Group 0 Registers
ICH_AP1R<n>_EL2: Interrupt Controller Hyp Active Priorities Group 1 Registers
ICH_EISR_EL2: Interrupt Controller End of Interrupt Status Register
ICH_ELRSR_EL2: Interrupt Controller Empty List Register Status Register
ICH_HCR_EL2: Interrupt Controller Hyp Control Register
ICH_LR<n>_EL2: Interrupt Controller List Registers
ICH_MISR_EL2: Interrupt Controller Maintenance Interrupt State Register
ICH_VMCR_EL2: Interrupt Controller Virtual Machine Control Register
ICH_VTR_EL2: Interrupt Controller VGIC Type Register
ICV_AP0R<n>_EL1: Interrupt Controller Virtual Active Priorities Group 0 Registers
ICV_AP1R<n>_EL1: Interrupt Controller Virtual Active Priorities Group 1 Registers
ICV_BPR0_EL1: Interrupt Controller Virtual Binary Point Register 0
ICV_BPR1_EL1: Interrupt Controller Virtual Binary Point Register 1
ICV_CTLR_EL1: Interrupt Controller Virtual Control Register
ICV_DIR_EL1: Interrupt Controller Deactivate Virtual Interrupt Register
ICV_EOIR0_EL1: Interrupt Controller Virtual End Of Interrupt Register 0
ICV_EOIR1_EL1: Interrupt Controller Virtual End Of Interrupt Register 1
ICV_HPPIR0_EL1: Interrupt Controller Virtual Highest Priority Pending Interrupt Register 0
ICV_HPPIR1_EL1: Interrupt Controller Virtual Highest Priority Pending Interrupt Register 1
ICV_IAR0_EL1: Interrupt Controller Virtual Interrupt Acknowledge Register 0
ICV_IAR1_EL1: Interrupt Controller Virtual Interrupt Acknowledge Register 1
ICV_IGRPEN0_EL1: Interrupt Controller Virtual Interrupt Group 0 Enable register
ICV_IGRPEN1_EL1: Interrupt Controller Virtual Interrupt Group 1 Enable register
ICV_PMR_EL1: Interrupt Controller Virtual Interrupt Priority Mask Register
ICV_RPR_EL1: Interrupt Controller Virtual Running Priority Register
ID_AA64AFR0_EL1: AArch64 Auxiliary Feature Register 0
ID_AA64AFR1_EL1: AArch64 Auxiliary Feature Register 1
ID_AA64DFR0_EL1: AArch64 Debug Feature Register 0
ID_AA64DFR1_EL1: AArch64 Debug Feature Register 1
ID_AA64ISAR0_EL1: AArch64 Instruction Set Attribute Register 0
ID_AA64ISAR1_EL1: AArch64 Instruction Set Attribute Register 1
ID_AA64ISAR2_EL1: AArch64 Instruction Set Attribute Register 2
ID_AA64MMFR0_EL1: AArch64 Memory Model Feature Register 0
ID_AA64MMFR1_EL1: AArch64 Memory Model Feature Register 1
ID_AA64MMFR2_EL1: AArch64 Memory Model Feature Register 2
ID_AA64PFR0_EL1: AArch64 Processor Feature Register 0
ID_AA64PFR1_EL1: AArch64 Processor Feature Register 1
ID_AA64ZFR0_EL1: SVE Feature ID register 0
ID_AFR0_EL1: AArch32 Auxiliary Feature Register 0
ID_DFR0_EL1: AArch32 Debug Feature Register 0
ID_DFR1_EL1: Debug Feature Register 1
ID_ISAR0_EL1: AArch32 Instruction Set Attribute Register 0
ID_ISAR1_EL1: AArch32 Instruction Set Attribute Register 1
ID_ISAR2_EL1: AArch32 Instruction Set Attribute Register 2
ID_ISAR3_EL1: AArch32 Instruction Set Attribute Register 3
ID_ISAR4_EL1: AArch32 Instruction Set Attribute Register 4
ID_ISAR5_EL1: AArch32 Instruction Set Attribute Register 5
ID_ISAR6_EL1: AArch32 Instruction Set Attribute Register 6
ID_MMFR0_EL1: AArch32 Memory Model Feature Register 0
ID_MMFR1_EL1: AArch32 Memory Model Feature Register 1
ID_MMFR2_EL1: AArch32 Memory Model Feature Register 2
ID_MMFR3_EL1: AArch32 Memory Model Feature Register 3
ID_MMFR4_EL1: AArch32 Memory Model Feature Register 4
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<th>Register Name</th>
<th>Purpose</th>
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<td><strong>ID_MMFR5_EL1</strong></td>
<td>AArch32 Memory Model Feature Register 5</td>
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<td><strong>ID_PFR0_EL1</strong></td>
<td>AArch32 Processor Feature Register 0</td>
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<td><strong>ID_PFR1_EL1</strong></td>
<td>AArch32 Processor Feature Register 1</td>
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<td><strong>ID_PFR2_EL1</strong></td>
<td>AArch32 Processor Feature Register 2</td>
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<td><strong>IFSR32_EL2</strong></td>
<td>Instruction Fault Status Register (EL2)</td>
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<td><strong>ISR_EL1</strong></td>
<td>Interrupt Status Register</td>
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<td><strong>LORC_EL1</strong></td>
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<td><strong>LOREA_EL1</strong></td>
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<td><strong>LORID_EL1</strong></td>
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<td><strong>LORN_EL1</strong></td>
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<td><strong>MAIR_EL1</strong></td>
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<td><strong>MAIR_EL2</strong></td>
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<td><strong>MAIR_EL3</strong></td>
<td>Memory Attribute Indirection Register (EL3)</td>
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<td><strong>MDCCINT_EL1</strong></td>
<td>Monitor DCC Interrupt Enable Register</td>
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<td><strong>MDCCSR_EL0</strong></td>
<td>Monitor DCC Status Register</td>
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<td><strong>MDCR_EL2</strong></td>
<td>Monitor Debug Configuration Register (EL2)</td>
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<td><strong>MDCR_EL3</strong></td>
<td>Monitor Debug Configuration Register (EL3)</td>
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<tr>
<td><strong>MDRAR_EL1</strong></td>
<td>Monitor Debug ROM Address Register</td>
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<td><strong>MDSCR_EL1</strong></td>
<td>Monitor Debug System Control Register</td>
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<td><strong>MIDR_EL1</strong></td>
<td>Main ID Register</td>
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<td><strong>MPAM0_EL1</strong></td>
<td>MPAM0 Register (EL1)</td>
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<td><strong>MPAM1_EL1</strong></td>
<td>MPAM1 Register (EL1)</td>
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<td><strong>MPAM2_EL2</strong></td>
<td>MPAM2 Register (EL2)</td>
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<td><strong>MPAM3_EL3</strong></td>
<td>MPAM3 Register (EL3)</td>
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<td><strong>MPAMHCR_EL2</strong></td>
<td>MPAM Hypervisor Control Register (EL2)</td>
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<tr>
<td><strong>MPAMIDR_EL1</strong></td>
<td>MPAM ID Register (EL1)</td>
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<td><strong>MPAMVPM0_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 0</td>
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<td><strong>MPAMVPM1_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 1</td>
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<tr>
<td><strong>MPAMVPM2_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 2</td>
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<tr>
<td><strong>MPAMVPM3_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 3</td>
</tr>
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<td><strong>MPAMVPM4_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 4</td>
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<td><strong>MPAMVPM5_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 5</td>
</tr>
<tr>
<td><strong>MPAMVPM6_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 6</td>
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<td><strong>MPAMVPM7_EL2</strong></td>
<td>MPAM Virtual PARTID Mapping Register 7</td>
</tr>
<tr>
<td><strong>MPAMVPMV_EL2</strong></td>
<td>MPAM Virtual Partition Mapping Valid Register</td>
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</table>
MPIDR_EL1: Multiprocessor Affinity Register
MVFR0_EL1: AArch32 Media and VFP Feature Register 0
MVFR1_EL1: AArch32 Media and VFP Feature Register 1
MVFR2_EL1: AArch32 Media and VFP Feature Register 2
NZCV: Condition Flags
OSDLR_EL1: OS Double Lock Register
OSDTRRX_EL1: OS Lock Data Transfer Register, Receive
OSDTRTX_EL1: OS Lock Data Transfer Register, Transmit
OSECCR_EL1: OS Lock Exception Catch Control Register
OSLAR_EL1: OS Lock Access Register
OSLSR_EL1: OS Lock Status Register
PAN: Privileged Access Never
PAR_EL1: Physical Address Register
PMBIDR_EL1: Profiling Buffer ID Register
PMBLIMITR_EL1: Profiling Buffer Limit Address Register
PMBPTR_EL1: Profiling Buffer Write Pointer Register
PMBSR_EL1: Profiling Buffer Status/syndrome Register
PMCCFILTR_EL0: Performance Monitors Cycle Count Filter Register
PMCCNTR_EL0: Performance Monitors Cycle Count Register
PMCEID0_EL0: Performance Monitors Common Event Identification register 0
PMCEID1_EL0: Performance Monitors Common Event Identification register 1
PMCNTENCLR_EL0: Performance Monitors Count Enable Clear register
PMCNTENSET_EL0: Performance Monitors Count Enable Set register
PMCR_EL0: Performance Monitors Control Register
PMEVCNTR<n>_EL0: Performance Monitors Event Count Registers
PMEVTYPER<n>_EL0: Performance Monitors Event Type Registers
PMINTENCLR_EL1: Performance Monitors Interrupt Enable Clear register
PMINTENSET_EL1: Performance Monitors Interrupt Enable Set register
PMMIR_EL1: Performance Monitors Machine Identification Register
PMOVSCLR_EL0: Performance Monitors Overflow Flag Status Clear Register
PMOVSSET_EL0: Performance Monitors Overflow Flag Status Set register
PMSCLR_EL1: Statistical Profiling Control Register (EL1)
PMSCLR_EL2: Statistical Profiling Control Register (EL2)
PMSELR_EL0: Performance Monitors Event Counter Selection Register
PMSERV_EL1: Sampling Event Filter Register
PMSFCR_EL1: Sampling Filter Control Register
**AArch64 System Registers**

**PMSICR_EL1**: Sampling Interval Counter Register  
**PMSIDR_EL1**: Sampling Profiling ID Register  
**PMSIRR_EL1**: Sampling Interval Reload Register  
**PMSLATFR_EL1**: Sampling Latency Filter Register  
**PMSNEVFR_EL1**: Sampling Inverted Event Filter Register  
**PMSWINC_EL0**: Performance Monitors Software Increment register  
**PUSERENR_EL0**: Performance Monitors User Enable Register  
**PXMEVCNTR_EL0**: Performance Monitors Selected Event Count Register  
**PXMEVTYPER_EL0**: Performance Monitors Selected Event Type Register  
**REVIDR_EL1**: Revision ID Register  
**RGSR_EL1**: Random Allocation Tag Seed Register  
**RMR_EL1**: Reset Management Register (EL1)  
**RMR_EL2**: Reset Management Register (EL2)  
**RMR_EL3**: Reset Management Register (EL3)  
**RNDR**: Random Number  
**RNDRRS**: Reseeded Random Number  
**RVBAR_EL1**: Reset Vector Base Address Register (if EL2 and EL3 not implemented)  
**RVBAR_EL2**: Reset Vector Base Address Register (if EL3 not implemented)  
**RVBAR_EL3**: Reset Vector Base Address Register (if EL3 implemented)  
**S3_<op1>_<Cn>_<Cm>_<op2>**: IMPLEMENTATION DEFINED registers  
**SCR_EL3**: Secure Configuration Register  
**SCTLR_EL1**: System Control Register (EL1)  
**SCTLR_EL2**: System Control Register (EL2)  
**SCTLR_EL3**: System Control Register (EL3)  
**SCXTNUM_EL0**: EL0 Read/Write Software Context Number  
**SCXTNUM_EL1**: EL1 Read/Write Software Context Number  
**SCXTNUM_EL2**: EL2 Read/Write Software Context Number  
**SCXTNUM_EL3**: EL3 Read/Write Software Context Number  
**SDER32_EL2**: AArch32 Secure Debug Enable Register  
**SDER32_EL3**: AArch32 Secure Debug Enable Register  
**SPSel**: Stack Pointer Select  
**SPSR_abt**: Saved Program Status Register (Abort mode)  
**SPSR_EL1**: Saved Program Status Register (EL1)  
**SPSR_EL2**: Saved Program Status Register (EL2)  
**SPSR_EL3**: Saved Program Status Register (EL3)  
**SPSR_fiq**: Saved Program Status Register (FIQ mode)
SPSR_irq: Saved Program Status Register (IRQ mode)

SPSR_und: Saved Program Status Register (Undefined mode)

SP_EL0: Stack Pointer (EL0)

SP_EL1: Stack Pointer (EL1)

SP_EL2: Stack Pointer (EL2)

SP_EL3: Stack Pointer (EL3)

SSBS: Speculative Store Bypass Safe

TCO: Tag Check Override

TCR_EL1: Translation Control Register (EL1)

TCR_EL2: Translation Control Register (EL2)

TCR_EL3: Translation Control Register (EL3)

TFSRE0_EL1: Tag Fault Status Register (EL0)

TFSR_EL1: Tag Fault Status Register (EL1)

TFSR_EL2: Tag Fault Status Register (EL2)

TFSR_EL3: Tag Fault Status Register (EL3)

TPIDRRO_EL0: EL0 Read-Only Software Thread ID Register

TPIDR_EL0: EL0 Read/Write Software Thread ID Register

TPIDR_EL1: EL1 Software Thread ID Register

TPIDR_EL2: EL2 Software Thread ID Register

TPIDR_EL3: EL3 Software Thread ID Register

TRFCR_EL1: Trace Filter Control Register (EL1)

TRFCR_EL2: Trace Filter Control Register (EL2)

TTBR0_EL1: Translation Table Base Register 0 (EL1)

TTBR0_EL2: Translation Table Base Register 0 (EL2)

TTBR0_EL3: Translation Table Base Register 0 (EL3)

TTBR1_EL1: Translation Table Base Register 1 (EL1)

TTBR1_EL2: Translation Table Base Register 1 (EL2)

UAO: User Access Override

VBAR_EL1: Vector Base Address Register (EL1)

VBAR_EL2: Vector Base Address Register (EL2)

VBAR_EL3: Vector Base Address Register (EL3)

VDISR_EL2: Virtual Deferred Interrupt Status Register

VMPIDR_EL2: Virtualization Multiprocessor ID Register

VNCR_EL2: Virtual Nested Control Register

VPIDR_EL2: Virtualization Processor ID Register

VSESRR_EL2: Virtual SError Exception Syndrome Register
**VSTCR_EL2**: Virtualization Secure Translation Control Register

**VSTTBR_EL2**: Virtualization Secure Translation Table Base Register

**VTCR_EL2**: Virtualization Translation Control Register

**VTTBR_EL2**: Virtualization Translation Table Base Register

**ZCR_EL1**: SVE Control Register for EL1

**ZCR_EL2**: SVE Control Register for EL2

**ZCR_EL3**: SVE Control Register for EL3
AArch64 System Instructions

AT S12E0R: Address Translate Stages 1 and 2 EL0 Read
AT S12E0W: Address Translate Stages 1 and 2 EL0 Write
AT S12E1R: Address Translate Stages 1 and 2 EL1 Read
AT S12E1W: Address Translate Stages 1 and 2 EL1 Write
AT S1E0R: Address Translate Stage 1 EL0 Read
AT S1E0W: Address Translate Stage 1 EL0 Write
AT S1E1R: Address Translate Stage 1 EL1 Read
AT S1E1W: Address Translate Stage 1 EL1 Write
AT S1E1RP: Address Translate Stage 1 EL1 Read PAN
AT S1E1WP: Address Translate Stage 1 EL1 Write PAN
AT S1E2R: Address Translate Stage 1 EL2 Read
AT S1E2W: Address Translate Stage 1 EL2 Write
AT S1E3R: Address Translate Stage 1 EL3 Read
AT S1E3W: Address Translate Stage 1 EL3 Write

CFP RCTX: Control Flow Prediction Restriction by Context
CPP RCTX: Cache Prefetch Prediction Restriction by Context
DC CGDSW: Clean of Data and Allocation Tags by Set/Way
DC CGDVAC: Clean of Data and Allocation Tags by VA to PoC
DC CGDVADP: Clean of Data and Allocation Tags by VA to PoDP
DC CGDVAP: Clean of Data and Allocation Tags by VA to PoP
DC CGSW: Clean of Allocation Tags by Set/Way
DC CGVAC: Clean of Allocation Tags by VA to PoC
DC CGVADP: Clean of Allocation Tags by VA to PoDP
DC CGVAP: Clean of Allocation Tags by VA to PoP
DC CIGDSW: Clean and Invalidate of Data and Allocation Tags by Set/Way
DC CIGDVAC: Clean and Invalidate of Data and Allocation Tags by VA to PoC
DC CIGSW: Clean and Invalidate of Allocation Tags by Set/Way
DC CIGVAC: Clean and Invalidate of Allocation Tags by VA to PoC
DC CISW: Data or unified Cache line Clean and Invalidate by Set/Way
DC CVAC: Data or unified Cache line Clean and Invalidate by VA to PoC
DC CSW: Data or unified Cache line Clean by Set/Way
DC CVAP: Data or unified Cache line Clean by VA to PoP
**AArch64 System Instructions**

- **DC CVAU**: Data or unified Cache line Clean by VA to PoU
- **DC GVA**: Data Cache set Allocation Tag by VA
- **DC GZVA**: Data Cache set Allocation Tags and Zero by VA
- **DC IGDSW**: Invalidate of Data and Allocation Tags by Set/Way
- **DC IGDVAC**: Invalidate of Data and Allocation Tags by VA to PoC
- **DC IGSW**: Invalidate of Allocation Tags by Set/Way
- **DC IGVAC**: Invalidate of Allocation Tags by VA to PoC
- **DC ISW**: Data or unified Cache line Invalidate by Set/Way
- **DC IVAC**: Data or unified Cache line Invalidate by VA to PoC
- **DC ZVA**: Data Cache Zero by VA
- **DVP RCTX**: Data Value Prediction Restriction by Context
- **IC IALLU**: Instruction Cache Invalidate All to PoU
- **IC IALLUIS**: Instruction Cache Invalidate All to PoU, Inner Shareable
- **IC IVAU**: Instruction Cache line Invalidate by VA to PoU
- **SYS S1_<op1>_<Cn>_<Cm>_<op2>, SYSL S1_<op1>_<Cn>_<Cm>_<op2>**: IMPLEMENTATION DEFINED
- **maintenance instructions**
- **TLBI ALLE1, TLBI ALLE1NXS**: TLB Invalidate All, EL1
- **TLBI ALLE1IS, TLBI ALLE1ISNXS**: TLB Invalidate All, EL1, Inner Shareable
- **TLBI ALLE1OS, TLBI ALLE1OSNXS**: TLB Invalidate All, EL1, Outer Shareable
- **TLBI ALLE2, TLBI ALLE2NXS**: TLB Invalidate All, EL2
- **TLBI ALLE2IS, TLBI ALLE2ISNXS**: TLB Invalidate All, EL2, Inner Shareable
- **TLBI ALLE2OS, TLBI ALLE2OSNXS**: TLB Invalidate All, EL2, Outer Shareable
- **TLBI ALLE3, TLBI ALLE3NXS**: TLB Invalidate All, EL3
- **TLBI ALLE3IS, TLBI ALLE3ISNXS**: TLB Invalidate All, EL3, Inner Shareable
- **TLBI ALLE3OS, TLBI ALLE3OSNXS**: TLB Invalidate All, EL3, Outer Shareable
- **TLBI ASIDE1, TLBI ASIDE1NXS**: TLB Invalidate by ASID, EL1
- **TLBI ASIDE1IS, TLBI ASIDE1ISNXS**: TLB Invalidate by ASID, EL1, Inner Shareable
- **TLBI ASIDE1OS, TLBI ASIDE1OSNXS**: TLB Invalidate by ASID, EL1, Outer Shareable
- **TLBI IPAS2E1, TLBI IPAS2E1NXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, EL1
- **TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable
- **TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable
- **TLBI IPAS2LE1, TLBI IPAS2LE1NXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1
- **TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable
- **TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS**: TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable
- **TLBI RIPAS2E1, TLBI RIPAS2E1NXS**: TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1
TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS: TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Inner Shareable

TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS: TLB Range Invalidate by Intermediate Physical Address, Stage 2, EL1, Outer Shareable

TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS: TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1

TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS: TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable

TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS: TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable

TLBI RVAAE1, TLBI RVAAE1NXS: TLB Range Invalidate by VA, All ASID, EL1

TLBI RVAAE1IS, TLBI RVAAE1ISNXS: TLB Range Invalidate by VA, All ASID, EL1, Inner Shareable

TLBI RVAAE1OS, TLBI RVAAE1OSNXS: TLB Range Invalidate by VA, All ASID, EL1, Outer Shareable

TLBI RVAAL1, TLBI RVALE1NXS: TLB Range Invalidate by VA, All ASID, Last level, EL1

TLBI RVAAL1IS, TLBI RVALE1ISNXS: TLB Range Invalidate by VA, All ASID, Last Level, EL1, Inner Shareable

TLBI RVALE1OS, TLBI RVALE1OSNXS: TLB Range Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable

TLBI RVAE1, TLBI RVAE1NXS: TLB Range Invalidate by VA, EL1

TLBI RVAE1IS, TLBI RVAE1ISNXS: TLB Range Invalidate by VA, EL1, Inner Shareable

TLBI RVAE1OS, TLBI RVAE1OSNXS: TLB Range Invalidate by VA, EL1, Outer Shareable

TLBI RVAE2, TLBI RVAE2NXS: TLB Range Invalidate by VA, EL2

TLBI RVAE2IS, TLBI RVAE2ISNXS: TLB Range Invalidate by VA, EL2, Inner Shareable

TLBI RVAE2OS, TLBI RVAE2OSNXS: TLB Range Invalidate by VA, EL2, Outer Shareable

TLBI RVAE3, TLBI RVAE3NXS: TLB Range Invalidate by VA, EL3

TLBI RVAE3IS, TLBI RVAE3ISNXS: TLB Range Invalidate by VA, EL3, Inner Shareable

TLBI RVAE3OS, TLBI RVAE3OSNXS: TLB Range Invalidate by VA, EL3, Outer Shareable

TLBI RVALE1, TLBI RVALE1NXS: TLB Range Invalidate by VA, Last level, EL1

TLBI RVALE1IS, TLBI RVALE1ISNXS: TLB Range Invalidate by VA, Last level, EL1, Inner Shareable

TLBI RVALE1OS, TLBI RVALE1OSNXS: TLB Range Invalidate by VA, Last level, EL1, Outer Shareable

TLBI RVALE2, TLBI RVALE2NXS: TLB Range Invalidate by VA, Last level, EL2

TLBI RVALE2IS, TLBI RVALE2ISNXS: TLB Range Invalidate by VA, Last level, EL2, Inner Shareable

TLBI RVALE2OS, TLBI RVALE2OSNXS: TLB Range Invalidate by VA, Last level, EL2, Outer Shareable

TLBI RVALE3, TLBI RVALE3NXS: TLB Range Invalidate by VA, Last level, EL3

TLBI RVALE3IS, TLBI RVALE3ISNXS: TLB Range Invalidate by VA, Last level, EL3, Inner Shareable

TLBI RVALE3OS, TLBI RVALE3OSNXS: TLB Range Invalidate by VA, Last level, EL3, Outer Shareable

TLBI VAAE1, TLBI VAAE1NXS: TLB Invalidate by VA, All ASID, EL1

TLBI VAAE1IS, TLBI VAAE1ISNXS: TLB Invalidate by VA, All ASID, EL1, Inner Shareable

TLBI VAAE1OS, TLBI VAAE1OSNXS: TLB Invalidate by VA, All ASID, EL1, Outer Shareable

TLBI VAAL1, TLBI VAAL1NXS: TLB Invalidate by VA, All ASID, Last level, EL1

TLBI VAAL1IS, TLBI VAAL1ISNXS: TLB Invalidate by VA, All ASID, Last Level, EL1, Inner Shareable

TLBI VAAL1OS, TLBI VAAL1OSNXS: TLB Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable
TLBI VALE1OS, TLBI VALE1OSNXS: TLB Invalidate by VA, All ASID, Last Level, EL1, Outer Shareable
TLBI VAE1, TLBI VAE1NXS: TLB Invalidate by VA, EL1
TLBI VAE1IS, TLBI VAE1ISNXS: TLB Invalidate by VA, EL1, Inner Shareable
TLBI VAE1OS, TLBI VAE1OSNXS: TLB Invalidate by VA, EL1, Outer Shareable
TLBI VAE2, TLBI VAE2NXS: TLB Invalidate by VA, EL2
TLBI VAE2IS, TLBI VAE2ISNXS: TLB Invalidate by VA, EL2, Inner Shareable
TLBI VAE2OS, TLBI VAE2OSNXS: TLB Invalidate by VA, EL2, Outer Shareable
TLBI VAE3, TLBI VAE3NXS: TLB Invalidate by VA, EL3
TLBI VAE3IS, TLBI VAE3ISNXS: TLB Invalidate by VA, EL3, Inner Shareable
TLBI VAE3OS, TLBI VAE3OSNXS: TLB Invalidate by VA, EL3, Outer Shareable
TLBI VALE1, TLBI VALE1NXS: TLB Invalidate by VA, Last level, EL1
TLBI VALE1IS, TLBI VALE1ISNXS: TLB Invalidate by VA, Last level, EL1, Inner Shareable
TLBI VALE1OS, TLBI VALE1OSNXS: TLB Invalidate by VA, Last level, EL1, Outer Shareable
TLBI VALE2, TLBI VALE2NXS: TLB Invalidate by VA, Last level, EL2
TLBI VALE2IS, TLBI VALE2ISNXS: TLB Invalidate by VA, Last level, EL2, Inner Shareable
TLBI VALE2OS, TLBI VALE2OSNXS: TLB Invalidate by VA, Last level, EL2, Outer Shareable
TLBI VALE3, TLBI VALE3NXS: TLB Invalidate by VA, Last level, EL3
TLBI VALE3IS, TLBI VALE3ISNXS: TLB Invalidate by VA, Last level, EL3, Inner Shareable
TLBI VALE3OS, TLBI VALE3OSNXS: TLB Invalidate by VA, Last level, EL3, Outer Shareable
TLBI VMALLE1, TLBI VMALLE1NXS: TLB Invalidate by VMID, All at stage 1, EL1
TLBI VMALLE1IS, TLBI VMALLE1ISNXS: TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
TLBI VMALLE1OS, TLBI VMALLE1OSNXS: TLB Invalidate by VMID, All at stage 1, EL1, Outer Shareable
TLBI VMALLS12E1, TLBI VMALLS12E1NXS: TLB Invalidate by VMID, All at Stage 1 and 2, EL1
TLBI VMALLS12E1IS, TLBI VMALLS12E1ISNXS: TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Inner Shareable
TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS: TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Outer Shareable
ACCDATA_EL1, Accelerator Data

The ACCDATA_EL1 characteristics are:

**Purpose**

Holds the lower 32 bits of the data that is stored by an ST64BV0, Single-copy atomic 64-byte EL0 store instruction.

**Configuration**

This register is present only when FEAT_LS64_ACCDATA is implemented. Otherwise, direct accesses to ACCDATA_EL1 are UNDEFINED.

**Attributes**

ACCDATA_EL1 is a 64-bit register.

**Field descriptions**

The ACCDATA_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit (63:32)</th>
<th>Bit (31:0)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0</td>
<td>ACCDATA</td>
</tr>
</tbody>
</table>

- **Bits [63:32]**
  - Reserved, RES0.

- **ACCDATA, bits [31:0]**
  - Accelerator Data field. Holds bits[31:0] of the data that is stored by an ST64BV0 instruction.

**Accessing the ACCDATA_EL1**

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ ACCDATA_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ADEn == '0' then
    UNDEFINED;
  elsif EL2Enabled() && ((HaveEL(EL3) && SCR_EL3.FGTEn == '0') || HFGWTR_EL2.nACCDATA_EL1 == '0') then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && SCR_EL3.ADEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ACCDATA_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ADEn == '0' then
    UNDEFINED;
  elseif HaveEL(EL3) && SCR_EL3.ADEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ACCDATA_EL1;
  end
elsif PSTATE.EL == EL3 then
  return ACCDATA_EL1;
end

MSR ACCDATA_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ADEn == '0' then
    UNDEFINED;
  elsif EL2Enabled() && ((HaveEL(EL3) && SCR_EL3.FGTEn == '0') || HFGWTR_EL2.nACCDATA_EL1 == '0') then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && SCR_EL3.ADEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ACCDATA_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ADEn == '0' then
    UNDEFINED;
  elseif HaveEL(EL3) && SCR_EL3.ADEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ACCDATA_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  ACCDATA_EL1 = X[t];
ACTLR_EL1, Auxiliary Control Register (EL1)

The ACTLR_EL1 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED configuration and control options for execution at EL1 and EL0.

**Note**

Arm recommends the contents of this register have no effect on the PE when \( \text{HCR\_EL2.\{E2H, TGE\}} \) is \{1, 1\}, and instead the configuration and control fields are provided by the ACTLR_EL2 register. This avoids the need for software to manage the contents of these register when switching between a Guest OS and a Host OS.

**Configuration**

AArch64 System register ACTLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register \( \text{ACTLR[31:0]} \).

AArch64 System register ACTLR_EL1 bits [63:32] are architecturally mapped to AArch32 System register \( \text{ACTLR2[31:0]} \).

**Attributes**

ACTLR_EL1 is a 64-bit register.

**Field descriptions**

The ACTLR_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | IMPLEMENTATION DEFINED |

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   | IMPLEMENTATION DEFINED |

**IMPLEMENTATION DEFINED, bits [63:0]**

**IMPLEMENTATION DEFINED.**

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ACTLR_EL1**

Accesses to this register use the following encodings:

\[ \text{MRS \langle Xt\rangle, ACTLR\_EL1} \]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TACR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    return NVMem[0x118];
  else
    return ACTLR_EL1;
  endif
elsif PSTATE.EL == EL2 then
  return ACTLR_EL1;
elsif PSTATE.EL == EL3 then
  return ACTLR_EL1;
endif

MSR ACTLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TACR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    NVMem[0x118] = X[t];
  else
    ACTLR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  ACTLR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  ACTLR_EL1 = X[t];
endif
The ACTLR_EL2 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED configuration and control options for EL2.

**Note**

Arm recommends the contents of this register are updated to apply to EL0 when HCR_EL2.{E2H, TGE} is {1, 1}, gaining configuration and control fields from the ACTLR_EL1. This avoids the need for software to manage the contents of these register when switching between a Guest OS and a Host OS.

**Configuration**

AArch64 System register ACTLR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HACTLR[31:0].

AArch64 System register ACTLR_EL2 bits [63:32] are architecturally mapped to AArch32 System register HACTLR2[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ACTLR_EL2 is a 64-bit register.

**Field descriptions**

The ACTLR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
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<td>57</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>47</td>
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<tr>
<td>46</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
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<td>45</td>
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<td>1</td>
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<td>0</td>
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**IMPLEMENTATION DEFINED, bits [63:0]**

- IMPLEMENTATION DEFINED.
- On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ACTLR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, ACTLR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return ACTLR_EL2;
elsif PSTATE.EL == EL3 then
    return ACTLR_EL2;

MSR ACTLR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    ACTLR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    ACTLR_EL2 = X[t];
ACTLR_EL3, Auxiliary Control Register (EL3)

The ACTLR_EL3 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED configuration and control options for EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to ACTLR_EL3 are UNDEFINED.

**Attributes**

ACTLR_EL3 is a 64-bit register.

**Field descriptions**

The ACTLR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ACTLR_EL3**

Accesses to this register use the following encodings:

**MRS <Xt>, ACTLR_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
  return ACTLR_EL3;

**MSR ACTLR_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    ACTLR_EL3 = X[t];
AFSR0_EL1, Auxiliary Fault Status Register 0 (EL1)

The AFSR0_EL1 characteristics are:

Purpose

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL1.

Configuration

AArch64 System register AFSR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ADFSR[31:0].

Attributes

AFSR0_EL1 is a 64-bit register.

Field descriptions

The AFSR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
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<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
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</table>

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the AFSR0_EL1

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic AFSR0_EL1 or AFSR0_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, AFSR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AFSR0_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x128];
    else
        return AFSR0_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return AFSR0_EL2;
    else
        return AFSR0_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return AFSR0_EL1;
end if;

MSR AFSR0_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AFSR0_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x128] = X[t];
    else
        AFSR0_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AFSR0_EL2 = X[t];
    else
        AFSR0_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    AFSR0_EL1 = X[t];
end if;

MRS <Xt>, AFSR0_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x128];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return AFSR0_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return AFSR0_EL1;
    else
        UNDEFINED;

MSR AFSR0_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
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<td>0b101</td>
<td>0b0101</td>
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<td>0b000</td>
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</tbody>
</table>

MSR AFSR0_EL0, <Xt>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x128] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AFSR0_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        AFSR0_EL1 = X[t];
    else
        UNDEFINED;
AFSR0_EL2, Auxiliary Fault Status Register 0 (EL2)

The AFSR0_EL2 characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL2.

**Configuration**

AArch64 System register AFSR0_EL2 bits [31:0] are architecturally mapped to AArch32 System register HADFSR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

AFSR0_EL2 is a 64-bit register.

**Field descriptions**

The AFSR0_EL2 bit assignments are:

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<th>Bit</th>
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<tr>
<td>8</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>7</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>6</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>5</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>4</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>3</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>2</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>1</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AFSR0_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic AFSR0_EL2 or AFSR0_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, AFSR0_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return AFSR0_EL2;
elsif PSTATE.EL == EL3 then
  return AFSR0_EL2;

MSR AFSR0_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AFSR0_EL1 == '1'
then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
  return NVMem[0x128];
else
  return AFSR0_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return AFSR0_EL2;
  else
    return AFSR0_EL1;
eslif PSTATE.EL == EL3 then
  return AFSR0_EL1;

MSR AFSR0_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  AFSR0_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  AFSR0_EL2 = X[t];

MRS <Xt>, AFSR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AFSR0_EL1 == '1'
then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
  return NVMem[0x128];
else
  return AFSR0_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return AFSR0_EL2;
  else
    return AFSR0_EL1;
eslif PSTATE.EL == EL3 then
  return AFSR0_EL1;

MSR AFSR0_EL1, <Xt>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AFSR0_EL1 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x128] = X[t];
    else
        AFSR0_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AFSR0_EL2 = X[t];
    else
        AFSR0_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    AFSR0_EL1 = X[t];
AFSR0_EL3, Auxiliary Fault Status Register 0 (EL3)

The AFSR0_EL3 characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to AFSR0_EL3 are UNDEFINED.

**Attributes**

AFSR0_EL3 is a 64-bit register.

**Field descriptions**

The AFSR0_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>61</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>60</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>59</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>58</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>57</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>56</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>55</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>54</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>53</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>52</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>51</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>50</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>49</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>48</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>47</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>46</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>44</td>
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<tr>
<td>42</td>
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<td>41</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>39</td>
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<td>37</td>
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<td>36</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>35</td>
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<td>34</td>
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<tr>
<td>19</td>
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<tr>
<td>18</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>17</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>16</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>12</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>11</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>10</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>9</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>8</td>
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<tr>
<td>7</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>6</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>5</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>4</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>3</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>2</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>1</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

If PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
return AFSR0_EL3;

**Accessing the AFSR0_EL3**

Accesses to this register use the following encodings:

MRS <Xt>, AFSR0_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
return AFSR0_EL3;

MSR AFSR0_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    AFSR0_EL3 = X[t];
AFSR1_EL1, Auxiliary Fault Status Register 1 (EL1)

The AFSR1_EL1 characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL1.

**Configuration**

AArch64 System register AFSR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register $AIFS[31:0]$.

**Attributes**

AFSR1_EL1 is a 64-bit register.

**Field descriptions**

The AFSR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AFSR1_EL1**

When $HCR_{EL2}.E2H$ is 1, without explicit synchronization, access from EL3 using the mnemonic AFSR1_EL1 or AFSR1_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS \langle Xt \rangle, AFSR1_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AFSR1_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return AFSR1_EL1;
  end
elsif PSTATE.EL == EL2 then
  if EL2Enabled() && HCR_EL2.E2H == '1' then
    return AFSR1_EL2;
  elseif PSTATE.EL == EL3 then
    return AFSR1_EL1;
end

MSR AFSR1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AFSR1_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AFSR1_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    AFSR1_EL2 = X[t];
  elseif AFSR1_EL1 == X[t];
elsif PSTATE.EL == EL3 then
  AFSR1_EL1 = X[t];

MRS <Xt>, AFSR1_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x130];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return AFSR1_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return AFSR1_EL1;
  else
    UNDEFINED;

MSR AFSR1_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x130] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    AFSR1_EL1 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    AFSR1_EL1 = X[t];
  else
    UNDEFINED;
AFSR1_EL2, Auxiliary Fault Status Register 1 (EL2)

The AFSR1_EL2 characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL2.

**Configuration**

AArch64 System register AFSR1_EL2 bits [31:0] are architecturally mapped to AArch32 System register HAIFSR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

AFSR1_EL2 is a 64-bit register.

**Field descriptions**

The AFSR1_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AFSR1_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic AFSR1_EL2 or AFSR1_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, AFSR1_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return AFSR1_EL2;
elsif PSTATE.EL == EL3 then
  return AFSR1_EL2;

MSR AFSR1_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  AFSR1_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  AFSR1_EL2 = X[t];

MRS <Xt>, AFSR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AFSR1_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x130];
  else
    return AFSR1_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return AFSR1_EL2;
  else
    return AFSR1_EL1;
elsif PSTATE.EL == EL3 then
  return AFSR1_EL1;

MSR AFSR1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AFSR1_EL1 == '1'
        then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x130] = X[t];
    else
        AFSR1_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AFSR1_EL2 = X[t];
    else
        AFSR1_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    AFSR1_EL1 = X[t];
AFSR1_EL3, Auxiliary Fault Status Register 1 (EL3)

The AFSR1_EL3 characteristics are:

Purpose

Provides additional IMPLEMENTATION DEFINED fault status information for exceptions taken to EL3.

Configuration

This register is present only when EL3 is implemented. Otherwise, direct accesses to AFSR1_EL3 are UNDEFINED.

Attributes

AFSR1_EL3 is a 64-bit register.

Field descriptions

The AFSR1_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the AFSR1_EL3

Accesses to this register use the following encodings:

MRS <Xt>, AFSR1_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return AFSR1_EL3;

MSR AFSR1_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    AFSR1_EL3 = X[t];
AIDR_EL1, Auxiliary ID Register

The AIDR_EL1 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED identification information.

The value of this register must be interpreted in conjunction with the value of MIDR_EL1.

**Configuration**

AArch64 System register AIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register AIDR[31:0].

**Attributes**

AIDR_EL1 is a 64-bit register.

**Field descriptions**

The AIDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-60</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>59-56</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>55-50</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>49-46</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>45-40</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>39-36</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>35-32</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

**IMPLEMENTATION DEFINED.**

**Accessing the AIDR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, AIDR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.AIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return AIDR_EL1;
elsif PSTATE.EL == EL2 then
  return AIDR_EL1;
elsif PSTATE.EL == EL3 then
  return AIDR_EL1;
AMAIR_EL1, Auxiliary Memory Attribute Indirection Register (EL1)

The AMAIR_EL1 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED memory attributes for the memory regions specified by AMAIR_EL1.

**Configuration**

AArch64 System register AMAIR_EL1 bits [31:0] are architecturally mapped to AArch32 System register AMAIR0[31:0].

AArch64 System register AMAIR_EL1 bits [63:32] are architecturally mapped to AArch32 System register AMAIR1[31:0].

**Attributes**

AMAIR_EL1 is a 64-bit register.

**Field descriptions**

The AMAIR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED, bits [63:0] |

AMAIR_EL1 is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AMAIR_EL1**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic AMAIR_EL1 or AMAIR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, AMAIR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AMAIR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x148];
    else
        return AMAIR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return AMAIR_EL2;
    else
        return AMAIR_EL1;
    end
elsif PSTATE.EL == EL3 then
    return AMAIR_EL1;
end

MSR AMAIR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AMAIR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x148] = X[t];
    else
        AMAIR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AMAIR_EL2 = X[t];
    else
        AMAIR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    AMAIR_EL1 = X[t];
end

MRS <Xt>, AMAIR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x148];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return AMAIR_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return AMAIR_EL1;
    else
        UNDEFINED;
else
    UNDEFINED;

MSR AMAIR_EL12, <Xt>  

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x148];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        AMAIR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        AMAIR_EL1 = X[t];
    else
        UNDEFINED;
AMAIR_EL2, Auxiliary Memory Attribute Indirection Register (EL2)

The AMAIR_EL2 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED memory attributes for the memory regions specified by MAIR_EL2.

**Configuration**

AArch64 System register AMAIR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HAMAIR0[31:0].

AArch64 System register AMAIR_EL2 bits [63:32] are architecturally mapped to AArch32 System register HAMAIR1[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

AMAIR_EL2 is a 64-bit register.

**Field descriptions**

The AMAIR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

AMAIR_EL2 is permitted to be cached in a TLB.

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AMAIR_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic AMAIR_EL2 or AMAIR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, AMAIR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if $\text{PSTATE.EL} == \text{EL0}$ then 
    UNDEFINED;
elsif $\text{PSTATE.EL} == \text{EL1}$ then
    if $\text{EL2Enabled}() \&\& \text{HCR_EL2.NV} == '1'$ then
        AArch64.SystemAccessTrap($\text{EL2}, 0x10$);
    else
        UNDEFINED;
    elsif $\text{PSTATE.EL} == \text{EL2}$ then
        return AMAIR_EL2;
    elsif $\text{PSTATE.EL} == \text{EL3}$ then
        return AMAIR_EL2;
    end if

MSR AMAIR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if $\text{PSTATE.EL} == \text{EL0}$ then 
    UNDEFINED;
elsif $\text{PSTATE.EL} == \text{EL1}$ then
    if $\text{EL2Enabled}() \&\& \text{HCR_EL2.NV} == '1'$ then
        AArch64.SystemAccessTrap($\text{EL2}, 0x10$);
    else
        UNDEFINED;
    elsif $\text{PSTATE.EL} == \text{EL2}$ then
        AMAIR_EL2 = X[t];
    elsif PSTATE.EL == EL3 then
        AMAIR_EL2 = X[t];
    end if

MRS <Xt>, AMAIR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if $\text{PSTATE.EL} == \text{EL0}$ then 
    UNDEFINED;
elsif $\text{PSTATE.EL} == \text{EL1}$ then
    if $\text{EL2Enabled}() \&\& \text{HCR_EL2.TRVM} == '1'$ then
        AArch64.SystemAccessTrap($\text{EL2}, 0x10$);
    elsif $\text{EL2Enabled}() \&\& (!\text{HaveEL(EL3)} || \text{SCR_EL3.FGTEn} == '1') \&\& \text{HFGRTR_EL2.AMAIR_EL1} == '1'$ then
        AArch64.SystemAccessTrap($\text{EL2}, 0x10$);
    elsif $\text{EL2Enabled}() \&\& \text{HCR_EL2.<NV2,NV1,NV>} == '111'$ then
        return NVMem[0x148];
    else
        return AMAIR_EL1;
    end if
elsif $\text{PSTATE.EL} == \text{EL2}$ then
    if $\text{HCR_EL2.E2H} == '1'$ then
        return AMAIR_EL2;
    else
        return AMAIR_EL1;
    end if
elsif PSTATE.EL == EL3 then
    return AMAIR_EL1;

MSR AMAIR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.AMAIR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x148] = X[t];
  else
    AMAIR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    AMAIR_EL2 = X[t];
  else
    AMAIR_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  AMAIR_EL1 = X[t];
AMAIR_EL3, Auxiliary Memory Attribute Indirection Register (EL3)

The AMAIR_EL3 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED memory attributes for the memory regions specified by AMAIR_EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to AMAIR_EL3 are UNDEFINED.

**Attributes**

AMAIR_EL3 is a 64-bit register.

**Field descriptions**

The AMAIR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
</tbody>
</table>

AMAIR_EL3 is permitted to be cached in a TLB.

**IMPLEMENTATION DEFINED, bits [63:0]**

All bits are IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AMAIR_EL3**

Accesses to this register use the following encodings:

\[
\text{MRS } \langle X_t \rangle, \text{ AMAIR_EL3}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return AMAIR_EL3;
### MSR AMAIR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   UNDEFINED;
elsif PSTATE.EL == EL2 then
   UNDEFINED;
elsif PSTATE.EL == EL3 then
   AMAIR_EL3 = X[t];
```
AMCFGR_EL0, Activity Monitors Configuration Register

The AMCFGR_EL0 characteristics are:

**Purpose**

Global configuration register for the activity monitors.

Provides information on supported features, the number of counter groups implemented, the total number of activity monitor event counters implemented, and the size of the counters. AMCFGR_EL0 is applicable to both the architectured and the auxiliary counter groups.

**Configuration**

AArch64 System register AMCFGR_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCFGR[31:0].

AArch64 System register AMCFGR_EL0 bits [31:0] are architecturally mapped to External register AMCFGR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCFGR_EL0 are UNDEFINED.

**Attributes**

AMCFGR_EL0 is a 64-bit register.

**Field descriptions**

The AMCFGR_EL0 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| NCG | RES0| HDBG| RAZ | SIZE| N   |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:32]**

Reserved, RES0.

**NCG, bits [31:28]**

Defines the number of counter groups.

The number of implemented counter groups is defined as [AMCFGR_EL0.NCG + 1].

If the number of implemented auxiliary activity monitor event counters is zero, this field has a value of 0b0000. Otherwise, this field has a value of 0b0001.

**Bits [27:25]**

Reserved, RES0.

**HDBG, bit [24]**

Halt-on-debug supported.

From Armv8, this feature must be supported, and so this bit is 0b1.
### Bits [23:14]

Reserved, RAZ.

### SIZE, bits [13:8]

Defines the size of activity monitor event counters.

The size of the activity monitor event counters implemented by the activity monitors Extension is defined as $[\text{AMCFGR\_EL0.\text{SIZE}} + 1]$. From Armv8, the counters are 64-bit, and so this field is `0b111111`.

Note

Software also uses this field to determine the spacing of counters in the memory-map. From Armv8, the counters are at doubleword-aligned addresses.

### N, bits [7:0]

Defines the number of activity monitor event counters.

The total number of counters implemented in all groups by the Activity Monitors Extension is defined as $[\text{AMCFGR\_EL0.\text{N}} + 1]$. 

### Accessing the AMCFGR\_EL0

Accesses to this register use the following encodings:

**MRS <Xt>, AMCFGR\_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      return AMCFGR_EL0;
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return AMCFGR_EL0;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return AMCFGR_EL0;
  end if
elsif PSTATE.EL == EL3 then
  return AMCFGR_EL0;
end if
AMCG1IDR_EL0, Activity Monitors Counter Group 1 Identification Register

The AMCG1IDR_EL0 characteristics are:

**Purpose**

Defines which auxiliary counters are implemented, and which of them have a corresponding virtual offset register, AMEVCNTOFF1<n>_EL2 implemented.

**Configuration**

This register is present only when FEAT_AMUv1p1 is implemented. Otherwise, direct accesses to AMCG1IDR_EL0 are UNDEFINED.

**Attributes**

AMCG1IDR_EL0 is a 64-bit register.

**Field descriptions**

The AMCG1IDR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>31-20</td>
<td>AMEVCNTOFF115_EL2</td>
<td>AMEVCNTOFF114_EL2 AMEVCNTOFF113_EL2 AMEVCNTOFF112_EL2 AMEVCNTOFF111_EL2</td>
</tr>
<tr>
<td>19-8</td>
<td>AMEVCNTOFF110_EL2</td>
<td>AMEVCNTOFF111_EL2 AMEVCNTOFF110_EL2 AMEVCNTOFF111_EL2 AMEVCNTOFF110_EL2</td>
</tr>
<tr>
<td>7-0</td>
<td>AMEVCNTR115_EL0</td>
<td>AMEVCNTR114_EL0 AMEVCNTR113_EL0 AMEVCNTR112_EL0 AMEVCNTR111_EL0</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**AMEVCNTOFF1<n>_EL2, bit [n+16], for n = 15 to 0**

Indicates which implemented auxiliary counters have a corresponding virtual offset register, AMEVCNTOFF1<n>_EL2 implemented.

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, mean that AMEVCNTR1&lt;n&gt;_EL0 does not have an offset, or is not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the offset AMEVCNTOFF1&lt;n&gt;_EL2 is implemented for AMEVCNTR1&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

**AMEVCNTR1<n>_EL0, bit [n], for n = 15 to 0**

Indicates which auxiliary counters AMEVCNTR1<n>_EL0 are implemented.

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is implemented.</td>
</tr>
</tbody>
</table>
Accessing the AMCG1IDR_EL0

Accesses to this register use the following encodings:

\[ \text{MRS} \langle X_t \rangle, \text{AMCG1IDR_EL0} \]

\[
\begin{array}{c|c|c|c|c}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b11 & 0b01l & 0b1101 & 0b0010 & 0b110 \\
\end{array}
\]

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    endif
else
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    return AMCG1IDR_EL0;
endif

elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    endif
else
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    return AMCG1IDR_EL0;
endif

elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    return AMCG1IDR_EL0;
endif

elsif PSTATE.EL == EL3 then
    return AMCG1IDR_EL0;
endif
The AMCGCR_EL0 characteristics are:

**Purpose**

Provides information on the number of activity monitor event counters implemented within each counter group.

**Configuration**

AArch64 System register AMCGCR_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCGCR[31:0].

AArch64 System register AMCGCR_EL0 bits [31:0] are architecturally mapped to External register AMCGCR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCGCR_EL0 are UNDEFINED.

**Attributes**

AMCGCR_EL0 is a 64-bit register.

**Field descriptions**

The AMCGCR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>RES0</th>
<th>CG1NC</th>
<th>CG0NC</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:16</td>
<td>RES0</td>
<td>CG1NC</td>
<td>CG0NC</td>
</tr>
<tr>
<td>31:0</td>
<td>RES0</td>
<td>CG1NC</td>
<td>CG0NC</td>
</tr>
</tbody>
</table>

**Bits [63:16]**

Reserved, RES0.

**CG1NC, bits [15:8]**

Counter Group 1 Number of Counters. The number of counters in the auxiliary counter group.

In an implementation that includes FEAT_AMUv1, the permitted range of values is 0x0 to 0x10.

**CG0NC, bits [7:0]**

Counter Group 0 Number of Counters. The number of counters in the architected counter group.

In an implementation that includes FEAT_AMUv1, the value of this field is 0x4.

**Accessing the AMCGCR_EL0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return AMCGCR_EL0;
    end if
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return AMCGCR_EL0;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return AMCGCR_EL0;
    end if
elsif PSTATE.EL == EL3 then
    return AMCGCR_EL0;
end if
The AMCNTENCLR0_EL0 characteristics are:

**Purpose**

Disable control bits for the architected activity monitors event counters, AMEVCTR0<n>_EL0.

**Configuration**

AArch64 System register AMCNTENCLR0_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENCLR0[31:0].

AArch64 System register AMCNTENCLR0_EL0 bits [31:0] are architecturally mapped to External register AMCNTENCLR0[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR0_EL0 are UNDEFINED.

**Attributes**

AMCNTENCLR0_EL0 is a 64-bit register.

**Field descriptions**

The AMCNTENCLR0_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-16</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15-0</td>
<td>P&lt;n&gt;</td>
<td>Activity monitor event counter disable bit for AMEVCTR0&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR_EL0.CG0NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCTR0&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCTR0&lt;n&gt;_EL0 is enabled. When written, disables AMEVCTR0&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENCLR0_EL0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      return AMCNTENCLR0_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return AMCNTENCLR0_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return AMCNTENCLR0_EL0;
  end
elsif PSTATE.EL == EL3 then
  return AMCNTENCLR0_EL0;
end

MR <Xt>, AMCNTENCLR0_EL0

if IsHighestEL(PSTATE.EL) then
  AMCNTENCLR0_EL0 = X[t];
else
  UNDEFINED;
end
AMCNTENCLR1_EL0, Activity Monitors Count Enable Clear Register 1

The AMCNTENCLR1_EL0 characteristics are:

**Purpose**

Disable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>_EL0.

**Configuration**

AArch64 System register AMCNTENCLR1_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENCLR1[31:0].

AArch64 System register AMCNTENCLR1_EL0 bits [31:0] are architecturally mapped to External register AMCNTENCLR1[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR1_EL0 are UNDEFINED.

**Attributes**

AMCNTENCLR1_EL0 is a 64-bit register.

**Field descriptions**

The AMCNTENCLR1_EL0 bit assignments are:

```
+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+--------+
| 63     | 62     | 61     | 60     | 59     | 58     | 57     | 56     | 55     | 54     | 53     | 52     | 51     | 50     | 49     |
| RES0   | RES0   |        |        |        |        |        |        |        |        |        |        |        |        |        |
| 48     | 47     | 46     | 45     | 44     | 43     | 42     | 41     | 40     | 39     | 38     | 37     | 36     | 35     | 34     |
|        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
| 33     | 32     | 31     | 30     | 29     | 28     | 27     | 26     | 25     | 24     | 23     | 22     | 21     | 20     | 19     |
|        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
| 18     | 17     | 16     | 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      | 7      | 6      | 5      | 4      |
|        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
| 3       | 2       | 1       | 0       |
```

Bits [63:16]

Reserved, RES0.

P<n>, bit [n], for n = 15 to 0

Activity monitor event counter disable bit for AMEVCNTR1<n>_EL0.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR_EL0.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is enabled. When written, disables AMEVCNTR1&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENCLR1_EL0**

If the number of auxiliary activity monitor event counters implemented is zero, reads and writes of AMCNTENCLR1_EL0 are UNDEFINED.
The number of auxiliary activity monitor event counters implemented is zero exactly when `AMCPGR_EL0.NCG == 0b0000`. 

Accesses to this register use the following encodings:

**MRS <Xt>, AMCNTENCLR1_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    else
        // More conditions...
        return AMCNTENCLR1_EL0;
    end
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        // More conditions...
        return AMCNTENCLR1_EL0;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        // More conditions...
        return AMCNTENCLR1_EL0;
    end
elsif PSTATE.EL == EL3 then
    return AMCNTENCLR1_EL0;
end
```
if IsHighestEL(PSTATE.EL) then
  AMCNTENCLR1_EL0 = X[t];
else
  UNDEFINED;
The AMCNTENSET0_EL0 characteristics are:

**Purpose**

Enable control bits for the architected activity monitors event counters, \texttt{AMEVCNTR0\:<n>_EL0}.  

**Configuration**

AArch64 System register AMCNTENSET0_EL0 bits [31:0] are architecturally mapped to AArch32 System register 
\texttt{AMCNTENSET0[31:0]}.  

AArch64 System register AMCNTENSET0_EL0 bits [31:0] are architecturally mapped to External register 
\texttt{AMCNTENSET0[31:0]}.  

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET0_EL0 are UNDEFINED.  

**Attributes**

AMCNTENSET0_EL0 is a 64-bit register.  

**Field descriptions**

The AMCNTENSET0_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
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<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>RES0</td>
<td>RES0</td>
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<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:16]**

Reserved, RES0.  

**P\:<n>, bit \:[n], for \:n = 15 to 0**

Activity monitor event counter enable bit for \texttt{AMEVCNTR0\:<n>_EL0}.  

Bits [31:16] are RES0. Bits [15:0] are RAZ/WI. N is the value in \texttt{AMCGCR_EL0.CG0NC}.  

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P:&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00b</td>
<td>When read, means that \texttt{AMEVCNTR0:&lt;n&gt;_EL0} is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>01b</td>
<td>When read, means that \texttt{AMEVCNTR0:&lt;n&gt;_EL0} is enabled. When written, enables \texttt{AMEVCNTR0:&lt;n&gt;_EL0}.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.  

**Accessing the AMCNTENSET0_EL0**

Accesses to this register use the following encodings:
MRS <Xt>, AMCNTENSET0_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && CR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && CR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL2.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return AMCNTENSET0_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return AMCNTENSET0_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return AMCNTENSET0_EL0;
  end
elsif PSTATE.EL == EL3 then
  return AMCNTENSET0_EL0;
endif

MSR AMCNTENSET0_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if IsHighestEL(PSTATE.EL) then
  AMCNTENSET0_EL0 = <Xt>;
else
  UNDEFINED;
AMCNTENSET1_EL0, Activity Monitors Count Enable Set Register 1

The AMCNTENSET1_EL0 characteristics are:

**Purpose**

Enable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>_EL0.

**Configuration**

AArch64 System register AMCNTENSET1_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENSET1[31:0].

AArch64 System register AMCNTENSET1_EL0 bits [31:0] are architecturally mapped to External register AMCNTENSET1[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET1_EL0 are UNDEFINED.

**Attributes**

AMCNTENSET1_EL0 is a 64-bit register.

**Field descriptions**

The AMCNTENSET1_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | P15 | P14 | P13 | P12 | P11 | P10 | P9  | P8  | P7  | P6  | P5  | P4  | P3  | P2  | P1  | P0  |

**Bits [63:16]**

Reserved, RES0.

**P<n>, bit [n], for n = 15 to 0**

Activity monitor event counter enable bit for AMEVCNTR1<n>_EL0.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR_EL0.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt;_EL0 is enabled. When written, enables AMEVCNTR1&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENSET1_EL0**

If the number of auxiliary activity monitor event counters implemented is zero, reads and writes of AMCNTENSET1_EL0 are UNDEFINED.
The number of auxiliary activity monitor counters implemented is zero when 
**AMCFGR_EL0**.NCG == 0b0000.

Accesses to this register use the following encodings:

MRS <Xt>, **AMCNTENSET1_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HAFGRTR_EL2.AMCNTEN1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTEN1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    end if
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    end if
    return AMCNTENSET1_EL0;
  elsif PSTATE.EL == EL3 then
    return AMCNTENSET1_EL0;
  else
    return AMCNTENSET1_EL0;
  end if

AArch64.SystemAccessTrap(EL3, 0x18);
MSR AMCNTENSET1_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if IsHighestEL(PSTATE.EL) then
  AMCNTENSET1_EL0 = X[t];
else
  UNDEFINED;

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The AMCR_EL0 characteristics are:

**Purpose**

Global control register for the activity monitors implementation. AMCR_EL0 is applicable to both the architectured and the auxiliary counter groups.

**Configuration**

AArch64 System register AMCR_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMCR[31:0].

AArch64 System register AMCR_EL0 bits [31:0] are architecturally mapped to External register AMCR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCR_EL0 are UNDEFINED.

**Attributes**

AMCR_EL0 is a 64-bit register.

**Field descriptions**

The AMCR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>CG1RZ</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>60</td>
<td>HDBG</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>57</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0.</td>
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<td>54</td>
<td>Reserved, RES0.</td>
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<td>53</td>
<td>Reserved, RES0.</td>
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<td>52</td>
<td>Reserved, RES0.</td>
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<td>51</td>
<td>Reserved, RES0.</td>
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<td>50</td>
<td>Reserved, RES0.</td>
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<tr>
<td>49</td>
<td>Reserved, RES0.</td>
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<tr>
<td>48</td>
<td>Reserved, RES0.</td>
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<td>47</td>
<td>Reserved, RES0.</td>
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<td>46</td>
<td>Reserved, RES0.</td>
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<td>45</td>
<td>Reserved, RES0.</td>
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<td>44</td>
<td>Reserved, RES0.</td>
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<tr>
<td>43</td>
<td>Reserved, RES0.</td>
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<tr>
<td>42</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, RES0.</td>
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<tr>
<td>40</td>
<td>Reserved, RES0.</td>
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<tr>
<td>39</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [63:18]**

Reserved, RES0.

**CG1RZ, bit [17]**

*When FEAT_AMUv1p1 is implemented:*

Counter Group 1 Read Zero.

<table>
<thead>
<tr>
<th>CG1RZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>System register reads of AMEVCNTR1&lt;n&gt;_EL0 return the event count at all implemented and enabled Exception levels.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the current Exception level is the highest implemented Exception level, system register reads of AMEVCNTR1&lt;n&gt;_EL0 return the event count. Otherwise, reads of AMEVCNTR1&lt;n&gt;_EL0 return a zero value.</td>
</tr>
</tbody>
</table>

**Note**

Reads from the memory-mapped view are unaffected by this field.

**Otherwise:**

Reserved, RES0.
Bits [16:11]

Reserved, RES0.

HDBG, bit [10]

This bit controls whether activity monitor counting is halted when the PE is halted in Debug state.

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Activity monitors do not halt counting when the PE is halted in Debug state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Activity monitors halt counting when the PE is halted in Debug state.</td>
</tr>
</tbody>
</table>

Bits [9:0]

Reserved, RES0.

Accessing the AMCR_EL0

Accesses to this register use the following encodings:

MRS <Xt>, AMCR_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elseif AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        if EL2Enabled() && CPTR_EL2.TAM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        elseif PSTATE.EL == EL1 then
            if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
                UNDEFINED;
            elseif EL2Enabled() && CPTR_EL2.TAM == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        else
            return AMCR_EL0;
        endif
    else
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elseif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        else
            return AMCR_EL0;
        endif
    else
        if IsHighestEL(PSTATE.EL) then
            AMCR_EL0 = X[t];
        else
            UNDEFINED;
        endif
    endif
else
    return AMCR_EL0;
endif

MSR AMCR_EL0, <Xt>
AMEVCNTR0<n>_EL0, Activity Monitors Event Counter Registers 0, n = 0 - 15

The AMEVCNTR0<n>_EL0 characteristics are:

**Purpose**

Provides access to the architected activity monitor event counters.

**Configuration**

AArch64 System register AMEVCNTR0<n>_EL0 bits [63:0] are architecturally mapped to AArch32 System register AMEVCNTR0<n>[63:0].

AArch64 System register AMEVCNTR0<n>_EL0 bits [63:0] are architecturally mapped to External register AMEVCNTR0<n>[63:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR0<n>_EL0 are UNDEFINED.

**Attributes**

AMEVCNTR0<n>_EL0 is a 64-bit register.

**Field descriptions**

The AMEVCNTR0<n>_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ACNT | ACNT |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**ACNT, bits [63:0]**

Architected activity monitor event counter n.

Value of architected activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If FEAT_AMUv1p1 is implemented, HCR_EL2.AMVOFFEN is 1, SCR_EL3.AMVOFFEN is 1, HCR_EL2.(E2H, TGE) is not {1,1}, and EL2 is implemented in the current Security state, access to these registers at EL0 or EL1 return (PCount<63:0> - AMEVCNTVOFF0<n>_EL2<63:0>).

PCount is the physical count returned when AMEVCNTR0<n>_EL0 is read from EL2 or EL3.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

**Accessing the AMEVCNTR0<n>_EL0**

If <n> is greater than or equal to the number of architected activity monitor event counters, reads and writes of AMEVCNTR0<n>_EL0 are UNDEFINED.

---

**Note**
**AMEVCNTR0<n>_EL0**, Activity Monitors Event Counter Registers 0, n = 0 - 15

**AMCGCR_EL0**. CG0NC identifies the number of architected activity monitor event counters.

**Accesses to this register use the following encodings:**

**MRS <Xt>, AMEVCNTR0<n>_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b010:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        if EL2Enabled() && CPTR_EL2.TAM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && CPTR_EL2.TAM != '1' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
            HAFGRTR_EL2.AMEVCNTR0<n>_EL0 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        end;
    endif
else
    return AMEVCNTR0_EL0[UInt(CRm<0>:op2<2:0>)];
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elseif EL2Enabled() && CPTR_EL2.TAM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
            HAFGRTR_EL2.AMEVCNTR0<n>_EL0 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        end;
    else
        return AMEVCNTR0_EL0[UInt(CRm<0>:op2<2:0>)];
    end;
else
    if PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elseif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            endif
        end:
    else
        return AMEVCNTR0_EL0[UInt(CRm<0>:op2<2:0>)];
    end;
else
    return AMEVCNTR0_EL0[UInt(CRm<0>:op2<2:0>)];
end;
```

**MSR AMEVCNTR0<n>_EL0, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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</tbody>
</table>
if IsHighestEL(PSTATE.EL) then
       AMEVCNTR0_EL0[UInt(CRm<0>:op2<2:0>)] = X[t];
else
       UNDEFINED;
AMEVCNTR1<n>._EL0, Activity Monitors Event Counter Registers 1, n = 0 - 15

The AMEVCNTR1<n>._EL0 characteristics are:

Purpose

Provides access to the auxiliary activity monitor event counters.

Configuration

AArch64 System register AMEVCNTR1<n>._EL0 bits [63:0] are architecturally mapped to AArch32 System register AMEVCNTR1<n>._EL0.

AArch64 System register AMEVCNTR1<n>._EL0 bits [63:0] are architecturally mapped to External register AMEVCNTR1<n>._EL0.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR1<n>._EL0 are UNDEFINED.

Attributes

AMEVCNTR1<n>._EL0 is a 64-bit register.

Field descriptions

The AMEVCNTR1<n>._EL0 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
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</tbody>
</table>

ACNT, bits [63:0]

Auxiliary activity monitor event counter n.

Value of auxiliary activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If FEAT_AMUv1p1 is implemented, HCR_EL2.AMVOFFEN is 1, SCR_EL3.AMVOFFEN is 1, HCR_EL2.{E2H, TGE} is not {1,1}, EL2 is implemented in the current Security state, and AMCR_EL0.CG1RZ is 0, reads to these registers at EL0 or EL1 return (PCount<63:0> - AMEVCNTRVOFF1<n>._EL2<63:0>).

PCount is the physical count returned when AMEVCNTR1<n>._EL0 is read from EL2 or EL3.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

Accessing the AMEVCNTR1<n>._EL0

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads and writes of AMEVCNTR1<n>._EL0 are UNDEFINED.

Note
AMCGCR_EL0 identifies the number of auxiliary activity monitor event counters.

Accesses to this register use the following encodings:

MRS <Xt>, AMEVCNTR1<n>_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b110:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMEVCNTR1<n>_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    elsif AMCR_EL0.CG1RZ == '1' then
      return Zeros();
    else
      return AMEVCNTR1_EL0[UInt(CRm<0>:op2<2:0>)];
    end
    elsif PSTATE.EL == EL1 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
      elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMEVCNTR1<n>_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.SystemAccessTrap(EL3, 0x18);
        end
      elsif !IsHighestEL(PSTATE.EL) && AMCR_EL0.CG1RZ == '1' then
        return Zeros();
      else
        return AMEVCNTR1_EL0[UInt(CRm<0>:op2<2:0>)];
      end
    elsif PSTATE.EL == EL2 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
      elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.SystemAccessTrap(EL3, 0x18);
        end
      elsif !IsHighestEL(PSTATE.EL) && AMCR_EL0.CG1RZ == '1' then
        return Zeros();
      else
        return AMEVCNTR1_EL0[UInt(CRm<0>:op2<2:0>)];
      end
    elsif PSTATE.EL == EL3 then
      return AMEVCNTR1_EL0[UInt(CRm<0>:op2<2:0>)];
  else
    MSR AMEVCNTR1<n>_EL0, Activity Monitors Event Counter Registers 1, n = 0 - 15

    | op0 | op1 | CRn | CRm | op2 |
    |-----|-----|-----|-----|-----|
    | 0b11 | 0b011 | 0b1101 | 0b110:n[3] | n[2:0] |

    if IsHighestEL(PSTATE.EL) then
      AMEVCNTR1_EL0[UInt(CRm<0>:op2<2:0>)] = X[t];
    else
      UNDEFINED;
AMEVCNTVOFF0<n>_EL2, Activity Monitors Event Counter Virtual Offset Registers 0, n = 0 - 15

The AMEVCNTVOFF0<n>_EL2 characteristics are:

**Purpose**

Holds the 64-bit virtual offset for architected activity monitor events.

**Configuration**

This register is present only when FEAT_AMUv1p1 is implemented. Otherwise, direct accesses to AMEVCNTVOFF0<n>_EL2 are **UNDEFINED**.

**Attributes**

AMEVCNTVOFF0<n>_EL2 is a 64-bit register.

**Field descriptions**

The AMEVCNTVOFF0<n>_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td><strong>Virtual offset</strong></td>
</tr>
<tr>
<td>31</td>
<td><strong>Virtual offset</strong></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual offset.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the AMEVCNTVOFF0<n>_EL2**

If <n> is not 0, 2 or 3, reads and writes of AMEVCNTVOFF0<n>_EL2 are **UNDEFINED**.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b100:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '1' then
        return NVMem[0xA00+8*UInt(CRm<0>:op2<2:0>)];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
else
    PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.AMVOFFEN == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.AMVOFFEN == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        elif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            return AMEVCNTVOFF0_EL2[UInt(CRm<0>:op2<2:0>)];
        end
    elsif PSTATE.EL == EL3 then
        return AMEVCNTVOFF0_EL2[UInt(CRm<0>:op2<2:0>)];
    end

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '1' then
        NVMem[0xA00+8*UInt(CRm<0>:op2<2:0>)] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
else
    PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.AMVOFFEN == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.AMVOFFEN == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        elif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AMEVCNTVOFF0_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
        end
    elsif PSTATE.EL == EL3 then
        AMEVCNTVOFF0_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
AMEVCNTVOFF1<n>_EL2, Activity Monitors Event Counter Virtual Offset Registers 1, n = 0 - 15

The AMEVCNTVOFF1<n>_EL2 characteristics are:

**Purpose**

Holds the 64-bit virtual offset for auxiliary activity monitor events.

**Configuration**

This register is present only when FEAT_AMUV1p1 is implemented. Otherwise, direct accesses to AMEVCNTVOFF1<n>_EL2 are **UNDEFINED**.

**Attributes**

AMEVCNTVOFF1<n>_EL2 is a 64-bit register.

**Field descriptions**

The AMEVCNTVOFF1<n>_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
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</tbody>
</table>

**Virtual offset**

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the AMEVCNTVOFF1<n>_EL2**

**Note**

AMECG1IDR_EL0 identifies which auxiliary activity monitor event counters have a corresponding virtual offset implemented.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b101:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0xA80+8*UInt(CRm<0>:op2<2:0>)];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.AMVOFFEN == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.AMVOFFEN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end if;
else
  return AMEVCNTVOFF1_EL2[UInt(CRm<0>:op2<2:0>)];
end if;

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0xA80+8*UInt(CRm<0>:op2<2:0>)] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.AMVOFFEN == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.AMVOFFEN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end if;
else
  AMEVCNTVOFF1_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
end if;
elsif PSTATE.EL == EL3 then
  AMEVCNTVOFF1_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
AMEVTYPER0<n>_EL0, Activity Monitors Event Type Registers 0, n = 0 - 15

The AMEVTYPER0<n>_EL0 characteristics are:

Purpose

Provides information on the events that an architected activity monitor event counter AMEVCNTR0<n>_EL0 counts.

Configuration

AArch64 System register AMEVTYPER0<n>_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMEVTYPER0<n>[31:0].

AArch64 System register AMEVTYPER0<n>_EL0 bits [31:0] are architecturally mapped to External register AMEVTYPER0<n>[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER0<n>_EL0 are undefined.

Attributes

AMEVTYPER0<n>_EL0 is a 64-bit register.

Field descriptions

The AMEVTYPER0<n>_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | evtCount |

Bits [63:16]

Reserved, RES0.

evtCount, bits [15:0]

Event to count. The event number of the event that is counted by the architected activity monitor event counter AMEVCNTR0<n>_EL0. The value of this field is architecturally mandated for each architected counter.

The following table shows the mapping between required event numbers and the corresponding counters:

<table>
<thead>
<tr>
<th>evtCount</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x8011</td>
<td>Processor frequency cycles</td>
<td>When n == 0</td>
</tr>
<tr>
<td>0x4004</td>
<td>Constant frequency cycles</td>
<td>When n == 1</td>
</tr>
<tr>
<td>0x4008</td>
<td>Instructions retired</td>
<td>When n == 2</td>
</tr>
<tr>
<td>0x4005</td>
<td>Memory stall cycles</td>
<td>When n == 3</td>
</tr>
</tbody>
</table>

Accessing the AMEVTYPER0<n>_EL0

If <n> is greater than or equal to the number of architected activity monitor event counters, reads and writes of AMEVTYPER0<n>_EL0 are undefined.

Note
AMEVTYPER0\langle n \rangle\_EL0, Activity Monitors Event Type Registers 0, n = 0 - 15

AMCGCR\_EL0.CG0NC identifies the number of architected activity monitor event counters.

Accesses to this register use the following encodings:

MRS <Xt>, AMEVTYPER0\langle n \rangle\_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm:n[3]</th>
<th>op2:n[2:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b011:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
    if Halted() && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return AMEVTYPER0\_EL0[UInt(CRm<0>:op2<2:0>)];
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return AMEVTYPER0\_EL0[UInt(CRm<0>:op2<2:0>)];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return AMEVTYPER0\_EL0[UInt(CRm<0>:op2<2:0>)];
  end if
elsif PSTATE.EL == EL3 then
  return AMEVTYPER0\_EL0[UInt(CRm<0>:op2<2:0>)];
else
  return AMEVTYPER0\_EL0[UInt(CRm<0>:op2<2:0>)];
end if

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AMEVTYPE1<n>_EL0, Activity Monitors Event Type Registers 1, n = 0 - 15

The AMEVTYPE1<n>_EL0 characteristics are:

**Purpose**

Provides information on the events that an auxiliary activity monitor event counter AMEVCNTR1<n>_EL0 counts.

**Configuration**

AArch64 System register AMEVTYPE1<n>_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMEVTYPE1<n>[31:0].

AArch64 System register AMEVTYPE1<n>_EL0 bits [31:0] are architecturally mapped to External register AMEVTYPE1<n>[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPE1<n>_EL0 are UNDEFINED.

**Attributes**

AMEVTYPE1<n>_EL0 is a 64-bit register.

**Field descriptions**

The AMEVTYPE1<n>_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | evtCount |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:16]**

Reserved, RES0.

**evtCount, bits [15:0]**

Event to count. The event number of the event that is counted by the auxiliary activity monitor event counter AMEVCNTR1<n>_EL0.

It is IMPLEMENTATION DEFINED what values are supported by each counter.

If software writes a value to this field which is not supported by the corresponding counter AMEVCNTR1<n>_EL0, then:

- It is UNPREDICTABLE which event will be counted.
- The value read back is UNKNOWN.

The event counted by AMEVCNTR1<n>_EL0 might be fixed at implementation. In this case, the field is read-only and writes are UNDEFINED.

If the corresponding counter AMEVCNTR1<n>_EL0 is enabled, writes to this register have UNPREDICTABLE results.
Accessing the AMEVTYPER1<n>_EL0

If \(<n>\) is greater than or equal to the number of auxiliary activity monitor event counters, reads and writes of AMEVTYPER1<n>_EL0 are UNDEFINED.

**Note**

AMEVTYPER1<n>_EL0 identifies the number of auxiliary activity monitor event counters.

Accesses to this register use the following encodings:

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b011 & 0b1101 & 0b111:n[3] & n[2:0] \\
\hline
\end{array}
\]
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMEVTYPER1<n>_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMEVTYPER1<n>_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      return AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      return AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif PSTATE.EL == EL3 then
    return AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return AMEVTYPER1_EL0[UInt(CRm<0>:op2<2:0>)];
  end
end

if IsHighestEL(PSTATE.EL) && !boolean IMPLEMENTATION_DEFINED "AMEVCNTR1<n>_EL0 is fixed" then
  AMEVTYPER1_EL0[UInt(CRm<0>:op2<2:0>)] = X[t];
else
  UNDEFINED;

MSR AMEVTYPER1<n>_EL0, <Xt>
The AMUSERENR_EL0 characteristics are:

**Purpose**

Global user enable register for the activity monitors. Enables or disables EL0 access to the activity monitors. AMUSERENR_EL0 is applicable to both the architected and the auxiliary counter groups.

**Configuration**

AArch64 System register AMUSERENR_EL0 bits [31:0] are architecturally mapped to AArch32 System register AMUSERENR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMUSERENR_EL0 are UNDEFINED.

**Attributes**

AMUSERENR_EL0 is a 64-bit register.

**Field descriptions**

The AMUSERENR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
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<tr>
<td>0</td>
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</tr>
</tbody>
</table>

**Bits [63:1]**

Reserved, RES0.

**EN, bit [0]**

Traps EL0 accesses to the activity monitors registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, as follows:

- In AArch64 state, accesses to the following registers are trapped, reported using EC syndrome value 0x18:
  - AMCFG_ELO, AMCGCR_ELO, AMCNTENCLR0_ELO, AMCNTENCLR1_ELO, AMCNTENSET0_ELO, AMCNTENSET1_ELO, AMCR_ELO, AMEVCTR0<_n>_EL0, AMEVCTR1<_n>_EL0, AMEVTPR0<_n>_EL0, and AMEVTPR1<_n>_EL0.

- In AArch32 state, MRC and MCR accesses to the following registers are trapped and reported using EC syndrome value 0x03, MRRC and MCRR accesses are trapped and reported using EC syndrome value 0x04:
  - AMCFG, AMCGCR, AMCNTENCLR0, AMCNTENCLR1, AMCNTENSET0, AMCNTENSET1, AMCR, AMEVCTR0<_n>, AMEVCTR1<_n>, AMEVTPR0<_n>, and AMEVTPR1<_n>.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the activity monitors registers are trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped. Software can access all activity monitor registers at EL0.</td>
</tr>
</tbody>
</table>

**Note**
• AMUSERENR_EL0 can always be read at EL0 and is not governed by this bit.

**Accessing the AMUSERENR_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, AMUSERENR_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return AMUSERENR_EL0;
    end
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return AMUSERENR_EL0;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return AMUSERENR_EL0;
    end
elsif PSTATE.EL == EL3 then
    return AMUSERENR_EL0;
else
    return AMUSERENR_EL0;
end

MSR AMUSERENR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
elif EL2Enabled() && CPTR_EL2.TAM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
eelif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
eelse
        AArch64.SystemAccessTrap(EL3, 0x18);
eelse
    AMUSERENR_EL0 = X[t];
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TAM == '1' then
        UNDEFINED;
elif HaveEL(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
eelse
        AArch64.SystemAccessTrap(EL3, 0x18);
eelse
    AMUSERENR_EL0 = X[t];
elif PSTATE.EL == EL3 then
    AMUSERENR_EL0 = X[t];
APDAKeyHi_EL1, Pointer Authentication Key A for Data (bits[127:64])

The APDAKeyHi_EL1 characteristics are:

**Purpose**

Holds bits[127:64] of key A used for authentication of data pointer values.

**Note**

The term APDAKey_EL1 is used to describe the concatenation of APDAKeyHi_EL1 : APDAKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APDAKeyHi_EL1 are UNDEFINED.

**Attributes**

APDAKeyHi_EL1 is a 64-bit register.

**Field descriptions**

The APDAKeyHi_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value on a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[127:64] of the 128 bit pointer authentication key value.

Accessing the APDAKeyHi_EL1

Accesses to this register use the following encodings:

MRS <Xt>, APDAKeyHi_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APDAKeyHi_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return APDAKeyHi_EL1;
  endif
elsif PSTATE.EL == EL3 then
  return APDAKeyHi_EL1;
endif

MSR APDAKeyHi_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return APDAKeyHi_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return APDAKeyHi_EL1;
  endif
elsif PSTATE.EL == EL3 then
  return APDAKeyHi_EL1;
endif
APDKeyHi_EL1, Pointer Authentication Key A for Data (bits[127:64])
The APDAKeyLo_EL1 characteristics are:

**Purpose**

Holds bits[63:0] of key A used for authentication of data pointer values.

**Note**

The term APDAKey_EL1 is used to describe the concatenation of APDAKeyHi_EL1: APDAKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APDAKeyLo_EL1 are UNDEFINED.

**Attributes**

APDAKeyLo_EL1 is a 64-bit register.

**Field descriptions**

The APDAKeyLo_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>31</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[63:0] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APDAKeyLo_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
delayed priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.APK == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDAKey == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return APDAKeyLo_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
delayed priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        APDAKeyLo_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    APDAKeyLo_EL1 = X[t];
else
    APDAKeyLo_EL1 = X[t];
end if;

MSR APDAKeyLo_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
APDBKeyHi_EL1, Pointer Authentication Key B for Data (bits[127:64])

The APDBKeyHi_EL1 characteristics are:

**Purpose**

Holds bits[127:64] of key B used for authentication of data pointer values.

**Note**

The term APDBKey_EL1 is used to describe the concatenation of APDBKeyHi_EL1: APDBKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APDBKeyHi_EL1 are UNDEFINED.

**Attributes**

APDBKeyHi_EL1 is a 64-bit register.

**Field descriptions**

The APDBKeyHi_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>31</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[127:64] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APDBKeyHi_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return APDBKeyHi_EL1;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return APDBKeyHi_EL1;
  end if;
elif PSTATE.EL == EL3 then
  return APDBKeyHi_EL1;
end if;

MSR APDBKeyHi_EL1, <Xt>
APDBKeyLo_EL1, Pointer Authentication Key B for Data (bits[63:0])

The APDBKeyLo_EL1 characteristics are:

**Purpose**

Holds bits[63:0] of key B used for authentication of data pointer values.

**Note**

The term APDBKey_EL1 is used to describe the concatenation of APDBKeyHi_EL1: APDBKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APDBKeyLo_EL1 are UNDEFINED.

**Attributes**

APDBKeyLo_EL1 is a 64-bit register.

**Field descriptions**

The APDBKeyLo_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-62</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>61-32</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[63:0] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APDBKeyLo_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS</th>
<th>APDBKeyLo_EL1</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APDBKeyLo_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APDBKeyLo_EL1;
  end
elsif PSTATE.EL == EL3 then
  return APDBKeyLo_EL1;
endif

MSR APDBKeyLo_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APDBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    APDBKeyLo_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    APDBKeyLo_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  APDBKeyLo_EL1 = X[t];
APDBKeyLo_EL1, Pointer Authentication Key B for Data (bits[63:0])
The APGAKeyHi_EL1 characteristics are:

**Purpose**

Holds bits[127:64] of key used for generic pointer authentication code.

**Note**

The term APGAKey_EL1 is used to describe the concatenation of APGAKeyHi_EL1: APGAKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APGAKeyHi_EL1 are UNDEFINED.

**Attributes**

APGAKeyHi_EL1 is a 64-bit register.

**Field descriptions**

The APGAKeyHi_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>62</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[127:64] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APGAKeyHi_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, APGAKeyHi_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.APK == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && !HaveEL(EL3) || SCR_EL3.FGTEn == '1' && HFGWTR_EL2.APGAKey == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return APGAKeyHi_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        APGAKeyHi_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    APGAKeyHi_EL1 = X[t];
else
    PSTATE.EL = EL3 then
    APGAKeyHi_EL1 = X[t];
end if;

MSR APGAKeyHi_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.APK == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && !HaveEL(EL3) || SCR_EL3.FGTEn == '1' && HFGWTR_EL2.APGAKey == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return APGAKeyHi_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        APGAKeyHi_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    APGAKeyHi_EL1 = X[t];
else
    APGAKeyHi_EL1 = X[t];
end if;
APGAKeyHi_EL1, Pointer Authentication Key A for Code (bits[127:64])
**APGAKeyLo_EL1, Pointer Authentication Key A for Code (bits[63:0])**

The APGAKeyLo_EL1 characteristics are:

**Purpose**

Holds bits[63:0] of key used for generic pointer authentication code.

**Note**

The term APGAKey_EL1 is used to describe the concatenation of APGAKeyHi_EL1: APGAKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APGAKeyLo_EL1 are UNDEFINED.

**Attributes**

APGAKeyLo_EL1 is a 64-bit register.

**Field descriptions**

The APGAKeyLo_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

64 bit value, bits[63:0] of the 128 bit pointer authentication key value

64 bit value, bits[63:0] of the 128 bit pointer authentication key value

**Bits [63:0]**

64 bit value, bits[63:0] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APGAKeyLo_EL1**

Accesses to this register use the following encodings:

\[ MRS <Xt>, APGAKeyLo_EL1 \]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.APK == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APGAKey == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return APGAKeyLo_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        APGAKeyLo_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    APGAKeyLo_EL1 = X[t];
else
    APGAKeyLo_EL1 = X[t];
end

MSR APGAKeyLo_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elseif EL2Enabled() && HCR_EL2.APK == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APGAKey == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        elseif
            AArch64.SystemAccessTrap(EL3, 0x18);
        elseif
            APGAKeyLo_EL1 = X[t];
        elseif
            APGAKeyLo_EL1 = X[t];
        else
            APGAKeyLo_EL1 = X[t];
        end
    else
        APGAKeyLo_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && SCR_EL3.APK == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        elseif
            AArch64.SystemAccessTrap(EL3, 0x18);
        elseif
            APGAKeyLo_EL1 = X[t];
        elseif
            APGAKeyLo_EL1 = X[t];
        else
            APGAKeyLo_EL1 = X[t];
        end
    else
        APGAKeyLo_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    APGAKeyLo_EL1 = X[t];
APGAKeyLo_EL1, Pointer Authentication Key A for Code (bits[63:0])
The APIAKeyHi_EL1 characteristics are:

**Purpose**

Holds bits[127:64] of key A used for authentication of instruction pointer values.

**Note**

The term APIAKey_EL1 is used to describe the concatenation of
APIAKeyHi_EL1: APIAKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APIAKeyHi_EL1 are UNDEFINED.

**Attributes**

APIAKeyHi_EL1 is a 64-bit register.

**Field descriptions**

The APIAKeyHi_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| 64 bit value, bits[127:64] of the 128 bit pointer authentication key value |
| 64 bit value, bits[127:64] of the 128 bit pointer authentication key value |

**Bits [63:0]**

64 bit value, bits[127:64] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APIAKeyHi_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, APIAKeyHi_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIAKeyHi_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIAKeyHi_EL1;
elsif PSTATE.EL == EL3 then
    return APIAKeyHi_EL1;
else
    MSR APIAKeyHi_EL1, <Xt>
end if

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    APIAKeyHi_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    APIAKeyHi_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    APIAKeyHi_EL1 = X[t];
else
    APIAKeyHi_EL1 = X[t];
**APIAKeyLo_EL1, Pointer Authentication Key A for Instruction (bits[63:0])**

The APIAKeyLo_EL1 characteristics are:

**Purpose**

Holds bits[63:0] of key A used for authentication of instruction pointer values.

**Note**

The term APIAKey_EL1 is used to describe the concatenation of `APIAKeyHi_EL1: APIAKeyLo_EL1`.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APIAKeyLo_EL1 are UNDEFINED.

**Attributes**

APIAKeyLo_EL1 is a 64-bit register.

**Field descriptions**

The APIAKeyLo_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>31</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[63:0] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APIAKeyLo_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, APIAKeyLo_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIAKeyLo_EL1;
else
  return APIAKeyLo_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIAKeyLo_EL1;
else
  return APIAKeyLo_EL1;
elsif PSTATE.EL == EL3 then
  return APIAKeyLo_EL1;

MSR APIAKeyLo_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIAKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIAKeyLo_EL1;
else
  return APIAKeyLo_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      return APIAKeyLo_EL1;
else
  return APIAKeyLo_EL1;
else
  return APIAKeyLo_EL1;
APIBKeyHi_EL1, Pointer Authentication Key B for Instruction (bits[127:64])

The APIBKeyHi_EL1 characteristics are:

**Purpose**

Holds bits[127:64] of key B used for authentication of instruction pointer values.

**Note**

The term APIBKey_EL1 is used to describe the concatenation of APIBKeyHi_EL1: APIBKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APIBKeyHi_EL1 are UNDEFINED.

**Attributes**

APIBKeyHi_EL1 is a 64-bit register.

**Field descriptions**

The APIBKeyHi_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>62</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>61</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>60</td>
<td>Bits [63:0]</td>
</tr>
<tr>
<td>59</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>58</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>57</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>56</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>55</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>54</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>53</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>52</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>51</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>50</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>49</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>48</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>47</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>46</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>45</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>44</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>43</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>42</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>41</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>40</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>39</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>38</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>37</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>36</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>35</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>34</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>33</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>32</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>31</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>30</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>29</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>28</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>27</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>26</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>25</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>24</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>23</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>22</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>21</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>20</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>19</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>18</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>17</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>16</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>15</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>14</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>13</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>12</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>11</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>10</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>9</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>8</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>7</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>6</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>5</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>4</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>3</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>2</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>1</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>0</td>
<td>64 bit value, bits[127:64] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

64 bit value, bits[127:64] of the 128 bit pointer authentication key value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APIBKeyHi_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, APIBKeyHi_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIBKeyHi_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIBKeyHi_EL1;
  end
elsif PSTATE.EL == EL3 then
  return APIBKeyHi_EL1;
endif

MSR APIBKeyHi_EL1, <Xt>

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>CRn</th>
<th>CRm</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIBKeyHi_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return APIBKeyHi_EL1;
  end
elsif PSTATE.EL == EL3 then
  return APIBKeyHi_EL1;
endif
APIBKeyHi_EL1, Pointer Authentication Key B for Instruction (bits[127:64])
APIBKeyLo_EL1, Pointer Authentication Key B for Instruction (bits[63:0])

The APIBKeyLo_EL1 characteristics are:

**Purpose**

Holds bits[63:0] of key B used for authentication of instruction pointer values.

**Note**

The term APIBKey_EL1 is used to describe the concatenation of APIBKeyHi_EL1: APIBKeyLo_EL1.

**Configuration**

This register is present only when FEAT_PAuth is implemented. Otherwise, direct accesses to APIBKeyLo_EL1 are UNDEFINED.

**Attributes**

APIBKeyLo_EL1 is a 64-bit register.

**Field descriptions**

The APIBKeyLo_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>64 bit value, bits[63:0] of the 128 bit pointer authentication key value</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the APIBKeyLo_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, APIBKeyLo_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIBKeyLo_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIBKeyLo_EL1;
elsif PSTATE.EL == EL3 then
    return APIBKeyLo_EL1;
else
    APIBKeyLo_EL1 = X[t];
end if

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif EL2Enabled() && HCR_EL2.APK == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.APIBKey == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIBKeyLo_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.APK == '0' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.APK == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
else
    return APIBKeyLo_EL1;
elsif PSTATE.EL == EL3 then
    return APIBKeyLo_EL1;
else
    APIBKeyLo_EL1 = X[t];
end if

MSR APIBKeyLo_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
AT S12E0R, Address Translate Stages 1 and 2 EL0 Read

The AT S12E0R characteristics are:

**Purpose**

Performs stage 1 and 2 address translations from EL0, with permissions as if reading from the given virtual address from EL0, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the EL2&0 translation regime.
- Otherwise, the EL1&0 translation regime.

**Configuration**

There are no configuration notes.

**Attributes**

AT S12E0R is a 64-bit System instruction.

**Field descriptions**

The AT S12E0R input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Input address for translation</th>
<th>Input address for translation</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S12E0R instruction**

Accesses to this instruction use the following encodings:

AT S12E0R, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00' then
        AT_S1E0R(X[t]);
    else
        AT_S1E0R(X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        AT_S1E0R(X[t]);
    elsif EL2Enabled() && (HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00') then
        AT_S1E0R(X[t]);
    else
        AT_S1E0R(X[t]);
AT S12E0W, Address Translate Stages 1 and 2 EL0 Write

The AT S12E0W characteristics are:

**Purpose**

Performs stage 1 and 2 address translations from EL0, with permissions as if writing to the given virtual address from EL0, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2 {E2H, TGE} is not {1, 1}, the EL1&0 translation regime.
  - If HCR_EL2 {E2H, TGE} is {1, 1}, the EL2&0 translation regime.
- Otherwise, the EL1&0 translation regime.

**Configuration**

There are no configuration notes.

**Attributes**

AT S12E0W is a 64-bit System instruction.

**Field descriptions**

The AT S12E0W input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Input address for translation</th>
<th>Input address for translation</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S12E0W instruction**

Accesses to this instruction use the following encodings:

AT S12E0W, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00' then
    AT_S1E0W(X[t]);
  else
    AT_S12E0W(X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    AT_S1E0W(X[t]);
  elseif EL2Enabled() && (HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00') then
    AT_S1E0W(X[t]);
  else
    AT_S12E0W(X[t]);
AT S12E1R, Address Translate Stages 1 and 2 EL1 Read

The AT S12E1R characteristics are:

**Purpose**

Performs stage 1 and 2 address translation, with permissions as if reading from the given virtual address from EL1, or from EL2 if the Effective value of HCR_EL2.(E2H, TGE) is {1, 1}, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.(E2H, TGE) is not {1, 1}, the EL1&0 translation regime, accessed from EL1.
  - If HCR_EL2.(E2H, TGE) is {1, 1}, the EL2&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

**Configuration**

There are no configuration notes.

**Attributes**

AT S12E1R is a 64-bit System instruction.

**Field descriptions**

The AT S12E1R input value bit assignments are:

```
   Bits [63:0]   
   63  62  61  60  59  58  57  56  55  54  53  52  51  50  49  48  47  46  45  44  43  42  41  40  39  38  37  36  35  34  33  32
   Input address for translation
   Input address for translation
   31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
```

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S12E1R instruction**

Accesses to this instruction use the following encodings:

```
   AT S12E1R, <Xt>
   op0     op1    CRn    CRm    op2
   0b01 0b100 0b0111 0b1000 0b100
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00' then
        AT_S1E1R(X[t]);
    else
        AT_S12E1R(X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        AT_S1E1R(X[t]);
    elseif EL2Enabled() && (HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00') then
        AT_S1E1R(X[t]);
    else
        AT_S12E1R(X[t]);

AT S12E1W, Address Translate Stages 1 and 2 EL1 Write

The AT S12E1W characteristics are:

**Purpose**

Performs stage 1 and 2 address translation, with permissions as if writing to the given virtual address from EL1, or from EL2 if the Effective value of \texttt{HCR\_EL2\_E2H, TGE} is \{1, 1\}, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of \texttt{SCR\_EL3} NS:
  - If \texttt{HCR\_EL2\_E2H, TGE} is not \{1, 1\}, the EL1\&0 translation regime, accessed from EL1.
  - If \texttt{HCR\_EL2\_E2H, TGE} is \{1, 1\}, the EL2\&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

**Configuration**

There are no configuration notes.

**Attributes**

AT S12E1W is a 64-bit System instruction.

**Field descriptions**

The AT S12E1W input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>Input address for translation</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the \texttt{PAR\_EL1}.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is \texttt{RES0}.

**Executing the AT S12E1W instruction**

Accesses to this instruction use the following encodings:

\[
\text{AT S12E1W, <Xt>}\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00' then
    AT_S1E1W(X[t]);
  else
    AT_S12E1W(X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    AT_S1E1W(X[t]);
  elseif EL2Enabled() && (HCR_EL2.<E2H,TGE> == '11' || HCR_EL2.<DC,VM> == '00') then
    AT_S1E1W(X[t]);
  else
    AT_S12E1W(X[t]);

AT S1E0R, Address Translate Stage 1 EL0 Read

The AT S1E0R characteristics are:

Purpose

Performs stage 1 address translation from EL0, with permissions as if reading from the given virtual address from EL0, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the EL2&0 translation regime.
- Otherwise, the EL1&0 translation regime.

Configuration

There are no configuration notes.

Attributes

AT S1E0R is a 64-bit System instruction.

Field descriptions

The AT S1E0R input value bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
</table>
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | 32
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

Bits [63:0]

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

Executing the AT S1E0R instruction

Accesses to this instruction use the following encodings:

AT S1E0R, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.AT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E0R == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AT_S1E0R(X[t]);
elsif PSTATE.EL == EL2 then
  AT_S1E0R(X[t]);
elsif PSTATE.EL == EL3 then
  AT_S1E0R(X[t]);
AT S1E0W, Address Translate Stage 1 EL0 Write

The AT S1E0W characteristics are:

**Purpose**

Performs stage 1 address translation from EL0, with permissions as if writing to the given virtual address from EL0, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the EL2&0 translation regime.
- Otherwise, the EL1&0 translation regime.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E0W is a 64-bit System instruction.

**Field descriptions**

The AT S1E0W input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E0W instruction**

Accesses to this instruction use the following encodings:

AT S1E0W, <Xt>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.AT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E0W == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AT_S1E0W(X[t]);
  endif
elsif PSTATE.EL == EL2 then
  AT_S1E0W(X[t]);
elsif PSTATE.EL == EL3 then
  AT_S1E0W(X[t]);

AT S1E1R, Address Translate Stage 1 EL1 Read

The AT S1E1R characteristics are:

**Purpose**

Performs stage 1 address translation, with permissions as if reading from the given virtual address from EL1, or from EL2 if the Effective value of HCR_EL2.(E2H, TGE) is \( \{1, 1\} \), using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.(E2H, TGE) is not \( \{1, 1\} \), the EL1&0 translation regime, accessed from EL1.
  - If HCR_EL2.(E2H, TGE) is \( \{1, 1\} \), the EL2&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E1R is a 64-bit System instruction.

**Field descriptions**

The AT S1E1R input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is \( \text{RES}0 \).

**Executing the AT S1E1R instruction**

Accesses to this instruction use the following encodings:

AT S1E1R, \(<Xt>\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E1R == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AT_S1E1R(X[t]);
    end
elsif PSTATE.EL == EL2 then
    AT_S1E1R(X[t]);
elsif PSTATE.EL == EL3 then
    AT_S1E1R(X[t]);
AT S1E1RP, Address Translate Stage 1 EL1 Read PAN

The AT S1E1RP characteristics are:

**Purpose**

Performs a stage 1 address translation, where the value of PSTATE.PAN determines if a read from a location will generate a permission fault for a privileged access, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the EL1&0 translation regime, accessed from EL1.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the EL2&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

**Configuration**

This instruction is present only when FEAT_PAN2 is implemented. Otherwise, direct accesses to AT S1E1RP are UNDEFINED.

**Attributes**

AT S1E1RP is a 64-bit System instruction.

**Field descriptions**

The AT S1E1RP input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E1RP instruction**

Accesses to this instruction use the following encodings:

AT S1E1RP, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E1RP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AT_S1E1RP(X[t]);
    end
elsif PSTATE.EL == EL2 then
    AT_S1E1RP(X[t]);
elsif PSTATE.EL == EL3 then
    AT_S1E1RP(X[t]);
The AT S1E1W characteristics are:

**Purpose**

Performs stage 1 address translation, with permissions as if writing to the given virtual address from EL1, or from EL2 if the Effective value of `HCR_EL2.{E2H, TGE}` is {1, 1}, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3.NS`:
  - If `HCR_EL2.{E2H, TGE}` is not {1, 1}, the EL1&0 translation regime, accessed from EL1.
  - If `HCR_EL2.{E2H, TGE}` is {1, 1}, the EL2&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E1W is a 64-bit System instruction.

**Field descriptions**

The AT S1E1W input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>Input address for translation</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>Input address for translation</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the `PAR_EL1`.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is `RES0`.

**Executing the AT S1E1W instruction**

Accesses to this instruction use the following encodings:

AT S1E1W, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E1W == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AT_S1E1W(X[t]);
    end
elsif PSTATE.EL == EL2 then
    AT_S1E1W(X[t]);
elsif PSTATE.EL == EL3 then
    AT_S1E1W(X[t]);

AT S1E1WP, Address Translate Stage 1 EL1 Write PAN

The AT S1E1WP characteristics are:

Purpose

Performs a stage 1 address translation, where the value of PSTATE.PAN determines if a write to a location will generate a permission fault for a privileged access, using the following translation regime:

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the EL1&0 translation regime, accessed from EL1.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the EL2&0 translation regime, accessed from EL2.
- Otherwise, the EL1&0 translation regime, accessed from EL1.

Configuration

This instruction is present only when FEAT_PAN2 is implemented. Otherwise, direct accesses to AT S1E1WP are UNDEFINED.

Attributes

AT S1E1WP is a 64-bit System instruction.

Field descriptions

The AT S1E1WP input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Input address for translation</td>
</tr>
<tr>
<td>62</td>
<td>Input address for translation</td>
</tr>
<tr>
<td>61</td>
<td>60</td>
</tr>
<tr>
<td>-----</td>
<td>----------------------</td>
</tr>
<tr>
<td>63</td>
<td>62</td>
</tr>
</tbody>
</table>

Bits [63:0]

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

Executing the AT S1E1WP instruction

Accesses to this instruction use the following encodings:

AT S1E1WP, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ATS1E1WP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AT_S1E1WP(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    AT_S1E1WP(X[t]);
elsif PSTATE.EL == EL3 then
    AT_S1E1WP(X[t]);
AT S1E2R, Address Translate Stage 1 EL2 Read

The AT S1E2R characteristics are:

**Purpose**

Performs stage 1 address translation as defined for EL2, with permissions as if reading from the given virtual address.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E2R is a 64-bit System instruction.

**Field descriptions**

The AT S1E2R input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Input address for translation</td>
</tr>
<tr>
<td>62</td>
<td>Input address for translation</td>
</tr>
<tr>
<td>31</td>
<td>Input address for translation</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E2R instruction**

Accesses to this instruction use the following encodings:

```
AT S1E2R, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  AT_S1E2R(X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    AT_S1E2R(X[t]);
AT S1E2W, Address Translate Stage 1 EL2 Write

The AT S1E2W characteristics are:

**Purpose**

Performs stage 1 address translation as defined for EL2, with permissions as if writing to the given virtual address.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E2W is a 64-bit System instruction.

**Field descriptions**

The AT S1E2W input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>62</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>61</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>60</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>59</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>58</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>57</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>56</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>55</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>54</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>53</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>52</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>51</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>49</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>48</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>47</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>46</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>45</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>44</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>43</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>42</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>41</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>40</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>39</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>38</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>37</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>36</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>35</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>34</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>33</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>32</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>31</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>28</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>27</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>26</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>24</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>23</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>22</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>21</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>20</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>19</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>18</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>17</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>16</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>15</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>14</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>13</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>12</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>11</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>Input address for translation</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E2W instruction**

Accesses to this instruction use the following encodings:

AT S1E2W, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  AT_S1E2W(X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    AT_S1E2W(X[t]);
```
AT S1E3R, Address Translate Stage 1 EL3 Read

The AT S1E3R characteristics are:

**Purpose**

Performs stage 1 address translation as defined for EL3, with permissions as if reading from the given virtual address.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E3R is a 64-bit System instruction.

**Field descriptions**

The AT S1E3R input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

*Input address for translation*

*Input address for translation*

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E3R instruction**

Accesses to this instruction use the following enccodings:

\[
\text{AT S1E3R, } \langle \text{Xt}\rangle \\
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b01 & 0b110 & 0b1111 & 0b1000 & 0b000 \\
\hline
\end{array}
\]

if \text{PSTATE.EL} == \text{EL0} then
    \text{UNDEFINED;}
elsif \text{PSTATE.EL} == \text{EL1} then
    \text{UNDEFINED;}
elsif \text{PSTATE.EL} == \text{EL2} then
    \text{UNDEFINED;}
elsif \text{PSTATE.EL} == \text{EL3} then
    \text{AT\_S1E3R}(X[t]);

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AT S1E3W, Address Translate Stage 1 EL3 Write

The AT S1E3W characteristics are:

**Purpose**

Performs stage 1 address translation as defined for EL3, with permissions as if writing to the given virtual address.

**Configuration**

There are no configuration notes.

**Attributes**

AT S1E3W is a 64-bit System instruction.

**Field descriptions**

The AT S1E3W input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:0]**

Input address for translation. The resulting address can be read from the PAR_EL1.

If the address translation instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then VA[63:32] is RES0.

**Executing the AT S1E3W instruction**

Accesses to this instruction use the following encodings:

AT S1E3W, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
  AT_S1E3W(X[t]);
CCSIDR2_EL1, Current Cache Size ID Register 2

The CCSIDR2_EL1 characteristics are:

**Purpose**

When FEAT_CCIDX is implemented, provides the information about the architecture of the currently selected cache from bits[63:32] of CCSIDR_EL1.

When FEAT_CCIDX is not implemented, this register is not implemented.

**Configuration**

AArch64 System register CCSIDR2_EL1 bits [31:0] are architecturally mapped to AArch32 System register CCSIDR2[31:0].

This register is present only when FEAT_CCIDX is implemented. Otherwise, direct accesses to CCSIDR2_EL1 are UNDEFINED.

In an AArch64 only implementation, it is IMPLEMENTATION DEFINED whether reading this register gives an UNKNOWN value or is UNDEFINED.

The implementation includes one CCSIDR2_EL1 for each cache that it can access. CSSELR_EL1 selects which Cache Size ID Register is accessible.

**Attributes**

CCSIDR2_EL1 is a 64-bit register.

**Field descriptions**

The CCSIDR2_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>RES0</td>
<td>NumSets</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**NumSets, bits [23:0]**

(Number of sets in cache) - 1, therefore a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

**Accessing the CCSIDR2_EL1**

If CSSELR_EL1 Level is programmed to a cache level that is not implemented, then on a read of the CCSIDR2_EL1 the behavior is CONSTRAINED UNPREDICTABLE, and can be one of the following:

- The CCSIDR2_EL1 read is treated as NOP.
- The CCSIDR2_EL1 read is UNDEFINED.
- The CCSIDR2_EL1 read returns an UNKNOWN value.

Accesses to this register use the following encodings:
MRS <Xt>, CCSIDR2_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TID4 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CCSIDR2_EL1;
elsif PSTATE.EL == EL2 then
  return CCSIDR2_EL1;
elsif PSTATE.EL == EL3 then
  return CCSIDR2_EL1;
The CCSIDR_EL1 characteristics are:

**Purpose**

Provides information about the architecture of the currently selected cache.

**Configuration**

AArch64 System register CCSIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register CCSIDR31:0.

AArch64 System register CCSIDR_EL1 bits [63:32] are architecturally mapped to AArch32 System register CCSIDR2[31:0].

The implementation includes one CCSIDR_EL1 for each cache that it can access. CSSELR_EL1 selects which Cache Size ID Register is accessible.

**Attributes**

CCSIDR_EL1 is a 64-bit register.

**Field descriptions**

The CCSIDR_EL1 bit assignments are:

**When FEAT_CCIDX is implemented:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | NumSets |
| RES0 | Associativity | LineSize |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Note**

The parameters NumSets, Associativity, and LineSize in these registers define the architecturally visible parameters that are required for the cache maintenance by Set/Way instructions. They are not guaranteed to represent the actual microarchitectural features of a design. You cannot make any inference about the actual sizes of caches based on these parameters.

**Bits [63:56]**

Reserved, RES0.

**NumSets, bits [55:32]**

(Number of sets in cache) - 1, therefore a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

**Bits [31:24]**

Reserved, RES0.
Associativity, bits [23:3]

(Associativity of cache) - 1, therefore a value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2.

LineSize, bits [2:0]

(Log₂(Number of bytes in cache line)) - 4. For example:

- For a line length of 16 bytes: Log₂(16) = 4, LineSize entry = 0. This is the minimum line length.
- For a line length of 32 bytes: Log₂(32) = 5, LineSize entry = 1.

When FEAT_MTE is implemented and enabled, where a cache only holds Allocation tags, this field is RES0.

Otherwise:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
</table>

NumSets, bits [27:13]

(Number of sets in cache) - 1, therefore a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

Associativity, bits [12:3]

(Associativity of cache) - 1, therefore a value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2.

LineSize, bits [2:0]

(Log₂(Number of bytes in cache line)) - 4. For example:

- For a line length of 16 bytes: Log₂(16) = 4, LineSize entry = 0. This is the minimum line length.
- For a line length of 32 bytes: Log₂(32) = 5, LineSize entry = 1.

Accessing the CCSIDR_EL1

If CSSEL_EL1.Level is programmed to a cache level that is not implemented, then on a read of the CCSIDR_EL1 the behavior is CONSTRAINED UNPREDICTABLE, and can be one of the following:

- The CCSIDR_EL1 read is treated as NOP.
- The CCSIDR_EL1 read is **UNDEFINED**.
- The CCSIDR_EL1 read returns an **UNKNOWN** value.

Accesses to this register use the following encodings:

### MRS <Xt>, CCSIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  else
    UNDEFINED;
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.TID4 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CCSIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CCSIDR_EL1;
  end
elsif PSTATE.EL == EL2 then
  return CCSIDR_EL1;
elsif PSTATE.EL == EL3 then
  return CCSIDR_EL1;
CFP RCTX, Control Flow Prediction Restriction by Context

The CFP RCTX characteristics are:

**Purpose**

Control Flow Prediction Restriction by Context applies to all Control Flow Prediction Resources that predict execution based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, control flow prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of prediction structures so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when FEAT_SPECRES is implemented. Otherwise, direct accesses to CFP RCTX are undefined.

**Attributes**

CFP RCTX is a 64-bit System instruction.

**Field descriptions**

The CFP RCTX input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>57</td>
<td>GVMID</td>
<td>Execution applies to all VMIDs or a specified VMID.</td>
</tr>
<tr>
<td>50</td>
<td>VMID</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>NS</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>ASID</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:49]**

Reserved, RES0.

**GVMID, bit [48]**

Execution of this instruction applies to all VMIDs or a specified VMID.
<table>
<thead>
<tr>
<th>GVMID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Applies to specified VMID for an EL0 or EL1 target execution context.</td>
</tr>
<tr>
<td>001</td>
<td>Applies to all VMIDs for an EL0 or EL1 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0 or EL1, this field is \texttt{RES0}.

If the instruction is executed at EL0 or EL1, this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is \texttt{RES0}.

**VMID, bits [47:32]**

Only applies when bit[48] is 0 and the target execution context is either:

- EL1.
- EL0 when \( \text{HCR} \_\text{EL2.E2H}==0 \) or \( \text{HCR} \_\text{EL2.TGE}==0 \).

Otherwise this field is \texttt{RES0}.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and \( \text{HCR} \_\text{EL2.E2H}==0 \) or \( \text{HCR} \_\text{EL2.TGE}==0 \), this field is treated as the current VMID.

When the instruction is executed at EL0 and \( \text{HCR} \_\text{EL2.E2H}==1 \) and \( \text{HCR} \_\text{EL2.TGE}==1 \), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is \texttt{RES0}.

**Bits [31:27]**

Reserved, \texttt{RES0}.

**NS, bit [26]**

Security State. Defined values are:

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure state.</td>
</tr>
</tbody>
</table>

When executed in Non-secure state, the Effective value of NS is 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>EL0</td>
</tr>
<tr>
<td>0b01</td>
<td>EL1</td>
</tr>
<tr>
<td>0b10</td>
<td>EL2</td>
</tr>
<tr>
<td>0b11</td>
<td>EL3</td>
</tr>
</tbody>
</table>

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**Bits [23:17]**

Reserved, \texttt{RES0}.

**GASID, bit [16]**

Execution of this instruction applies to all ASIDs or a specified ASID.
<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0, this field is RES0.

If the instruction is executed at EL0, this field has an Effective value of 0.

**ASID, bits [15:0]**

Only applies for an EL0 target execution context and when bit[16] is 0.

Otherwise, this field is RES0.

When the instruction is executed at EL0, this field is treated as the current ASID.

**Executing the CFP RCTX instruction**

Accesses to this instruction use the following encodings:

**CFP RCTX, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.EnRCTX == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.CFPRCTX == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        endif
    endif
    elseif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.CFPRCTX == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        CFP_RCTX(X[t]);
    endif
else if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.CFPRCTX == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            CFP_RCTX(X[t]);
        endif
    endif
else
    CFP_RCTX(X[t]);
endif
```
The CLIDR_EL1 characteristics are:

**Purpose**

Identifies the type of cache, or caches, that are implemented at each level and can be managed using the architected cache maintenance instructions that operate by set/way, up to a maximum of seven levels. Also identifies the Level of Coherence (LoC) and Level of Unification (LoU) for the cache hierarchy.

**Configuration**

AArch64 System register CLIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register CLIDR[31:0].

**Attributes**

CLIDR_EL1 is a 64-bit register.

**Field descriptions**

The CLIDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [63:47]</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>Ttype&lt;n&gt;, bits [2(n-1)+34:2(n-1)+33], for n = 7 to 1</td>
<td>Tag cache type. Indicate the type of cache that is implemented and can be managed using the architected cache maintenance instructions that operate by set/way at each level, from Level 1 up to a maximum of seven levels of cache hierarchy.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ttype&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No Tag Cache.</td>
</tr>
<tr>
<td>0b01</td>
<td>Separate Allocation Tag Cache.</td>
</tr>
<tr>
<td>0b10</td>
<td>Unified Allocation Tag and Data cache, Allocation Tags and Data in unified lines.</td>
</tr>
<tr>
<td>0b11</td>
<td>Unified Allocation Tag and Data cache, Allocation Tags and Data in separate lines.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

**ICB, bits [32:30]**

Inner cache boundary. This field indicates the boundary for caching Inner Cacheable memory regions.

The possible values are:
<table>
<thead>
<tr>
<th>ICB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Not disclosed by this mechanism.</td>
</tr>
<tr>
<td>0b001</td>
<td>L1 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b010</td>
<td>L2 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b011</td>
<td>L3 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b100</td>
<td>L4 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b101</td>
<td>L5 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b110</td>
<td>L6 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b111</td>
<td>L7 cache is the highest Inner Cacheable level.</td>
</tr>
</tbody>
</table>

**LoUU, bits [29:27]**

Level of Unification Uniprocessor for the cache hierarchy.

**Note**

When FEAT S2FWB is implemented, the architecture requires that this field is zero so that no levels of data cache need to be cleaned in order to manage coherency with instruction fetches.

**LoC, bits [26:24]**

Level of Coherence for the cache hierarchy.

**LoUIS, bits [23:21]**

Level of Unification Inner Shareable for the cache hierarchy.

**Note**

When FEAT S2FWB is implemented, the architecture requires that this field is zero so that no levels of data cache need to be cleaned in order to manage coherency with instruction fetches.

**Ctype<n>, bits [3(n-1)+2:3(n-1)], for n = 7 to 1**

Cache Type fields. Indicate the type of cache that is implemented and can be managed using the architected cache maintenance instructions that operate by set/way at each level, from Level 1 up to a maximum of seven levels of cache hierarchy. Possible values of each field are:

<table>
<thead>
<tr>
<th>Ctype&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>No cache.</td>
</tr>
<tr>
<td>0b001</td>
<td>Instruction cache only.</td>
</tr>
<tr>
<td>0b010</td>
<td>Data cache only.</td>
</tr>
<tr>
<td>0b011</td>
<td>Separate instruction and data caches.</td>
</tr>
<tr>
<td>0b100</td>
<td>Unified cache.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If software reads the Cache Type fields from Ctype1 upwards, once it has seen a value of 000, no caches that can be managed using the architected cache maintenance instructions that operate by set/way exist at further-out levels of the hierarchy. So, for example, if Ctype3 is the first Cache Type field with a value of 000, the values of Ctype4 to Ctype7 must be ignored.

**Accessing the CLIDR_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, CLIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TID4 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CLIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CLIDR_EL1;
elsif PSTATE.EL == EL2 then
  return CLIDR_EL1;
elsif PSTATE.EL == EL3 then
  return CLIDR_EL1;
The CNTFRQ_EL0 characteristics are:

**Purpose**

This register is provided so that software can discover the frequency of the system counter. It must be programmed with this value as part of system initialization. The value of the register is not interpreted by hardware.

**Configuration**

AArch64 System register CNTFRQ_EL0 bits [31:0] are architecturally mapped to AArch32 System register CNTFRQ[31:0].

**Attributes**

CNTFRQ_EL0 is a 64-bit register.

**Field descriptions**

The CNTFRQ_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>Clock frequency</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

Clock frequency. Indicates the system counter clock frequency, in Hz.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTFRQ_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, CNTFRQ_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.<EL0PCTEN,EL0VCTEN> == '00' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.<EL0PCTEN,EL0VCTEN> == '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CNTFRQ_EL0;
  elsif PSTATE.EL == EL1 then
    return CNTFRQ_EL0;
  elsif PSTATE.EL == EL2 then
    return CNTFRQ_EL0;
  elsif PSTATE.EL == EL3 then
    return CNTFRQ_EL0;

MSR CNTFRQ_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if IsHighestEL(PSTATE.EL) then
  CNTFRQ_EL0 = X[t];
else
  UNDEFINED;
The CNTHCTL_EL2 characteristics are:

**Purpose**

Controls the generation of an event stream from the physical counter, and access from EL1 to the physical counter and the EL1 physical timer.

**Configuration**

AArch64 System register CNTHCTL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHCTL[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

CNTHCTL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHCTL_EL2 bit assignments are:

**When FEAT_VHE is implemented and HCR_EL2.E2H == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>EVNTS</td>
</tr>
<tr>
<td>61</td>
<td>EVNTI</td>
</tr>
<tr>
<td>60</td>
<td>EL1NVCT</td>
</tr>
<tr>
<td>59</td>
<td>EL1VPCT</td>
</tr>
<tr>
<td>58</td>
<td>EL1TVCT</td>
</tr>
<tr>
<td>57</td>
<td>EL1VT</td>
</tr>
<tr>
<td>56</td>
<td>ECV</td>
</tr>
<tr>
<td>55</td>
<td>EL1PTEN</td>
</tr>
<tr>
<td>54</td>
<td>EL1PCTEN</td>
</tr>
<tr>
<td>53</td>
<td>EL0PTEN</td>
</tr>
<tr>
<td>52</td>
<td>EL0VTEN</td>
</tr>
<tr>
<td>51</td>
<td>EVNTI</td>
</tr>
<tr>
<td>50</td>
<td>EVNTDIR</td>
</tr>
</tbody>
</table>

**Bits [63:18]**

Reserved, RES0.

**EVNTIS, bit [17]**

When FEAT_ECV is implemented:

Controls the scale of the generation of the event stream.

<table>
<thead>
<tr>
<th>EVNTIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CNTHCTL_EL2.EVNTI field applies to CNTPCT_EL0[15:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>The CNTHCTL_EL2.EVNTI field applies to CNTPCT_EL0[23:8].</td>
</tr>
</tbody>
</table>

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**EL1NVVCT, bit [16]**

When FEAT_ECV is implemented:

Traps EL1 accesses to the specified EL1 virtual timer registers using the EL02 descriptors to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>EL1NVVCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If ((HCR_EL2.E2H==1 &amp;&amp; HCR_EL2.TGE==1)</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**EL1NVPCT, bit [15]**

When FEAT_ECV is implemented:

Traps EL1 accesses to the specified EL1 physical timer registers using the EL02 descriptors to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>EL1NVPCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If ((HCR_EL2.E2H==1 &amp;&amp; HCR_EL2.TGE==1)</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**EL1TVCT, bit [14]**

CNTHCTL_EL2, Counter-timer Hypervisor Control register

Page 165
When FEAT_ECV is implemented:

Traps EL0 and EL1 accesses to the EL1 virtual counter registers to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>EL1TVCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1     | If HCR_EL2.(E2H, TGE) is {1, 1}, this control does not cause any instructions to be trapped.  
If HCR_EL2.E2H is 0 or HCR_EL2.TGE is 0, then:  
• In AArch64 state, traps EL0 and EL1 accesses to CNTVCT_EL0 to EL2, unless they are trapped by CNTKCTL_EL1.EL0VCTEN.  
• In AArch32 state, traps EL0 and EL1 accesses to CNTVCT to EL2, unless they are trapped by CNTKCTL_EL1.EL0VCTEN or CNTKCTL.PL0VCTEN. |

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EL1TVT, bit [13]

When FEAT_ECV is implemented:

Traps EL0 and EL1 accesses to the EL1 virtual timer registers to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>EL1TVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1     | If HCR_EL2.(E2H, TGE) is {1, 1}, this control does not cause any instructions to be trapped.  
If HCR_EL2.E2H is 0 or HCR_EL2.TGE is 0, then:  
• In AArch64 state, traps EL0 and EL1 accesses to CNTV_CTL_EL0, CNTV_CVAL_EL0, and CNTV_TVAL_EL0 to EL2, unless they are trapped by CNTKCTL_EL1.EL0VTEN.  
• In AArch32 state, traps EL0 and EL1 accesses to CNTV_CTL, CNTV_CVAL, and CNTV_TVAL to EL2, unless they are trapped by CNTKCTL_EL1.EL0VTEN or CNTKCTL.PL0VTEN. |

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
**ECV, bit [12]**

When **FEAT_ECV** is implemented:

Enables the Enhanced Counter Virtualization functionality registers.

<table>
<thead>
<tr>
<th>ECV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Enhanced Counter Virtualization functionality is disabled.</td>
</tr>
</tbody>
</table>
| 0b1 | When \(HCR\_EL2.\{E2H, \text{TGE}\} = \{1, 1\}\) or \(SCR\_EL3.\{\text{NS, EEL2}\} = \{0, 0\}\), then Enhanced Counter Virtualization functionality is disabled.  
When \(SCR\_EL3.\text{NS}\) or \(SCR\_EL3.\text{EEL2}\) are 1, and \(HCR\_EL2.\text{E2H}\) or \(HCR\_EL2.\text{TGE}\) are 0, then Enhanced Counter Virtualization functionality is enabled when EL2 is enabled for the current Security state. This means that:
  - An MRS to \(\text{CNTPCT\_EL0}\) from either EL0 or EL1 that is not trapped will return the value \((\text{PCount}<63:0> - \text{CNTPOFF\_EL2}<63:0>)\).  
  - The EL1 physical timer interrupt is triggered when \((\text{PCount}<63:0> - \text{CNTPOFF\_EL2}<63:0>) - \text{PCVal}<63:0>\) is greater than or equal to 0. \(\text{PCount}<63:0>\) is the physical count returned when \(\text{CNTPCT\_EL0}\) is read from EL2 or EL3. \(\text{PCVal}<63:0>\) is the EL1 physical timer compare value for this timer. |

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

---

**EL1PTEN, bit [11]**

When \(HCR\_EL2.\text{TGE}\) is 0, traps EL0 and EL1 accesses to the E1 physical timer registers to EL2 when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>EL1PTEN</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0     | From AArch64 state: EL0 and EL1 accesses to the \(\text{CNTP\_CTL\_EL0, CNTP\_CVAL\_EL0, and CNTP\_TVAL\_EL0}\) are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by \(\text{CNTKCTL\_EL1.EL0PTEN}\).  
From AArch32 state: EL0 and EL1 accesses to the \(\text{CNTP\_CTL, CNTP\_CVAL, and CNTP\_TVAL}\) are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by \(\text{CNTKCTL\_EL1.EL0PTEN}\) or \(\text{CNTKCTL\_PL0PTEN}\). |
| 0b1     | This control does not cause any instructions to be trapped. |

When \(HCR\_EL2.\text{TGE}\) is 1, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

---

**EL1PCTEN, bit [10]**

When \(HCR\_EL2.\text{TGE}\) is 0, traps EL0 and EL1 accesses to the EL1 physical counter register to EL2 when EL2 is enabled in the current Security state, as follows:

- In AArch64 state, accesses to \(\text{CNTPCT\_EL0}\) are trapped to EL2, reported using EC syndrome value 0x18.  
- In AArch32 state, MRRC or MCRR accesses to \(\text{CNTPCT}\) are trapped to EL2, reported using EC syndrome value 0x04.
EL1PCTEN

| Meaning | 0b0 | From AArch64 state: EL0 and EL1 accesses to the CNTPCT_EL0 are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1.EL0PCTEN.
| 0b1 | This control does not cause any instructions to be trapped. |

From AArch32 state: EL0 and EL1 accesses to the CNTPCT are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1.EL0PCTEN or CNTKCTL.PL0PCTEN.

When HCR_EL2.TGE is 1, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EL0PTEN, bit [9]

When HCR_EL2.TGE is 0, this control does not cause any instructions to be trapped.

When HCR_EL2.TGE is 1, traps EL0 accesses to the physical timer registers to EL2.

| Meaning | 0b0 | EL0 using AArch64: EL0 accesses to the CNTP_CTL_EL0, CNTP_CVAL_EL0, and CNTP_TVAL_EL0 registers are trapped to EL2.
| 0b1 | EL0 using AArch32: EL0 accesses to the CNTP_CTL, CNTP_CVAL, and CNTP_TVAL registers are trapped to EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EL0VTEN, bit [8]

When HCR_EL2.TGE is 0, this control does not cause any instructions to be trapped.

When HCR_EL2.TGE is 1, traps EL0 accesses to the virtual timer registers to EL2.

| Meaning | 0b0 | EL0 using AArch64: EL0 accesses to the CNTV_CTL_EL0, CNTV_CVAL_EL0, and CNTV_TVAL_EL0 registers are trapped to EL2.
| 0b1 | EL0 using AArch32: EL0 accesses to the CNTV_CTL, CNTV_CVAL, and CNTV_TVAL registers are trapped to EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EVNTI, bits [7:4]

Selects which bit of the counter register CNTPCT_EL0 is the trigger for the event stream generated from that counter, when that stream is enabled.

If FEAT_ECV is implemented, and CNTHCTL_EL2.EVNTIS is 1, this field selects a trigger bit in the range 8 to 23 of the counter register CNTPCT_EL0.

Otherwise, this field selects a trigger bit in the range 0 to 15 of the counter register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EVNTDIR, bit [3]

Controls which transition of the counter register CNTPCT_EL0 trigger bit, defined by EVNTI, generates an event when the event stream is enabled.
### EVNTDIR

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>A 0 to 1 transition of the trigger bit triggers an event.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>A 1 to 0 transition of the trigger bit triggers an event.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EVNTEN, bit [2]

Enables the generation of an event stream from the counter register `CNTPCT_EL0`.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disables the event stream.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Enables the event stream.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EL0VCTEN, bit [1]

When `HCR_EL2.TGE` is 0, this control does not cause any instructions to be trapped.

When `HCR_EL2.TGE` is 1, traps EL0 accesses to the frequency register and virtual counter register to EL2.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0 using AArch64: EL0 accesses to the <code>CNTVCT_EL0</code> register are trapped to EL2, if <code>CNTHCTL_EL2.EL0PCTEN</code> is also 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0 using AArch32: EL0 accesses to the <code>CNTVCT</code> register are trapped to EL2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0 using AArch32: EL0 accesses to the <code>CNTFRQ</code> register are trapped to EL2, if <code>CNTHCTL_EL2.EL0PCTEN</code> is also 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>This control does not cause any instructions to be trapped.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EL0PCTEN, bit [0]

When `HCR_EL2.TGE` is 0, this control does not cause any instructions to be trapped.

When `HCR_EL2.TGE` is 1, traps EL0 accesses to the frequency register and physical counter register to EL2.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>EL0 using AArch64: EL0 accesses to the <code>CNTPCT_EL0</code> register are trapped to EL2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0 using AArch64: EL0 accesses to the <code>CNTFRQ_EL0</code> register are trapped to EL2, if <code>CNTHCTL_EL2.EL0VCTEN</code> is also 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0 using AArch32: EL0 accesses to the <code>CNTVCT</code> register are trapped to EL2.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EL0 using AArch32: EL0 accesses to the <code>CNTFRQ</code> register are trapped to EL2, if <code>CNTHCTL_EL2.EL0VCTEN</code> is also 0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>This control does not cause any instructions to be trapped.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

This format applies in all Armv8.0 implementations, and it also contains a description of the behavior when EL3 is implemented and EL2 is not implemented.
Bits [63:18]
Reserved, RES0.

EVNTIS, bit [17]
When FEAT_ECV is implemented:
Controls the scale of the generation of the event stream.

<table>
<thead>
<tr>
<th>EVNTIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CNTHCTL_EL2.EVNTI field applies to CNTPCT_EL0[15:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>The CNTHCTL_EL2.EVNTI field applies to CNTPCT_EL0[23:8].</td>
</tr>
</tbody>
</table>

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

EL1NVVCT, bit [16]
When FEAT_ECV is implemented:
Traps EL1 accesses to the specified EL1 virtual timer registers using the EL02 descriptors to EL2, when EL2 is enabled for the current Security state.

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

EL1NVPCT, bit [15]
When FEAT_ECV is implemented:
Traps EL1 accesses to the specified EL1 physical timer registers using the EL02 descriptors to EL2, when EL2 is enabled for the current Security state.
### EL1NVPCT

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If ((HCR_EL2.E2H==1 &amp; HCR_EL2.TGE==1)</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

Reserved, RES0.

### EL1TVCT, bit [14]

#### When FEAT_ECV is implemented:

Traps EL0 and EL1 accesses to the EL1 virtual counter registers to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If HCR_EL2.{E2H, TGE} is {1, 1}, this control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

Reserved, RES0.

### EL1TVT, bit [13]

#### When FEAT_ECV is implemented:

Traps EL0 and EL1 accesses to the EL1 virtual timer registers to EL2, when EL2 is enabled for the current Security state.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1   | If HCR_EL2.E2H is 0 or HCR_EL2.TGE is 0, then:

In AArch64 state, traps EL0 and EL1 accesses to CNTVCT_EL0 to EL2, unless they are trapped by CNTKCTL_EL1.EL0VCTEN. In AArch32 state, traps EL0 and EL1 accesses to CNTVCT to EL2, unless they are trapped by CNTKCTL_EL1.EL0VCTEN or CNTKCTL.PL0VCTEN. |

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

Reserved, RES0.
### E1TVD

<table>
<thead>
<tr>
<th>E1TVD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If HCR_EL2, (E2H, TGE) is {1, 1}, this control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If HCR_EL2.E2H is 0 or HCR_EL2.TGE is 0, then:
- In AArch64 state, traps EL0 and EL1 accesses to CNTV_CTL_EL0, CNTV_CVAL_EL0, and CNTV_TVAL_EL0 to EL2, unless they are trapped by CNTKCTL_EL1.EL0VTEN.
- In AArch32 state, traps EL0 and EL1 accesses to CNTV_CTL, CNTV_CVAL, and CNTV_TVAL to EL2, unless they are trapped by CNTKCTL_EL1.EL0VTEN or CNTKCTL.PL0VTEN.

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 0 other than for the purpose of a direct read.

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

Reserved, RES0.

### ECV, bit [12]

#### When FEAT_ECV is implemented:

Enables the Enhanced Counter Virtualization functionality registers.

<table>
<thead>
<tr>
<th>ECV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Enhanced Counter Virtualization functionality is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>When HCR_EL2, (E2H, TGE) == {1, 1} or SCR_EL3, {NS, EEL2} == {0, 0}, then Enhanced Counter Virtualization functionality is disabled.</td>
</tr>
</tbody>
</table>

When SCR_EL3.NS or SCR_EL3.EEL2 are 1, and HCR_EL2.E2H or HCR_EL2.TGE are 0, then Enhanced Counter Virtualization functionality is enabled when EL2 is enabled for the current Security state. This means that:
- An MRS to CNTPCT_EL0 from either EL0 or EL1 that is not trapped will return the value (PCount<63:0> - CNTPOFF_EL2<63:0>).
- The EL1 physical timer interrupt is triggered when ((PCount<63:0> - CNTPOFF_EL2<63:0>) - PCVal<63:0>) is greater than or equal to 0. PCount is the physical count returned when CNTPCT_EL0 is read from EL2 or EL3. PCVal<63:0> is the EL1 physical timer compare value for this timer.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Otherwise:

Reserved, RES0.

### Bits [11:8]

Reserved, RES0.

### EVNTI, bits [7:4]

Selects which bit of the counter register CNTPCT_EL0 is the trigger for the event stream generated from that counter, when that stream is enabled.
If FEAT_ECV is implemented, and CNTHCTL_EL2.EVNTIS is 1, this field selects a trigger bit in the range 8 to 23 of the counter register CNTPCT_EL0.

Otherwise, this field selects a trigger bit in the range 0 to 15 of the counter register.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTDIR, bit [3]**

Controls which transition of the counter register CNTPCT_EL0 trigger bit, defined by EVNTI, generates an event when the event stream is enabled.

<table>
<thead>
<tr>
<th>EVNTDIR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A 0 to 1 transition of the trigger bit triggers an event.</td>
</tr>
<tr>
<td>0b1</td>
<td>A 1 to 0 transition of the trigger bit triggers an event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTEN, bit [2]**

Enables the generation of an event stream from the counter register CNTPCT_EL0.

<table>
<thead>
<tr>
<th>EVNTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables the event stream.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables the event stream.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**EL1PCEN, bit [1]**

Traps EL0 and EL1 accesses to the EL1 physical timer registers to EL2 when EL2 is enabled in the current Security state, as follows:

- In AArch64 state, accesses to CNTP_CTL_EL0, CNTP_CVAL_EL0, CNTP_TVAL_EL0 are trapped to EL2, reported using EC syndrome value 0x18.
- In AArch32 state, MRC or MCR accesses to the following registers are trapped to EL2 reported using EC syndrome value 0x3 and MRRC and MCRR accesses are trapped to EL2, reported using EC syndrome value 0x04:
  - CNTP_CTL, CNTP_CVAL, CNTP_TVAL.

<table>
<thead>
<tr>
<th>EL1PCEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>From AArch64 state: EL0 and EL1 accesses to the CNTP_CTL_EL0, CNTP_CVAL_EL0, and CNTP_TVAL_EL0 are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1_EL0PTEN. From AArch32 state: EL0 and EL1 accesses to the CNTP_CTL, CNTP_CVAL, and CNTP_TVAL are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1_EL0PTEN or CNTKCTL.PL0PTEN.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EL1PCTEN, bit [0]**

Traps EL0 and EL1 accesses to the EL1 physical counter register to EL2 when EL2 is enabled in the current Security state, as follows:

- In AArch64 state, accesses to CNTPCT_EL0 are trapped to EL2, reported using EC syndrome value 0x18.
- In AArch32 state, MRRC or MCRR accesses to CNTPCT are trapped to EL2, reported using EC syndrome value 0x04.
ELPCTEN | Meaning
--- | ---
0b0 | From AArch64 state: EL0 and EL1 accesses to the CNTPCT_EL0 are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1.EL0PCTEN.
From AArch32 state: EL0 and EL1 accesses to the CNTPCT are trapped to EL2 when EL2 is enabled in the current Security state, unless they are trapped by CNTKCTL_EL1.EL0PCTEN or CNTKCTL.PL0PCTEN.
0b1 | This control does not cause any instructions to be trapped.

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHCTL_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CNTHCTL_EL2 or CNTKCTL_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CNTHCTL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHCTL_EL2;
elsif PSTATE.EL == EL3 then
    return CNTHCTL_EL2;

MSR CNTHCTL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHCTL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHCTL_EL2 = X[t];

MRS <Xt>, CNTKCTL_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    return CNTKCTL_EL1;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return CNTHCTL_EL2;
    else
        return CNTKCTL_EL1;
else if PSTATE.EL == EL3 then
    return CNTKCTL_EL1;

MSR CNTKCTL_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    CNTKCTL_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CNTHCTL_EL2 = X[t];
    else
        CNTKCTL_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    CNTKCTL_EL1 = X[t];
The CNTHP_CTL_EL2 characteristics are:

**Purpose**

Control register for the EL2 physical timer.

**Configuration**

AArch64 System register CNTHP_CTL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHP_CTL[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_CTL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHP_CTL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | ISTATUS | IMASK | ENABLE |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is **UNKNOWN**.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>
For more information, see the description of the ISTATUS bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTHP_TVAL_EL2** continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTHP_CTL_EL2**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL2 using the mnemonic **CNTHP_CTL_EL2** or **CNTP_CTL_EL0** are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, CNTHP_CTL_EL2**

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHP_CTL_EL2;
elsif PSTATE.EL == EL3 then
    return CNTHP_CTL_EL2;
```

**MSR CNTHP_CTL_EL2, <Xt>**

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHP_CTL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHP_CTL_EL2 = X[t];
```
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    return CNTHPS_CTL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHP_CTL_EL2;
  else
    return CNTP_CTL_EL0;
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x180];
    else
      return CNTP_CTL_EL0;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHPS_CTL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHP_CTL_EL2;
    else
      return CNTP_CTL_EL0;
  elsif PSTATE.EL == EL3 then
    return CNTP_CTL_EL0;
  else
    return CNTP_CTL_EL0;
end if

MSR CNTP_CTL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

MSR <Xt>, CNTP_CTL_EL0, <Xt>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  endif
  elif EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  endelsif
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CTL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elif EL2Enabled() && HCR_EL2.E2H == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CTL_EL2 = X[t];
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  CNTP_CTL_EL0 = X[t];
CNTHP_CVAL_EL2, Counter-timer Physical Timer CompareValue register (EL2)

The CNTHP_CVAL_EL2 characteristics are:

**Purpose**

Holds the compare value for the EL2 physical timer.

**Configuration**

AArch64 System register CNTHP_CVAL_EL2 bits [63:0] are architecturally mapped to AArch32 System register CNTHP_CVAL[63:0].

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_CVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHP_CVAL_EL2 bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
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<th>46</th>
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<th>36</th>
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<th>32</th>
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</thead>
<tbody>
<tr>
<td></td>
<td>CompareValue</td>
<td>CompareValue</td>
<td></td>
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<tr>
<td>31</td>
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<td>25</td>
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<td>23</td>
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<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL2 physical timer CompareValue.

When CNTHP_CTL_EL2 ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHP_CTL_EL2.ISTATUS is set to 1.
- If CNTHP_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHP_CTL_EL2 ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHP_CVAL_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CNTHP_CVAL_EL2 or CNTP_CVAL_EL0 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:
MRS <Xt>, CNTHP_CVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return CNTHP_CVAL_EL2;
elsif PSTATE.EL == EL3 then
  return CNTHP_CVAL_EL2;

MSR CNTHP_CVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  CNTHP_CVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  CNTHP_CVAL_EL2 = X[t];

MRS <Xt>, CNTP_CVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    return CNTHPS_CVAL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHP_CVAL_EL2;
  else
    return CNTP_CVAL_EL0;
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x178];
    else
      return CNTP_CVAL_EL0;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHPS_CVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHP_CVAL_EL2;
    else
      return CNTP_CVAL_EL0;
  elsif PSTATE.EL == EL3 then
    return CNTP_CVAL_EL0;
else
  return CNTP_CVAL_EL0;

MSR CNTP_CVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
        CNTHPS_CVAL_EL2 = X[t];
      else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
          CNTP_CVAL_EL0 = X[t];
      else
        CNTHP_CVAL_EL2 = X[t];
    endif
  endif
endif
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if EL2Enabled() && HCR_EL2.<E2H,TGE> == '111' then
        NVMem[0x178] = X[t];
      else
        CNTP_CVAL_EL0 = X[t];
      endif
    endif
  else
    if PSTATE.EL == EL2 then
      if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
        CNTHPS_CVAL_EL2 = X[t];
      elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
        CNTHP_CVAL_EL2 = X[t];
      else
        CNTP_CVAL_EL0 = X[t];
      endif
    elseif PSTATE.EL == EL3 then
      CNTP_CVAL_EL0 = X[t];
    endif
  endif
The CNTHP_TVAL_EL2 characteristics are:

**Purpose**

Holds the timer value for the EL2 physical timer.

**Configuration**

AArch64 System register CNTHP_TVAL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHP_TVAL[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_TVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHP_TVAL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TimerValue |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**TimerValue, bits [31:0]**

The TimerValue view of the EL2 physical timer.

On a read of this register:

- If CNTHP_CTL_EL2.ENABLE is 0, the value returned is **UNKNOWN**.
- If CNTHP_CTL_EL2.ENABLE is 1, the value returned is (CNTHP_CVAL_EL2 - CNTPCT_EL0).

On a write of this register, CNTHP_CVAL_EL2 is set to (CNTPCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHP_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CNTHP_CVAL_EL2) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHP_CTL_EL2.ISTATUS is set to 1.
- If CNTHP_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHP_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Accessing the CNTHP_TVAL_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CNTHP_TVAL_EL2 or CNTP_TVAL_EL0 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CNTHP_TVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == ‘1’ then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHP_TVAL_EL2;
elsif PSTATE.EL == EL3 then
    return CNTHP_TVAL_EL2;

MSR CNTHP_TVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
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<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == ‘1’ then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHP_TVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHP_TVAL_EL2 = X[t];

MRS <Xt>, CNTP_TVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_TVAL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_TVAL_EL2;
    else
        return CNTP_TVAL_EL0;
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return CNTP_TVAL_EL0;
        endif
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHPS_TVAL_EL2;
        elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            return CNTHP_TVAL_EL2;
        else
            return CNTP_TVAL_EL0;
        endif
    elsif PSTATE.EL == EL3 then
        return CNTP_TVAL_EL0;
    endif
endif

MSR CNTP_TVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
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<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHPS_TVAL_EL2 = X\[t\];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        CNTHP_TVAL_EL2 = X\[t\];
    else
        CNTP_TVAL_EL0 = X\[t\];
    endif
else PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        CNTP_TVAL_EL0 = X\[t\];
    endif
else PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHPS_TVAL_EL2 = X\[t\];
    elsif HCR_EL2.<E2H,TGE> == '1' && SCR_EL3.NS == '1' then
        CNTHP_TVAL_EL2 = X\[t\];
    else
        CNTP_TVAL_EL0 = X\[t\];
    endif
else PSTATE.EL == EL3 then
    CNTP_TVAL_EL0 = X\[t\];
end if
CNTHPS_CTL_EL2, Counter-timer Secure Physical Timer Control register (EL2)

The CNTHPS_CTL_EL2 characteristics are:

**Purpose**

Control register for the Secure EL2 physical timer.

**Configuration**

AArch64 System register CNTHPS_CTL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHPS_CTL[31:0].

This register is present only when FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_CTL_EL2 are **UNDEFINED**.

**Attributes**

CNTHPS_CTL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHPS_CTL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | RES0 | RES0 | ISTATUS | IMASK | ENABLE |

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the CNTHPS_CTL_EL2.ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the CNTHPS_CTL_EL2.ENABLE bit is 0, the ISTATUS field is **UNKNOWN**.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>
For more information, see the description of the ISTATUS bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from \texttt{CNTHPS_TVAL_EL2} continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTHPS_CTL_EL2**

Accesses to this register use the following encodings:

\[ MRS \ <Xt>, \ CNTHPS\_CTL\_EL2 \]

\[ MSR \ CNTHPS\_CTL\_EL2, \ <Xt> \]
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    CNTHPS_CTL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    CNTHPS_CTL_EL2 = X[t];
MRS <Xt>, CNTP_CTL_EL0

<table>
<thead>
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<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHPS_CTL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      return CNTHP_CTL_EL2;
    else
      return CNTP_CTL_EL0;
  else
    return CNTHPS_CTL_EL2;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x180];
  else
    return CNTP_CTL_EL0;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    return CNTHPS_CTL_EL2;
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    return CNTHP_CTL_EL2;
  else
    return CNTP_CTL_EL0;
elsif PSTATE.EL == EL3 then
  return CNTP_CTL_EL0;
if PSTATE.EL == EL0 then
  if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() & HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_CTL_EL2 = X[t];
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      CNTHP_CTL_EL2 = X[t];
    else
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '0' & CNTKCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '1' & CNTKCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & CNTKCTL_EL2.EL0PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '0' &
      IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_CTL_EL2 = X[t];
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '1' then
      CNTHP_CTL_EL2 = X[t];
    else
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' & CNTKCTL_EL2.EL0PTEN == '0' &
      IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_CTL_EL2 = X[t];
    elseif EL2Enabled() & HCR_EL2.E2H == '1' & SCR_EL3.NS == '1' then
      CNTHP_CTL_EL2 = X[t];
    else
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '0' &
      IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_CTL_EL2 = X[t];
    elseif EL2Enabled() & HCR_EL2.E2H == '1' &
      IsFeatureImplemented(FEAT_SEL2) then
      CNTHP_CTL_EL2 = X[t];
    else
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' then
      NVMem[0x180] = X[t];
    else
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' then
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' then
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' then
      CNTP_CTL_EL0 = X[t];
  else
    elseif EL2Enabled() & HCR_EL2.E2H == '1' then
      CNTP_CTL_EL0 = X[t];
CNTHPS_CVAL_EL2, Counter-timer Secure Physical Timer CompareValue register (EL2)

The CNTHPS_CVAL_EL2 characteristics are:

**Purpose**

Holds the compare value for the Secure EL2 physical timer.

**Configuration**

AArch64 System register CNTHPS_CVAL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHPS_CVAL[31:0].

This register is present only when EL2 is implemented and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_CVAL_EL2 are UNDEFINED.

**Attributes**

CNTHPS_CVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHPS_CVAL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CompareValue |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  | CompareValue |

**CompareValue, bits [63:0]**

Holds the EL2 physical timer CompareValue.

When CNTHPS_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHPS_CTL_EL2.ISTATUS is set to 1.
- If CNTHPS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHPS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHPS_CVAL_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, CNTHPS_CVAL_EL2
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && SCR_EL3.NS == '1' then
        UNDEFINED;
    else
        return CNTHPS_CVAL_EL2;
elsif PSTATE.EL == EL3 then
    if SCR_EL3.EEL2 == '0' then
        UNDEFINED;
    else
        return CNTHPS_CVAL_EL2;

MSR CNTHPS_CVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
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<td>0b1110</td>
<td>0b0101</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && SCR_EL3.NS == '1' then
        UNDEFINED;
    else
        CNTHPS_CVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    if SCR_EL3.EEL2 == '0' then
        UNDEFINED;
    else
        CNTHPS_CVAL_EL2 = X[t];

MRS <Xt>, CNTP_CVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
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</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_CVAL_EL2;
      elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CVAL_EL2;
      else
        return CNTP_CVAL_EL0;
  elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x178];
    else
      return CNTP_CVAL_EL0;
  elseif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      return CNTHPS_CVAL_EL2;
    elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHP_CVAL_EL2;
    else
      return CNTP_CVAL_EL0;
  elseif PSTATE.EL == EL3 then
    return CNTP_CVAL_EL0;
else
  MSR CNTP_CVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CVAL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHP_CVAL_EL2 = X[t];
  else
    CNTP_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x178] = X[t];
  else
    CNTP_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CVAL_EL2 = X[t];
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHP_CVAL_EL2 = X[t];
  else
    CNTP_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  CNTP_CVAL_EL0 = X[t];
end if
The CNTHPS_TVAL_EL2 characteristics are:

**Purpose**

Holds the timer value for the Secure EL2 physical timer.

**Configuration**

AArch64 System register CNTHPS_TVAL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHPS_TVAL[31:0].

This register is present only when EL2 is implemented and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_TVAL_EL2 are UNDEFINED.

**Attributes**

CNTHPS_TVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHPS_TVAL_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>TimerValue</td>
</tr>
<tr>
<td>61</td>
<td>58</td>
</tr>
<tr>
<td>60</td>
<td>55</td>
</tr>
<tr>
<td>59</td>
<td>53</td>
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<tr>
<td>58</td>
<td>52</td>
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<td>57</td>
<td>50</td>
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<td>56</td>
<td>49</td>
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<td>55</td>
<td>48</td>
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<td>54</td>
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<td>53</td>
<td>46</td>
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<td>52</td>
<td>45</td>
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<td>51</td>
<td>44</td>
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<td>50</td>
<td>43</td>
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<td>49</td>
<td>42</td>
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<td>48</td>
<td>41</td>
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<td>47</td>
<td>40</td>
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<td>46</td>
<td>39</td>
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<td>45</td>
<td>38</td>
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<td>44</td>
<td>37</td>
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<td>43</td>
<td>36</td>
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<tr>
<td>42</td>
<td>35</td>
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<tr>
<td>41</td>
<td>34</td>
</tr>
<tr>
<td>40</td>
<td>33</td>
</tr>
<tr>
<td>39</td>
<td>32</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**TimerValue, bits [31:0]**

The TimerValue view of the EL2 physical timer.

On a read of this register:

- If CNTHPS_CTL_EL2.ENABLE is 0, the value returned is UNKNOWN.
- If CNTHPS_CTL_EL2.ENABLE is 1, the value returned is (CNTHPS_CVAL_EL2 - CNTPCT_EL0).

On a write of this register, CNTHPS_CVAL_EL2 is set to (CNTPCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHPS_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CNTHPS_CVAL_EL2) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHPS_CTL_EL2.ISTATUS is set to 1.
- If CNTHPS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHPS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the CNTHPS_TVAL_EL2

Accesses to this register use the following encodings:

MRS \(<X_t>, \text{CNTHPS}_TVAL_EL2\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsesif PSTATE.EL == EL1 then
  if HaveEl(EL3) \&\& SCR_EL3.NS == '1' then
    UNDEFINED;
elsesif EL2Enabled() \&\& HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    UNDEFINED;
elsesif PSTATE.EL == EL2 then
  if HaveEl(EL3) \&\& SCR_EL3.NS == '1' then
    UNDEFINED;
else
    return CNTHPS_TVAL_EL2;
elsesif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
else
    return CNTHPS_TVAL_EL2;

MSR \(\text{CNTHPS}_TVAL_EL2, <X_t>\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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<td>0b1110</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsesif PSTATE.EL == EL1 then
  if HaveEl(EL3) \&\& SCR_EL3.NS == '1' then
    UNDEFINED;
elsesif EL2Enabled() \&\& HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    UNDEFINED;
elsesif PSTATE.EL == EL2 then
  if HaveEl(EL3) \&\& SCR_EL3.NS == '1' then
    UNDEFINED;
else
    CNTHPS_TVAL_EL2 = X[t];
elsesif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
else
    CNTHPS_TVAL_EL2 = X[t];

MRS \(<X_t>, \text{CNTVAL}_EL0\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return CNTP_TVAL_EL0;
    elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_TVAL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_TVAL_EL2;
    else
        return CNTP_TVAL_EL0;
else
    return CNTP_TVAL_EL0;
endif

if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTP_TVAL_EL0;
endif

if PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_TVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
        return CNTHP_TVAL_EL2;
    else
        return CNTP_TVAL_EL0;
endif

if PSTATE.EL == EL3 then
    return CNTP_TVAL_EL0;
endif

MSR CNTP_TVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
      if EL2Enabled() && HCR_EL2.TGE == '1' then
         AArch64.SystemAccessTrap(EL2, 0x18);
      else
         AArch64.SystemAccessTrap(EL1, 0x18);
      end
   else
      if EL2Enabled() && HCR_EL2.<E2H, TGE> == '10' && CNTHCTL_EL2.EL1PCEN == '0' then
         AArch64.SystemAccessTrap(EL2, 0x18);
      elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11' && CNTHCTL_EL2.EL1PTEN == '0' then
         AArch64.SystemAccessTrap(EL2, 0x18);
      elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11' && SCR_EL3.NS == '0' &&
         IsFeatureImplemented(FEAT_SEL2) then
         CNTHPS_TVAL_EL2 = X[t];
      elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '11' && SCR_EL3.NS == '1' then
         CNTHP_TVAL_EL2 = X[t];
      else
         CNTP_TVAL_EL0 = X[t];
      end
   else
      if EL2Enabled() && HCR_EL2.<E2H, TGE> == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
         AArch64.SystemAccessTrap(EL1, 0x18);
      elsif EL2Enabled() && HCR_EL2.<E2H, TGE> == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
         AArch64.SystemAccessTrap(EL2, 0x18);
      else
         AArch64.SystemAccessTrap(EL0, 0x18);
      end
   else
      if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
         CNTHPS_TVAL_EL2 = X[t];
      elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
         CNTHP_TVAL_EL2 = X[t];
      else
         CNTP_TVAL_EL0 = X[t];
      end
   end
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      CNTP_TVAL_EL0 = X[t];
   end
elsif PSTATE.EL == EL2 then
   if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_TVAL_EL2 = X[t];
   elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      CNTHP_TVAL_EL2 = X[t];
   else
      CNTP_TVAL_EL0 = X[t];
   end
elsif PSTATE.EL == EL3 then
   CNTP_TVAL_EL0 = X[t];
CNTHV_CTL_EL2, Counter-timer Virtual Timer Control register (EL2)

The CNTHV_CTL_EL2 characteristics are:

**Purpose**

Control register for the EL2 virtual timer.

**Configuration**

AArch64 System register CNTHV_CTL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHV_CTL[31:0].

This register is present only when FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_CTL_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHV_CTL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHV_CTL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | RES0 | ISTATUS | IMASK | ENABLE |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:
**IMASK**

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTHV_TVAL_EL2** continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTHV_CTL_EL2**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL2 using the mnemonic **CNTHV_CTL_EL2** or **CNTV_CTL_EL0** are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, CNTHV_CTL_EL2**

```asm
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHV_CTL_EL2;
elsif PSTATE.EL == EL3 then
    return CNTHV_CTL_EL2;
end

MSR CNTHV_CTL_EL2, <Xt>
```

**MSR CNTHV_CTL_EL2, <Xt>**

```asm
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHV_CTL_EL2;
elsif PSTATE.EL == EL3 then
    return CNTHV_CTL_EL2;
end
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHV_CTL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHV_CTL_EL2 = X[t];

MRS <Xt>, CNTV_CTL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && SCR_EL3.NS == '1' then
        if IsFeatureImplemented(FEAT_SEL2) then
            return CNTHV_CTL_EL2;
        else
            return CNTHV_CTL_EL0;
        end
    elsif EL2Enabled() && SCR_EL3.NS == '0' then
        if IsFeatureImplemented(FEAT_SEL2) then
            return CNTHV_CTL_EL2;
        else
            return CNTHV_CTL_EL0;
        end
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x170];
    else
        return CNTV_CTL_EL0;
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHV_CTL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
        return CNTHV_CTL_EL2;
    else
        return CNTHV_CTL_EL0;
    end
elsif PSTATE.EL == EL3 then
    return CNTV_CTL_EL0;

MSR CNTV_CTL_EL0, <Xt>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> !='11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CTL_EL2 = X[t];
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHV_CTL_EL2 = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x170] = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
elseif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
     IsFeatureImplemented(FEAT_SEL2) then
    CNTHV_CTL_EL2 = X[t];
  elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHV_CTL_EL2 = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
elseif PSTATE.EL == EL3 then
  CNTV_CTL_EL0 = X[t];
endif

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The CNTHV_CVAL_EL2 characteristics are:

**Purpose**

Holds the compare value for the EL2 virtual timer.

**Configuration**

AArch64 System register CNTHV_CVAL_EL2 bits [63:0] are architecturally mapped to AArch32 System register CNTHV_CVAL[63:0].

This register is present only when FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_CVAL_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHV_CVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHV_CVAL_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CompareValue</td>
</tr>
<tr>
<td>62</td>
<td>CompareValue</td>
</tr>
<tr>
<td>61</td>
<td>CompareValue</td>
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<td>60</td>
<td>CompareValue</td>
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<td>3</td>
<td>CompareValue</td>
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<tr>
<td>2</td>
<td>CompareValue</td>
</tr>
<tr>
<td>1</td>
<td>CompareValue</td>
</tr>
<tr>
<td>0</td>
<td>CompareValue</td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL2 virtual timer CompareValue.

When CNTHV_CTL_EL2 ENABLE is 1, the timer condition is met when (CNTVCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHV_CTL_EL2.ISTATUS is set to 1.
- If CNTHV_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHV_CTL_EL2 ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHV_CVAL_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CNTHV_CVAL_EL2 or CNTV_CVAL_EL0 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:
MRS <Xt>, CNTHV_CVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHV_CVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHV_CVAL_EL2 = X[t];

MSR CNTHV_CVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
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<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHV_CVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTHV_CVAL_EL2 = X[t];

MRS <Xt>, CNTV_CVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
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<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTKCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHVS_CVAL_EL2;
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      return CNTHV_CVAL_EL2;
    else
      return CNTV_CVAL_EL0;
  elseif PSTATE_EL == EL1 then
    if EL2Enabled() && CNTKCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x168];
    else
      return CNTV_CVAL_EL0;
  elseif PSTATE_EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHVS_CVAL_EL2;
    elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHV_CVAL_EL2;
    else
      return CNTV_CVAL_EL0;
  elseif PSTATE_EL == EL3 then
  return CNTV_CVAL_EL0;
else
  return CNTV_CVAL_EL0;

MSR CNTV_CVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
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<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      CNTHVS_CVAL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      CNTHV_CVAL_EL2 = X[t];
    else
      CNTV_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x168] = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CVAL_EL2 = X[t];
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  CNTV_CVAL_EL0 = X[t];
CNTHV_TVAL_EL2, Counter-timer Virtual Timer

TimerValue Register (EL2)

The CNTHV_TVAL_EL2 characteristics are:

Purpose

Holds the timer value for the EL2 virtual timer.

Configuration

AArch64 System register CNTHV_TVAL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHV_TVAL[31:0].

This register is present only when FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_TVAL_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

Attributes

CNTHV_TVAL_EL2 is a 64-bit register.

Field descriptions

The CNTHV_TVAL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TimerValue |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:32]

Reserved, RES0.

TimerValue, bits [31:0]

The TimerValue view of the EL2 virtual timer.

On a read of this register:

- If CNTHV_CTL_EL2.ENABLE is 0, the value returned is UNKNOWN.
- If CNTHV_CTL_EL2.ENABLE is 1, the value returned is (CNTHV_CVAL_EL2 - CNTVCT_EL0).

On a write of this register, CNTHV_CVAL_EL2 is set to (CNTVCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHV_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTVCT_EL0 - CNTHV_CVAL_EL2) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHV_CTL_EL2.ISTATUS is set to 1.
- If CNTHV_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHV_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the CNTHV_TVAL_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CNTHV_TVAL_EL2 or CNTV_TVAL_EL0 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CNTHV_TVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return CNTHV_TVAL_EL2;
elsif PSTATE.EL == EL3 then
  return CNTHV_TVAL_EL2;

MRS CNTHV_TVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
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<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  CNTHV_TVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  CNTHV_TVAL_EL2 = X[t];

MRS <Xt>, CNTV_TVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
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<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTTHCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_TVAL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHV_TVAL_EL2;
  else
    return CNTV_TVAL_EL0;
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CNTV_TVAL_EL0;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
      IsFeatureImplemented(FEAT_SEL2) then
      return CNTHVS_TVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHV_TVAL_EL2;
    else
      return CNTV_TVAL_EL0;
    end
elsif PSTATE.EL == EL3 then
  return CNTV_TVAL_EL0;
else
  return CNTV_TVAL_EL0;
end

MSR CNTV_TVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
            CNTHVS_TVAL_EL2 = X[t];
        elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            CNTHV_TVAL_EL2 = X[t];
        else
            CNTV_TVAL_EL0 = X[t];
    end
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            CNTV_TVAL_EL0 = X[t];
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
            CNTHVS_TVAL_EL2 = X[t];
        elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            CNTHV_TVAL_EL2 = X[t];
        else
            CNTV_TVAL_EL0 = X[t];
    elsif PSTATE.EL == EL3 then
        CNTV_TVAL_EL0 = X[t];
end
CNTHVS_CTL_EL2, Counter-timer Secure Virtual Timer Control register (EL2)

The CNTHVS_CTL_EL2 characteristics are:

**Purpose**

Control register for the Secure EL2 virtual timer.

**Configuration**

AArch64 System register CNTHVS_CTL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHVS_CTL[31:0].

This register is present only when EL2 is implemented and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_CTL_EL2 are UNDEFINED.

**Attributes**

CNTHVS_CTL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHVS_CTL_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
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<td>60</td>
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<td>46</td>
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<td>45</td>
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<td></td>
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<tr>
<td>44</td>
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<td>43</td>
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<td>42</td>
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<td>41</td>
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<td>40</td>
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<td>39</td>
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<td>38</td>
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<td>37</td>
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<tr>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>ISTATUS</td>
<td>The status of the timer. This bit indicates whether the timer condition is met:</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
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<td>5</td>
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<td>4</td>
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<td>3</td>
<td></td>
<td></td>
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<tr>
<td>2</td>
<td></td>
<td></td>
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<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the CNTHVS_CTL_EL2.ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>
For more information, see the description of the CNTHVS_CTL_EL2.ISTATUS bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTHVS_TVAL_EL2** continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the CNTHVS_CTL_EL2

Accesses to this register use the following encodings:

**MRS <Xt>, CNTHVS_CTL_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && SCR_EL3.NS == '1' then
            UNDEFINED;
        else
            return CNTHVS_CTL_EL2;
    elsif PSTATE.EL == EL3 then
        if SCR_EL3.EEL2 == '0' then
            UNDEFINED;
        else
            return CNTHVS_CTL_EL2;
else
    MSR CNTHVS_CTL_EL2, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  end if
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    CNTHVS_CTL_EL2 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    CNTHVS_CTL_EL2 = X[t];
  end if
end if

MRS <Xt>, CNTV_CTL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_CTL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHV_CTL_EL2;
  else
    return CNTV_CTL_EL0;
  end if
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x170];
  else
    return CNTV_CTL_EL0;
  end if
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_CTL_EL2;
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    return CNTHV_CTL_EL2;
  else
    return CNTHV_CTL_EL2;
  end if
elsif PSTATE.EL == EL3 then
  return CNTV_CTL_EL0;
else
  return CNTV_CTL_EL0;
end if

MSR CNTV_CTL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CTL_EL2 = X[t];
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHVS_CTL_EL2 = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
endif

elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x170] = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
endif

elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CTL_EL2 = X[t];
  elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHV_CTL_EL2 = X[t];
  else
    CNTV_CTL_EL0 = X[t];
  endif
endif

elsif PSTATE.EL == EL3 then
  CNTV_CTL_EL0 = X[t];
endif
CNTHVS_CVAL_EL2, Counter-timer Secure Virtual Timer CompareValue register (EL2)

The CNTHVS_CVAL_EL2 characteristics are:

**Purpose**

Holds the compare value for the Secure EL2 virtual timer.

**Configuration**

AArch64 System register CNTHVS_CVAL_EL2 bits [63:0] are architecturally mapped to AArch32 System register CNTHVS_CVAL[63:0].

This register is present only when EL2 is implemented and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_CVAL_EL2 are UNDEFINED.

**Attributes**

CNTHVS_CVAL_EL2 is a 64-bit register.

**Field descriptions**

The CNTHVS_CVAL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CompareValue |
| CompareValue |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**CompareValue, bits [63:0]**

Holds the Secure EL2 virtual timer CompareValue.

When CNTHVS_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTVCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHVS_CTL_EL2.ISTATUS is set to 1.
- If CNTHVS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHVS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHVS_CVAL_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, CNTHVS_CVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

Page 216
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    return CNTHVS_CVAL_EL2;
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    return CNTHVS_CVAL_EL2;

MSR CNTHVS_CVAL_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    CNTHVS_CVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    CNTHVS_CVAL_EL2 = X[t];

MRS <Xt>, CNTV_CVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
       IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_CVAL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHV_CVAL_EL2;
  else
    return CNTV_CVAL_EL0;
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1VT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x168];
    else
      return CNTV_CVAL_EL0;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
       IsFeatureImplemented(FEAT_SEL2) then
      return CNTHVS_CVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      return CNTHV_CVAL_EL2;
    else
      return CNTV_CVAL_EL0;
  elsif PSTATE.EL == EL3 then
    return CNTV_CVAL_EL0;
else
  return CNTHV_CVAL_EL2;

MSR CNTV_CVAL_EL0, <Xt>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CVAL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x168] = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CVAL_EL2 = X[t];
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  CNTV_CVAL_EL0 = X[t];
endif

The CNTHVS_TVAL_EL2 characteristics are:

Purpose

Holds the timer value for the Secure EL2 virtual timer.

Configuration

AArch64 System register CNTHVS_TVAL_EL2 bits [31:0] are architecturally mapped to AArch32 System register CNTHVS_TVAL[31:0].

This register is present only when EL2 is implemented and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_TVAL_EL2 are UNDEFINED.

Attributes

CNTHVS_TVAL_EL2 is a 64-bit register.

Field descriptions

The CNTHVS_TVAL_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

Bits [63:32]

Reserved, RES0.

TimerValue, bits [31:0]

The TimerValue view of the EL2 virtual timer.

On a read of this register:

- If CNTHVS_CTL_EL2.ENABLE is 0, the value returned is UNKNOWN.
- If CNTHVS_CTL_EL2.ENABLE is 1, the value returned is (CNTHVS_CVAL_EL2 - CNTVCT_EL0).

On a write of this register, CNTHVS_CVAL_EL2 is set to (CNTVCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHVS_CTL_EL2.ENABLE is 1, the timer condition is met when ((CNTVCT_EL0 - CNTHVS_CVAL_EL2) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHVS_CTL_EL2.ISTATUS is set to 1.
- If CNTHVS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHVS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the CNTHVS_TVAL_EL2

Accesses to this register use the following encodings:

MRS `<Xt>`, CNTHVS_TVAL_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
else
  return CNTHVS_TVAL_EL2;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    return CNTHVS_TVAL_EL2;
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    CNTHVS_TVAL_EL2 = X[t];
else
  CNTHVS_TVAL_EL2 = X[t];

MSR CNTHVS_TVAL_EL2, `<Xt>`

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    CNTHVS_TVAL_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
else
  CNTHVS_TVAL_EL2 = X[t];

MRS `<Xt>`, CNTV_TVAL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    end if
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
          IsFeatureImplemented(FEAT_SEL2) then
        return CNTHVS_TVAL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHV_TVAL_EL2;
    else
        return CNTV_TVAL_EL0;
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTV_TVAL_EL0;
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
          IsFeatureImplemented(FEAT_SEL2) then
        return CNTHVS_TVAL_EL2;
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
        return CNTHV_TVAL_EL2;
    else
        return CNTV_TVAL_EL0;
    end if
elsif PSTATE.EL == EL3 then
    return CNTV_TVAL_EL0;
end if

MSR CNTV_TVAL_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        CNTV_TVAL_EL0 = X[t];
    end;
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            CNTV_TVAL_EL0 = X[t];
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
            CNTHVS_TVAL_EL2 = X[t];
        elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            CNTHV_TVAL_EL2 = X[t];
        else
            CNTV_TVAL_EL0 = X[t];
    elseif PSTATE.EL == EL3 then
        CNTV_TVAL_EL0 = X[t];
else
    CNTV_TVAL_EL0 = X[t];
CNTKCTL_EL1, Counter-timer Kernel Control register

The CNTKCTL_EL1 characteristics are:

**Purpose**

When FEAT_VHE is not implemented, or when HCR_EL2.E2H, TGE is not {1, 1}, this register controls the generation of an event stream from the virtual counter; and access from EL0 to the physical counter, virtual counter, EL1 physical timers, and the virtual timer.

When FEAT_VHE is implemented and HCR_EL2.E2H, TGE is {1, 1}, this register does not cause any event stream from the virtual counter to be generated, and does not control access to the counters and timers. The access to counters and timers at EL0 is controlled by CNTHCTL_EL2.

**Configuration**

AArch64 System register CNTKCTL_EL1 bits [31:0] are architecturally mapped to AArch32 System register CNTKCTL[31:0].

**Attributes**

CNTKCTL_EL1 is a 64-bit register.

**Field descriptions**

The CNTKCTL_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:18</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td>EVNTIS, bit [17]</td>
</tr>
<tr>
<td></td>
<td>Controls the scale of the generation of the event stream.</td>
</tr>
<tr>
<td>EVNTIS</td>
<td>Meaning</td>
</tr>
<tr>
<td>0b0</td>
<td>The CNTKCTL_EL1.EVNTI field applies to CNTVCT_EL0[15:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>The CNTKCTL_EL1.EVNTI field applies to CNTVCT_EL0[23:8].</td>
</tr>
</tbody>
</table>

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
Bits [16:10]
Reserved, RES0.

ELOPTEN, bit [9]
Traps EL0 accesses to the physical timer registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and \texttt{HCR\_EL2.TGE} is 1, as follows:

- In AArch64 state, the following registers are trapped, reported using EC syndrome value 0x18:
  - \texttt{CNTP\_CTL\_EL0}, \texttt{CNTP\_CVAL\_EL0}, and \texttt{CNTP\_TVAL\_EL0}.
- In AArch32 state, MRC and MCR accesses to the following registers are trapped, reported using EC syndrome value 0x03, MRRC and MCRR accesses are trapped, reported using EC syndrome value 0x04:
  - \texttt{CNTP\_CTL}, \texttt{CNTP\_CVAL}, \texttt{CNTP\_TVAL}.

<table>
<thead>
<tr>
<th>ELOPTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the physical timer registers are trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When \texttt{FEAT\_VHE} is implemented and \texttt{HCR\_EL2.(E2H, TGE) is \{1, 1\}}, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ELOVTEN, bit [8]
Traps EL0 accesses to the virtual timer registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and \texttt{HCR\_EL2.TGE} is 1, as follows:

- In AArch64 state, accesses to the following registers are trapped, reported using EC syndrome value 0x18:
  - \texttt{CNTV\_CTL\_EL0}, \texttt{CNTV\_CVAL\_EL0}, and \texttt{CNTV\_TVAL\_EL0}.
- In AArch32 state, MRC and MCR accesses to the following registers are trapped and reported using EC syndrome value 0x03, MRRC and MCRR accesses are trapped using EC syndrome value 0x04:
  - \texttt{CNTV\_CTL}, \texttt{CNTV\_CVAL}, and \texttt{CNTV\_TVAL}.

<table>
<thead>
<tr>
<th>ELOVTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the virtual timer registers are trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When \texttt{FEAT\_VHE} is implemented and \texttt{HCR\_EL2.(E2H, TGE) is \{1, 1\}}, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EVNTI, bits [7:4]
Selects which bit of the counter register \texttt{CNTVCT\_EL0} is the trigger for the event stream generated from that counter, when that stream is enabled.

If \texttt{FEAT\_ECV} is implemented, and \texttt{CNTKCTL\_EL1.EVTIS} is 1, this field selects a trigger bit in the range 8 to 23 of the counter register \texttt{CNTVCT\_EL0}.

Otherwise, this field selects a trigger bit in the range 0 to 15 of the counter register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EVNTDIR, bit [3]
Controls which transition of the counter register \texttt{CNTVCT\_EL0} trigger bit, defined by EVNTI, generates an event when the event stream is enabled.
## EVNTDIR

<table>
<thead>
<tr>
<th>Meanings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A 0 to 1 transition of the trigger bit triggers an event.</td>
</tr>
<tr>
<td>0b1</td>
<td>A 1 to 0 transition of the trigger bit triggers an event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EVNTEN, bit [2]

When FEAT_VHE is not implemented, or when HCR_EL2.E2H, TGE is not \{1, 1\}, enables the generation of an event stream from the counter register CNTVCT_EL0.

<table>
<thead>
<tr>
<th>Meanings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables the event stream.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables the event stream.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented and HCR_EL2.E2H, TGE is \{1, 1\}, this control does not enable the event stream.

On a Warm reset, this field resets to 0.

### EL0VCTEN, bit [1]

Traps EL0 accesses to the frequency register and virtual counter register to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, as follows:

- In AArch64 state, accesses to the following registers are trapped and reported using EC syndrome value 0x18:
  - CNTVCT_EL0 if CNTKCTL_EL1.EL0PCTEN is 0, CNTFRQ_EL0.
- In AArch32 state, MRC and MCR accesses to the following registers are trapped and reported using EC syndrome value 0x03, MRRC and MCRR accesses are trapped and reported using EC syndrome value 0x04:
  - CNTVCT and if CNTKCTL_EL1.EL0PCTEN is 0, CNTFRQ.

<table>
<thead>
<tr>
<th>Meanings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the frequency register and virtual counter registers are trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented and HCR_EL2.E2H, TGE is \{1, 1\}, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EL0PCTEN, bit [0]

Traps EL0 accesses to the frequency register and physical counter register to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, as follows:

- In AArch64 state, the following registers are trapped, reported using EC syndrome value 0x18:
  - CNTPCT_EL0 if CNTKCTL_EL1.EL0PCTEN is 0, CNTFRQ_EL0.
- In AArch32 state, MCR or MRC accesses the following registers are trapped, reported using EC syndrome value 0x03, MCRR or MRRC accesses are trapped and reported using EC syndrome value 0x04:
  - CNTPCT and if CNTKCTL_EL1.EL0PCTEN is 0, CNTFRQ.

<table>
<thead>
<tr>
<th>Meanings</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the frequency register and physical counter register are trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented and HCR_EL2.E2H, TGE is \{1, 1\}, this control does not cause any instructions to be trapped.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Accessing the CNTKCTL_EL1

When \texttt{HCR\_EL2.E2H} is 1, without explicit synchronization, access from EL3 using the mnemonic CNTKCTL\_EL1 or CNTKCTL\_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

\texttt{MRS <Xt>, CNTKCTL\_EL1}

\begin{verbatim}
\begin{verbatim}
\begin{tabular}{|c|c|c|c|c|}
\hline
 op0 & op1 & CRn & CRm & op2 \\
\hline
 0b11 & 0b000 & 0b1110 & 0b0001 & 0b000 \\
\hline
\end{tabular}
\end{verbatim}
\end{verbatim}

\begin{verbatim}
if \texttt{PSTATE.EL == EL0} then
\texttt{UNDEFINED};
elsif \texttt{PSTATE.EL == EL1} then
return \texttt{CNTKCTL\_EL1};
elsif \texttt{PSTATE.EL == EL2} then
  if \texttt{HCR\_EL2.E2H == '1'} then
    return \texttt{CNTKCTL\_EL2};
  else
    return \texttt{CNTKCTL\_EL1};
elsif \texttt{PSTATE.EL == EL3} then
return \texttt{CNTKCTL\_EL1};
\end{verbatim}

\texttt{MSR CNTKCTL\_EL1, <Xt>}

\begin{verbatim}
\begin{verbatim}
\begin{tabular}{|c|c|c|c|c|}
\hline
 op0 & op1 & CRn & CRm & op2 \\
\hline
 0b11 & 0b000 & 0b1110 & 0b0001 & 0b000 \\
\hline
\end{tabular}
\end{verbatim}
\end{verbatim}

\begin{verbatim}
if \texttt{PSTATE.EL == EL0} then
\texttt{UNDEFINED};
elsif \texttt{PSTATE.EL == EL1} then
  \texttt{CNTKCTL\_EL1 = X[t]};
elsif \texttt{PSTATE.EL == EL2} then
  if \texttt{HCR\_EL2.E2H == '1'} then
    \texttt{CNTKCTL\_EL2 = X[t]};
  else
    \texttt{CNTKCTL\_EL1 = X[t]};
elsif \texttt{PSTATE.EL == EL3} then
  \texttt{CNTKCTL\_EL1 = X[t]};
\end{verbatim}

\texttt{MRS <Xt>, CNTKCTL\_EL12}

\begin{verbatim}
\begin{verbatim}
\begin{tabular}{|c|c|c|c|c|}
\hline
 op0 & op1 & CRn & CRm & op2 \\
\hline
 0b11 & 0b101 & 0b1110 & 0b0001 & 0b000 \\
\hline
\end{tabular}
\end{verbatim}
\end{verbatim}

\begin{verbatim}
if \texttt{PSTATE.EL == EL0} then
\texttt{UNDEFINED};
elsif \texttt{PSTATE.EL == EL1} then
  \texttt{CNTKCTL\_EL1 = X[t]};
elsif \texttt{PSTATE.EL == EL2} then
  if \texttt{HCR\_EL2.E2H == '1'} then
    \texttt{CNTKCTL\_EL2 = X[t]};
  else
    \texttt{CNTKCTL\_EL1 = X[t]};
elsif \texttt{PSTATE.EL == EL3} then
  \texttt{CNTKCTL\_EL1 = X[t]};
\end{verbatim}
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return CNTKCTL_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return CNTKCTL_EL1;
    else
        UNDEFINED;

MSR CNTKCTL_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CNTKCTL_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        CNTKCTL_EL1 = X[t];
    else
        UNDEFINED;
The CNTP_CTL_EL0 characteristics are:

**Purpose**

Control register for the EL1 physical timer.

**Configuration**

AArch64 System register CNTP_CTL_EL0 bits [31:0] are architecturally mapped to AArch32 System register CNTP_CTL[31:0].

**Attributes**

CNTP_CTL_EL0 is a 64-bit register.

**Field descriptions**

The CNTP_CTL_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>ISTATUS</td>
</tr>
<tr>
<td>60</td>
<td>IMASK</td>
</tr>
<tr>
<td>59</td>
<td>ENABLE</td>
</tr>
<tr>
<td>58</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>RES0</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTP_TVAL_EL0** continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTP_CTL_EL0**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL3 using the mnemonic **CNTP_CTL_EL0** or **CNTP_CTL_EL02** are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CNTP_CTL_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' then
            AArch64.SystemAccessTrap(EL1, 0x18);
        elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
        return CNTHPS_CTL_EL2;
    endif
    else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHPS_CTL_EL2;
        elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            return CNTHP_CTL_EL2;
        else
            return CNTP_CTL_EL0;
        endif
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' &
            CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
            return NVMem[0x180];
        else
            return CNTP_CTL_EL0;
        endif
    elseif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHPS_CTL_EL2;
        elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            return CNTHP_CTL_EL2;
        else
            return CNTP_CTL_EL0;
        endif
    elseif PSTATE.EL == EL3 then
        return CNTP_CTL_EL0;
    endif
endif

MSR CNTP_CTL_EL0, <xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTPS_CTL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<E2H,TGE> == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
    CNTHPS_CTL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CTL_EL2 = X[t];
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  CNTP_CTL_EL0 = X[t];
endif
MRS <Xt>, CNTP_CTL_EL02

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b01</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTKCTL_EL2.ELINVPCT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return NVMem[0x180];
    endif
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    CNTHPS_CTL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '110' then
    CNTHP_CTL_EL2 = X[t];
  else
    CNTP_CTL_EL0 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return CNTP_CTL_EL0;
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return CNTP_CTL_EL0;
  else
    UNDEFINED;
  endif
endif
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1NVPCT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      NVMem[0x180] = X[t];
    endif
  else
    AArch64.SystemAccessTrap(EL2, 0x18);
  endif
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    CNTP_CTL_EL0 = X[t];
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    CNTP_CTL_EL0 = X[t];
  else
    UNDEFINED;
  endif
endif

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
CNTP_CVAL_EL0, Counter-timer Physical Timer CompareValue register

The CNTP_CVAL_EL0 characteristics are:

**Purpose**

Holds the compare value for the EL1 physical timer.

**Configuration**

AArch64 System register CNTP_CVAL_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTP_CVAL[63:0].

**Attributes**

CNTP_CVAL_EL0 is a 64-bit register.

**Field descriptions**

The CNTP_CVAL_EL0 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

CompareValue, bits [63:0]

Holds the EL1 physical timer CompareValue.

When \texttt{CNTP_CTL_EL0.ENABLE} is 1, the timer condition is met when (\texttt{CNTPCT_EL0} - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- \texttt{CNTP_CTL_EL0.ISTATUS} is set to 1.
- If \texttt{CNTP_CTL_EL0.IMASK} is 0, an interrupt is generated.

When \texttt{CNTP_CTL_EL0.ENABLE} is 0, the timer condition is not met, but \texttt{CNTPCT_EL0} continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTP_CVAL_EL0**

When \texttt{HCR_EL2.E2H} is 1, without explicit synchronization, access from EL3 using the mnemonic CNTP_CVAL_EL0 or CNTP_CVAL_EL02 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

- \texttt{MRS <Xt>, CNTP_CVAL_EL0}
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_CVAL_EL2;
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CVAL_EL2;
    else
        return CNTP_CVAL_EL0;
else
    elseif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && HCR_EL2.E2H == '1' && CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
            return NVMem[0x178];
        else
            return CNTP_CVAL_EL0;
    elseif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHPS_CVAL_EL2;
        elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            return CNTHP_CVAL_EL2;
        else
            return CNTP_CVAL_EL0;
    elseif PSTATE.EL == EL3 then
        return CNTP_CVAL_EL0;

MSR CNTP_CVAL_EL0, <Xt>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  endif
  elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTTHCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTTHPS_CVAL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHP_CVAL_EL2 = X[t];
  else
    CNTP_CVAL_EL0 = X[t];
  endif
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTTHCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
      if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTTHCTL_EL2.EL1NVPCT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      else
        return NVMem[0x178];
      endif
    else
      UNDEFINED;
    endif
  endwhile
else
  if PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      return CNTP_CVAL_EL0;
    else
      UNDEFINED;
    endif
  endwhile
else
  if PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
      return CNTP_CVAL_EL0;
    else
      UNDEFINED;
    endif
  endwhile
else
  UNDEFINED;
endif

MRS <Xt>, CNTP_CVAL_EL02

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
else
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTTHCTL_EL2.EL1NVPCT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return NVMem[0x178];
    endif
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  endif
else
  if PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      return CNTP_CVAL_EL0;
    else
      UNDEFINED;
    endif
  else
    UNDEFINED;
  endif
else
  if PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
      return CNTP_CVAL_EL0;
    else
      UNDEFINED;
    endif
  endif
else
  UNDEFINED;
endif
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1NVPCT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            NVMem[0x178] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CNTP_CVAL_EL0 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        CNTP_CVAL_EL0 = X[t];
    else
        UNDEFINED;
The CNTP_TVAL_EL0 characteristics are:

**Purpose**

Holds the timer value for the EL1 physical timer.

**Configuration**

AArch64 System register CNTP_TVAL_EL0 bits [31:0] are architecturally mapped to AArch32 System register \texttt{CNTP\_TVAL\[31:0].}

**Attributes**

CNTP_TVAL_EL0 is a 64-bit register.

**Field descriptions**

The CNTP_TVAL_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    |    |    |    |    |    |    |    |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|    |

**Bits [63:32]**

Reserved, RES0.

**TimerValue, bits [31:0]**

The TimerValue view of the EL1 physical timer.

On a read of this register:

- If \texttt{CNTP\_CTL\_EL0.ENABLE} is 0, the value returned is unknown.
- If \texttt{CNTP\_CTL\_EL0.ENABLE} is 1, the value returned is \((\texttt{CNTP\_CVAL\_EL0} - \texttt{CNTPCT\_EL0}).

On a write of this register, \texttt{CNTP\_CVAL\_EL0} is set to \((\texttt{CNTPCT\_EL0} + \text{TimerValue}), where TimerValue is treated as a signed 32-bit integer:

When \texttt{CNTP\_CTL\_EL0.ENABLE} is 1, the timer condition is met when \((\texttt{CNTPCT\_EL0} - \texttt{CNTP\_CVAL\_EL0})\) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- \texttt{CNTP\_CTL\_EL0.ISTATUS} is set to 1.
- If \texttt{CNTP\_CTL\_EL0.IMASK} is 0, an interrupt is generated.

When \texttt{CNTP\_CTL\_EL0.ENABLE} is 0, the timer condition is not met, but \texttt{CNTPCT\_EL0} continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally unknown value.
**Accessing the CNTP_TVAL_EL0**

When `HCR_EL2.E2H` is 1, without explicit synchronization, access from EL3 using the mnemonic `CNTP_TVAL_EL0` or `CNTP_TVAL_EL02` are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```
MRS <Xt>, CNTP_TVAL_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if `PSTATE.EL == EL0` then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    return CNTHPS_TVAL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHP_TVAL_EL2;
  else
    return CNTP_TVAL_EL0;
else
  if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CNTP_TVAL_EL0;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    return CNTHPS_TVAL_EL2;
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    return CNTHP_TVAL_EL2;
  else
    return CNTP_TVAL_EL0;
elsif PSTATE.EL == EL3 then
  return CNTP_TVAL_EL0;
```

```
MSR CNTP_TVAL_EL0, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
    IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_TVAL_EL2 = X[t];
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTP_TVAL_EL0 = X[t];
else
  CNTP_TVAL_EL0 = X[t];
else
  CNTP_TVAL_EL0 = X[t];
else
  CNTP_TVAL_EL0 = X[t];
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
   elsif EL2Enabled() && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
  else
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      CNTHPS_TVAL_EL2 = X[t];
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
      CNTP_TVAL_EL2 = X[t];
    else
      UNDEFINED;
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
      return CNTP_TVAL_EL0;
    else
      UNDEFINED;
  else
    if PSTATE.EL == EL3 then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return CNTP_TVAL_EL0;
    else
        UNDEFINED;

MRS <Xt>, CNTP_TVAL_EL02

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return CNTP_TVAL_EL0;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return CNTP_TVAL_EL0;
else
  UNDEFINED;

MSR CNTP_TVAL_EL02, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CNTP_TVAL_EL0 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        CNTP_TVAL_EL0 = X[t];
    else
        UNDEFINED;
CNTPCT_EL0, Counter-timer Physical Count register

The CNTPCT_EL0 characteristics are:

Purpose

Holds the 64-bit physical count value.

Configuration

AArch64 System register CNTPCT_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTPCT[63:0].

All reads to the CNTPCT_EL0 occur in program order relative to reads to CNTPCTSS_EL0 or CNTPCT_EL0.

Attributes

CNTPCT_EL0 is a 64-bit register.

Field descriptions

The CNTPCT_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    | Physical count value |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

Bits [63:0]

Physical count value.

Reads of CNTPCT_EL0 from EL0 or EL1 return (PCount<63:0> - CNTPOFF_EL2<63:0>) if the access is not trapped, and all of the following are true:

- CNTHCTL_EL2.ECV is 1.
- HCR_EL2.{E2H, TGE} is not {1, 1}.

Where PCount<63:0> is the physical count returned when CNTPCT_EL0 is read from EL2 or EL3.

Accessing the CNTPCT_EL0

Accesses to this register use the following encodings:

MRS <Xt>, CNTPCT_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PCTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL0PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTPCT_EL0;
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTPCT_EL0;
    end if
elsif PSTATE.EL == EL2 then
    return CNTPCT_EL0;
elsif PSTATE.EL == EL3 then
    return CNTPCT_EL0;
CNTPCTSS_EL0, Counter-timer Self-Synchronized Physical Count register

The CNTPCTSS_EL0 characteristics are:

**Purpose**

Holds the self-synchronized view of the 64-bit physical count value.

**Configuration**

AArch64 System register CNTPCTSS_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTPCTSS[63:0].

This register is present only when FEAT_ECV is implemented. Otherwise, direct accesses to CNTPCTSS_EL0 are UNDEFINED.

All reads to the CNTPCTSS_EL0 occur in program order relative to reads to CNTPCT_EL0 or CNTPCTSS_EL0.

This register is a self-synchronised view of the CNTPCT_EL0 counter, and cannot be read speculatively.

**Attributes**

CNTPCTSS_EL0 is a 64-bit register.

**Field descriptions**

The CNTPCTSS_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Self-synchronized physical count</td>
</tr>
<tr>
<td>62</td>
<td>value</td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
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<td>56</td>
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<td>55</td>
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<td>54</td>
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<td>53</td>
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<td>51</td>
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<td>48</td>
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<td>42</td>
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<td>7</td>
<td></td>
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<td>6</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Accessing the CNTPCTSS_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, CNTPCTSS_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') & CNTKCTL_EL1.EL0PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    elseif EL2Enabled() & HCR_EL2.E2H == '0' & CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '10' & CNTHCTL_EL2.EL0PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & CNTHCTL_EL2.EL0PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTPCTSS_EL0;
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTPCTSS_EL0;
    endif
elsif PSTATE.EL == EL2 then
    return CNTPCTSS_EL0;
elsif PSTATE.EL == EL3 then
    return CNTPCTSS_EL0;

The CNTPOFF_EL2 characteristics are:

### Purpose

Holds the 64-bit physical offset. This is the offset for the AArch64 physical timers and counters when Enhanced Counter Virtualization is enabled.

### Configuration

This register is present only when FEAT_ECV is implemented. Otherwise, direct accesses to CNTPOFF_EL2 are **UNDEFINED**.

The offsetting of the timers and counters based on EL2 using AArch64 apply at:

- EL1 when EL1 is using AArch64 or AArch32.
- EL0 when EL0 is using AArch64 or AArch32.

When EL2 is implemented and enabled in the current Security state, the physical counter uses a fixed physical offset of zero if either of the following are true:

- **CNTHCTL_EL2.ECV** is 0.
- **SCR_EL3.ECVEn** is 0.
- **HCR_EL2.{E2H, TGE}** is {1, 1}.

### Attributes

CNTPOFF_EL2 is a 64-bit register.

### Field descriptions

The CNTPOFF_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62-0</td>
<td>Physical offset</td>
</tr>
</tbody>
</table>

| Bits [63:0] |

Physical offset.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the CNTPOFF_EL2

Accesses to this register use the following encodings:

```
MRS <Xt>, CNTPOFF_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x1A8];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
        priority when SDD == '1'" && SCR_EL3.ECVEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ECVEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return CNTPOFF_EL2;
    end
elsif PSTATE.EL == EL3 then
    return CNTPOFF_EL2;
 end

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x1A8] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
        priority when SDD == '1'" && SCR_EL3.ECVEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ECVEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        CNTPOFF_EL2 = X[t];
    end
elsif PSTATE.EL == EL3 then
    CNTPOFF_EL2 = X[t];
end
CNTPS_CTL_EL1, Counter-timer Physical Secure Timer Control register

The CNTPS_CTL_EL1 characteristics are:

**Purpose**

Control register for the secure physical timer, usually accessible at EL3 but configurably accessible at EL1 in Secure state.

**Configuration**

There are no configuration notes.

**Attributes**

CNTPS_CTL_EL1 is a 64-bit register.

**Field descriptions**

The CNTPS_CTL_EL1 bit assignments are:

|       | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|-------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|       | RES0 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
|       | RES0 |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |
| 31    | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTPS_TVAL_EL1** continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the CNTPS_CTL_EL1

Accesses to this register use the following encodings:

**MRS <Xt>, CNTPS_CTL_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '0' then
        if SCR_EL3.EEL2 == '1' then
            UNDEFINED;
        elseif SCR_EL3.ST == '0' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return CNTPS_CTL_EL1;
        end
    endif
else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return CNTPS_CTL_EL1;
```

**MSR CNTPS_CTL_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '0' then
    if SCR_EL3.EEL2 == '1' then
      UNDEFINED;
    elsif SCR_EL3.ST == '0' then
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      CNTPS_CTL_EL1 = X[t];
  else
    UNDEFINED;
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  CNTPS_CTL_EL1 = X[t];
CNTPS_CVAL_EL1, Counter-timer Physical Secure Timer CompareValue register

The CNTPS_CVAL_EL1 characteristics are:

Purpose

Holds the compare value for the secure physical timer, usually accessible at EL3 but configurably accessible at EL1 in Secure state.

Configuration

There are no configuration notes.

Attributes

CNTPS_CVAL_EL1 is a 64-bit register.

Field descriptions

The CNTPS_CVAL_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

CompareValue, bits [63:0]

Holds the secure physical timer CompareValue.

When CNTPS_CTL_EL1.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTPS_CTL_EL1.ISTATUS is set to 1.
- If CNTPS_CTL_EL1.IMASK is 0, an interrupt is generated.

When CNTPS_CTL_EL1.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the CNTPS_CVAL_EL1

Accesses to this register use the following encodings:

MRS <Xt>, CNTPS_CVAL_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '0' then
        if SCR_EL3.EEL2 == '1' then
            UNDEFINED;
        elsif SCR_EL3.ST == '0' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return CNTPS_CVAL_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return CNTPS_CVAL_EL1;

MSR CNTPS_CVAL_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b111</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '0' then
        if SCR_EL3.EEL2 == '1' then
            UNDEFINED;
        elsif SCR_EL3.ST == '0' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            CNTPS_CVAL_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    CNTPS_CVAL_EL1 = X[t];

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The CNTPS_TVAL_EL1 characteristics are:

**Purpose**

Holds the timer value for the secure physical timer, usually accessible at EL3 but configurably accessible at EL1 in Secure state.

**Configuration**

There are no configuration notes.

**Attributes**

CNTPS_TVAL_EL1 is a 64-bit register.

**Field descriptions**

The CNTPS_TVAL_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31-0</td>
<td>TimerValue</td>
<td>The TimerValue view of the secure physical timer. On a read of this register:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If CNTPS_CTL_EL1.ENABLE is 0, the value returned is UNKNOWN.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If CNTPS_CTL_EL1.ENABLE is 1, the value returned is (CNTPS_CVAL_EL1 - CNTPCT_EL0). On a write of this register, CNTPS_CVAL_EL1 is set to (CNTPCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer: When CNTPS_CTL_EL1.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CNTPS_CVAL_EL1) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- CNTPS_CTL_EL1.ISTATUS is set to 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- If CNTPS_CTL_EL1.IMASK is 0, an interrupt is generated. When CNTPS_CTL_EL1.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count, so the TimerValue view appears to continue to count down. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**TimerValue, bits [31:0]**

The TimerValue view of the secure physical timer.
Accessing the CNTPS_TVAL_EL1

Accesses to this register use the following encodings:

MRS <Xt>, CNTPS_TVAL_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '0' then
        if SCR_EL3.EEL2 == '1' then
            UNDEFINED;
        elsif SCR_EL3.ST == '0' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return CNTPS_TVAL_EL1;
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        UNDEFINED;
    elsif PSTATE.EL == EL3 then
        return CNTPS_TVAL_EL1;

MSR CNTPS_TVAL_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && SCR_EL3.NS == '0' then
        if SCR_EL3.EEL2 == '1' then
            UNDEFINED;
        elsif SCR_EL3.ST == '0' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            CNTPS_TVAL_EL1 = X[t];
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        UNDEFINED;
    elsif PSTATE.EL == EL3 then
        CNTPS_TVAL_EL1 = X[t];
The CNTV_CTL_EL0 characteristics are:

**Purpose**

Control register for the virtual timer.

**Configuration**

AArch64 System register CNTV_CTL_EL0 bits [31:0] are architecturally mapped to AArch32 System register CNTV_CTL[31:0].

**Attributes**

CNTV_CTL_EL0 is a 64-bit register.

**Field descriptions**

The CNTV_CTL_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>ISTATUS, bit [2]</td>
<td>0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>61</td>
<td>ISTATUS, bit [2]</td>
<td>1</td>
<td>Timer condition is met.</td>
</tr>
<tr>
<td>60</td>
<td>IMASK, bit [1]</td>
<td>0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>59</td>
<td>IMASK, bit [1]</td>
<td>1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE (bit 0)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from `CNTV_TVAL_EL0` continues to count down.

---

**Note**

Disabling the output signal might be a power-saving option.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTV_CTL_EL0**

When `HCR_EL2.E2H` is 1, without explicit synchronization, access from EL3 using the mnemonic `CNTV_CTL_EL0` or `CNTV_CTL_EL02` are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```
MRS <Xt>, CNTV_CTL_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

`CNTV_CTL_EL0`, Counter-timer Virtual Timer Control register
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
  IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_CTL_EL2;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    return CNTHV_CTL_EL2;
  else
    return CNTV_CTL_EL0;
endif

elsif PSTATE.EL == EL1 then
  if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x170];
  else
    return CNTV_CTL_EL0;
endif

elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    return CNTHVS_CTL_EL2;
  elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    return CNTHV_CTL_EL2;
  else
    return CNTV_CTL_EL0;
endif

elsif PSTATE.EL == EL3 then
  return CNTV_CTL_EL0;
endif

MSR CNTV_CTL_EL0, <Xt>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS_CTL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        CNTHV_CTL_EL2 = X[t];
    else
        CNTV_CTL_EL0 = X[t];
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x170] = X[t];
    else
        CNTV_CTL_EL0 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS_CTL_EL2 = X[t];
    elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
        CNTHV_CTL_EL2 = X[t];
    else
        CNTV_CTL_EL0 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    CNTV_CTL_EL0 = X[t];
MRS <Xt>, CNTV_CTL_EL02

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return NVMem[0x170];
        end if
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return CNTV_CTL_EL0;
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return CNTV_CTL_EL0;
    else
        UNDEFINED;
    end if
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1NVVCT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            NVMem[0x170] = X[t];
        end if
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end if
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CNTV_CTL_EL0 = X[t];
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        CNTV_CTL_EL0 = X[t];
    else
        UNDEFINED;
    end if
The CNTV_CVAL_EL0 characteristics are:

**Purpose**

Holds the compare value for the virtual timer.

**Configuration**

AArch64 System register CNTV_CVAL_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTV_CVAL[63:0].

**Attributes**

CNTV_CVAL_EL0 is a 64-bit register.

**Field descriptions**

The CNTV_CVAL_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**CompareValue, bits [63:0]**

Holds the EL1 virtual timer CompareValue.

When CNTV_CTL_EL0.ENABLE is 1, the timer condition is met when (CNTVCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTV_CTL_EL0.ISTATUS is set to 1.
- If CNTV_CTL_EL0.IMASK is 0, an interrupt is generated.

When CNTV_CTL_EL0.ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTV_CVAL_EL0**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic CNTV_CVAL_EL0 or CNTV_CVAL_EL02 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```assembly
MRS <Xt>, CNTV_CVAL_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
        IsFeatureImplemented(FEAT_SEL2) then
        return CNTHVS_CVAL_EL2;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHV_CVAL_EL2;
    else
        return CNTV_CVAL_EL0;
    end
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && CNTHCTL_EL2.EL1VT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
            return NVMem[0x168];
        else
            return CNTV_CVAL_EL0;
        end
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHVS_CVAL_EL2;
        elsif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
            return CNTHV_CVAL_EL2;
        else
            return CNTV_CVAL_EL0;
        end
    elsif PSTATE.EL == EL3 then
        return CNTV_CVAL_EL0;
    end
end

MSR CNTV_CVAL_EL0, <Xt>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTHVS_CVAL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
else
  CNTV_CVAL_EL0 = X[t];
endif

if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL1TVT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      CNTHVS_CVAL_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
endif

if PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTHV_CVAL_EL2 = X[t];
  elseif HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHV_CVAL_EL2 = X[t];
  else
    CNTV_CVAL_EL0 = X[t];
  endif
endif

if PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return CNTV_CVAL_EL0;
  else
    UNDEFINED;
  endif
endif

MRS <Xt>, CNTV_CVAL_EL02

<table>
<thead>
<tr>
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</thead>
<tbody>
<tr>
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<td>0b101</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1NVVCT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
      elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' then
          return NVMem[0x168];
        elseif EL2Enabled() && HCR_EL2.NV == '1' then
          AArch64.SystemAccessTrap(EL2, 0x18);
        else
          UNDEFINED;
        endif
      else
        UNDEFINED;
      endif
  else
    return CNTV_CVAL_EL0;
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return CNTV_CVAL_EL0;
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return CNTV_CVAL_EL0;
  else
    UNDEFINED;
  endif
endif
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1NVVCT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      NVMem[0x168] = X[t];
    end if
  end if
elsif EL2Enabled() && HCR_EL2.NV == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    CNTV_CVAL_EL0 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    CNTV_CVAL_EL0 = X[t];
  else
    UNDEFINED;
else
  UNDEFINED;
The CNTV_TVAL_EL0 characteristics are:

**Purpose**

Holds the timer value for the EL1 virtual timer.

**Configuration**

AArch64 System register CNTV_TVAL_EL0 bits [31:0] are architecturally mapped to AArch32 System register CNTV_TVAL[31:0].

**Attributes**

CNTV_TVAL_EL0 is a 64-bit register.

**Field descriptions**

The CNTV_TVAL_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0                     | TimerValue               |

**Bits [33:32]**

Reserved, RES0.

**TimerValue, bits [31:0]**

The TimerValue view of the EL1 virtual timer.

On a read of this register:

- If CNTV_CTL_EL0.ENABLE is 0, the value returned is UNKNOWN.
- If CNTV_CTL_EL0.ENABLE is 1, the value returned is (CNTV_CVAL_EL0 - CNTVCT_EL0).

On a write of this register, CNTV_CVAL_EL0 is set to (CNTVCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer:

When CNTV_CTL_EL0 ENABLE is 1, the timer condition is met when (CNTVCT_EL0 - CNTV_CVAL_EL0) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTV_CTL_EL0.ISTATUS is set to 1.
- If CNTV_CTL_EL0.IMASK is 0, an interrupt is generated.

When CNTV_CTL_EL0.ENABLE is 0, the timer condition is not met, but CNTVCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the CNTV_TVAL_EL0

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic CNTV_TVAL_EL0 or CNTV_TVAL_EL02 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CNTV_TVAL_EL0

<table>
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<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
          AArch64.SystemAccessTrap(EL2, 0x18);
        else
          if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' &&
            IsFeatureImplemented(FEAT_SEL2) then
            return CNTHVS_TVAL_EL2;
          elf EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            return CNTHV_TVAL_EL2;
          else
            return CNTV_TVAL_EL0;
          elsif PSTATE.EL == EL1 then
            if EL2Enabled() && CNTHCTL_EL2.EL1TVT == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            else
              return CNTV_TVAL_EL0;
            elsif PSTATE.EL == EL2 then
              if HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' &&
                IsFeatureImplemented(FEAT_SEL2) then
                return CNTHVS_TVAL_EL2;
              else
                return CNTHV_TVAL_EL2;
              elsif PSTATE.EL == EL3 then
                return CNTV_TVAL_EL0;
              else
                return CNTV_TVAL_EL0;
          elsif PSTATE.EL == EL0 then
            return CNTV_TVAL_EL0;

MSR CNTV_TVAL_EL0, <Xt>

<table>
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<td>0b1110</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') & CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() & HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & CNTHCTL_EL2.E2H == '1' & IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS_TVAL_EL2 = X[t];
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '0' &
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & CNTHCTL_EL2.EL1 TVT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '1' then
        CNTHV_TVAL_EL2 = X[t];
    else
        CNTV_TVAL_EL0 = X[t];
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() & HCR_EL2.E2H == '1' & CNTHCTL_EL2.EL1 TVT == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            CNTV_TVAL_EL0 = X[t];
        endif
else
    if PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' & SCR_EL3.NS == '0' & IsFeatureImplemented(FEAT_SEL2) then
            CNTHVS_TVAL_EL2 = X[t];
        elsif HCR_EL2.E2H == '1' & SCR_EL3.NS == '1' then
            CNTHV_TVAL_EL2 = X[t];
        else
            CNTV_TVAL_EL0 = X[t];
        endif
else
    if PSTATE.EL == EL3 then
        if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            CNTV_TVAL_EL0 = X[t];
        endif
    endif
if PSTATE.EL == EL0 then
    if EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() & HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & CNTHCTL_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '0' &
    elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCR_EL3.NS == '1' then
        CNTHV_TVAL_EL2 = X[t];
    else
        CNTV_TVAL_EL0 = X[t];
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() & SCR_EL3.NS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL3 then
        if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
    endif
if PSTATE.EL == EL0 then
    UNDEFINED;
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() & HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL3 then
        if EL2Enabled() & ELUsingAArch32(EL2) & HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
    endif
MSR CNTV_TVAL_EL02, <Xt>

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<tr>
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<td>0b1110</td>
<td>0b0011</td>
<td>0b0000</td>
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</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() & HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
        endif
else
    if PSTATE.EL == EL3 then
        if EL2Enabled() & ELUsingAArch32(EL2) & HCR_EL2.E2H == '1' then
            return CNTV_TVAL_EL0;
        else
            UNDEFINED;
    endif
MSR CNTV_TVAL_EL02, <Xt>

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</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    CNTV_TVAL_EL0 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    CNTV_TVAL_EL0 = X[t];
  else
    UNDEFINED;
CNTVCT_EL0, Counter-timer Virtual Count register

The CNTVCT_EL0 characteristics are:

**Purpose**

Holds the 64-bit virtual count value. The virtual count value is equal to the physical count value minus the virtual offset visible in CNTVOFF_EL2.

**Configuration**

AArch64 System register CNTVCT_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTVCT[63:0].

The value of this register is the same as the value of CNTPCT_EL0 in the following conditions:

- When EL2 is not implemented.
- When EL2 is implemented, HCR_EL2.E2H is 1, and this register is read from EL2.
- When EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H, TGE} is {1, 1}, and this register is read from EL0 or EL2.

All reads to the CNTVCT_EL0 occur in program order relative to reads to CNTVCTSS_EL0 or CNTVCT_EL0.

**Attributes**

CNTVCT_EL0 is a 64-bit register.

**Field descriptions**

The CNTVCT_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Virtual count value</td>
</tr>
<tr>
<td>62</td>
<td>Virtual count value</td>
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<tr>
<td>61</td>
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<td>35</td>
<td>Virtual count value</td>
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<td>34</td>
<td>Virtual count value</td>
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<tr>
<td>33</td>
<td>Virtual count value</td>
</tr>
<tr>
<td>32</td>
<td>Virtual count value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual count value.

**Accessing the CNTVCT_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, CNTVCT_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VCTEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVCT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTVCT_EL0;
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVCT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTVCT_EL0;
    end
elsif PSTATE.EL == EL2 then
    return CNTVCT_EL0;
elsif PSTATE.EL == EL3 then
    return CNTVCT_EL0;
else
    return CNTVCT_EL0;
end
The CNTVCTSS_EL0 characteristics are:

**Purpose**

Holds the 64-bit virtual count value. The virtual count value is equal to the physical count value visible in CNTPCT_EL0 minus the virtual offset visible in CNTVOFF_EL2.

**Configuration**

AArch64 System register CNTVCTSS_EL0 bits [63:0] are architecturally mapped to AArch32 System register CNTVCTSS[63:0].

This register is present only when FEAT_ECV is implemented. Otherwise, direct accesses to CNTVCTSS_EL0 are UNDEFINED.

All reads to the CNTVCTSS_EL0 occur in program order relative to reads to CNTPCT_EL0 or CNTVCTSS_EL0.

This register is a self-synchronised view of the CNTPCT_EL0 counter, and cannot be read speculatively.

**Attributes**

CNTVCTSS_EL0 is a 64-bit register.

**Field descriptions**

The CNTVCTSS_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Self-synchronized virtual count value</td>
</tr>
<tr>
<td>31</td>
<td>Self-synchronized virtual count value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Self-synchronized virtual count value.

**Accessing the CNTVCTSS_EL0**

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{CNTVCTSS} \ \text{EL0}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VCTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVCT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTVCTSS_EL0;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && CNTHCTL_EL2.EL1TVCT == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CNTVCTSS_EL0;
elsif PSTATE.EL == EL2 then
    return CNTVCTSS_EL0;
else if PSTATE.EL == EL3 then
    return CNTVCTSS_EL0;
CNTVOFF_EL2, Counter-timer Virtual Offset register

The CNTVOFF_EL2 characteristics are:

**Purpose**

Holds the 64-bit virtual offset. This is the offset between the physical count value visible in CNTPCT_EL0 and the virtual count value visible in CNTVCT_EL0.

**Configuration**

AArch64 System register CNTVOFF_EL2 bits [63:0] are architecturally mapped to AArch32 System register CNTVOFF[63:0].

If EL2 is not implemented, this register is RES0 from EL3 and the virtual counter uses a fixed virtual offset of zero.

**Note**

When EL2 is implemented and enabled in the current Security state, and is using AArch64, the virtual counter uses a fixed virtual offset of zero in the following situations:

- HCR_EL2.E2H is 1, and CNTVCT_EL0 is read from EL2.
- HCR_EL2.{E2H, TGE} is {1, 1}, and either:
  - CNTVCT_EL0 is read from EL0 or EL2.
  - CNTVCT is read from EL0.

**Attributes**

CNTVOFF_EL2 is a 64-bit register.

**Field descriptions**

The CNTVOFF_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Virtual offset</td>
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<tr>
<td>62</td>
<td>Virtual offset</td>
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<td>61</td>
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<tr>
<td>2</td>
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<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
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</tbody>
</table>

**Bits [63:0]**

Virtual offset.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTVOFF_EL2**

Accesses to this register use the following encodings:
MRS <Xt>, CNTVOFF_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x060];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    return CNTVOFF_EL2;
elsif PSTATE.EL == EL3 then
    return CNTVOFF_EL2;
endif

MSR CNTVOFF_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x060] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    CNTVOFF_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CNTVOFF_EL2 = X[t];
endif
CONTEXTIDR_EL1, Context ID Register (EL1)

The CONTEXTIDR_EL1 characteristics are:

**Purpose**

Identifies the current Process Identifier.

The value of the whole of this register is called the Context ID and is used by:

- The debug logic, for Linked and Unlinked Context ID matching.
- The trace logic, to identify the current process.

The significance of this register is for debug and trace use only.

**Configuration**

AArch64 System register CONTEXTIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register CONTEXTIDR[31:0].

**Attributes**

CONTEXTIDR_EL1 is a 64-bit register.

**Field descriptions**

The CONTEXTIDR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | PROCID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**PROCID, bits [31:0]**

Process Identifier. This field must be programmed with a unique value that identifies the current process.

**Note**

In AArch32 state, when TTBCR.EAE is set to 0, CONTEXTIDR. ASID holds the ASID.

In AArch64 state, CONTEXTIDR_EL1 is independent of the ASID, and for the EL1&0 translation regime either TTBR0_EL1 or TTBR1_EL1 holds the ASID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CONTEXTIDR_EL1**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic CONTEXTIDR_EL1 or CONTEXTIDR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CONTEXTIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x108];
    else
        return CONTEXTIDR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return CONTEXTIDR_EL2;
    else
        return CONTEXTIDR_EL1;
    end
elsif PSTATE.EL == EL3 then
    return CONTEXTIDR_EL1;
fi

MSR CONTEXTIDR_EL1, <Xt>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CONTEXTIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x108] = X[t];
    else
        CONTEXTIDR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CONTEXTIDR_EL2 = X[t];
    else
        CONTEXTIDR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    CONTEXTIDR_EL1 = X[t];
fi

MRS <Xt>, CONTEXTIDR_EL12

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CONTEXTIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x108];
    else
        CONTEXTIDR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CONTEXTIDR_EL2 = X[t];
    else
        CONTEXTIDR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    CONTEXTIDR_EL1 = X[t];
fi
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x108];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return CONTEXTIDR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return CONTEXTIDR_EL1;
  else
    UNDEFINED;

MSR CONTEXTIDR_EL12, <Xt>
The CONTEXTIDR_EL2 characteristics are:

**Purpose**

Identifies the current Process Identifier for EL2.

The value of the whole of this register is called the Context ID and is used by:

- The debug logic, for Linked and Unlinked Context ID matching.
- The trace logic, to identify the current process.

The significance of this register is for debug and trace use only.

**Configuration**

This register is present only when FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented. Otherwise, direct accesses to CONTEXTIDR_EL2 are *undefined*.

If EL2 is not implemented, this register is *res0* from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

CONTEXTIDR_EL2 is a 64-bit register.

**Field descriptions**

The CONTEXTIDR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>31</td>
<td>PROCID</td>
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<td>30</td>
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<tr>
<td>19</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
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<tr>
<td>14</td>
<td></td>
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<tr>
<td>13</td>
<td></td>
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<tr>
<td>12</td>
<td></td>
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<tr>
<td>11</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
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<tr>
<td>9</td>
<td></td>
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<tr>
<td>8</td>
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<td>7</td>
<td></td>
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<td>6</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
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<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, *res0*.

**PROCID, bits [31:0]**

Process Identifier. This field must be programmed with a unique value that identifies the current process.

On a Warm reset, this field resets to an architecturally *unknown* value.

**Accessing the CONTEXTIDR_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic CONTEXTIDR_EL2 or CONTEXTIDR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, CONTEXTIDR_EL2
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CONTEXTIDR_EL2;
elsif PSTATE.EL == EL3 then
    return CONTEXTIDR_EL2;

MSR CONTEXTIDR_EL2, <xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CONTEXTIDR_EL1 == '1' then
        return NVMem[0x108];
    else
        return CONTEXTIDR_EL1;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return CONTEXTIDR_EL2;
    else
        return CONTEXTIDR_EL1;
elsif PSTATE.EL == EL3 then
    return CONTEXTIDR_EL1;

MRS <xt>, CONTEXTIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TRVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CONTEXTIDR_EL1 == '1' then
        return CONTEXTIDR_EL1;
    else
        return CONTEXTIDR_EL1;
elsif PSTATE.EL == EL2 then
    CONTEXTIDR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CONTEXTIDR_EL2 = X[t];

MSR CONTEXTIDR_EL1, <xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CONTEXTIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x108] = X[t];
    else
        CONTEXTIDR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        CONTEXTIDR_EL2 = X[t];
    else
        CONTEXTIDR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    CONTEXTIDR_EL1 = X[t];
else
The CPACR_EL1 characteristics are:

**Purpose**

Controls access to trace, SVE, Advanced SIMD and floating-point functionality.

**Configuration**

AArch64 System register CPACR_EL1 bits [31:0] are architecturally mapped to AArch32 System register CPACR[31:0].

When HCR_EL2.{E2H, TGE} == {1, 1}, the fields in this register have no effect on execution at EL0 and EL1. In this case, the controls provided by CPTR_EL2 are used.

**Attributes**

CPACR_EL1 is a 64-bit register.

**Field descriptions**

The CPACR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-29</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>28</td>
<td>TTA</td>
<td>Traps EL0 and EL1 System register accesses to all implemented trace registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.{E2H, TGE} is {0,1}, from both Execution states as follows:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In AArch64 state, accesses to trace registers are trapped, reported using ESR_ELx.EC value 0x18.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In AArch32 state, MRC and MCR accesses to trace registers are trapped, reported using ESR_ELx.EC value 0x85.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In AArch32 state, MRRC and MCRR accesses to trace registers are trapped, reported using ESR_ELx.EC value 0x0C.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control causes EL0 and EL1 System register accesses to all implemented trace registers to be trapped.</td>
</tr>
</tbody>
</table>

**Note**

- The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are **UNDEFINED**, and any resulting exception is higher
priority than an exception that would be generated because the value of \texttt{CPACR\_EL1.\_TTA} is 1.

- The Armv8-A architecture does not provide traps on trace register accesses through the optional memory-mapped interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

If System register access to the trace functionality is not implemented, this bit is \texttt{RES0}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Bits [27:22]**

Reserved, \texttt{RES0}.

**FPEN, bits [21:20]**

Traps EL0 and EL1 accesses to SVE, Advanced SIMD and floating-point registers to EL1, reported using ESR\_ELx.EC value 0x07, or to EL2 reported using ESR\_ELx.EC value 0x00, when EL2 is implemented and enabled for the current Security state and \texttt{HCR\_EL2.\{E2H, TGE\}} is \{0,1\}, from both Execution states as follows:

- In AArch64 state, accesses to \texttt{FPCR}, \texttt{FPSCR}, any of the SIMD and floating-point registers V0-V31, including their views as D0-D31 registers or S0-31 registers.
- In AArch32 state, \texttt{FPSCR}, and any of the SIMD and floating-point registers Q0-15, including their views as D0-D31 registers or S0-31 registers.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPACR\_EL1.ZEN has precedence over the value of CPACR\_EL1.FPEN.

<table>
<thead>
<tr>
<th>FPEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>This control causes any instructions at EL0 or EL1 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped.</td>
</tr>
<tr>
<td>0b01</td>
<td>This control causes any instructions at EL0 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped, but does not cause any instruction at EL1 to be trapped.</td>
</tr>
<tr>
<td>0b10</td>
<td>This control causes any instructions at EL0 or EL1 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped.</td>
</tr>
<tr>
<td>0b11</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

Writes to \texttt{MVFR0, MVFR1} and \texttt{MVFR2} from EL1 or higher are \texttt{CONSTRAINED\_UNPREDICTABLE} and whether these accesses can be trapped by this control depends on implemented \texttt{CONSTRAINED\_UNPREDICTABLE} behavior.

**Note**

- Attempts to write to the FPSID count as use of the registers for accesses from EL1 or higher.
- Accesses from EL0 to \texttt{FPSID, MVFR0, MVFR1, MVFR2, and FPEXC} are \texttt{UNDEFINED}, and any resulting exception is higher priority than an exception that would be generated because the value of CPACR\_EL1.FPEN is not 0b11.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Bits [19:18]**

Reserved, \texttt{RES0}. 

---

\texttt{CPACR\_EL1, Architectural Feature Access Control Register}
**ZEN, bits [17:16]**

When `FEAT_SVE` is implemented:

Traps EL0 and EL1 execution of SVE instructions and instructions that directly access `ZCR_EL1` System register to EL1, or to EL2 when EL2 is implemented and enabled for the current Security state and `HCR_EL2` (E2H, TGE) is \{0,1\}.

The exception is reported using `ESR_ELx.EC` value 0x19.

Trapping behavior is affected by precedence as follows: A trap taken as a result of `CPACR_EL1.ZEN` has precedence over the value of `CPACR_EL1.FPEN`.

<table>
<thead>
<tr>
<th>ZEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>This control causes these instructions executed at EL0 or EL1 to be trapped.</td>
</tr>
<tr>
<td>0b01</td>
<td>This control causes these instructions executed at EL0 to be trapped, but does not cause any instruction at EL1 to be trapped.</td>
</tr>
<tr>
<td>0b10</td>
<td>This control causes these instructions executed at EL0 or EL1 to be trapped.</td>
</tr>
<tr>
<td>0b11</td>
<td>This control does not cause any instruction to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, `RES0`.

**Bits [15:0]**

Reserved, `RES0`.

**Accessing the CPACR_EL1**

When `HCR_EL2.E2H` is 1, without explicit synchronization, access from EL3 using the mnemonic `CPACR_EL1` or `CPACR_EL12` are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```
MRS <Xt>, CPACR_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b001</td>
<td>0b000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TCPAC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CPACR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x100];
  else
    return CPACR_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HCR_EL2.E2H == '1' then
    return CPTR_EL2;
  else
    return CPACR_EL1;
  endif
elsif PSTATE.EL == EL3 then
  return CPACR_EL1;
endif

MSR CPACR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
        UNDEFINED;
elseself EL2Enabled() && CPTR_EL2.TCPAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elseself EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CPACR_EL1 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
elseself HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
elseself EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
                NVMem[0x100] = X[t];
elseself HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
elseself HCR_EL2.E2H == '1' then
                CPTR_EL2 = X[t];
elseself PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
        UNDEFINED;
elseself HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
elseself CPACR_EL1 = X[t];
elseself PSTATE.EL == EL3 then
    CPACR_EL1 = X[t];

MRS <Xt>, CPACR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CMn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x100];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() & & HaveEL(EL3) & & EDSCR.SDD == '1' & & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & & CPTR_EL3.TCPAC == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) & & CPTR_EL3.TCPAC == '1' then
            if Halted() & & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            return CPACR_EL1;
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.E2H == '1' then
        return CPACR_EL1;
    else
        UNDEFINED;
else
    UNDEFINED;

MSR CPACR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & & HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x100] = X[t];
    elsif EL2Enabled() & & HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() & & HaveEL(EL3) & & EDSCR.SDD == '1' & & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & & CPTR_EL3.TCPAC == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) & & CPTR_EL3.TCPAC == '1' then
            if Halted() & & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            CPACR_EL1 = X[t];
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.E2H == '1' then
        CPACR_EL1 = X[t];
    else
        UNDEFINED;
The CPP RCTX characteristics are:

**Purpose**

Cache Prefetch Prediction Restriction by Context applies to all Cache Allocation Resources that predict cache allocations based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, cache prefetch prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction applies to all:

- Instruction caches.
- Data caches.
- TLB prefetching hardware used by the executing PE that applies to the supplied context or contexts.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of Cache Allocation Resources so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when FEAT_SPECRES is implemented. Otherwise, direct accesses to CPP RCTX are UNDEFINED.

**Attributes**

CPP RCTX is a 64-bit System instruction.

**Field descriptions**

The CPP RCTX input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:49]</td>
<td>RES0</td>
<td>GVMID</td>
</tr>
<tr>
<td>[31:0]</td>
<td>RES0</td>
<td>NS</td>
</tr>
</tbody>
</table>

**Bits [63:49]**

Reserved, RES0.
**GVMID, bit [48]**

Execution of this instruction applies to all VMIDs or a specified VMID.

<table>
<thead>
<tr>
<th>GVMID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified VMID for an EL0 or EL1 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all VMIDs for an EL0 or EL1 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0 and EL1, this field is RES0.

If the instruction is executed at EL0 or EL1, this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**VMID, bits [47:32]**

Only applies when bit[48] is 0 and the target execution context is either:

- EL1.
- EL0 when \((HCR\_EL2.E2H==0 \text{ or } HCR\_EL2.TGE==0)\).

Otherwise this field is RES0.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and \((HCR\_EL2.E2H==0 \text{ or } HCR\_EL2.TGE==0)\), this field is treated as the current VMID.

When the instruction is executed at EL0 and \((HCR\_EL2.E2H==1 \text{ and } HCR\_EL2.TGE==1)\), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**Bits [31:27]**

Reserved, RES0.

**NS, bit [26]**

Security State. Defined values are:

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure state.</td>
</tr>
</tbody>
</table>

When executed in Non-secure state, the Effective value of NS is 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>EL0.</td>
</tr>
<tr>
<td>0b01</td>
<td>EL1.</td>
</tr>
<tr>
<td>0b10</td>
<td>EL2.</td>
</tr>
<tr>
<td>0b11</td>
<td>EL3.</td>
</tr>
</tbody>
</table>

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**Bits [23:17]**

Reserved, RES0.
GASID, bit [16]

Execution of this instruction applies to all ASIDs or a specified ASID.

<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0, this field is RES0.

If the instruction is executed at EL0, this field has an Effective value of 0.

ASID, bits [15:0]

Only applies for an EL0 target execution context and when bit[16] is 0.

Otherwise, this field is RES0.

When the instruction is executed at EL0, this field is treated as the current ASID.

Executing the CPP RCTX instruction

Accesses to this instruction use the following encodings:

CPP RCTX, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.EnRCTX == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.CPPRCTX == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.EnRCTX == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        CPP_RCTX(X[t]);
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.CPPRCTX == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        CPP_RCTX(X[t]);
    end
elsif PSTATE.EL == EL2 then
    CPP_RCTX(X[t]);
elsif PSTATE.EL == EL3 then
    CPP_RCTX(X[t]);
```

30/09/2020 15:07; cceed0cb9f089f9ceec50268e82aec9e71047211

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CPTR_EL2, Architectural Feature Trap Register (EL2)

The CPTR_EL2 characteristics are:

**Purpose**

Controls trapping to EL2 of accesses to CPACR, CPACR_EL1, trace, Activity Monitor, SVE, Advanced SIMD and floating-point functionality.

**Configuration**

AArch64 System register CPTR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HCPTR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

CPTR_EL2 is a 64-bit register.

**Field descriptions**

The CPTR_EL2 bit assignments are:

**When FEAT_VHE is implemented and HCR_EL2.E2H == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>TCPAC</td>
</tr>
<tr>
<td>31</td>
<td>TCPAC</td>
</tr>
<tr>
<td>30</td>
<td>TAM</td>
</tr>
<tr>
<td>29</td>
<td>RESO</td>
</tr>
<tr>
<td>28</td>
<td>TTA</td>
</tr>
<tr>
<td>27</td>
<td>RESO</td>
</tr>
<tr>
<td>26</td>
<td>RESO</td>
</tr>
<tr>
<td>25</td>
<td>FPEN</td>
</tr>
<tr>
<td>24</td>
<td>RESO</td>
</tr>
<tr>
<td>23</td>
<td>ZEN</td>
</tr>
<tr>
<td>22</td>
<td>RESO</td>
</tr>
<tr>
<td>21</td>
<td>RESO</td>
</tr>
<tr>
<td>20</td>
<td>RESO</td>
</tr>
<tr>
<td>19</td>
<td>RESO</td>
</tr>
<tr>
<td>18</td>
<td>RESO</td>
</tr>
<tr>
<td>17</td>
<td>RESO</td>
</tr>
<tr>
<td>16</td>
<td>RESO</td>
</tr>
<tr>
<td>15</td>
<td>RESO</td>
</tr>
<tr>
<td>14</td>
<td>RESO</td>
</tr>
<tr>
<td>13</td>
<td>RESO</td>
</tr>
<tr>
<td>12</td>
<td>RESO</td>
</tr>
<tr>
<td>11</td>
<td>RESO</td>
</tr>
<tr>
<td>10</td>
<td>RESO</td>
</tr>
<tr>
<td>9</td>
<td>RESO</td>
</tr>
<tr>
<td>8</td>
<td>RESO</td>
</tr>
<tr>
<td>7</td>
<td>RESO</td>
</tr>
<tr>
<td>6</td>
<td>RESO</td>
</tr>
<tr>
<td>5</td>
<td>RESO</td>
</tr>
<tr>
<td>4</td>
<td>RESO</td>
</tr>
<tr>
<td>3</td>
<td>RESO</td>
</tr>
<tr>
<td>2</td>
<td>RESO</td>
</tr>
<tr>
<td>1</td>
<td>RESO</td>
</tr>
<tr>
<td>0</td>
<td>RESO</td>
</tr>
</tbody>
</table>

Bits [63:32]

Reserved, RES0.

**TCPAC, bit [31]**

When HCR_EL2.TGE is 0, traps EL1 accesses to CPACR_EL1 reported using ESR_ELx.EC value 0x18, and accesses to CPACR reported using ESR_ELx.EC value 0x03, to EL2 when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>TCPAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to CPACR_EL1 and CPACR are trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, this control does not cause any instructions to be trapped.

**Note**

CPACR_EL1 and CPACR are not accessible at EL0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
TAM, bit [30]

When FEAT_AMUv1 is implemented:

Trap Activity Monitor access. Traps EL1 and EL0 accesses to all Activity Monitor registers to EL2, as follows:

- In AArch64 state, accesses to the following registers are trapped to EL2, reported using ESR_ELx.EC value 0x18:
  - $\text{AMUSERENR}_{EL0}$, $\text{AMCFGR}_{EL0}$, $\text{AMCGCR}_{EL0}$, $\text{AMCNTENCLR0}_{EL0}$, $\text{AMCNTENCLR1}_{EL0}$, $\text{AMCNTENSET0}_{EL0}$, $\text{AMCNTENSET1}_{EL0}$, $\text{AMCR}_{EL0}$, $\text{AMEVCNTR0}_{n}\_EL0$, $\text{AMEVTYPER0}_{n}\_EL0$, and $\text{AMEVTYPER1}_{n}\_EL0$.

- In AArch32 state, MRC or MCR accesses to the following registers are trapped to EL2 and reported using ESR_ELx.EC value 0x03:
  - $\text{AMUSERENR}$, $\text{AMCFGR}$, $\text{AMCGCR}$, $\text{AMCNTENCLR0}$, $\text{AMCNTENCLR1}$, $\text{AMCNTENSET0}$, $\text{AMCNTENSET1}$, $\text{AMCR}$, $\text{AMEVTYPER0}_{n}$, and $\text{AMEVTYPER1}_{n}$.

- In AArch32 state, MRRC or MCRR accesses to $\text{AMEVCNTR0}_{n}$ and $\text{AMEVCNTR1}_{n}$, are trapped to EL2, reported using ESR_ELx.EC value 0x04.

<table>
<thead>
<tr>
<th>TAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses from EL1 and EL0 to Activity Monitor registers are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses from EL1 and EL0 to Activity Monitor registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [29]

Reserved, RES0.

TTA, bit [28]

Traps System register accesses to all implemented trace registers to EL2 when EL2 is enabled in the current Security state, from both Execution states as follows:

- In AArch64 state, accesses to trace registers with op0=2, op1=1, and CRn<0b1000 are trapped to EL2, reported using EC syndrome value 0x18.

- In AArch32 state, MRC or MCR accesses to trace registers with cpnum=14, opc1=1, and CRn<0b1000 are trapped to EL2, reported using EC syndrome value 0x05.

<table>
<thead>
<tr>
<th>TTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt at EL0, EL1 or EL2, to execute a System register access to an implemented trace register is trapped to EL2 when EL2 is enabled in the current Security state, unless $\text{HCR}<em>{EL2}.\text{TGE}$ is 0 and it is trapped by $\text{CPACR}.\text{NSTRCDIS}$ or $\text{CPACR}</em>{EL1}.\text{TTA}$. When $\text{HCR}_{EL2}.\text{TGE}$ is 1, any attempt at EL0 or EL2 to execute a System register access to an implemented trace register is trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

**Note**

The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 access to the trace registers are UNDEFINED, and any resulting exception is higher priority than this trap exception that would be generated because the value of CPTR_EL2.TTA is 1.
EL2 does not provide traps on trace register accesses through the optional Memory-mapped interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

If System register access to the trace functionality is not supported, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [27:22]**

Reserved, RES0.

**FPEN, bits [21:20]**

Traps execution at EL2, EL1, and EL0 of instructions that directly access the SVE, Advanced SIMD and floating-point registers to EL2 when EL2 is enabled in the current Security state, from both Execution states.

The exception is reported using ESR_ELx.EC value 0x07.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPTR_EL2.ZEN has precedence over the value of CPTR_EL2.FPEN.

<table>
<thead>
<tr>
<th>FPEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>This control causes any instructions at EL0, EL1, or EL2 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped, subject to the exception prioritization rules.</td>
</tr>
<tr>
<td>0b01</td>
<td>When HCR_EL2.TGE is 0, this control does not cause any instructions to be trapped. When HCR_EL2.TGE is 1, this control causes instructions at EL0 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped, but does not cause any instruction at EL2 to be trapped.</td>
</tr>
<tr>
<td>0b10</td>
<td>This control causes any instructions at EL0, EL1, or EL2 that use the registers associated with SVE, Advanced SIMD and floating-point execution to be trapped, subject to the exception prioritization rules.</td>
</tr>
<tr>
<td>0b11</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

Writes to MVFR0, MVFR1, and MVFR2 from EL1 or higher are CONSTRAINED UNPREDICTABLE and whether these accesses can be trapped by this control depends on implemented CONSTRAINED UNPREDICTABLE behavior.

**Note**

- Attempts to write to the FPSID count as use of the registers for accesses from EL1 or higher.
- Accesses from EL0 to FPSID, MVFR0, MVFR1, MVFR2, and FPEXC are UNDEFINED, and any resulting exception is higher priority than an exception that would be generated because the value of CPTR_EL2.FPEN is not 0b11.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:18]**

Reserved, RES0.

**ZEN, bits [17:16]**

When FEAT_SVE is implemented:

Traps execution at EL2, EL1, and EL0 of SVE instructions, and instructions that directly access the ZCR_EL1 and ZCR_EL2 System registers to EL2 when EL2 is enabled in the current Security state.
The exception is reported using ESR_ELx.EC value 0x19.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPTR_EL2.ZEN has precedence over the value of CPTR_EL2.FPEN.

<table>
<thead>
<tr>
<th>ZEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>This control causes execution at EL2, EL1, and EL0 of these instructions to be trapped, subject to the exception prioritization rules.</td>
</tr>
<tr>
<td>0b01</td>
<td>When HCR_EL2.TGE is 0, this control does not cause any instruction to be trapped. When HCR_EL2.TGE is 1, this control causes these instructions executed at EL0 to be trapped, but does not cause any instruction at EL2 to be trapped.</td>
</tr>
<tr>
<td>0b10</td>
<td>This control causes execution at EL2, EL1, and EL0 of these instructions to be trapped, subject to the exception prioritization rules.</td>
</tr>
<tr>
<td>0b11</td>
<td>This control does not cause any instruction to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [15:0]

Reserved, RES0.

Otherwise:

| Bit 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TCPAC  | TAM | RES0 | ITA | RES0 | RES1 | RES0 | TFP | RES0 | TZ | RES1 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

This format applies in all Armv8.0 implementations.

Bits [63:32]

Reserved, RES0.

TCPAC, bit [31]

Traps EL1 accesses to CPACR_EL1, reported using ESR_ELx.EC value 0x18 and accesses to CPACR, reported using ESR_ELx.EC value 0x03, to EL2 when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>TCPAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to CPACR_EL1 and CPACR are trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, this control does not cause any instructions to be trapped.

Note

CPACR_EL1 and CPACR are not accessible at EL0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
When FEAT_AMUv1 is implemented:

Trap Activity Monitor access. Traps EL1 and EL0 accesses to all Activity Monitor registers to EL2, as follows:

- In AArch64 state, accesses to the following registers are trapped to EL2, reported using ESR_ELx.EC value 0x18:
  - AMUSERENR_EL0, AMCFGR_EL0, AMCGCR_EL0, AMCNTENCLR0_EL0, AMCNTENCLR1_EL0, AMCNTENSET0_EL0, AMCNTENSET1_EL0, AMCR_EL0, AMEVCNTR0<n>_EL0, AMEVTYPER0<n>_EL0, and AMEVTYPER1<n>_EL0.

- In AArch32 state, MCR or MRC accesses to the following registers are trapped to EL2 and reported using ESR_ELx.EC value 0x03:
  - AMUSERENR, AMCFGR, AMCGCR, AMCNTENCLR0, AMCNTENCLR1, AMCNTENSET0, AMCNTENSET1, AMCR, AMEVTYPER0<n>, and AMEVTYPER1<n>.

- In AArch32 state, MCRR or MRRC accesses to AMEVCNTR0<n> and AMEVCNTR1<n>, are trapped to EL2, reported using ESR_ELx.EC value 0x04.

<table>
<thead>
<tr>
<th>TAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses from EL1 and EL0 to Activity Monitor registers are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses from EL1 and EL0 to Activity Monitor registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [29:21]

Reserved, RES0.

TTA, bit [20]

Traps System register accesses to all implemented trace registers to EL2 when EL2 is enabled in the current Security state, from both Execution states as follows:

- In AArch64 state, accesses to trace registers with op0=2, op1=1, and CRn<0b1000 are trapped to EL2, reported using EC syndrome value 0x18.

- In AArch32 state, MRC or MCR accesses to trace registers with cpnum=14, opc1=1, and CRn<0b1000 are trapped to EL2, reported using EC syndrome value 0x05.

<table>
<thead>
<tr>
<th>TTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt at EL0, EL1, or EL2, to execute a System register access to an implemented trace register is trapped to EL2 when EL2 is enabled in the current Security state, unless it is trapped by CPACR.TRCDIS or CPACR_EL1.TTA.</td>
</tr>
</tbody>
</table>

Note

- The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are UNDEFINED, and any resulting exception is higher priority than an exception that would be generated because the value of CPTR_EL2.TTA is 1.
- EL2 does not provide traps on trace register accesses through the optional memory-mapped interface.
System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

If System register access to the trace functionality is not supported, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:14]**

Reserved, RES0.

**Bits [13:12]**

Reserved, RES1.

**Bit [11]**

Reserved, RES0.

**TFP, bit [10]**

Traps accesses to SVE, Advanced SIMD and floating-point functionality to EL2 when EL2 is enabled in the current Security state, from both Execution states, as follows:

- In AArch64 state, accesses to the following registers are trapped to EL2, reported using ESR_ELx.EC value 0x07:
  - FPCR, FPSR, FPEXC32_EL2, any of the SIMD and floating-point registers V0-V31, including their views as D0-D31 registers or S0-31 registers.
- In AArch32 state, accesses to the following registers are trapped to EL2, reported using ESR_ELx.EC value 0x07:
  - MVFR0, MVFR1, MVFR2, FPSCR, FPEXC, and any of the SIMD and floating-point registers Q0-15, including their views as D0-D31 registers or S0-31 registers. For the purposes of this trap, the architecture defines a VMSR access to FPSID from EL1 or higher as an access to a SIMD and floating-point register. Otherwise, permitted VMSR accesses to FPSID are ignored.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPTR_EL2.TZ has precedence over the value of CPTR_EL2.TFP.

<table>
<thead>
<tr>
<th>TFP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt at EL0, EL1 or EL2, to execute an instruction that uses the registers associated with SVE, Advanced SIMD and floating-point execution is trapped to EL2 when EL2 is enabled in the current Security state, subject to the exception prioritization rules.</td>
</tr>
</tbody>
</table>

**Note**

FPEXC32_EL2 is not accessible from EL0 using AArch64.

FPSID, MVFR0, MVFR1, and FPEXC are not accessible from EL0 using AArch32.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [9]**

Reserved, RES1.
TZ, bit [8]

When FEAT_SVE is implemented:

Traps execution at EL2, EL1, or EL0 of SVE instructions and instructions that directly access the ZCR_EL2 and ZCR_EL1 System registers to EL2 when EL2 is enabled in the current Security state.

The exception is reported using ESR_ELx.EC value 0x19.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPTR_EL2.TZ has precedence over the value of CPTR_EL2.TFP.

<table>
<thead>
<tr>
<th>TZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instruction to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control causes these instructions to be trapped, subject to the exception prioritization rules.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

Bits [7:0]

Reserved, RES1.

Accessing the CPTR_EL2

Accesses to this register use the following encodings:

**MRS <Xt>, CPTR_EL2**

```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return CPTR_EL2;
  end
elsif PSTATE.EL == EL3 then
  return CPTR_EL2;
else
  return CPTR_EL2;
end

**MSR CPTR_EL2, <Xt>**

```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if EL2Enabled() && CPTR_EL2.TCPAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        CPTR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    CPTR_EL2 = X[t];

MRS <Xt>, CPACR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif EL2Enabled() && CPTR_EL2.TCPAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
elsif PSTATE.EL == EL3 then
    return CPACR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return CPACR_EL1;
elsif PSTATE.EL == EL3 then
    return CPACR_EL1;
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif EL2Enabled() && CPTR_EL2.TCPAC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    CPACR_EL1 = X[t];
else
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    CPACR_EL1 = X[t];
else
  AArch64.SystemAccessTrap(EL3, 0x18);
elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
  NVMem[0x100] = X[t];
else
  CPACR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif HCR_EL2.E2H == '1' then
    CPTR_EL2 = X[t];
else
  CPACR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  CPACR_EL1 = X[t];
**CPTR_EL3, Architectural Feature Trap Register (EL3)**

The CPTR_EL3 characteristics are:

**Purpose**

Controls trapping to EL3 of accesses to CPACR, CPACR_EL1, HCPTR, CPTR_EL2, trace, Activity Monitor, SVE, Advanced SIMD and floating-point functionality.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to CPTR_EL3 are UNDEFINED.

**Attributes**

CPTR_EL3 is a 64-bit register.

**Field descriptions**

The CPTR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>TCPAC</th>
<th>TAM</th>
<th>RES0</th>
<th>TTA</th>
<th>RES0</th>
<th>TFP</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
</tr>
<tr>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
</tr>
<tr>
<td>47</td>
<td>46</td>
<td>45</td>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
</tr>
<tr>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**TCPAC, bit [31]**

Traps all of the following to EL3, from both Security states and both Execution states.

- EL2 accesses to CPTR_EL2, reported using ESR_ELx.EC value 0x18, or HCPTR, reported using ESR_ELx.EC value 0x03.
- EL2 and EL1 accesses to CPACR_EL1 reported using ESR_ELx.EC value 0x18, or CPACR reported using ESR_ELx.EC value 0x03.

When CPTR_EL3.TCPAC is:

<table>
<thead>
<tr>
<th>TCPAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 accesses to the CPTR_EL2 or HCPR, and EL2 and EL1 accesses to the CPACR_EL1 or CPACR, are trapped to EL3, unless they are trapped by CPTR_EL2.TCPAC.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TAM, bit [30]**

When FEAT_AMUv1 is implemented:

Trap Activity Monitor access. Traps EL2, EL1 and EL0 accesses to all Activity Monitor registers to EL3.

Accesses to the Activity Monitors registers are trapped as follows:

- In AArch64 state, the following registers are trapped to EL3 and reported with ESR_ELx.EC value 0x18:
AMUSERENR_EL0, AMCFGR_EL0, AMCGCR_EL0, AMCNTENCLR0_EL0, AMCNTENCLR1_EL0, AMCNTENSET0_EL0, AMCNTENSET1_EL0, AMCR_EL0, AMEVCNTR<n>_EL0, AMEVTCYPER<n>_EL0, and AMEVTPERM<n>_EL0.

- In AArch32 state, accesses with MRC or MCR to the following registers reported with ESR_ELx.EC value 0x03:
  - AMUSERENR, AMCFGR, AMCGCR, AMCNTENCLR0, AMCNTENCLR1, AMCNTENSET0, AMCNTENSET1, AMCR, AMEVTCYPER<n>, and AMEVTPERM<n>.

- In AArch32 state, accesses with MRRC or MCRR to the following registers, reported with ESR_ELx.EC value 0x04:
  - AMEVCNTR<n>, AMEVTCYPER1<n>.

### TAM

<table>
<thead>
<tr>
<th>TAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses from EL2, EL1, and EL0 to Activity Monitor registers are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses from EL2, EL1, and EL0 to Activity Monitor registers are trapped to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [29:21]**

Reserved, RES0.

**TTA, bit [20]**

Traps System register accesses. Accesses to the trace registers, from all Exception levels, both Security states, and both Execution states are trapped to EL3 as follows:

- In AArch64 state, Trace registers with op0=2, op1=1, and CRn<0b1000 are trapped to EL3 and reported using EC syndrome value 0x18.

- In AArch32 state, accesses using MCR or MRC to the Trace registers with cpnum=14, opc1=1, and CRn<0b1000 are reported using EC syndrome value 0x05.

<table>
<thead>
<tr>
<th>TTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any System register access to the trace registers is trapped to EL3, subject to the exception prioritization rules, unless it is trapped by CPACR.TRCDIS, CPACR_EL1.TTA or CPTER_EL2.TTA.</td>
</tr>
</tbody>
</table>

If System register access to trace functionality is not supported, this bit is RES0.

**Note**

The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are UNDEFINED, and any resulting exception is higher priority than this trap exception.

EL3 does not provide traps on trace register accesses through the Memory-mapped interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, no side-effects occur before the exception is taken, see 'Traps on instructions'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [19:11]

Reserved, RES0.

TFP, bit [10]

Traps all accesses to SVE, Advanced SIMD and floating-point functionality, from all Exception levels, both Security states, and both Execution states, to EL3.

This includes the following registers, all reported using ESR_ELx.EC value 0x07:

- **FPCR, FPSR, FPEXC32_EL2**, any of the SIMD and floating-point registers V0-V31, including their views as D0-D31 registers or S0-31 registers.
- **MVFR0, MVFR1, MVFR2, FPSCR, FPEXC**, and any of the SIMD and floating-point registers Q0-15, including their views as D0-D31 registers or S0-31 registers.

Permitted VMSR accesses to **FPSID** are ignored, but for the purposes of this trap the architecture define a VMSR access to the **FPSID** from EL1 or higher as an access to a SIMD and floating-point register.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPT_EL3.EZ has precedence over the value of CPT_EL3.TFP.

Defined values are:

<table>
<thead>
<tr>
<th>TFP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt at any Exception level to execute an instruction that uses the registers associated with SVE, Advanced SIMD and floating-point is trapped to EL3, subject to the exception prioritization rules.</td>
</tr>
</tbody>
</table>

Note

- **FPEXC32_EL2** is not accessible from EL0 using AArch64.
- **FPSID, MVFR0, MVFR1, and FPEXC** are not accessible from EL0 using AArch32.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [9]

Reserved, RES0.

EZ, bit [8]

When FEAT_SVE is implemented:

Traps execution of SVE instructions and instructions that directly access the **ZCR_EL3, ZCR_EL2, and ZCR_EL1** System registers, from all Exception levels and both Security states, to EL3.

The exception is reported using ESR_ELx.EC value 0x19.

Trapping behavior is affected by precedence as follows: A trap taken as a result of CPT_EL3.EZ has precedence over the value of CPT_EL3.TFP.

<table>
<thead>
<tr>
<th>EZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control causes these instructions executed at any Exception level to be trapped, subject to the exception prioritization rules.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instruction to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

Bits [7:0]

Reserved, RES0.

### Accessing the CPTR_EL3

Accesses to this register use the following encodings:

MRS <Xt>, CPTR_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return CPTR_EL3;

MSR CPTR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  CPTR_EL3 = X[t];
CSSELR_EL1, Cache Size Selection Register

The CSSELR_EL1 characteristics are:

**Purpose**

Selects the current Cache Size ID Register, CSIDR_EL1, by specifying the required cache level and the cache type (either instruction or data cache).

**Configuration**

AArch64 System register CSSELR_EL1 bits [31:0] are architecturally mapped to AArch32 System register CSSEL[31:0].

**Attributes**

CSSELR_EL1 is a 64-bit register.

**Field descriptions**

The CSSELR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>TnD, bit [4]</td>
</tr>
<tr>
<td>60</td>
<td>Level, bits [3:1]</td>
</tr>
<tr>
<td>59</td>
<td>InD</td>
</tr>
</tbody>
</table>

**Bits [63:5]**

Reserved, RES0.

**TnD, bit [4]**

*When FEAT_MTE is implemented:*

Allocation Tag not Data bit.

<table>
<thead>
<tr>
<th>TnD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Data, Instruction or Unified cache.</td>
</tr>
<tr>
<td>001</td>
<td>Separate Allocation Tag cache.</td>
</tr>
</tbody>
</table>

When CSSELR_EL1.InD == 1, this bit is RES0.

If CSSELR_EL1.Level is programmed to a cache level that is not implemented, then the value for this field on a read of CSSELR_EL1 is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Level, bits [3:1]**

Cache level of required cache.
<table>
<thead>
<tr>
<th>Level</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Level 1 cache.</td>
</tr>
<tr>
<td>0b001</td>
<td>Level 2 cache.</td>
</tr>
<tr>
<td>0b010</td>
<td>Level 3 cache.</td>
</tr>
<tr>
<td>0b011</td>
<td>Level 4 cache.</td>
</tr>
<tr>
<td>0b100</td>
<td>Level 5 cache.</td>
</tr>
<tr>
<td>0b101</td>
<td>Level 6 cache.</td>
</tr>
<tr>
<td>0b110</td>
<td>Level 7 cache.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If CSSEL_EL1.Level is programmed to a cache level that is not implemented, then the value for this field on a read of CSSEL_EL1 is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**InD, bit [0]**

Instruction not Data bit.

<table>
<thead>
<tr>
<th>InD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Data or unified cache.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction cache.</td>
</tr>
</tbody>
</table>

If CSSEL_EL1.Level is programmed to a cache level that is not implemented, then a read of CSSEL_EL1 is CONSTRAINED UNPREDICTABLE, and returns UNKNOWN values for CSSEL_EL1.{Level, InD}.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CSSEL_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, CSSEL_EL1**

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TID4 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CSSELR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return CSSEL_EL1;
  end if
elsif PSTATE.EL == EL2 then
  return CSSEL_EL1;
elsif PSTATE.EL == EL3 then
  return CSSEL_EL1;
end if
```

**MSR CSSEL_EL1, <Xt>**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b010</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TID4 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.CSSELR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    CSSELR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  CSSELR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  CSSELR_EL1 = X[t];
The CTR_EL0 characteristics are:

**Purpose**

Provides information about the architecture of the caches.

**Configuration**

AArch64 System register CTR_EL0 bits [31:0] are architecturally mapped to AArch32 System register CTR[31:0].

**Attributes**

CTR_EL0 is a 64-bit register.

**Field descriptions**

The CTR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | DIC | IDC | CWG | ERG | DminLine | L1Ip | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 |

**Bits [63:38]**

Reserved, RES0.

**TminLine, bits [37:32]**

When FEAT_MTE is implemented:

Tag minimum Line. $\log_2$ of the number of words covered by Allocation Tags in the smallest cache line of all caches which can contain Allocation tags that are controlled by the PE.

---

**Note**

- For an implementation with cache lines containing 64 bytes of data and 4 Allocation Tags, this will be $\log_2(64/4) = 4$.
- For an implementation with Allocations Tags in separate cache lines of 128 Allocation Tags per line, this will be $\log_2(128*16/4) = 9$.

---

**Otherwise:**

Reserved, RES0.

**Bit [31]**

Reserved, RES1.

**Bit [30]**

Reserved, RES0.
DIC, bit [29]

Instruction cache invalidation requirements for data to instruction coherence.

<table>
<thead>
<tr>
<th>DIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction cache invalidation to the Point of Unification is required for data to instruction coherence.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction cache invalidation to the Point of Unification is not required for data to instruction coherence.</td>
</tr>
</tbody>
</table>

IDC, bit [28]

Data cache clean requirements for instruction to data coherence. The meaning of this bit is:

<table>
<thead>
<tr>
<th>IDC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Data cache clean to the Point of Unification is required for instruction to data coherence, unless CLIDR_EL1.LoC == 0b000 or (CLIDR_EL1.LoUIS == 0b000 &amp;&amp; CLIDR_EL1.LoUU == 0b000).</td>
</tr>
<tr>
<td>0b1</td>
<td>Data cache clean to the Point of Unification is not required for instruction to data coherence.</td>
</tr>
</tbody>
</table>

CWG, bits [27:24]

Cache writeback granule. Log_2 of the number of words of the maximum size of memory that can be overwritten as a result of the eviction of a cache entry that has had a memory location in it modified.

A value of 0b0000 indicates that this register does not provide Cache writeback granule information and either:

- The architectural maximum of 512 words (2KB) must be assumed.
- The Cache writeback granule can be determined from maximum cache line size encoded in the Cache Size ID Registers.

Values greater than 0b1001 are reserved.

Arm recommends that an implementation that does not support cache write-back implements this field as 0b0001. This applies, for example, to an implementation that supports only write-through caches.

ERG, bits [23:20]

Exclusives reservation granule. Log_2 of the number of words of the maximum size of the reservation granule that has been implemented for the Load-Exclusive and Store-Exclusive instructions.

The use of the value 0b0000 is deprecated.

The value 0b0001 and values greater than 0b1001 are reserved.

DminLine, bits [19:16]

Log_2 of the number of words in the smallest cache line of all the data caches and unified caches that are controlled by the PE.

L1Ip, bits [15:14]

Level 1 instruction cache policy. Indicates the indexing and tagging policy for the L1 instruction cache. Possible values of this field are:

<table>
<thead>
<tr>
<th>L1Ip</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>VMID aware Physical Index, Physical tag (VPIPT)</td>
</tr>
<tr>
<td>0b01</td>
<td>ASID-tagged Virtual Index, Virtual Tag (AIVIVT)</td>
</tr>
<tr>
<td>0b10</td>
<td>Virtual Index, Physical Tag (VIPT)</td>
</tr>
<tr>
<td>0b11</td>
<td>Physical Index, Physical Tag (PIPT)</td>
</tr>
</tbody>
</table>

The value 0b01 is reserved in Armv8.
The value 0b00 is permitted only in an implementation that includes FEAT_VPIPT, otherwise the value is reserved.

**Bits [13:4]**

Reserved, RES0.

**ImiLine, bits [3:0]**

Log2 of the number of words in the smallest cache line of all the instruction caches that are controlled by the PE.

### Accessing the CTR_EL0

Accesses to this register use the following encodings:

```
MRS <Xt>, CTR_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCT == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TID2 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CTR_EL0;
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID2 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.CTR_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return CTR_EL0;
    end
elsif PSTATE.EL == EL2 then
    return CTR_EL0;
elsif PSTATE.EL == EL3 then
    return CTR_EL0;
```

30/09/2020 15:07; cceed0cb9f0899ceec50268e82aec9e71047211

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CurrentEL, Current Exception Level

The CurrentEL characteristics are:

**Purpose**

Holds the current Exception level.

**Configuration**

There are no configuration notes.

**Attributes**

CurrentEL is a 64-bit register.

**Field descriptions**

The CurrentEL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>EL</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>EL</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>57</td>
<td>EL</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>55</td>
<td>EL</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>53</td>
<td>EL</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>51</td>
<td>EL</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>49</td>
<td>EL</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>47</td>
<td>EL</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>45</td>
<td>EL</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>43</td>
<td>EL</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>41</td>
<td>EL</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>39</td>
<td>EL</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>37</td>
<td>EL</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>35</td>
<td>EL</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>33</td>
<td>EL</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:4]**

Reserved, RES0.

**EL, bits [3:2]**

Current Exception level. Possible values of this field are:

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>EL0</td>
</tr>
<tr>
<td>0b01</td>
<td>EL1</td>
</tr>
<tr>
<td>0b10</td>
<td>EL2</td>
</tr>
<tr>
<td>0b11</td>
<td>EL3</td>
</tr>
</tbody>
</table>

When the HCR_EL2 NV bit is 1, EL1 read accesses to the CurrentEL register return the value of 0b10 in this field.

This field resets to the highest implemented Exception Level.

**Bits [1:0]**

Reserved, RES0.

**Accessing the CurrentEL**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        return Zeros(60):'10':Zeros(2);
    else
        return Zeros(60):PSTATE.EL:Zeros(2);
    end if;
elsif PSTATE.EL == EL2 then
    return Zeros(60):PSTATE.EL:Zeros(2);
elsif PSTATE.EL == EL3 then
    return Zeros(60):PSTATE.EL:Zeros(2);
DACR32_EL2, Domain Access Control Register

The DACR32_EL2 characteristics are:

**Purpose**

Allows access to the AArch32 DACR register from AArch64 state only. Its value has no effect on execution in AArch64 state.

**Configuration**

AArch64 System register DACR32_EL2 bits [31:0] are architecturally mapped to AArch32 System register DACR[31:0].

This register is present only when EL1 is capable of using AArch32. Otherwise, direct accesses to DACR32_EL2 are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, and EL1 is capable of using AArch32, then this register is not RES0.

**Attributes**

DACR32_EL2 is a 64-bit register.

**Field descriptions**

The DACR32_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>D15</td>
<td>D14</td>
<td>D13</td>
<td>D12</td>
<td>D11</td>
<td>D10</td>
<td>D9</td>
<td>D8</td>
<td>D7</td>
<td>D6</td>
<td>D5</td>
<td>D4</td>
<td>D3</td>
<td>D2</td>
<td>D1</td>
<td>D0</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**D<n>, bits [2n+1:2n], for n = 15 to 0**

Domain n access permission, where n = 0 to 15. Permitted values are:

<table>
<thead>
<tr>
<th>D&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No access. Any access to the domain generates a Domain fault.</td>
</tr>
<tr>
<td>0b01</td>
<td>Client. Accesses are checked against the permission bits in the translation tables.</td>
</tr>
<tr>
<td>0b11</td>
<td>Manager: Accesses are not checked against the permission bits in the translation tables.</td>
</tr>
</tbody>
</table>

The value 0b10 is reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DACR32_EL2**

Accesses to this register use the following encodings:
MRS <Xt>, DACR32_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return DACR32_EL2;
elsif PSTATE.EL == EL3 then
  return DACR32_EL2;

MSR DACR32_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  DACR32_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  DACR32_EL2 = X[t];

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DAIF, Interrupt Mask Bits

The DAIF characteristics are:

Purpose

Allows access to the interrupt mask bits.

Configuration

There are no configuration notes.

Attributes

DAIF is a 64-bit register.

Field descriptions

The DAIF bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | D | A | I | F | RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:10]

Reserved, RES0.

D, bit [9]

Process state D mask. The possible values of this bit are:

<table>
<thead>
<tr>
<th>D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint, Breakpoint, and Software Step exceptions targeted at the current Exception level are not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint, Breakpoint, and Software Step exceptions targeted at the current Exception level are masked.</td>
</tr>
</tbody>
</table>

When the target Exception level of the debug exception is higher than the current Exception level, the exception is not masked by this bit.

On a Warm reset, this field resets to 1.

A, bit [8]

SError interrupt mask bit. The possible values of this bit are:

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 1.

I, bit [7]

IRQ mask bit. The possible values of this bit are:
### DAIF, Interrupt Mask Bits

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 1.

### F, bit [6]

FIQ mask bit. The possible values of this bit are:

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 1.

### Bits [5:0]

Reserved, RES0.

### Accessing the DAIF

Accesses to this register use the following encodings:

**MRS <Xt>, DAIF**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if (EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') || SCTLR_EL1.UMA == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        return Zeros(54):PSTATE.<D,A,I,F>:Zeros(6);
elsif PSTATE.EL == EL1 then
    return Zeros(54):PSTATE.<D,A,I,F>:Zeros(6);
elsif PSTATE.EL == EL2 then
    return Zeros(54):PSTATE.<D,A,I,F>:Zeros(6);
elsif PSTATE.EL == EL3 then
    return Zeros(54):PSTATE.<D,A,I,F>:Zeros(6);

MSR DAIF, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' || SCTLR_EL1.UMA == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        PSTATE.<D,A,I,F> = X[t]<9:6>;
    endif
elsif PSTATE.EL == EL1 then
    PSTATE.<D,A,I,F> = X[t]<9:6>;
elsif PSTATE.EL == EL2 then
    PSTATE.<D,A,I,F> = X[t]<9:6>;
elsif PSTATE.EL == EL3 then
    PSTATE.<D,A,I,F> = X[t]<9:6>;
else
    PSTATE.<D,A,I,F> = X[t]<9:6>;
endif

MSR DAIFSet, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b110</td>
</tr>
</tbody>
</table>

MSR DAIFClr, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
**DBGAUTHSTATUS_EL1, Debug Authentication Status register**

The DBGAUTHSTATUS_EL1 characteristics are:

**Purpose**

Provides information about the state of the IMPLEMENTATION DEFINED authentication interface for debug.

**Configuration**

AArch64 System register DBGAUTHSTATUS_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGAUTHSTATUS[31:0].

AArch64 System register DBGAUTHSTATUS_EL1 bits [31:0] are architecturally mapped to External register DBGAUTHSTATUS_EL1[31:0].

**Attributes**

DBGAUTHSTATUS_EL1 is a 64-bit register.

**Field descriptions**

The DBGAUTHSTATUS_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>SNID, bits [7:6]</td>
</tr>
<tr>
<td>60</td>
<td>Bits [63:8]</td>
</tr>
</tbody>
</table>

**Bits [63:8]**

Reserved, RES0.

**SNID, bits [7:6]**

*When FEAT_Debugv8p4 is implemented:*

Secure non-invasive debug.

This field has the same value as DBGAUTHSTATUS_EL1.SID.

*Otherwise:*

Secure non-invasive debug.

<table>
<thead>
<tr>
<th>SNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.
**SID, bits [5:4]**

Secure invasive debug.

<table>
<thead>
<tr>
<th>SID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSNID, bits [3:2]**

When FEAT_Debugv8p4 is implemented:

Non-secure non-invasive debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. EL3 is implemented or the Effective value of SCR_EL3.NS is 1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Otherwise:

Non-secure non-invasive debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSID, bits [1:0]**

Non-secure invasive debug.

<table>
<thead>
<tr>
<th>NSID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Accessing the DBGAUTHSTATUS_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, DBGAUTHSTATUS_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

Page 317
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGAUTHSTATUS_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return DBGAUTHSTATUS_EL1;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return DBGAUTHSTATUS_EL1;
    end if
elsif PSTATE.EL == EL3 then
    return DBGAUTHSTATUS_EL1;
else
    return DBGAUTHSTATUS_EL1;
end if
DBGBCR<n>_EL1, Debug Breakpoint Control Registers, n = 0 - 15

The DBGBCR<n>_EL1 characteristics are:

**Purpose**

Holds control information for a breakpoint. Forms breakpoint n together with value register DBGVR<n>_EL1.

**Configuration**

AArch64 System register DBGBCR<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGBCR<n>[31:0].

AArch64 System register DBGBCR<n>_EL1 bits [31:0] are architecturally mapped to External register DBGBCR<n>_EL1[31:0].

If breakpoint n is not implemented, accesses to this register are UNDEFINED.

**Attributes**

DBGBCR<n>_EL1 is a 64-bit register.

**Field descriptions**

The DBGBCR<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23-20</td>
<td>Breakpoint Type, BT</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**BT, bits [23:20]**

Breakpoint Type. Possible values are:
<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Unlinked instruction address match. DBGBVR&lt;n&gt;_EL1 is the address of an instruction.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As 0b0000, but linked to a Context matching breakpoint.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Unlinked Context ID match. When FEAT_VHE is implemented, EL2 is using AArch64, and the Effective value of HCR_EL2.E2H is 1, if either the PE is executing at EL0 with HCR_EL2.TGE set to 1 or the PE is executing at EL2, then DBGBVR&lt;n&gt;_EL1.ContextID must match the CONTEXTIDR_EL2 value. Otherwise, DBGBVR&lt;n&gt;_EL1.ContextID must match the CONTEXTIDR_EL1 value</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, with linking enabled.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Unlinked VMID match. DBGBVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As 0b1000, with linking enabled.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Unlinked VMID and Context ID match. DBGBVR&lt;n&gt;_EL1.ContextID is a Context ID compared against CONTEXTIDR_EL1, and DBGBVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b0111</td>
<td>As 0b1100, with linking enabled.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Unlinked VMID match. DBGBVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Unlinked VMID and Context ID match. DBGBVR&lt;n&gt;_EL1.ContextID is a Context ID compared against CONTEXTIDR_EL1, and DBGBVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b1011</td>
<td>As 0b1010, with linking enabled.</td>
</tr>
<tr>
<td>0b1100</td>
<td>Unlinked CONTEXTIDR_EL2 match. DBGBVR&lt;n&gt;_EL1.ContextID2 is a Context ID compared against CONTEXTIDR_EL2.</td>
</tr>
<tr>
<td>0b1101</td>
<td>As 0b1100, with linking enabled.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Unlinked Full Context ID match. DBGBVR&lt;n&gt;_EL1.ContextID is compared against CONTEXTIDR_EL1, and DBGBVR&lt;n&gt;_EL1.ContextID2 is compared against CONTEXTIDR_EL2.</td>
</tr>
<tr>
<td>0b1111</td>
<td>As 0b1110, with linking enabled.</td>
</tr>
</tbody>
</table>

All other values are reserved. Constraints on breakpoint programming mean other values are reserved under some conditions.

The fields that indicate when the breakpoint can be generated are: HMC, SSC, and PMC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

For more information on the effect of programming the fields to a reserved value, see 'Reserved DBGBCR<n>_EL1.BT values'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**LBN, bits [19:16]**

Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.

For all other breakpoint types this field is ignored and reads of the register return an UNKNOWN value.

This field is ignored when the value of DBGBCR<n>_EL1.E is 0.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**SSC, bits [15:14]**

Security state control. Determines the Security states under which a Breakpoint debug event for breakpoint n is generated.

The fields that indicate when the breakpoint can be generated are: HMC, SSC, and PMC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.
For more information on the operation of these fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

For more information on the effect of programming the fields to a reserved set of values, see 'Reserved DBGBCR<n>_EL1.{SSC, HMC, PMC} values'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**HMC, bit [13]**

Higher mode control. Determines the debug perspective for deciding when a Breakpoint debug event for breakpoint n is generated.

The fields that indicate when the breakpoint can be generated are: HMC, SSC, and PMC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

For more information, see DBGBCR<n>_EL1.SSC.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [12:9]**

Reserved, RES0.

**BAS, bits [8:5]**

_When AArch32 is supported at any Exception level:_

Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and Execution state.

The permitted values depend on the breakpoint type.

For Address match breakpoints, the permitted values are:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Match instruction at</th>
<th>Constraint for debuggers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0011</td>
<td>DBGBVR&lt;n&gt;_EL1</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1100</td>
<td>DBGBVR&lt;n&gt;_EL1 + 2</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1111</td>
<td>DBGBVR&lt;n&gt;_EL1</td>
<td>Use for A64 and A32 instructions</td>
</tr>
</tbody>
</table>

All other values are reserved. For more information, see 'Reserved DBGBCR<n>_EL1.BAS values'.

For more information on using the BAS field in address match breakpoints, see 'Using the BAS field in Address Match breakpoints'.

For Context matching breakpoints, this field is RES1 and ignored.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.

**Bits [4:3]**

Reserved, RES0.

**PMC, bits [2:1]**

Privilege mode control. Determines the Exception level or levels at which a Breakpoint debug event for breakpoint n is generated.
The fields that indicate when the breakpoint can be generated are: HMC, SSC, and PMC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

For more information, see DBGBCR<n>_EL1.SSC.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**E, bit [0]**

Enable breakpoint DBGVR<n>_EL1.

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Breakpoint disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Breakpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGBCR<n>_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, DBGBCR<n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
            Halt(DebugHalt_SoftwareAccess);
        else
            return DBGBCR_EL1[UInt(CRm<3:0>)];
        end if;
    end if;
elsif PSTATE_EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        if HaltingAllowed() then
            Halt(DebugHalt_SoftwareAccess);
        else
            return DBGBCR_EL1[UInt(CRm<3:0>)];
        end if;
    end if;
elsif PSTATE_EL == EL3 then
    if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        return DBGBCR_EL1[UInt(CRm<3:0>)];
    end if;
end if;

MSR DBGBCR<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGCRn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
  Halt(DebugHalt_SoftwareAccess);
else
  DBGCR_EL1[UInt(CRm<3:0>)] = X[t];
endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
      Halt(DebugHalt_SoftwareAccess);
    else
      DBGCR_EL1[UInt(CRm<3:0>)] = X[t];
    endif
  endif
elsif PSTATE.EL == EL3 then
  if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGCR_EL1[UInt(CRm<3:0>)] = X[t];
endif
The DBGBVR<n> EL1 characteristics are:

**Purpose**

Holds a virtual address, or a VMID and/or a context ID, for use in breakpoint matching. Forms breakpoint n together with control register DBGBCR<n> EL1.

**Configuration**

AArch64 System register DBGBVR<n> EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGBVR<n>[31:0].

AArch64 System register DBGBVR<n> EL1 bits [63:32] are architecturally mapped to AArch32 System register DBGBXVR<n>[31:0].

AArch64 System register DBGBVR<n> EL1 bits [63:0] are architecturally mapped to External register DBGBVR<n> EL1[63:0].

How this register is interpreted depends on the value of DBGBCR<n> EL1.BT.

- When DBGBCR<n> EL1.BT is 0b000x, this register holds a virtual address.
- When DBGBCR<n> EL1.BT is 0b001x, 0b011x, or 0b110x, this register holds a Context ID.
- When DBGBCR<n> EL1.BT is 0b100x, this register holds a VMID.
- When DBGBCR<n> EL1.BT is 0b101x, this register holds a VMID and a Context ID.
- When DBGBCR<n> EL1.BT is 0b111x, this register holds two Context ID values.

For other values of DBGBCR<n> EL1.BT, this register is RES0.

If breakpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGBVR<n> EL1 is a 64-bit register.

**Field descriptions**

The DBGBVR<n> EL1 bit assignments are:

**When DBGBCR<n> EL1.BT == 0b000x:**

|------------|----------|------|

**RESS[14:4], bits [63:53]**

Reserved, Sign extended. Software must set all bits in this field to the same value as the most significant bit of the VA field. If all bits in this field are not the same value as the most significant bit of the VA field, then all of the following apply:

- It is CONSTRAINED UNPREDICTABLE whether the PE ignores this field when comparing an address.
- If the breakpoint is not context-aware, it is IMPLEMENTATION DEFINED whether the value read back in each bit of this field is a copy of the most significant bit of the VA field or the value written.
VA[52:49], bits [52:49]

When FEAT_LVA is implemented:


On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:


VA[48:2], bits [48:2]

Bits[48:2] of the address value for comparison.

When FEAT_LVA is implemented, VA[52:49] forms the upper part of the address value. Otherwise, bits [52:49] are part of the RESS field.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [1:0]

Reserved, RES0.

When DBGBCR<n>_EL1.BT == 0b001x:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ContextID |

Bits [63:32]

Reserved, RES0.

ContextID, bits [31:0]

Context ID value for comparison.

The value is compared against CONTEXTIDR_EL2 when (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented), HCR_EL2.E2H is 1, and either:

- The PE is executing at EL2.
- HCR_EL2.TGE is 1, the PE is executing at EL0, and EL2 is enabled in the current Security state.

Otherwise, the value is compared against CONTEXTIDR_EL1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR<n>_EL1.BT == 0b011x:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ContextID |

Bits [63:32]

Reserved, RES0.
ContextID, bits [31:0]

Context ID value for comparison against CONTEXTIDR_EL1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR<n>_EL1.BT == 0b100x and EL2 is implemented:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Bits [63:48]

Reserved, RES0.

VMID[15:8], bits [47:40]

When FEAT_VMID16 is implemented, VTCR_EL2.VS == 1 and EL2 is using AArch64:

Extension to VMID[7:0]. See DBGBVR<n>_EL1.VMID[7:0] for more details.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

VMID[7:0], bits [39:32]

VMID value for comparison.

The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [31:0]

Reserved, RES0.

When DBGBCR<n>_EL1.BT == 0b101x and EL2 is implemented:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Bits [63:48]

Reserved, RES0.

VMID[15:8], bits [47:40]

When FEAT_VMID16 is implemented, VTCR_EL2.VS == 1 and EL2 is using AArch64:

Extension to VMID[7:0]. See DBGBVR<n>_EL1.VMID[7:0] for more details.
On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**VMID[7:0], bits [39:32]**

VMID value for comparison.

The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**ContextID, bits [31:0]**

Context ID value for comparison against CONTEXTIDR_EL1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**When DBGBCR<n> _EL1.BT == 0b110x, EL2 is implemented and (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented):**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
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**ContextID2, bits [63:32]**

Context ID value for comparison against CONTEXTIDR_EL2.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [31:0]**

Reserved, RES0.

**When DBGBCR<n> _EL1.BT == 0b111x, EL2 is implemented and (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented):**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
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**ContextID2, bits [63:32]**

Context ID value for comparison against CONTEXTIDR_EL2.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**ContextID, bits [31:0]**

Context ID value for comparison against CONTEXTIDR_EL1.
On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the DBGBVR<\n>_EL1

Accesses to this register use the following encodings:

MRS \(<Xt>, \ DBGBVR<\n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGBVRn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
            Halt(DebugHalt_SoftwareAccess);
        else
            return DBGBVR_EL1[UInt(CRm<3:0>)];
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
                Halt(DebugHalt_SoftwareAccess);
            else
                return DBGBVR_EL1[UInt(CRm<3:0>)];
        elsif PSTATE.EL == EL3 then
            if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
                Halt(DebugHalt_SoftwareAccess);
            else
                return DBGBVR_EL1[UInt(CRm<3:0>)];

MSR DBGBVR<\n>_EL1, \(<Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGBVRn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    DBGBVR_EL1[UInt(CRm<3:0>)] = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    DBGBVR_EL1[UInt(CRm<3:0>)] = X[t];
  end
elsif PSTATE.EL == EL3 then
  if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBVR_EL1[UInt(CRm<3:0>)] = X[t];
  end
else
  DBGBVR_EL1[UInt(CRm<3:0>)] = X[t];
end
The DBGCLAIMCLR_EL1 characteristics are:

**Purpose**

Used by software to read the values of the CLAIM tag bits, and to clear CLAIM tag bits to 0.

The architecture does not define any functionality for the CLAIM tag bits.

**Note**

CLAIM tags are typically used for communication between the debugger and target software.

Used in conjunction with the DBGCLAIMSET_EL1 register.

**Configuration**

AArch64 System register DBGCLAIMCLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGCLAIMCLR[31:0].

AArch64 System register DBGCLAIMCLR_EL1 bits [31:0] are architecturally mapped to External register DBGCLAIMCLR_EL1[31:0].

An implementation must include eight CLAIM tag bits.

**Attributes**

DBGCLAIMCLR_EL1 is a 64-bit register.

**Field descriptions**

The DBGCLAIMCLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31-24</td>
<td>Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.</td>
</tr>
<tr>
<td>7-0</td>
<td>CLAIM, bits [7:0]</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:8]**

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.

**CLAIM, bits [7:0]**

Read or clear CLAIM tag bits. Reading this field returns the current value of the CLAIM tag bits.

Writing a 1 to one of these bits clears the corresponding CLAIM tag bit to 0. This is an indirect write to the CLAIM tag bits. A single write operation can clear multiple CLAIM tag bits to 0.

Writing 0 to one of these bits has no effect.
On a Cold reset, this field resets to 0.

**Accessing the DBGCLAIMCLR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, DBGCLAIMCLR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && !HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGCLAIM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        return DBGCLAIMCLR_EL1;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && MDCR_EL3.TDA == '1' then
            UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGCLAIMCLR_EL1;
    elsif PSTATE.EL == EL3 then
        return DBGCLAIMCLR_EL1;
   🆚

**MSR DBGCLAIMCLR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGCLAIM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    DBGCLAIMCLR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    DBGCLAIMCLR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  DBGCLAIMCLR_EL1 = X[t];
else
  DBGCLAIMCLR_EL1 = X[t];

DBGCLAIMSET_EL1, Debug CLAIM Tag Set register

The DBGCLAIMSET_EL1 characteristics are:

**Purpose**

Used by software to set the CLAIM tag bits to 1.

The architecture does not define any functionality for the CLAIM tag bits.

---

**Note**

CLAIM tags are typically used for communication between the debugger and target software.

---

Used in conjunction with the DBGCLAIMCLR_EL1 register.

**Configuration**

AArch64 System register DBGCLAIMSET_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGCLAIMSET[31:0].

AArch64 System register DBGCLAIMSET_EL1 bits [31:0] are architecturally mapped to External register DBGCLAIMSET_EL1[31:0].

An implementation must include eight CLAIM tag bits.

**Attributes**

DBGCLAIMSET_EL1 is a 64-bit register.

**Field descriptions**

The DBGCLAIMSET_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
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<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
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</table>

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
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<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAZ/SBZ</td>
<td>CLAIM</td>
<td></td>
<td></td>
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</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:8]**

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.

**CLAIM, bits [7:0]**

Set CLAIM tag bits.

This field is RAO.

Writing a 1 to one of these bits sets the corresponding CLAIM tag bit to 1. This is an indirect write to the CLAIM tag bits. A single write operation can set multiple CLAIM tag bits to 1.
Writing 0 to one of these bits has no effect.

**Accessing the DBGCLAIMSET_EL1**

Accesses to this register use the following encodings:

\[
\begin{array}{cccccc}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b10 & 0b000 & 0b0111 & 0b1000 & 0b110 \\
\end{array}
\]

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGCLAIM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  else
    return DBGCLAIMSET_EL1;
  endif;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  else
    return DBGCLAIMSET_EL1;
  endif;
elsif PSTATE.EL == EL3 then
  return DBGCLAIMSET_EL1;
end if;
```

\[
\begin{array}{cccccc}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b10 & 0b000 & 0b0111 & 0b1000 & 0b110 \\
\end{array}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGCLAIM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        DBGCLAIMSET_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        DBGCLAIMSET_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    DBGCLAIMSET_EL1 = X[t];
else
    DBGCLAIMSET_EL1 = X[t];
DBGDTR_EL0, Debug Data Transfer Register, half-duplex

The DBGDTR_EL0 characteristics are:

**Purpose**

Transfers 64 bits of data between the PE and an external debugger. Can transfer both ways using only a single register.

**Configuration**

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to AArch32 System register DBGDTRRXint[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to External register DBGDTRRX_EL0[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to AArch64 System register DBGDTRRX_EL0[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRTXint[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [31:0] are architecturally mapped to External register DBGDTRTX_EL0[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [31:0] are architecturally mapped to AArch64 System register DBGDTRTX_EL0[31:0] when written.

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to AArch32 System register DBGDTRTXint[31:0] when read.

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to External register DBGDTRTX_EL0[31:0] when read.

AArch64 System register DBGDTR_EL0 bits [63:32] are architecturally mapped to AArch64 System register DBGDTRTXint[31:0] when read.

AArch64 System register DBGDTR_EL0 bits [31:0] are architecturally mapped to External register DBGDTRTX_EL0[31:0] when read.

AArch64 System register DBGDTR_EL0 bits [31:0] are architecturally mapped to AArch64 System register DBGDTRTX_EL0[31:0] when read.

**Attributes**

DBGDTR_EL0 is a 64-bit register.

**Field descriptions**

The DBGDTR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Mapping</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
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</tbody>
</table>
HighWord, bits [63:32]

Writes to this register set DTRRX to the value in this field and do not change RXfull.

Reads of this register:

- If RXfull is set to 1, return the last value written to DTRTX.
- If RXfull is set to 0, return an **UNKNOWN** value.

After the read, RXfull is cleared to 0.

LowWord, bits [31:0]

Writes to this register set DTRTX to the value in this field and set TXfull to 1.

Reads of this register:

- If RXfull is set to 1, return the last value written to DTRRX.
- If RXfull is set to 0, return an **UNKNOWN** value.

After the read, RXfull is cleared to 0.

**Accessing the DBGDTR_EL0**

Accesses to this register use the following encodings:

```
MRS <Xt>, DBGDTR_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b011</td>
<td>0b000</td>
<td>0b010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if Halted() then
    return DBGDTR_EL0;
elsif PSTATE.EL == EL0 then
    if MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDA> != '00') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTR_EL0;
    end if;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTR_EL0;
    end if;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTR_EL0;
    end if;
elsif PSTATE.EL == EL3 then
    return DBGDTR_EL0;
end if;

MSR DBGDTR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b011</td>
<td>0b0000</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if Halted() then
    DBGDTR_EL0 = X[t];
elsif PSTATE_EL == EL0 then
    if MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    elsif EL2Enabled() & MDSCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (HCR_EL2.TGE == '1' || MDSCR_EL2.<TDE,TDA> != '00') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        DBGDTR_EL0 = X[t];
    endif
elsif PSTATE_EL == EL1 then
    if EL2Enabled() & MDSCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        DBGDTR_EL0 = X[t];
    endif
elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        DBGDTR_EL0 = X[t];
    endif
elsif PSTATE_EL == EL3 then
    DBGDTR_EL0 = X[t];
The DBGDTRRX_EL0 characteristics are:

**Purpose**

Transfers data from an external debugger to the PE. For example, it is used by a debugger transferring commands and data to a debug target. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communications Channel.

**Configuration**

AArch64 System register DBGDTRRX_EL0 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRRXint[31:0].

AArch64 System register DBGDTRRX_EL0 bits [31:0] are architecturally mapped to External register DBGDTRRX_EL0[31:0].

**Attributes**

DBGDTRRX_EL0 is a 64-bit register.

**Field descriptions**

The DBGDTRRX_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved</td>
</tr>
<tr>
<td>62</td>
<td>Update DTRRX</td>
</tr>
<tr>
<td>61</td>
<td>Reserved</td>
</tr>
<tr>
<td>60</td>
<td>Reserved</td>
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<td>59</td>
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<td>33</td>
<td>Reserved</td>
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<tr>
<td>32</td>
<td>Reserved</td>
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</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

Update DTRRX.

Reads of this register:

- If RXfull is set to 1, return the last value written to DTRRX.
- If RXfull is set to 0, return an **UNKNOWN** value.

After the read, RXfull is cleared to 0.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the DBGDTRRX_EL0**

Accesses to this register use the following encodings:
if Halted() then
    return DBGDTRRX_EL0;
elsif PSTATE.EL == EL0 then
    if MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    endif
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDA> != '00') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTRRX_EL0;
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTRRX_EL0;
    endif
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return DBGDTRRX_EL0;
    endif
elsif PSTATE.EL == EL3 then
    return DBGDTRRX_EL0;
DBGDTRTX_EL0, Debug Data Transfer Register, Transmit

The DBGDTRTX_EL0 characteristics are:

**Purpose**

Transfers data from the PE to an external debugger. For example, it is used by a debug target to transfer data to the debugger. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communication Channel.

**Configuration**

AArch64 System register DBGDTRTX_EL0 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRTXint[31:0].

AArch64 System register DBGDTRTX_EL0 bits [31:0] are architecturally mapped to External register DBGDTRTX_EL0[31:0].

**Attributes**

DBGDTRTX_EL0 is a 64-bit register.

**Field descriptions**

The DBGDTRTX_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>Return DTRTX</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

Return DTRTX.

Writes to this register:

- If TXfull is set to 1, set DTRRX and DTRTX to UNKNOWN.
- If TXfull is set to 0, update the value in DTRTX.

After the write, TXfull is set to 1.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGDTRTX_EL0**

Accesses to this register use the following encodings:
if Halted() then
    DBGDTRTX_EL0 = X[t];
elsif PSTATE.EL == EL0 then
    if MDSCR_EL1.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    endif
elsif EL2Enabled() && (HCR_EL2.TGE == '1' || MDSCR_EL2.<TDE,TDA> != '00') then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    DBGDTRTX_EL0 = X[t];
endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && MDSCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    endif
elsif EL2Enabled() && MDSCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    DBGDTRTX_EL0 = X[t];
endif
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    DBGDTRTX_EL0 = X[t];
endif
elsif PSTATE.EL == EL3 then
    DBGDTRTX_EL0 = X[t];
endfunction
DBGPRCR_EL1, Debug Power Control Register

The DBGPRCR_EL1 characteristics are:

**Purpose**

Controls behavior of the PE on powerdown request.

**Configuration**

AArch64 System register DBGPRCR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGPRCR[31:0].

Bit [0] of this register is mapped to EDPRCR.CORENPDRQ, bit [0] of the external view of this register.

The other bits in these registers are not mapped to each other.

**Attributes**

DBGPRCR_EL1 is a 64-bit register.

**Field descriptions**

The DBGPRCR_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| RES0| CORENPDRQ |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:1]**

Reserved, RES0.

**CORENPDRQ, bit [0]**

*When FEAT_DoPD is implemented:*

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to its Cold reset value on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states see 'Core power domain power states'.

**Note**
Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, if the powerup request is implemented and the powerup request has been asserted, this field is set to an IMPLEMENTATION DEFINED choice of 0 or 1. If the powerup request is not asserted, this field is set to 0.

Otherwise:

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to the value of EDPRCR, COREPURQ on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states see 'Core power domain power states'.

Note

Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, this field resets to the value in EDPRCR, COREPURQ.

Accessing the DBGPRCR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, DBGPRCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGPRCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDOSA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    end if
else
    return DBGPRCR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    end if
else
    return DBGPRCR_EL1;
elsif PSTATE.EL == EL3 then
    return DBGPRCR_EL1;
end if

MSR DBGPRCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGPRCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDOSA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        DBGPRCR_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        DBGPRCR_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    DBGPRCR_EL1 = X[t];
else
    DBGPRCR_EL1 = X[t];
**DBGVCR32_EL2, Debug Vector Catch Register**

The DBGVCR32_EL2 characteristics are:

**Purpose**

Allows access to the AArch32 register DBGVCR from AArch64 state only. Its value has no effect on execution in AArch64 state.

**Configuration**

AArch64 System register DBGVCR32_EL2 bits [31:0] are architecturally mapped to AArch32 System register DBGVCR[31:0].

This register is present only when EL1 is capable of using AArch32. Otherwise, direct accesses to DBGVCR32_EL2 are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, and EL1 is capable of using AArch32, then this register is not present.

**Attributes**

DBGVCR32_EL2 is a 64-bit register.

**Field descriptions**

The DBGVCR32_EL2 bit assignments are:

**When EL3 is implemented:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NSF| NSI| RES0| NSF| NSD| NSP| NSI| RES0| SF| SI| RES0| SD| SP| SS| SU| RES0|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**Bits [63:32]**

Reserved, RES0.

**NSF, bit [31]**

FIQ vector catch enable in Non-secure state.

The exception vector offset is 0x1C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**NSI, bit [30]**

IRQ vector catch enable in Non-secure state.

The exception vector offset is 0x18.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [29]**

Reserved, RES0.
NSD, bit [28]
Data Abort vector catch enable in Non-secure state.
The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSP, bit [27]
Prefetch Abort vector catch enable in Non-secure state.
The exception vector offset is 0x0C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSS, bit [26]
Supervisor Call (SVC) vector catch enable in Non-secure state.
The exception vector offset is 0x08.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSU, bit [25]
Undefined Instruction vector catch enable in Non-secure state.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [24:8]
Reserved, RES0.

SF, bit [7]
FIQ vector catch enable in Secure state.
The exception vector offset is 0x1C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SI, bit [6]
IRQ vector catch enable in Secure state.
The exception vector offset is 0x18.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]
Reserved, RES0.

SD, bit [4]
Data Abort vector catch enable in Secure state.
The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
SP, bit [3]

Prefetch Abort vector catch enable in Secure state.
The exception vector offset is 0x0C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SS, bit [2]

Supervisor Call (SVC) vector catch enable in Secure state.
The exception vector offset is 0x08.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SU, bit [1]

Undefined Instruction vector catch enable in Secure state.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [0]

Reserved, RES0.

When EL3 is not implemented:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | F | I | RES0 | D | P | S | U | RES0 |

Bits [63:8]

Reserved, RES0.

F, bit [7]

FIQ vector catch enable.
The exception vector offset is 0x1C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [6]

IRQ vector catch enable.
The exception vector offset is 0x18.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.
D, bit [4]

Data Abort vector catch enable.
The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

P, bit [3]

Prefetch Abort vector catch enable.
The exception vector offset 0x0C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

S, bit [2]

Supervisor Call (SVC) vector catch enable.
The exception vector offset is 0x08.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

U, bit [1]

Undefined Instruction vector catch enable.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [0]

Reserved, RES0.

Accessing the DBGVCR32_EL2

Accesses to this register use the following encodings:

```
MRS <Xt>, DBGVCR32_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elifs HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return DBGVCR32_EL2;
elif PSTATE.EL == EL3 then
    return DBGVCR32_EL2;

MSR DBGVCR32_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elifs HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return DBGVCR32_EL2 = X[t];
elif PSTATE.EL == EL3 then
    DBGVCR32_EL2 = X[t];
DBGWCR<n>_EL1, Debug Watchpoint Control Registers, n = 0 - 15

The DBGWCR<n>_EL1 characteristics are:

**Purpose**

Holds control information for a watchpoint. Forms watchpoint n together with value register DBGWVR<n>_EL1.

**Configuration**

AArch64 System register DBGWCR<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGWCR<n>[31:0].

AArch64 System register DBGWCR<n>_EL1 bits [31:0] are architecturally mapped to External register DBGWCR<n>_EL1[31:0].

If watchpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGWCR<n>_EL1 is a 64-bit register.

**Field descriptions**

The DBGWCR<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:29]</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>[28:24]</td>
<td>MASK, bits</td>
</tr>
</tbody>
</table>

**Bits [63:29]**

Reserved, RES0.

**MASK, bits [28:24]**

Address mask. Only objects up to 2GB can be watched using a single mask.

<table>
<thead>
<tr>
<th>MASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000</td>
<td>No mask.</td>
</tr>
<tr>
<td>0b00001</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b00010</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

If programmed with a reserved value, a watchpoint must behave as if either:

- MASK has been programmed with a defined value, which might be 0 (no mask), other than for a direct read of DBGWCRn_EL1.
- The watchpoint is disabled.

Software must not rely on this property because the behavior of reserved values might change in a future revision of the architecture.

Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits (0x00000007 mask for address) to 0b11111 masking 31 address bits (0x7FFFFFFF mask for address).

On a Cold reset, this field resets to an architecturally UNKNOWN value.
**Bits [23:21]**

Reserved, RES0.

**WT, bit [20]**

Watchpoint type. Possible values are:

<table>
<thead>
<tr>
<th>WT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unlinked data address match.</td>
</tr>
<tr>
<td>0b1</td>
<td>Linked data address match.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**LBN, bits [19:16]**

Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**SSC, bits [15:14]**

Security state control. Determines the Security states under which a Watchpoint debug event for watchpoint n is generated.

The fields that indicate when the watchpoint can be generated are: HMC, SSC, and PAC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

For more information on the effect of programming the fields to a reserved value, see 'Reserved DBGBCR<n>_EL1.{SSC, HMC, PMC} values'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**HMC, bit [13]**

Higher mode control. Determines the debug perspective for deciding when a Watchpoint debug event for watchpoint n is generated.

The fields that indicate when the watchpoint can be generated are: HMC, SSC, and PAC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see 'Execution conditions for which a watchpoint generates Watchpoint exceptions'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**BAS, bits [12:5]**

Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.

<table>
<thead>
<tr>
<th>BAS</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxxx111</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1</td>
</tr>
<tr>
<td>xxxx1xxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 1</td>
</tr>
<tr>
<td>xxxx1xx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 2</td>
</tr>
<tr>
<td>xxxx1xx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 3</td>
</tr>
</tbody>
</table>

In cases where DBGWVR<n>_EL1 addresses a double-word:

The valid values for BAS are non-zero binary numbers all of whose set bits are contiguous. All other values are reserved and must not be used by software. See ‘Reserved DBGWCR<n>_EL1.BAS values’.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**LSC, bits [4:3]**

Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are:

<table>
<thead>
<tr>
<th>LSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>Match instructions that load from a watchpointed address.</td>
</tr>
<tr>
<td>0b10</td>
<td>Match instructions that store to a watchpointed address.</td>
</tr>
<tr>
<td>0b11</td>
<td>Match instructions that load from or store to a watchpointed address.</td>
</tr>
</tbody>
</table>

All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**PAC, bits [2:1]**

Privilege of access control. Determines the Exception level or levels at which a Watchpoint debug event for watchpoint n is generated.

The fields that indicate when the watchpoint can be generated are: HMC, SSC, and PAC. These fields must be considered in combination, and the values that are permitted for these fields are constrained.

For more information on the operation of these fields, see ‘Execution conditions for which a watchpoint generates Watchpoint exceptions’.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**E, bit [0]**

Enable watchpoint n. Possible values are:

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGWCR<n>_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, DBGWCR<n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>b0000</td>
<td>b0000</td>
<td>n[3:0]</td>
<td>b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.DBGWCRn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    return DBGWCR_EL1[UInt(CRm<3:0>)];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    return DBGWCR_EL1[UInt(CRm<3:0>)];
  endif
elsif PSTATE.EL == EL3 then
  if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    return DBGWCR_EL1[UInt(CRm<3:0>)];
  endif
endif

MSR DBGWCR<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.DBGWTR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
      if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
      else
        DBGWCR_EL1[UInt(CRm<3:0>)] = X[t];
      endif
    endif
  else
    DBGWCR_EL1[UInt(CRm<3:0>)] = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
      if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
      else
        DBGWCR_EL1[UInt(CRm<3:0>)] = X[t];
      endif
    endif
  else
    DBGWCR_EL1[UInt(CRm<3:0>)] = X[t];
  endif
elsif PSTATE.EL == EL3 then
  if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGWCR_EL1[UInt(CRm<3:0>)] = X[t];
  endif
The DBGWVR<n>_EL1 characteristics are:

**Purpose**

Holds a data address value for use in watchpoint matching. Forms watchpoint n together with control register DBGWCR<n>_EL1.

**Configuration**

AArch64 System register DBGWVR<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGWVR<n>[31:0].

AArch64 System register DBGWVR<n>_EL1 bits [63:0] are architecturally mapped to External register DBGWVR<n>_EL1[63:0].

If watchpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGWVR<n>_EL1 is a 64-bit register.

**Field descriptions**

The DBGWVR<n>_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**RESS[14:4], bits [63:53]**

Reserved, Sign extended. Software must set all bits in this field to the same value as the most significant bit of the VA field. If all bits in this field are not the same value as the most significant bit of the VA field, then all of the following apply:

- It is CONstrained UNpredictable whether the PE ignores this field when comparing an address.
- It is IMPLEMENTation DEFINED whether the value read back in each bit of this field is a copy of the most significant bit of the VA field or the value written.

**VA[52:49], bits [52:49]**

When FEAT_LVA is implemented:


On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

**VA[48:2], bits [48:2]**

Bits [48:2] of the address value for comparison.

When FEAT_LVA is implemented, VA[52:49] forms the upper part of the address value. Otherwise, bits [52:49] are part of the RESS field.

Arm deprecates setting \texttt{DBGWVR<n>\_EL1[2]} == 1.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Bits [1:0]**

Reserved, RES0.

**Accessing the DBGWVR<n>_EL1**

Accesses to this register use the following encodings:

\[
\text{MRS} \ \langle X_t \rangle, \ \text{DBGWVR<n>_EL1}
\]

<table>
<thead>
<tr>
<th>\text{op0}</th>
<th>\text{op1}</th>
<th>\text{CRn}</th>
<th>\text{CRm}</th>
<th>\text{op2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>\text{n[3:0]}</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if \text{PSTATE.EL} == \text{EL0} then
    \text{UNDEFINED};
elsif \text{PSTATE.EL} == \text{EL1} then
    if \text{Halted()} \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& boolean \text{IMPLEMENTATION_DEFINED} "EL3 trap priority when SDD == '1'" \&\& \text{MDCR_EL3.TDA} == '1' then
        \text{UNDEFINED};
    elsif \text{EL2Enabled()} \&\& (!\text{HaveEL(EL3)} \&\& \text{SCR_EL3.FGTEn} == '1') \&\& \text{HDFGRTR_EL2.DBGWVRn_EL1} == '1' then
        \text{AArch64.SystemAccessTrap(EL2, 0x18)};
    else
        \text{AArch64.SystemAccessTrap(EL3, 0x18)};
    end if
else
    \text{OSLSR_EL1.OSLK} == '0' \&\& \text{HaltingAllowed()} \&\& \text{EDSCR.TDA} == '1' then
        \text{Halt(DebuHalt\_SoftwareAccess)};
    else
        \text{return DBGWVR_EL1[UInt(CRm<3:0>)];}
endif

elsif \text{PSTATE.EL} == \text{EL2} then
    if \text{Halted()} \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& boolean \text{IMPLEMENTATION_DEFINED} "EL3 trap priority when SDD == '1'" \&\& \text{MDCR_EL3.TDA} == '1' then
        \text{UNDEFINED};
    elsif \text{HaveEL(EL3)} \&\& \text{MDCR_EL3.TDA} == '1' then
        if \text{Halted()} \&\& \text{EDSCR.SDD} == '1' then
            \text{UNDEFINED};
        else
            \text{AArch64.SystemAccessTrap(EL3, 0x18)};
        end if
    else
        \text{OSLSR_EL1.OSLK} == '0' \&\& \text{HaltingAllowed()} \&\& \text{EDSCR.TDA} == '1' then
            \text{Halt(DebuHalt\_SoftwareAccess)};
        else
            \text{return DBGWVR_EL1[UInt(CRm<3:0>)];}
endif

elsif \text{PSTATE.EL} == \text{EL3} then
    if \text{OSLSR_EL1.OSLK} == '0' \&\& \text{HaltingAllowed()} \&\& \text{EDSCR.TDA} == '1' then
        \text{Halt(DebuHalt\_SoftwareAccess)};
    else
        \text{return DBGWVR_EL1[UInt(CRm<3:0>)];}
endif

elsif \text{PSTATE.EL} == \text{EL4} then
    if \text{OSLSR_EL1.OSLK} == '0' \&\& \text{HaltingAllowed()} \&\& \text{EDSCR.TDA} == '1' then
        \text{Halt(DebuHalt\_SoftwareAccess)};
    else
        \text{return DBGWVR_EL1[UInt(CRm<3:0>)];}
endif
### MSR DBGWVR<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2(DBGWVRn_EL1 == '1
    then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGWVR_EL1[UInt(CRm<3:0>)] = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGWVR_EL1[UInt(CRm<3:0>)] = X[t];
elsif PSTATE.EL == EL3 then
  if OSLSR_EL1.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGWVR_EL1[UInt(CRm<3:0>)] = X[t];
DC CGDSW, Clean of Data and Allocation Tags by Set/Way

The DC CGDSW characteristics are:

**Purpose**

Clean data and Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC CGDSW are UNDEFINED.

**Attributes**

DC CGDSW is a 64-bit System instruction.

**Field descriptions**

The DC CGDSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Bit Assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
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<td>34</td>
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<td>33</td>
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<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:
- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = Log2(ASSOCIATIVITY), L = Log2(LINELEN), B = (L + S), S = Log2(NSETS).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CGDSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

DC CGDSW, \(<X_t>\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGDSW(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_CGDSW(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CGDSW(X[t]);
The DC CGDVAC characteristics are:

**Purpose**

Clean data and Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC CGDVAC are UNDEFINED.

**Attributes**

DC CGDVAC is a 64-bit System instruction.

**Field descriptions**

The DC CGDVAC input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Virtual address to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGDVAC instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in ‘Permission fault’.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see ‘The data cache maintenance instruction (DC)’.

Accesses to this instruction use the following encodings:

DC CGDVAC, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end;
else
    EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
        HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGDVAC(X[t]);
    end;
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
        HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGDVAC(X[t]);
    end;
elseif PSTATE.EL == EL2 then
    DC_CGDVAC(X[t]);
elseif PSTATE.EL == EL3 then
    DC_CGDVAC(X[t]);
DC CGDVADP, Clean of Data and Allocation Tags by VA to PoDP

The DC CGDVADP characteristics are:

**Purpose**

Clean Allocation Tags and data in data cache by address to Point of Deep Persistence.

If the memory system does not identify a Point of Deep Persistence, then this instruction behaves as a **DC CGDVAP**.

**Configuration**

This instruction is present only when FEAT_DPB2 is implemented and FEAT_MTE is implemented. Otherwise, direct accesses to DC CGDVADP are **UNDEFINED**.

**Attributes**

DC CGDVADP is a 64-bit System instruction.

**Field descriptions**

The DC CGDVADP input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Virtual address to use</th>
<th>Virtual address to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td></td>
<td></td>
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<td>62</td>
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<td>32</td>
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</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGDVADP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

DC CGDVADP, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGDVADP(X[t]);
  endif
else
  DC_CGDVADP(X[t]);
endif

if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGDVADP(X[t]);
  endif
else
  DC_CGDVADP(X[t]);
endif

if PSTATE.EL == EL2 then
  DC_CGDVADP(X[t]);
else
  DC_CGDVADP(X[t]);
endif

if PSTATE.EL == EL3 then
  DC_CGDVADP(X[t]);
else
  DC_CGDVADP(X[t]);
endif
**DC CGDVAP, Clean of Data and Allocation Tags by VA to PoP**

The DC CGDVAP characteristics are:

**Purpose**

Clean data and Allocation Tags in data cache by address to Point of Persistence.

If the memory system does not identify a Point of Persistence, then this instruction behaves as a `DC CGDVAC`.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC CGDVAP are UNDEFINED.

**Attributes**

DC CGDVAP is a 64-bit System instruction.

**Field descriptions**

The DC CGDVAP input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>59</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>31</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGDVAP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  end if
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGDVAP(X[t]);
  end if
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGDVAP(X[t]);
  end if
elsif PSTATE.EL == EL2 then
  DC_CGDVAP(X[t]);
elsif PSTATE.EL == EL3 then
  DC_CGDVAP(X[t]);
DC CGSW, Clean of Allocation Tags by Set/Way

The DC CGSW characteristics are:

**Purpose**

Clean Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC CGSW are UNDEFINED.

**Attributes**

DC CGSW is a 64-bit System instruction.

**Field descriptions**

The DC CGSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
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<td>56</td>
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<td>55</td>
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<td>54</td>
<td></td>
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<tr>
<td>53</td>
<td></td>
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<tr>
<td>52</td>
<td></td>
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<td>51</td>
<td></td>
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<tr>
<td>50</td>
<td></td>
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<tr>
<td>49</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = \(\log_2(\text{ASSOCIATIVITY})\), \(L = \log_2(\text{LINELEN})\), \(B = (L + S)\), \(S = \log_2(\text{NSETS})\).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CGSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is **CONSTRAINED UNPREDICTABLE** and one of the following occurs:

- The instruction is **UNDEFINED**.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

**DC CGSW, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TSW == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGSW(X[t]);
  endif
elsif PSTATE.EL == EL2 then
  DC_CGSW(X[t]);
elsif PSTATE.EL == EL3 then
  DC_CGSW(X[t]);
```

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DC CGVAC, Clean of Allocation Tags by VA to PoC

The DC CGVAC characteristics are:

**Purpose**

Clean Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC CGVAC are UNDEFINED.

**Attributes**

DC CGVAC is a 64-bit System instruction.

**Field descriptions**

The DC CGVAC input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Virtual address to use**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGVAC instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in ‘Permission fault’.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC CGVAC, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') & SCTLR_EL1.UCI == '0' then
        if EL2Enabled() & HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &
        HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGVAC(X[t]);
    endif
elseif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGVAC(X[t]);
    endif
elseif PSTATE.EL == EL2 then
    DC_CGVAC(X[t]);
elseif PSTATE.EL == EL3 then
    DC_CGVAC(X[t]);
DC CGVADP, Clean of Allocation Tags by VA to PoDP

The DC CGVADP characteristics are:

**Purpose**

Clean Allocation tags by address to Point of Deep Persistence.

If the memory system does not identify a Point of Deep Persistence, then this instruction behaves as a DC CGVAP.

**Configuration**

This instruction is present only when FEAT_DPB2 is implemented and FEAT_MTE is implemented. Otherwise, direct accesses to DC CGVADP are UNDEFINED.

**Attributes**

DC CGVADP is a 64-bit System instruction.

**Field descriptions**

The DC CGVADP input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| Virtual address to use | Virtual address to use |

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGVADP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

```
DC CGVADP, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    endif
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGVADP(X[t]);
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CGVADP(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_CGVADP(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CGVADP(X[t]);
DC CGVAP, Clean of Allocation Tags by VA to PoP

The DC CGVAP characteristics are:

**Purpose**

Clean Allocation Tags in data cache by address to Point of Persistence.

If the memory system does not identify a Point of Persistence, then this instruction behaves as a DC CGVAC.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC CGVAP are UNDEFINED.

**Attributes**

DC CGVAP is a 64-bit System instruction.

**Field descriptions**

The DC CGVAP input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | Virtual address to use |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CGVAP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC CGVAP, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGVAP(X[t]);
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CGVAP(X[t]);
  end
elsif PSTATE.EL == EL2 then
  DC_CGVAP(X[t]);
elsif PSTATE.EL == EL3 then
  DC_CGVAP(X[t]);
DC CIGDSW, Clean and Invalidate of Data and Allocation Tags by Set/Way

The DC CIGDSW characteristics are:

**Purpose**

Clean and Invalidate data and Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC CIGDSW are UNDEFINED.

**Attributes**

DC CIGDSW is a 64-bit System instruction.

**Field descriptions**

The DC CIGDSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SetWay, bits [31:4]</strong></td>
<td>Contains two fields:</td>
</tr>
<tr>
<td>• Way, bits[31:32-A], the number of the way to operate on.</td>
<td></td>
</tr>
<tr>
<td>• Set, bits[B-1:L], the number of the set to operate on.</td>
<td></td>
</tr>
<tr>
<td>Bits[L-1:4] are RES0.</td>
<td></td>
</tr>
</tbody>
</table>

A = \(\log_2(\text{ASSOCIATIVITY})\), \(L = \log_2(\text{LINELEN})\), \(B = (L + S)\), \(S = \log_2(\text{NSETS})\).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CIGDSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

DC CIGDSW, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCISW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CIGDSW(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_CIGDSW(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CIGDSW(X[t]);
The DC CIGDVAC characteristics are:

**Purpose**

Clean and Invalidate data and Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC CIGDVAC are UNDEFINED.

**Attributes**

DC CIGDVAC is a 64-bit System instruction.

**Field descriptions**

The DC CIGDVAC input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CIGDVAC instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    endif
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCIVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CIGDVAC(X[t]);
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCIVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CIGDVAC(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_CIGDVAC(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CIGDVAC(X[t]);
DC CIGSW, Clean and Invalidate of Allocation Tags by Set/Way

The DC CIGSW characteristics are:

**Purpose**

Clean and Invalidate Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC CIGSW are UNDEFINED.

**Attributes**

DC CIGSW is a 64-bit System instruction.

**Field descriptions**

The DC CIGSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31-4</td>
<td>SetWay, contains two fields:</td>
</tr>
<tr>
<td></td>
<td>• Way, bits[31:32-A], the number of the way to operate on.</td>
</tr>
<tr>
<td></td>
<td>• Set, bits[B-1:L], the number of the set to operate on.</td>
</tr>
<tr>
<td>3-0</td>
<td>Level, cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = Log2(ASSOCIATIVITY), L = Log2(LINELEN), B = (L + S), S = Log2(NSETS).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CIGSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

\[
\text{DC CIGSW, } \langle X_t \rangle
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TSW == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCISW == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CIGSW(X[t]);
  endif
elsif PSTATE.EL == EL2 then
  DC_CIGSW(X[t]);
elsif PSTATE.EL == EL3 then
  DC_CIGSW(X[t]);
```

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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DC CIGVAC, Clean and Invalidate of Allocation Tags by VA to PoC

The DC CIGVAC characteristics are:

**Purpose**

Clean and Invalidate Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC CIGVAC are UNDEFINED.

**Attributes**

DC CIGVAC is a 64-bit System instruction.

**Field descriptions**

The DC CIGVAC input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---- |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Virtual address to use

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---- |

Virtual address to use

Bits [63:0]

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CIGVAC instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Accesses to this instruction use the following encodings:

DC CIGVAC, <xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCIVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CIGVAC(X[t]);
    end
else if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCIVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CIGVAC(X[t]);
    end
elsif PSTATE.EL == EL2 then
    DC_CIGVAC(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CIGVAC(X[t]);
DC CISW, Data or unified Cache line Clean and Invalidate by Set/Way

The DC CISW characteristics are:

**Purpose**

Clean and Invalidate data cache by set/way.

When FEAT_MTE is implemented, this instruction might clean and invalidate Allocation Tags from caches.

**Configuration**

AArch64 System instruction DC CISW performs the same function as AArch32 System instruction DCCISW.

**Attributes**

DC CISW is a 64-bit System instruction.

**Field descriptions**

The DC CISW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
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<th>Bit</th>
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<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
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<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td></td>
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<tr>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RES0</td>
<td>SetWay</td>
<td>Level</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = \(\text{Log}_2(\text{ASSOCIATIVITY})\), \(L = \text{Log}_2(\text{LINELEN})\), \(B = (L + S)\), \(S = \text{Log}_2(\text{NSETS})\).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CISW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

**DC CISW, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCISW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CISW(X[t]);
    elsif PSTATE.EL == EL2 then
        DC_CISW(X[t]);
elseif PSTATE.EL == EL3 then
    DC_CISW(X[t]);
```

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The DC CIVAC characteristics are:

**Purpose**

Clean and Invalidate data cache by address to Point of Coherency.

When FEAT_MTE is implemented, this instruction might clean and invalidate Allocation Tags from caches.

**Configuration**

AArch64 System instruction DC CIVAC performs the same function as AArch32 System instruction DCCIMVAC.

**Attributes**

DC CIVAC is a 64-bit System instruction.

**Field descriptions**

The DC CIVAC input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:0</td>
<td>Virtual address to use. No alignment restrictions apply to this VA.</td>
</tr>
</tbody>
</table>

**Executing the DC CIVAC instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') & SCTLR_EL1.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &
    HFGITR_EL2.DCCIVAC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & SCTLR_EL2.UCI == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_CIVAC(X[t]);
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.TPCP == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HFGITR_EL2.DCCIVAC == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      DC_CIVAC(X[t]);
  elsif PSTATE.EL == EL2 then
    DC_CIVAC(X[t]);
  elsif PSTATE.EL == EL3 then
    DC_CIVAC(X[t]);
DC CSW, Data or unified Cache line Clean by Set/Way

The DC CSW characteristics are:

**Purpose**

Clean data cache by set/way.

When FEAT_MTE is implemented, this instruction might clean Allocation Tags from caches.

**Configuration**

AArch64 System instruction DC CSW performs the same function as AArch32 System instruction DCCSW.

**Attributes**

DC CSW is a 64-bit System instruction.

**Field descriptions**

The DC CSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>SetWay</td>
</tr>
<tr>
<td>61</td>
<td>Level</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>Reserved</td>
</tr>
<tr>
<td>58</td>
<td>Reserved</td>
</tr>
<tr>
<td>57</td>
<td>Reserved</td>
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<td>56</td>
<td>Reserved</td>
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<td>41</td>
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<td>Reserved</td>
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<td>31</td>
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<td>Reserved</td>
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<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

\[
A = \log_2(\text{ASSOCIATIVITY}), \quad L = \log_2(\text{LINELEN}), \quad B = (L + S), \quad S = \log_2(\text{NSETS}).
\]

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC CSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

DC CSW, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CSW(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_CSW(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CSW(X[t]);
endif
DC CVAC, Data or unified Cache line Clean by VA to PoC

The DC CVAC characteristics are:

**Purpose**

Clean data cache by address to Point of Coherency.

When FEAT_MTE is implemented, this instruction might clean Allocation Tags from caches.

**Configuration**

AArch64 System instruction DC CVAC performs the same function as AArch32 System instruction [DCCMVAC].

**Attributes**

DC CVAC is a 64-bit System instruction.

**Field descriptions**

The DC CVAC input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>Virtual address to use</td>
<td>Virtual address to use. No alignment restrictions apply to this VA.</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CVAC instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CVAC(X[t]);
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CVAC(X[t]);
    end
elsif PSTATE.EL == EL2 then
    DC_CVAC(X[t]);
elsif PSTATE.EL == EL3 then
    DC_CVAC(X[t]);
DC CVADP, Data or unified Cache line Clean by VA to PoDP

The DC CVADP characteristics are:

**Purpose**

Clean data cache by address to Point of Deep Persistence.

If the memory system does not identify a Point of Deep Persistence, then this instruction behaves as a DC CVAP.

When FEAT_MTE is implemented, this instruction might clean Allocation Tags from caches.

**Configuration**

This instruction is present only when FEAT_DPB2 is implemented. Otherwise, direct accesses to DC CVADP are UNDEFINED.

**Attributes**

DC CVADP is a 64-bit System instruction.

**Field descriptions**

The DC CVADP input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Virtual address to use</th>
<th>Virtual address to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>Virtual address to use</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>Virtual address to use</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CVADP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC CVADP, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end if
else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CVADP(X[t]);
    end if
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TPCP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVADP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            DC_CVADP(X[t]);
        end if
    elsif PSTATE.EL == EL2 then
        DC_CVADP(X[t]);
    elsif PSTATE.EL == EL3 then
        DC_CVADP(X[t]);
    end if
end if
The DC CVAP characteristics are:

**Purpose**

Clean data cache by address to Point of Persistence.

If the memory system does not identify a Point of Persistence, then this instruction behaves as a DC CVAC.

When FEAT_MTE is implemented, this instruction might clean Allocation Tags from caches.

**Configuration**

This instruction is present only when FEAT_DPB is implemented. Otherwise, direct accesses to DC CVAP are UNDEFINED.

**Attributes**

DC CVAP is a 64-bit System instruction.

**Field descriptions**

The DC CVAP input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Virtual address to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Executing the DC CVAP instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, see 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC CVAP, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    endif
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CVAP(X[t]);
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TPCP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            DC_CVAP(X[t]);
        endif
    else
        if PSTATE.EL == EL2 then
            DC_CVAP(X[t]);
        else
            if PSTATE.EL == EL3 then
                DC_CVAP(X[t]);
            endif
        endif
    endif
endif
**DC CVAU, Data or unified Cache line Clean by VA to PoU**

The DC CVAU characteristics are:

**Purpose**

Clean data cache by address to Point of Unification.

**Configuration**

AArch64 System instruction DC CVAU performs the same function as AArch32 System instruction DCCMVAU.

**Attributes**

DC CVAU is a 64-bit System instruction.

**Field descriptions**

The DC CVAU input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

Virtual address to use

1. Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC CVAU instruction**

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>DC CVAU, &lt;Xt&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b01</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && HCR_EL2.TOE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TOCU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_CVAU(X[t]);
        if EL2Enabled() && HCR_EL2.TPU == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.TOCU == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAU == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            DC_CVAU(X[t]);
            if EL2Enabled() && HCR_EL2.TPU == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && HCR_EL2.TOCU == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCCVAU == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                DC_CVAU(X[t]);
            end
            if PSTATE.EL == EL2 then
                DC_CVAU(X[t]);
            elsif PSTATE.EL == EL3 then
                DC_CVAU(X[t]);
The DC GVA characteristics are:

**Purpose**

Write a value to the Allocation Tags of a naturally aligned block of N bytes, where the size of N is identified in DCZID_EL0. The Allocation Tag used is determined by the input address.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC GVA are UNDEFINED.

**Attributes**

DC GVA is a 64-bit System instruction.

**Field descriptions**

The DC GVA input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:0]**

Virtual address to use. There is no alignment restriction on the address within the block of N bytes that is used.

**Executing the DC GVA instruction**

When this instruction is executed, it can generate memory faults or watchpoints which are prioritized in the same way as other memory-related faults or watchpoints. If a synchronous data abort fault or a watchpoint is generated, the CM bit in the ESR_ELx.ISS field is not set.

If the memory region being modified is any type of Device memory, this instruction can give an alignment fault that is prioritized in the same way as other alignment faults that are determined by the memory type.

This instruction applies to Normal memory regardless of cacheability attributes.

This instruction behaves as a set of stores to each Allocation Tag within the block being accessed, and so it:

- Generates a Permission Fault if the translation system does not permit writes to the locations.
- Requires the same considerations for ordering and the management of coherency as any other store instructions.

Accesses to this instruction use the following encodings:

**DC GVA, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() & HCR_EL2.<E2H,TGE> == '11') & SCTLR_EL1.DZE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end if
elsif EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & HCR_EL2.TDZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() & HCR_EL2.<E2H,TGE> == '11' & (HaveEL(EL3) || SCR_EL3.FGTEn == '1') &
    HFGITR_EL2.DCZVA == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    DC_GVA(X[t]);
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.TDZ == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & (HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HFGITR_EL2.DCZVA == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_GVA(X[t]);
    end if
elsif PSTATE.EL == EL2 then
    DC_GVA(X[t]);
elsif PSTATE.EL == EL3 then
    DC_GVA(X[t]);
DC GZVA, Data Cache set Allocation Tags and Zero by VA

The DC GZVA characteristics are:

**Purpose**

Zero data and write a value to the Allocation Tags of a naturally aligned block of N bytes, where the size of N is identified in DCZID_EL0. The Allocation Tag used is determined by the input address.

**Configuration**

This instruction is present only when FEAT_MTE is implemented. Otherwise, direct accesses to DC GZVA are UNDEFINED.

**Attributes**

DC GZVA is a 64-bit System instruction.

**Field descriptions**

The DC GZVA input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

Virtual address to use

Virtual address to use

**Bits [63:0]**

Virtual address to use. There is no alignment restriction on the address within the block of N bytes that is used.

**Executing the DC GZVA instruction**

When this instruction is executed, it can generate memory faults or watchpoints which are prioritized in the same way as other memory-related faults or watchpoints. If a synchronous data abort fault or a watchpoint is generated, the CM bit in the ESR_ELx.ISS field is not set.

If the memory region being zeroed is any type of Device memory, this instruction can give an alignment fault which is prioritized in the same way as other alignment faults that are determined by the memory type.

This instruction applies to Normal memory regardless of cacheability attributes.

This instruction behaves as a set of Stores to each byte and Allocation tag within the block being accessed, and so it:

- Generates a Permission Fault if the translation system does not permit writes to the locations.
- Requires the same considerations for ordering and the management of coherency as any other store instructions.

Accesses to this instruction use the following encodings:

**DC GZVA, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.DZE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TDZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCZVA == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.DZE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_GZVA(X[t]);
else if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TDZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCZVA == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DC_GZVA(X[t]);
elsif PSTATE.EL == EL2 then
  DC_GZVA(X[t]);
elsif PSTATE.EL == EL3 then
  DC_GZVA(X[t]);
The DC IGDSW characteristics are:

**Purpose**

Invalidate data and Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC IGDSW are UNDEFINED.

**Attributes**

DC IGDSW is a 64-bit System instruction.

**Field descriptions**

The DC IGDSW input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SetWay | Level | RES0 |

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = Log2(ASSOCIATIVITY), L = Log2(LINELEN), B = (L + S), S = Log2(NSETS).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC IGDSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

DC IGDSW, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b110</td>
</tr>
</tbody>
</table>

```java
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCISW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.SWIO == '1' then
        DC_CIGDSW(X[t]);
    elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
        DC_CIGDSW(X[t]);
    else
        DC_IGDSW(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_IGDSW(X[t]);
elsif PSTATE.EL == EL3 then
    DC_IGDSW(X[t]);
```

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DC IGDVAC, Invalidate of Data and Allocation Tags by VA to PoC

The DC IGDVAC characteristics are:

**Purpose**

Invalidate data and Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC IGDVAC are UNDEFINED.

**Attributes**

DC IGDVAC is a 64-bit System instruction.

**Field descriptions**

The DC IGDVAC input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC IGDVAC instruction**

When the instruction is executed, it can generate a watchpoint, which is prioritized in the same way as other watchpoints. If a watchpoint is generated, the CM bit in the ESR_ELx.ISS field is set to 1.

This instruction requires write access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC IGDVAC, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.TPCP == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCIVAC == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
      DC_CIGDVAC(X[t]);
   else
      DC_INVDVAC(X[t]);
   end if;
elsif PSTATE.EL == EL2 then
   DC_CIGDVAC(X[t]);
elsif PSTATE.EL == EL3 then
   DC_CIGDVAC(X[t]);
DC IGSW, Invalidate of Allocation Tags by Set/Way

The DC IGSW characteristics are:

**Purpose**

Invalidate Allocation Tags in data cache by set/way.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC IGSW are UNDEFINED.

**Attributes**

DC IGSW is a 64-bit System instruction.

**Field descriptions**

The DC IGSW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Field 1</th>
<th>Field 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>62–4</td>
<td>SetWay</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>Reserved, RES0.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30–1</td>
<td>Level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

\[
A = \log_2(\text{ASSOCIATIVITY}), \quad L = \log_2(\text{LINELEN}), \quad B = (L + S), \quad S = \log_2(\text{NSETS}).
\]

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC IGSW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is **CONSTRAINED UNPREDICTABLE** and one of the following occurs:

- The instruction is **UNDEFINED**.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

DC IGSW, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TSW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCISW == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.SWIO == '1' then
        DC_CIGSW(X[t]);
    elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
        DC_CIGSW(X[t]);
    else
        DC_IGSW(X[t]);
    endif
else
    DC_IGSW(X[t]);
endif
```

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DC IGVAC, Invalidate of Allocation Tags by VA to PoC

The DC IGVAC characteristics are:

**Purpose**

Invalidate Allocation Tags in data cache by address to Point of Coherency.

**Configuration**

This instruction is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to DC IGVAC are UNDEFINED.

**Attributes**

DC IGVAC is a 64-bit System instruction.

**Field descriptions**

The DC IGVAC input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Virtual address to use

Virtual address to use

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC IGVAC instruction**

When the instruction is executed, it can generate a watchdog point, which is prioritized in the same way as other watchdog points. If a watchdog point is generated, the CM bit in the ESR_ELx.ISS field is set to 1.

This instruction requires write access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

DC IGVAC, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b011</td>
</tr>
</tbody>
</table>

Page 410
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCIVAC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
        DC_CIGVAC(X[t]);
    else
        DC_IGVAC(X[t]);
    end if
else
    DC_IGVAC(X[t]);
elsif PSTATE.EL == EL2 then
    DC_IGVAC(X[t]);
elsif PSTATE.EL == EL3 then
    DC_IGVAC(X[t]);
The DC ISW characteristics are:

**Purpose**

Invalidate data cache by set/way.

When FEAT_MTE is implemented, this instruction might invalidate Allocation Tags from caches. When it invalidates Allocation Tags from caches, it also cleans them.

**Configuration**

AArch64 System instruction DC ISW performs the same function as AArch32 System instruction DCISW.

**Attributes**

DC ISW is a 64-bit System instruction.

**Field descriptions**

The DC ISW input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:32]**

Reserved, RES0.

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

\[ A = \log_2(\text{ASSOCIATIVITY}), \quad L = \log_2(\text{LINELEN}), \quad B = (L + S), \quad S = \log_2(\text{NSETS}). \]

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.
Executing the DC ISW instruction

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED.
- The instruction performs cache maintenance on one of:
  - No cache lines.
  - A single arbitrary cache line.
  - Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

**DC ISW, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TSW == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCISW == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.SWIO == '1' then
    DC_CISW(X[t]);
  elseif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
    DC_CISW(X[t]);
  else
    DC_ISW(X[t]);
  endif;
elseif PSTATE.EL == EL2 then
  DC_ISW(X[t]);
elseif PSTATE.EL == EL3 then
  DC_ISW(X[t]);
endif;
```

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DC IVAC, Data or unified Cache line Invalidate by VA to PoC

The DC IVAC characteristics are:

**Purpose**

Invalidate data cache by address to Point of Coherency.

When FEAT_MTE is implemented, this instruction might invalidate Allocation Tags from caches. When it invalidates Allocation Tags from caches, it also cleans them.

**Configuration**

AArch64 System instruction DC IVAC performs the same function as AArch32 System instruction DCIMVAC.

**Attributes**

DC IVAC is a 64-bit System instruction.

**Field descriptions**

The DC IVAC input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>31</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DC IVAC instruction**

When the instruction is executed, it can generate a watchpoint, which is prioritized in the same way as other watchpoints. If a watchpoint is generated, the CM bit in the ESR_ELx.ISS field is set to 1.

This instruction requires write access permission to the VA, otherwise it generates a Permission Fault, subject to the constraints described in 'Permission fault'.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The data cache maintenance instruction (DC)'.

Accesses to this instruction use the following encodings:

**DC IVAC, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TPCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCIVAC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
    DC_CIVAC(X[t]);
  else
    DC_IVAC(X[t]);
elsif PSTATE.EL == EL2 then
  DC_IVAC(X[t]);
elsif PSTATE.EL == EL3 then
  DC_IVAC(X[t]);
DC ZVA, Data Cache Zero by VA

The DC ZVA characteristics are:

**Purpose**

Zero data cache by address. Zeroes a naturally aligned block of N bytes, where the size of N is identified in DCZID_EL0.

**Configuration**

There are no configuration notes.

**Attributes**

DC ZVA is a 64-bit System instruction.

**Field descriptions**

The DC ZVA input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Virtual address to use**

Virtual address to use. There is no alignment restriction on the address within the block of N bytes that is used.

**Executing the DC ZVA instruction**

When this instruction is executed, it can generate memory faults or watchpoints which are prioritized in the same way as other memory-related faults or watchpoints. If a synchronous data abort fault or a watchpoint is generated, the CM bit in the ESR_ELx.ISS field is set to 0.

If the memory region being zeroed is any type of Device memory, this instruction can give an Alignment fault which is prioritized in the same way as other Alignment faults that are determined by the memory type.

This instruction applies to Normal memory regardless of cacheability attributes.

This instruction behaves as a set of Stores to each byte within the block being accessed, and so it:

- Generates a Permission Fault if the translation system does not permit writes to the locations.
- Requires the same considerations for ordering and the management of coherency as any other store instructions.

Accesses to this instruction use the following encodings:

**DC ZVA, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.DZE == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TDZ == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
        HFGITR_EL2.DCZVA == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_ZVA(X[t]);
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TDZ == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DCZVA == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        DC_ZVA(X[t]);
    endif
elsif PSTATE.EL == EL2 then
    DC_ZVA(X[t]);
elsif PSTATE.EL == EL3 then
    DC_ZVA(X[t]);
The DCZID_EL0 characteristics are:

**Purpose**

Indicates the block size that is written with byte values of 0 by the **DC ZVA** (Data Cache Zero by Address) System instruction.

If **FEAT_MTE** is implemented, this register also indicates the granularity at which the **DC GVA** and **DC GZVA** instructions write.

**Configuration**

There are no configuration notes.

**Attributes**

DCZID_EL0 is a 64-bit register.

**Field descriptions**

The DCZID_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>DZP, bit [4]</td>
<td>Data Zero Prohibited. This field indicates whether use of <strong>DC ZVA</strong> instructions is permitted or prohibited.</td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55</td>
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<td>54</td>
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<td>34</td>
<td></td>
<td></td>
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<tr>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:5]**

Reserved, RES0.

**DZP, bit [4]**

Data Zero Prohibited. This field indicates whether use of **DC ZVA** instructions is permitted or prohibited.

If **FEAT_MTE** is implemented, this field also indicates whether use of the **DC GVA** and **DC GZVA** instructions are permitted or prohibited.

<table>
<thead>
<tr>
<th>DZP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instructions are permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instructions are prohibited.</td>
</tr>
</tbody>
</table>

The value read from this field is governed by the access state and the values of the **HCR_EL2.TDZ** and **SCTLR_EL1.DZE** bits.

**BS, bits [3:0]**

Log2 of the block size in words. The maximum size supported is 2KB (value == 9).

**Accessing the DCZID_EL0**

Accesses to this register use the following encodings:
MRS <Xt>, DCZID_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
    HFGTR_EL2.DCZID_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return DCZID_EL0;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGTR_EL2.DCZID_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return DCZID_EL0;
elsif PSTATE.EL == EL2 then
  return DCZID_EL0;
elsif PSTATE.EL == EL3 then
  return DCZID_EL0;
DISR_EL1, Deferred Interrupt Status Register

The DISR_EL1 characteristics are:

**Purpose**

Records that an SError interrupt has been consumed by an ESB instruction.

**Configuration**

AArch64 System register DISR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DISR[31:0]. This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to DISR_EL1 are UNDEFINED.

**Attributes**

DISR_EL1 is a 64-bit register.

**Field descriptions**

The DISR_EL1 bit assignments are:

*When DISR_EL1.IDS == 0:*

<table>
<thead>
<tr>
<th>Bits</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:32]</td>
<td>RES0</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>[31]</td>
<td>A</td>
<td>Set to 1 when an ESB instruction defers an asynchronous SError interrupt. If the implementation does not include any sources of SError interrupt that can be synchronized by an Error Synchronization Barrier, then this bit is RES0. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**A, bit [31]**

Set to 1 when an ESB instruction defers an asynchronous SError interrupt. If the implementation does not include any sources of SError interrupt that can be synchronized by an Error Synchronization Barrier, then this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [30:25]**

Reserved, RES0.

**IDS, bit [24]**

Indicates the deferred SError interrupt type.

<table>
<thead>
<tr>
<th>IDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Deferred error uses architecturally-defined format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**DISR_EL1, Deferred Interrupt Status Register**

**Bits [23:13]**

Reserved, RES0.

**AET, bits [12:10]**

Asynchronous Error Type. See the description of ESR_ELx.AET for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EA, bit [9]**

External abort Type. See the description of ESR_ELx.EA for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [8:6]**

Reserved, RES0.

**DFSC, bits [5:0]**

Fault Status Code. See the description of ESR_ELx.DFSC for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**When DISR_EL1.IDS == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>57</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>45</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>43</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0.</td>
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<tr>
<td>9</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**IDS, bit [24]**

Indicates the deferred SError interrupt type.

<table>
<thead>
<tr>
<th>IDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Deferred error uses IMPLEMENTATION DEFINED format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ISS, bits [23:0]**

IMPLEMENTATION DEFINED syndrome. See the description of ESR_ELx[23:0] for an SError interrupt.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the DISR_EL1

An indirect write to DISR_EL1 made by an ESB instruction does not require an explicit synchronization operation for the value that is written to be observed by a direct read of DISR_EL1 occurring in program order after the ESB instruction.

DISR_EL1 is RAZ/WI if EL3 is implemented, the PE is in Non-debug state, `SCR_EL3.EA == 1`, and any of the following apply:

- At EL2.
- At EL1 and \((\text{SCR_EL3.NS} == 0 \&\& \text{SCR_EL3.EEL2} == 0) \lor \text{HCR_EL2.AMO} == 0\).

Accesses to this register use the following encodings:

**MRS <Xt>, DISR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() \&\& HCR_EL2.AMO == '1' then
      return VDISR_EL2;
   else
      return DISR_EL1;
else if PSTATE.EL == EL2 then
   return DISR_EL1;
elsif PSTATE.EL == EL3 then
   return DISR_EL1;

**MSR DISR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() \&\& HCR_EL2.AMO == '1' then
      VDISR_EL2 = X[t];
   else
      DISR_EL1 = X[t];
else if PSTATE.EL == EL2 then
   DISR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
   DISR_EL1 = X[t];
The DIT characteristics are:

**Purpose**

Allows access to the Data Independent Timing bit.

**Configuration**

This register is present only when FEAT_DIT is implemented. Otherwise, direct accesses to DIT are **UNDEFINED**.

**Attributes**

DIT is a 64-bit register.

**Field descriptions**

The DIT bit assignments are:

```
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 63| 62| 61| 60| 59| 58| 57| 56| 55| 54| 53| 52| 51| 50| 49| 48| 47| 46| 45| 44| 43| 42| 41| 40| 39| 38| 37| 36| 35| 34| 33| 32|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RES0|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RES0|
| 31| 30| 29| 28| 27| 26| 25| 24| 23| 22| 21| 20| 19| 18| 17| 16| 15| 14| 13| 12| 11| 10|  9|  8|  7|  6|  5|  4|  3|  2|  1|  0|
```

**Bits [63:25]**

Reserved, RES0.

**DIT, bit [24]**

Data Independent Timing.

<table>
<thead>
<tr>
<th>DIT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The architecture makes no statement about the timing properties of any instructions.</td>
</tr>
<tr>
<td>1</td>
<td>The architecture requires that:</td>
</tr>
<tr>
<td></td>
<td>• The timing of every load and store instruction is insensitive to the value of the data being loaded or stored.</td>
</tr>
<tr>
<td></td>
<td>• For certain data processing instructions, the instruction takes a time which is independent of:</td>
</tr>
<tr>
<td></td>
<td>◦ The values of the data supplied in any of its registers.</td>
</tr>
<tr>
<td></td>
<td>◦ The values of the NZCV flags.</td>
</tr>
<tr>
<td></td>
<td>• For certain data processing instructions, the response of the instruction to asynchronous exceptions does not vary based on:</td>
</tr>
<tr>
<td></td>
<td>◦ The values of the data supplied in any of its registers.</td>
</tr>
<tr>
<td></td>
<td>◦ The values of the NZCV flags.</td>
</tr>
</tbody>
</table>

The data processing instructions affected by this bit are:

- All cryptographic instructions. These instructions are:
  - AESD, AESE, AESIMC, AESMC, SHA1C, SHA1H, SHA1M, SHA1P, SHA1SU0, SHA1SU1, SHA256H, SHA256H2, SHA256SU0, SHA256SU1, SHA512H, SHA512H2, SHA512SU0, SHA512SU1, EOR3, RAX1, XAR, BCAx, SM3S1, SM3TT1A, SM3TT1B, SM3TT2A, SM3TT2B, SM3PARTW1, SM3PARTW2, SM4E, and SM4EKEY.
A subset of those instructions which use the general-purpose register file. These instructions are:

- ADC, ADCS, ADD, ADDS, AND, ANDS, ASR, ASRV, BFC, BFI, BFMI, BFXL, BIC, BICS, CCMN, CCMP, CFINV, CINC, CINV, CLS, CLZ, CMN, CMP, CNEG, CSEL, CSBT, CSETM, CSINC, CSINV, CSENE, EON, EOR, EXTR, LSL, LSLV, LSR, LSRR, MAD, MNEG, MOV, MOVK, MOVN, MOVZ, MSUB, MUL, MVN, NEG, NEQ, NG, NGC, NGE, NSC, NOP, OR, ORR, RBIT, RET, REV, REV16, REV32, REV64, RMIF, ROR, RORV, SBC, SBCS, SBFZ, SBFI, SBFX, SETF8, SETF16, SOMADDL, SMNEG, SMSUBL, SMULH, SMULL, SUB, SUBS, SXTB, SXTX, TST, UBZ, UBFM, UBFX, UMADDL, UMNGL, UMSUBL, UMULH, UMULL, UXTH.

A subset of those instructions which use the SIMD&FP register file. These instructions are:

- ABS, ADD, ADDHN, ADDHN2, ADDP, ADDV, AND, BIC, BIF, BIT, BSL, CLS, CLZ, CMEQ, CMGE, CMGT, CMHI, CMNS, CMLE, CLMT, CMTST, CNT, CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, CRC32CX, DUP, EOR, EXT, FCEL, INS, MLA, MLS, MOV, MOVI, MUL, MVN, MVI, NEG, NOT, ORN, ORR, PMUL, PMULL, PMULL2, RADDHN, RADDHN2, RBIT, REV16, REV32, RSHRN, RSHRN2, RSUBHN, RSUBHNN, SABA, SABD, SABAL, SABAL2, SABDL, SADLP, SADDLP, ADDDL2, SADDL2, SADDLP, SADML2, SADML2, SADML2, SADML2, SHRN, SHRN2, SHSUB, SLI, SMAX, SMAXP, SMAXX, SMIN, SMINP, SMOV, SMLA, SMLA2, SMLAL2, SMLSL, SMLSL2, SMV, SMULL, SMULL2, SRI, SSSH, SHLL, SHLL2, SHRN, SHRN2, SMV, SMLA, SMLA2, SMLSL, SMLSL2, SMV, SMULL, SMLA, SMLA2, SMLSL, SMLSL2, SMV, SMULL, SMULL2, SRI, SSSH, SHLL, SHLL2, SHRN, SHRN2, SSSH, SSSH, SSSH, SSSH.

### Note

The architecture makes no statement about the timing properties when the PSTATE.DIT bit is not set. However, it is likely that many of these instructions have timing that is invariant of the data in many situations.

In particular, Arm strongly recommends that the Armv8.3 pointer authentication instructions do not have their timing dependent on the key value used in the pointer authentication in all cases, regardless of the PSTATE.DIT bit.

On a Warm reset, this field resets to 0.

**Bits [23:0]**

Reserved, RES0.

### Accessing the DIT

Accesses to this register use the following encodings:

**MRS <Xt>, DIT**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    return Zeros(39):PSTATE.DIT:Zeros(24);
elseif PSTATE.EL == EL1 then
    return Zeros(39):PSTATE.DIT:Zeros(24);
elseif PSTATE.EL == EL2 then
    return Zeros(39):PSTATE.DIT:Zeros(24);
elseif PSTATE.EL == EL3 then
    return Zeros(39):PSTATE.DIT:Zeros(24);

**MSR DIT, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

Page 424
if PSTATE.EL == EL0 then
    PSTATE.DIT = X[t]<24>;
elsif PSTATE.EL == EL1 then
    PSTATE.DIT = X[t]<24>;
elsif PSTATE.EL == EL2 then
    PSTATE.DIT = X[t]<24>;
elsif PSTATE.EL == EL3 then
    PSTATE.DIT = X[t]<24>;

MSR DIT, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82a9e71047211

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DLR_EL0, Debug Link Register

The DLR_EL0 characteristics are:

**Purpose**

In Debug state, holds the address to restart from.

**Configuration**

AArch64 System register DLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register DLR[31:0].

**Attributes**

DLR_EL0 is a 64-bit register.

**Field descriptions**

The DLR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Restart address</td>
</tr>
<tr>
<td>62</td>
<td>Restart address</td>
</tr>
<tr>
<td>31</td>
<td>Restart address</td>
</tr>
<tr>
<td>30</td>
<td>Restart address</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Restart address.

**Accessing the DLR_EL0**

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{DLR} \_\text{EL0}
\]

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

if !Halted() then

UNDEFINED;

else

return DLR_EL0;

\[
\text{MSR} \ \text{DLR} \_\text{EL0}, \ <Xt>
\]

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

if !Halted() then

UNDEFINED;

else

DLR_EL0 = X[t];
```
DSPSR_EL0, Debug Saved Program Status Register

The DSPSR_EL0 characteristics are:

**Purpose**

Holds the saved process state for Debug state. On entering Debug state, PSTATE information is written to this register. On exiting Debug state, values are copied from this register to PSTATE.

**Configuration**

AArch64 System register DSPSR_EL0 bits [31:0] are architecturally mapped to AArch32 System register DSPSR[31:0].

**Attributes**

DSPSR_EL0 is a 64-bit register.

**Field descriptions**

The DSPSR_EL0 bit assignments are:

When AArch32 is supported at any Exception level and exiting Debug state to AArch32 state:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31</td>
<td>N, bit [31]</td>
</tr>
<tr>
<td>30</td>
<td>Negative Condition flag. Copied to PSTATE.N on exiting Debug state.</td>
</tr>
<tr>
<td>29</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>28</td>
<td>Z, bit [30]</td>
</tr>
<tr>
<td>27</td>
<td>Zero Condition flag. Copied to PSTATE.Z on exiting Debug state.</td>
</tr>
<tr>
<td>26</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>25</td>
<td>C, bit [29]</td>
</tr>
<tr>
<td>24</td>
<td>Carry Condition flag. Copied to PSTATE.C on exiting Debug state.</td>
</tr>
<tr>
<td>23</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>22</td>
<td>V, bit [28]</td>
</tr>
<tr>
<td>21</td>
<td>Overflow Condition flag. Copied to PSTATE.V on exiting Debug state.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Q, bit [27]**

Overflow or saturation flag. Copied to PSTATE.Q on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Copied to PSTATE.IT[1:0] on exiting Debug state.

On exiting Debug state DSPSR_EL0.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DIT, bit [24]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Copied to PSTATE.DIT on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Copied to PSTATE.SSBS on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Copied to PSTATE.PAN on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**SS, bit [21]**

Software Step. Copied to PSTATE.SS on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
IL, bit [20]

Illegal Execution state. Copied to PSTATE.IL on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

GE, bits [19:16]

Greater than or Equal flags. Copied to PSTATE.GE on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

IT[7:2], bits [15:10]

If-Then. Copied to PSTATE.IT[7:2] on exiting Debug state.

DSPSR_EL0.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

E, bit [9]

Endianness. Copied to PSTATE.E on exiting Debug state.

If the implementation does not support big-endian operation, DSPSR_EL0.E is **RES0**. If the implementation does not support little-endian operation, DSPSR_EL0.E is **RES1**. On exiting Debug state, if the implementation does not support big-endian operation at the Exception level being returned to, DSPSR_EL0.E is **RES0**, and if the implementation does not support little-endian operation at the Exception level being returned to, DSPSR_EL0.E is **RES1**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

A, bit [8]

SError interrupt mask. Copied to PSTATE.A on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

I, bit [7]

IRQ interrupt mask. Copied to PSTATE.I on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

F, bit [6]

FIQ interrupt mask. Copied to PSTATE.F on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

T, bit [5]

T32 Instruction set state. Copied to PSTATE.T on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

M[4], bit [4]

Execution state. Copied to PSTATE.nRW on exiting Debug state.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>AArch32 execution state.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**M[3:0], bits [3:0]**

AArch32 Mode. Copied to PSTATE.M[3:0] on exiting Debug state.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>User.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b0010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Monitor.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b1111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If DSPSR_EL0.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, exiting Debug state is an illegal return event, as described in 'Illegal return events from AArch64 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When AArch64 is supported at any Exception level and entering or exiting Debug state from or to AArch64 state:**

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>Z</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>C</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>V</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>Other values</td>
<td><strong>RES0</strong></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, **RES0**.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on entering Debug state, and copied to PSTATE.N on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on entering Debug state, and copied to PSTATE.Z on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on entering Debug state, and copied to PSTATE.C on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on entering Debug state, and copied to PSTATE.V on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [27:26]

Reserved, RES0.

TCO, bit [25]

When FEAT_MTE is implemented:

Tag Check Override. Set to the value of PSTATE.TCO on entering Debug state, and copied to PSTATE.TCO on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

DIT, bit [24]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on entering Debug state, and copied to PSTATE.DIT on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

UAO, bit [23]

When FEAT_UAO is implemented:

User Access Override. Set to the value of PSTATE.UAO on entering Debug state, and copied to PSTATE.UAO on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on entering Debug state, and copied to PSTATE.PAN on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

SS, bit [21]

Software Step. Set to the value of PSTATE.SS on entering Debug state, and conditionally copied to PSTATE.SS on exiting Debug state.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on entering Debug state, and copied to PSTATE.IL on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [19:13]**

Reserved, RES0.

**SSBS, bit [12]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on entering Debug state, and copied to PSTATE.SSBS on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**BTYPE, bits [11:10]**

*When FEAT_BTI is implemented:*

Branch Type Indicator. Set to the value of PSTATE.BTYPE on entering Debug state, and copied to PSTATE.BTYPE on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**D, bit [9]**

Debug exception mask. Set to the value of PSTATE.D on entering Debug state, and copied to PSTATE.D on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on entering Debug state, and copied to PSTATE.A on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on entering Debug state, and copied to PSTATE.I on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.


F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on entering Debug state, and copied to PSTATE.F on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.

M[4], bit [4]

Execution state. Set to 0b0, the value of PSTATE.nRW, on entering Debug state from AArch64 state, and copied to PSTATE.nRW on exiting Debug state.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch64 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]

AArch64 Exception level and selected Stack Pointer.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL0t.</td>
</tr>
<tr>
<td>0b0100</td>
<td>EL1t.</td>
</tr>
<tr>
<td>0b0101</td>
<td>EL1h.</td>
</tr>
<tr>
<td>0b1000</td>
<td>EL2t.</td>
</tr>
<tr>
<td>0b1001</td>
<td>EL2h.</td>
</tr>
<tr>
<td>0b1100</td>
<td>EL3t.</td>
</tr>
<tr>
<td>0b1101</td>
<td>EL3h.</td>
</tr>
</tbody>
</table>

Other values are reserved. If DSPSR_EL0.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, exiting Debug state is an illegal return event, as described in 'Illegal return events from AArch64 state'.

The bits in this field are interpreted as follows:

- M[3:2] is set to the value of PSTATE.EL on entering Debug state and copied to PSTATE.EL on exiting Debug state.
- M[1] is unused and is 0 for all non-reserved values.
- M[0] is set to the value of PSTATE.SP on entering Debug state and copied to PSTATE.SP on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

## Accessing the DSPSR_EL0

Accesses to this register use the following encodings:

\[
\text{MRS} \ <\text{Xt}, \ DSPSR\_EL0 > \\
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if !Halted() then
    UNDEFINED;
else
    return DSPSR_EL0;
```
MSR DSPSR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !Halted() then
    UNDEFINED;
else
    DSPSR_EL0 = X[t];
The DVP RCTX characteristics are:

**Purpose**

Data Value Prediction Restriction by Context applies to all Data Value Prediction Resources that predict execution based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, data value prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of prediction structures so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when FEAT_SPECRES is implemented. Otherwise, direct accesses to DVP RCTX are UNDEFINED.

**Attributes**

DVP RCTX is a 64-bit System instruction.

**Field descriptions**

The DVP RCTX input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | GVMID | VMID |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | NS | EL | RES0 | GASID | ASID |

**Bits [63:49]**

Reserved, RES0.

**GVMID, bit [48]**

Execution of this instruction applies to all VMIDs or a specified VMID.
GVMID | Meaning
---|---
0b0 | Applies to specified VMID for an EL0 or EL1 target execution context.
0b1 | Applies to all VMIDs for an EL0 or EL1 target execution context.

For target execution contexts other than EL0 or EL1, this field is RES0.

If the instruction is executed at EL0 or EL1, then this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**VMID, bits [47:32]**

Only applies when bit[48] is 0 and the target execution context is either:

- EL1.
- EL0 when (HCR_EL2.E2H==0 or HCR_EL2.TGE==0).

Otherwise this field is RES0.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==0 or HCR_EL2.TGE==0), this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==1 and HCR_EL2.TGE==1), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**Bits [31:27]**

Reserved, RES0.

**NS, bit [26]**

Security State. Defined values are:

| NS | Meaning
|---|---
| 0b0 | Secure state.
| 0b1 | Non-secure state.

When executed in Non-secure state, the Effective value of NS is 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

| EL | Meaning
|---|---
| 0b00 | EL0.
| 0b01 | EL1.
| 0b10 | EL2.
| 0b11 | EL3.

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**Bits [23:17]**

Reserved, RES0.

**GASID, bit [16]**

Execution of this instruction applies to all ASIDs or a specified ASID.
<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0, this field is RES0.

If the instruction is executed at EL0, this field has an Effective value of 0.

**ASID, bits [15:0]**

Only applies for an EL0 target execution context and when bit[16] is 0.

Otherwise this field is RES0.

When the instruction is executed at EL0, this field is treated as the current ASID.

**Executing the DVP RCTX instruction**

Accesses to this instruction use the following encodings:

DVP RCTX, <Xt>

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b011</td>
<td>0b0111</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>
```

```c
if PSTATE.EL == EL0 then
  if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.EnRCTX == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DVPRCTX == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    DVP_RCTX(X[t]);
  end
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.DVPRCTX == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      DVP_RCTX(X[t]);
    end
  elsif PSTATE.EL == EL2 then
    DVP_RCTX(X[t]);
  elsif PSTATE.EL == EL3 then
    DVP_RCTX(X[t]);
end
```
ELR_EL1, Exception Link Register (EL1)

The ELR_EL1 characteristics are:

**Purpose**

When taking an exception to EL1, holds the address to return to.

**Configuration**

There are no configuration notes.

**Attributes**

ELR_EL1 is a 64-bit register.

**Field descriptions**

The ELR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Return address</td>
</tr>
<tr>
<td>62</td>
<td>Return address</td>
</tr>
<tr>
<td>61</td>
<td>Return address</td>
</tr>
<tr>
<td>60</td>
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<td>15</td>
<td>Return address</td>
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<td>14</td>
<td>Return address</td>
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<td>11</td>
<td>Return address</td>
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<td>10</td>
<td>Return address</td>
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<td>9</td>
<td>Return address</td>
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<td>Return address</td>
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<td>7</td>
<td>Return address</td>
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<td>6</td>
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<td>5</td>
<td>Return address</td>
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<tr>
<td>4</td>
<td>Return address</td>
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<tr>
<td>3</td>
<td>Return address</td>
</tr>
<tr>
<td>2</td>
<td>Return address</td>
</tr>
<tr>
<td>1</td>
<td>Return address</td>
</tr>
<tr>
<td>0</td>
<td>Return address</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Return address.

An exception return from EL1 using AArch64 makes ELR_EL1 become **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ELR_EL1**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL3 using the mnemonic ELR_EL1 or ELR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```markdown
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.%NV2,NV1% == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.%NV2,NV1,NV% == '111' then
    return NVMem[0x230];
  else
    return ELR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ELR_EL2;
  else
    return ELR_EL1;
elsif PSTATE.EL == EL3 then
  return ELR_EL1;

MSR ELR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.%NV2,NV1% == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.%NV2,NV1,NV% == '111' then
    NVMem[0x230] = X[t];
  else
    ELR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    ELR_EL2 = X[t];
  else
    ELR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  ELR_EL1 = X[t];

MRS <Xt>, ELR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.%NV2,NV1% == '101' then
    return NVMem[0x230];
  elsif EL2Enabled() && HCR_EL2.%NV% == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ELR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return ELR_EL1;
  else
    UNDEFINED;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '101' then
        NVMem[0x230] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if EL2Enabled() && HCR_EL2.E2H == '1' then
        ELR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        ELR_EL1 = X[t];
    else
        UNDEFINED;
MRS <Xt>, ELR_EL2

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return ELR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return ELR_EL2;
elsif PSTATE.EL == EL3 then
    return ELR_EL2;
MSR ELR_EL2, <Xt>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        ELR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    ELR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    ELR_EL2 = X[t];
ELR_EL2, Exception Link Register (EL2)

The ELR_EL2 characteristics are:

**Purpose**

When taking an exception to EL2, holds the address to return to.

**Configuration**

AArch64 System register ELR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ELR_hyp[31:0]. This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ELR_EL2 is a 64-bit register.

**Field descriptions**

The ELR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>56</th>
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<th>35</th>
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<th>33</th>
<th>32</th>
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</thead>
<tbody>
<tr>
<td>Return address</td>
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<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Return address.

An exception return from EL2 using AArch64 makes ELR_EL2 become **UNKNOWN**.

When EL2 is in AArch32 Execution state and an exception is taken from EL0, EL1, or EL2 to EL3 and AArch64 execution, the upper 32-bits of ELR_EL2 are either set to 0 or hold the same value that they did before AArch32 execution. Which option is adopted is determined by an implementation, and might vary dynamically within an implementation. Correspondingly software must regard the value as being an **UNKNOWN** choice between the two values.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ELR_EL2**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL2 using the mnemonic ELR_EL2 or ELR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

\[
\text{MRS } \langle Xt \rangle, \text{ ELR_EL2}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    ELR_EL1 = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  ELR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  ELR_EL2 = X[t];
MRS ELR_EL1, <Xt>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    ELR_EL1 = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ELR_EL2;
  else
    return ELR_EL1;
elsif PSTATE.EL == EL3 then
  return ELR_EL1;
MSR ELR_EL1, <Xt>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x230];
  else
    return ELR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ELR_EL2;
  else
    return ELR_EL1;
elsif PSTATE.EL == EL3 then
  return ELR_EL1;
MRS <Xt>, ELR_EL1

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '01' then
    return ELR_EL1;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x230];
  else
    return ELR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ELR_EL2;
  else
    return ELR_EL1;
elsif PSTATE.EL == EL3 then
  return ELR_EL1;
MSR ELR_EL1, <Xt>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x230] = X[t];
    else
        ELR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        ELR_EL2 = X[t];
    else
        ELR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    ELR_EL1 = X[t];
ELR_EL3, Exception Link Register (EL3)

The ELR_EL3 characteristics are:

**Purpose**

When taking an exception to EL3, holds the address to return to.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to ELR_EL3 are **UNDEFINED**.

**Attributes**

ELR_EL3 is a 64-bit register.

**Field descriptions**

The ELR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:0]**

Return address.

An exception return from EL3 using AArch64 makes ELR_EL3 become **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ELR_EL3**

Accesses to this register use the following encodings:

**MRS <Xt>, ELR_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b10</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  UNDEFINED;
elsf PSTATE.EL == EL2 then
  UNDEFINED;
elsf PSTATE.EL == EL3 then
  return ELR_EL3;

**MSR ELR_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    ELR_EL3 = X[t];
The ERRIDR_EL1 characteristics are:

**Purpose**

Defines the highest numbered index of the error records that can be accessed through the Error Record System registers.

**Configuration**

AArch64 System register ERRIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register ERRIDR[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERRIDR_EL1 are UNDEFINED.

**Attributes**

ERRIDR_EL1 is a 64-bit register.

**Field descriptions**

The ERRIDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15</td>
<td>Num, bits [15:0] Highest numbered index of the records that can be accessed through the Error Record System registers plus one. Zero indicates no records can be accessed through the Error Record System registers. Each implemented record is owned by a node. A node might own multiple records.</td>
</tr>
</tbody>
</table>

**Accessing the ERRIDR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ERRIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERRIDR_EL1 == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end
    return ERRIDR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return ERRIDR_EL1;
    end
    return ERRIDR_EL1;
elsif PSTATE.EL == EL3 then
    return ERRIDR_EL1;
ERRSELR_EL1, Error Record Select Register

The ERRSELR_EL1 characteristics are:

**Purpose**

Selects an error record to be accessed through the Error Record System registers.

**Configuration**

AArch64 System register ERRSELR_EL1 bits [31:0] are architecturally mapped to AArch32 System register ERRSELR[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERRSELR_EL1 are UNDEFINED.

If ERRIDR_EL1 indicates that zero error records are implemented, then it is IMPLEMENTATION DEFINED whether ERRSELR_EL1 is UNDEFINED or RES0.

**Attributes**

ERRSELR_EL1 is a 64-bit register.

**Field descriptions**

The ERRSELR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>71-32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31</td>
<td>SEL, bits [15:0]</td>
</tr>
</tbody>
</table>

**SEL, bits [15:0]**

Selects the error record accessed through the ERX registers.

For example, if ERRSELR_EL1.SEL is set to 0x0004, then direct reads and writes of ERXSTATUS_EL1 access ERR4STATUS.

If ERRSELR_EL1.SEL is set to a value greater than or equal to ERRIDR_EL1.NUM, then all of the following apply:

- The value read back from ERRSELR_EL1.SEL is UNKNOWN.
- One of the following occurs:
  - An UNKNOWN error record is selected.
  - The ERX* EL1 registers are RAZ/WI.
  - ERX* EL1 register reads and writes are NOPs.
  - ERX* EL1 register reads and writes are UNDEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ERRSELR_EL1**

Accesses to this register use the following encodings:
MRS \(<Xt>\), ERRSELR_EL1

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b0101 & 0b0011 & 0b001 \\
\hline
\end{array}
\]

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
  && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HGRTR_EL2.ERRSELR_EL1 == '1'
  then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return ERRSELR_EL1;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
  && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return ERRSELR_EL1;
  end if
elsif PSTATE.EL == EL3 then
  return ERRSELR_EL1;
endif

MSR ERRSELR_EL1, \(<Xt>\)

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b0101 & 0b0011 & 0b001 \\
\hline
\end{array}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
then
    UNDEFINED;
elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERRSELR_EL1 == '1'
then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        ERRSELR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
then
    UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
else
    ERRSELR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    ERRSELR_EL1 = X[t];
**ERXADDR_EL1, Selected Error Record Address Register**

The ERXADDR_EL1 characteristics are:

**Purpose**

Accesses \( \text{ERR}<n>\text{ADDR} \) for the error record \(<n>\) selected by \( \text{ERRSELR_EL1}.\text{SEL} \).

**Configuration**

AArch64 System register ERXADDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register \( \text{ERXADDR}[31:0] \).

AArch64 System register ERXADDR_EL1 bits [63:32] are architecturally mapped to AArch32 System register \( \text{ERXADDR2}[31:0] \).

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXADDR_EL1 are UNDEFINED.

**Attributes**

ERXADDR_EL1 is a 64-bit register.

**Field descriptions**

The ERXADDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \text{ERR}&lt;n&gt;\text{ADDR} )</td>
<td>( \text{ERR}&lt;n&gt;\text{ADDR} )</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:0]

ERXADDR_EL1 accesses \( \text{ERR}<n>\text{ADDR} \), where \(<n>\) is the value in \( \text{ERRSELR_EL1}.\text{SEL} \).

**Accessing the ERXADDR_EL1**

If \( \text{ERRIDR_EL1}.\text{NUM} == 0x0000 \) or \( \text{ERRSELR_EL1}.\text{SEL} \) is set to a value greater than or equal to \( \text{ERRIDR_EL1}.\text{NUM} \), then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXADDR_EL1 is RAZ/WI.
- Direct reads and writes of ERXADDR_EL1 are NOPs.
- Direct reads and writes of ERXADDR_EL1 are UNDEFINED.

\( \text{ERR}<n>\text{ADDR} \) describes additional constraints that also apply when \( \text{ERR}<n>\text{ADDR} \) is accessed through ERXADDR_EL1.

Accesses to this register use the following encodings:

**MRS \(<Xt>, \text{ERXADDR_EL1}>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXADDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return ERXADDR_EL1;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return ERXADDR_EL1;
  end if;
elsif PSTATE.EL == EL3 then
  return ERXADDR_EL1;
end if;

MSR ERXADDR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXADDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        ERXADDR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        ERXADDR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    ERXADDR_EL1 = X[t];
ERXCTRL_EL1, Selected Error Record Control Register

The ERXCTRL_EL1 characteristics are:

**Purpose**

Accesses \( \text{ERR}<n>\text{CTRL} \) for the error record \(<n>\) selected by \( \text{ERRSELR_EL1}.\text{SEL} \).

**Configuration**

AArch64 System register ERXCTRL_EL1 bits [31:0] are architecturally mapped to AArch32 System register \( \text{ERXCTRL}[31:0] \).

AArch64 System register ERXCTRL_EL1 bits [63:32] are architecturally mapped to AArch32 System register \( \text{ERXCTRL2}[31:0] \).

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXCTRL_EL1 are UNDEFINED.

**Attributes**

ERXCTRL_EL1 is a 64-bit register.

**Field descriptions**

The ERXCTRL_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>ERR(&lt;n&gt;\text{CTRL})</td>
<td>ERR(&lt;n&gt;\text{CTRL})</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXCTRL_EL1 accesses \( \text{ERR}<n>\text{CTRL} \), where \(<n>\) is the value in \( \text{ERRSELR_EL1}.\text{SEL} \).

**Accessing the ERXCTRL_EL1**

If \( \text{ERRIDR_EL1}.\text{NUM} == 0x0000 \) or \( \text{ERRSELR_EL1}.\text{SEL} \) is set to a value greater than or equal to \( \text{ERRIDR_EL1}.\text{NUM} \), then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXCTRL_EL1 is RAZ/WI.
- Direct reads and writes of ERXCTRL_EL1 are NOPs.
- Direct reads and writes of ERXCTRL_EL1 are UNDEFINED.

If \( \text{ERRSELR_EL1}.\text{SEL} \) is not the index of the first error record owned by a node, then \( \text{ERR}<n>\text{CTRL} \) is not present, meaning reads and writes of ERXCTRL_EL1 are RES0.

Accesses to this register use the following encodings:

\[
\begin{array}{c|c|c|c|c}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b0101 & 0b0100 & 0b001 \\
\end{array}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXCTLR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
else
    return ERXCTLR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
else
    return ERXCTLR_EL1;
elsif PSTATE.EL == EL3 then
    return ERXCTLR_EL1;
end

MSR ERXCTLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXCTLR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            ERXCTLR_EL1 = X[t];
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
            UNDEFINED;
        elsif Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            ERXCTLR_EL1 = X[t];
    elsif PSTATE.EL == EL3 then
        ERXCTLR_EL1 = X[t];
ERXFR_EL1, Selected Error Record Feature Register

The ERXFR_EL1 characteristics are:

**Purpose**

Accesses **ERR<n>FR** for the error record <n> selected by **ERRSELR_EL1.SEL**.

**Configuration**

AArch64 System register ERXFR_EL1 bits [31:0] are architecturally mapped to AArch32 System register **ERXFR[31:0]**.

AArch64 System register ERXFR_EL1 bits [63:32] are architecturally mapped to AArch32 System register **ERXFR2[31:0]**.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXFR_EL1 are **UNDEFINED**.

**Attributes**

ERXFR_EL1 is a 64-bit register.

**Field descriptions**

The ERXFR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ERR<n>FR | ERR<n>FR |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

Bits [63:0]

ERXFR_EL1 accesses **ERR<n>FR**, where <n> is the value in **ERRSELR_EL1.SEL**.

**Accessing the ERXFR_EL1**

If **ERRIDR_EL1.NUM** == 0x0000 or **ERRSELR_EL1.SEL** is set to a value greater than or equal to **ERRIDR_EL1.NUM**, then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXFR_EL1 is RAZ.
- Direct reads of ERXFR_EL1 are NOPs.
- Direct reads of ERXFR_EL1 are **UNDEFINED**.

Accesses to this register use the following encodings:

**MRS <Xt>, ERXFR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXFR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return ERXFR_EL1;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            else
                return ERXFR_EL1;
    elsif PSTATE.EL == EL3 then
        return ERXFR_EL1;
ERXMISC0_EL1, Selected Error Record Miscellaneous Register 0

The ERXMISC0_EL1 characteristics are:

**Purpose**

Accesses `ERR<n>MISC0` for the error record `<n>` selected by `ERRSELR_EL1.SEL`.

**Configuration**

AArch64 System register ERXMISC0_EL1 bits [31:0] are architecturally mapped to AArch32 System register `ERXMISC0[31:0]`.

AArch64 System register ERXMISC0_EL1 bits [63:32] are architecturally mapped to AArch32 System register `ERXMISC1[31:0]`.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC0_EL1 are UNDEFINED.

**Attributes**

ERXMISC0_EL1 is a 64-bit register.

**Field descriptions**

The ERXMISC0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Accesses</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-31</td>
<td><code>ERR&lt;n&gt;MISC0</code></td>
</tr>
<tr>
<td>30-32</td>
<td><code>ERR&lt;n&gt;MISC0</code></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXMISC0_EL1 accesses `ERR<n>MISC0`, where `<n>` is the value in `ERRSELR_EL1.SEL`.

**Accessing the ERXMISC0_EL1**

If `ERRIDR_EL1.NUM == 0x0000` or `ERRSELR_EL1.SEL` set to a value greater than or equal to `ERRIDR_EL1.NUM`, then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXMISC0_EL1 is RAZ/WI.
- Direct reads and writes of ERXMISC0_EL1 are NOPs.
- Direct reads and writes of ERXMISC0_EL1 are UNDEFINED.

`ERR<n>MISC0` describes additional constraints that also apply when `ERR<n>MISC0` is accessed through ERXMISC0_EL1.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS <code>&lt;Xt&gt;</code>, ERXMISC0_EL1</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>op0</code></td>
</tr>
<tr>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXMISCn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  return ERXMISCO_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    return ERXMISCO_EL1;
  return ERXMISCO_EL1;
elsif PSTATE.EL == EL3 then
  return ERXMISCO_EL1;

MSR ERXMISCO_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXMISCn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        ERXMISC0_EL1 = X[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        ERXMISC0_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    ERXMISC0_EL1 = X[t];
else
    if HaveEL(EL3) then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        ERXMISC0_EL1 = X[t];
    endif
else
    ERXMISC0_EL1 = X[t];
endif
**ERXMISC1_EL1, Selected Error Record Miscellaneous Register 1**

The ERXMISC1_EL1 characteristics are:

**Purpose**

Accesses \( \text{ERR}<n}\text{MISC1} \) for the error record \(<n> \) selected by \( \text{ERRSELR_EL1.SEL} \).

**Configuration**

AArch64 System register ERXMISC1_EL1 bits [31:0] are architecturally mapped to AArch32 System register \( \text{ERXMISC2}[31:0] \).

AArch64 System register ERXMISC1_EL1 bits [63:32] are architecturally mapped to AArch32 System register \( \text{ERXMISC3}[31:0] \).

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC1_EL1 are UNDEFINED.

**Attributes**

ERXMISC1_EL1 is a 64-bit register.

**Field descriptions**

The ERXMISC1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
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<th>54</th>
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<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
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<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXMISC1_EL1 accesses \( \text{ERR}<n>\text{MISC1} \), where \(<n>\) is the value in \( \text{ERRSELR_EL1.SEL} \).

**Accessing the ERXMISC1_EL1**

If \( \text{ERRIDR_EL1.NUM} == 0x0000 \) or \( \text{ERRSELR_EL1.SEL} \) is set to a value greater than or equal to \( \text{ERRIDR_EL1.NUM} \), then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXMISC1_EL1 is RAZ/WI.
- Direct reads and writes of ERXMISC1_EL1 are NOPs.
- Direct reads and writes of ERXMISC1_EL1 are UNDEFINED.

**ERR<n>\text{MISC1}** describes additional constraints that also apply when \( \text{ERR<n>\text{MISC1}} \) is accessed through ERXMISC1_EL1.

Accesses to this register use the following encodings:

\[
\begin{array}{c|c|c|c|c}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b11 & 0b000 & 0b0101 & 0b0101 & 0b001 \\
\end{array}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXMISCn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return ERXMISC1_EL1;
    end
elsif PSTATE.EL == EL3 then
    return ERXMISC1_EL1;
end

MSR ERXMISC1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
  priority when SDD == '1'' && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXMISCn_EL1 == '1'
  then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ERXMISC1_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
  priority when SDD == '1'' && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ERXMISC1_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  ERXMISC1_EL1 = X[t];
ERXMISC2_EL1, Selected Error Record Miscellaneous Register 2

The ERXMISC2_EL1 characteristics are:

**Purpose**

Accesses \( \text{ERR}<n>\text{MISC2} \) for the error record \(<n>\) selected by \( \text{ERRSELR_EL1}.\text{SEL} \).

**Configuration**

AArch64 System register ERXMISC2_EL1 bits [31:0] are architecturally mapped to AArch32 System register \( \text{ERXMISC4}\{31:0\} \).

AArch64 System register ERXMISC2_EL1 bits [63:32] are architecturally mapped to AArch32 System register \( \text{ERXMISC5}\{31:0\} \).

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXMISC2_EL1 are UNDEFINED.

**Attributes**

ERXMISC2_EL1 is a 64-bit register.

**Field descriptions**

The ERXMISC2_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | Errn|MISC2|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |

**Bits [63:0]**

ERXMISC2_EL1 accesses \( \text{ERR}<n>\text{MISC2} \), where \(<n>\) is the value in \( \text{ERRSELR_EL1}.\text{SEL} \).

**Accessing the ERXMISC2_EL1**

If \( \text{ERRIDR_EL1}.\text{NUM} == 0x0000 \) or \( \text{ERRSELR_EL1}.\text{SEL} \) is set to a value greater than or equal to \( \text{ERRIDR_EL1}.\text{NUM} \), then one of the following occurs:

- An unknown error record is selected.
- ERXMISC2_EL1 is RAZ/WI.
- Direct reads and writes of ERXMISC2_EL1 are NOPs.
- Direct reads and writes of ERXMISC2_EL1 are UNDEFINED.

\( \text{ERR}<n>\text{MISC2} \) describes additional constraints that also apply when \( \text{ERR}<n>\text{MISC2} \) is accessed through ERXMISC2_EL1.

Accesses to this register use the following encodings:

MRS \(<Xt>, \text{ERXMISC2_EL1}\)

<table>
<thead>
<tr>
<th>( \text{op0} )</th>
<th>( \text{op1} )</th>
<th>( \text{CRn} )</th>
<th>( \text{CRm} )</th>
<th>( \text{op2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif EL2Enabled() && HCR_EL2.TERR == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXMISCn_EL1 == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
else
  AArch64.SystemAccessTrap(EL3, 0x18);
else
  return ERXMISC_E1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch64.SystemAccessTrap(EL3, 0x18);
else
  return ERXMISC_E1;
elsif PSTATE.EL == EL3 then
  return ERXMISC_E1;

MSR ERXMISC_E1, \<Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXMISCn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ERXMISC2_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ERXMISC2_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  ERXMISC2_EL1 = X[t];
The ERXMISC3_EL1 characteristics are:

**Purpose**

Accesses ERR<n>MISC3 for the error record <n> selected by ERRSELR_EL1.SEL.

**Configuration**

AArch64 System register ERXMISC3_EL1 bits [31:0] are architecturally mapped to AArch32 System register ERXMISC6[31:0].

AArch64 System register ERXMISC3_EL1 bits [63:32] are architecturally mapped to AArch32 System register ERXMISC7[31:0].

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXMISC3_EL1 are UNDEFINED.

**Attributes**

ERXMISC3_EL1 is a 64-bit register.

**Field descriptions**

The ERXMISC3_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ERR&lt;n&gt;MISC3</td>
</tr>
<tr>
<td>62</td>
<td>ERR&lt;n&gt;MISC3</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>ERR&lt;n&gt;MISC3</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXMISC3_EL1 accesses ERR<n>MISC3, where <n> is the value in ERRSELR_EL1.SEL.

**Accessing the ERXMISC3_EL1**

If ERRIDR_EL1.NUM == 0x0000 or ERRSELR_EL1.SEL is set to a value greater than or equal to ERRIDR_EL1.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC3_EL1 is RAZ/WI.
- Direct reads and writes of ERXMISC3_EL1 are NOPs.
- Direct reads and writes of ERXMISC3_EL1 are UNDEFINED.

ERR<n>MISC3 describes additional constraints that also apply when ERR<n>MISC3 is accessed through ERXMISC3_EL1.

Accesses to this register use the following encodings:

\[
\begin{array}{c|c|c|c|c}
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
\end{array}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXMISCn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    return ERXMISC3_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
else
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    return ERXMISC3_EL1;
elsif PSTATE.EL == EL3 then
    return ERXMISC3_EL1;

MSR ERXMISC3_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TERR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXMISCn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && SCR_EL3.TERR == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ERXMISC3_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  ERXMISC3_EL1 = X[t];
endif
elsif PSTATE.EL == EL3 then
  ERXMISC3_EL1 = X[t];
ERXPFGCDN_EL1, Selected Pseudo-fault Generation Countdown register

The ERXPFGCDN_EL1 characteristics are:

**Purpose**

Accesses `ERR<n>PFGCDN` for the error record `<n>` selected by `ERRSELR_EL1.SEL`.

**Configuration**

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXPFGCDN_EL1 are UNDEFINED.

**Attributes**

ERXPFGCDN_EL1 is a 64-bit register.

**Field descriptions**

The ERXPFGCDN_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td><code>ERR&lt;n&gt;PFGCDN</code></td>
</tr>
<tr>
<td>62</td>
<td><code>ERR&lt;n&gt;PFGCDN</code></td>
</tr>
<tr>
<td></td>
<td><code>ERR&lt;n&gt;PFGCDN</code></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXPFGCDN_EL1 accesses `ERR<n>PFGCDN`, where `<n>` is the value in `ERRSELR_EL1.SEL`.

**Accessing the ERXPFGCDN_EL1**

If `ERRIDR_EL1.NUM == 0x0000` or `ERRSELR_EL1.SEL` is set to a value greater than or equal to `ERRIDR_EL1.NUM`, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXPFGCDN_EL1 is RAZ/WI.
- Direct reads and writes of ERXPFGCDN_EL1 are NOPs.
- Direct reads and writes of ERXPFGCDN_EL1 are UNDEFINED.

If `ERRSELR_EL1.SEL` selects an error record owned by a node that does not implement the RAS Common Fault Injection Model Extension, then one of the following occurs:

- ERXPFGCDN_EL1 is RAZ/WI.
- Direct reads and writes of ERXPFGCDN_EL1 are NOPs.
- Direct reads and writes of ERXPFGCDN_EL1 are UNDEFINED.

**Note**

A node does not implement the RAS Common Fault Injection Model Extension when `ERR<q>FR.INJ == 0b00`. `<q>` is the index of the first error record owned by the same node as error record `<n>`, where `<n>` is the value in `ERRSELR_EL1.SEL`. If the node owns a single record, then `q = n`.

If `ERRSELR_EL1.SEL` is not the index of the first error record owned by a node, then `ERR<n>PFGCDN` is not present, meaning reads and writes of ERXPFGCDN_EL1 are RES0.
ERR\textsf{PFGCDN} describes additional constraints that also apply when ERR\textsf{PFGCDN} is accessed through ERXPFGCDN\_EL1.

Accesses to this register use the following encodings:

\textbf{MRS} \textit{<Xt>}, ERXPFGCDN\_EL1

<table>
<thead>
<tr>
<th>\textbf{op0}</th>
<th>\textbf{op1}</th>
<th>\textbf{CRn}</th>
<th>\textbf{CRm}</th>
<th>\textbf{op2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b110</td>
</tr>
</tbody>
</table>

\begin{verbatim}
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.FIEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXPFGCDN_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x10);
    else
      return ERXPFGCDN\_EL1;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x10);
      else
        return ERXPFGCDN\_EL1;
    elsif PSTATE.EL == EL3 then
      return ERXPFGCDN\_EL1;

MSR ERXPFGCDN\_EL1, <Xt>

<table>
<thead>
<tr>
<th>\textbf{op0}</th>
<th>\textbf{op1}</th>
<th>\textbf{CRn}</th>
<th>\textbf{CRm}</th>
<th>\textbf{op2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
\end{verbatim}
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.FIEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXPFGCDN_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ERXPFGCDN_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ERXPFGCDN_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    ERXPFGCDN_EL1 = X[t];
The ERXPFGCTL_EL1 characteristics are:

**Purpose**

Accesses \( \text{ERR}<n> \text{PFGCTL} \) for the error record \(<n>\) selected by \( \text{ERRSELR_EL1}.\text{SEL} \).

**Configuration**

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXPFGCTL_EL1 are UNDEFINED.

**Attributes**

ERXPFGCTL_EL1 is a 64-bit register.

**Field descriptions**

The ERXPFGCTL_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Address</th>
<th>Bit Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ERR&lt;n&gt;PFGCTL</td>
</tr>
<tr>
<td>31</td>
<td>ERR&lt;n&gt;PFGCTL</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXPFGCTL_EL1 accesses \( \text{ERR}<n> \text{PFGCTL} \) where \(<n>\) is the value in \( \text{ERRSELR_EL1}.\text{SEL} \).

**Accessing the ERXPFGCTL_EL1**

If \( \text{ERRIDR_EL1}.\text{NUM} == 0x0000 \) or \( \text{ERRSELR_EL1}.\text{SEL} \) is set to a value greater than or equal to \( \text{ERRIDR_EL1}.\text{NUM} \), then one of the following occurs:

- An \text{UNKNOWN} \ error record is selected.
- ERXPFGCTL_EL1 is RAZ/WI.
- Direct reads and writes of ERXPFGCTL_EL1 are NOPs.
- Direct reads and writes of ERXPFGCTL_EL1 are UNDEFINED.

If \( \text{ERRSELR_EL1}.\text{SEL} \) selects an error record owned by a node that does not implement the RAS Common Fault Injection Model Extension, then one of the following occurs:

- ERXPFGCTL_EL1 is RAZ/WI.
- Direct reads and writes of ERXPFGCTL_EL1 are NOPs.
- Direct reads and writes of ERXPFGCTL_EL1 are UNDEFINED.

**Note**

A node does not implement the RAS Common Fault Injection Model Extension when \( \text{ERR}<q>\text{FR.INJ} == 0b00 \). \(<q>\) is the index of the first error record owned by the same node as error record \(<n>\), where \(<n>\) is the value in \( \text{ERRSELR_EL1}.\text{SEL} \). If the node owns a single record, then \(<q> = <n>\).

If \( \text{ERRSELR_EL1}.\text{SEL} \) is not the index of the first error record owned by a node, then \( \text{ERR}<n> \text{PFGCTL} \) is not present, meaning reads and writes of ERXPFGCTL_EL1 are RES0.
ERR<PFGCTL> describes additional constraints that also apply when ERR<PFGCTL> is accessed through ERXPFGCTL_EL1.

Accesses to this register use the following encodings:

MRS <Xt>, ERXPFGCTL_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1l</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

| if PSTATE.EL == EL0 then | UNDEFINED; |
| elsif PSTATE.EL == EL1 then |
| | if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then |
| | UNDEFINED; |
| | elsif EL2Enabled() && HCR_EL2.FIEN == '0' then |
| | AArch64.SystemAccessTrap(EL2, 0x18); |
| | elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXPFGCTL_EL1 == '1' then |
| | AArch64.SystemAccessTrap(EL2, 0x18); |
| | elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then |
| | if Halted() && EDSCR.SDD == '1' then |
| | UNDEFINED; |
| | else |
| | AArch64.SystemAccessTrap(EL3, 0x18); |
| | else |
| | return ERXPFGCTL_EL1; |
| elsif PSTATE.EL == EL2 then |
| if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then |
| UNDEFINED; |
| elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then |
| if Halted() && EDSCR.SDD == '1' then |
| UNDEFINED; |
| else |
| AArch64.SystemAccessTrap(EL3, 0x18); |
| else |
| return ERXPFGCTL_EL1; |
| elsif PSTATE.EL == EL3 then |
| return ERXPFGCTL_EL1; |

MSR ERXPFGCTL_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1l</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
  priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.FIEN == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXPFGCTL_EL1 ==
    '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  else
    ERXPFGCTL_EL1 = X[t];
  end;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
  priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  else
    ERXPFGCTL_EL1 = X[t];
  end;
elsif PSTATE.EL == EL3 then
  ERXPFGCTL_EL1 = X[t];
ERXPFGF_EL1, Selected Pseudo-fault Generation Feature register

The ERXPFGF_EL1 characteristics are:

**Purpose**

Accesses ER<n>PFGF for the error record <n> selected by ERRSELR_EL1.SEL.

**Configuration**

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXPFGF_EL1 are UNDEFINED.

**Attributes**

ERXPFGF_EL1 is a 64-bit register.

**Field descriptions**

The ERXPFGF_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ERR&lt;n&gt;PFGF</td>
</tr>
<tr>
<td>31</td>
<td>ERR&lt;n&gt;PFGF</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXPFGF_EL1 accesses ER<n>PFGF, where <n> is the value in ERRSELR_EL1.SEL.

**Accessing the ERXPFGF_EL1**

If ERRIDR_EL1.NUM == 0x0000 or ERRSELR_EL1.SEL is set to a value greater than or equal to ERRIDR_EL1.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXPFGF_EL1 is RAZ.
- Direct reads of ERXPFGF_EL1 are NOPs.
- Direct reads of ERXPFGF_EL1 are UNDEFINED.

If ERRSELR_EL1.SEL selects an error record owned by a node that does not implement the RAS Common Fault Injection Model Extension, then one of the following occurs:

- ERXPFGF_EL1 is RAZ.
- Direct reads of ERXPFGF_EL1 are NOPs.
- Direct reads of ERXPFGF_EL1 are UNDEFINED.

**Note**

A node does not implement the RAS Common Fault Injection Model Extension when ER<n>FR.INJ == 0b00. <q> is the index of the first error record owned by the same node as error record <n>, where <n> is the value in ERRSELR_EL1.SEL. If the node owns a single record, then q = n.

If ERRSELR_EL1.SEL is not the index of the first error record owned by a node, then ER<n>PFGF is not present, meaning reads of ERXPFGF_EL1 are RES0.
ERR\textsubscript{PFGF} describes additional constraints that also apply when ERR\textsubscript{PFGF} is accessed through ERXPFGF\_EL1.

Accesses to this register use the following encodings:

$$\text{MRS } \langle Xt \rangle, \text{ ERXPFGF\_EL1}$$

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.FIEN == '0' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ERXPFGF_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return ERXPFGF_EL1;
        endif
    else
        AArch64.SystemAccessTrap(EL3, 0x10);
        return ERXPFGF_EL1;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIEN == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FIEN == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x10);
        endif
    else
        AArch64.SystemAccessTrap(EL3, 0x10);
        return ERXPFGF_EL1;
    endif
elsif PSTATE.EL == EL3 then
    return ERXPFGF_EL1;
ERXSTATUS_EL1, Selected Error Record Primary Status Register

The ERXSTATUS_EL1 characteristics are:

**Purpose**

Accesses `ERR<n>STATUS` for the error record `<n>` selected by `ERRSEL_EL1.SEL`.

**Configuration**

AArch64 System register ERXSTATUS_EL1 bits [31:0] are architecturally mapped to AArch32 System register `ERXSTATUS[31:0]`.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXSTATUS_EL1 are **UNDEFINED**.

**Attributes**

ERXSTATUS_EL1 is a 64-bit register.

**Field descriptions**

The ERXSTATUS_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>ERXSTATUS_EL1 Access</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td><code>ERR&lt;n&gt;STATUS</code></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

ERXSTATUS_EL1 accesses `ERR<n>STATUS`, where `<n>` is the value in `ERRSEL_EL1.SEL`.

**Accessing the ERXSTATUS_EL1**

If `ERRIDR_EL1.NUM` == 0x0000 or `ERRSEL_EL1.SEL` is set to a value greater than or equal to `ERRIDR_EL1.NUM`, then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXSTATUS_EL1 is RAZ/WI.
- Direct reads and writes of ERXSTATUS_EL1 are NOPs.
- Direct reads and writes of ERXSTATUS_EL1 are **UNDEFINED**.

`ERR<n>STATUS` describes additional constraints that also apply when `ERR<n>STATUS` is accessed through ERXSTATUS_EL1.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
    return ERXSTATUS_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
    return ERXSTATUS_EL1;
elsif PSTATE.EL == EL3 then
    return ERXSTATUS_EL1;

MSR ERXSTATUS_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TERR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ERXSTATUS_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ERXSTATUS_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ERXSTATUS_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    ERXSTATUS_EL1 = X[t];
ESR_EL1, Exception Syndrome Register (EL1)

The ESR_EL1 characteristics are:

**Purpose**

Holds syndrome information for an exception taken to EL1.

**Configuration**

AArch64 System register ESR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DFSR[31:0].

**Attributes**

ESR_EL1 is a 64-bit register.

**Field descriptions**

The ESR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit allocation</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td></td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
<td></td>
</tr>
<tr>
<td>58</td>
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<tr>
<td>33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ESR_EL1 is made UNKNOWN as a result of an exception return from EL1.

When an UNPREDICTABLE instruction is treated as UNDEFINED, and the exception is taken to EL1, the value of ESR_EL1 is UNKNOWN. The value written to ESR_EL1 must be consistent with a value that could be created as a result of an exception from the same Exception level that generated the exception as a result of a situation that is not UNPREDICTABLE at that Exception level, in order to avoid the possibility of a privilege violation.

**Bits [63:37]**

Reserved, RES0.

**ISS2, bits [36:32]**

When FEAT_LS64 is implemented:

If a memory access generated by an ST64BV or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xs.

For any other Data Abort, this field is RES0.

Otherwise:

Reserved, RES0.

**EC, bits [31:26]**

Exception Class. Indicates the reason for the exception that this register holds information about.

For each EC value, the table references a subsection that gives information about:

- The cause of the exception, for example the configuration required to enable the trap.
- The encoding of the associated ISS.
Possible values of the EC field are:
<table>
<thead>
<tr>
<th>EC</th>
<th>Meaning</th>
<th>ISS encoding for exceptions with an unknown reason</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Unknown reason.</td>
<td>ISS encoding for an exception from a WF* instruction</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Trapped WF* instruction execution. Conditional WF* instructions that fail their condition code check do not cause an exception.</td>
<td>ISS encoding for an exception from a WF* instruction</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Trapped MCR or MRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b000100</td>
<td>Trapped MCRR or MRRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCRR or MRRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b000101</td>
<td>Trapped MCR or MRC access with (coproc==0b1110).</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b000110</td>
<td>Trapped LDC or STC access. The only architected uses of these instruction are:</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>• An STC to write data to memory from DBGDTRRXint.</td>
<td>ISS encoding for an exception from an LDC or STC instruction</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td></td>
<td>• An LDC to read data from memory to DBGDTRRXint.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Access to SVE, Advanced SIMD or floating-point functionality trapped by CPACR_EL1, FPEN, CPTR_EL2, FPEN, CPTR_EL2, TFP, or CPTR_EL3, TFP control. Excludes exceptions resulting from CPACR_EL1 when the value of HCR_EL2.TGE is 1, or because SVE or Advanced SIMD and floating-point are not implemented. These are reported with EC value 0b000000 as described in 'The EC used to report an exception routed to EL2 because HCR_EL2.TGE is 1'.</td>
<td>ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality resulting from the FPEN and TFP traps</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Trapped execution of an LD64B, ST64B,</td>
<td>ISS encoding for an exception</td>
<td>When FEAT_LS64</td>
</tr>
</tbody>
</table>
ST64BV, or ST64BV0 instruction.

0b001100  Trapped MRRC access with (coproc==0b1110). 
ISS encoding for an exception from an MCRR or MRRC access is implemented.

0b001101  Branch Target Exception.
ISS encoding for an exception from Branch Target Identification instruction.

0b001110  Illegal Execution state.
ISS encoding for an exception from an illegal Execution state, or a PC or SP alignment fault.

0b010001  SVC instruction execution in AArch32 state.
This is reported in ESR_EL2 only when the exception is generated because the value of HCR_EL2.TGE is 1.
ISS encoding for an exception from HVC or SVC instruction execution.

0b010101  SVC instruction execution in AArch64 state.
ISS encoding for an exception from HVC or SVC instruction execution.

0b011000  Trapped MSR, MRS or System instruction execution in AArch64 state, that is not reported using EC 0b000000, 0b000001, or 0b000111.
This includes all instructions that cause exceptions that are part of the encoding space defined in 'System instruction class encoding overview', except for those exceptions reported using EC values 0b000000, 0b000001, or 0b000111.
ISS encoding for an exception from MSR, MRS, or System instruction execution in AArch64 state.

0b011001  Access to SVE functionality trapped as a result of CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ, that is not reported using EC 0b000000.
ISS encoding for an exception from an access to SVE functionality resulting from CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ.

0b011100  Exception from a Pointer Authentication instruction authentication failure
ISS encoding for an exception from a Pointer Authentication.

When AArch32 is supported at any Exception level.

When AArch32 is supported at any Exception level.

When AArch32 is supported at any Exception level.

When AArch64 is supported at any Exception level.

When AArch64 is supported at any Exception level.

When FEAT_SVE is implemented.

When FEAT_FPAC is implemented.
<table>
<thead>
<tr>
<th>ISS Encoding</th>
<th>Exception Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b100000</strong></td>
<td>Instruction Abort from a lower Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td><strong>0b100001</strong></td>
<td>Instruction Abort taken without a change in Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td><strong>0b100010</strong></td>
<td>PC alignment fault exception.</td>
</tr>
<tr>
<td><strong>0b100100</strong></td>
<td>Data Abort from a lower Exception level. Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td><strong>0b100101</strong></td>
<td>Data Abort taken without a change in Exception level. Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td><strong>0b100110</strong></td>
<td>SP alignment fault exception.</td>
</tr>
</tbody>
</table>
Trapped floating-point exception taken from AArch32 state. This EC value is valid if the implementation supports trapping of floating-point exceptions, otherwise it is reserved. Whether a floating-point implementation supports trapping of floating-point exceptions is IMPLEMENTATION DEFINED.

Trapped floating-point exception taken from AArch64 state. This EC value is valid if the implementation supports trapping of floating-point exceptions, otherwise it is reserved. Whether a floating-point implementation supports trapping of floating-point exceptions is IMPLEMENTATION DEFINED.

SErrror interrupt.

Breakpoint exception from a lower Exception level.

Breakpoint exception taken without a change in Exception level.

Software Step exception from a lower Exception level.

Software Step exception taken without a change in Exception level.

Watchpoint exception from a lower Exception level.

Watchpoint exception taken without a change in Exception level.

BKPT instruction execution in AArch32 state.

When AArch32 is supported at any Exception level.

When AArch64 is supported at any Exception level.
Exception level 0b111100 BRK instruction execution in AArch64 state. This is reported in ESR_EL3 only if a BRK instruction is executed.

ISS encoding for an exception from execution of a Breakpoint instruction

When AArch64 is supported at any Exception level

All other EC values are reserved by Arm, and:

* Unused values in the range 0b000000 - 0b101100 (0x00 - 0x2C) are reserved for future use for synchronous exceptions.
* Unused values in the range 0b101101 - 0b111111 (0x2D - 0x3F) are reserved for future use, and might be used for synchronous or asynchronous exceptions.

The effect of programming this field to a reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IL, bit [25]

Instruction Length for synchronous exceptions. Possible values of this bit are:

<table>
<thead>
<tr>
<th>IL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>16-bit instruction trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>32-bit instruction trapped. This value is also used when the exception is one of the following:</td>
</tr>
<tr>
<td></td>
<td>• An SError interrupt.</td>
</tr>
<tr>
<td></td>
<td>• An Instruction Abort exception.</td>
</tr>
<tr>
<td></td>
<td>• A PC alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• An SP alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• A Data Abort exception for which the value of the ISV bit is 0.</td>
</tr>
<tr>
<td></td>
<td>• An Illegal Execution state exception.</td>
</tr>
<tr>
<td></td>
<td>• Any debug exception except for Breakpoint instruction exceptions.</td>
</tr>
<tr>
<td></td>
<td>For Breakpoint instruction exceptions, this bit has its standard meaning:</td>
</tr>
<tr>
<td></td>
<td>◦ 0b0: 16-bit T32 BKPT instruction.</td>
</tr>
<tr>
<td></td>
<td>◦ 0b1: 32-bit A32 BKPT instruction or A64 BRK instruction.</td>
</tr>
<tr>
<td></td>
<td>• An exception reported using EC value 0b000000.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS, bits [24:0]

Instruction Specific Syndrome. Architecturally, this field can be defined independently for each defined Exception class. However, in practice, some ISS encodings are used for more than one Exception class.

Typically, an ISS encoding has a number of subfields. When an ISS subfield holds a register number, the value returned in that field is the AArch64 view of the register number.

For an exception taken from AArch32 state, see 'Mapping of the general-purpose registers between the Execution states'.

If the AArch32 register descriptor is 0b1111, then:

* If the instruction that generated the exception was not UNPREDICTABLE, the field takes the value 0b11111.
* If the instruction that generated the exception was UNPREDICTABLE, the field takes an UNKNOWN value that must be either:
  ◦ The AArch64 view of the register number of a register that might have been used at the Exception level from which the exception was taken.
  ◦ The value 0b11111.

When the EC field is 0b000000, indicating an exception with an unknown reason, the ISS field is not valid, RES0.
ISS encoding for exceptions with an unknown reason

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |

Bits [24:0]

Reserved, RES0.

When an exception is reported using this EC code the IL field is set to 1.

This EC code is used for all exceptions that are not covered by any other EC value. This includes exceptions that are generated in the following situations:

- The attempted execution of an instruction bit pattern that has no allocated instruction or that is not accessible at the current Exception level and Security state, including:
  - A read access using a System register pattern that is not allocated for reads or that does not permit reads at the current Exception level and Security state.
  - A write access using a System register pattern that is not allocated for writes or that does not permit writes at the current Exception level and Security state.
  - Instruction encodings that are unallocated.
  - Instruction encodings for instructions or System registers that are not implemented in the implementation.
- In Debug state, the attempted execution of an instruction bit pattern that is not accessible in Debug state.
- In Non-debug state, the attempted execution of an instruction bit pattern that is not accessible in Non-debug state.
- In AArch32 state, attempted execution of a short vector floating-point instruction.
- In an implementation that does not include Advanced SIMD and floating-point functionality, an attempted access to Advanced SIMD or floating-point functionality under conditions where that access would be permitted if that functionality was present. This includes the attempted execution of an Advanced SIMD or floating-point instruction, and attempted accesses to Advanced SIMD and floating-point System registers.
- An exception generated because of the value of one of the SCTLR_EL1. {ITD, SED, CP15BEN} control bits.
- Attempted execution of:
  - An HVC instruction when disabled by HCR_EL2.HCD or SCR_EL3.HCE.
  - An SMC instruction when disabled by SCR_EL3.SMD.
  - An HLT instruction when disabled by EDSCR.HDE.
- Attempted execution of an MSR or MRS instruction to access SP_EL0 when the value of SPSel.SP is 0.
- Attempted execution of an MSR or MRS instruction using a _EL12 register name when HCR_EL2.E2H == 0.
- Attempted execution, in Debug state, of:
  - A DCPS1 instruction when the value of HCR_EL2.TGE is 1 and EL2 is disabled or not implemented in the current Security state.
  - A DCPS2 instruction from EL1 or EL0 when EL2 is disabled or not implemented in the current Security state.
  - A DCPS3 instruction when the value of EDSCR.SDD is 1, or when EL3 is not implemented.
- When EL3 is using AArch64, attempted execution from Secure EL1 of an SRS instruction using R13 mon. See ‘Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32’.
- In Debug state when the value of EDSCR.SDD is 1, the attempted execution at EL2, EL1, or EL0 of an instruction that is configured to trap to EL3.
- In AArch32 state, the attempted execution of an MRS (banked register) or an MSR (banked register) instruction to SPSR_mon, SP_mon, or LR_mon.
- An exception that is taken to EL2 because the value of HCR_EL2.TGE is 1 that, if the value of HCR_EL2.TGE was 0 would have been reported with an ESR_ELx.EC value of 0b000111.

ISS encoding for an exception from a WF* instruction

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |

CV, bit [24]

Condition code valid.
The COND field is not valid.
The COND field is valid.

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:2]**

Reserved, RES0.

**TI, bits [1:0]**

Trapped instruction. Possible values of this bit are:

<table>
<thead>
<tr>
<th>TI</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>WFI trapped.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>WFE trapped.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>WFIT trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
<tr>
<td>0b11</td>
<td>WFET trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
</tbody>
</table>

When FEAT_WFxT is implemented, this is a two bit field as shown. Otherwise, bit[1] is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following fields describe configuration settings for generating this exception:

- **SCTLR_EL1**, {nTWE, nTWI}.
- **HCR_EL2**, {TWE, TWI}.
- **SCR_EL3**, {TWE, TWI}.
ISS encoding for an exception from an MCR or MRC access

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>Opc2</th>
<th>Opc1</th>
<th>CRn</th>
<th>Rt</th>
<th>CRm</th>
<th>Direction</th>
</tr>
</thead>
</table>

CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Opc2, bits [19:17]

The Opc2 value from the issued instruction.

For a trapped VMRS access, holds the value 0b000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Opc1, bits [16:14]

The Opc1 value from the issued instruction.

For a trapped VMRS access, holds the value 0b111.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
CRn, bits [13:10]

The CRn value from the issued instruction.

For a trapped VMRS access, holds the reg field from the VMRS instruction encoding.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Rt, bits [9:5]

The Rt value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRm, bits [4:1]

The CRm value from the issued instruction.

For a trapped VMRS access, holds the value 0b0000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Direction, bit [0]

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRC or VMRS instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b008811:

- **CNTKCTL_EL1. {EL0PTEN, EL0VTEN, EL0PTCTEN, EL0VCTEN},** for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0. {ER, CR, SW, EN},** for accesses to Performance Monitor registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0. EN,** for accesses to Activity Monitors registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2. {TRVM, TVM},** for accesses to virtual memory control registers from EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2. TTLB,** for execution of TLB maintenance instructions at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2. TSW, TPC, TPU} for execution of cache maintenance instructions at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2. TACR,** for accesses to the Auxiliary Control Register at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2. TIDCP,** for accesses to lockdown, DMA, and TCM operations at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2. {TID1, TID2, TID3},** for accesses to ID registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2. TCPAC,** for accesses to **CPACR_EL1** or **CPACR** using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HSTR_EL2 T<n>,** for accesses to System registers using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CNTHTCTL_EL2. EL1PCEN,** for accesses to the Generic Timer registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2. {TPM, TPMCR},** for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2. TAM,** for accesses to Activity Monitors registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
• **CPTR_EL3.TCPAC**, for accesses to **CPACR** from EL1 and EL2, and accesses to **HCPTR** from EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.

• **MDCR_EL3.TPM**, for accesses to Performance Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.

• **CPTR_EL3.TAM**, for accesses to Activity Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.

• For information on other traps using EC value 0b000011, see ‘Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32’.

• If FEAT_FGT is implemented, MCR or MRC access to some registers at EL0, trapped to EL2.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000101:

• **CPACR_EL1.TTA** for accesses to trace registers, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.

• **MDSCR_EL1.TDCC**, for accesses to the Debug Communications Channel (DCC) registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.

• If FEAT_FGT is implemented, **MDCR_EL2.TDCC** for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

• **HCR_EL2.TID0**, for accesses to the **JIDR** register in the ID group 0 at EL0 and EL1 using AArch32, MRC access (coproc == 0b1110) trapped to EL2.

• **CPTR_EL2.TTA**, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDRA**, for accesses to Debug ROM registers **DBGDRAR** and AArch-DBGDSAR using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDOSA**, for accesses to powerdown debug registers, using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDA**, for accesses to other debug registers, using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDOSA**, for accesses to powerdown debug registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDA**, for accesses to other debug registers, using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b001000:

• **HCR_EL2.TID0**, for accesses to the **FPSID** register in ID group 0 at EL1 using AArch32 state, VMRS access trapped to EL2.

• **HCR_EL2.TID3**, for accesses to registers in ID group 3 including **MVFR0**, **MVFR1**, and **MVFR2**, VMRS access trapped to EL2.

### ISS encoding for an exception from an LD64B or ST64B* instruction

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **ISS** |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

<table>
<thead>
<tr>
<th>ISS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000000000000000000000</td>
<td>ST64BV instruction trapped.</td>
</tr>
<tr>
<td>0b000000000000000000000001</td>
<td>ST64BV0 instruction trapped.</td>
</tr>
<tr>
<td>0b000000000000000000000010</td>
<td>LD64B or ST64B instruction trapped.</td>
</tr>
</tbody>
</table>

All other values are reserved.

### ISS encoding for an exception from an MCRR or MRRC access

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| **CV** | **COND** | **Opc1** | **RES0** | **Rt2** | **Rt** | **CRm** | **Direction** |
| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Opc1, bits [19:16]

The Opc1 value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [15]

Reserved, RES0.

Rt2, bits [14:10]

The Rt2 value from the issued instruction, the second general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Rt, bits [9:5]

The Rt value from the issued instruction, the first general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRm, bits [4:1]

The CRm value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Direction, bit [0]

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCRR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRRC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000100:

- **CNTKCTL_EL1**, {EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCTEN}, for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0**, (CR, EN), for accesses to Performance Monitor registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0**, (EN), for accesses to Activity Monitors registers AMEVNTR0<n> and AMEVNTR1<n> from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**, {TRVM, TVM}, for accesses to virtual memory control registers from EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **HSTR_EL2.T<n>**, for accesses to System registers using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CNTHCCTL_EL2**, {EL1PCEN, EL1PCTEN}, for accesses to the Generic Timer registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2**, (TPM, TPMCR), for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2.TAM**, for accesses to Activity Monitors registers registers AMEVNTR0<n> and AMEVNTR1<n> from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL3**, TPM, for accesses to Performance Monitor registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.
- **MDCR_EL3.TDA**, for accesses to Activity Monitors registers registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.
- **CPACR_EL1.TTA** for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **CPTR_EL2.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.

The following sections describe configuration settings for generating exceptions that are reported using EC value 0b001100:

- **MDSCR_EL1.TDCC**, for accesses to the Debug ROM registers DBGDSAR and DBGDRAR at EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **MDCR_EL2.TDRA**, for accesses to Debug ROM registers DBGDRAR and AArch-DBGDSAR using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **MDCR_EL3.TDA**, for accesses to debug registers, using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.
- **CPACR_EL1.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **CPTR_EL2.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.
If the Armv8-A architecture is implemented with an ETMv4 implementation, MCRR and MRRC accesses to trace registers are UNDEFINED and the resulting exception is higher priority than an exception due to these traps.

**ISS encoding for an exception from an LDC or STC instruction**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | imm8 | RES0 | Rn | Offset | AM | Direction |

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**imm8, bits [19:12]**

The immediate value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [11:10]

Reserved, RES0.

Rn, bits [9:5]

The Rn value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

This field is valid only when AM[2] is 0, indicating an immediate form of the LDC or STC instruction. When AM[2] is 1, indicating a literal form of the LDC or STC instruction, this field is unknown.

On a Warm reset, this field resets to an architecturally unknown value.

Offset, bit [4]

Indicates whether the offset is added or subtracted:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Subtract offset.</td>
</tr>
<tr>
<td>0b1</td>
<td>Add offset.</td>
</tr>
</tbody>
</table>

This bit corresponds to the U bit in the instruction encoding.

On a Warm reset, this field resets to an architecturally unknown value.

AM, bits [3:1]

Addressing mode. The permitted values of this field are:

<table>
<thead>
<tr>
<th>AM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Immediate unindexed.</td>
</tr>
<tr>
<td>0b001</td>
<td>Immediate post-indexed.</td>
</tr>
<tr>
<td>0b010</td>
<td>Immediate offset.</td>
</tr>
<tr>
<td>0b011</td>
<td>Immediate pre-indexed.</td>
</tr>
<tr>
<td>0b100</td>
<td>For a trapped STC instruction or a trapped T32 LDC instruction this encoding is reserved.</td>
</tr>
<tr>
<td>0b110</td>
<td>For a trapped STC instruction, this encoding is reserved.</td>
</tr>
</tbody>
</table>

The values 0b101 and 0b111 are reserved. The effect of programming this field to a reserved value is that behavior is constrained unpredictable, as described in ‘Reserved values in System and memory-mapped registers and translation table entries’.

Bit [2] in this subfield indicates the instruction form, immediate or literal.

Bits [1:0] in this subfield correspond to the bits {P, W} in the instruction encoding.

On a Warm reset, this field resets to an architecturally unknown value.

Direction, bit [0]

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to memory. STC instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from memory. LDC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

The following fields describe the configuration settings for the traps that are reported using EC value 0b000110:

- **MDSCR_EL1.TDCC**, for accesses using AArch32 state, LDC access to **DBGDTRTXint** or STC access to **DBGDTRRXint** trapped to EL1 or EL2.
• **MDCR_EL2.TDA**, for accesses using AArch32 state, LDC access to **DBGDTRTXint** or STC access to **DBGDTRRXint** MCR or MRC access trapped to EL2.

• **MDCR_EL3.TDA**, for accesses using AArch32 state, LDC access to **DBGDTRTXint** or STC access to **DBGDTRRXint** MCR or MRC access trapped to EL3.

• If FEAT_FGT is implemented, **MDCR_EL2.TDCC** for LDC and STC accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

**ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality, resulting from the FPEN and TFP traps**

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The accesses covered by this trap include:

- Execution of SVE or Advanced SIMD and floating-point instructions.
- Accesses to the Advanced SIMD and floating-point System registers.

For an implementation that does not include either SVE or support for floating-point and Advanced SIMD, the exception is reported using the EC value 0b01000000.

**CV, bit [24]**

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [19:0]

Reserved, RES0.

The following sections describe the configuration settings for the traps that are reported using EC value 0b00000:

- **CPACR_EL1.FPEN**, for accesses to SIMD and floating-point registers trapped to EL1.
- **CPACR_EL2.TFP**, for accesses to SIMD and floating-point registers trapped to EL2.
- **CPACR_EL3.TFP**, for accesses to SIMD and floating-point registers trapped to EL3.

**ISS encoding for an exception from an access to SVE functionality, resulting from CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

The accesses covered by this trap include:

- Execution of SVE instructions.
- Accesses to the SVE System register, ZCR_ELx.

For an implementation that does not include SVE, the exception is reported using the EC value 0b000000.

Bits [24:0]

Reserved, RES0.

The following sections describe the configuration settings for the traps that are reported using EC value 0b011001:

- **CPACR_EL1.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0 or EL1, trapped to EL2.
- **CPTR_EL2.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL2.TZ**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL3.EZ**, for execution of SVE instructions and accesses to SVE registers from all Exception levels, trapped to EL3.

**ISS encoding for an exception from an Illegal Execution state, or a PC or SP alignment fault**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

**Bits [24:0]**

Reserved, RES0.

There are no configuration settings for generating Illegal Execution state exceptions and PC alignment fault exceptions. For more information about these exceptions, see 'The Illegal Execution state exception' and 'PC alignment checking'.

'SP alignment checking' describes the configuration settings for generating SP alignment fault exceptions.

**ISS encoding for an exception from HVC or SVC instruction execution**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

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Bits [24:16]

Reserved, res0.

imm16, bits [15:0]

The value of the immediate field from the HVC or SVC instruction.

For an HVC instruction, and for an A64 SVC instruction, this is the value of the imm16 field of the issued instruction.

For an A32 or T32 SVC instruction:

- If the instruction is unconditional, then:
  - For the T32 instruction, this field is zero-extended from the imm8 field of the instruction.
  - For the A32 instruction, this field is the bottom 16 bits of the imm24 field of the instruction.
- If the instruction is conditional, this field is unknown.

On a Warm reset, this field resets to an architecturally unknown value.

In AArch32 state, the HVC instruction is unconditional, and a conditional SVC instruction generates an exception only if it passes its condition code check. Therefore, the syndrome information for these exceptions does not require conditionality information.

For T32 and A32 instructions, see 'SVC' and 'HVC'.

For A64 instructions, see 'SVC' and 'HVC'.

If FEAT_FGT is implemented, HFGITR_EL2.{SVC_EL1, SVC_EL0} control fine-grained traps on SVC execution.

ISS encoding for an exception from SMC instruction execution in AArch32 state

```
<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>CCKOWNPASS</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

For an SMC instruction that completes normally and generates an exception that is taken to EL3, the ISS encoding is res0.

For an SMC instruction that is trapped to EL2 from EL1 because HCR_EL2.TSC is 1, the ISS encoding is as shown in the diagram.

CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is implementation defined whether CV is set to 1 or set to 0. See the description of the COND field for more information.

This field is valid only if CCKOWNPASS is 1, otherwise it is res0.

On a Warm reset, this field resets to an architecturally unknown value.

COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.
The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

This field is valid only if CCKNOWNPASS is 1, otherwise it is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CCKNOWNPASS, bit [19]**

Indicates whether the instruction might have failed its condition code check.

<table>
<thead>
<tr>
<th>CCKNOWNPASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The instruction was unconditional, or was conditional and passed its condition code check.</td>
</tr>
<tr>
<td>0b1</td>
<td>The instruction was conditional, and might have failed its condition code check.</td>
</tr>
</tbody>
</table>

**Note**

In an implementation in which an SMC instruction that fails it code check is not trapped, this field can always return the value 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [18:0]**

Reserved, RES0.

HCR_EL2.TSC describes the configuration settings for trapping SMC instructions to EL2.

'System calls' describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from SMC instruction execution in AArch64 state**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | imm16 | | | | | | | | | | | | |

**Bits [24:16]**

Reserved, RES0.
imm16, bits [15:0]

The value of the immediate field from the issued SMC instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The value of ISS[24:0] described here is used both:

- When an SMC instruction is trapped from EL1 modes.
- When an SMC instruction is not trapped, so completes normally and generates an exception that is taken to EL3.

HCR_EL2.TSC describes the configuration settings for trapping SMC from EL1 modes.

'System calls' describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from MSR, MRS, or System instruction execution in AArch64 state**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Op0</td>
<td>Op2</td>
<td>Op1</td>
<td>CRn</td>
<td>Rt</td>
<td>CRm</td>
<td>Direction</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:22]

Reserved, RES0.

**Op0, bits [21:20]**

The Op0 value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Op2, bits [19:17]**

The Op2 value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Op1, bits [16:14]**

The Op1 value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRn, bits [13:10]**

The CRn value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Rt, bits [9:5]**

The Rt value from the issued instruction, the general-purpose register used for the transfer.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write access, including MSR instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read access, including MRS instructions.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For exceptions caused by System instructions, see 'System instructions' subsection of 'Branches, exception generating and System instructions' for the encoding values returned by an instruction.

The following fields describe configuration settings for generating the exception that is reported using EC value 0b011000:

- `SCTLR_EL1.UCI`, for execution of cache maintenance instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `SCTLR_EL1.UCT`, for accesses to `CTR_EL0` using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `SCTLR_EL1.DZE`, for execution of DC ZVA instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `SCTLR_EL1.UMA`, for accesses to the PSTATE interrupt masks using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `CPACR_EL1.TTA`, for accesses to the trace registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `MDSCR_EL1.TDCC`, for accesses to the Debug Communications Channel (DCC) registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- If `FEAT_FGT` is implemented, `MDCR_EL2.TDCC` for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and `MDCR_EL3.TDCC` for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.
- `CNTKCTL_EL1`, `{EL0PTEN, EL0VTEN, EL0PCTEN, ELOVCTEN}` accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `PMUSERENR_EL0.ER, CR, SW, EN`, for accesses to the Performance Monitor registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `AMUSERENR_EL0.EN`, for accesses to Activity Monitors registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `HCR_EL2.TRVM, TVM`, for accesses to virtual memory control registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `HCR_EL2.TDA`, for accesses to DC ZVA instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- `HCR_EL2.TTLB`, for execution of TLB maintenance instructions using AArch64 state, MSR or MRS access trapped to EL2.
- `HCR_EL2.TSW, TPC, TPU`, for execution of cache maintenance instructions using AArch64 state, MSR or MRS access trapped to EL2.
- `HCR_EL2.TACR`, for accesses to the Auxiliary Control Register, `ACTLR_EL1`, using AArch64 state, MSR or MRS access trapped to EL2.
- `HCR_EL2.TIDCP`, for accesses to lockdown, DMA, and TCM operations using AArch64 state, MSR or MRS access trapped to EL2.
- `HCR_EL2.TID1, TID2, TID3`, for accesses to ID group 1, ID group 2 or ID group 3 registers, using AArch64 state, MSR or MRS access trapped to EL2.
- `CPTR_EL2.TCPAC`, for accesses to `CPACR_EL1`, using AArch64 state, MSR or MRS access trapped to EL2.
- `CPTR_EL2.TAM`, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access trapped to EL2.
- `MDCR_EL2.TTRF`, for accesses to the trace filter control register, `TRFCR_EL1`, using AArch64 state, MSR or MRS access trapped to EL2.
- `MDCR_EL2.TDRA`, for accesses to Debug ROM registers, using AArch64 state, MSR or MRS access trapped to EL2.
- `MDCR_EL2.TDOSA`, for accesses to powerdown debug registers using AArch64 state, MSR or MRS access trapped to EL2.
- `CNTKCTL_EL2`, `{EL1PCEN, EL1PCTEN}` for accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL2.
- `MDCR_EL2.TDA`, for accesses to debug registers using AArch64 state, MSR or MRS access trapped to EL2.
- `MDCR_EL2.TPM, TPMCR`, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL2.
HCR_EL2.APK, for accesses to Pointer authentication key registers, using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.{NV, NV1}, for Nested virtualization register access, using AArch64 state, MSR or MRS access, trapped to EL2.

HCR_EL2.AT, for execution of AT S1E* instructions, using AArch64 state, MSR or MRS access, trapped to EL2.

HCR_EL2.{TERR, FIEN}, for accesses to RAS registers, using AArch64 state, MSR or MRS access, trapped to EL2.

SCR_EL2.APK, for accesses to Pointer authentication key registers, using AArch64 state, MSR or MRS access trapped to EL3.

SCR_EL2.ST, for accesses to the Counter-timer Physical Secure timer registers, using AArch64 state, MSR or MRS access trapped to EL3.

SCR_EL2.{TERR, FIEN}, for accesses to RAS registers, using AArch64 state, MSR or MRS access trapped to EL3.

CPTR_EL3.TCPAC, for accesses to CPTR_EL2 and CPACR_EL1 using AArch64 state, MSR or MRS access trapped to EL3.

CPTR_EL3.TTA, for accesses to the trace registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TTRF, for accesses to the trace filter control registers, TRFCR_EL1 and TRFCR_EL2, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TDA, for accesses to debug registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TDOSA, for accesses to powerdown debug registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TPM, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL3.

CPTR_EL3.TAM, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access, trapped to EL3.

If FEAT_EVT is implemented, the following registers control traps for EL1 and EL0 Cache controls that use this EC value:

- HCR_EL2.{TTLBOS, TTLBIS, TICAB, TOCU, TID4}.
- HCR2.{TTLBIS, TICAB, TOCU, TID4}.

If FEAT_FGT is implemented:

- SCR_EL3.FGTEn, for accesses to the fine-grained trap registers, MSR or MRS access at EL2 trapped to EL3.
  - HFGTR_EL2 for reads and HFGWTR_EL2 for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 trapped to EL2.
  - HDFGRTR_EL2 for reads and HDFGWTR_EL2 for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 state trapped to EL2.
  - HAFGRTR_EL2 for reads of Activity Monitor counters, using AArch64 state, MRS access at EL0 and EL1 trapped to EL2.

ISS encoding for an IMPLEMENTATION DEFINED exception to EL3

| 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [24:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS encoding for an exception from an Instruction Abort

| 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
| RES0 | SET | Fn | VE | EA | RES0 | S1PTW | RES0 | IFSC |

Bits [24:13]

Reserved, RES0.

SET, bits [12:11]

Reserved.
When FEAT_RAS is implemented:

Synchronous Error Type. When IFSC is 0b010000, describes the PE error state after taking the Instruction Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the IFSC code is 0b010000. It is res0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, res0.

FnV, bit [10]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is valid only if the IFSC code is 0b010000. It is res0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EA, bit [9]

External abort type. This bit can provide an IMPLEMENTATION DEFINED classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [8]

Reserved, res0.

S1PTW, bit [7]

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>
For any abort other than a stage 2 fault this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [6]**

Reserved, RES0.

**IFSC, bits [5:0]**

Instruction Fault Status Code.
<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td></td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b101001</td>
<td>Address size fault, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b101010</td>
<td>Address size fault, level -2.</td>
<td></td>
</tr>
<tr>
<td>0b101011</td>
<td>Address size fault, level -3.</td>
<td></td>
</tr>
</tbody>
</table>

ESR_EL1, Exception Syndrome Register (EL1)
When FEAT_LPA2 is implemented

**TLB conflict abort.**

When FEAT_HAFDBS is implemented

**Unsupported atomic hardware update fault.**

All other values are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults’.

**Note**

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### ISS encoding for an exception from a Data Abort

| Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| **ISV** | **SAS** | **SSR** | **SRT** | **SF** | **A** | **V** | **N** | **CR** | **Bits[12:11]** | **Fr** | **V** | **E** | **A** | **CM** | **S1PTW** | **WnR** | **DFSC** |

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this ISS encoding includes ISS2, **bits[36:32]**.

**ISV, bit [24]**

Instruction Syndrome Valid. Indicates whether the syndrome information in ISS[23:14] is valid.

<table>
<thead>
<tr>
<th><strong>ISV</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No valid instruction syndrome. ISS[23:14] are <strong>RES0</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>ISS[23:14] hold a valid instruction syndrome.</td>
</tr>
</tbody>
</table>

In ESR_EL2, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

For other faults reported in ESR_EL2, ISV is 0 except for the following stage 2 aborts:

- AArch64 loads and stores of a single general-purpose register (including the register specified with 0b11111, including those with Acquire/Release semantics, but excluding Load Exclusive or Store Exclusive and excluding those with writeback).
- AArch32 instructions where the instruction:
  - Is an LDR, LDA, LDRH, LDRB, LDRRT, LDRSH, LDRRT, LDRRT, , LDRRT, LDRB, LDRB, LDRRT, STR, STR, STR, STR, STR, STLH, STRHT, STRB, or STRBT instruction.
  - Is not performing register writeback.
  - Is not using R15 as a source or destination register.

For these stage 2 aborts, ISV is **UNKNOWN** if the exception was generated in Debug state in memory access mode, and otherwise indicates whether ISS[23:14] hold a valid syndrome.

For faults reported in ESR_EL1 or ESR_EL3, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault. ISV is 0 for all other faults reported in ESR_EL1 or ESR_EL3.

When FEAT_RAS is implemented, ISV is 0 for any synchronous External abort.

For ISS reporting, a stage 2 abort on a stage 1 translation table walk does not return a valid instruction syndrome, and therefore ISV is 0 for these aborts.
When FEAT_RAS is not implemented, it is IMPLEMENTATION DEFINED whether ISV is set to 1 or 0 on a synchronous External abort on a stage 2 translation table walk.

When FEAT_MTE is implemented, for a synchronous Tag Check Fault abort taken to ELx, ESR_ELx.FNV is 0 and FAR_ELx is valid.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SAS, bits [23:22]**

When ISV == ‘1’:

Syndrome Access Size. Indicates the size of the access attempted by the faulting operation.

<table>
<thead>
<tr>
<th>SAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Byte</td>
</tr>
<tr>
<td>0b01</td>
<td>Halfword</td>
</tr>
<tr>
<td>0b10</td>
<td>Word</td>
</tr>
<tr>
<td>0b11</td>
<td>Doubleword</td>
</tr>
</tbody>
</table>

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0b11.

This field is UNKNOWN when the value of ISV is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SSE, bit [21]**

When ISV == ‘1’:

Syndrome Sign Extend. For a byte, halfword, or word load operation, indicates whether the data item must be sign extended.

<table>
<thead>
<tr>
<th>SSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sign-extension not required.</td>
</tr>
<tr>
<td>0b1</td>
<td>Data item must be sign-extended.</td>
</tr>
</tbody>
</table>

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

For all other operations, this field is 0.

This field is UNKNOWN when the value of ISV is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SRT, bits [20:16]**

When ISV == ‘1’:

Syndrome Register Transfer. When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xt.
If the exception was taken from an Exception level that is using AArch32, then this is the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**SF, bit [15]**

**When ISV == ‘1’:**

Width of the register accessed by the instruction is Sixty-Four.

<table>
<thead>
<tr>
<th>SF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction loads/stores a 32-bit wide register.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction loads/stores a 64-bit wide register.</td>
</tr>
</tbody>
</table>

**Note**

This field specifies the register width identified by the instruction, not the Execution state.

When FEAT LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 1.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**AR, bit [14]**

**When ISV == ‘1’:**

Acquire/Release.

<table>
<thead>
<tr>
<th>AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction did not have acquire/release semantics.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction did have acquire/release semantics.</td>
</tr>
</tbody>
</table>

When FEAT LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.
**VNCR, bit [13]**

When FEAT_NV2 is implemented:

Indicates that the fault came from use of VNCR_EL2 register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault was not generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault was generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
</tbody>
</table>

This field is 0 in ESR_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SET, bits [12:11]**

When FEAT_RAS is implemented and FEAT_LS64 is not implemented:

Synchronous Error Type. When DFSC is 0b010000, describes the PE error state after taking the Data Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Note**

Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the DFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When FEAT_LS64 is implemented:

Load/Store Type. Used when an LD64B, ST64B, ST64BV, or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

<table>
<thead>
<tr>
<th>LST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>An ST64BV instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b10</td>
<td>An LD64B or ST64B instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b11</td>
<td>An ST64BV0 instruction generated the Data Abort.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is valid only if the DFSC code is 0b110101. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
FnV, bit [10]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an unknown value.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010000. It is res0 for all other aborts.

On a Warm reset, this field resets to an architecturally unknown value.

EA, bit [9]

External abort type. This bit can provide an implementation defined classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally unknown value.

CM, bit [8]

Cache maintenance. Indicates whether the Data Abort came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Data Abort was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Data Abort was generated by either the execution of a cache maintenance instruction or by a synchronous fault on the execution of an address translation instruction. The DC ZVA, DC GVA, and DC GZVA instructions are not classified as cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

S1PTW, bit [7]

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is res0.

On a Warm reset, this field resets to an architecturally unknown value.

WnR, bit [6]

Write not Read. Indicates whether a synchronous abort was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For faults on cache maintenance and address translation instructions, this bit always returns a value of 1.
For faults from an atomic instruction that both reads and writes from a memory location, this bit is set to 0 if a read of the address specified by the instruction would have generated the fault which is being reported, otherwise it is set to 1. The architecture permits, but does not require, a relaxation of this requirement such that for all stage 2 aborts on stage 1 translation table walks for atomic instructions, the WnR bit is always 0.

This field is **UNKNOWN** for:

- An External abort on an Atomic access.
- A fault reported using a DFSC value of **0b110101** or **0b110001**, indicating an unsupported Exclusive or atomic access.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DFSC, bits [5:0]**

Data Fault Status Code.
<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 0.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td>When FEAT_MTE is implemented When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010001</td>
<td>Synchronous Tag Check Fault.</td>
<td></td>
</tr>
<tr>
<td>0b010010</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>
Alignment fault.
Address size fault, level -1.
Translation fault, level -1.
TLB conflict abort.
Unsupported atomic hardware update fault.
IMPLEMENTATION DEFINED fault (Lockdown).
IMPLEMENTATION DEFINED fault (Unsupported Exclusive or Atomic access).

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults'.

Note

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

### ISS encoding for an exception from a trapped floating-point exception

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{RES0}\texttt{TFV}</td>
<td>\texttt{RES0}</td>
</tr>
</tbody>
</table>

#### Bit [24]

Reserved, \texttt{RES0}.

#### TFV, bit [23]

Trapped Fault Valid bit. Indicates whether the IDF, IXF, UFF, OFF, DZF, and IOF bits hold valid information about trapped floating-point exceptions.

<table>
<thead>
<tr>
<th>TFV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0}</td>
<td>The IDF, IXF, UFF, OFF, DZF, and IOF bits do not hold valid information about trapped floating-point exceptions and are \texttt{UNKNOWN}.</td>
</tr>
<tr>
<td>\texttt{0b1}</td>
<td>One or more floating-point exceptions occurred during an operation performed while executing the reported instruction. The IDF, IXF, UFF, OFF, DZF, and IOF bits indicate trapped floating-point exceptions that occurred. For more information, see 'Floating-point exceptions and exception traps'.</td>
</tr>
</tbody>
</table>

It is \texttt{IMPLEMENTATION DEFINED} whether this field is set to 0 on an exception generated by a trapped floating point exception from a vector instruction.

Note

This is not a requirement. Implementations can set this field to 1 on a trapped floating-point exception from a vector instruction and return valid information in the \{IDF, IXF, UFF, OFF, DZF, IOF\} fields.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [22:11]**

Reserved, **RES0**.

**VECITR, bits [10:8]**

For a trapped floating-point exception from an instruction executed in AArch32 state this field is **RES1**.

For a trapped floating-point exception from an instruction executed in AArch64 state this field is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IDF, bit [7]**

Input Denormal floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IDF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input denormal floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input denormal floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [6:5]**

Reserved, **RES0**.

**IXF, bit [4]**

Inexact floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IXF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inexact floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inexact floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**UFF, bit [3]**

Underflow floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>UFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**OFF, bit [2]**

Overflow floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>OFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Overflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DZF, bit [1]**

Divide by Zero floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>DZF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Divide by Zero floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Divide by Zero floating-point exception occurred during</td>
</tr>
<tr>
<td></td>
<td>execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IOF, bit [0]**

Invalid Operation floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IOF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalid Operation floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalid Operation floating-point exception occurred during</td>
</tr>
<tr>
<td></td>
<td>execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

In an implementation that supports the trapping of floating-point exceptions:

- From an Exception level using AArch64, the **FPCR**.{IDE, IXE, UFE, OFE, DZE, IOE} bits enable each of the floating-point exception traps.
- From an Exception level using AArch32, the **FPSCR**.{IDE, IXE, UFE, OFE, DZE, IOE} bits enable each of the floating-point exception traps.

**ISS encoding for an SError interrupt**

| 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| IDS | RES0| IESB| AET | EA  | RES0| DFSC|

**IDS, bit [24]**

**IMPLEMENTATION DEFINED** syndrome.

<table>
<thead>
<tr>
<th>IDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits [23:0] of the ISS field holds the fields described in this encoding.</td>
</tr>
</tbody>
</table>

**Note**

If FEAT_RAS is not implemented, bits [23:0] of the ISS field are **RES0**.

| 0b1 | Bits [23:0] of the ISS field holds **IMPLEMENTATION DEFINED** syndrome information that can be used to provide additional information about the SError interrupt. |

**Note**

This field was previously called ISV.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [23:14]**

Reserved, **RES0**.
IESB, bit [13]

When FEAT_IESB is implemented:

Implicit error synchronization event.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The SError interrupt was either not synchronized by the implicit error synchronization event or not taken immediately.</td>
</tr>
<tr>
<td>0b1</td>
<td>The SError interrupt was synchronized by the implicit error synchronization event and taken immediately.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

AET, bits [12:10]

When FEAT_RAS is implemented:

Asynchronous Error Type.

When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception.

<table>
<thead>
<tr>
<th>AET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b001</td>
<td>Unrecoverable state (UEU).</td>
</tr>
<tr>
<td>0b010</td>
<td>Restartable state (UEO).</td>
</tr>
<tr>
<td>0b011</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b110</td>
<td>Corrected (CE).</td>
</tr>
</tbody>
</table>

All other values are reserved.

If multiple errors are taken as a single SError interrupt exception, the overall PE error state is reported.

Note

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EA, bit [9]

When FEAT_RAS is implemented:

External abort type. When DFSC is 0b010001, provides an IMPLEMENTATION DEFINED classification of External aborts.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

Bits [8:6]

Reserved, RES0.

DFSC, bits [5:0]

When FEAT_RAS is implemented:

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Uncategorized error.</td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

ISS encoding for an exception from a Breakpoint or Vector Catch debug exception

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
<th>RES0</th>
<th>IFSC</th>
</tr>
</thead>
</table>

Bits [24:6]

Reserved, RES0.

IFSC, bits [5:0]

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions:

- For exceptions from AArch64, see ‘Breakpoint exceptions’.
- For exceptions from AArch32, see ‘Breakpoint exceptions’ and ‘Vector Catch exceptions’.

ISS encoding for an exception from a Software Step exception

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
<th>ISV</th>
<th>RES0</th>
<th>EX</th>
<th>IFSC</th>
</tr>
</thead>
</table>

ISV, bit [24]

Instruction syndrome valid. Indicates whether the EX bit, ISS[6], is valid, as follows:
ISV | Meaning
--- | ---
0b0 | EX bit is RES0.
0b1 | EX bit is valid.

See the EX bit description for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [23:7]**

Reserved, RES0.

**EX, bit [6]**

Exclusive operation. If the ISV bit is set to 1, this bit indicates whether a Load-Exclusive instruction was stepped.

<table>
<thead>
<tr>
<th>EX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An instruction other than a Load-Exclusive instruction was stepped.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Load-Exclusive instruction was stepped.</td>
</tr>
</tbody>
</table>

If the ISV bit is set to 0, this bit is RES0, indicating no syndrome data is available.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IFSC, bits [5:0]**

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see ‘Software Step exceptions’.

**ISS encoding for an exception from a Watchpoint exception**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0VNCR | RES0 | CMRES0WnR | DFSC |

**Bits [24:15]**

Reserved, RES0.

**Bit [14]**

Reserved, RES0.

**VNCR, bit [13]**

When FEAT_NV2 is implemented:

Indicates that the watchpoint came from use of VNCR_EL2 register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The watchpoint was not generated by the use of VNCR_EL2 by EL1 code.</td>
</tr>
<tr>
<td>0b1</td>
<td>The watchpoint was generated by the use of VNCR_EL2 by EL1 code.</td>
</tr>
</tbody>
</table>

This field is 0 in ESR_EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [12:9]

Reserved, RES0.

CM, bit [8]

Cache maintenance. Indicates whether the Watchpoint exception came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Watchpoint exception was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Watchpoint exception was generated by either the execution of a cache maintenance instruction or by a synchronous Watchpoint exception on the execution of an address translation instruction. The DC ZVA, DC GVA, and DC GZVA instructions are not classified as a cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [7]

Reserved, RES0.

WnR, bit [6]

Write not Read. Indicates whether the Watchpoint exception was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint exception caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint exception caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For Watchpoint exceptions on cache maintenance and address translation instructions, this bit always returns a value of 1.

For Watchpoint exceptions from an atomic instruction, this field is set to 0 if a read of the location would have generated the Watchpoint exception, otherwise it is set to 1.

If multiple watchpoints match on the same access, it is UNPREDICTABLE which watchpoint generates the Watchpoint exception.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DFSC, bits [5:0]

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
For more information about generating these exceptions, see 'Watchpoint exceptions'.

**ISS encoding for an exception from execution of a Breakpoint instruction**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Comment</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [24:16]**

Reserved, RES0.

**Comment, bits [15:0]**

Set to the instruction comment field value, zero extended as necessary.

For the AArch32 BKPT instructions, the comment field is described as the immediate field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see 'Breakpoint instruction exceptions'.

**ISS encoding for an exception from an ERET, ERETA, or ERETAB instruction**

| 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | ERETERETA |

This EC value applies when FEAT_FGT is implemented, or when HCR_EL2.NV is 1.

**Bits [24:2]**

Reserved, RES0.

**ERET, bit [1]**

Indicates whether an ERET or ERETA* instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERET instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETA or ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

If this bit is 0, the ERETA field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EREOTA, bit [0]**

Indicates whether an ERETA or ERETAB instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERETA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERETA instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

When the ERET field is 0, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see HCR_EL2.NV.

If FEAT_FGT is implemented, HFGITR_EL2.ERET controls fine-grained trap exceptions from ERET, ERETA and ERETAB execution.
ISS encoding for an exception from Branch Target Identification instruction

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|    |    |    |    |    |    |    | BTYPE |

**Bits [24:2]**

Reserved, RES0.

**BTYPE, bits [1:0]**

This field is set to the PSTATE.BTYPE value that generated the Branch Target Exception.

For more information about generating these exceptions, see ’The AArch64 application level programmers model’.

ISS encoding for an exception from a Pointer Authentication instruction when HCR_EL2.API == 0 || SCR_EL3.API == 0

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|    |    |    |    |    |    |    |    |

**Bits [24:0]**

Reserved, RES0.

For more information about generating these exceptions, see:

- HCR_EL2.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL2.
- SCR_EL3.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL3.

ISS encoding for an exception from a Pointer Authentication instruction authentication failure

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|    |    |    |    |    |    |    |    |

**Bits [24:2]**

Reserved, RES0.

**Bit [1]**

This field indicates whether the exception is as a result of an Instruction key or a Data key.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [0]

This field indicates whether the exception is as a result of an A key or a B key.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

The following instructions generate an exception when the Pointer Authentication Code (PAC) is incorrect:

- AUTIASP, AUTIAZ, AUTIA1716.
- AUTIBSP, AUTIBZ, AUTIB1716.
- AUTIA, AUTDA, AUTIB, AUTDB.
- AUTIZA, AUTIZB, AUTDZA, AUTDZB.

It is implementation defined whether the following instructions generate an exception directly from the authorization failure, rather than changing the address in a way that will generate a translation fault when the address is accessed:

- RETAA, RETAB.
- BRAA, BRAB, BLRAA, BLRAB.
- BRAAZ, BRABZ, BLRAAZ, BLRABZ.
- ERETA, ERETAB.
- LDRAA, LDRAB, whether the authenticated address is written back to the base register or not.

**Accessing the ESR_EL1**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic ESR_EL1 or ESR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, ESR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ESR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x138];
  else
    return ESR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ESR_EL2;
  else
    return ESR_EL1;
elsif PSTATE.EL == EL3 then
  return ESR_EL1;

**MSR ESR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ESR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x138] = X[t];
  else
    ESR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    ESR_EL2 = X[t];
  else
    ESR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  ESR_EL1 = X[t];

MRS <Xt>, ESR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x138];
  elseif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return ESR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return ESR_EL1;
  else
    UNDEFINED;

MSR ESR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NMem[0x138] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if EL2Enabled() && HCR_EL2.E2H == '1' then
        ESR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        ESR_EL1 = X[t];
    else
        UNDEFINED;
MRS <Xt>, ESR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return ESR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return ESR_EL2;
elsif PSTATE.EL == EL3 then
    return ESR_EL2;
MSR ESR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        ESR_EL2 = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    ESR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    ESR_EL2 = X[t];
ESR_EL2, Exception Syndrome Register (EL2)

The ESR_EL2 characteristics are:

**Purpose**

Holds syndrome information for an exception taken to EL2.

**Configuration**

AArch64 System register ESR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HSR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ESR_EL2 is a 64-bit register.

**Field descriptions**

The ESR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EC | IL | RES0 | ISS2 |

ESR_EL2 is made UNKNOWN as a result of an exception return from EL2.

When an UNPREDICTABLE instruction is treated as UNDEFINED, and the exception is taken to EL2, the value of ESR_EL2 is UNKNOWN. The value written to ESR_EL2 must be consistent with a value that could be created as a result of an exception from the same Exception level that generated the exception as a result of a situation that is not UNPREDICTABLE at that Exception level, in order to avoid the possibility of a privilege violation.

**Bits [63:37]**

Reserved, RES0.

**ISS2, bits [36:32]**

When FEAT_LS64 is implemented:

If a memory access generated by an ST64BV or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xs.

For any other Data Abort, this field is RES0.

Otherwise:

Reserved, RES0.

**EC, bits [31:26]**

Exception Class. Indicates the reason for the exception that this register holds information about.
For each EC value, the table references a subsection that gives information about:

- The cause of the exception, for example the configuration required to enable the trap.
- The encoding of the associated ISS.

Possible values of the EC field are:
<table>
<thead>
<tr>
<th>EC</th>
<th>Meaning</th>
<th>ISS encoding for exceptions with an unknown reason</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Unknown reason.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Trapped WF* instruction execution. Conditional WF* instructions that fail their condition code check do not cause an exception.</td>
<td>ISS encoding for an exception from a WF* instruction</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Trapped MCR or MRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b000100</td>
<td>Trapped MCRR or MRRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCRR or MRRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b000101</td>
<td>Trapped MCR or MRC access with (coproc==0b1110).</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
</tbody>
</table>
| 0b000110 | Trapped LDC or STC access. The only architected uses of these instruction are:  
  • An STC to write data to memory from DBGDTRRXint.  
  • An LDC to read data from memory to DBGDTRRXint. | ISS encoding for an exception from an LDC or STC instruction | When AArch32 is supported at any Exception level |
| 0b000111 | Access to SVE, Advanced SIMD or floating-point functionality trapped by CPACR_EL1.FPEN, CPTR_EL2.FPEN, CPTR_EL2.TFP, or CPTR_EL3.TFP control. Excludes exceptions resulting from CPACR_EL1 when the value of HCR_EL2.TGE is 1, or because SVE or Advanced SIMD and floating-point are not implemented. These are reported with EC value 0b000000 as described in 'The EC used to report an exception routed to EL2 because HCR_EL2.TGE is 1'. | ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality resulting from the FPEN and TFP traps |                                                  |
| 0b001000 | Trapped VMRS access, from ID group trap.                                | ISS encoding for an exception                       | When AArch32 is supported at any Exception level |
that is not reported using EC 0b000111.

**0b001001**
Trapped use of a Pointer authentication instruction because HCR_EL2.API == 0 || SCR_EL3.API == 0.

**ISS encoding for an exception from a Pointer Authentication instruction when HCR_EL2.API == 0 || SCR_EL3.API == 0.**

When FEAT_PAuth is implemented.

**0b001010**
Trapped execution of an LD64B, ST64B, ST64BV, or ST64BV0 instruction.

**ISS encoding for an exception from an LD64B or ST64B* instruction.**

When FEAT_LS64 is implemented.

**0b001100**
Trapped MRRC access with (coproc==0b1110).

**ISS encoding for an exception from an MCRR or MRRC access.**

When AArch32 is supported at any Exception level.

**0b001101**
Branch Target Exception.

**ISS encoding for an exception from Branch Target Identification instruction.**

When FEAT_BTI is implemented.

**0b001110**
Illegal Execution state.

**ISS encoding for an exception from an Illegal Execution state, or a PC or SP alignment fault.**

When AArch32 is supported at any Exception level.

**0b010001**
SVC instruction execution in AArch32 state.

This is reported in ESR_EL2 only when the exception is generated because the value of HCR_EL2.TGE is 1.

**ISS encoding for an exception from HVC or SVC instruction execution.**

When AArch32 is supported at any Exception level.

**0b010010**
HVC instruction execution in AArch32 state, when HVC is not disabled.

**ISS encoding for an exception from HVC or SVC instruction execution.**

When AArch32 is supported at any Exception level.

**0b010011**
SMC instruction execution in AArch32 state, when SMC is not disabled.

This is reported in ESR_EL2 only when the exception is generated because the value of HCR_EL2.TSC is 1.

**ISS encoding for an exception from SMC instruction execution in AArch32 state.**

When AArch32 is supported at any Exception level.

**0b010101**
SVC instruction execution in AArch64 state.

**ISS encoding for an exception from HVC or SVC instruction execution.**

When AArch64 is supported at any Exception level.

**0b010110**
HVC instruction execution in AArch64 state.

**ISS encoding for an exception from HVC or SVC instruction execution.**

When AArch64 is supported at any Exception level.
**ESR_EL2, Exception Syndrome Register (EL2)**

state, when HVC is not disabled.

<table>
<thead>
<tr>
<th>Exception</th>
<th>Encoding</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b010111</td>
<td>SMC instruction execution in AArch64 state, when SMC is not disabled. This is reported in ESR_EL2 only when the exception is generated because the value of \text{HCR_EL2}.TSC is 1.</td>
<td>ISS encoding for an exception from SMC instruction execution in AArch64 state</td>
</tr>
<tr>
<td>0b011000</td>
<td>Trapped MSR, MRS or System instruction execution in AArch64 state, that is not reported using EC 0b000000, 0b000001 or 0b000111. This includes all instructions that cause exceptions that are part of the encoding space defined in 'System instruction class encoding overview', except for those exceptions reported using EC values 0b000000, 0b000001, or 0b000111.</td>
<td>ISS encoding for an exception from MSR, MRS, or System instruction execution in AArch64 state</td>
</tr>
<tr>
<td>0b011001</td>
<td>Access to SVE functionality trapped as a result of \text{CPACR_EL1}.ZEN, \text{CPTR_EL1}.ZEN, \text{CPTR_EL2}.TZ, or \text{CPTR_EL3}.EZ, that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an access to SVE functionality resulting from \text{CPACR_EL1}.ZEN, \text{CPTR_EL1}.ZEN, \text{CPTR_EL2}.TZ, or \text{CPTR_EL3}.EZ</td>
</tr>
<tr>
<td>0b011010</td>
<td>Trapped ERET, ERETTA, or ERETAB instruction execution.</td>
<td>ISS encoding for an exception from an ERET, ERETTA, or ERETAB instruction</td>
</tr>
<tr>
<td>0b011100</td>
<td>Exception from a Pointer Authentication instruction authentication failure</td>
<td>ISS encoding for an exception from a Pointer Authentication instruction authentication failure</td>
</tr>
<tr>
<td>0b100000</td>
<td>Instruction Abort from a lower Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
<td>ISS encoding for an exception from an Instruction Abort</td>
</tr>
</tbody>
</table>

When AArch64 is supported at any Exception level.
<table>
<thead>
<tr>
<th>ISS Encoding</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100001</td>
<td>Instruction Abort taken without a change in Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td>0b100010</td>
<td>PC alignment fault exception.</td>
</tr>
<tr>
<td>0b100100</td>
<td>Data Abort from a lower Exception level, excluding Data Aborts taken to EL2 as a result of accesses generated associated with VNCR_EL2 as part of nested virtualization support. These Data Aborts might be generated from Exception levels in any Execution state. Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td>0b100101</td>
<td>Data Abort without a change in Exception level, or Data Aborts taken to EL2 as a result of accesses generated associated with VNCR_EL2 as part of nested virtualization support. Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.</td>
</tr>
<tr>
<td>0b100110</td>
<td>SP alignment fault exception.</td>
</tr>
</tbody>
</table>
or a PC or SP alignment fault
ISS encoding for an exception from a trapped floating-point exception
When AArch32 is supported at any Exception level

Trapped floating-point exception taken from AArch32 state. This EC value is valid if the implementation supports trapping of floating-point exceptions, otherwise it is reserved. Whether a floating-point implementation supports trapping of floating-point exceptions is IMPLEMENTATION DEFINED.

ISS encoding for an exception from a trapped floating-point exception
When AArch64 is supported at any Exception level

Trapped floating-point exception taken from AArch64 state. This EC value is valid if the implementation supports trapping of floating-point exceptions, otherwise it is reserved. Whether a floating-point implementation supports trapping of floating-point exceptions is IMPLEMENTATION DEFINED.

ISS encoding for an exception from a trapped floating-point exception
When AArch64 is supported at any Exception level

SErrror interrupt.
ISS encoding for an SError interrupt

Breakpoint exception from a lower Exception level.
ISS encoding for an exception from a Breakpoint or Vector Catch debug exception

Breakpoint exception taken without a change in Exception level.
ISS encoding for an exception from a Breakpoint or Vector Catch debug exception

Software Step exception from a lower Exception level.
ISS encoding for an exception from a Software Step exception

Software Step exception taken without a change in Exception level.
ISS encoding for an exception from a Software Step exception

Watchpoint from a lower Exception level, excluding Watchpoint Exceptions taken to EL2 as a result of accesses generated associated with VNCR_EL2 as part of nested virtualization support. These Watchpoint Exceptions might be generated from
ISS encoding for an exception from a Watchpoint exception
Exception levels using any Execution state.

0b110101 Watchpoint exceptions without a change in Exception level, or Watchpoint exceptions taken to EL2 as a result of accesses generated associated with VNCR_EL2 as part of nested virtualization support. 

**ISS encoding for an exception from a Watchpoint exception**

0b111000 BKPT instruction execution in AArch32 state.

**ISS encoding for an exception from execution of a Breakpoint instruction**

When AArch32 is supported at any Exception level

0b111010 Vector Catch exception from AArch32 state.

The only case where a Vector Catch exception is taken to an Exception level that is using AArch64 is when the exception is routed to EL2 and EL2 is using AArch64.

**ISS encoding for an exception from a Breakpoint or Vector Catch debug exception**

When AArch32 is supported at any Exception level

0b111100 BRK instruction execution in AArch64 state.

This is reported in ESR_EL3 only if a BRK instruction is executed.

**ISS encoding for an exception from execution of a Breakpoint instruction**

When AArch64 is supported at any Exception level

All other EC values are reserved by Arm, and:

- Unused values in the range 0b000000 - 0b101100 (0x00 - 0x2C) are reserved for future use for synchronous exceptions.
- Unused values in the range 0b101101 - 0b111111 (0x2D - 0x3F) are reserved for future use, and might be used for synchronous or asynchronous exceptions.

The effect of programming this field to a reserved value is that behavior is **CONSTRAINED UNPREDICTABLE**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [25]**

Instruction Length for synchronous exceptions. Possible values of this bit are:
<table>
<thead>
<tr>
<th>IL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>16-bit instruction trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>32-bit instruction trapped. This value is also used when the exception is one of the following:</td>
</tr>
<tr>
<td></td>
<td>• An SError interrupt.</td>
</tr>
<tr>
<td></td>
<td>• An Instruction Abort exception.</td>
</tr>
<tr>
<td></td>
<td>• A PC alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• An SP alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• A Data Abort exception for which the value of the ISV bit is 0.</td>
</tr>
<tr>
<td></td>
<td>• An Illegal Execution state exception.</td>
</tr>
<tr>
<td></td>
<td>• Any debug exception except for Breakpoint instruction exceptions. For Breakpoint instruction exceptions, this bit has its standard meaning:</td>
</tr>
<tr>
<td></td>
<td>◦ 0b0: 16-bit T32 BKPT instruction.</td>
</tr>
<tr>
<td></td>
<td>◦ 0b1: 32-bit A32 BKPT instruction or A64 BRK instruction.</td>
</tr>
<tr>
<td></td>
<td>• An exception reported using EC value 0b000000.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ISS, bits [24:0]**

Instruction Specific Syndrome. Architecturally, this field can be defined independently for each defined Exception class. However, in practice, some ISS encodings are used for more than one Exception class.

Typically, an ISS encoding has a number of subfields. When an ISS subfield holds a register number, the value returned in that field is the AArch64 view of the register number.

For an exception taken from AArch32 state, see 'Mapping of the general-purpose registers between the Execution states'.

If the AArch32 register descriptor is 0b1111, then:

- If the instruction that generated the exception was not UNPREDICTABLE, the field takes the value 0b11111.
- If the instruction that generated the exception was UNPREDICTABLE, the field takes an UNKNOWN value that must be either:
  ◦ The AArch64 view of the register number of a register that might have been used at the Exception level from which the exception was taken.
  ◦ The value 0b11111.

When the EC field is 0b000000, indicating an exception with an unknown reason, the ISS field is not valid, RES0.

**ISS encoding for exceptions with an unknown reason**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [24:0]**

Reserved, RES0.

When an exception is reported using this EC code the IL field is set to 1.

This EC code is used for all exceptions that are not covered by any other EC value. This includes exceptions that are generated in the following situations:

- The attempted execution of an instruction bit pattern that has no allocated instruction or that is not accessible at the current Exception level and Security state, including:
  ◦ A read access using a System register pattern that is not allocated for reads or that does not permit reads at the current Exception level and Security state.
  ◦ A write access using a System register pattern that is not allocated for writes or that does not permit writes at the current Exception level and Security state.
  ◦ Instruction encodings that are unallocated.
  ◦ Instruction encodings for instructions or System registers that are not implemented in the implementation.
In Debug state, the attempted execution of an instruction bit pattern that is not accessible in Debug state.

In Non-debug state, the attempted execution of an instruction bit pattern that is not accessible in Non-debug state.

In AArch32 state, attempted execution of a short vector floating-point instruction.

In an implementation that does not include Advanced SIMD and floating-point functionality, an attempted access to Advanced SIMD or floating-point functionality under conditions where that access would be permitted if that functionality was present. This includes the attempted execution of an Advanced SIMD or floating-point instruction, and attempted accesses to Advanced SIMD and floating-point System registers.

An exception generated because of the value of one of the SCTLR_EL1. {ITD, SED, CP15BEN} control bits.

Attempted execution of:
- An HVC instruction when disabled by HCR_EL2.HCD or SCR_EL3.HCE.
- An SMC instruction when disabled by SCR_EL3.SMD.
- An HLT instruction when disabled by EDSCR.HDE.

Attempted execution of an MSR or MRS instruction to access SP_EL0 when the value of SPSel.SP is 0.

Attempted execution of an MSR or MRS instruction using an _EL12 register name when HCR_EL2.E2H == 0.

Attempted execution, in Debug state, of:
- A DCPS1 instruction when the value of HCR_EL2.TGE is 1 and EL2 is disabled or not implemented in the current Security state.
- A DCPS2 instruction from EL1 or EL0 when EL2 is disabled or not implemented in the current Security state.
- A DCPS3 instruction when the value of EDSCR.SDD is 1, or when EL3 is not implemented.

When EL3 is using AArch64, attempted execution from Secure EL1 of an SRS instruction using R13 mon. See ‘Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32’.

In Debug state when the value of EDSCR.SDD is 1, the attempted execution at EL2, EL1, or EL0 of an instruction that is configured to trap to EL3.

In AArch32 state, the attempted execution of an MRS (banked register) or an MSR (banked register) instruction to SPSR_mon, SP_mon, or LR_mon.

An exception that is taken to EL2 because the value of HCR_EL2.TGE is 1 that, if the value of HCR_EL2.TGE was 0 would have been reported with an ESR_ELx.EC value of 0b000111.

### ISS encoding for an exception from a WF* instruction

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | RES0 | TI |

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
If the instruction is conditional, COND is set to the condition code field value from the instruction.

- If the instruction is unconditional, COND is set to \(0b1110\).

- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to \(0b1110\), the value for unconditional.
  - With the COND value held in the instruction.

- When a T32 instruction is trapped, it is implementation defined whether:
  - CV is set to 0 and COND is set to an unknown value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is implementation defined whether the COND field is set to \(0b1110\), or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally unknown value.

**Bits [19:2]**

Reserved, \(\text{RES0}\).

**TI, bits [1:0]**

Trapped instruction. Possible values of this bit are:

<table>
<thead>
<tr>
<th>TI</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>WFI trapped.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>WFE trapped.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>WFIT trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
<tr>
<td>0b11</td>
<td>WFET trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
</tbody>
</table>

When FEAT_WFxT is implemented, this is a two bit field as shown. Otherwise, bit[1] is \(\text{RES0}\).

On a Warm reset, this field resets to an architecturally unknown value.

The following fields describe configuration settings for generating this exception:

- SCTLR_EL1.{nTWE, nTWI}.
- HCR_EL2.{TWE, TWI}.
- SCR_EL3.{TWE, TWI}.

**ISS encoding for an exception from an MCR or MRC access**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|   CV | COND | Opc2 | Opc1 | CRn |    Rt |    CRm | Direction |

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is implementation defined whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally unknown value.
COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Opc2, bits [19:17]

The Opc2 value from the issued instruction.

For a trapped VMRS access, holds the value 0b000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Opc1, bits [16:14]

The Opc1 value from the issued instruction.

For a trapped VMRS access, holds the value 0b111.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRn, bits [13:10]

The CRn value from the issued instruction.

For a trapped VMRS access, holds the reg field from the VMRS instruction encoding.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Rt, bits [9:5]

The Rt value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRm, bits [4:1]

The CRm value from the issued instruction.

For a trapped VMRS access, holds the value 0b000.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRC or VMRS instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000011:

- **CNTKCTL_EL1**, \{EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCTEN\}, for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0** (ER, CR, SW, EN), for accesses to Performance Monitor registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0**.EN, for accesses to Activity Monitors registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**.\{TRVM, TVM\}, for accesses to virtual memory control registers from EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2**.TTLB, for execution of TLB maintenance instructions at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2**.\{TSW, TPC, TPU\} for execution of cache maintenance instructions at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2**.TACR, for accesses to the Auxiliary Control Register at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2**.TIDCP, for accesses to lockdown, DMA, and TCM operations at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HCR_EL2**.TID1, TID2, TID3, for accesses to ID registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2**.TCPAC, for accesses to **CPACR_EL1** or **CPACR** using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HSTR_EL2**.T<n>, for accesses to System registers using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CNTKCTL_EL2**.EL1PCEN, for accesses to the Generic Timer registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2**.\{TPM, TPMCR\}, for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2**.TAM, for accesses to Activity Monitors registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL3**.TAPA, for accesses to **CPACR** from EL1 and EL2, and accesses to **HCPTR** from EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- **MDCR_EL3**.TPM, for accesses to Performance Monitor registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- **CPTR_EL3**.TAM, for accesses to Activity Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- For information on other traps using EC value 0b000011, see 'Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32'.
- If FEAT_FGT is implemented, MCR or MRC access to some registers at EL0, trapped to EL2.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b0000101:

- **CPACR_EL1**.TTA for accesses to trace registers, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **MDSCR_EL1**.TDCC, for accesses to the Debug Communications Channel (DCC) registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.
- If FEAT_FGT is implemented, **MDCR_EL2**.TDCC for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3**.TDCC for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.
- **HCR_EL2**.TID0, for accesses to the **JIDR** register in the ID group 0 at EL0 and EL1 using AArch32, MRC access (coproc == 0b1110) trapped to EL2.
- **CPTR_EL2**.TTA, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.
• **MDCR_EL2.TDRA**, for accesses to Debug ROM registers **DBGDRAR** and AArch32-DBGDSAR using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDOSA**, for accesses to powerdown debug registers, using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDA**, for accesses to other debug registers, using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDOSA**, for accesses to powerdown debug registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDA**, for accesses to other debug registers, using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b001000:

• **HCR_EL2.TID0**, for accesses to the **FPSID** register in ID group 0 at EL1 using AArch32 state, VMRS access trapped to EL2.

• **HCR_EL2.TID3**, for accesses to registers in ID group 3 including **MVFR0**, **MVFR1** and **MVFR2**, VMRS access trapped to EL2.

## ISS encoding for an exception from an LD64B or ST64B* instruction

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
<th>ISS</th>
</tr>
</thead>
</table>

### ISS, bits [24:0]

<table>
<thead>
<tr>
<th>ISS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000000000000000000000000</td>
<td>ST64BV instruction trapped.</td>
</tr>
<tr>
<td>0b0000000000000000000000001</td>
<td>ST64BV0 instruction trapped.</td>
</tr>
<tr>
<td>0b0000000000000000000000010</td>
<td>LD64B or ST64B instruction trapped.</td>
</tr>
</tbody>
</table>

All other values are reserved.

## ISS encoding for an exception from an MCRR or MRRC access

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
<th>CV</th>
<th>COND</th>
<th>Opc1</th>
<th>RES0</th>
<th>Rt2</th>
<th>Rt</th>
<th>CRm</th>
<th>Direction</th>
</tr>
</thead>
</table>

### CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

• When an A32 instruction is trapped, CV is set to 1.

• When a T32 instruction is trapped, it is IMPLEMENTATIONDEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.
The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to $0b1110$.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to $0b1110$, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to $0b1110$, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Opc1, bits [19:16]**

The Opc1 value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [15]**

Reserved, RES0.

**Rt2, bits [14:10]**

The Rt2 value from the issued instruction, the second general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Rt, bits [9:5]**

The Rt value from the issued instruction, the first general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCRR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRCC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000100:

- **CNTKCTL_EL1**, {EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCTEN}, for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0**, {CR, EN}, for accesses to Performance Monitor registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0**, {EN}, for accesses to Activity Monitors registers AMEVCNTR0<n> and AMEVCNTR1<n> from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**, {TRVM, TVM}, for accesses to virtual memory control registers from EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **PMUSERENR_EL0**, {CR, EN}, for accesses to Performance Monitor registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0**, {EN}, for accesses to Activity Monitors registers AMEVCNTR0<n> and AMEVCNTR1<n> from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**, {TRVM, TVM}, for accesses to virtual memory control registers from EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2**, {TPM, TPMCR}, for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2**, {TAM}, for accesses to Activity Monitors registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL3**, {TPM, TPMCR}, for accesses to Performance Monitor registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.
- **CPTR_EL3**, {TAM}, for accesses to Activity Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.

If FEAT_FGT is implemented, **HDFGRTR_EL2**, PMCCNTR_EL0 for MRRC access and **HDFGWTR_EL2**, PMCCNTR_EL0 for MCRR access to PMCCNTR at EL0, trapped to EL2.

The following sections describe configuration settings for generating exceptions that are reported using EC value 0b001100:

- **MDSCR_EL1**, {TDCC}, for accesses to the Debug ROM registers DBGDSAR and DBGDRAR at EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **MDCR_EL2**, {TDRA}, for accesses to Debug ROM registers DBGDRAR and AArchDBGDSAR using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **MDCR_EL3**, {TDA}, for accesses to debug registers, using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.
- **CPACR_EL1**, {TTA}, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **CPTR_EL2**, {TTA}, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **CPTR_EL3**, {TTA}, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.

### Note

If the Armv8-A architecture is implemented with an ETMv4 implementation, MCRR and MRRC accesses to trace registers are **UNDEFINED** and the resulting exception is higher priority than an exception due to these traps.

### ISS encoding for an exception from an LDC or STC instruction

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>imm8</th>
<th>RES0</th>
<th>Rn</th>
<th>Offset</th>
<th>AM</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>CV</td>
<td>COND</td>
<td>imm8</td>
<td>RES0</td>
<td>Rn</td>
<td>Offset</td>
<td>AM</td>
<td>Direction</td>
</tr>
</tbody>
</table>

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.
For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**imm8, bits [19:12]**

The immediate value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [11:10]**

Reserved, RES0.

**Rn, bits [9:5]**

The Rn value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

This field is valid only when AM[2] is 0, indicating an immediate form of the LDC or STC instruction. When AM[2] is 1, indicating a literal form of the LDC or STC instruction, this field is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Offset, bit [4]**

Indicates whether the offset is added or subtracted:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Subtract offset.</td>
</tr>
<tr>
<td>0b1</td>
<td>Add offset.</td>
</tr>
</tbody>
</table>

This bit corresponds to the U bit in the instruction encoding.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**AM, bits [3:1]**

Addressing mode. The permitted values of this field are:

<table>
<thead>
<tr>
<th>AM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Immediate unindexed.</td>
</tr>
<tr>
<td>0b01</td>
<td>Immediate post-indexed.</td>
</tr>
<tr>
<td>0b10</td>
<td>Immediate offset.</td>
</tr>
<tr>
<td>0b11</td>
<td>Immediate pre-indexed.</td>
</tr>
<tr>
<td>0b100</td>
<td>For a trapped STC instruction or a trapped T32 LDC instruction this encoding is reserved.</td>
</tr>
<tr>
<td>0b110</td>
<td>For a trapped STC instruction, this encoding is reserved.</td>
</tr>
</tbody>
</table>

The values 0b101 and 0b111 are reserved. The effect of programming this field to a reserved value is that behavior is **CONSTRAINED UNPREDICTABLE**, as described in 'Reserved values in System and memory-mapped registers and translation table entries'.

Bit [2] in this subfield indicates the instruction form, immediate or literal.

Bits [1:0] in this subfield correspond to the bits \{P, W\} in the instruction encoding.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to memory. STC instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from memory. LDC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following fields describe the configuration settings for the traps that are reported using EC value 0b000010:

- **MDSCR_EL1.TDCC**, for accesses using AArch32 state, LDC access to DBGDTRTXint or STC access to DBGDTRRXint trapped to EL1 or EL2.
- **MDCR_EL2.TDA**, for accesses using AArch32 state, LDC access to DBGDTRTXint or STC access to DBGDTRRXint MCR or MRC access trapped to EL2.
- **MDCR_EL3.TDA**, for accesses using AArch32 state, LDC access to DBGDTRTXint or STC access to DBGDTRRXint MCR or MRC access trapped to EL3.
- If FEAT_FGT is implemented, **MDCR_EL2.TDCC** for LDC and STC accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

**ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality, resulting from the FPEN and TFP traps**

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>RES0</th>
</tr>
</thead>
</table>

The accesses covered by this trap include:

- Execution of SVE or Advanced SIMD and floating-point instructions.
- Accesses to the Advanced SIMD and floating-point System registers.

For an implementation that does not include either SVE or support for floating-point and Advanced SIMD, the exception is reported using the EC value 0b000000.

**CV, bit [24]**

Condition code valid.
<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:0]**

Reserved, RES0.

The following sections describe the configuration settings for the traps that are reported using EC value 0b000011:

- CPACR_EL1.FPEN, for accesses to SIMD and floating-point registers trapped to EL1.
- CPTR_EL2.TFP, for accesses to SIMD and floating-point registers trapped to EL2.
- CPTR_EL3.TFP, for accesses to SIMD and floating-point registers trapped to EL3.

**ISS encoding for an exception from an access to SVE functionality, resulting from CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ**

|   | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|   |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

The accesses covered by this trap include:

- Execution of SVE instructions.
- Accesses to the SVE System register, ZCR_ELx.

For an implementation that does not include SVE, the exception is reported using the EC value 0b000000.
The following sections describe the configuration settings for the traps that are reported using EC value 0b011001:

- **CPACR_EL1.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0 or EL1, trapped to EL2.
- **CPTR_EL2.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL2.TZ**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL3.EZ**, for execution of SVE instructions and accesses to SVE registers from all Exception levels, trapped to EL3.

**ISS encoding for an exception from an Illegal Execution state, or a PC or SP alignment fault**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
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<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
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</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td>RES0</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [24:0]**

Reserved, RES0.

There are no configuration settings for generating Illegal Execution state exceptions and PC alignment fault exceptions. For more information about these exceptions, see ‘The Illegal Execution state exception’ and ‘PC alignment checking’.

‘SP alignment checking’ describes the configuration settings for generating SP alignment fault exceptions.

**ISS encoding for an exception from HVC or SVC instruction execution**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td>imm16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [24:16]**

Reserved, RES0.

**imm16, bits [15:0]**

The value of the immediate field from the HVC or SVC instruction.

For an HVC instruction, and for an A64 SVC instruction, this is the value of the imm16 field of the issued instruction.

For an A32 or T32 SVC instruction:

- If the instruction is unconditional, then:
  - For the T32 instruction, this field is zero-extended from the imm8 field of the instruction.
  - For the A32 instruction, this field is the bottom 16 bits of the imm24 field of the instruction.
- If the instruction is conditional, this field is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

In AArch32 state, the HVC instruction is unconditional, and a conditional SVC instruction generates an exception only if it passes its condition code check. Therefore, the syndrome information for these exceptions does not require conditionality information.

For T32 and A32 instructions, see ‘SVC’ and ‘HVC’.

For A64 instructions, see ‘SVC’ and ‘HVC’.
If FEAT_FGT is implemented, \texttt{HFGITR_EL2} \{SVC\_EL1, SVC\_EL0\} control fine-grained traps on SVC execution.

**ISS encoding for an exception from SMC instruction execution in AArch32 state**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | CCKNOWNPASS | RES0 |

For an SMC instruction that completes normally and generates an exception that is taken to EL3, the ISS encoding is \texttt{RES0}.

For an SMC instruction that is trapped to EL2 from EL1 because \texttt{HCR\_EL2}.TSC is 1, the ISS encoding is as shown in the diagram.

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0}</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>\texttt{0b1}</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is \texttt{IMPLEMENTATION DEFINED} whether CV is set to 1 or set to 0. See the description of the COND field for more information.

This field is valid only if CCKNOWNPASS is 1, otherwise it is \texttt{RES0}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to \texttt{0b1110}.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to \texttt{0b1110}.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to \texttt{0b1110}, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is \texttt{IMPLEMENTATION DEFINED} whether:
  - CV is set to 0 and COND is set to an \texttt{UNKNOWN} value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is \texttt{IMPLEMENTATION DEFINED} whether the COND field is set to \texttt{0b1110}, or to the value of any condition that applied to the instruction.

This field is valid only if CCKNOWNPASS is 1, otherwise it is \texttt{RES0}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.
**CCKNOWNPASS, bit [19]**

Indicates whether the instruction might have failed its condition code check.

<table>
<thead>
<tr>
<th>CCKNOWNPASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The instruction was unconditional, or was conditional and passed its condition code check.</td>
</tr>
<tr>
<td>0b1</td>
<td>The instruction was conditional, and might have failed its condition code check.</td>
</tr>
</tbody>
</table>

**Note**

In an implementation in which an SMC instruction that fails its code check is not trapped, this field can always return the value 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [18:0]**

Reserved, **RES0**.

HCR_EL2.TSC describes the configuration settings for trapping SMC instructions to EL2.

‘System calls’ describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from SMC instruction execution in AArch64 state**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| imm16 | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Bits [24:16]**

Reserved, **RES0**.

**imm16, bits [15:0]**

The value of the immediate field from the issued SMC instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The value of ISS[24:0] described here is used both:

- When an SMC instruction is trapped from EL1 modes.
- When an SMC instruction is not trapped, so completes normally and generates an exception that is taken to EL3.

HCR_EL2.TSC describes the configuration settings for trapping SMC from EL1 modes.

‘System calls’ describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from MSR, MRS, or System instruction execution in AArch64 state**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Op0 | Op2 | Op1 | CRn | | Rt | | CRm | | | | | | | | | | | | | | | | | | | |

**Bits [24:22]**

Reserved, **RES0**.
Op0, bits [21:20]
The Op0 value from the issued instruction.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Op2, bits [19:17]
The Op2 value from the issued instruction.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Op1, bits [16:14]
The Op1 value from the issued instruction.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRn, bits [13:10]
The CRn value from the issued instruction.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Rt, bits [9:5]
The Rt value from the issued instruction, the general-purpose register used for the transfer.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

CRm, bits [4:1]
The CRm value from the issued instruction.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Direction, bit [0]
Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write access, including MSR instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read access, including MRS instructions.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For exceptions caused by System instructions, see 'System instructions' subsection of 'Branches, exception generating and System instructions' for the encoding values returned by an instruction.

The following fields describe configuration settings for generating the exception that is reported using EC value 0b011000:

- **SCTLR_EL1.UCI**, for execution of cache maintenance instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.UCT**, for accesses to **CTR_EL0** using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.DZE**, for execution of DC ZVA instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.UMA**, for accesses to the PSTATE interrupt masks using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **CPACR_EL1.TTA**, for accesses to the trace registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **MDSCR_EL1.TDCC**, for accesses to the Debug Communications Channel (DCC) registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
If FEAT_FGT is implemented, MDCR_EL2.TDCC for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and MDCR_EL3.TDCC for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

CNTKCTL_EL1.EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCTEN accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.

PMUSERENR_EL0.ER, CR, SW, EN, for accesses to the Performance Monitor registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.

AMUSERENR_EL0.EN, for accesses to Activity Monitors registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.

HCR_EL2.TRVM, TVM, for accesses to virtual memory control registers using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TDZ, for execution of DC ZVA instructions using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TTLB, for execution of TLB maintenance instructions using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TSW, TPC, TPU, for execution of cache maintenance instructions using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.ACTLR, for accesses to the Auxiliary Control Register, ACTLR_EL1, using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TIDCP, for accesses to lockdown, DMA, and TCM operations using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TID1, TID2, TID3, for accesses to ID group 1, ID group 2 or ID group 3 registers, using AArch64 state, MSR or MRS access trapped to EL2.

CPTR_EL2.TTCPAC, for accesses to CPACR_EL1, using AArch64 state, MSR or MRS access trapped to EL2.

CPTR_EL2.TTA, for accesses to the trace registers, using AArch64 state, MSR or MRS access trapped to EL2.

MDCR_EL2.TTRF, for accesses to the trace filter control register, TRFCR_EL1, using AArch64 state, MSR or MRS access trapped to EL2.

MDCR_EL2.TDRA, for accesses to Debug ROM registers, using AArch64 state, MSR or MRS access trapped to EL2.

MDCR_EL2.TDOSA, for accesses to powerdown debug registers using AArch64 state, MSR or MRS access trapped to EL2.

CNTHCTL_EL2.EL1PCEN, EL1PCTEN, for accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL2.

CPTR_EL2.TAM, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.APK, for accesses to Pointer authentication key registers, using AArch64 state, MSR or MRS access trapped to EL2.

HCR_EL2.TERR, FIEN, for accesses to RAS registers, using AArch64 state, MSR or MRS access trapped to EL2.

MDCR_EL3.TTPM, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL2.TTTRF, for accesses to the trace filter control registers, TRFCR_EL1 and TRFCR_EL2, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TDA, for accesses to debug registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL2.TDOSA, for accesses to powerdown debug registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL2.TPM, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL3.

MDCR_EL3.TAM, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access trapped to EL3.
• If FEAT_EVT is implemented, the following registers control traps for EL1 and EL0 Cache controls that use this EC value:
  ◦ **HCR_EL2**. {TTLBOS, TTLBIS, TICAB, TOCU, TID4}.
  ◦ **HCR2**. {TTLBIS, TICAB, TOCU, TID4}.

• If FEAT_FGT is implemented:
  ◦ **SCR_EL3.FGTEn**, for accesses to the fine-grained trap registers, MSR or MRS access at EL2 trapped to EL3.
  ◦ **HFGRTR_EL2** for reads and **HFGWTR_EL2** for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 trapped to EL2.
  ◦ **HFGITR_EL2** for execution of system instructions, MSR or MRS access trapped to EL2.
  ◦ **HDFGRTR_EL2** for reads and **HDFGWTR_EL2** for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 state trapped to EL2.
  ◦ **HAFGRTR_EL2** for reads of Activity Monitor counters, using AArch64 state, MRS access at EL0 and EL1 trapped to EL2.

### ISS encoding for an IMPLEMENTATION DEFINED exception to EL3

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |

**IMPLEMENTATION DEFINED**, bits [24:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### ISS encoding for an exception from an Instruction Abort

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SET | FnVEA | RES0 | S1PTW | RES0 | IFSC |

**Bits [24:13]**

Reserved, **RES0**.

**SET, bits [12:11]**

When **FEAT_RAS** is implemented:

Synchronous Error Type. When IFSC is 0b010000, describes the PE error state after taking the Instruction Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Note**

Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the IFSC code is 0b010000. It is **RES0** for all other aborts.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.
**FnV, bit [10]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an <strong>UNKNOWN</strong> value.</td>
</tr>
</tbody>
</table>

This field is valid only if the IFSC code is **0b010000**. It is **RES0** for all other aborts.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EA, bit [9]**

External abort type. This bit can provide an **IMPLEMENTATION DEFINED** classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [8]**

Reserved, **RES0**.

**S1PTW, bit [7]**

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [6]**

Reserved, **RES0**.

**IFSC, bits [5:0]**

Instruction Fault Status Code.
<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 0.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td></td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b101001</td>
<td>Address size fault, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
</tbody>
</table>
When FEAT_LPA2 is implemented

0b110000 TLB conflict abort.

0b110001 Unsupported atomic hardware update fault.

When FEAT_HAFDBS is implemented

All other values are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults’.

Note

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS encoding for an exception from a Data Abort

| Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 0      | 1      |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        | ISS  |

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this ISS encoding includes ISS2, bits[36:32].

ISV, bit [24]

Instruction Syndrome Valid. Indicates whether the syndrome information in ISS[23:14] is valid.

<table>
<thead>
<tr>
<th>ISV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No valid instruction syndrome. ISS[23:14] are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>ISS[23:14] hold a valid instruction syndrome.</td>
</tr>
</tbody>
</table>

In ESR_EL2, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

For other faults reported in ESR_EL2, ISV is 0 except for the following stage 2 aborts:

- AArch64 loads and stores of a single general-purpose register (including the register specified with 0b111111, including those with Acquire/Release semantics, but excluding Load Exclusive or Store Exclusive and excluding those with writeback).
- AArch32 instructions where the instruction:
  - Is an LDR, LDA, LDRH, LDRSH, LDRSHT, LDRH, LDAH, LDRHT, LDRSB, LDRSBT, LDRB, LDAB, LDRBT, STR, ST, STRT, STRH, STLH, STRHT, STRB, STL, or STRBT instruction.
  - Is not performing register writeback.
  - Is not using R15 as a source or destination register.

For these stage 2 aborts, ISV is UNKNOWN if the exception was generated in Debug state in memory access mode, and otherwise indicates whether ISS[23:14] hold a valid syndrome.

For faults reported in ESR_EL1 or ESR_EL3, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault. ISV is 0 for all other faults reported in ESR_EL1 or ESR_EL3.

When FEAT_RAS is implemented, ISV is 0 for any synchronous External abort.

For ISS reporting, a stage 2 abort on a stage 1 translation table walk does not return a valid instruction syndrome, and therefore ISV is 0 for these aborts.
When FEAT_RAS is not implemented, it is \textit{IMPLEMENTATION DEFINED} whether ISV is set to 1 or 0 on a synchronous External abort on a stage 2 translation table walk.

When FEAT_MTE is implemented, for a synchronous Tag Check Fault abort taken to ELx, ESR_ELx.FNV is 0 and FAR_ELx is valid.

On a Warm reset, this field resets to an architecturally \textit{UNKNOWN} value.

\textbf{SAS, bits [23:22]}

\textbf{When ISV == \textquoteleft\textquoteleft 1\textquoteright\textquoteright:}

Syndrome Access Size. Indicates the size of the access attempted by the faulting operation.

\begin{tabular}{|c|c|}
\hline
\textbf{SAS} & \textbf{Meaning} \\
\hline
0b0 & Byte \\
0b01 & Halfword \\
0b10 & Word \\
0b11 & Doubleword \\
\hline
\end{tabular}

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0b11.

This field is \textit{UNKNOWN} when the value of ISV is \textit{UNKNOWN}.

On a Warm reset, this field resets to an architecturally \textit{UNKNOWN} value.

\textbf{Otherwise:}

Reserved, RES0.

\textbf{SSE, bit [21]}

\textbf{When ISV == \textquoteleft\textquoteleft 1\textquoteright\textquoteright:}

Syndrome Sign Extend. For a byte, halfword, or word load operation, indicates whether the data item must be sign extended.

\begin{tabular}{|c|c|}
\hline
\textbf{SSE} & \textbf{Meaning} \\
\hline
0b0 & Sign-extension not required. \\
0b1 & Data item must be sign-extended. \\
\hline
\end{tabular}

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

For all other operations, this field is 0.

This field is \textit{UNKNOWN} when the value of ISV is \textit{UNKNOWN}.

On a Warm reset, this field resets to an architecturally \textit{UNKNOWN} value.

\textbf{Otherwise:}

Reserved, RES0.

\textbf{SRT, bits [20:16]}

\textbf{When ISV == \textquoteleft\textquoteleft 1\textquoteright\textquoteright:}

Syndrome Register Transfer. When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xt.
If the exception was taken from an Exception level that is using AArch32, then this is the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**SF, bit [15]**

**When ISV == ‘1’:**

Width of the register accessed by the instruction is Sixty-Four.

<table>
<thead>
<tr>
<th>SF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction loads/stores a 32-bit wide register.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction loads/stores a 64-bit wide register.</td>
</tr>
</tbody>
</table>

**Note**

This field specifies the register width identified by the instruction, not the Execution state.

When **FEAT_LS64** is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 1.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**AR, bit [14]**

**When ISV == ‘1’:**

Acquire/Release.

<table>
<thead>
<tr>
<th>AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction did not have acquire/release semantics.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction did have acquire/release semantics.</td>
</tr>
</tbody>
</table>

When **FEAT_LS64** is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.
VNCR, bit [13]

When FEAT_NV2 is implemented:

Indicates that the fault came from use of VNCR_EL2 register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault was not generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault was generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
</tbody>
</table>

This field is 0 in ESR_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

SET, bits [12:11]

When FEAT_RAS is implemented and FEAT_LS64 is not implemented:

Synchronous Error Type. When DFSC is 0b010000, describes the PE error state after taking the Data Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the DFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When FEAT_LS64 is implemented:

Load/Store Type. Used when an LD64B, ST64B, ST64BV, or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

<table>
<thead>
<tr>
<th>LST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>An ST64BV instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b10</td>
<td>An LD64B or ST64B instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b11</td>
<td>An ST64BV0 instruction generated the Data Abort.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is valid only if the DFSC code is 0b110101. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
**FnV, bit [10]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an <strong>UNKNOWN</strong> value.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is **0b010000**. It is **RES0** for all other aborts.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EA, bit [9]**

External abort type. This bit can provide an **IMPLEMENTATION DEFINED** classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CM, bit [8]**

Cache maintenance. Indicates whether the Data Abort came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Data Abort was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Data Abort was generated by either the execution of a cache maintenance instruction or by a synchronous fault on the execution of an address translation instruction. The <strong>DC ZVA</strong>, <strong>DC GVA</strong>, and <strong>DC GZVA</strong> instructions are not classified as cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**S1PTW, bit [7]**

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**WnR, bit [6]**

Write not Read. Indicates whether a synchronous abort was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For faults on cache maintenance and address translation instructions, this bit always returns a value of 1.
For faults from an atomic instruction that both reads and writes from a memory location, this bit is set to 0 if a read of the address specified by the instruction would have generated the fault which is being reported, otherwise it is set to 1. The architecture permits, but does not require, a relaxation of this requirement such that for all stage 2 aborts on stage 1 translation table walks for atomic instructions, the WnR bit is always 0.

This field is UNKNOWN for:

- An External abort on an Atomic access.
- A fault reported using a DFSC value of \(0b110101\) or \(0b110001\), indicating an unsupported Exclusive or atomic access.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DFSC, bits [5:0]**

Data Fault Status Code.
<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 0.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td></td>
</tr>
<tr>
<td>0b010001</td>
<td>Synchronous Tag Check Fault.</td>
<td>When FEAT_MTE is implemented</td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>
0b100001 Alignment fault.
0b101001 Address size fault, level -1. When FEAT_LPA2 is implemented
0b101011 Translation fault, level -1. When FEAT_LPA2 is implemented
0b110000 TLB conflict abort.
0b110001 Unsupported atomic hardware update fault. When FEAT_HAFDBS is implemented
0b110100 IMPLEMENTATION DEFINED fault (Lockdown).
0b110101 IMPLEMENTATION DEFINED fault (Unsupported Exclusive or Atomic access).

All other values are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults’.

Note

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS encoding for an exception from a trapped floating-point exception

24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RES0 TFV RES0 VECITR IDF RES0 I XF U FF OFF DZF IOF

Bit [24]

Reserved, RES0.

TFV, bit [23]

Trapped Fault Valid bit. Indicates whether the IDF, IXF, UFF, OFF, DZF, and IOF bits hold valid information about trapped floating-point exceptions.

<table>
<thead>
<tr>
<th>TFV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The IDF, IXF, UFF, OFF, DZF, and IOF bits do not hold valid information about trapped floating-point exceptions and are UNKNOWN.</td>
</tr>
<tr>
<td>0b1</td>
<td>One or more floating-point exceptions occurred during an operation performed while executing the reported instruction. The IDF, IXF, UFF, OFF, DZF, and IOF bits indicate trapped floating-point exceptions that occurred. For more information, see ‘Floating-point exceptions and exception traps’.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field is set to 0 on an exception generated by a trapped floating point exception from a vector instruction.

Note

This is not a requirement. Implementations can set this field to 1 on a trapped floating-point exception from a vector instruction and return valid information in the {IDF, IXF, UFF, OFF, DZF, IOF} fields.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [22:11]**

Reserved, **RES0**.

**VECITR, bits [10:8]**

For a trapped floating-point exception from an instruction executed in AArch32 state this field is **RES1**.

For a trapped floating-point exception from an instruction executed in AArch64 state this field is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IDF, bit [7]**

Input Denormal floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IDF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input denormal floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input denormal floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [6:5]**

Reserved, **RES0**.

**IXF, bit [4]**

Inexact floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IXF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inexact floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inexact floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**UFF, bit [3]**

Underflow floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>UFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**OFF, bit [2]**

Overflow floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>OFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Overflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DZF, bit [1]**

Divide by Zero floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>DZF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Divide by Zero floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Divide by Zero floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IOF, bit [0]**

Invalid Operation floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IOF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalid Operation floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalid Operation floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

In an implementation that supports the trapping of floating-point exceptions:

- From an Exception level using AArch64, the FPCR.{IDE, IXE, UFE, OFE, DZE, IOE} bits enable each of the floating-point exception traps.
- From an Exception level using AArch32, the FPSCR.{IDE, IXE, UFE, OFE, DZE, IOE} bits enable each of the floating-point exception traps.

**ISS encoding for an SError interrupt**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IDS</td>
<td>RES0</td>
<td>IESB</td>
<td>AET</td>
<td>EA</td>
<td>RES0</td>
<td>DFSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**IDS, bit [24]**

IMPLEMENTATION DEFINED syndrome.

<table>
<thead>
<tr>
<th>IDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits [23:0] of the ISS field holds the fields described in this encoding.</td>
</tr>
</tbody>
</table>

**Note**

If FEAT_RAS is not implemented, bits [23:0] of the ISS field are RES0.

| 0b1 | Bits [23:0] of the ISS field holds IMPLEMENTATION DEFINED syndrome information that can be used to provide additional information about the SError interrupt. |

**Note**

This field was previously called ISV.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [23:14]**

Reserved, RES0.
IESB, bit [13]

When FEAT_IESB is implemented:

Implicit error synchronization event.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The SError interrupt was either not synchronized by the implicit error synchronization event or not taken immediately.</td>
</tr>
<tr>
<td>0b1</td>
<td>The SError interrupt was synchronized by the implicit error synchronization event and taken immediately.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

AET, bits [12:10]

When FEAT_RAS is implemented:

Asynchronous Error Type.

When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception.

<table>
<thead>
<tr>
<th>AET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b001</td>
<td>Unrecoverable state (UEU).</td>
</tr>
<tr>
<td>0b010</td>
<td>Restartable state (UEO).</td>
</tr>
<tr>
<td>0b011</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b110</td>
<td>Corrected (CE).</td>
</tr>
</tbody>
</table>

All other values are reserved.

If multiple errors are taken as a single SError interrupt exception, the overall PE error state is reported.

Note

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EA, bit [9]

When FEAT_RAS is implemented:

External abort type. When DFSC is 0b010001, provides an IMPLEMENTATION DEFINED classification of External aborts.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**Bits [8:6]**

Reserved, RES0.

**DFSC, bits [5:0]**

*When FEAT_RAS is implemented:*

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Uncategorized error.</td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**ISS encoding for an exception from a Breakpoint or Vector Catch debug exception**

| 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| IFSC|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [24:6]**

Reserved, RES0.

**IFSC, bits [5:0]**

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For more information about generating these exceptions:

- For exceptions from AArch64, see 'Breakpoint exceptions'.
- For exceptions from AArch32, see 'Breakpoint exceptions' and 'Vector Catch exceptions'.

**ISS encoding for an exception from a Software Step exception**

| 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| ISV | RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| EX  |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| IFSC|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**ISV, bit [24]**

Instruction syndrome valid. Indicates whether the EX bit, ISS[6], is valid, as follows:
See the EX bit description for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [23:7]**

Reserved, RES0.

**EX, bit [6]**

Exclusive operation. If the ISV bit is set to 1, this bit indicates whether a Load-Exclusive instruction was stepped.

<table>
<thead>
<tr>
<th>EX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An instruction other than a Load-Exclusive instruction was stepped.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Load-Exclusive instruction was stepped.</td>
</tr>
</tbody>
</table>

If the ISV bit is set to 0, this bit is RES0, indicating no syndrome data is available.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IFSC, bits [5:0]**

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see 'Software Step exceptions'.

**ISS encoding for an exception from a Watchpoint exception**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0 RES0VNCR RES0 CM RES0WnR DFSC</td>
</tr>
</tbody>
</table>

**Bits [24:15]**

Reserved, RES0.

**Bit [14]**

Reserved, RES0.

**VNCR, bit [13]**

When FEAT_NV2 is implemented:

Indicates that the watchpoint came from use of VNCR_EL2 register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The watchpoint was not generated by the use of VNCR_EL2 by EL1 code.</td>
</tr>
<tr>
<td>0b1</td>
<td>The watchpoint was generated by the use of VNCR_EL2 by EL1 code.</td>
</tr>
</tbody>
</table>

This field is 0 in ESR_EL1.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**Bits [12:9]**

Reserved, **RES0**.

**CM, bit [8]**

Cache maintenance. Indicates whether the Watchpoint exception came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Watchpoint exception was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Watchpoint exception was generated by either the execution of a cache maintenance instruction or by a synchronous Watchpoint exception on the execution of an address translation instruction. The <strong>DC ZVA</strong>, <strong>DC GVA</strong>, and <strong>DC GZVA</strong> instructions are not classified as a cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [7]**

Reserved, **RES0**.

**WnR, bit [6]**

Write not Read. Indicates whether the Watchpoint exception was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint exception caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint exception caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For Watchpoint exceptions on cache maintenance and address translation instructions, this bit always returns a value of 1.

For Watchpoint exceptions from an atomic instruction, this field is set to 0 if a read of the location would have generated the Watchpoint exception, otherwise it is set to 1.

If multiple watchpoints match on the same access, it is **UNPREDICTABLE** which watchpoint generates the Watchpoint exception.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DFSC, bits [5:0]**

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
For more information about generating these exceptions, see 'Watchpoint exceptions'.

**ISS encoding for an exception from execution of a Breakpoint instruction**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0 Comment</td>
</tr>
</tbody>
</table>

**Bits [24:16]**

Reserved, RES0.

**Comment, bits [15:0]**

Set to the instruction comment field value, zero extended as necessary.
For the AArch32 BKPT instructions, the comment field is described as the immediate field.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
For more information about generating these exceptions, see 'Breakpoint instruction exceptions'.

**ISS encoding for an exception from an ERET, ERETA, or ERETAB instruction**

<table>
<thead>
<tr>
<th>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0 ERET ERETA</td>
</tr>
</tbody>
</table>

This EC value applies when FEAT_FGT is implemented, or when HCR_EL2.NV is 1.

**Bits [24:2]**

Reserved, RES0.

**ERET, bit [1]**

Indicates whether an ERET or ERETA* instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERET instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETA or ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

If this bit is 0, the ERETA field is RES0.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ERETA, bit [0]**

Indicates whether an ERETA or ERETAB instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERETA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERETA instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

When the ERET field is 0, this bit is RES0.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
For more information about generating these exceptions, see HCR_EL2.NV.
If FEAT_FGT is implemented, HFGITR_EL2.ERET controls fine-grained trap exceptions from ERET, ERETA and ERETAB execution.
ISS encoding for an exception from Branch Target Identification instruction

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    | BTYPE |

Bits [24:2]

Reserved, RES0.

BTYPE, bits [1:0]

This field is set to the PSTATE.BTYPE value that generated the Branch Target Exception.

For more information about generating these exceptions, see ‘The AArch64 application level programmers model’.

ISS encoding for an exception from a Pointer Authentication instruction when HCR_EL2.API == 0 || SCR_EL3.API == 0

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    |    |

Bits [24:0]

Reserved, RES0.

For more information about generating these exceptions, see:

- HCR_EL2.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL2.
- SCR_EL3.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL3.

ISS encoding for an exception from a Pointer Authentication instruction authentication failure

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td>Exception as a result of an Instruction key or a Data key</td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:2]

Reserved, RES0.

Bit [1]

This field indicates whether the exception is as a result of an Instruction key or a Data key.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>Instruction Key.</th>
<th>0b1</th>
<th>Data Key.</th>
</tr>
</thead>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Bit [0]**

This field indicates whether the exception is as a result of an A key or a B key.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0     | A key.  
| 0b1     | B key.  

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following instructions generate an exception when the Pointer Authentication Code (PAC) is incorrect:

- AUTIASP, AUTIAZ, AUTIA1716.
- AUTIBSP, AUTIBZ, AUTIB1716.
- AUTIA, AUTDA, AUTIB, AUTDB.
- AUTIZA, AUTIZB, AUTDZA, AUTDZB.

It is **IMPLEMENTATION DEFINED** whether the following instructions generate an exception directly from the authorization failure, rather than changing the address in a way that will generate a translation fault when the address is accessed:

- RETAA, RETAB.
- BRAA, BRAB, BLRAA, BLRAB.
- BRAAZ, BRABZ, BLRAAZ, BLRABZ.
- ERETA, ERETAB.
- LDRAA, LDRAB, whether the authenticated address is written back to the base register or not.

**Accessing the ESR_EL2**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL2 using the mnemonic ESR_EL2 or ESR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, ESR_EL2**

```plaintext
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return ESR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return ESR_EL2;
elsif PSTATE.EL == EL3 then
    return ESR_EL2;

MSR ESR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
      ESR_EL1 = X[t];
   elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
   elsif PSTATE.EL == EL2 then
      ESR_EL2 = X[t];
   elsif PSTATE.EL == EL3 then
      ESR_EL2 = X[t];

MRS <Xt>, ESR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.TRVM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ESR_EL1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x138];
   else
      return ESR_EL1;
   elsif PSTATE.EL == EL2 then
      if HCR_EL2.E2H == '1' then
         return ESR_EL2;
      else
         return ESR_EL1;
      elsif PSTATE.EL == EL3 then
         return ESR_EL1;

MSR ESR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.TVM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ESR_EL1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      NVMem[0x138] = X[t];
   else
      ESR_EL1 = X[t];
   elsif PSTATE.EL == EL2 then
      if HCR_EL2.E2H == '1' then
         ESR_EL2 = X[t];
      else
         ESR_EL1 = X[t];
      elseif PSTATE.EL == EL3 then
         ESR_EL1 = X[t];
ESR_EL3, Exception Syndrome Register (EL3)

The ESR_EL3 characteristics are:

Purpose

Holds syndrome information for an exception taken to EL3.

Configuration

This register is present only when EL3 is implemented. Otherwise, direct accesses to ESR_EL3 are UNDEFINED.

Attributes

ESR_EL3 is a 64-bit register.

Field descriptions

The ESR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

ESR_EL3 is made UNKNOWN as a result of an exception return from EL3.

When an UNPREDICTABLE instruction is treated as UNDEFINED, and the exception is taken to EL3, the value of ESR_EL3 is UNKNOWN. The value written to ESR_EL3 must be consistent with a value that could be created as a result of an exception from the same Exception level that generated the exception as a result of a situation that is not UNPREDICTABLE at that Exception level, in order to avoid the possibility of a privilege violation.

Bits [63:37]

Reserved, RES0.

ISS2, bits [36:32]

When FEAT_LS64 is implemented:

If a memory access generated by an ST64BV or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xs.

For any other Data Abort, this field is RES0.

Otherwise:

Reserved, RES0.

EC, bits [31:26]

Exception Class. Indicates the reason for the exception that this register holds information about.

For each EC value, the table references a subsection that gives information about:

- The cause of the exception, for example the configuration required to enable the trap.
- The encoding of the associated ISS.
Possible values of the EC field are:
<table>
<thead>
<tr>
<th>EC</th>
<th>Meaning</th>
<th>ISS encoding for exceptions with an unknown reason</th>
<th>ISS encoding for an exception from a WF* instruction</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Unknown reason.</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Trapped WF* instruction execution. Conditional WF* instructions that fail their condition code check do not cause an exception.</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Trapped MCR or MRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Trapped MCRR or MRRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Trapped MCR or MRC access with (coproc==0b1110).</td>
<td>ISS encoding for an exception from an MCR or MRC access</td>
<td>When AArch32 is supported at any Exception level</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Trapped LDC or STC access. The only architected uses of these instruction are: • An STC to write data to memory from DBGDTRRXint. • An LDC to read data from memory to DBGDTRTXint.</td>
<td>ISS encoding for an exception from an LDC or STC instruction</td>
<td>When AArch32 is supported at any Exception level</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Access to SVE, Advanced SIMD or floating-point functionality trapped by CPACR_EL1,FPEN, CPTR_EL2,FPEN, CPTR_EL2,TFP, or CPTR_EL3,TFP control. Excludes exceptions resulting from CPACR_EL1 when the value of HCR_EL2,TGE is 1, or because SVE or Advanced SIMD and floating-point are not implemented. These are reported with EC value 0b000000 as described in 'The EC used to report an exception routed to</td>
<td>ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality resulting from the FPEN and TFP traps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Code</td>
<td>Description</td>
<td>Condition</td>
<td>Exception Level</td>
<td></td>
</tr>
<tr>
<td>------------</td>
<td>-----------------------------------------------------------------------------</td>
<td>---------------------------------------------------------------------------</td>
<td>-----------------</td>
<td></td>
</tr>
<tr>
<td>0b00101</td>
<td>Trapped use of a Pointer authentication instruction because HCR_EL2.API == 0 | SCR_EL3.API == 0.</td>
<td>When FEAT_PAuth is implemented</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b00100</td>
<td>Trapped execution of an LD64B, ST64B, ST64BV, or ST64BV0 instruction.</td>
<td>When FEAT_LS64 is implemented When AArch32 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b00110</td>
<td>Trapped MRRC access with (coproc==0b1110).</td>
<td>When FEAT_BTI is implemented</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b00111</td>
<td>Branch Target Exception.</td>
<td></td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b00110</td>
<td>Illegal Execution state.</td>
<td></td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b01011</td>
<td>SMC instruction execution in AArch32 state, when SMC is not disabled. This is reported in ESR_EL2 only when the exception is generated because the value of HCR_EL2.TSC is 1.</td>
<td>When AArch32 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b01010</td>
<td>SVC instruction execution in AArch64 state.</td>
<td>When AArch64 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b01010</td>
<td>HVC instruction execution in AArch64 state, when HVC is not disabled.</td>
<td>When AArch64 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b01101</td>
<td>SMC instruction execution in AArch64 state, when SMC is not disabled. This is reported in ESR_EL2 only when the exception is generated because the value of HCR_EL2.TSC is 1.</td>
<td>When AArch64 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
<tr>
<td>0b01100</td>
<td>Trapped MSR, MRS or System instruction execution in AArch64 state, that is not reported using EC 0b000000,</td>
<td>When AArch64 is supported at any Exception level</td>
<td>EL2</td>
<td></td>
</tr>
</tbody>
</table>
0b000001 or 0b000011. This includes all instructions that cause exceptions that are part of the encoding space defined in 'System instruction class encoding overview', except for those exceptions reported using EC values 0b000000, 0b000001, or 0b000011.

0b011001 Access to SVE functionality trapped as a result of CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ, that is not reported using EC 0b000000.

0b011100 Exception from a Pointer Authentication instruction authentication failure

0b011111 IMPLEMENTATION DEFINED exception to EL3.

0b100000 Instruction Abort from a lower Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.

0b100001 Instruction Abort taken without a change in Exception level. Used for MMU faults generated by instruction accesses and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.

0b100010 PC alignment fault exception.

0b100100 Data Abort from a lower Exception level.
Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.

**0b100101**  
Data Abort taken without a change in Exception level. Used for MMU faults generated by data accesses, alignment faults other than those caused by Stack Pointer misalignment, and synchronous External aborts, including synchronous parity or ECC errors. Not used for debug-related exceptions.

**0b100110**  
SP alignment fault exception.

**0b101100**  
Trapped floating-point exception taken from AArch64 state. This EC value is valid if the implementation supports trapping of floating-point exceptions, otherwise it is reserved. Whether a floating-point implementation supports trapping of floating-point exceptions is IMPLEMENTATION DEFINED.

**0b101111**  
SError interrupt.

**0b111000**  
BRK instruction execution in AArch64 state. This is reported in ESR_EL3 only if a BRK instruction is executed.

All other EC values are reserved by Arm, and:
ESR_EL3, Exception Syndrome Register (EL3)

- Unused values in the range 0b000000 - 0b101100 (0x00 - 0x2C) are reserved for future use for synchronous exceptions.
- Unused values in the range 0b101101 - 0b111111 (0x2D - 0x3F) are reserved for future use, and might be used for synchronous or asynchronous exceptions.

The effect of programming this field to a reserved value is that behavior is **CONstrained UnPRe dictable**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [25]**

Instruction Length for synchronous exceptions. Possible values of this bit are:

<table>
<thead>
<tr>
<th>IL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>16-bit instruction trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>32-bit instruction trapped. This value is also used when the exception is one of the following:</td>
</tr>
<tr>
<td></td>
<td>• An SError interrupt.</td>
</tr>
<tr>
<td></td>
<td>• An Instruction Abort exception.</td>
</tr>
<tr>
<td></td>
<td>• A PC alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• An SP alignment fault exception.</td>
</tr>
<tr>
<td></td>
<td>• A Data Abort exception for which the value of the ISV bit is 0.</td>
</tr>
<tr>
<td></td>
<td>• An Illegal Execution state exception.</td>
</tr>
<tr>
<td></td>
<td>• Any debug exception except for Breakpoint instruction exceptions.</td>
</tr>
<tr>
<td></td>
<td>• An exception reported using EC value 0b000000.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ISS, bits [24:0]**

Instruction Specific Syndrome. Architecturally, this field can be defined independently for each defined Exception class. However, in practice, some ISS encodings are used for more than one Exception class.

Typically, an ISS encoding has a number of subfields. When an ISS subfield holds a register number, the value returned in that field is the AArch64 view of the register number.

For an exception taken from AArch32 state, see 'Mapping of the general-purpose registers between the Execution states'.

If the AArch32 register descriptor is 0b1111, then:

- If the instruction that generated the exception was not **UnPRe dictable**, the field takes the value 0b11111.
- If the instruction that generated the exception was **UnPRe dictable**, the field takes an **UNKNOWN** value that must be either:
  - The AArch64 view of the register number of a register that might have been used at the Exception level from which the exception was taken.
  - The value 0b11111.

When the EC field is 0b000000, indicating an exception with an unknown reason, the ISS field is not valid, **RES0**.

**ISS encoding for exceptions with an unknown reason**

| 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0 |
|-------------------------------|-------------------|
| RES0                           |                   |

**Bits [24:0]**

Reserved, **RES0**.

When an exception is reported using this EC code the **IL** field is set to 1.

This EC code is used for all exceptions that are not covered by any other EC value. This includes exceptions that are generated in the following situations:
• The attempted execution of an instruction bit pattern that has no allocated instruction or that is not accessible at the current Exception level and Security state, including:
  ◦ A read access using a System register pattern that is not allocated for reads or that does not permit reads at the current Exception level and Security state.
  ◦ A write access using a System register pattern that is not allocated for writes or that does not permit writes at the current Exception level and Security state.
  ◦ Instruction encodings that are unallocated.
  ◦ Instruction encodings for instructions or System registers that are not implemented in the implementation.
• In Debug state, the attempted execution of an instruction bit pattern that is not accessible in Debug state.
• In Non-debug state, the attempted execution of an instruction bit pattern that is not accessible in Non-debug state.
• In AArch32 state, attempted execution of a short vector floating-point instruction.
• In an implementation that does not include Advanced SIMD and floating-point functionality, an attempted access to Advanced SIMD or floating-point functionality under conditions where that access would be permitted if that functionality was present. This includes the attempted execution of an Advanced SIMD or floating-point instruction, and attempted accesses to Advanced SIMD and floating-point System registers.
• An exception generated because of the value of one of the SCTLR_EL1, {ITD, SED, CP15BEN} control bits.
• Attempted execution of:
  ◦ An HVC instruction when disabled by HCR_EL2.HCD or SCR_EL3.HCE.
  ◦ An SMC instruction when disabled by SCR_EL3.SMD.
  ◦ An HLT instruction when disabled by EDSCR.HDE.
• Attempted execution of an MSR or MRS instruction to access SP_EL0 when the value of SPSEL.SP is 0.
• Attempted execution of an MSR or MRS instruction using a _EL12 register name when HCR_EL2.E2H == 0.
• Attempted execution, in Debug state, of:
  ◦ A DCPS1 instruction when the value of HCR_EL2.TGE is 1 and EL2 is disabled or not implemented in the current Security state.
  ◦ A DCPS2 instruction from EL1 or EL0 when EL2 is disabled or not implemented in the current Security state.
  ◦ A DCPS3 instruction when the value of EDSCR.SDD is 1, or when EL3 is not implemented.
• When EL3 is using AArch64, attempted execution from Secure EL1 of an SRS instruction using R13_mon. See ‘Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32’.
• In Debug state when the value of EDSCR.SDD is 1, the attempted execution at EL2, EL1, or EL0 of an instruction that is configured to trap to EL3.
• In AArch32 state, the attempted execution of an MRS (banked register) or an MSR (banked register) instruction to SPSR_mon, SP_mon, or LR_mon.
• An exception that is taken to EL2 because the value of HCR_EL2.TGE is 1 that, if the value of HCR_EL2.TGE was 0 would have been reported with an ESR_ELx.EC value of 0b000111.

ISS encoding for an exception from a WF* instruction

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>RES0</th>
<th>TI</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

• When an A32 instruction is trapped, CV is set to 1.
• When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [19:2]

Reserved, RES0.

TI, bits [1:0]

Trapped instruction. Possible values of this bit are:

<table>
<thead>
<tr>
<th>TI</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>WFI trapped.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>WFE trapped.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>WFIT trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
<tr>
<td>0b11</td>
<td>WFET trapped.</td>
<td>When FEAT_WFxT is implemented</td>
</tr>
</tbody>
</table>

When FEAT_WFxT is implemented, this is a two bit field as shown. Otherwise, bit[1] is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following fields describe configuration settings for generating this exception:

- SCTL_EL1.\{nTWE, nTWI\}.
- HCR_EL2.\{TWE, TWI\}.
- SCR_EL3.\{TWE, TWI\}.

ISS encoding for an exception from an MCR or MRC access

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>Opc2</th>
<th>Opc1</th>
<th>CRn</th>
<th>Rt</th>
<th>CRm</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
</tbody>
</table>

CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.
For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to \(0b1110\).

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to \(0b1110\).
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to \(0b1110\), the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to \(0b1110\), or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Opc2, bits [19:17]**

The Opc2 value from the issued instruction.

For a trapped VMRS access, holds the value \(0b000\).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Opc1, bits [16:14]**

The Opc1 value from the issued instruction.

For a trapped VMRS access, holds the value \(0b111\).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRn, bits [13:10]**

The CRn value from the issued instruction.

For a trapped VMRS access, holds the reg field from the VMRS instruction encoding.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Rt, bits [9:5]**

The Rt value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.
On a Warm reset, this field resets to an architecturally unknown value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.

For a trapped VMRS access, holds the value 0b0000.

On a Warm reset, this field resets to an architecturally unknown value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRC or VMRS instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000011:

- **CNTKCTL_EL1** (EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCTEN), for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0** (ER, CR, SW, EN), for accesses to Performance Monitor registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0** EN, for accesses to Activity Monitors registers from EL0 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2** (TRVM, TVM), for accesses to virtual memory control registers from EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**.TTLB, for execution of TLB maintenance instructions at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL1**.TSW, TPC, MPU, for execution of cache maintenance instructions at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**.TACR, for accesses to the Auxiliary Control Register at EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**.TIDCP, for accesses to lockdown, DMA, and TCM operations at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**.TID1, TID2, TID3, for accesses to ID registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **CPTR_EL2**.TCPAC, for accesses to CPACR_EL1 or CPACR using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **HSTR_EL2**.T<n>, for accesses to System registers using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CNTHCTL_EL2**.EL1PCEN, for accesses to the Generic Timer registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2**.TPM, TPMCR, for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2**.TAM, for accesses to Activity Monitors registers from EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL3**.TCPAC, for accesses to CPACR from EL1 and EL2, and accesses to HCPTR from EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- **MDCR_EL3**.TPM, for accesses to Performance Monitor registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- **CPTR_EL3**.TAM, for accesses to Activity Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCR or MRC access (coproc == 0b1111) trapped to EL3.
- For information on other traps using EC value 0b000011, see ‘Traps to EL3 of Secure monitor functionality from Secure EL1 using AArch32’.
- If FEAT_FGT is implemented, MCR or MRC access to some registers at EL0, trapped to EL2.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b000101:

- **CPACR_EL1**.TTA for accesses to trace registers, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.
• **MDSCR_EL1.TDCC**, for accesses to the Debug Communications Channel (DCC) registers at EL0 and EL1 using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL1 or EL2.

• If FEAT_FGT is implemented, **MDCR_EL2.TDCC** for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

• **HCR_EL2.TID0**, for accesses to the **JIDR** register in the ID group 0 at EL0 and EL1 using AArch32, MRC access (coproc == 0b1110) trapped to EL2.

• **CPTER_EL2.TTA**, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDRA**, for accesses to Debug ROM registers **DBGDRAR** and AArch-DBGDSAR using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDOSA**, for accesses to powerdown debug registers, using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **MDCR_EL2.TDA**, for accesses to other debug registers, using AArch32 state, MCR or MRC access (coproc == 0b1110) trapped to EL2.

• **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDOSA**, for accesses to powerdown debug registers using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

• **MDCR_EL3.TDA**, for accesses to other debug registers, using AArch32, MCR or MRC access (coproc == 0b1110) trapped to EL3.

The following fields describe configuration settings for generating exceptions that are reported using EC value 0b001000:

• **HCR_EL2.TID0**, for accesses to the **FPSID** register in ID group 0 at EL1 using AArch32 state, VMRS access trapped to EL2.

• **HCR_EL2.TID3**, for accesses to registers in ID group 3 including **MVFR0**, **MVFR1**, and **MVFR2**, VMRS access trapped to EL2.

**ISS encoding for an exception from an LD64B or ST64B* instruction**

<table>
<thead>
<tr>
<th>ISS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000000000000000000000000</td>
<td>ST64BV instruction trapped.</td>
</tr>
<tr>
<td>0b0000000000000000000000001</td>
<td>ST64BV0 instruction trapped.</td>
</tr>
<tr>
<td>0b0000000000000000000000010</td>
<td>LD64B or ST64B instruction trapped.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**ISS encoding for an exception from an MCRR or MRRC access**

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>Opc1</th>
<th>RES0</th>
<th>Rt2</th>
<th>Rt</th>
<th>CRm</th>
<th>Direction</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>CV</td>
<td>COND</td>
<td>Opc1</td>
<td>RES0</td>
<td>Rt2</td>
<td>Rt</td>
<td>CRm</td>
<td>Direction</td>
</tr>
</tbody>
</table>

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is **IMPLEMENTATION DEFINED** whether CV is set to 1 or set to 0. See the description of the COND field for more information.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to **0b1110**.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to **0b1110**.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to **0b1110**, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is **IMPLEMENTATION DEFINED** whether:
  - CV is set to 0 and COND is set to an **UNKNOWN** value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is **IMPLEMENTATION DEFINED** whether the COND field is set to **0b1110**, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Opc1, bits [19:16]**

The Opc1 value from the issued instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [15]**

Reserved, RES0.

**Rt2, bits [14:10]**

The Rt2 value from the issued instruction, the second general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Rt, bits [9:5]**

The Rt value from the issued instruction, the first general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Direction, bit [0]

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCRR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRRC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following fields describe configuration settings for generating exceptions that are reported using EC value **0b001100**:

- **CNTKCTL_EL1**, \{EL0PTEN, EL0VTEN, EL0PCTEN, ELOVCTEN\}, for accesses to the Generic Timer Registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **PMUSERENR_EL0**, \{CR, EN\}, for accesses to Performance Monitor registers from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **AMUSERENR_EL0**, \{EN\}, for accesses to Activity Monitors registers AMEVCNTR0<n> and AMEVCNTR1<n> from EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL1 or EL2.
- **HCR_EL2**, \{TRVM, TVM\}, for accesses to virtual memory control registers from EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **HSTR_EL2.T<n>**, for accesses to System registers using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CNTHCTL_EL2**, \{EL1PCEN, EL1PCTEN\}, for accesses to the Generic Timer registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL2**, \{TPM, TPMCR\}, for accesses to Performance Monitor registers from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **CPTR_EL2.TAM**, for accesses to Activity Monitors registers registers AMEVCNTR0<n> and AMEVCNTR1<n> from EL0 and EL1 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL2.
- **MDCR_EL3.TPM**, for accesses to Performance Monitor registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.
- **CPTR_EL3.TAM**, for accesses to Activity Monitors registers from EL0, EL1 and EL2 using AArch32 state, MCRR or MRRC access (coproc == 0b1111) trapped to EL3.
- If FEAT_FGT is implemented, **HDFGRTR_EL2**, PMCCNTR_EL0 for MRRC access and **HDFGWTR_EL2**, PMCCNTR_EL0 for MCRR access to **PMCCNTR** at EL0, trapped to EL2.

The following sections describe configuration settings for generating exceptions that are reported using EC value **0b001100**:

- **MDSCR_EL1.TDCC**, for accesses to the Debug ROM registers DBGDSAR and DBGDRAR at EL0 using AArch32 state, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **MDCR_EL2.TDRA**, for accesses to Debug ROM registers DBGDRAR and AArch-DBGDSAR using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **MDCR_EL3.TDA**, for accesses to debug registers, using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.
- **CPACR_EL1.TTA** for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL1 or EL2.
- **CPTR_EL2.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL2.
- **CPTR_EL3.TTA**, for accesses to trace registers using AArch32, MCRR or MRRC access (coproc == 0b1110) trapped to EL3.

**Note**

If the Armv8-A architecture is implemented with an ETMv4 implementation, MCRR and MRRC accesses to trace registers are **UNDEFINED** and the resulting exception is higher priority than an exception due to these traps.

**ISS encoding for an exception from an LDC or STC instruction**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | imm8 | RES0 | Rn | Offset | AM | Direction |
**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
  - With the COND value held in the instruction.
- When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  - CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**imm8, bits [19:12]**

The immediate value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [11:10]**

Reserved, RES0.

**Rn, bits [9:5]**

The Rn value from the issued instruction, the general-purpose register used for the transfer. The reported value gives the AArch64 view of the register. See 'Mapping of the general-purpose registers between the Execution states'.

This field is valid only when AM[2] is 0, indicating an immediate form of the LDC or STC instruction. When AM[2] is 1, indicating a literal form of the LDC or STC instruction, this field is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Offset, bit [4]

Indicates whether the offset is added or subtracted:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Subtract offset.</td>
</tr>
<tr>
<td>0b1</td>
<td>Add offset.</td>
</tr>
</tbody>
</table>

This bit corresponds to the U bit in the instruction encoding.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**AM, bits [3:1]**

Addressing mode. The permitted values of this field are:

<table>
<thead>
<tr>
<th>AM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Immediate unindexed.</td>
</tr>
<tr>
<td>0b001</td>
<td>Immediate post-indexed.</td>
</tr>
<tr>
<td>0b010</td>
<td>Immediate offset.</td>
</tr>
<tr>
<td>0b011</td>
<td>Immediate pre-indexed.</td>
</tr>
<tr>
<td>0b100</td>
<td>For a trapped STC instruction or a trapped T32 LDC instruction this encoding is reserved.</td>
</tr>
<tr>
<td>0b101</td>
<td>For a trapped STC instruction, this encoding is reserved.</td>
</tr>
</tbody>
</table>

The values 0b101 and 0b111 are reserved. The effect of programming this field to a reserved value is that behavior is **CONSTRAINED UNPREDICTABLE**, as described in 'Reserved values in System and memory-mapped registers and translation table entries'.

Bit [2] in this subfield indicates the instruction form, immediate or literal.

Bits [1:0] in this subfield correspond to the bits \{P, W\} in the instruction encoding.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction.

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to memory. STC instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from memory. LDC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following fields describe the configuration settings for the traps that are reported using EC value 0b000110:

- **MDSCR_EL1.TDCC**, for accesses using AArch32 state, LDC access to **DBGDTRXint** or STC access to **DBGDTRRXint** trapped to EL1 or EL2.
- **MDCR_EL2.TDA**, for accesses using AArch32 state, LDC access to **DBGDTRXint** or STC access to **DBGDTRRXint** MCR or MRC access trapped to EL2.
- **MDCR_EL3.TDA**, for accesses using AArch32 state, LDC access to **DBGDTRXint** or STC access to **DBGDTRRXint** MCR or MRC access trapped to EL3.
- If **FEAT_FGT** is implemented, **MDCR_EL2.TDCC** for LDC and STC accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.

**ISS encoding for an exception from an access to SVE, Advanced SIMD or floating-point functionality, resulting from the FPEN and TFP traps**

```
  24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
 CV COND RES0
```

The accesses covered by this trap include:
• Execution of SVE or Advanced SIMD and floating-point instructions.
• Accesses to the Advanced SIMD and floating-point System registers.

For an implementation that does not include either SVE or support for floating-point and Advanced SIMD, the exception is reported using the EC value 0b000000.

**CV, bit [24]**

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

• When an A32 instruction is trapped, CV is set to 1.
• When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. See the description of the COND field for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

• When an A32 instruction is trapped, CV is set to 1 and:
  ◦ If the instruction is conditional, COND is set to the condition code field value from the instruction.
  ◦ If the instruction is unconditional, COND is set to 0b1110.
• A conditional A32 instruction that is known to pass its condition code check can be presented either:
  ◦ With COND set to 0b1110, the value for unconditional.
  ◦ With the COND value held in the instruction.
• When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
  ◦ CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  ◦ CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
• For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:0]**

Reserved, RES0.

The following sections describe the configuration settings for the traps that are reported using EC value 0b000111:

• **CPACR_EL1.FPEN**, for accesses to SIMD and floating-point registers trapped to EL1.
• **CPTR_EL2.TFP**, for accesses to SIMD and floating-point registers trapped to EL2.
• **CPTR_EL3.TFP**, for accesses to SIMD and floating-point registers trapped to EL3.
ISS encoding for an exception from an access to SVE functionality, resulting from CPACR_EL1.ZEN, CPTR_EL2.ZEN, CPTR_EL2.TZ, or CPTR_EL3.EZ

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

The accesses covered by this trap include:

- Execution of SVE instructions.
- Accesses to the SVE System register, ZCR_ELx.

For an implementation that does not include SVE, the exception is reported using the EC value 0b000000.

**Bits [24:0]**

Reserved, RES0.

The following sections describe the configuration settings for the traps that are reported using EC value 0b011001:

- **CPACR_EL1.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0 or EL1, trapped to EL2.
- **CPTR_EL2.ZEN**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL2.TZ**, for execution of SVE instructions and accesses to SVE registers at EL0, EL1, or EL2, trapped to EL2.
- **CPTR_EL3.EZ**, for execution of SVE instructions and accesses to SVE registers from all Exception levels, trapped to EL3.

ISS encoding for an exception from an Illegal Execution state, or a PC or SP alignment fault

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
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<th>10</th>
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<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
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<td></td>
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</tbody>
</table>

**Bits [24:0]**

Reserved, RES0.

There are no configuration settings for generating Illegal Execution state exceptions and PC alignment fault exceptions. For more information about these exceptions, see ‘The Illegal Execution state exception’ and ‘PC alignment checking’.

‘SP alignment checking’ describes the configuration settings for generating SP alignment fault exceptions.

ISS encoding for an exception from HVC or SVC instruction execution

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
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<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>imm16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [24:16]**

Reserved, RES0.

**imm16, bits [15:0]**

The value of the immediate field from the HVC or SVC instruction.

For an HVC instruction, and for an A64 SVC instruction, this is the value of the imm16 field of the issued instruction.
For an A32 or T32 SVC instruction:

- If the instruction is unconditional, then:
  - For the T32 instruction, this field is zero-extended from the imm8 field of the instruction.
  - For the A32 instruction, this field is the bottom 16 bits of the imm24 field of the instruction.
- If the instruction is conditional, this field is "UNKNOWN".

On a Warm reset, this field resets to an architecturally "UNKNOWN" value.

In AArch32 state, the HVC instruction is unconditional, and a conditional SVC instruction generates an exception only if it passes its condition code check. Therefore, the syndrome information for these exceptions does not require conditionality information.

For T32 and A32 instructions, see 'SVC' and 'HVC'.

For A64 instructions, see 'SVC' and 'HVC'.

If FEAT_FGT is implemented, HFGITR_EL2 {SVC_EL1, SVC_EL0} control fine-grained traps on SVC execution.

### ISS encoding for an exception from SMC instruction execution in AArch32 state

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV</td>
<td>COND</td>
<td>CKNOWNPASS</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

For an SMC instruction that completes normally and generates an exception that is taken to EL3, the ISS encoding is "RES0".

For an SMC instruction that is trapped to EL2 from EL1 because HCR_EL2.TSC is 1, the ISS encoding is as shown in the diagram.

### CV, bit [24]

Condition code valid.

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

For exceptions taken from AArch64, CV is set to 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1.
- When a T32 instruction is trapped, it is "IMPLEMENTATION DEFINED" whether CV is set to 1 or set to 0. See the description of the COND field for more information.

This field is valid only if CKNOWNPASS is 1, otherwise it is "RES0".

On a Warm reset, this field resets to an architecturally "UNKNOWN" value.

### COND, bits [23:20]

For exceptions taken from AArch64, this field is set to 0b1110.

The condition code for the trapped instruction. This field is valid only for exceptions taken from AArch32, and only when the value of CV is 1.

For exceptions taken from AArch32:

- When an A32 instruction is trapped, CV is set to 1 and:
  - If the instruction is conditional, COND is set to the condition code field value from the instruction.
  - If the instruction is unconditional, COND is set to 0b1110.
- A conditional A32 instruction that is known to pass its condition code check can be presented either:
  - With COND set to 0b1110, the value for unconditional.
With the COND value held in the instruction.

- When a T32 instruction is trapped, it is **IMPLEMENTATION DEFINED** whether:
  - CV is set to 0 and COND is set to an **UNKNOWN** value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  - CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
- For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is **IMPLEMENTATION DEFINED** whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

This field is valid only if CCKNOWNPASS is 1, otherwise it is res0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CCKNOWNPASS, bit [19]**

Indicates whether the instruction might have failed its condition code check.

<table>
<thead>
<tr>
<th>CCKNOWNPASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The instruction was unconditional, or was conditional and passed its condition code check.</td>
</tr>
<tr>
<td>0b1</td>
<td>The instruction was conditional, and might have failed its condition code check.</td>
</tr>
</tbody>
</table>

**Note**

In an implementation in which an SMC instruction that fails it code check is not trapped, this field can always return the value 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [18:0]**

Reserved, res0.

HCR_EL2.TSC describes the configuration settings for trapping SMC instructions to EL2.

'System calls' describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from SMC instruction execution in AArch64 state**

```
  24 23 22 21 20 19 18 17 16 15 14 13 12 11 10  9  8  7  6  5  4  3  2  1  0
  |RES0|imm16|
```

**Bits [24:16]**

Reserved, res0.

**imm16, bits [15:0]**

The value of the immediate field from the issued SMC instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The value of ISS[24:0] described here is used both:

- When an SMC instruction is trapped from EL1 modes.
- When an SMC instruction is not trapped, so completes normally and generates an exception that is taken to EL3.

HCR_EL2.TSC describes the configuration settings for trapping SMC from EL1 modes.
‘System calls' describes the case where these exceptions are trapped to EL3.

**ISS encoding for an exception from MSR, MRS, or System instruction execution in AArch64 state**

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>24-22</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>21-20</td>
<td>Op0</td>
<td>The Op0 value from the issued instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>19-17</td>
<td>Op2</td>
<td>The Op2 value from the issued instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>16-14</td>
<td>Op1</td>
<td>The Op1 value from the issued instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>13-10</td>
<td>CRn</td>
<td>The CRn value from the issued instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>9-5</td>
<td>Rt</td>
<td>The Rt value from the issued instruction, the general-purpose register used for the transfer.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>4-1</td>
<td>CRm</td>
<td>The CRm value from the issued instruction.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>On a Warm reset, this field resets to an architecturally <strong>UNKNOWN</strong> value.</td>
</tr>
<tr>
<td>0</td>
<td>Direction</td>
<td>Indicates the direction of the trapped instruction.</td>
</tr>
<tr>
<td></td>
<td>0b0</td>
<td>Write access, including MSR instructions.</td>
</tr>
<tr>
<td></td>
<td>0b1</td>
<td>Read access, including MRS instructions.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For exceptions caused by System instructions, see ‘System instructions' subsection of 'Branches, exception generating and System instructions' for the encoding values returned by an instruction.
The following fields describe configuration settings for generating the exception that is reported using EC value 0b011000:

- **SCTLR_EL1.UCI**, for execution of cache maintenance instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.UCT**, for accesses to **CTR_EL0** using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.DZE**, for execution of DC ZVA instructions using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **SCTLR_EL1.UMA**, for accesses to the PSTATE interrupt masks using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **CPACR_EL1.TTA**, for accesses to the trace registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **MDSCR_EL1.TDCC**, for accesses to the Debug Communications Channel (DCC) registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- If FEAT_FGT is implemented, **MDCR_EL2.TDCC** for accesses to the DCC registers at EL0 and EL1 trapped to EL2, and **MDCR_EL3.TDCC** for accesses to the DCC registers at EL0, EL1, and EL2 trapped to EL3.
- **CNTKCTL_EL1.EL0PTEN, EL0VTEN, EL0PCTEN, EL0VCCTEN** accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **PMUSERENR_EL0.ER, CR, SW, EN**, for accesses to the Performance Monitor registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **AMUSERENR_EL0.ER, CR, SW, EN**, for accesses to Activity Monitors registers using AArch64 state, MSR or MRS access trapped to EL1 or EL2.
- **HCR_EL2.TRVM, TVM**, for accesses to virtual memory control registers using AArch64 state, MSR or MRS access trapped to EL2.
- **HCR_EL2.TID1, TID2, TID3**, for accesses to ID group 1, ID group 2 or ID group 3 registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **CPTR_EL2.TCPAC**, for accesses to **CPACR_EL1**, using AArch64 state, MSR or MRS access trapped to EL2.
- **CPTR_EL2.TTA**, for accesses to the trace registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **MDCR_EL2.TRF**, for accesses to the trace filter control register, **TRFCR_EL1**, using AArch64 state, MSR or MRS access trapped to EL2.
- **MDCR_EL2.TDRA**, for accesses to Debug ROM registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **MDCR_EL2.TDOSA**, for accesses to powerdown debug registers using AArch64 state, MSR or MRS access trapped to EL2.
- **CNTHCTL_EL2.EL1PCEN, EL1PCCTEN**, for accesses to the Generic Timer registers using AArch64 state, MSR or MRS access trapped to EL2.
- **DCR_EL2.TDA**, for accesses to registers using AArch64 state, MSR or MRS access trapped to EL2.
- **MDCR_EL2.TPM, TPMCR**, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **CPTR_EL2.TAM**, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **HCR_EL2.APK**, for accesses to Pointer authentication key registers, using AArch64 state, MSR or MRS access trapped to EL2.
- **HCR_EL2.NV, NV1**, for Nested virtualization register access, using AArch64 state, MSR or MRS access, trapped to EL2.
- **HCR_EL2.AT**, for execution of AT S1E* instructions, using AArch64 state, MSR or MRS access, trapped to EL2.
- **SCR_EL3.APK**, for accesses to RAS registers, using AArch64 state, MSR or MRS access, trapped to EL3.
- **SCR_EL3.APK**, for accesses to Pointer authentication key registers, using AArch64 state, MSR or MRS access trapped to EL3.
- **SCR_EL3.ST**, for accesses to the Counter-timer Physical Secure timer registers, using AArch64 state, MSR or MRS access trapped to EL3.
• **CPTR_EL3.TCPAC**, for accesses to **CPTR_EL2** and **CPACR_EL1** using AArch64 state, MSR or MRS access trapped to EL3.
• **CPTR_EL2.TTA**, for accesses to the trace registers, using AArch64 state, MSR or MRS access trapped to EL3.
• **MDCR_EL3.TTRF**, for accesses to the trace filter control registers, **TRFCR_EL1** and **TRFCR_EL2**, using AArch64 state, MSR or MRS access trapped to EL3.
• **MDCR_EL3.TDA**, for accesses to debug registers, using AArch64 state, MSR or MRS access trapped to EL3.
• **MDCR_EL3.TTOSA**, for accesses to powerdown debug registers, using AArch64 state, MSR or MRS access trapped to EL3.
• **MDCR_EL3.TPM**, for accesses to Performance Monitor registers, using AArch64 state, MSR or MRS access trapped to EL3.
• **CPTR_EL3.TAM**, for accesses to Activity Monitors registers, using AArch64 state, MSR or MRS access, trapped to EL3.
• If **FEAT.EVT** is implemented, the following registers control traps for EL1 and EL0 Cache controls that use this EC value:
  - **HCR_EL2.{TTLBOS, TTLBIS, TICAB, TOCU, TID4}**.
  - **HCR2.{TTLBIS, TICAB, TOCU, TID4}**.
• If **FEAT_FGT** is implemented:
  - **SCR_EL3.FGTEn**, for accesses to the fine-grained trap registers, MSR or MRS access at EL2 trapped to EL3.
  - **HFGITR_EL2** for reads and **HFGWTR_EL2** for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 trapped to EL2.
  - **HDFGRTR_EL2** for reads and **HDFGWTR_EL2** for writes of registers, using AArch64 state, MSR or MRS access at EL0 and EL1 state trapped to EL2.
  - **HAFGRTR_EL2** for reads of Activity Monitor counters, using AArch64 state, MRS access at EL0 and EL1 trapped to EL2.

### ISS encoding for an IMPLEMENTATION DEFINED exception to EL3

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |

**IMPLEMENTATION DEFINED**, bits [24:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### ISS encoding for an exception from an Instruction Abort

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SET | FnVEA | RES0 | S1PTW | RES0 | IFSC |

**Bits [24:13]**

Reserved, RES0.

**SET, bits [12:11]**

When **FEAT_RAS** is implemented:

Synchronous Error Type. When IFSC is 0b010000, describes the PE error state after taking the Instruction Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Note**
Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the IFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**FnV, bit [10]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is valid only if the IFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EA, bit [9]**

External abort type. This bit can provide an IMPLEMENTATION DEFINED classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [8]**

Reserved, RES0.

**S1PTW, bit [7]**

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [6]**

Reserved, RES0.

**IFSC, bits [5:0]**

Instruction Fault Status Code.
<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b00001100</td>
<td>Access flag fault, level 1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b000100</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b00011100</td>
<td>Access flag fault, level 3.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 0.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td></td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b101000</td>
<td>Address size fault, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
</tbody>
</table>
Translation fault, level -1. When FEAT_LPA2 is implemented
TLB conflict abort.
Unsupported atomic hardware update fault.

All other values are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults’.

Note

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage 2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS encoding for an exception from a Data Abort

<table>
<thead>
<tr>
<th>ISV</th>
<th>SAS</th>
<th>SSE</th>
<th>SRT</th>
<th>SF</th>
<th>AR</th>
<th>VNCR</th>
<th>Bits[12:11]</th>
<th>Fr</th>
<th>V</th>
<th>EA</th>
<th>CM</th>
<th>S1PTW</th>
<th>WnR</th>
<th>DFSC</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No valid instruction syndrome. ISS[23:14] are RES0.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>ISS[23:14] hold a valid instruction syndrome.</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

In ESR_EL2, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

For other faults reported in ESR_EL2, ISV is 0 except for the following stage 2 aborts:

- AArch64 loads and stores of a single general-purpose register (including the register specified with 0b11111, including those with Acquire/Release semantics, but excluding Load Exclusive or Store Exclusive and excluding those with writeback).
- AArch32 instructions where the instruction:
  - Is an LDR, LDA, LDRSH, LDRSHT, LDRH, LDAH, LDRHT, LDRSB, LDRSBT, LDRB, LDB, LDRBT, STR, STL, STRT, STRH, STLH, STRHT, STRB, STL, or STRBT instruction.
  - Is not performing register writeback.
  - Is not using R15 as a source or destination register.

For these stage 2 aborts, ISV is UNKNOWN if the exception was generated in Debug state in memory access mode, and otherwise indicates whether ISS[23:14] hold a valid syndrome.

For faults reported in ESR_EL1 or ESR_EL3, ISV is 1 when FEAT_LS64 is implemented and a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault. ISV is 0 for all other faults reported in ESR_EL1 or ESR_EL3.

When FEAT_RAS is implemented, ISV is 0 for any synchronous External abort.

For ISS reporting, a stage 2 abort on a stage 1 translation table walk does not return a valid instruction syndrome, and therefore ISV is 0 for these aborts.
When FEAT_RAS is not implemented, it is implementation defined whether ISV is set to 1 or 0 on a synchronous External abort on a stage 2 translation table walk.

When FEAT_MTE is implemented, for a synchronous Tag Check Fault abort taken to ELx, ESR_ELx.FNV is 0 and FAR_ELx is valid.

On a Warm reset, this field resets to an architecturally unknown value.

**SAS, bits [23:22]**

*When ISV == '1':*

Syndrome Access Size. Indicates the size of the access attempted by the faulting operation.

<table>
<thead>
<tr>
<th>SAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Byte</td>
</tr>
<tr>
<td>0b01</td>
<td>Halfword</td>
</tr>
<tr>
<td>0b10</td>
<td>Word</td>
</tr>
<tr>
<td>0b11</td>
<td>Doubleword</td>
</tr>
</tbody>
</table>

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0b11.

This field is unknown when the value of ISV is unknown.

On a Warm reset, this field resets to an architecturally unknown value.

*Otherwise:*

Reserved, RES0.

**SSE, bit [21]**

*When ISV == '1':*

Syndrome Sign Extend. For a byte, halfword, or word load operation, indicates whether the data item must be sign extended.

<table>
<thead>
<tr>
<th>SSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sign-extension not required.</td>
</tr>
<tr>
<td>0b1</td>
<td>Data item must be sign-extended.</td>
</tr>
</tbody>
</table>

When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

For all other operations, this field is 0.

This field is unknown when the value of ISV is unknown.

On a Warm reset, this field resets to an architecturally unknown value.

*Otherwise:*

Reserved, RES0.

**SRT, bits [20:16]**

*When ISV == '1':*

Syndrome Register Transfer. When FEAT_LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field holds register specifier, Xt.
If the exception was taken from an Exception level that is using AArch32, then this is the AArch64 view of the register. See ‘Mapping of the general-purpose registers between the Execution states’.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**SF, bit [15]**

**When ISV == ‘1’:**

Width of the register accessed by the instruction is Sixty-Four.

<table>
<thead>
<tr>
<th>SF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction loads/stores a 32-bit wide register.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction loads/stores a 64-bit wide register.</td>
</tr>
</tbody>
</table>

**Note**

This field specifies the register width identified by the instruction, not the Execution state.

When FEAT LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 1.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**AR, bit [14]**

**When ISV == ‘1’:**

Acquire/Release.

<table>
<thead>
<tr>
<th>AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction did not have acquire/release semantics.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction did have acquire/release semantics.</td>
</tr>
</tbody>
</table>

When FEAT LS64 is implemented, if a memory access generated by an ST64BV, ST64BV0, ST64B, or LD64B instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault, then this field is 0.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.
VNCR, bit [13]

When FEAT_NV2 is implemented:

Indicates that the fault came from use of VNCR_EL2 register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault was not generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault was generated by the use of VNCR_EL2, by an MRS or MSR instruction executed at EL1.</td>
</tr>
</tbody>
</table>

This field is 0 in ESR_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

SET, bits [12:11]

When FEAT_RAS is implemented and FEAT_LS64 is not implemented:

Synchronous Error Type. When DFSC is 0b010000, describes the PE error state after taking the Data Abort exception.

<table>
<thead>
<tr>
<th>SET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b11</td>
<td>Restartable state (UEO).</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

Software can use this information to determine what recovery might be possible. Taking a synchronous External Abort exception might result in a PE state that is not recoverable.

This field is valid only if the DFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When FEAT_LS64 is implemented:

Load/Store Type. Used when an LD64B, ST64B, ST64BV, or ST64BV0 instruction generates a Data Abort for a Translation fault, Access flag fault, or Permission fault.

<table>
<thead>
<tr>
<th>LST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>An ST64BV instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b10</td>
<td>An LD64B or ST64B instruction generated the Data Abort.</td>
</tr>
<tr>
<td>0b11</td>
<td>An ST64BV0 instruction generated the Data Abort.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is valid only if the DFSC code is 0b110101. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
FnV, bit [10]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>FAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EA, bit [9]

External abort type. This bit can provide an IMPLEMENTATION DEFINED classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CM, bit [8]

Cache maintenance. Indicates whether the Data Abort came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Data Abort was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Data Abort was generated by either the execution of a cache maintenance instruction or by a synchronous fault on the execution of an address translation instruction. The DC ZVA, DC GVA, and DC GZVA instructions are not classified as cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

S1PTW, bit [7]

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

WnR, bit [6]

Write not Read. Indicates whether a synchronous abort was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For faults on cache maintenance and address translation instructions, this bit always returns a value of 1.
For faults from an atomic instruction that both reads and writes from a memory location, this bit is set to 0 if a read of the address specified by the instruction would have generated the fault which is being reported, otherwise it is set to 1. The architecture permits, but does not require, a relaxation of this requirement such that for all stage 2 aborts on stage 1 translation table walks for atomic instructions, the WnR bit is always 0.

This field is UNKNOWN for:

- An External abort on an Atomic access.
- A fault reported using a DFSC value of \(0b110101\) or \(0b110001\), indicating an unsupported Exclusive or atomic access.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DFSC, bits [5:0]**

Data Fault Status Code.
<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base register.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td>When FEAT_MTE is implemented</td>
</tr>
<tr>
<td>0b010001</td>
<td>Synchronous Tag Check Fault.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010010</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 0.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>
Alignment fault.

Address size fault, level -1. When FEAT_LPA2 is implemented

Translation fault, level -1. When FEAT_LPA2 is implemented

TLB conflict abort.

Unsupported atomic hardware update fault. When FEAT_HAFDBS is implemented

IMPLEMENTATION DEFINED fault (Lockdown).

IMPLEMENTATION DEFINED fault (Unsupported Exclusive or Atomic access).

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults'.

Note

Because Access flag faults and Permission faults can result only from a Block or Page translation table descriptor, they cannot occur at level 0.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ISS encoding for an exception from a trapped floating-point exception**

| Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| RES0   | TFV    | RES0   | VECITR | IDF    | RES0   | IXF    | UFF    | OFF    | DZF    | IOF    |

**Bit [24]**

Reserved, RES0.

**TFV, bit [23]**

Trapped Fault Valid bit. Indicates whether the IDF, IXF, UFF, OFF, DZF, and IOF bits hold valid information about trapped floating-point exceptions.

<table>
<thead>
<tr>
<th>TFV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The IDF, IXF, UFF, OFF, DZF, and IOF bits do not hold valid information about trapped floating-point exceptions and are UNKNOWN.</td>
</tr>
<tr>
<td>0b1</td>
<td>One or more floating-point exceptions occurred during an operation performed while executing the reported instruction. The IDF, IXF, UFF, OFF, DZF, and IOF bits indicate trapped floating-point exceptions that occurred. For more information, see 'Floating-point exceptions and exception traps'.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field is set to 0 on an exception generated by a trapped floating-point exception from a vector instruction.

**Note**

This is not a requirement. Implementations can set this field to 1 on a trapped floating-point exception from a vector instruction and return valid information in the {IDF, IXF, UFF, OFF, DZF, IOF} fields.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [22:11]**

Reserved, RES0.

**VECITR, bits [10:8]**

For a trapped floating-point exception from an instruction executed in AArch32 state this field is RES1.
For a trapped floating-point exception from an instruction executed in AArch64 state this field is UNKNOWN.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IDF, bit [7]**

Input Denormal floating-point exception trapped bit. If the TFV field is 0, this bit is UNKNOWN. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IDF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input denormal floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input denormal floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [6:5]**

Reserved, RES0.

**IXF, bit [4]**

Inexact floating-point exception trapped bit. If the TFV field is 0, this bit is UNKNOWN. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IXF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inexact floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inexact floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**UFF, bit [3]**

Underflow floating-point exception trapped bit. If the TFV field is 0, this bit is UNKNOWN. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>UFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**OFF, bit [2]**

Overflow floating-point exception trapped bit. If the TFV field is 0, this bit is UNKNOWN. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>OFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Overflow floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overflow floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DZF, bit [1]**

Divide by Zero floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>DZF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Divide by Zero floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Divide by Zero floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IOF, bit [0]**

Invalid Operation floating-point exception trapped bit. If the TFV field is 0, this bit is **UNKNOWN**. Otherwise, the possible values of this bit are:

<table>
<thead>
<tr>
<th>IOF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalid Operation floating-point exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalid Operation floating-point exception occurred during execution of the reported instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

In an implementation that supports the trapping of floating-point exceptions:

- From an Exception level using AArch64, the FPSCR.\{IDE, IXE, UFE, OFE, DZE, IOE\} bits enable each of the floating-point exception traps.
- From an Exception level using AArch32, the FPSCR.\{IDE, IXE, UFE, OFE, DZE, IOE\} bits enable each of the floating-point exception traps.

**ISS encoding for an SError interrupt**

```
| IDS | RES0 | IESB | AET | EA | RES0 | DFSC |
```

**IDS, bit [24]**

**IMPLEMENTATION DEFINED** syndrome.

<table>
<thead>
<tr>
<th>IDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits [23:0] of the ISS field holds the fields described in this encoding.</td>
</tr>
</tbody>
</table>

**Note**

If FEAT_RAS is not implemented, bits [23:0] of the ISS field are RES0.

| 0b1  | Bits [23:0] of the ISS field holds IMPLEMENTATION DEFINED syndrome information that can be used to provide additional information about the SError interrupt. |

**Note**

This field was previously called ISV.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [23:14]**

Reserved, RES0.
IESB, bit [13]

When FEAT_IESB is implemented:

Implicit error synchronization event.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The SError interrupt was either not synchronized by the implicit error synchronization event or not taken immediately.</td>
</tr>
<tr>
<td>0b1</td>
<td>The SError interrupt was synchronized by the implicit error synchronization event and taken immediately.</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

AET, bits [12:10]

When FEAT_RAS is implemented:

Asynchronous Error Type.

When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception.

<table>
<thead>
<tr>
<th>AET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b001</td>
<td>Unrecoverable state (UEU).</td>
</tr>
<tr>
<td>0b010</td>
<td>Restartable state (UEO).</td>
</tr>
<tr>
<td>0b011</td>
<td>Recoverable state (UER).</td>
</tr>
<tr>
<td>0b110</td>
<td>Corrected (CE).</td>
</tr>
</tbody>
</table>

All other values are reserved.

If multiple errors are taken as a single SError interrupt exception, the overall PE error state is reported.

Note

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EA, bit [9]

When FEAT_RAS is implemented:

External abort type. When DFSC is 0b010001, provides an IMPLEMENTATION DEFINED classification of External aborts.

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other errors.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

Bits [8:6]

Reserved, RES0.

DFSC, bits [5:0]

When FEAT_RAS is implemented:

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Uncategorized error.</td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

ISS encoding for an exception from a Breakpoint or Vector Catch debug exception

| 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|------------------------|------------------------|
|                        |                        |
| RES0                   | IFSC                   |

Bits [24:6]

Reserved, RES0.

IFSC, bits [5:0]

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions:

- For exceptions from AArch64, see ‘Breakpoint exceptions’.
- For exceptions from AArch32, see ‘Breakpoint exceptions’ and ‘Vector Catch exceptions’.

ISS encoding for an exception from a Software Step exception

| 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|------------------------|------------------------|
| ISV                    | RES0                   | EX       | IFSC     |

ISV, bit [24]

Instruction syndrome valid. Indicates whether the EX bit, ISS[6], is valid, as follows:
See the EX bit description for more information.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [23:7]**

Reserved, **RES0**.

**EX, bit [6]**

Exclusive operation. If the ISV bit is set to 1, this bit indicates whether a Load-Exclusive instruction was stepped.

<table>
<thead>
<tr>
<th>EX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An instruction other than a Load-Exclusive instruction was stepped.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Load-Exclusive instruction was stepped.</td>
</tr>
</tbody>
</table>

If the ISV bit is set to 0, this bit is **RES0**, indicating no syndrome data is available.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IFSC, bits [5:0]**

Instruction Fault Status Code.

<table>
<thead>
<tr>
<th>IFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For more information about generating these exceptions, see ‘Software Step exceptions’.

**ISS encoding for an exception from a Watchpoint exception**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0| RES0|VNC R| RES0| CM | RES0| WnR| DF SC|

**Bits [24:15]**

Reserved, **RES0**.

**Bit [14]**

Reserved, **RES0**.

**VNCR, bit [13]**

When **FEAT_NV2** is implemented:

Indicates that the watchpoint came from use of **VNCR_EL2** register by EL1 code.

<table>
<thead>
<tr>
<th>VNCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The watchpoint was not generated by the use of <strong>VNCR_EL2</strong> by EL1 code.</td>
</tr>
<tr>
<td>0b1</td>
<td>The watchpoint was generated by the use of <strong>VNCR_EL2</strong> by EL1 code.</td>
</tr>
</tbody>
</table>

This field is 0 in **ESR_EL1**.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**Bits [12:9]**

Reserved, **RES0**.

**CM, bit [8]**

Cache maintenance. Indicates whether the Watchpoint exception came from a cache maintenance or address translation instruction:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Watchpoint exception was not generated by the execution of one of the System instructions identified in the description of value 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Watchpoint exception was generated by either the execution of a cache maintenance instruction or by a synchronous Watchpoint exception on the execution of an address translation instruction. The <strong>DC ZVA</strong>, <strong>DC GVA</strong>, and <strong>DC GZVA</strong> instructions are not classified as a cache maintenance instructions, and therefore their execution cannot cause this field to be set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [7]**

Reserved, **RES0**.

**WnR, bit [6]**

Write not Read. Indicates whether the Watchpoint exception was caused by an instruction writing to a memory location, or by an instruction reading from a memory location.

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint exception caused by an instruction reading from a memory location.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint exception caused by an instruction writing to a memory location.</td>
</tr>
</tbody>
</table>

For Watchpoint exceptions on cache maintenance and address translation instructions, this bit always returns a value of 1.

For Watchpoint exceptions from an atomic instruction, this field is set to 0 if a read of the location would have generated the Watchpoint exception, otherwise it is set to 1.

If multiple watchpoints match on the same access, it is **UNPREDICTABLE** which watchpoint generates the Watchpoint exception.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DFSC, bits [5:0]**

Data Fault Status Code.

<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
For more information about generating these exceptions, see 'Watchpoint exceptions'.

**ISS encoding for an exception from execution of a Breakpoint instruction**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [24:16]**

Reserved, RES0.

**Comment, bits [15:0]**

Set to the instruction comment field value, zero extended as necessary.

For the AArch32 BKPT instructions, the comment field is described as the immediate field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see 'Breakpoint instruction exceptions'.

**ISS encoding for an exception from an ERET, ERETA, or ERETAB instruction**

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This EC value applies when FEAT_FGT is implemented, or when HCR_EL2.NV is 1.

**Bits [24:2]**

Reserved, RES0.

**ERET, bit [1]**

Indicates whether an ERET or ERETA* instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERET instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETA or ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

If this bit is 0, the ERETA field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ERETA, bit [0]**

Indicates whether an ERETA or ERETAB instruction was trapped to EL2.

<table>
<thead>
<tr>
<th>ERETA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERETA instruction trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERETAB instruction trapped to EL2.</td>
</tr>
</tbody>
</table>

When the ERET field is 0, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For more information about generating these exceptions, see HCR_EL2.NV.

If FEAT_FGT is implemented, HFGITR_EL2.ERET controls fine-grained trap exceptions from ERET, ERETA and ERETAB execution.
ISS encoding for an exception from Branch Target Identification instruction

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>BTYPE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:2]

Reserved, RES0.

BTYPE, bits [1:0]

This field is set to the PSTATE.BTYPE value that generated the Branch Target Exception.

For more information about generating these exceptions, see 'The AArch64 application level programmers model'.

ISS encoding for an exception from a Pointer Authentication instruction when HCR_EL2.API == 0 || SCR_EL3.API == 0

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:0]

Reserved, RES0.

For more information about generating these exceptions, see:

- HCR_EL2.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL2.
- SCR_EL3.API, for exceptions from Pointer authentication instructions, using AArch64 state, trapped to EL3.

ISS encoding for an exception from a Pointer Authentication instruction authentication failure

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Exception as a result of an Instruction key or a Data key</td>
<td>Exception as a result of an A key or a B key</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:2]

Reserved, RES0.

Bit [1]

This field indicates whether the exception is as a result of an Instruction key or a Data key.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Bit [0]**

This field indicates whether the exception is as a result of an A key or a B key.

<table>
<thead>
<tr>
<th>Meaning</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A key.</td>
</tr>
<tr>
<td>0b1</td>
<td>B key.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following instructions generate an exception when the Pointer Authentication Code (PAC) is incorrect:

- AUTIASP, AUTIAZ, AUTIA1716.
- AUTIBSP, AUTIBZ, AUTIB1716.
- AUTIA, AUTDA, AUTIB, AUTDB.
- AUTIZA, AUTIZB, AUTDZA, AUTDZB.

It is **IMPLEMENTATION DEFINED** whether the following instructions generate an exception directly from the authorization failure, rather than changing the address in a way that will generate a translation fault when the address is accessed:

- RETAA, RETAB.
- BRAA, BRAB, BLRAA, BLRAB.
- BRAAZ, BRABZ, BLRAAZ, BLRABZ.
- ERETTA, ERETAB.
- LDRAA, LDRAB, whether the authenticated address is written back to the base register or not.

**Accessing the ESR_EL3**

Accesses to this register use the following encodings:

**MRS <Xt>, ESR_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
  return ESR_EL3;

**MSR ESR_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
  ESR_EL3 = X[t];
FAR_EL1, Fault Address Register (EL1)

The FAR_EL1 characteristics are:

**Purpose**

Holds the faulting Virtual Address for all synchronous Instruction or Data Abort, PC alignment fault and Watchpoint exceptions that are taken to EL1.

**Configuration**

AArch64 System register FAR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DFAR[31:0] (NS).

AArch64 System register FAR_EL1 bits [63:32] are architecturally mapped to AArch32 System register IFAR[31:0] (NS).

**Attributes**

FAR_EL1 is a 64-bit register.

**Field descriptions**

The FAR_EL1 bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| 63     | 62     | 61     | 60     | 59     | 58     | 57     | 56     | 55     | 54     | 53     | 52     | 51     | 50     | 49     | 48     | 47     | 46     | 45     | 44     | 43     | 42     | 41     | 40     | 39     | 38     | 37     | 36     | 35     | 34     | 33     | 32     |
|---------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Faulting Virtual Address for synchronous exceptions taken to EL1 |
| Faulting Virtual Address for synchronous exceptions taken to EL1 |

**Bits [63:0]**

Faulting Virtual Address for synchronous exceptions taken to EL1. Exceptions that set the FAR_EL1 are Instruction Aborts (EC 0x20 or 0x21), Data Aborts (EC 0x24 or 0x25), PC alignment faults (EC 0x22), and Watchpoints (EC 0x34 or 0x35). ESR_EL1 EC holds the EC value for the exception.

For a synchronous External abort, if the VA that generated the abort was from an address range for which TCR_ELx.TBI[<0|1>] == 1 for the translation regime in use when the abort was generated, then the top eight bits of FAR_EL1 are UNKNOWN.

For a synchronous External abort other than a synchronous External abort on a translation table walk, this field is valid only if ESR_EL1.FnV is 0, and the FAR_EL1 is UNKNOWN if ESR_EL1.FnV is 1.

For all other exceptions taken to EL1, the FAR_EL1 is UNKNOWN.

If a memory fault that sets FAR_EL1, other than a Tag Check Fault, is generated from a data cache maintenance or other DC instruction, this field holds the address specified in the register argument of the instruction.

On an exception due to a Tag Check Fault caused by a data cache maintenance or other DC instruction, the address held in FAR_EL1 is IMPLEMENTATION DEFINED as one of the following:

- The lowest address that gave rise to the fault.
- The address specified in the register argument of the instruction as generated by MMU faults caused by DC ZVA.

If the exception that updates FAR_EL1 is taken from an Exception level that is using AArch32, the top 32 bits are all zero, unless both of the following apply, in which case the top 32 bits of FAR_ELx are 0x00000001:

- The faulting address was generated by a load or store instruction that sequentially incremented from address 0xFFFFFFFF. Such a load or store is CONSTRAINED UNPREDICTABLE.
- The implementation treats such incrementing as setting bit[32] of the virtual address to 1.
For a Data Abort or Watchpoint exception, if address tagging is enabled for the address accessed by the data access that caused the exception, then this field includes the tag. For more information about address tagging, see 'Address tagging in AArch64 state'.

For a synchronous Tag Check Fault abort, bits[63:60] are UNKNOWN.

Execution at EL0 makes FAR_EL1 become UNKNOWN.

---

**Note**

The address held in this field is an address accessed by the instruction fetch or data access that caused the exception that gave rise to the instruction or data abort. It is the lower address that gave rise to the fault. Where different faults from different addresses arise from the same instruction, such as for an instruction that loads or stores a mis-aligned address that crosses a page boundary, the architecture does not prioritize between those different faults.

FAR_EL1 is made UNKNOWN on an exception return from EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the FAR_EL1

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic FAR_EL1 or FAR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, FAR_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
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<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.FAR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x220];
  else
    return FAR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return FAR_EL2;
  else
    return FAR_EL1;
elsif PSTATE.EL == EL3 then
  return FAR_EL1;

MSR FAR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
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</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.FAR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x220] = X[t];
else
  FAR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    FAR_EL2 = X[t];
  else
    FAR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  FAR_EL1 = X[t];

MRS <Xt>, FAR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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</thead>
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</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x220];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return FAR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return FAR_EL1;
  else
    UNDEFINED;

MSR FAR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
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</thead>
<tbody>
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<td>0b101</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '101' then
        NVMem[0x220] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        FAR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() & & ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        FAR_EL1 = X[t];
    else
        UNDEFINED;

MRS <Xt>, FAR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
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<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return FAR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    FAR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    FAR_EL2 = X[t];

MSR FAR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        FAR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    FAR_EL2 = X[t];
else
    FAR_EL2 = X[t];
FAR_EL2, Fault Address Register (EL2)

The FAR_EL2 characteristics are:

**Purpose**

Holds the faulting Virtual Address for all synchronous Instruction or Data Abort, PC alignment fault and Watchpoint exceptions that are taken to EL2.

**Configuration**

AArch64 System register FAR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HDFAR[31:0].

AArch64 System register FAR_EL2 bits [63:32] are architecturally mapped to AArch32 System register HIFAR[31:0].

AArch64 System register FAR_EL2 bits [31:0] are architecturally mapped to AArch32 System register DFAR[31:0] when EL2 is implemented.

AArch64 System register FAR_EL2 bits [63:32] are architecturally mapped to AArch32 System register IFAR[31:0] when EL2 is implemented.

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

FAR_EL2 is a 64-bit register.

**Field descriptions**

The FAR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 |

| Faulting Virtual Address for synchronous exceptions taken to EL2 |
| Faulting Virtual Address for synchronous exceptions taken to EL2 |

**Bits [63:0]**

Faulting Virtual Address for synchronous exceptions taken to EL2. Exceptions that set the FAR_EL2 are Instruction Aborts (EC 0x20 or 0x21), Data Aborts (EC 0x24 or 0x25), PC alignment faults (EC 0x22), and Watchpoints (EC 0x34 or 0x35). ESR_EL2.EC holds the EC value for the exception.

For a synchronous External abort, if the VA that generated the abort was from an address range for which TCR_ELx.TBI{<0|1>} == 1 for the translation regime in use when the abort was generated, then the top eight bits of FAR_EL2 are UNKNOWN.

For a synchronous External abort other than a synchronous External abort on a translation table walk, this field is valid only if ESR_EL2.FnV is 0, and the FAR_EL2 is UNKNOWN if ESR_EL2.FnV is 1.

For all other exceptions taken to EL2, the FAR_EL2 is UNKNOWN.

If a memory fault that sets FAR_EL2, other than a Tag Check Fault, is generated from a data cache maintenance or other DC instruction, this field holds the address specified in the register argument of the instruction.

On an exception due to a Tag Check Fault caused by a data cache maintenance or other DC instruction, the address held in FAR_EL2 is IMPLEMENTATION DEFINED as one of the following:

- The lowest address that gave rise to the fault.
• The address specified in the register argument of the instruction as generated by MMU faults caused by DC ZVA.

If the exception that updates FAR_EL2 is taken from an Exception level that is using AArch32, the top 32 bits are all zero, unless both of the following apply, in which case the top 32 bits of FAR_ELx are 0x00000001:

• The faulting address was generated by a load or store instruction that sequentially incremented from address 0xFFFFFFFF. Such a load or store instruction is CONSTRAINED UNPREDICTABLE.
• The implementation treats such incrementing as setting bit[32] of the virtual address to 1.

For a Data Abort or Watchpoint exception, if address tagging is enabled for the address accessed by the data access that caused the exception, then this field includes the tag. For more information about address tagging, see 'Address tagging in AArch64 state'.

For a synchronous Tag Check Fault abort, bits[63:60] are UNKNOWN.

Execution at EL1 or EL0 makes FAR_EL2 become UNKNOWN.

---

**Note**

The address held in this field is an address accessed by the instruction fetch or data access that caused the exception that gave rise to the instruction or data abort. It is the lower address that gave rise to the fault. Where different faults from different addresses arise from the same instruction, such as for an instruction that loads or stores a mis-aligned address that crosses a page boundary, the architecture does not prioritize between those different faults.

FAR_EL2 is made UNKNOWN on an exception return from EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the FAR_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic FAR_EL2 or FAR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, FAR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.<NV2,NV> == '11' then
        return FAR_EL1;
    elsif EL2Enabled() & HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        return FAR_EL2;
    elsif PSTATE.EL == EL3 then
        return FAR_EL2;

**MSR FAR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        FAR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    FAR_EL2 = X[t];
else
    FAR_EL1 = X[t];

MRS <Xt>, FAR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
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<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TRVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.FAR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return NVMem[0x220];
    end
    return FAR_EL1;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return FAR_EL2;
    else
        return FAR_EL1;
    end
elsif PSTATE.EL == EL3 then
    return FAR_EL1;

MSR FAR_EL1, <Xt>

<table>
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<th>op1</th>
<th>CRn</th>
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<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.FAR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return NVMem[0x220] = X[t];
    end
    FAR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        FAR_EL2 = X[t];
    else
        FAR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    FAR_EL1 = X[t];
FAR_EL3, Fault Address Register (EL3)

The FAR_EL3 characteristics are:

Purpose

Holds the faulting Virtual Address for all synchronous Instruction or Data Abort and PC alignment fault exceptions that are taken to EL3.

Configuration

This register is present only when EL3 is implemented. Otherwise, direct accesses to FAR_EL3 are UNDEFINED.

Attributes

FAR_EL3 is a 64-bit register.

Field descriptions

The FAR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Faulting Virtual Address for synchronous exceptions taken to EL3 |
| Faulting Virtual Address for synchronous exceptions taken to EL3 |

Bits [63:0]

Faulting Virtual Address for synchronous exceptions taken to EL3. Exceptions that set the FAR_EL3 are Instruction Aborts (EC 0x20 or 0x21), Data Aborts (EC 0x24 or 0x25), and PC alignment faults (EC 0x22). ESR_EL3.EC holds the EC value for the exception.

For a synchronous External abort, if the VA that generated the abort was from an address range for which TCR_ELx.TBI{<0|1>} == 1 for the translation regime in use when the abort was generated, then the top eight bits of FAR_EL3 are UNKNOWN.

For a synchronous External abort other than a synchronous External abort on a translation table walk, this field is valid only if ESR_EL3.FnV is 0, and the FAR_EL3 is UNKNOWN if ESR_EL3.FnV is 1.

For all other exceptions taken to EL3, the FAR_EL3 is UNKNOWN.

If a memory fault that sets FAR_EL3, other than a Tag Check Fault, is generated from a data cache maintenance or other DC instruction, this field holds the address specified in the register argument of the instruction.

On an exception due to a Tag Check Fault caused by a data cache maintenance or other DC instruction, the address held in FAR_EL3 is IMPLEMENTATION DEFINED as one of the following:

- The lowest address that gave rise to the fault.
- The address specified in the register argument of the instruction as generated by MMU faults caused by DC ZVA.

If the exception that updates FAR_EL3 is taken from an Exception Level using AArch32, the top 32 bits are all zero, unless both of the following apply, in which case the top 32 bits of FAR_ELx are 0x80000001:

- The faulting address was generated by a load or store instruction that sequentially incremented from address 0xffffffff. Such a load or store instruction is CONSTRAINED UNPREDICTABLE.
- The implementation treats such incrementing as setting bit[32] of the virtual address to 1.

If a Data Abort or Watchpoint exception, if address tagging is enabled for the address accessed by the data access that caused the exception, then this field includes the tag. For more information about address tagging, see ‘Address tagging in AArch64 state’.
For a synchronous Tag Check Fault abort, bits[63:60] are **UNKNOWN**.

Execution at EL2, EL1 or EL0 makes FAR_EL3 become **UNKNOWN**.

---

**Note**

The address held in this register is an address accessed by the instruction fetch or data access that caused the exception that actually gave rise to the instruction or data abort. It is the lowest address that gave rise to the fault. Where different faults from different addresses arise from the same instruction, such as for an instruction that loads or stores a mis-aligned address that crosses a page boundary, the architecture does not prioritize between those different faults.

---

FAR_EL3 is made **UNKNOWN** on an exception return from EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the FAR_EL3

Accesses to this register use the following encodings:

**MRS <Xt>, FAR_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
return FAR_EL3;

**MSR FAR_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
FAR_EL3 = X[t];
FPCR, Floating-point Control Register

The FPCR characteristics are:

**Purpose**

Controls floating-point behavior.

**Configuration**

The named fields in this register map to the equivalent fields in the AArch32 FPSCR.

It is **IMPLEMENTATION DEFINED** whether the Len and Stride fields can be programmed to non-zero values, which will cause some AArch32 floating-point instruction encodings to be **UNDEFINED**, or whether these fields are RAZ.

**Attributes**

FPCR is a 64-bit register.

**Field descriptions**

The FPCR bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
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<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td>RES0</td>
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<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:27]**

Reserved, RES0.

**AHP, bit [26]**

Alternative half-precision control bit.

<table>
<thead>
<tr>
<th>AHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IEEE half-precision format selected.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alternative half-precision format selected.</td>
</tr>
</tbody>
</table>

This bit is used only for conversions between half-precision floating-point and other floating-point formats.

The data-processing instructions added as part of the FEAT_FP16 extension always use the IEEE half-precision format, and ignore the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DN, bit [25]**

Default NaN mode control bit.
DN, bit [23]

NaN operands propagate through to the output of a floating-point operation.

0b1

Any operation involving one or more NaNs returns the Default NaN.

If FPCR.AH is 1, this bit has no effect on the output of the FMAX, FMAXP, FMAXV, FMIN, FMINP, and FMINV instructions, and a default NaN is never returned as a result of these instructions.

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

FZ, bit [24]

Flush-to-zero mode control bit.

0b0

Flush-to-zero mode disabled. Behavior of the floating-point system is fully compliant with the IEEE 754 standard.

0b1

Flush-to-zero mode enabled.

If FPCR.AH is 1:

• This bit does not generate Input Denormal exceptions.
• This bit does not cause input denormal operands to be flushed to zero.
• When the output is flushed to zero:
  ◦ An Inexact floating-point exception is generated.
  ◦ The test for a denormalized number for half-precision, single-precision, and double-precision numbers occurs after rounding with an unbounded exponent.

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

This bit has no effect on half-precision calculations.

If the result of an FMAX, FMAXP, FMAXV, FMIN, FMINP, or FMINV instruction is a denormalized number, it is not flushed to zero, regardless of the value of this bit.

Denormalized outputs of the following instructions, as determined after rounding with an unbounded exponent, are not affected by the value of this bit:

• The BFCVT, BFCVTN, BFCVTN2, BFCVTNT, BFMLALB, and BFMLALT instructions.
• Single-precision and double-precision FRECPE, FRECPS, FRECPX, FRSQRTE, and FRSQRTS instructions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RMode, bits [23:22]

Rounding Mode control field.

0b00

Round to Nearest (RN) mode.

0b01

Round towards Plus Infinity (RP) mode.

0b10

Round towards Minus Infinity (RM) mode.

0b11

Round towards Zero (RZ) mode.

The specified rounding mode is used by both scalar and Advanced SIMD floating-point instructions.

If FPCR.AH is 1, then the following instructions use Round to Nearest mode regardless of the value of this bit:

• The FRECPE, FRECPS, FRECPX, FRSQRTE, and FRSQRTS instructions.
• The BFCVT, BFCVTN, BFCVTN2, BFCVTNT, BFMLALB, and BFMLALT instructions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Stride, bits [21:20]

This field has no function in AArch64 state, and non-zero values are ignored during execution in AArch64 state.

This field is included only for context saving and restoration of the AArch32 FPSCR.Stride field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

FZ16, bit [19]

When FEAT_FP16 is implemented:

Flush-to-zero mode control bit on half-precision data-processing instructions.

<table>
<thead>
<tr>
<th>FZ16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Flush-to-zero mode disabled. Behavior of the floating-point system is fully compliant with the IEEE 754 standard.</td>
</tr>
</tbody>
</table>
| 0b1  | Flush-to-zero mode enabled. If FPCR.AH is 1:  
  • When the output is flushed to zero:  
    ◦ An Inexact floating-point exception is generated.  
    ◦ The test for a denormalized number for half-precision, single-precision, and double-precision numbers occurs after rounding with an unbounded exponent. |

The value of this bit applies to both scalar and Advanced SIMD floating-point half-precision calculations. A half-precision floating-point number that is flushed to zero as a result of the value of the FZ16 bit does not generate an Input Denormal exception.

If the result of an FMAX, FMAXP, FMAXV, FMIN, FMINP, or FMINV instruction is a denormalized number, it is not flushed to zero, regardless of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Len, bits [18:16]

This field has no function in AArch64 state, and non-zero values are ignored during execution in AArch64 state.

This field is included only for context saving and restoration of the AArch32 FPSCR.Len field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IDE, bit [15]

Input Denormal floating-point exception trap enable.

<table>
<thead>
<tr>
<th>IDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the FPSR.IDC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the FPSR.IDC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Bits [14:13]**

Reserved, RES0.

**IXE, bit [12]**

Inexact floating-point exception trap enable.

<table>
<thead>
<tr>
<th>IXE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untracked exception handling selected. If the floating-point exception occurs, the FPSR.IXC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the FPSR.IXC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.

On a warm reset, this field resets to an architecturally UNKNOWN value.

**UFE, bit [11]**

Underflow floating-point exception trap enable.

<table>
<thead>
<tr>
<th>UFE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untracked exception handling selected. If the floating-point exception occurs, the FPSR.UFC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs and Flush-to-zero is not enabled, the PE does not update the FPSR.UFC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.

On a warm reset, this field resets to an architecturally UNKNOWN value.

**OFE, bit [10]**

Overflow floating-point exception trap enable.

<table>
<thead>
<tr>
<th>OFE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untracked exception handling selected. If the floating-point exception occurs, the FPSR.OFC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the FPSR.OFC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.

On a warm reset, this field resets to an architecturally UNKNOWN value.

**DZE, bit [9]**

Divide by Zero floating-point exception trap enable.

<table>
<thead>
<tr>
<th>DZE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untracked exception handling selected. If the floating-point exception occurs, the FPSR.DZC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the FPSR.DZC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### IOE, bit [8]

Invalid Operation floating-point exception trap enable.

<table>
<thead>
<tr>
<th>IOE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the FPSR.IOC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the FPSR.IOC bit.</td>
</tr>
</tbody>
</table>

The value of this bit controls both scalar and Advanced SIMD floating-point arithmetic.

If the implementation does not support this exception, this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [7:3]

Reserved, **RES0**.

### NEP, bit [2]

When FEAT_AFP is implemented:

Controls how the output elements other than the lowest element of the vector are determined for Advanced SIMD scalar instructions.

<table>
<thead>
<tr>
<th>NEP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not affect how the output elements other than the lowest are determined for Advanced SIMD scalar instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>The output elements other than the lowest are taken from the following registers:</td>
</tr>
<tr>
<td></td>
<td>• For 3-input scalar versions of the FMLA (by element) and FMLS (by element) instructions, the &lt;Hd&gt;, &lt;Sd&gt;, or &lt;Dd&gt; register.</td>
</tr>
<tr>
<td></td>
<td>• For 3-input versions of the FMADD, FMSUB, FNMAADD, and FNMSUB instructions, the &lt;Ha&gt;, &lt;Sa&gt;, or &lt;Da&gt; register.</td>
</tr>
<tr>
<td></td>
<td>• For 2-input scalar versions of the FACGE, FACGT, FCMGE (register), FCMGT (register) instructions, the &lt;Hm&gt;, &lt;Sm&gt;, or &lt;Dm&gt; register.</td>
</tr>
<tr>
<td></td>
<td>• For 2-input scalar versions of the FABD, FADD (scalar), FDIV (scalar), FMAX (scalar), FMAXNM (scalar), FMIN (scalar), FMINNM (scalar), FMUL (by element), FMUL (scalar), FMULX, FMUL (scalar), FRECPS, FRSSQRTS, and FSUB (scalar) instructions, the &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register.</td>
</tr>
<tr>
<td></td>
<td>• For 1-input scalar versions of the following instructions, the &lt;Hd&gt;, &lt;Sd&gt;, or &lt;Dd&gt; register:</td>
</tr>
<tr>
<td></td>
<td>• The (vector) versions of the FCVTAS, FCVTAU, FCVTMS, FCVTMU, FCVTNS, FCVTNU, FCVTPS, and FCVTPU instructions.</td>
</tr>
<tr>
<td></td>
<td>• The (vector, fixed-point) and (vector, integer) versions of the FCVTZS, FCVTZU, SCVTFS, and UCVTF instructions.</td>
</tr>
<tr>
<td></td>
<td>• The (scalar) versions of the FABS, FNEG, FRINT32X, FRINT32Z, FRINT64X, FRINT64Z, FRINTA, FRINTI, FRINTM, FRINTP, FRINTX, FRINTZ, and FSQRT instructions.</td>
</tr>
<tr>
<td></td>
<td>• The (integer) versions of the SCVTF and UCVTF instructions.</td>
</tr>
<tr>
<td></td>
<td>• The BFCVT, FCVT, FCVTXN, FRECPE, FRECPX, and FRSQRS instructions.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**AH, bit [1]**

When **FEAT_AFP** is implemented:

Alternate Handling. Controls alternate handling of denormalized floating-point numbers.
<table>
<thead>
<tr>
<th>AH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not affect handling of denormalized floating-point numbers. The sign-bit of the default NaN encoding is set to 1. For all floating-point instructions other than BFDOT and BFMMAL, detection of underflow occurs after rounding with an unbounded exponent. If an operation, other than FMAX, FMAXP, FMAXV, FMIN, FMINP, and FMINV, has two floating-point inputs in the &lt;Vn&gt;, &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register or the &lt;Vm&gt;, &lt;Hm&gt;, &lt;Sm&gt;, or &lt;Dm&gt; register, and two NaN inputs, then the output is derived from the NaN held in the &lt;Vn&gt;, &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register, regardless of whether any input is a signaling NaN or a quiet NaN. For the BFMLALB, BFMLALT, FCMLA, FMADD, FMA, FMLAL, FMLAL2, FMLS, FMLS, FMLSL, FMLS, FMSUB, FNMADD, and FNMSUB instructions, regardless of whether any input is a signaling NaN or a quiet NaN:</td>
</tr>
<tr>
<td></td>
<td>• If the operation has three NaN inputs, then the output is derived from the NaN held in the &lt;Vn&gt;, &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register.</td>
</tr>
<tr>
<td></td>
<td>• If the operation has two NaN inputs and the &lt;Vn&gt;, &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register holds a NaN, then the output is derived from the NaN held in that register.</td>
</tr>
<tr>
<td></td>
<td>• If the operation has two NaN inputs and the &lt;Vn&gt;, &lt;Hn&gt;, &lt;Sn&gt;, or &lt;Dn&gt; register does not hold a NaN, then the output is derived from the NaN held in the &lt;Hm&gt;, &lt;Sm&gt;, or &lt;Dm&gt; register.</td>
</tr>
<tr>
<td>0b1</td>
<td>The FMAX, FMAXP, FMAXV, FMIN, FMINP, and FMINV instructions change their algorithm to calculate the minimum and maximum so that:</td>
</tr>
<tr>
<td></td>
<td>• If the result is a denormalized number, it is not flushed to zero, regardless of FPCR.FZ or FPCR.FZ16.</td>
</tr>
<tr>
<td></td>
<td>• If either input is a quiet NaN or a signaling NaN, then the second operand is returned as the result of the instruction and an Invalid Operation floating-point exception is generated.</td>
</tr>
<tr>
<td></td>
<td>• If the two operands are +0 and -0 in any order, the second operand of the instruction is returned as the result of the instruction.</td>
</tr>
<tr>
<td></td>
<td>• FPCR.DN has no effect on the output and a default NaN is never returned as the result of the instruction.</td>
</tr>
</tbody>
</table>

The FCVTAS, FCVTAU, FCVTPS, FCVTPU, FCVTPS, FCVTPU, FJCVTZS, FJCVTZS, FRINT32X, FRINT32Z, FRINT64X, FRINT64Z, FRINTA, FRINTI, FRINTM, FRINTN, FRINTP, FRINTX, and FRINTZ instructions never generate an Input Denormal floating-point exception.

The BFVCVT, BFVCVTN2, BFVCVTNT, BFVCVTN2, BFVCVTNT, BFMLALB, and BFMLALT instructions: |
|     | • Use Round to Nearest rounding mode, regardless of the rounding mode selected in FPCR.RMode. |
|     | • Flush all denormalized inputs to zero, retaining the sign, regardless of FPCR.FIZ. |
|     | • Flush all denormalized outputs, as determined after rounding with an unbounded exponent, to zero, retaining the sign, regardless of FPCR.FZ. |
|     | • Do not generate any floating-point exceptions, regardless of their input or output values. |

The FRECEP, FRECPS, FRECPX, FRSLRTE, and FRSLRTS instructions: |
|     | • Use Round to Nearest rounding mode, regardless of the rounding mode selected in FPCR.RMode. |
|     | • Do not generate any floating-point exceptions. |
|     | • The single-precision and double-precision variants of these instructions: |
|     | ◦ Flush all denormalized inputs to zero, retaining the sign, regardless of FPCR.FIZ. |
|     | ◦ Flush all denormalized outputs, as determined after rounding with an unbounded exponent, to zero, retaining the sign, regardless of FPCR.FZ. |

When the output is flushed to zero: |
|     | • An Inexact floating-point exception is generated.
The test for a denormalized number for half-precision, single-precision, and double-precision numbers occurs after rounding with an unbounded exponent. If FPCR.FZ is 1, this does not cause any Input Denormal exceptions and does not cause input denormal operands to be flushed to zero. If FPCR.FIZ is 0, any operation that unpacks a denormalized floating-point number, other than a BFloat or half-precision number, will generate an Input Denormal floating-point exception, except when:

- One of the other operands of the instruction is a NaN.
- The operation also generates an Invalid Operation floating-point exception or a Divide by Zero floating-point exception.
- The operation was generated by a BFCVT, BFCVTN, BFCVTN2, or BFCVTNT instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**FIZ, bit [0]**

**When FEAT_AFP is implemented:**

Flush Inputs to Zero. Controls whether single-precision, double-precision, and BFloat16 input operands that are denormalized numbers are flushed to zero.

<table>
<thead>
<tr>
<th>FIZ</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0 | If FPCR.AH is 0, does not affect whether denormalized floating-point inputs are flushed to zero. If FPCR.AH is 1, any operation that unpacks a single-precision or double-precision denormalized floating-point number will generate an Input Denormal floating-point exception, except when:  
  - One of the other operands of the instruction is a NaN.  
  - The operation also generates an Invalid Operation floating-point exception or a Divide by Zero floating-point exception.  
  - The operation was generated by a BFCVTN, BFCVTN2, BFCVT, or a BFCVTNT instruction. |
| 0b1 | All single-precision, double-precision, and BFloat16 input operands that are denormalized numbers, except FABS and FNEG, are flushed to zero, retaining the sign. If FPCR.AH is 1 or FPCR.FZ is 0, denormalized numbers that are flushed to zero by this field do not generate an Input Denormal exception. |

The following instructions are not affected by the value of this bit:

- The BFCVT, BFCVTN, BFCVTN2, BFCVTNT, BFMLALB, and BFMLALT instructions.
- Single-precision and double-precision variants of the FRECPE, FRECPS, FRECPX, FRSQRTE, and FRSQRTS instructions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Accessing the FPCR**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
        UNDEFINED;
    elsif !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CPACR_EL1.FPEN != '11' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x00);
        else
            AArch64.SystemAccessTrap(EL1, 0x07);
        endif
    else
        AArch64.SystemAccessTrap(EL2, 0x07);
    endif
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
            UNDEFINED;
        elsif CPACR_EL1.FPEN == 'x0' then
            AArch64.SystemAccessTrap(EL1, 0x07);
        elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x07);
        elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x07);
        elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x07);
            endif
        else
            return FPCR;
        endif
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
            UNDEFINED;
        elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.SystemAccessTrap(EL2, 0x07);
        elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
            AArch64.SystemAccessTrap(EL2, 0x07);
        elseif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x07);
            endif
        else
            return FPCR;
        endif
    elsif PSTATE.EL == EL3 then
        if CPTR_EL3.TFP == '1' then
            AArch64.SystemAccessTrap(EL3, 0x07);
        else
            return FPCR;
        endif
    else
        return FPCR;
    endif
else
    return FPCR;
endif

FPCR, Floating-point Control Register
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
        UNDEFINED;
    elsif !((EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CPACR_EL1.FPEN != '11') && CPACR_EL1.FPEN == '00' then
        FPCR = X[t];
    else
        AArch64.SystemAccessTrap(EL1, 0x07);
    end if;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
        UNDEFINED;
    elsif CPACR_EL1.FPEN == '00' then
        AArch64.SystemAccessTrap(EL1, 0x07);
    else
        FPCR = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
        UNDEFINED;
    elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x07);
    elseif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == '0x0' then
        AArch64.SystemAccessTrap(EL2, 0x07);
    elseif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x07);
        end if;
    end if;
else
    FPCR = X[t];
end if;
elsif PSTATE.EL == EL3 then
    if CPTR_EL3.TFP == '1' then
        AArch64.SystemAccessTrap(EL3, 0x07);
    else
        FPCR = X[t];
    end if;
else
    FPCR = X[t];
end if;
FPEXC32_EL2, Floating-Point Exception Control register

The FPEXC32_EL2 characteristics are:

**Purpose**

Allows access to the AArch32 register FPEXC from AArch64 state only. Its value has no effect on execution in AArch64 state.

**Configuration**

AArch64 System register FPEXC32_EL2 bits [31:0] are architecturally mapped to AArch32 System register FPEXC[31:0].

This register is present only when EL1 is capable of using AArch32. Otherwise, direct accesses to FPEXC32_EL2 are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, and EL1 is capable of using AArch32, then this register is not RES0.

Implemented only if the implementation includes the Advanced SIMD and floating-point functionality.

**Attributes**

FPEXC32_EL2 is a 64-bit register.

**Field descriptions**

The FPEXC32_EL2 bit assignments are:

| Bit 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|--------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| **RES0** |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:32]**

Reserved, RES0.

**EX, bit [31]**

Exception bit. From Armv8, this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EN, bit [30]**

Enables access to the Advanced SIMD and floating-point functionality from all Exception levels, except that setting this field to 0 does not disable the following:

- VMSR accesses to the FPEXC or FPSID.
- VMRS accesses from the FPEXC, FPSID, MVFR0, MVFR1, or MVFR2.
Meaning

Accesses to the **FPSCR**, and any of the SIMD and floating-point registers Q0-Q15, including their views as D0-D31 registers or S0-S31 registers, are **UNDEFINED** at all Exception levels.

This control permits access to the Advanced SIMD and floating-point functionality at all Exception levels.

Execution of floating-point and Advanced SIMD instructions in AArch32 state can be disabled or trapped by the following controls:

- **CPACR**.cp10, or, if executing at EL0, **CPACR_EL1**.FPEN.
- **FPEXC.EN**.
- If executing in Non-secure state:
  - **HCPTR**.TCP10, or if EL2 is using AArch64, **CPTR_EL2**.TFP.
  - **NSACR**.cp10, or if EL3 is using AArch64, **CPTR_EL3**.TFP.
- For Advanced SIMD instructions only:
  - **CPACR**.ASEDIS.
  - If executing in Non-secure state, **HCPTR**.TASE and **NSACR**.NSTRCDIS.

See the descriptions of the controls for more information.

**Note**

When executing at EL0 using AArch32:

- If EL1 is using AArch64 then behavior is as if the value of FPEXC.EN is 1.
- If EL2 is using AArch64 and enabled in the current Security state, and the value of **HCR_EL2**.(RW, TGE) is {1, 1} then behavior is as if the value of FPEXC.EN is 1.
- If EL2 is using AArch64 and enabled in the current Security state, and the value of **HCR_EL2**.(RW, TGE) is {0, 1} then it is **IMPLEMENTATION DEFINED** whether the behavior is:
  - As if the value of FPEXC.EN is 1.
  - Determined by the value of FPEXC32_EL2.EN, as described in this field description. However, Arm deprecates using the value of FPEXC32_EL2.EN to determine behavior.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DEX, bit [29]**

Defined synchronous exception on floating-point execution.

This field identifies whether a synchronous exception generated by the attempted execution of an instruction was generated by an unallocated encoding. The instruction must be in the encoding space that is identified by the pseudocode function ExecutingCP10or11Instr() returning TRUE. This field also indicates whether the **FPEXC32_EL2.TFV** field is valid.

The meaning of this bit is:

<table>
<thead>
<tr>
<th>DEX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The exception was generated by the attempted execution of an unallocated instruction in the encoding space that is identified by the pseudocode function ExecutingCP10or11Instr(). If <strong>FPEXC32_EL2.TFV</strong> is RW then it is invalid and <strong>UNKNOWN</strong>. If <strong>FPEXC32_EL2.</strong>{IDF, IXF, UFF, OFF, DZF, IOF} are RW then they are invalid and <strong>UNKNOWN</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>The exception was generated during the execution of an unallocated encoding. <strong>FPEXC32_EL2.TFV</strong> is valid and indicates the cause of the exception.</td>
</tr>
</tbody>
</table>

On an exception that sets this bit to 1 the exception-handling routine must clear this bit to 0.

On an implementation that both does not support trapping of floating-point exceptions and implements the AArch32 **FPSCR** {Stride, Len} fields as RAZ, this bit is **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
FP2V, bit [28]

FPINST2 instruction valid bit. From Armv8, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

VV, bit [27]

VECITR valid bit. From Armv8, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TFV, bit [26]

Trapped Fault Valid bit. Valid only when the value of FPEXC.DEX is 1. When valid, it indicates the cause of the exception and therefore whether the FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} bits are valid.

<table>
<thead>
<tr>
<th>TFV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The exception was caused by the execution of a floating-point VABS, VADD, VDIV, VFMA, VFMS, VFNMA, VFNMS, VMLA, VMLS, VMOV, VMUL, VNEG, VNMLA, VNMLS, VNmul, VSQRT, or VSUB instruction when one or both of FPSCR. (Stride, Len) was non-zero. If the FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} bits are RW then they are invalid and UNKNOWN.</td>
</tr>
<tr>
<td>0b1</td>
<td>FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} indicate the presence of trapped floating-point exceptions that had occurred at the time of the exception. Bits are set for all trapped exceptions that had occurred at the time of the exception.</td>
</tr>
</tbody>
</table>

This bit returns a status value and ignores writes.

When the value of FPEXC.DEX is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On an implementation that supports the trapping of floating-point exceptions and implements FPSCR. {Stride, Len} as RAZ, this bit is RAO/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [25:11]

Reserved, RES0.

VECITR, bits [10:8]

Vector iteration count. From Armv8, this field is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IDF, bit [7]

Input Denormal trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Input Denormal exception occurred while FPSCR.IDE was 1:

<table>
<thead>
<tr>
<th>IDF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input Denormal exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input Denormal exception has occurred.</td>
</tr>
</tbody>
</table>

Input Denormal exceptions can occur only when FPSCR.FZ is 1.

Note
A half-precision floating-point value that is flushed to zero because the value of the FPSCR.FZ16 bit is 1 does not generate an Input Denormal exception.

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC32_EL2.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [6:5]**

Reserved, RES0.

**IXF, bit [4]**

Inexact trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Inexact exception occurred while the FPSCR.IXE bit was 1:

<table>
<thead>
<tr>
<th>IXF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inexact exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inexact exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**UFF, bit [3]**

Underflow trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Underflow exception occurred while the FPSCR.UFE was 1:

<table>
<thead>
<tr>
<th>UFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow exception has occurred.</td>
</tr>
</tbody>
</table>

Underflow trapped exceptions can occur:

- On half-precision data-processing instructions only when the FPSCR.FZ16 is 0.
- Otherwise only when the FPSCR.FZ is 0.

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC32_EL2.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**OFF, bit [2]**

Overflow trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Overflow exception occurred while the FPSCR.OFE was 1:

<table>
<thead>
<tr>
<th>OFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Overflow exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overflow exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.
When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DZF, bit [1]**

Divide by Zero trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether a Divide by Zero exception occurred while FPSCR.DZE was 1:

<table>
<thead>
<tr>
<th>DZF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Divide by Zero exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Divide by Zero exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IOF, bit [0]**

Invalid Operation trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Invalid Operation exception occurred while FPSCR.IOE was 1:

<table>
<thead>
<tr>
<th>IOF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalid Operation exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalid Operation exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the FPEXC32_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, FPEXC32_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
    UNDEFINED;
  elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x07);
  elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x07);
  elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x07);
    end if;
  else
    return FPEXC32_EL2;
  end if;
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.TFP == '1' then
    AArch64.SystemAccessTrap(EL3, 0x07);
  else
    FPEXC32_EL2 = X[t];
  end if;
else
  FPEXC32_EL2 = X[t];
endif;

FPEXC32_EL2, Floating-Point Exception Control register

MSR FPEXC32_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

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The FPSR characteristics are:

**Purpose**

Provides floating-point system status information.

**Configuration**

The named fields in this register map to the equivalent fields in the AArch32 FPSCR.

**Attributes**

FPSR is a 64-bit register.

**Field descriptions**

The FPSR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| N  | Z  | C  | V  | QC | RES0 | DC | RES0 | XC | UFC | OFC | DC | RES0 | ZC | OFC | DC | RES0 | ZC | OFC | DC | RES0 | ZC | OFC | DC | RES0 | ZC | OFC | DC | RES0 | ZC | OFC | DC | RES0 |
|----|----|----|----|----|------|----|------|----|-----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|------|----|-----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

*When AArch32 is supported at any Exception level and AArch32 floating-point is implemented:*

Negative condition flag for AArch32 floating-point comparison operations.

**Note**

AArch64 floating-point comparisons set the PSTATE.N flag instead.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Z, bit [30]**

*When AArch32 is supported at any Exception level and AArch32 floating-point is implemented:*

Zero condition flag for AArch32 floating-point comparison operations.

**Note**

AArch64 floating-point comparisons set the PSTATE.Z flag instead.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**C, bit [29]**

*When AArch32 is supported at any Exception level and AArch32 floating-point is implemented:*

Carry condition flag for AArch32 floating-point comparison operations.

---

**Note**

AArch64 floating-point comparisons set the PSTATE.C flag instead.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**V, bit [28]**

*When AArch32 is supported at any Exception level and AArch32 floating-point is implemented:*

Overflow condition flag for AArch32 floating-point comparison operations.

---

**Note**

AArch64 floating-point comparisons set the PSTATE.V flag instead.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**QC, bit [27]**

Cumulative saturation bit, Advanced SIMD only. This bit is set to 1 to indicate that an Advanced SIMD integer operation has saturated since 0 was last written to this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [26:8]**

Reserved, RES0.

**IDC, bit [7]**

Input Denormal cumulative floating-point exception bit. This bit is set to 1 to indicate that the Input Denormal floating-point exception has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the **FPCR.IDE** bit. This bit is set to 1 to indicate a floating-point exception only if **FPCR.IDE** is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [6:5]
Reserved, RES0.

IXC, bit [4]
Inexact cumulative floating-point exception bit. This bit is set to 1 to indicate that the Inexact exception floating-point has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the FPCR.IXE bit. This bit is set to 1 to indicate a floating-point exception only if FPCR.IXE is 0.

The criteria for the Inexact floating-point exception to occur are different in Flush-to-zero mode. For details, see 'Flush-to-zero'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

UFC, bit [3]
Underflow cumulative floating-point exception bit. This bit is set to 1 to indicate that the Underflow floating-point exception has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the FPCR.UFE bit. This bit is set to 1 to indicate a floating-point exception only if FPCR.UFE is 0 or Flush-to-zero is enabled.

The criteria for the Underflow floating-point exception to occur are different in Flush-to-zero mode. For details, see 'Flush-to-zero'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

OFC, bit [2]
Overflow cumulative floating-point exception bit. This bit is set to 1 to indicate that the Overflow floating-point exception has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the FPCR.OFE bit. This bit is set to 1 to indicate a floating-point exception only if FPCR.OFE is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DZC, bit [1]
Divide by Zero cumulative floating-point exception bit. This bit is set to 1 to indicate that the Divide by Zero floating-point exception has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the FPCR.DZE bit. This bit is set to 1 to indicate a floating-point exception only if FPCR.DZE is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IOC, bit [0]
Invalid Operation cumulative floating-point exception bit. This bit is set to 1 to indicate that the Invalid Operation floating-point exception has occurred since 0 was last written to this bit.

How scalar and Advanced SIMD floating-point instructions update this bit depends on the value of the FPCR.IOE bit. This bit is set to 1 to indicate a floating-point exception only if FPCR.IOE is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the FPSR
Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CPACR_EL1.FPEN != '11' then
if EL2Enabled() && HCR_EL2.TGE == '1' then
AArch64.SystemAccessTrap(EL2, 0x00);
else
AArch64.SystemAccessTrap(EL1, 0x07);
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CPACR_EL1.FPEN != '11' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
return FPSR;
elsif PSTATE.EL == EL1 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif CPACR_EL1.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL1, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
return FPSR;
elsif PSTATE.EL == EL2 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
return FPSR;
elsif PSTATE.EL == EL3 then
if CPTR_EL3.TFP == '1' then
AArch64.SystemAccessTrap(EL3, 0x07);
else
return FPSR;
if PSTATE.EL == EL0 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && (HCR_EL2.TGE == '1') then
AArch64.SystemAccessTrap(EL2, 0x00);
else
AArch64.SystemAccessTrap(EL1, 0x07);
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' && (HCR_EL2.TGE == '1') then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '1' && (HCR_EL2.TGE == '1') then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H != '1' && (HCR_EL2.TGE == '1') then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
FPSR = X[t];
elsif PSTATE.EL == EL1 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif CPACR_EL1.FPEN == 'x0' then
AArch64.SystemAccessTrap(EL1, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
FPSR = X[t];
elsif PSTATE.EL == EL2 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.TFP == '1' then
UNDEFINED;
elsif HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HCR_EL2.E2H == '1' && CPTR_EL2.TFP == '1' then
AArch64.SystemAccessTrap(EL2, 0x07);
elsif HaveEL(EL3) && CPTR_EL3.TFP == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x07);
else
FPSR = X[t];
elsif PSTATE.EL == EL3 then
if CPTR_EL3.TFP == '1' then
AArch64.SystemAccessTrap(EL3, 0x07);
else
FPSR = X[t];
GCR_EL1, Tag Control Register.

The GCR_EL1 characteristics are:

**Purpose**

Tag Control Register.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to GCR_EL1 are UNDEFINED.

**Attributes**

GCR_EL1 is a 64-bit register.

**Field descriptions**

The GCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
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<tr>
<td>60</td>
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<td>4</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:17]**

Reserved, RES0.

**RRND, bit [16]**

Controls generation of tag values by the IRG instruction.

<table>
<thead>
<tr>
<th>RRND</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRG generates a tag value as defined by RandomTag().</td>
</tr>
<tr>
<td>0b1</td>
<td>IRG generates an implementation-specific tag value with a</td>
</tr>
<tr>
<td></td>
<td>distribution of tag values no worse than generated with</td>
</tr>
<tr>
<td></td>
<td>GCR_EL1.RRND == 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Exclude, bits [15:0]**

Allocation Tag values excluded from selection by ChooseNonExcludedTag().

If all bits of GCR_EL1.Exclude are 1, then the Allocation Tag value 0 will be used.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GCR_EL1**

Accesses to this register use the following encodings:
MRS \(<Xt>\), GCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if \( \text{PSTATE.EL} == \text{EL0} \) then
UNDEFINED;
elseif \( \text{PSTATE.EL} == \text{EL1} \) then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
     UNDEFINED;
   elseif EL2Enabled() && HCR_EL2.ATA == '0' then
     AArch64.SystemAccessTrap(EL2, 0x18);
   elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
     if Halted() && EDSCR.SDD == '1' then
       UNDEFINED;
     else
       AArch64.SystemAccessTrap(EL3, 0x18);
     else
       return GCR_EL1;
   elsif \( \text{PSTATE.EL} == \text{EL2} \) then
     if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
       UNDEFINED;
     elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
       if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
       else
         AArch64.SystemAccessTrap(EL3, 0x18);
       else
         return GCR_EL1;
   elsif \( \text{PSTATE.EL} == \text{EL3} \) then
     return GCR_EL1;
   return GCR_EL1;

MSR GCR_EL1, \(<Xt>\)
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        GCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        GCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    GCR_EL1 = X[t];
else
    GCR_EL1 = X[t];
*GMID_EL1, Multiple tag transfer ID register*

The GMID_EL1 characteristics are:

**Purpose**

Indicates the block size that is accessed by the LDGM and STGM System instructions.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to GMID_EL1 are **UNDEFINED**.

**Attributes**

GMID_EL1 is a 64-bit register.

**Field descriptions**

The GMID_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-4</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31-28</td>
<td>BS, bits [3:0]</td>
</tr>
<tr>
<td>27-19</td>
<td>Log2 of the block size in words. The minimum supported size is 16B (value == 2) and the maximum is 256B (value == 6).</td>
</tr>
</tbody>
</table>

**Accessing the GMID_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>CRn</th>
<th>op0</th>
<th>op1</th>
<th>op2</th>
<th>CRm</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>0b11</td>
<td>0b001</td>
<td>0b100</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID5 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return GMID_EL1;
    end if
elsif PSTATE.EL == EL2 then
    return GMID_EL1;
elsif PSTATE.EL == EL3 then
    return GMID_EL1;
HACR_EL2, Hypervisor Auxiliary Control Register

The HACR_EL2 characteristics are:

**Purpose**

Controls trapping to EL2 of IMPLEMENTATION DEFINED aspects of EL1 or EL0 operation.

**Note**

Arm recommends that the values in this register do not cause unnecessary traps to EL2 when HCR_EL2.{E2H, TGE} == \{1, 1\}.

**Configuration**

AArch64 System register HACR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HACR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

HACR_EL2 is a 64-bit register.

**Field descriptions**

The HACR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Field Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63–32</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>31–0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HACR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, HACR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HACR_EL2;
elsif PSTATE.EL == EL3 then
  return HACR_EL2;

MSR HACR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HACR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  HACR_EL2 = X[t];

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HAFGRTR_EL2, Hypervisor Activity Monitors Fine-Grained Read Trap Register

The HAFGRTR_EL2 characteristics are:

**Purpose**

Provides controls for traps of MRS reads of Activity Monitors System registers.

**Configuration**

This register is present only when FEAT_AMUv1 is implemented and FEAT_FGT is implemented. Otherwise, direct accesses to HAFGRTR_EL2 are UNDEFINED.

**Attributes**

HAFGRTR_EL2 is a 64-bit register.

**Field descriptions**

The HAFGRTR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>AMEVTYPER16_EL0</td>
<td>MRS reads of AMEVTYPER16_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVTYPER16_EL0 at EL0 using AArch32 are not affected by this bit.</td>
</tr>
<tr>
<td>62</td>
<td>AMEVCTR16_EL0</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>AMEVTYPER15_EL0</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>AMEVCTR15_EL0</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>AMEVTYPER14_EL0</td>
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</tr>
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<td>58</td>
<td>AMEVCTR14_EL0</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>AMEVTYPER13_EL0</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>AMEVCTR13_EL0</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>AMEVTYPER12_EL0</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>AMEVCTR12_EL0</td>
<td></td>
</tr>
<tr>
<td>53</td>
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<td>00</td>
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</tr>
</tbody>
</table>

Bits [63:50]

Reserved, RES0.

AMEVTYPER1<x>_EL0, bit [19+2x], for x = 15 to 0

Trap MRS reads of AMEVTYPER1<x>_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVTYPER1<x> at EL0 using AArch32 when EL1 is using AArch64 to EL2.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
AMEVCNTR1<x>_EL0, bit [18+2x], for x = 15 to 0

Trap MRS reads of AMEVCNTR1<x>_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVCNTR1<x> at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>AMEVCNTR1&lt;x&gt;_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of AMEVCNTR1&lt;x&gt;_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVCNTR1&lt;x&gt; at EL0 using AArch32 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MRS reads of AMEVCNTR1&lt;x&gt;_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MRC reads of AMEVCNTR1&lt;x&gt; at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

AMCNTEN<x>, bit [17x], for x = 1 to 0

Trap MRS reads and MRC reads of multiple System registers.

Enables a trap to EL2 the following operations:

• At EL1 and EL0 using AArch64: MRS reads of AMCNTENCLR<x> EL0 and AMCNTENSET<x> EL0.
• At EL0 using Arch32 when EL1 is using AArch64: MRC reads of AMCNTENCLR<x> and AMCNTENSET<x>.

<table>
<thead>
<tr>
<th>AMCNTEN&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MRS reads at EL1 and EL0 using AArch64 of AMCNTENCLR&lt;x&gt; EL0 and AMCNTENSET&lt;x&gt; EL0 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MRC reads at EL0 using AArch32 of AMCNTENCLR&lt;x&gt; and AMCNTENSET&lt;x&gt; are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Bits [16:5]

Reserved, RES0.

AMEVCNTR0<x>_EL0, bit [x+1], for x = 3 to 0

Trap MRS reads of AMEVCNTR0<x>_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVCNTR0<x> at EL0 using AArch32 when EL1 is using AArch64 to EL2.
AMEVCNTR0<x>_EL0  Meaning
0b0 MRS reads of AMEVCNTR0<x>_EL0 at EL1 and EL0 using AArch64 and MRC reads of AMEVCNTR0<x> at EL0 using AArch32 are not affected by this bit.
0b1 If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:
  • MRS reads of AMEVCNTR0<x>_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.
  • MRC reads of AMEVCNTR0<x> at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Accessing the HAFGRTR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, HAFGRTR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elseslf PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x1E8];
elseslf EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elseslf HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
elseslf Halted() && EDSCR.SDD == '1' then
  AArch64.SystemAccessTrap(EL3, 0x18);
elseslf PSTATE.EL == EL2 then
  return HAFGRTR_EL2;
elseslf PSTATE.EL == EL3 then
  return HAFGRTR_EL2;

MSR HAFGRTR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x1E8] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && SCR_EL3.FGTEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        HAFGRTR_EL2 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    HAFGRTR_EL2 = X[t];
HCR_EL2, Hypervisor Configuration Register

The HCR_EL2 characteristics are:

**Purpose**

Provides configuration controls for virtualization, including defining whether various operations are trapped to EL2.

**Configuration**

AArch64 System register HCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HCR[31:0].

AArch64 System register HCR_EL2 bits [63:32] are architecturally mapped to AArch32 System register HCR2[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

The bits in this register behave as if they are 0 for all purposes other than direct reads of the register if EL2 is not enabled in the current Security state.

**Attributes**

HCR_EL2 is a 64-bit register.

**Field descriptions**

The HCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>TWEDEL</td>
<td>TWE Delay. A 4-bit unsigned number that, when HCR_EL2.TWEEn is 1, encodes the minimum delay in taking a trap of WFE* caused by HCR_EL2.TWE as (2^{(\text{TWEDEL} + 8)}) cycles. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>62</td>
<td>TWEEn</td>
<td>TWE Delay Enable. Enables a configurable delayed trap of the WFE* instruction caused by HCR_EL2.TWE.</td>
</tr>
<tr>
<td>61</td>
<td>TID5</td>
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<tr>
<td>60</td>
<td>DCT</td>
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<td>59</td>
<td>ATA</td>
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<td>58</td>
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<td>57</td>
<td>TTLBSE</td>
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<td>0</td>
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</tbody>
</table>

**TWEDEN, bits [63:60]**

When FEAT_TWED is implemented:

TWE Delay. A 4-bit unsigned number that, when HCR_EL2.TWEDEn is 1, encodes the minimum delay in taking a trap of WFE* caused by HCR_EL2.TWE as \(2^{(\text{TWEDEL} + 8)}\) cycles.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TWEDEn, bit [59]**

When FEAT_TWED is implemented:

TWE Delay Enable. Enables a configurable delayed trap of the WFE* instruction caused by HCR_EL2.TWE.

<table>
<thead>
<tr>
<th>TWEDEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The delay for taking the trap is IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The delay for taking the trap is at least the number of cycles defined in HCR_EL2.TWEDEL.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, res0.

**TID5, bit [58]**

When FEAT_MTE2 is implemented:

Trap ID group 5. Traps the following register accesses to EL2, when EL2 is enabled in the current Security state:

AArch64:

<table>
<thead>
<tr>
<th>TID5</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 and EL0 accesses to ID group 5 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

When the value of HCR_EL2.{E2H, TGE} is {1, 1}, this field has an Effective value of 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, res0.

**DCT, bit [57]**

When FEAT_MTE2 is implemented:

Default Cacheability Tagging. When HCR_EL2.DC is in effect, controls whether stage 1 translations are treated as Tagged or Untagged.

<table>
<thead>
<tr>
<th>DCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 translations are treated as Untagged.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 translations are treated as Tagged.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, res0.

**ATA, bit [56]**

When FEAT_MTE2 is implemented:

Allocation Tag Access. When HCR_EL2.{E2H,TGE} != {1,1}, controls EL1 and EL0 access to Allocation Tags.

When access is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.
- MRS and MSR instructions at EL1 using GCR_EL1, RGSR_EL1, TFSR_EL1, TFSR_EL2, or TFSRE0_EL1 that are not UNDEFINED are trapped to EL2.
ATA

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TTLBOS, bit [55]

When FEAT_EVT is implemented:

Trap TLB maintenance instructions that operate on the Outer Shareable domain. Traps execution of those TLB maintenance instructions at EL1 to EL2, when EL2 is enabled in the current Security state. This applies to the following instructions:

TLBI VMALLE1OS, TLBI VAE1OS, TLBI ASIDE1OS, TLBI VAAE1OS, TLBI VALE1OS, TLBI VAAL1OS, TLBI RVAE1OS, TLBI RVAAL1OS, and TLBI RVAALE1OS.

<table>
<thead>
<tr>
<th>TTLBOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions are trapped to EL2.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TTLBIS, bit [54]

When FEAT_EVT is implemented:

Trap TLB maintenance instructions that operate on the Inner Shareable domain. Traps execution of those TLB maintenance instructions at EL1 to EL2, when EL2 is enabled in the current Security state. This applies to the following instructions:

- When EL1 is using AArch64, TLBI VMALLE1IS, TLBI VAE1IS, TLBI ASIDE1IS, TLBI VAAE1IS, TLBI VALE1IS, TLBI VAAE1IS, TLBI RVAE1IS, TLBI RVAAL1IS, and TLBI RVAALE1IS.
- When EL1 is using AArch32, TLBIALLIS, TLBIMVAIS, TLBIASIDIS, TLBIMVAALIS, and TLBIMVAAALIS.

<table>
<thead>
<tr>
<th>TTLBIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions are trapped to EL2.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EnSCXT, bit [53]
When `FEAT_CSV2` is implemented:

Enable Access to the `SCXTNUM_EL1` and `SCXTNUM_EL0` registers. The defined values are:

<table>
<thead>
<tr>
<th>EnSCXT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When (HCR_EL2.TGE==0 or HCR_EL2.E2H==0) and EL2 is enabled in the current Security state, EL1 and EL0 access to <code>SCXTNUM_EL0</code> and EL1 access to <code>SCXTNUM_EL1</code> is disabled by this mechanism, causing an exception to EL2, and the values of these registers to be treated as 0. When ((HCR_EL2.TGE==1 and HCR_EL2.E2H==1) and EL2 is enabled in the current Security state, EL0 access to <code>SCXTNUM_EL0</code> is disabled by this mechanism, causing an exception to EL2, and the value of this register to be treated as 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause accesses to <code>SCXTNUM_EL0</code> or <code>SCXTNUM_EL1</code> to be trapped.</td>
</tr>
</tbody>
</table>

When `FEAT_VHE` is implemented, and the value of `HCR_EL2.{E2H, TGE}` is `{1,1}`, this bit has no effect on execution at EL0.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

Otherwise:

Reserved, RES0.

**TOCU, bit [52]**

When `FEAT_EVT` is implemented:

Trap cache maintenance instructions that operate to the Point of Unification. Traps execution of those cache maintenance instructions to EL2, when EL2 is enabled in the current Security state. This applies to the following instructions:

- When `SCTLR_EL1.UCI` is 1, HCR_EL2.{TGE, E2H} is not `{1, 1}`, and EL0 is using AArch64, `IC IVAU, DC CVAU`.
- When EL1 is using AArch64, `IC IVAU, IC IALLU, DC CVAU`.
- When EL1 is using AArch32, `ICIMVAU, ICIALLU, DCCMVAU`.

**Note**

An exception generated because an instruction is `UNDEFINED` at EL0 is higher priority than this trap to EL2. In addition:

- `IC IALLUIS` and `IC IALLU` are always `UNDEFINED` at EL0 using AArch64.
- `ICIMVAU, ICIALLU, ICIALLUIS,` and `DCCMVAU` are always `UNDEFINED` at EL0 using AArch32.

<table>
<thead>
<tr>
<th>TOCU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions are trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of data cache, it is `IMPLEMENTATION DEFINED` whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is `IMPLEMENTATION DEFINED` whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.

When `FEAT_VHE` is implemented, and the value of `HCR_EL2.{E2H, TGE}` is `{1,1}`, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.
Otherwise:

Reserved, RES0.

**AMVOFFEN, bit [51]**

*When FEAT_AMUv1p1 is implemented:*

Activity Monitors Virtual Offsets Enable.

<table>
<thead>
<tr>
<th>AMVOFFEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtualization of the Activity Monitors is disabled. Indirect reads of the virtual offset registers are zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtualization of the Activity Monitors is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**TICAB, bit [50]**

*When FEAT_EVT is implemented:*

Trap ICIALLUIS/IC IALLUIS cache maintenance instructions. Traps execution of those cache maintenance instructions at EL1 to EL2, when EL2 is enabled in the current Security state. This applies to the following instructions:

- When EL1 is using AArch64, **ICIALLUIS**.
- When EL1 is using AArch32, **ICIALLUIS**.

<table>
<thead>
<tr>
<th>TICAB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 execution of the specified instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of instruction cache, it is **IMPLEMENTATION DEFINED** whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.

When **FEAT_VHE** is implemented, and the value of **HCR_EL2.(E2H, TGE)** is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**TID4, bit [49]**

*When FEAT_EVT is implemented:*

Trap ID group 4. Traps the following register accesses to EL2, when EL2 is enabled in the current Security state:

**AArch64:**

- EL1 reads of **CCSIDR_EL1, CCSIDR2_EL1, CLIDR_EL1**, and **CSSELR_EL1**.
- EL1 writes to **CSSELR_EL1**.

**AArch32:**

- EL1 reads of **CCSIDR, CCSIDR2, CLIDR**, and **CSSELR**.
- EL1 writes to **CSSELR**.
<table>
<thead>
<tr>
<th>TID4</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 and EL0 accesses to ID group 4 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bit [48]**

Reserved, RES0.

**FIEN, bit [47]**

**When FEAT_RASv1p1 is implemented:**

Fault Injection Enable. Unless this bit is set to 1, accesses to the ERXPFGCDN_EL1, ERXPFGCTL_EL1, and ERXPFGF_EL1 registers from EL1 generate a Trap exception to EL2, when EL2 is enabled in the current Security state, reported using EC syndrome value 0x18.

<table>
<thead>
<tr>
<th>FIEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to the specified registers from EL1 are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If EL2 is disabled in the current Security state, the Effective value of HCR_EL2.FIEN is 0b1.

If ERRIDR_EL1.NUM is zero, meaning no error records are implemented, or no error record accessible using System registers is owned by a node that implements the RAS Common Fault Injection Model Extension, then this bit might be RES0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**FWB, bit [46]**

**When FEAT_S2FWB is implemented:**

Forced Write-Back. Defines the combined cacheability attributes in a 2 stage translation regime.

**Note**

When FEAT_MTE2 is implemented, if the stage 1 page or block descriptor specifies the Tagged attribute, the final memory type is Tagged only if the final cacheable memory type is Inner and Outer Write-back cacheable and the final allocation hints are Read-Allocate, Write-Allocate.
Meaning

<table>
<thead>
<tr>
<th>FWB</th>
<th>When this bit is 0, then:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>• The combination of stage 1 and stage 2 translations on memory type and cacheability attributes are as described in the Armv8.0 architecture. For more information, see 'Combining the stage 1 and stage 2 attributes, EL1&amp;0 translation regime'.</td>
</tr>
<tr>
<td></td>
<td>• The encoding of the stage 2 memory type and cacheability attributes in bits[5:2] of the stage 2 page or block descriptors are as described in the Armv8.0 architecture.</td>
</tr>
<tr>
<td>0b1</td>
<td>When this bit is 1, then:</td>
</tr>
<tr>
<td></td>
<td>• Bit[5] of stage 2 page or block descriptor is RES0.</td>
</tr>
<tr>
<td></td>
<td>• When bit[4] of stage 2 page or block descriptor is 1 and when:</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b11, the resultant memory type and inner or outer cacheability attribute is the same as the stage 1 memory type and inner or outer cacheability attribute.</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b10, the resultant memory type and attribute is Normal Write-Back.</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b0x, the resultant memory type will be Normal Non-cacheable except where the stage 1 memory type was Device-&lt;attr&gt; the resultant memory type will be Device-&lt;attr&gt;</td>
</tr>
<tr>
<td></td>
<td>• When bit[4] of stage 2 page or block descriptor is 0 the memory type is Device, and when:</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b00, the stage 2 memory type is Device-nGnRnE.</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b01, the stage 2 memory type is Device-nGnRE.</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b10, the stage 2 memory type is Device-nGRE.</td>
</tr>
<tr>
<td></td>
<td>◦ Bits[3:2] of stage 2 page or block descriptor are 0b11, the stage 2 memory type is Device-GRE.</td>
</tr>
<tr>
<td></td>
<td>• If the stage 1 translation specifies a cacheable memory type, then the stage 1 cache allocation hint is applied to the final cache allocation hint where the final memory type is cacheable.</td>
</tr>
<tr>
<td></td>
<td>• If the stage 1 translation does not specify a cacheable memory type, then if the final memory type is cacheable, it is treated as read allocate, write allocate.</td>
</tr>
</tbody>
</table>

The stage 1 and stage 2 memory types are combined in the manner described in 'Combining the stage 1 and stage 2 attributes, EL1&0 translation regime'.

In Secure state, this bit applies to both the Secure stage 2 translation and the Non-secure stage 2 translation.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

NV2, bit [45]

When FEAT_NV2 is implemented:

Nested Virtualization. Changes the behaviors of HCR_EL2.(NV1, NV) to provide a mechanism for hardware to transform reads and writes from System registers into reads and writes from memory.
When HCR_EL2.NV is 0, the Effective value of this field is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**AT, bit [44]**

When FEAT_NV is implemented:

Address Translation. EL1 execution of the following address translation instructions is trapped to EL2, when EL2 is enabled in the current Security state, reported using EC syndrome value 0x18:

- AT S1E0R, AT S1E0W, AT S1E1R, AT S1E1W, AT S1E1RP, AT S1E1WP.

<table>
<thead>
<tr>
<th>AT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 execution of the specified instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**NV1, bit [43]**

When FEAT_NV2 is implemented:

Nested Virtualization.

<table>
<thead>
<tr>
<th>NV1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If HCR_EL2.{NV2, NV} are both 1, accesses executed from EL1 to implemented EL12, EL02, or EL2 registers are transformed to loads and stores. If HCR_EL2.NV2 is 0 or HCR_EL2.{NV2, NV} == {1, 0}, this control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If HCR_EL2.NV1 defines which EL1 register accesses are transformed to loads and stores. If HCR_EL2.NV2 is 1, accesses executed from EL1 to implemented EL2 registers are transformed to loads and stores. If HCR_EL2.NV2 is 0, EL1 accesses to VBAR_EL1, ELR_EL1, SPSR_EL1, and, when FEAT_CSV2 is implemented, SCXTNUM_EL1, are trapped to EL2, when EL2 is enabled in the current Security state, and are reported using EC syndrome value 0x18.</td>
</tr>
</tbody>
</table>

If HCR_EL2.NV2 is 1, the value of HCR_EL2.NV1 defines which EL1 register accesses are transformed to loads and stores. These transformed accesses have priority over the trapping of registers.

The trapping of EL1 registers caused by other control bits has priority over the transformation of these accesses.

If a register is specified that is not implemented by an implementation, then access to that register are UNDEFINED.

For the list of registers affected, see 'Enhanced support for nested virtualization'.
If HCR_EL2.{NV1, NV} is {0, 1}, any exception taken from EL1, and taken to EL1, causes the SPSR_EL1.M[3:2] to be set to 0b10, and not 0b01.

If HCR_EL2.{NV1, NV} is {1, 1}, then:

- The EL1 translation table Block and Page descriptors:
  - Bit[54] holds the PXN instead of the UXN.
  - Bit[53] is RES0.
  - Bit[6] is treated as 0 regardless of the actual value.
- If Hierarchical Permissions are enabled, the EL1 translation table Table descriptors are as follows:
  - Bit[61] is treated as 0 regardless of the actual value.
  - Bit[60] holds the PXNTable instead of the UXNTable.
  - Bit[59] is RES0.
- When executing at EL1, the PSTATE.PAN bit is treated as zero for all purposes except reading the value of the bit.
- When executing at EL1, the LDTR* instructions are treated as the equivalent LDR* instructions, and the STTR* instructions are treated as the equivalent STR* instructions.

If HCR_EL2.{NV1, NV} are {1, 0}, then the behavior is a CONSTRAINED UNPREDICTABLE choice of:

- Behaving as if HCR_EL2.NV is 1 and HCR_EL2.NV1 is 1 for all purposes other than reading than reading back the value of the HCR_EL2.NV bit.
- Behaving as if HCR_EL2.NV is 0 and HCR_EL2.NV1 is 0 for all purposes other than reading than reading back the value of the HCR_EL2.NV1 bit.
- Behaving with regard to the HCR_EL2.NV and HCR_EL2.NV1 bits behavior as defined in the rest of this description.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When FEAT_NV is implemented:

Nested Virtualization. EL1 accesses to certain registers are trapped to EL2, when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>NV1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to VBAR_EL1, ELR_EL1, SPSR_EL1, and, when FEAT_CSV2 is implemented, SCXNUM_EL1, are trapped to EL2, when EL2 is enabled in the current Security state, and are reported using EC syndrome value 0x18.</td>
</tr>
</tbody>
</table>

If HCR_EL2.NV is 1 and HCR_EL2.NV1 is 0, then the following effects also apply:

- Any exception taken from EL1, and taken to EL1, causes the SPSR_EL1.M[3:2] to be set to 0b10, and not 0b01.

If HCR_EL2.NV and HCR_EL2.NV1 are both set to 1, then the following effects also apply:

- The EL1 translation table Block and Page descriptors:
  - Bit[54] holds the PXN instead of the UXN.
  - Bit[53] is RES0.
  - Bit[6] is treated as 0 regardless of the actual value.
- If Hierarchical Permissions are enabled, the EL1 translation table Table descriptors are as follows:
  - Bit[61] is treated as 0 regardless of the actual value.
  - Bit[60] holds the PXNTable instead of the UXNTable.
  - Bit[59] is RES0.
- When executing at EL1, the PSTATE.PAN bit is treated as zero for all purposes except reading the value of the bit.
- When executing at EL1, the LDTR* instructions are treated as the equivalent LDR* instructions, and the STTR* instructions are treated as the equivalent STR* instructions.

If HCR_EL2.NV is 0 and HCR_EL2.NV1 is 1, then the behavior is a CONSTRAINED UNPREDICTABLE choice of:

- Behaving as if HCR_EL2.NV is 1 and HCR_EL2.NV1 is 1 for all purposes other than reading than reading back the value of the HCR_EL2.NV bit.
- Behaving as if HCR_EL2.NV is 0 and HCR_EL2.NV1 is 0 for all purposes other than reading than reading back the value of the HCR_EL2.NV1 bit.
• Behaving with regard to the HCR_EL2.NV and HCR_EL2.NV1 bits behavior as defined in the rest of this description.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**NV, bit [42]**

**When FEAT_NV2 is implemented:**

Nested Virtualization.

When HCR_EL2.NV2 is 1, redefines register accesses so that:

• Instructions accessing the Special purpose registers `SPSR_EL2` and `ELR_EL2` instead access `SPSR_EL1` and `ELR_EL1` respectively.

• Instructions accessing the System registers `ESR_EL2` and `FAR_EL2` instead access `ESR_EL1` and `FAR_EL1`.

When HCR_EL2.NV2 is 0, or if FEAT_NV2 is not implemented, traps functionality that is permitted at EL2 and would be **UNDEFINED** at EL1 if this field was 0, when EL2 is enabled in the current Security state. This applies to the following operations:

• EL1 accesses to Special-purpose registers that are not **UNDEFINED** at EL2.

• EL1 accesses to System registers that are not **UNDEFINED** at EL2.

• Execution of EL1 or EL2 translation regime address translation and TLB maintenance instructions for EL2 and above.

<table>
<thead>
<tr>
<th>NV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When this bit is set to 0, then the PE behaves as if HCR_EL2.NV2 is 0 for all purposes other than reading this register. This control does not cause any instructions to be trapped. When HCR_EL2.NV2 is 1, no FEAT_NV2 functionality is implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>When HCR_EL2.NV2 is 0, or if FEAT_NV2 is not implemented, EL1 accesses to the specified registers or the execution of the specified instructions are trapped to EL2, when EL2 is enabled in the current Security state. EL1 read accesses to the <code>CurrentEL</code> register return a value of 0x2. When HCR_EL2.NV2 is 1, this control redefines EL1 register accesses so that instructions accessing <code>SPSR_EL2</code>, <code>ELR_EL2</code>, <code>ESR_EL2</code>, and <code>FAR_EL2</code> instead access <code>SPSR_EL1</code>, <code>ELR_EL1</code>, <code>ESR_EL1</code>, and <code>FAR_EL1</code> respectively.</td>
</tr>
</tbody>
</table>

When HCR_EL2.NV2 is 0, or if FEAT_NV2 is not implemented, then:

• The System or Special-purpose registers for which accesses are trapped and reported using EC syndrome value 0x18 are as follows:
  ◦ Registers accessed using MRS or MSR with a name ending in _EL2, except `SP_EL2`.
  ◦ Registers accessed using MRS or MSR with a name ending in _EL12.
  ◦ Registers accessed using MRS or MSR with a name ending in _EL02.
  ◦ Special-purpose registers `SPSR_irq`, `SPSR_abt`, `SPSR_und` and `SPSR_fiq`, accessed using MRS or MSR.
  ◦ Special-purpose register `SP_EL1` accessed using the dedicated MRS or MSR instruction.

• The instructions for which the execution is trapped and reported using EC syndrome value 0x18 are as follows:
  ◦ EL2 translation regime Address Translation instructions and TLB maintenance instructions.
  ◦ EL1 translation regime Address Translation instructions and TLB maintenance instructions that are accessible only from EL2 and EL3.

• The instructions for which the execution is trapped as follows:
  ◦ SMC in an implementation that does not include EL3 and when HCR_EL2.TSC is 1. HCR_EL2.TSC bit is not RES0 in this case. This is reported using EC syndrome value 0x17.
  ◦ The ERET, ERETTAA, and ERETAB instructions, reported using EC syndrome value 0x1A.

**Note**
The priority of this trap is higher than the priority of the HCR_EL2.API trap. If both of these bits are set so that EL1 execution of an ERETAA or ERETAB instruction is trapped to EL2, then the syndrome reported is 0x1A.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When FEAT_NV is implemented:**

Nested Virtualization. Traps functionality that is permitted at EL2 and would be **UNDEFINED** at EL1 if this field was 0, when EL2 is enabled in the current Security state. This applies to the following operations:

- EL1 accesses to Special-purpose registers that are not **UNDEFINED** at EL2.
- EL1 accesses to System registers that are not **UNDEFINED** at EL2.
- Execution of EL1 or EL2 translation regime address translation and TLB maintenance instructions for EL2 and above.

The possible values are:

<table>
<thead>
<tr>
<th>NV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to the specified registers or the execution of the specified instructions are trapped to EL2, when EL2 is enabled in the current Security state. EL1 read accesses to the <strong>CurrentEL</strong> register return a value of 0x2.</td>
</tr>
</tbody>
</table>

The System or Special-purpose registers for which accesses are trapped and reported using EC syndrome value 0x18 are as follows:

- Registers accessed using MRS or MSR with a name ending in _EL2, except **SP_EL2**.
- Registers accessed using MRS or MSR with a name ending in _EL12.
- Registers accessed using MRS or MSR with a name ending in _EL02.
- Special-purpose registers **SPSR_irq**, **SPSR_abt**, **SPSR_und** and **SPSR_fiq**, accessed using MRS or MSR.
- Special-purpose register **SP_EL1** accessed using the dedicated MRS or MSR instruction.

The instructions for which the execution is trapped and reported using EC syndrome value 0x18 are as follows:

- EL2 translation regime Address Translation instructions and TLB maintenance instructions.
- EL1 translation regime Address Translation instructions and TLB maintenance instructions that are accessible only from EL2 and EL3.

The execution of the ERET, ERETAA, and ERETAB instructions are trapped and reported using EC syndrome value 0x1A

**Note**

The priority of this trap is higher than the priority of the HCR_EL2.API trap. If both of these bits are set so that EL1 execution of an ERETAA or ERETAB instruction is trapped to EL2, then the syndrome reported is 0x1A.

The execution of the SMC instructions in an implementation that does not include EL3 and when HCR_EL2.TSC is 1 are trapped and reported using EC syndrome value 0x17. HCR_EL2.TSC bit is not **RES0** in this case.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.
API, bit [41]

When FEAT_PAuth is implemented:

Controls the use of instructions related to Pointer Authentication:

- In EL0, when HCR_EL2.TGE==0 or HCR_EL2.E2H==0, and the associated SCTLR_EL1.En<N><M>=1.
- In EL1, the associated SCTLR_EL1.En<N><M>=1.

Traps are reported using EC syndrome value 0x09. The Pointer Authentication instructions trapped are:

- AUTDA, AUTDB, AUTDZA, AUTDZB, AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZA, AUTIZB.
- PACGA, PACDA, PACDB, PACDZA, PACDZB, PACIA, PACIA1716, PACIASP, PACIAZ, PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZA, PACIZB.
- RETAA, RETAB, BRAA, BRAB, BLRAA, BLRAB, BRAAZ, BRABZ, BLRAAZ, BLRABZ.
- ERETTA, ERETTAB, LDRAA and LDRAB.

<table>
<thead>
<tr>
<th>API</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0 | The instructions related to Pointer Authentication are trapped to EL2, when EL2 is enabled in the current Security state and the instructions are enabled for the EL1&0 translation regime, from:  
    - EL0 when HCR_EL2.TGE==0 or HCR_EL2.E2H==0.  
    - EL1.  
    If HCR_EL2.NV is 1, the HCR_EL2.NV trap takes precedence over the HCR_EL2.API trap for the ERETTA and ERETTAB instructions.  
    If EL2 is implemented and enabled in the current Security state and HFGITR_EL2.ERET == 1, execution at EL1 using AArch64 of ERETTA or ERETTAB instructions is reported with EC syndrome value 0x1A with its associated ISS field, as the fine-grained trap has higher priority than the HCR_EL2.API == 0. |
| 0b1 | This control does not cause any instructions to be trapped. |

If FEAT_PAuth is implemented but EL2 is not implemented or disabled in the current Security state, the system behaves as if this bit is 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

APK, bit [40]

When FEAT_PAuth is implemented:

Trap registers holding “key” values for Pointer Authentication. Traps accesses to the following registers from EL1 to EL2, when EL2 is enabled in the current Security state, reported using EC syndrome value 0x18:

- APITKeyLo_EL1, APITKeyHI_EL1, APITKeyLo_EL1, APITKeyHI_EL1, APDKeyLo_EL1, APDKeyHi_EL1, APDKeyLo_EL1, APDKeyHi_EL1.

<table>
<thead>
<tr>
<th>APK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to the registers holding “key” values for pointer authentication from EL1 are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

Note

If FEAT_PAuth is implemented but EL2 is not implemented or is disabled in the current Security state, the system behaves as if this bit is 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**Bit [39]**

Reserved, RES0.

**MIOCNCE, bit [38]**

Mismatched Inner/Outer Cacheable Non-Coherency Enable, for the EL1&0 translation regimes.

<table>
<thead>
<tr>
<th>MIOCNCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For the EL1&amp;0 translation regimes, for permitted accesses to a memory location that use a common definition of the Shareability and Cacheability of the location, there must be no loss of coherency if the Inner Cacheability attribute for those accesses differs from the Outer Cacheability attribute.</td>
</tr>
<tr>
<td>0b1</td>
<td>For the EL1&amp;0 translation regimes, for permitted accesses to a memory location that use a common definition of the Shareability and Cacheability of the location, there might be a loss of coherency if the Inner Cacheability attribute for those accesses differs from the Outer Cacheability attribute.</td>
</tr>
</tbody>
</table>

For more information see 'Mismatched memory attributes'.

This field can be implemented as RAZ/WI.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TEA, bit [37]**

When FEAT_RAS is implemented:

Route synchronous External abort exceptions to EL2.

<table>
<thead>
<tr>
<th>TEA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause exceptions to be routed from EL0 and EL1 to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Route synchronous External abort exceptions from EL0 and EL1 to EL2, when EL2 is enabled in the current Security state, if not routed to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TERR, bit [36]**

When FEAT_RAS is implemented:

Trap Error record accesses. Trap accesses to the RAS error registers from EL1 to EL2 as follows:

- If EL1 is using AArch64 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value 0x18:
  - ERRIDR_EL1, ERRSELR_EL1, ERXADDR_EL1, ERXCTLR_EL1, ERXFR_EL1, ERXMISC0_EL1, ERXMISC1_EL1, and ERXSTATUS_EL1.

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When FEAT_RASv1p1 is implemented, ERXMISC2_EL1, and ERXMISC3_EL1.

- If EL1 is using AArch32 state, MCR or MRC accesses are trapped to EL2, reported using EC syndrome value 0x03, MCRR or MRRC accesses are trapped to EL2, reported using EC syndrome value 0x04:
  - ERRIDR, ERRSELB, ERXADDR, ERXADDR2, ERXCTRLR, ERXCTRLR2, ERXF, ERXF2, ERXMISC0, ERXMISC1, ERXMISC2, ERXMISC3, and ERXSTATUS.
- When FEAT_RASv1p1 is implemented, ERXMISC4, ERXMISC5, ERXMISC6, and ERXMISC7.

<table>
<thead>
<tr>
<th>TERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to the specified registers from EL1 generate a Trap exception to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TLOR, bit [35]

When FEAT_LOR is implemented:

Trap LOR registers. Traps Non-secure EL1 accesses to LORSA_EL1, LOREA_EL1, LORN_EL1, LORC_EL1, and LORID_EL1 registers to EL2.

<table>
<thead>
<tr>
<th>TLOR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to the LOR registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

E2H, bit [34]

When FEAT_VHE is implemented:

EL2 Host. Enables a configuration where a Host Operating System is running in EL2, and the Host Operating System's applications are running in EL0.

<table>
<thead>
<tr>
<th>E2H</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The facilities to support a Host Operating System at EL2 are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>The facilities to support a Host Operating System at EL2 are enabled.</td>
</tr>
</tbody>
</table>

For information on the behavior of this bit see ‘Behavior of HCR_EL2.E2H’.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
ID, bit [33]

Stage 2 Instruction access cacheability disable. For the EL1&0 translation regime, when EL2 is enabled in the current Security state and HCR_EL2.VM==1, this control forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable.

<table>
<thead>
<tr>
<th>ID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on stage 2 of the EL1&amp;0 translation regime.</td>
</tr>
<tr>
<td>0b1</td>
<td>Forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL2, EL2&0, or EL3 translation regimes.

When FEAT_VHE is implemented, and the value of HCR_EL2 (E2H, TGE) is {1, 1}, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CD, bit [32]

Stage 2 Data access cacheability disable. For the EL1&0 translation regime, when EL2 is enabled in the current Security state and HCR_EL2.VM==1, this control forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable.

<table>
<thead>
<tr>
<th>CD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on stage 2 of the EL1&amp;0 translation regime for data accesses and translation table walks.</td>
</tr>
<tr>
<td>0b1</td>
<td>Forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL2, EL2&0, or EL3 translation regimes.

When FEAT_VHE is implemented, and the value of HCR_EL2 (E2H, TGE) is {1, 1}, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RW, bit [31]

When AArch32 is supported at any Exception level:

Execution state control for lower Exception levels:

<table>
<thead>
<tr>
<th>RW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Lower levels are all AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Execution state for EL1 is AArch64. The Execution state for EL0 is determined by the current value of PSTATE.nRW when executing at EL0.</td>
</tr>
</tbody>
</table>

If AArch32 state is not supported by the implementation at EL1, then this bit is RAO/WI.

In an implementation that includes EL3, when EL2 is not enabled in Secure state, the PE behaves as if this bit has the same value as the SCR_EL3.RW bit for all purposes other than a direct read or write access of HCR_EL2.

The RW bit is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of HCR_EL2 (E2H, TGE) is {1, 1}, this field behaves as 1 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAO/WI.
TRVM, bit [30]

Trap Reads of Virtual Memory controls. Traps EL1 reads of the virtual memory control registers to EL2, when EL2 is enabled in the current Security state, as follows:

- If EL1 is using AArch64 state, the following registers are trapped to EL2 and reported using EC syndrome value 0x18:
  - SCTLR_EL1, TTBR0_EL1, TTBR1_EL1, TCR_EL1, ESR_EL1, FAR_EL1, AFSR0_EL1, AFSR1_EL1, MAIR_EL1, AMAIR_EL1, CONTEXTIDR_EL1.

- If EL1 is using AArch32 state, accesses using MRC to the following registers are trapped to EL2 and reported using EC syndrome value 0x03, accesses using MRRC are trapped to EL2 and reported using EC syndrome value 0x04:
  - SCTLR, TTBR0, TTBR1, TTBCR, TTBCR2, DACR, DFSR, IFSR, DFAR, IFAR, ADFSR, AIFSR, PRRR, NMRR, MAIR0, MAIR1, AMAIR0, AMAIR1, CONTEXTIDR.

<table>
<thead>
<tr>
<th>TRVM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 read accesses to the specified Virtual Memory controls are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When **HCR_EL2.TGE** is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

**Note**

EL2 provides a second stage of address translation, that a hypervisor can use to remap the address map defined by a Guest OS. In addition, a hypervisor can trap attempts by a Guest OS to write to the registers that control the memory system. A hypervisor might use this trap as part of its virtualization of memory management.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

HCD, bit [29]

**When EL3 is not implemented:**

HVC instruction disable. Disables EL1 execution of HVC instructions, from both Execution states, when EL2 is enabled in the current Security state, reported using EC syndrome value 0x00.

<table>
<thead>
<tr>
<th>HCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>HVC instruction execution is enabled at EL2 and EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>HVC instructions are UNDEFINED at EL2 and EL1. Any resulting exception is taken to the Exception level at which the HVC instruction is executed.</td>
</tr>
</tbody>
</table>

**Note**

HVC instructions are always UNDEFINED at EL0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

TDZ, bit [28]

Trap **DC ZVA** instructions. Traps EL0 and EL1 execution of **DC ZVA** instructions to EL2, when EL2 is enabled in the current Security state, from AArch64 state only, reported using EC syndrome value 0x18.

If **FEAT_MTE2** is implemented, this trap also applies to **DC GVA** and **DC GZVA**.
TDZ

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1 In AArch64 state, any attempt to execute an instruction this trap applies to at EL1, or at EL0 when the instruction is not UNDEFINED at EL0, is trapped to EL2 when EL2 is enabled in the current Security state. Reading the DCZID_EL0 returns a value that indicates that the instructions this trap applies to are not supported.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.E2H, TGE is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TGE, bit [27]

Trap General Exceptions, from EL0.

<table>
<thead>
<tr>
<th>TGE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on execution at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>When EL2 is not enabled in the current Security state, this control has no effect on execution at EL0. When EL2 is enabled in the current Security state, in all cases:</td>
</tr>
<tr>
<td>•</td>
<td>All exceptions that would be routed to EL1 are routed to EL2.</td>
</tr>
<tr>
<td>•</td>
<td>If EL1 is using AArch64, the SCTLR_EL1.M field is treated as being 0 for all purposes other than returning the result of a direct read of SCTLR_EL1.</td>
</tr>
<tr>
<td>•</td>
<td>If EL1 is using AArch32, the SCTLR.M field is treated as being 0 for all purposes other than returning the result of a direct read of SCTLR.</td>
</tr>
<tr>
<td>•</td>
<td>All virtual interrupts are disabled.</td>
</tr>
<tr>
<td>•</td>
<td>Any IMPLEMENTATION DEFINED mechanisms for signaling virtual interrupts are disabled.</td>
</tr>
<tr>
<td>•</td>
<td>An exception return to EL1 is treated as an illegal exception return.</td>
</tr>
<tr>
<td>•</td>
<td>The MDCR_EL2.TDRA, TDOSA, TDA, TDE fields are treated as being 1 for all purposes other than returning the result of a direct read of MDCR_EL2.</td>
</tr>
</tbody>
</table>

In addition, when EL2 is enabled in the current Security state, if:

| &bull; | HCR_EL2.E2H is 0, the Effective values of the HCR_EL2, \( \{\text{FMO, IMO, AMO}\} \) fields are 1. |
| &bull; | HCR_EL2.E2H is 1, the Effective values of the HCR_EL2, \( \{\text{FMO, IMO, AMO}\} \) fields are 0. |

For further information on the behavior of this bit when E2H is 1, see 'Behavior of HCR_EL2.E2H'.

HCR_EL2.TGE must not be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TVM, bit [26]

Trap Virtual Memory controls. Traps EL1 writes to the virtual memory control registers to EL2, when EL2 is enabled in the current Security state, as follows:

| &bull; | If EL1 is using AArch64 state, the following registers are trapped to EL2 and reported using EC syndrome value 0x18: |
| &bull; | &middot; SCTLR_EL1, TTBR0_EL1, TTBR1_EL1, TCR_EL1, ESR_EL1, FAR_EL1, AFSR0_EL1, AFSR1_EL1, MAIR_EL1, AMAIR_EL1, CONTEXTIDR_EL1. |
| &bull; | If EL1 is using AArch32 state, accesses using MCR to the following registers are trapped to EL2 and reported using EC syndrome value 0x03, accesses using MCRR are trapped to EL2 and reported using EC syndrome value 0x04: |
| &bull; | &middot; SCTLR, TTBR0, TTBR1, TTBCR, TTBCR2, DACR, DFSR, IFSR, DFAR, IFAR, ADFSR, AIFSR, PRRR, NMRR, MAIR0, MAIR1, AMAIR0, AMAIR1, CONTEXTIDR. |
TVM

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 write accesses to the specified EL1 virtual memory control registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When **HCR_EL2.TGE** is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TTLB, bit [25]**

Trap TLB maintenance instructions. Traps EL1 execution of TLB maintenance instructions to EL2, when EL2 is enabled in the current Security state, as follows:

- When EL1 is using AArch64 state, the following instructions are trapped to EL2 and reported using EC syndrome value 0x18:
  - TLBI VMALLE1, TLBI VAE1, TLBI ASIDE1, TLBI VAAE1, TLBI VALE1, TLBI VAALE1.
  - TLBI VMALLE1IS, TLBI VAE1IS, TLBI ASIDE1IS, TLBI VAAE1IS, TLBI VALE1IS, TLBI VAALE1IS.
  - If FEAT TLB IOS is implemented, this trap applies to TLBI VMMALLE1OS, TLBI VAE1OS, TLBI ASIDE1OS, TLBI VAAE1OS, TLBI VALE1OS, TLBI VAALE1OS.
  - If FEAT TLBIRANGE is implemented, this trap applies to TLBI RVAE1, TLBI RVAAE1, TLBI RVALE1, TLBI RVAALE1, TLBI RVAE1IS, TLBI RVAAE1IS, TLBI RVALE1IS, TLBI RVAALE1IS.
  - If FEAT TLB IOS and FEAT TLBIRANGE are implemented, this trap applies to TLBI RVAE1OS, TLBI RVAAE1OS, TLBI RVALE1OS, TLBI RVAALE1OS.

- When EL1 is using AArch32 state, the following instructions are trapped to EL2 and reported using EC syndrome value 0x03:
  - TLBIMVAI, TLBIMVAA, TLBIMVAIS, TLBIMVAIS, TLBIMVAAL, TLBIMVAAL.
  - TLBIMVA, TLBIMVAA, TLBIMVAIS, TLBIMVAAL.
  - DTBIMVA, DTBIMVAA, DTBIMVAIS, DTBIMVAAL.

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 execution of the specified TLB maintenance instructions are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When **HCR_EL2.TGE** is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

**Note**

The TLB maintenance instructions are **UNDEFINED** at EL0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TPU, bit [24]**

Trap cache maintenance instructions that operate to the Point of Unification. Traps execution of those cache maintenance instructions to EL2, when EL2 is enabled in the current Security state as follows:

- If EL0 is using AArch64 state and the value of **SCTLR_EL1.UCI** is not 0, the following instructions are trapped to EL2 and reported with EC syndrome value 0x18:
  - IC IVAU, DC CVAU. If the value of **SCTLR_EL1.UCI** is 0 these instructions are **UNDEFINED** at EL0 and any resulting exception is higher priority than this trap to EL2.
- If EL1 is using AArch64 state, the following instructions are trapped to EL2 and reported with EC syndrome value 0x18:
  - IC IVAU, IC IALLU, IC IALLUIS, DC CVAU.
- If EL1 is using AArch32 state, the following instructions are trapped to EL2 and reported with EC syndrome value 0x18:
  - ICIMVVAU, IC IALLU, IC IALLUIS, DCCMVAU.

**Note**
An exception generated because an instruction is **undefined** at EL0 is higher priority than this trap to EL2. In addition:

- **IC IALLUIS** and **IC IALLU** are always **undefined** at EL0 using AArch64.
- **ICIMVAU, ICIALLU, ICIALLUIS**, and **DCDMVAU** are always **undefined** at EL0 using AArch32.

<table>
<thead>
<tr>
<th>TPU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions is trapped to EL2, when</td>
</tr>
<tr>
<td></td>
<td>EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of data cache, it is **implementation defined** whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is **implementation defined** whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.

When FEAT_VHE is implemented, and the value of **HCR_EL2.\{E2H, TGE\}** is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **unknown** value.

**TPCP, bit [23]**

**When FEAT_DPB is implemented:**

Trap data or unified cache maintenance instructions that operate to the Point of Coherency or Persistence. Traps execution of those cache maintenance instructions to EL2, when EL2 is enabled in the current Security state as follows:

- If EL0 is using AArch64 state and the value of **SCTLR_EL1.UCI** is not 0, the following instructions are trapped to EL2 and reported using EC syndrome value 0x18:
  - **DC CIVAC, DC CVAC, DC CVAP**. If the value of **SCTLR_EL1.UCI** is 0 these instructions are **undefined** at EL0 and any resulting exception is higher priority than this trap to EL2.
- If EL1 is using AArch64 state, the following instructions are trapped to EL2 and reported using EC syndrome value 0x18:
  - **DC IVAC, DC CIVAC, DC CVAC, DC CVAP**.
- If EL1 is using AArch32 state, the following instructions are trapped to EL2 and reported using EC syndrome value 0x03:
  - **DCIMVAC, DCCIMVAC, DCCMVAC**.

If FEAT_DPB2 is implemented, this trap also applies to **DC CVADP**.

If FEAT_MTE2 is implemented, this trap also applies to **DC CIGVAC, DC CIGDVAC, DC IGVAC, DC IGDVAC, DC CGVAC, DC CGDVAC, DC CGVAP**, and **DC CGDVAP**.

If FEAT_DPB2 and FEAT_MTE2 are implemented, this trap also applies to **DC CGVADP** and **DC CGDVADP**.

**Note**

- An exception generated because an instruction is **undefined** at EL0 is higher priority than this trap to EL2. In addition:
  - AArch64 instructions which invalidate by VA to the Point of Coherency are always **undefined** at EL0 using AArch64.
  - **DCIMVAC, DCCIMVAC**, and **DCCMVAC** are always **undefined** at EL0 using AArch32.
- In Armv8.0 and Armv8.1, this field is named TPC. From Armv8.2 it is named TPCP.

<table>
<thead>
<tr>
<th>TPCP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions is trapped to EL2, when</td>
</tr>
<tr>
<td></td>
<td>EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

If the Point of Coherency is before any level of data cache, it is **implementation defined** whether the execution of any data or unified cache clean, invalidate, or clean and invalidate instruction that operates by VA to the point of coherency can be trapped when the value of this control is 1.
If \( \text{HCR}_{EL2}.\{\text{E2H}, \text{TGE}\} \) is set to \( \{1, 1\} \), this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Trap data or unified cache maintenance instructions that operate to the Point of Coherency. Traps execution of those cache maintenance instructions to \( EL2 \), when \( EL2 \) is enabled in the current Security state as follows:

- If \( EL0 \) is using AArch64 state and the value of \( \text{SCTLR}_{EL1}.\text{UCI} \) is not 0, accesses to the following registers are trapped and reported using EC syndrome value \( 0x18 \):
  - \( \text{DC_CIVAC}, \text{DC_CVAC} \). However, if the value of \( \text{SCTLR}_{EL1}.\text{UCI} \) is 0 these instructions are **UNDEFINED** at \( EL0 \) and any resulting exception is higher priority than this trap to \( EL2 \).
- If \( EL1 \) is using AArch64 state, accesses to \( \text{DC_IVAC}, \text{DC_CIVAC}, \text{DC_CVAC} \) are trapped and reported using EC syndrome value \( 0x18 \).
- When \( EL1 \) is using AArch32, accesses to \( \text{DCIMVAC}, \text{DCCIMVAC}, \text{and DCCMVAC} \) are trapped and reported using EC syndrome value \( 0x03 \).

**Note**

- An exception generated because an instruction is **UNDEFINED** at \( EL0 \) is higher priority than this trap to \( EL2 \). In addition:
  - AArch64 instructions which invalidate by VA to the Point of Coherency are always **UNDEFINED** at \( EL0 \) using AArch64.
  - \( \text{DCIMVAC}, \text{DCCIMVAC}, \text{and DCCMVAC} \) are always **UNDEFINED** at \( EL0 \) using AArch32.
- In Armv8.0 and Armv8.1, this field is named TPC. From Armv8.2 it is named TPCP.

<table>
<thead>
<tr>
<th>TPC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions is trapped to ( EL2 ), when ( EL2 ) is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

If the Point of Coherency is before any level of data cache, it is **IMPLEMENTATION DEFINED** whether the execution of any data or unified cache clean, invalidate, or clean and invalidate instruction that operates by VA to the point of coherency can be trapped when the value of this control is 1.

When \( \text{FEAT_VHE} \) is implemented, and the value of \( \text{HCR}_{EL2}.\{\text{E2H}, \text{TGE}\} \) is \( \{1, 1\} \), this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TSW, bit [22]**

Trap data or unified cache maintenance instructions that operate by Set/Way. Traps execution of those cache maintenance instructions at \( EL1 \) to \( EL2 \), when \( EL2 \) is enabled in the current Security state as follows:

- If \( EL1 \) is using AArch64 state, accesses to \( \text{DC_ISW}, \text{DC_CSW}, \text{DC_CISW} \) are trapped to \( EL2 \), reported using EC syndrome value \( 0x18 \).
- If \( EL1 \) is using AArch32 state, accesses to \( \text{DCISW}, \text{DCCSW}, \text{DCCISW} \) are trapped to \( EL2 \), reported using EC syndrome value \( 0x03 \).

If \( \text{FEAT_MTE2} \) is implemented, this trap also applies to \( \text{DC IGSW}, \text{DC IGDSW}, \text{DC CGSW}, \text{DC CGDW}, \text{DC CIGSW}, \) and \( \text{DC CIGDSW} \).

**Note**

An exception generated because an instruction is **UNDEFINED** at \( EL0 \) is higher priority than this trap to \( EL2 \), and these instructions are always **UNDEFINED** at \( EL0 \).

<table>
<thead>
<tr>
<th>TSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of the specified instructions is trapped to ( EL2 ), when ( EL2 ) is enabled in the current Security state.</td>
</tr>
</tbody>
</table>
When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TACR, bit [21]**

Trap Auxiliary Control Registers. Traps EL1 accesses to the Auxiliary Control Registers to EL2, when EL2 is enabled in the current Security state, as follows:

- If EL1 is using AArch64 state, accesses to ACTLR_EL1 to EL2, are trapped to EL2 and reported using EC syndrome value 0x18.
- If EL1 is using AArch32 state, accesses to ACTLR and, if implemented, ACTLR2 are trapped to EL2 and reported using EC syndrome value 0x03.

<table>
<thead>
<tr>
<th>TACR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to the specified registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

**Note**

ACTLR_EL1 is not accessible at EL0

ACTLR, and ACTLR2 are not accessible at EL0.

The Auxiliary Control Registers are IMPLEMENTATION DEFINED registers that might implement global control bits for the PE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TIDCP, bit [20]**

Trap IMPLEMENTATION DEFINED functionality. Traps EL1 accesses to the encodings reserved for IMPLEMENTATION DEFINED functionality to EL2, when EL2 is enabled in the current Security state as follows:

- In AArch64 state, access to any of the encodings in the following reserved encoding spaces are trapped and reported using EC syndrome 0x18:
  - IMPLEMENTATION DEFINED System instructions, which are accessed using SYS and SYSL, with CRn == {11, 15}.
  - IMPLEMENTATION DEFINED System registers, which are accessed using MRS and MSR with the S3_<op1>_<Cn>_<Cm>_<op2> register name.
- In AArch32 state, MCR and MRC access to instructions with the following encodings are trapped and reported using EC syndrome 0x03:
  - All coproc==p15, CRn==c9, opc1 == {0-7}, CRm == {c0-c2, c5-c8}, opc2 == {0-7},
  - All coproc==p15, CRn==c10, opc1 =={0-7}, CRm == {c0, c1, c4, c8}, opc2 == {0-7},
  - All coproc==p15, CRn==c11, opc1=={0-7}, CRm == {c0-c8, c13}, opc2 == {0-7}.

When the value of HCR_EL2.TIDCP is 1, it is IMPLEMENTATION DEFINED whether any of this functionality accessed from EL0 is trapped to EL2. If it is not, then it is UNDEFINED, and any attempt to access it from EL0 generates an exception that is taken to EL1.

<table>
<thead>
<tr>
<th>TIDCP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to or execution of the specified encodings reserved for IMPLEMENTATION DEFINED functionality are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

An implementation can also include IMPLEMENTATION DEFINED registers that provide additional controls, to give finer-grained control of the trapping of IMPLEMENTATION DEFINED features.

**Note**

Arm expects the trapping of EL0 accesses to these functions to EL2 to be unusual, and used only when the hypervisor is virtualizing EL0 operation. Arm
strongly recommends that unless the hypervisor must virtualize EL0 operation, an EL0 access to any of these functions is UNDEFINED, as it would be if the implementation did not include EL2. The PE then takes any resulting exception to EL1.

The trapping of accesses to these registers from EL1 is higher priority than an exception resulting from the register access being UNDEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TSC, bit [19]**

Trap SMC instructions. Traps EL1 execution of SMC instructions to EL2, when EL2 is enabled in the current Security state.

If execution is in AArch64 state, the trap is reported using EC syndrome value 0x17.

If execution is in AArch32 state, the trap is reported using EC syndrome value 0x13.

**Note**

HCR_EL2.TSC traps execution of the SMC instruction. It is not a routing control for the SMC exception. Trap exceptions and SMC exceptions have different preferred return addresses.

<table>
<thead>
<tr>
<th>TSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL3 is implemented, then any attempt to execute an SMC instruction at EL1 is trapped to EL2, when EL2 is enabled in the current Security state, regardless of the value of SCR_EL3.SMD. If EL3 is not implemented, FEAT_NV is implemented, and HCR_EL2.NV is 1, then any attempt to execute an SMC instruction at EL1 using AArch64 is trapped to EL2, when EL2 is enabled in the current Security state. If EL3 is not implemented, and either FEAT_NV is not implemented or HCR_EL2.NV is 0, then it is IMPLEMENTATION DEFINED whether:</td>
</tr>
<tr>
<td></td>
<td>• Any attempt to execute an SMC instruction at EL1 is trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
<tr>
<td></td>
<td>• Any attempt to execute an SMC instruction is UNDEFINED.</td>
</tr>
</tbody>
</table>

In AArch32 state, the Armv8-A architecture permits, but does not require, this trap to apply to conditional SMC instructions that fail their condition code check, in the same way as with traps on other conditional instructions.

SMC instructions are UNDEFINED at EL0.

If EL3 is not implemented and HCR_EL2.NV is 0, it is IMPLEMENTATION DEFINED whether this bit is:

- RES0.
- Implemented with the functionality as described in HCR_EL2.TSC.

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TID3, bit [18]**

Trap ID group 3. Traps EL1 reads of group 3 ID registers to EL2, when EL2 is enabled in the current Security state, as follows:

In AArch64 state:

- Reads of the following registers are trapped to EL2, reported using EC syndrome value 0x18:
  - ID_PFR0_EL1, ID_PFR1_EL1, ID_PFR2_EL1, ID_DFR0_EL1, ID_AFR0_EL1, ID_MMFR0_EL1, ID_MMFR1_EL1, ID_MMFR2_EL1, ID_MMFR3_EL1, ID_ISAR0_EL1, ID_ISAR1_EL1.
HCR_EL2, Hypervisor Configuration Register

ID_ISAR2_EL1, ID_ISAR3_EL1, ID_ISAR4_EL1, ID_ISAR5_EL1, MVFR0_EL1, MVFR1_EL1, MVFR2_EL1.

- ID_AA64PFR0_EL1, ID_AA64PFR1_EL1, ID_AA64DFR0_EL1, ID_AA64DFR1_EL1, ID_AA64ISAR0_EL1, ID_AA64ISAR1_EL1, ID_AA64MMFR0_EL1, ID_AA64MMFR1_EL1, ID_AA64AFR0_EL1, ID_AA64AFR1_EL1.

- If FEAT_FGT is implemented:
  - ID_MMFR4_EL1 and ID_MMFR5_EL1 are trapped to EL2.
  - ID_AA64MMFR2_EL1 and ID_ISAR6_EL1 are trapped to EL2.
  - ID_DFR1_EL1 is trapped to EL2.
  - ID_AA64ZFR0_EL1 is trapped to EL2.
  - ID_AA64ISAR2_EL1 is trapped to EL2.
  - This field traps all MRS accesses to registers in the following range that are not already mentioned in this field description: Op0 == 3, op1 == 0, CRn == c0, CRm == {c1-c7}, op2 == {0-7}.

- If FEAT_FGT is not implemented:
  - ID_MMFR4_EL1 and ID_MMFR5_EL1 are trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_MMFR4_EL1 or ID_MMFR5_EL1 are trapped to EL2.
  - ID_AA64MMFR2_EL1 and ID_ISAR6_EL1 are trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_AA64MMFR2_EL1 or ID_ISAR6_EL1 are trapped to EL2.
  - ID_DFR1_EL1 is trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_DFR1_EL1 are trapped to EL2.
  - ID_AA64ZFR0_EL1 is trapped to EL2, unless implemented as RAZ then it is IMPLEMENTATION DEFINED whether accesses to ID_AA64ZFR0_EL1 are trapped to EL2.
  - ID_AA64ISAR2_EL1 is trapped to EL2, unless implemented as RAZ then it is IMPLEMENTATION DEFINED whether accesses to ID_AA64ISAR2_EL1 are trapped to EL2.
  - Otherwise, it is IMPLEMENTATION DEFINED whether this bit traps MRS accesses to registers in the following range that are not already mentioned in this field description: Op0 == 3, op1 == 0, CRn == c0, CRm == {c1-c7}, op2 == {0-7}.

In AArch32 state:

- VMRS access to MVFR0, MVFR1, and MVFR2, are trapped to EL2, reported using EC syndrome value 0x08, unless access is also trapped by HCPTR which takes priority.

- MRC access to the following registers are trapped to EL2, reported using EC syndrome value 0x03:
  - ID_PFR0, ID_PFR1, ID_PFR2, ID_DFR0, ID_AFR0, ID_MMFR0, ID_MMFR1, ID_MMFR2, ID_MMFR3, ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, ID_ISAR4, ID_ISAR5.

- If FEAT_FGT is implemented:
  - ID_MMFR4 and ID_MMFR5 are trapped to EL2.
  - ID_ISAR6 is trapped to EL2.
  - ID_DFR1 is trapped to EL2.
  - This field traps all MRC accesses to encodings in the following range that are not already mentioned in this field description: coproc == p15, opc1 == 0, CRn == c0, CRm == {c2-c7}, opc2 == {0-7}.

- If FEAT_FGT is not implemented:
  - ID_MMFR4 and ID_MMFR5 are trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_MMFR4 or ID_MMFR5 are trapped.
ID_ISR6 is trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_ISR6 are trapped to EL2.

ID_DFR1 is trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_DFR1 are trapped to EL2.

Otherwise, it is IMPLEMENTATION DEFINED whether this bit traps all MRC accesses to registers in the following range not already mentioned in this field description with coproc == p15, opc1 == 0, CRn == c0, CRm == {c2-c7}, opc2 == {0-7}.

TID3

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 read accesses to ID group 3 registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TID2, bit [17]

Trap ID group 2. Traps the following register accesses to EL2, when EL2 is enabled in the current Security state, as follows:

- If EL1 is using AArch64, reads of CTR_EL0, CCSIDR_EL1, CCSIDR2_EL1, CLIDR_EL1, and CSSELR_EL1 are trapped to EL2, reported using EC syndrome value 0x18.
- If EL0 is using AArch64 and the value of SCTLR_EL1.UCT is not 0, reads of CTR_EL0 are trapped to EL2, reported using EC syndrome value 0x18. If the value of SCTLR_EL1.UCT is 0 then EL0 reads of CTR_EL0 are UNDEFINED and any resulting exception takes precedence over this trap.
- If EL1 is using AArch64, writes to CSSELR_EL1 are trapped to EL2, reported using EC syndrome value 0x18.
- If EL1 is using AArch32, reads of CTR, CCSIDR, CCSIDR2, CLIDR, and CSSELR are trapped to EL2, reported using EC syndrome value 0x03.
- If EL1 is using AArch32, writes to CSSELR are trapped to EL2, reported using EC syndrome value 0x03.

TID2

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 and EL0 accesses to ID group 2 registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TID1, bit [16]

Trap ID group 1. Traps EL1 reads of the following registers to EL2, when EL2 is enabled in the current Security state as follows:

- In AArch64 state, accesses of REVIDR_EL1, AIDR_EL1, reported using EC syndrome value 0x18.
- In AArch32 state, accesses of TCMTR, TLBTR, REVIDR, AIDR, reported using EC syndrome value 0x03.

TID1

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 read accesses to ID group 1 registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**TID0, bit [15]**

When AArch32 is supported at any Exception level:

Trap ID group 0. Traps the following register accesses to EL2:

- EL1 reads of the JIDR, reported using EC syndrome value 0x05.
- If the JIDR is RAZ from EL0, EL0 reads of the JIDR, reported using EC syndrome value 0x05.
- EL1 accesses using VMRS of the FPSID, reported using EC syndrome value 0x08.

**Note**

- It is IMPLEMENTATION DEFINED whether the JIDR is RAZ or UNDEFINED at EL0. If it is UNDEFINED at EL0 then any resulting exception takes precedence over this trap.
- The FPSID is not accessible at EL0 using AArch32.
- Writes to the FPSID are ignored, and not trapped by this control.

<table>
<thead>
<tr>
<th>TID0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified EL1 read accesses to ID group 0 registers are trapped to EL2, when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**TWE, bit [14]**

Traps EL0 and EL1 execution of WFE instructions to EL2, when EL2 is enabled in the current Security state, from both Execution states, reported using EC syndrome value 0x01.

When FEAT_WFxT is implemented, this trap also applies to the WFET instruction.

<table>
<thead>
<tr>
<th>TWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFE instruction at EL0 or EL1 is trapped to EL2, when EL2 is enabled in the current Security state, the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by SCTLR.nTWE or SCTLR.EL1.nTWE.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFE instruction is trapped only if the instruction passes its condition code check.

**Note**

Since a WFE can complete at any time, even without a Wakeup event, the traps on WFE are not guaranteed to be taken, even if the WFE is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

For more information about when WFE instructions can cause the PE to enter a low-power state, see 'Wait for Event mechanism and Send event'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**TWI, bit [13]**

Traps EL0 and EL1 execution of WFI instructions to EL2, when EL2 is enabled in the current Security state, from both Execution states, reported using EC syndrome value 0x01.

When FEAT_WFxT is implemented, this trap also applies to the WFIT instruction.

<table>
<thead>
<tr>
<th>TWI Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1 Any attempt to execute a WFI instruction at EL0 or EL1 is trapped to EL2, when EL2 is enabled in the current Security state, if the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by SCTLR.nTWI or SCTLR_EL1.nTWI.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFI instruction is trapped only if the instruction passes its condition code check.

**Note**

Since a WFI can complete at any time, even without a Wakeup event, the traps on WFI are not guaranteed to be taken, even if the WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

For more information about when WFI instructions can cause the PE to enter a low-power state, see 'Wait for Interrupt'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DC, bit [12]**

Default Cacheability.

<table>
<thead>
<tr>
<th>DC Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 This control has no effect on the EL1&amp;0 translation regime.</td>
</tr>
<tr>
<td>0b1 In both Security states:</td>
</tr>
<tr>
<td>• When EL1 is using AArch64, the PE behaves as if the value of the SCTLR_EL1.M field is 0 for all purposes other than returning the value of a direct read of SCTLR_EL1.</td>
</tr>
<tr>
<td>• When EL1 is using AArch32, the PE behaves as if the value of the SCTLR.M field is 0 for all purposes other than returning the value of a direct read of SCTLR.</td>
</tr>
<tr>
<td>• The PE behaves as if the value of the HCR_EL2.VM field is 1 for all purposes other than returning the value of a direct read of HCR_EL2.</td>
</tr>
<tr>
<td>• The memory type produced by stage 1 of the EL1&amp;0 translation regime is Normal Non-Shareable, Inner Write-Back Read-Allocate Write-Allocate, Outer Write-Back Read-Allocate Write-Allocate.</td>
</tr>
</tbody>
</table>

This field has no effect on the EL2, EL2&0, and EL3 translation regimes.

This field is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**BSU, bits [11:10]**

Barrier Shareability upgrade. This field determines the minimum shareability domain that is applied to any barrier instruction executed from EL1 or EL0:

<table>
<thead>
<tr>
<th>BSU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No effect.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Full system.</td>
</tr>
</tbody>
</table>

This value is combined with the specified level of the barrier held in its instruction, using the same principles as combining the shareability attributes from two stages of address translation.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is {1, 1}, this field behaves as 0b00 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**FB, bit [9]**

Force broadcast. Causes the following instructions to be broadcast within the Inner Shareable domain when executed from EL1:

AArch32: BPIALL, TLBIALL, TLBIMVA, TLBIASID, DTLBIALL, DTLBIMVA, DTLBIASID, ITLBIA, ITLBIMVA, ITLBIMVAS, TLBIMVE, TLBIMVAA.

AArch64: TLBIVVALL, TLBIVVAE1, TLBIVVAE1, TLBIVVAE1, TLBIVVAE1, TLBIVVAAE, TLBIVVAAE, TLBIVVAAE, TLBIVVAAE, TLBIVVAAE, TLBIVVAAE.

<table>
<thead>
<tr>
<th>FB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This field has no effect on the operation of the specified instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>When one of the specified instruction is executed at EL1, the instruction is broadcast within the Inner Shareable shareability domain.</td>
</tr>
</tbody>
</table>

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VSE, bit [8]**

Virtual SError interrupt.

<table>
<thead>
<tr>
<th>VSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This mechanism is not making a virtual SError interrupt pending.</td>
</tr>
<tr>
<td>0b1</td>
<td>A virtual SError interrupt is pending because of this mechanism.</td>
</tr>
</tbody>
</table>

The virtual SError interrupt is enabled only when the value of HCR_EL2.(TGE, AMO) is {0, 1}.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VI, bit [7]**

Virtual IRQ Interrupt.

<table>
<thead>
<tr>
<th>VI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This mechanism is not making a virtual IRQ pending.</td>
</tr>
<tr>
<td>0b1</td>
<td>A virtual IRQ is pending because of this mechanism.</td>
</tr>
</tbody>
</table>

The virtual IRQ is enabled only when the value of HCR_EL2.(TGE, IMO) is {0, 1}.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
VF, bit [6]

Virtual FIQ Interrupt.

<table>
<thead>
<tr>
<th><strong>VF</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This mechanism is not making a virtual FIQ pending.</td>
</tr>
<tr>
<td>0b1</td>
<td>A virtual FIQ is pending because of this mechanism.</td>
</tr>
</tbody>
</table>

The virtual FIQ is enabled only when the value of HCR_EL2.{TGE, FMO} is \{0, 1\}.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

AMO, bit [5]

Physical SError interrupt routing.

<table>
<thead>
<tr>
<th><strong>AMO</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When executing at Exception levels below EL2, and EL2 is in EL1:</td>
</tr>
<tr>
<td></td>
<td>• Physical SError interrupts are not taken to EL2.</td>
</tr>
<tr>
<td></td>
<td>• When the value of HCR_EL2.TGE is 0, if the PE is executing at EL2</td>
</tr>
<tr>
<td></td>
<td>using AArch64, physical SError interrupts are not taken unless they</td>
</tr>
<tr>
<td></td>
<td>are routed to EL3 by the SCR_EL3.EA bit.</td>
</tr>
<tr>
<td></td>
<td>• Virtual SError interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>When executing at any Exception level, and EL2 is enabled in the</td>
</tr>
<tr>
<td></td>
<td>current Security state:</td>
</tr>
<tr>
<td></td>
<td>• Physical SError interrupts are taken to EL2, unless they are</td>
</tr>
<tr>
<td></td>
<td>routed to EL3.</td>
</tr>
<tr>
<td></td>
<td>• When the value of HCR_EL2.TGE is 0, then virtual SError interrupts</td>
</tr>
<tr>
<td></td>
<td>are enabled.</td>
</tr>
</tbody>
</table>

If EL2 is enabled in the current Security state and the value of HCR_EL2.TGE is 1:

- Regardless of the value of the AMO bit physical asynchronous External aborts and SError interrupts target EL2 unless they are routed to EL3.
- When FEAT VHE is not implemented, or if HCR_EL2.E2H is 0, this field behaves as 1 for all purposes other than a direct read of the value of this bit.
- When FEAT VHE is implemented and HCR_EL2.E2H is 1, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

IMO, bit [4]

Physical IRQ Routing.

<table>
<thead>
<tr>
<th><strong>IMO</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When executing at Exception levels below EL2, and EL2 is in EL1:</td>
</tr>
<tr>
<td></td>
<td>• Physical IRQ interrupts are not taken to EL2.</td>
</tr>
<tr>
<td></td>
<td>• When the value of HCR_EL2.TGE is 0, if the PE is executing at EL2</td>
</tr>
<tr>
<td></td>
<td>using AArch64, physical IRQ interrupts are not taken unless they are</td>
</tr>
<tr>
<td></td>
<td>routed to EL3 by the SCR_EL3.IRQ bit.</td>
</tr>
<tr>
<td></td>
<td>• Virtual IRQ interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>When executing at any Exception level, and EL2 is enabled in the</td>
</tr>
<tr>
<td></td>
<td>current Security state:</td>
</tr>
<tr>
<td></td>
<td>• Physical IRQ interrupts are taken to EL2, unless they are routed to</td>
</tr>
<tr>
<td></td>
<td>EL3.</td>
</tr>
<tr>
<td></td>
<td>• When the value of HCR_EL2.TGE is 0, then Virtual IRQ interrupts</td>
</tr>
<tr>
<td></td>
<td>are enabled.</td>
</tr>
</tbody>
</table>

If EL2 is enabled in the current Security state, and the value of HCR_EL2.TGE is 1:

- Regardless of the value of the IMO bit, physical IRQ Interrupts target EL2 unless they are routed to EL3.
- When FEAT VHE is not implemented, or if HCR_EL2.E2H is 0, this field behaves as 1 for all purposes other than a direct read of the value of this bit.
• When FEAT_VHE is implemented and HCR_EL2.E2H is 1, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**FMO, bit [3]**

Physical FIQ Routing.

<table>
<thead>
<tr>
<th>FMO</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0 | When executing at Exception levels below EL2, and EL2 is enabled in the current Security state:  
• Physical FIQ interrupts are not taken to EL2.  
• When the value of HCR_EL2.TGE is 0, if the PE is executing at EL2 using AArch64, physical FIQ interrupts are not taken unless they are routed to EL3 by the SCR_EL3.FIQ bit.  
• Virtual FIQ interrupts are disabled.  
| 0b1 | When executing at any Exception level, and EL2 is enabled in the current Security state:  
• Physical FIQ interrupts are taken to EL2, unless they are routed to EL3.  
• When HCR_EL2.TGE is 0, then Virtual FIQ interrupts are enabled. |

If EL2 is enabled in the current Security state and the value of HCR_EL2.TGE is 1:

• Regardless of the value of the FMO bit, physical FIQ Interrupts target EL2 unless they are routed to EL3.  
• When FEAT_VHE is not implemented, or if HCR_EL2.E2H is 0, this field behaves as 1 for all purposes other than a direct read of the value of this bit.  
• When FEAT_VHE is implemented and HCR_EL2.E2H is 1, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PTW, bit [2]**

Protected Table Walk. In the EL1&0 translation regime, a translation table access made as part of a stage 1 translation table walk is subject to a stage 2 translation. The combining of the memory type attributes from the two stages of translation means the access might be made to a type of Device memory. If this occurs, then the value of this bit determines the behavior:

<table>
<thead>
<tr>
<th>PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table walk occurs as if it is to Normal Non-cacheable memory. This means it can be made speculatively.</td>
</tr>
<tr>
<td>0b1</td>
<td>The memory access generates a stage 2 Permission fault.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

When HCR_EL2.TGE is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SWIO, bit [1]**

Set/Way Invalidation Override. Causes EL1 execution of the data cache invalidate by set/way instructions to perform a data cache clean and invalidate by set/way:

<table>
<thead>
<tr>
<th>SWIO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the operation of data cache invalidate by set/way instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Data cache invalidate by set/way instructions perform a data cache clean and invalidate by set/way.</td>
</tr>
</tbody>
</table>
When the value of this bit is 1:

AArch32: **DCISW** performs the same invalidation as a **DCCISW** instruction.

AArch64: **DC ISW** performs the same invalidation as a **DC CISW** instruction.

This bit can be implemented as **RES1**.

When **HCR_EL2.TGE** is 1, the PE ignores the value of this field for all purposes other than a direct read of this field.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**VM, bit [0]**

Virtualization enable. Enables stage 2 address translation for the EL1&0 translation regime, when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>VM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1&amp;0 stage 2 address translation disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1&amp;0 stage 2 address translation enabled.</td>
</tr>
</tbody>
</table>

When the value of this bit is 1, data cache invalidate instructions executed at EL1 perform a data cache clean and invalidate. For the invalidate by set/way instruction this behavior applies regardless of the value of the **HCR_EL2.SWIO** bit.

This bit is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of **HCR_EL2.{E2H, TGE}** is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the HCR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, HCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x078];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HCR_EL2;
elsif PSTATE.EL == EL3 then
  return HCR_EL2;

MSR HCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x078] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HCR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  HCR_EL2 = X[t];
HCRX_EL2, Extended Hypervisor Configuration Register

The HCRX_EL2 characteristics are:

**Purpose**

Provides configuration controls for virtualization, including defining whether various operations are trapped to EL2.

**Configuration**

This register is present only when FEAT_HCX is implemented. Otherwise, direct accesses to HCRX_EL2 are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

The bits in this register behave as if they are 0 for all purposes other than direct reads of the register if:

- EL2 is not enabled in the current Security state.
- SCR_EL3.HXEn is 0.

**Attributes**

HCRX_EL2 is a 64-bit register.

**Field descriptions**

The HCRX_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | FGTnXS | FnXS | EnASR | EnALS | EnAS0 |

**Bits [63:5]**

Reserved, RES0.

**FGTnXS, bit [4]**

**When FEAT_XS is implemented:**

Determines if the fine-grained traps in HFGITR_EL2 that apply to each of the TLBI maintenance instructions that are accessible at EL1 also apply to the corresponding TLBI maintenance instructions with the nXS qualifier.

<table>
<thead>
<tr>
<th>FGTnXS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fine-grained trap in the HFGITR_EL2 that applies to a TLBI maintenance instruction at EL1 also applies to the corresponding TLBI instruction with the nXS qualifier at EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fine-grained trap in the HFGITR_EL2 that applies to a TLBI maintenance instruction at EL1 does not apply to the corresponding TLBI instruction with the nXS qualifier at EL1.</td>
</tr>
</tbody>
</table>

**Otherwise:**

Reserved, RES0.
**FnXS, bit [3]**

*When FEAT_XS is implemented:*

Determines the behavior of TLBI instructions affected by the XS attribute.

This control bit also determines whether an AArch64 DSB instruction behaves as a DSB instruction with an nXS qualifier when executed at EL0 and EL1.

<table>
<thead>
<tr>
<th>FnXS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not have any effect on the behavior of the TLBI maintenance instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLBI maintenance instruction without the nXS qualifier executed at EL1 behaves in the same way as the corresponding TLBI maintenance instruction with the nXS qualifier. An AArch64 DSB instruction executed at EL1 or EL0 behaves in the same way as the corresponding DSB instruction with the nXS qualifier executed at EL1 or EL0.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

*Otherwise:*

Reserved, RES0.

**EnASR, bit [2]**

*When FEAT_LS64 is implemented:*

When \( \text{HCR\_EL2.\{E2H, TGE\} \neq \{1, 1\} } \), traps execution of an ST64BV instruction at EL0 or EL1 to EL2.

<table>
<thead>
<tr>
<th>EnASR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV instruction at EL0 is trapped to EL2 if the execution is not trapped by SCTL_EL1.EnASR. Execution of an ST64BV instruction at EL1 is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV instruction is reported using an ESR\_ELx.EC value of 0x0A, with an ISS code of 0x00000000.

On a Warm reset, when EL3 is not implemented and EL2 is implemented, this field resets to 0.

*Otherwise:*

Reserved, RES0.

**EnALS, bit [1]**

*When FEAT_LS64 is implemented:*

When \( \text{HCR\_EL2.\{E2H, TGE\} \neq \{1, 1\} } \), traps execution of an LD64B or ST64B instruction at EL0 or EL1 to EL2.

<table>
<thead>
<tr>
<th>EnALS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an LD64B or ST64B instruction at EL0 is trapped to EL2 if the execution is not trapped by SCTL_EL1.EnALS. Execution of an LD64B or ST64B instruction at EL1 is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an LD64B or ST64B instruction is reported using an ESR\_ELx.EC value of 0x0A, with an ISS code of 0x00000002.

On a Warm reset, when EL3 is not implemented and EL2 is implemented, this field resets to 0.
Otherwise:
Reserved, RES0.

EnAS0, bit [0]

When FEAT_LS64 is implemented:

When HCR_EL2.{E2H, TGE} != {1, 1}, traps execution of an ST64BV0 instruction at EL0 or EL1 to EL2.

<table>
<thead>
<tr>
<th>EnAS0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV0 instruction at EL0 is trapped to EL2 if the execution is not trapped by SCTLR_EL1.EnAS0. Execution of an ST64BV0 instruction at EL1 is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV0 instruction is reported using an ESR_ELx.EC value of 0x0A, with an ISS code of 0x00000001.

On a Warm reset, when EL3 is not implemented and EL2 is implemented, this field resets to 0.

Otherwise:
Reserved, RES0.

Accessing the HCRX_EL2

Accesses to this register use the following encodings:

MRS <Xt>, HCRX_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0xA0];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.HXEn == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.HXEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return HCRX_EL2;
elsif PSTATE.EL == EL3 then
  return HCRX_EL2;

MSR HCRX_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0xA0] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.HXEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.HXEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        HCRX_EL2 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    HCRX_EL2 = X[t];
The HDFGRTR_EL2 characteristics are:

**Purpose**

Provides controls for traps of MRS and MRC reads of debug, trace, PMU, and Statistical Profiling System registers.

**Configuration**

This register is present only when FEAT_FGT is implemented. Otherwise, direct accesses to HDFGRTR_EL2 are **UNDEFINED**.

**Attributes**

HDFGRTR_EL2 is a 64-bit register.

**Field descriptions**

The HDFGRTR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>61</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>60</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>59</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>58</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>57</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
<tr>
<td>56</td>
<td>nPMSNEVFR_EL1, bit [62]</td>
</tr>
</tbody>
</table>

nPMSNEVFR_EL1, bit [62]

When FEAT_SPEv1p2 is implemented:

- **Trap MRS reads of PMSNEVFR_EL1 at EL1 using AArch64 to EL2.**

<table>
<thead>
<tr>
<th>nPMSNEVFR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If EL2 is implemented and enabled in the current Security state then MRS reads of PMSNEVFR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td>MRS reads of PMSNEVFR_EL1 are not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE and treated as zero when EL3 is implemented and SCR_EL3.FGTEn == 0b0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

- Reserved, RES0.
Bits [61:59]

Reserved, RES0.

PMCEIDn_EL0, bit [58]

When FEAT_PMUv3 is implemented:

Trap MRS reads of PMCEID<n> at EL0 at EL1 and EL0 using AArch64 and MRC reads of PMCEID<n> at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMCEIDn_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMCEID&lt;n&gt; at EL0 at EL1 and EL0 using AArch64 and MRC reads of PMCEID&lt;n&gt; at EL0 using AArch32 are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1         | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:  
• MRS reads of PMCEID<n> at EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.  
• MRC reads of PMCEID<n> at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMUSERENR_EL0, bit [57]

When FEAT_PMUv3 is implemented:

Trap MRS reads of PMUSERENR_EL0 at EL1 and EL0 using AArch64 and MRC reads of PMUSERENR at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMUSERENR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMUSERENR_EL0 at EL1 and EL0 using AArch64 and MRC reads of PMUSERENR at EL0 using AArch32 are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1           | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:  
• MRS reads of PMUSERENR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.  
• MRC reads of PMUSERENR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
Bits [56:49]

Reserved, RES0.

TRCVICTLR, bit [48]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCVICTLR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCVICTLR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCVICTLR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCVICTLR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCSTATR, bit [47]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCSTATR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCSTATR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCSTATR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCSTATR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCSSCSRn, bit [46]

When FEAT_ETMv4 is implemented, TRCSSCSR<n> are implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCSSCSR<n> at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCSSCSRn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCSSCSR&lt;n&gt; are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCSSCSR&lt;n&gt; at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If Single-shot Comparator n is not implemented, a read of TRCSSCSR<n> is UNDEFINED.
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCSEQSTR, bit [45]

When FEAT_ETMv4 is implemented, TRCSEQSTR is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCSEQSTR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCSEQSTR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCSEQSTR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCSEQSTR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCPRGCTRLR, bit [44]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCPRGCTRLR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCPRGCTRLR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCPRGCTRLR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCPRGCTRLR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCOSLSR, bit [43]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCOSLSR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCOSLSR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCOSLSR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCOSLSR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**Bit [42]**

Reserved, RES0.

**TRCIMSPECn, bit [41]**

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCIMSPEC<n> at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCIMSPECn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCIMSPEC&lt;n&gt; are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCIMSPEC&lt;n&gt; at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

TRCIMSPEC<1-7> are optional. If TRCIMSPEC<n> is not implemented, a read of TRCIMSPEC<n> is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TRCID, bit [40]**

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- TRCDEVAARCH.
- TRCDEVVID.
- TRCIDR<n>.

<table>
<thead>
<tr>
<th>TRCID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
Bits [39:38]

Reserved, RES0.

TRCCNTVRn, bit [37]

When FEAT_ETMv4 is implemented, TRCCNTVR<n> are implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCCNTVR<n> at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCCNTVRn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCCNTVR&lt;n&gt; are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of TRCCNTVR&lt;n&gt; at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If Counter n is not implemented, a read of TRCCNTVR<n> is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCCLAIM, bit [36]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- TRCCLAIMCLR
- TRCCLAIMSET

<table>
<thead>
<tr>
<th>TRCCLAIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCAUXCTLR, bit [35]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCAUXCTLR at EL1 using AArch64 to EL2.
TRCAUXCTLR

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCAUXCTLR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and</td>
</tr>
<tr>
<td></td>
<td>either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads</td>
</tr>
<tr>
<td></td>
<td>of TRCAUXCTLR at EL1 using AArch64 are trapped to EL2 and reported with</td>
</tr>
<tr>
<td></td>
<td>EC syndrome value 0x18, unless the read generates a higher priority</td>
</tr>
<tr>
<td></td>
<td>exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

TRCAUTHSTATUS, bit [34]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of TRCAUTHSTATUS at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCAUTHSTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of TRCAUTHSTATUS are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and</td>
</tr>
<tr>
<td></td>
<td>either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads</td>
</tr>
<tr>
<td></td>
<td>of TRCAUTHSTATUS at EL1 using AArch64 are trapped to EL2 and reported with</td>
</tr>
<tr>
<td></td>
<td>EC syndrome value 0x18, unless the read generates a higher priority</td>
</tr>
<tr>
<td></td>
<td>exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

TRC, bit [33]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- TRCACATR<n>
- TRCACVR<n>
- TRCBBCTLR
- TRCCCTLR
- TRCCIDCCTLRO
- TRCCIDCCTLRI
- TRCICIDVR<n>
- TRCCNCTLTR<n>
- TRCCNTRLDVR<n>
- TRCCONFIGR
- TRCEVENTCTL0R
- TRCEVENTCTL1R
- TRCEXITINSELR
- TRCOCTLR
- TRCROSCTR<n>
- TRCSEQEVR<n>
- TRCSEQSTEV R
- TRCSSCCR<n>
- TRCSSPCICR<n>
- TRCSTALLCTLR
• TRCSYNCPR
• TRCTRACEIDR
• TRCTSCCTRL
• TRCVIIECTRL
• TRCVIPCSSCTRL
• TRCVISSCTRL
• TRCVMIDCCTRL0
• TRCVMIDCCTRL1
• TRCVMIDCVR<n>

<table>
<thead>
<tr>
<th>TRC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

A read of an unimplemented register is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSLATFR_EL1, bit [32]

When FEAT_SPE is implemented:

Trap MRS reads of PMSLATFR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSLATFR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSLATFR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSLATFR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSIRR_EL1, bit [31]

When FEAT_SPE is implemented:

Trap MRS reads of PMSIRR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSIRR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSIRR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSIRR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSIDR_EL1, bit [30]**

**When FEAT_SPE is implemented:**

Trap MRS reads of PMSIDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSIDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSIDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSICR_EL1, bit [29]**

**When FEAT_SPE is implemented:**

Trap MRS reads of PMSICR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSICR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSICR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSICR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSFCR_EL1, bit [28]**

**When FEAT_SPE is implemented:**

Trap MRS reads of PMSFCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSFCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSFCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSFCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

PMSEVFR_EL1, bit [27]

When FEAT_SPE is implemented:

Trap MRS reads of PMSEVFR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSEVFR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSEVFR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSEVFR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

PMSCR_EL1, bit [26]

When FEAT_SPE is implemented:

Trap MRS reads of PMSCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMSCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMSCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

PMBSR_EL1, bit [25]

When FEAT_SPE is implemented:

Trap MRS reads of PMBSR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMBSR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMBSR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMBSR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMBPTR_EL1, bit [24]**

When FEAT_SPE is implemented:

Trap MRS reads of **PMBPTR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMBPTR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>PMBPTR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of <strong>PMBPTR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMBLIMITR_EL1, bit [23]**

When FEAT_SPE is implemented:

Trap MRS reads of **PMBLIMITR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMLIMITR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>PMBLIMITR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of <strong>PMBLIMITR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMMIR_EL1, bit [22]**

When FEAT_PMUv3 is implemented:

Trap MRS reads of **PMMIR_EL1** at EL1 using AArch64 to EL2.
**PMMIR_EL1**

| 0b0 | MRS reads of PMMIR_EL1 are not affected by this bit. |
| 0b1 | If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of PMMIR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bits [21:20]**

Reserved, RES0.

**PMSEL_EL0, bit [19]**

When FEAT_PMUv3 is implemented:

Trap MRS reads of PMSEL_EL0 at EL1 and EL0 using AArch64 and MRC reads of PMSEL at EL0 using AArch32 when EL1 is using AArch64 to EL2.

| 0b0 | MRS reads of PMSEL_EL0 at EL1 and EL0 using AArch64 and MRC reads of PMSEL at EL0 using AArch32 are not affected by this bit. |
| 0b1 | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:  
  • MRS reads of PMSEL_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.  
  • MRC reads of PMSEL at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**PMOVS, bit [18]**

When FEAT_PMUv3 is implemented:

Trap MRS reads and MRC reads of multiple System registers.

Enables a trap to EL2 the following operations:

- At EL1 and EL0 using AArch64: MRS reads of PMOVSSLR_EL0 and PMOVSSET_EL0.
- At EL0 using Arch32 when EL1 is using AArch64: MRC reads of PMOVSRS and PMOVSSET.
### PMOVS

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1 | If EL2 is implemented and enabled in the current Security state, \( \text{HCR}_{EL2}.(E2H,TGE) \neq \{1,1\} \), EL1 is using AArch64, and either EL3 is not implemented or \( \text{SCR}_{EL3}.\text{FGTEn} = 0b1 \), then, unless the read generates a higher priority exception:  
  - MRS reads at EL1 and EL0 using AArch64 of \( \text{PMOVSCLR}_{EL0} \) and \( \text{PMOVSET}_{EL0} \) are trapped to EL2 and reported with EC syndrome value 0x18.  
  - MRC reads at EL0 using AArch32 of \( \text{PMOVSR} \) and \( \text{PMOVSET} \) are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### PMINTEN, bit [17]

**When FEAT_PMUv3 is implemented:**

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- \( \text{PMINTENCLR}_{EL1} \)
- \( \text{PMINTENSET}_{EL1} \)

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or ( \text{SCR}_{EL3}.\text{FGTEn} = 0b1 ), then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### PMCNTEN, bit [16]

**When FEAT_PMUv3 is implemented:**

Trap MRS reads and MRC reads of multiple System registers.

Enables a trap to EL2 the following operations:

- At EL1 and EL0 using AArch64: MRS reads of \( \text{PMCNTENCLR}_{EL0} \) and \( \text{PMCNTENSET}_{EL0} \).
- At EL0 using Arch32 when EL1 is using AArch64: MRC reads of \( \text{PMCNTENCLR} \) and \( \text{PMCNTENSET} \).
PMCNTEN

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1 | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:
  - MRS reads at EL1 and EL0 using AArch64 of PMCNTENCLR_EL0 and PMCNTENSET_EL0 are trapped to EL2 and reported with EC syndrome value 0x18.
  - MRC reads at EL0 using AArch32 of PMCNTENCLR and PMCNTENSET are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMCCNTR_EL0, bit [15]

When FEAT_PMUv3 is implemented:

Trap MRS reads of PMCCNTR_EL0 at EL1 and EL0 using AArch64 and MRC and MRRC reads of PMCCNTR at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMCCNTR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of PMCCNTR_EL0 at EL1 and EL0 using AArch64 and MRC and MRRC reads of PMCCNTR at EL0 using AArch32 are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1 | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:
  - MRS reads of PMCCNTR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.
  - MRC and MRRC reads of PMCCNTR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03 (for MRC) or 0x04 (for MRRC). |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMCCFILTR_EL0, bit [14]

When FEAT_PMUv3 is implemented:

Trap MRS reads of PMCCFILTR_EL0 at EL1 and EL0 using AArch64 and MRC reads of PMCCFILTR at EL0 using AArch32 when EL1 is using AArch64 to EL2.
PMCCFILTR_EL0 can also be accessed in AArch64 state using PMXEVTYPER_EL0 when PMSELR_EL0.SEL == 31, and PMCCFILTR can also be accessed in AArch32 state using PMXEVTYPER when PMSELR.SEL == 31.

Setting this bit to 1 has no effect on accesses to PMXEVTYPER_EL0 and PMXEVTYPER, regardless of the value of PMSELR_EL0.SEL or PMSELR.SEL.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

### PMEVTYPEPERn_EL0, bit [13]

When FEAT_PMUv3 is implemented:

Trap MRS reads and MRC reads of multiple System registers.

Enables a trap to EL2 the following operations:

- At EL1 and EL0 using AArch64: MRS reads of PMEVTYPEPER<\text{n}>_EL0 and PMXEVTYPER_EL0.
- At EL0 using Arch32 when EL1 is using AArch64: MRC reads of PMEVTYPEPER<\text{n}> and PMXEVTYPER.

<table>
<thead>
<tr>
<th>PMEVTYPEPERn_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the read generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MRS reads at EL1 and EL0 using AArch64 of PMEVTYPEPER&lt;\text{n}&gt;_EL0 and PMXEVTYPER_EL0 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MRC reads at EL0 using Arch32 of PMEVTYPEPER&lt;\text{n}&gt; and PMXEVTYPER are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

When FEAT_FGT is implemented, then, regardless of the value of this bit, for each value n:

- If event counter n is not implemented, the following accesses are **UNDEFINED**:
  - In AArch64 state, a read of PMEVTYPEPER<\text{n}>_EL0, or, if n is not 31, a read of PMXEVTYPER_EL0 when PMSELR_EL0.SEL == n.
  - In AArch32 state, a read of PMEVTYPEPER<\text{n}>, or, if n is not 31, a read of PMXEVTYPER when PMSELR.SEL == n.
- If event counter n is implemented and EL2 is implemented and enabled in the current Security state, the following generate a Trap exception to EL2 from EL0 or EL1:
In AArch64 state, a read of PMEVTYPER<n>_EL0, or a read of PMXEVTYPER_EL0 when PMSELR_EL0.SEL == n, reported with EC syndrome value 0x18.

In AArch32 state, a read of PMEVTYPER<n>, or a read of PMXEVTYPER when PMSELR.SEL == n, reported with EC syndrome value 0x03.

See also HDFGRTR_EL2.PMCCFILTR_EL0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMEVCNTRn_EL0, bit [12]**

*When FEAT_PMUv3 is implemented:*

Traps MRS reads and MRC reads of multiple System registers.

Enables a trap to EL2 the following operations:

- At EL1 and EL0 using AArch64: MRS reads of PMEVCNTR<n>_EL0 and PMXEVCNTR_EL0.
- At EL0 using Arch32 when EL1 is using AArch64: MRC reads of PMEVCNTR<n> and PMXEVCNTR.

<table>
<thead>
<tr>
<th>PMEVCNTRn_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.E2H,TGE != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3,FGTEn == 0b1, then, unless the read generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MRS reads at EL1 and EL0 using AArch64 of PMEVCNTR&lt;n&gt;_EL0 and PMXEVCNTR_EL0 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MRC reads at EL0 using AArch32 of PMEVCNTR&lt;n&gt; and PMXEVCNTR are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

When FEAT_FGT is implemented, then, regardless of the value of this bit, for each value n:

- If event counter n is not implemented, the following accesses are UNDEFINED:
  - In AArch64 state, a read of PMEVCNTR<n>_EL0, or a read of PMXEVCNTR_EL0 when PMSELR_EL0.SEL == n.
  - In AArch32 state, a read of PMEVCNTR<n>, or a read of PMXEVCNTR when PMSELR.SEL == n.

- If event counter n is implemented, and EL2 is implemented and enabled in the current Security state, the following generate a Trap exception to EL2 from EL0 or EL1:
  - In AArch64 state, a read of PMEVCNTR<n>_EL0, or a read of PMXEVCNTR_EL0 when PMSELR_EL0.SEL == n, reported with EC syndrome value 0x18.
  - In AArch32 state, a read of PMEVCNTR<n>, or a read of PMXEVCNTR when PMSELR.SEL == n, reported with EC syndrome value 0x03.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**OSDLR_EL1, bit [11]**

*When FEAT_DoubleLock is implemented:*

Trap MRS reads of OSDLR_EL1 at EL1 using AArch64 to EL2.
OSDLR_EL1, Hypervisor Debug Fine-Grained Read Trap Register

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of OSDLR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of OSDLR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

OSECCR_EL1, bit [10]

Trap MRS reads of OSECCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of OSECCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of OSECCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

OSLSR_EL1, bit [9]

Trap MRS reads of OSLSR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of OSLSR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of OSLSR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Bit [8]

Reserved, RES0.

DBGPRCR_EL1, bit [7]

Trap MRS reads of DBGPRCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of DBGPRCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of DBGPRCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
**DBGAUTHSTATUS_EL1, bit [6]**

Trap MRS reads of **DBGAUTHSTATUS_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>DBGAUTHSTATUS_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>DBGAUTHSTATUS_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then <strong>MRS</strong> reads of <strong>DBGAUTHSTATUS_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGCLAIM, bit [5]**

Trap MRS reads of multiple System registers. Enables a trap on **MRS** reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **DBGCLAIMCLR_EL1**.
- **DBGCLAIMSET_EL1**.

<table>
<thead>
<tr>
<th><strong>DBGCLAIM</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then <strong>MRS</strong> reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**MDSCR_EL1, bit [4]**

Trap MRS reads of **MDSCR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>MDSCR_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>MDSCR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MRS reads of <strong>MDSCR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGWVRn_EL1, bit [3]**

Trap MRS reads of **DBGWVR<n>_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>DBGWVRn_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>DBGWVR&lt;n&gt;_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MRS reads of <strong>DBGWVR&lt;n&gt;_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>
If watchpoint n is not implemented, a read of DBGW<n>_EL1 is **UNDEFINED**.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGWCRn_EL1, bit [2]**

Trap MRS reads of DBGWCR<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGWCRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of DBGWCR&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of DBGWCR&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If watchpoint n is not implemented, a read of DBGWCR<n>_EL1 is **UNDEFINED**.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGVRn_EL1, bit [1]**

Trap MRS reads of DBGV<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGVRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of DBGV&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of DBGV&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If breakpoint n is not implemented, a read of DBGV<n>_EL1 is **UNDEFINED**.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGBCRn_EL1, bit [0]**

Trap MRS reads of DBGBC<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGBCRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of DBGBC&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of DBGBC&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If breakpoint n is not implemented, a read of DBGBC<n>_EL1 is **UNDEFINED**.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Accessing the HDFGRTR_EL2**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x1D0];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        HDFGRTR_EL2;
    end if;
elsif PSTATE.EL == EL3 then
    HDFGRTR_EL2 = X[t];
else
    HDFGRTR_EL2;
end if;

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x1D0] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        HDFGRTR_EL2 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    HDFGRTR_EL2 = X[t];
else
    HDFGRTR_EL2 = X[t];
end if;
The HDFGWTR_EL2 characteristics are:

**Purpose**

Provides controls for traps of MSR and MCR writes of debug, trace, PMU, and Statistical Profiling System registers.

**Configuration**

This register is present only when FEAT_FGT is implemented. Otherwise, direct accesses to HDFGWTR_EL2 are UNDEFINED.

**Attributes**

HDFGWTR_EL2 is a 64-bit register.

**Field descriptions**

The HDFGWTR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0, nPMSNEVFR_EL1</td>
<td>Reserved, 1 if EL2 is present and enabled, otherwise 0. If EL2 is enabled but not present, and nPMSNEVFR_EL1 is 1, a trap occurs.</td>
</tr>
<tr>
<td>62</td>
<td>nPMSNEVFR_EL1</td>
<td>If EL2 is implemented and enabled in the current Security state then MSR writes of PMSNEVFR_EL1 at EL1 using AArch64 are trapped to EL2, and reported with EC syndrome value 0x18, unless the write generates a higher priority exception. If this bit is 0, MSR writes of PMSNEVFR_EL1 are not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE and treated as zero when EL3 is implemented and SCR_EL3.FGTEn == 0b0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
Bits [61:58]

Reserved, RES0.

**PMUSERENR_EL0, bit [57]**

When FEAT_PMUv3 is implemented:

Trap MSR writes of `PMUSERENR_EL0` at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMUSERENR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <code>PMUSERENR_EL0</code> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <code>SCR_EL3.FGTEn == 0b1</code>, then MSR writes of <code>PMUSERENR_EL0</code> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**Bits [56:50]**

Reserved, RES0.

**TRFCR_EL1, bit [49]**

When FEAT_TRF is implemented:

Trap MSR writes of `TRFCR_EL1` at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRFCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <code>TRFCR_EL1</code> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <code>SCR_EL3.FGTEn == 0b1</code>, then MSR writes of <code>TRFCR_EL1</code> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TRCVICTLR, bit [48]**

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of `TRCVICTLR` at EL1 using AArch64 to EL2.
TRCVICTLR

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong></td>
</tr>
<tr>
<td>MSR writes of TRCVICTLR are not affected by this bit.</td>
</tr>
<tr>
<td><strong>0b1</strong></td>
</tr>
<tr>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td>SCR_EL3_FGTEn == 0b1, then MSR writes of TRCVICTLR</td>
</tr>
<tr>
<td>at EL1 using AArch64 are trapped to EL2 and reported</td>
</tr>
<tr>
<td>with EC syndrome value 0x18, unless the write generates</td>
</tr>
<tr>
<td>a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**Bit [47]**

Reserved, RES0.

**TRCSSCSRn, bit [46]**

When FEAT_ETMv4 is implemented, TRCSSCSR<n> are implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of TRCSSCSR<n> at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCSSCSRn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong></td>
<td>MSR writes of TRCSSCSR&lt;n&gt; are not affected by this bit.</td>
</tr>
<tr>
<td><strong>0b1</strong></td>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td></td>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td></td>
<td>SCR_EL3.FGTEn == 0b1, then MSR writes of TRCSSCSR&lt;n&gt; at EL1 using AArch64 are trapped to</td>
</tr>
<tr>
<td></td>
<td>EL2 and reported with EC syndrome value 0x18, unless the write generates</td>
</tr>
<tr>
<td></td>
<td>a higher priority exception.</td>
</tr>
</tbody>
</table>

If Single-shot Comparator n is not implementented, a write of TRCSSCSR<n> is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TRCSEQSTR, bit [45]**

When FEAT_ETMv4 is implemented, TRCSEQSTR is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of TRCSEQSTR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCSEQSTR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong></td>
<td>MSR writes of TRCSEQSTR are not affected by this bit.</td>
</tr>
<tr>
<td><strong>0b1</strong></td>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td></td>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td></td>
<td>SCR_EL3.FGTEn == 0b1, then MSR writes of TRCSEQSTR at EL1 using AArch64 are trapped to EL2</td>
</tr>
<tr>
<td></td>
<td>and reported with EC syndrome value 0x18, unless the write generates</td>
</tr>
<tr>
<td></td>
<td>a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Otherwise:

Reserved, RES0.

**TRCPRGCTLR, bit [44]**

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of TRCPRGCTLR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCPRGCTLR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TRCPRGCTLR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGETn == 0b1, then MSR writes of TRCPRGCTLR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**Bit [43]**

Reserved, RES0.

**TRCOSLAR, bit [42]**

When System register access to the PE Trace Unit registers is implemented and FEAT_ETMv4 is implemented:

Trap MSR writes of TRCOSLAR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCOSLAR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TRCOSLAR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGETn == 0b1, then MSR writes of TRCOSLAR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**TRCIMSPECn, bit [41]**

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of TRCIMSPEC<n> at EL1 using AArch64 to EL2.
TRCIMSPEC<n> are not affected by this bit.

0b1 If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of TRCIMSPEC<n> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.

TRCIMSPEC<1-7> are optional. If TRCIMSPEC<n> is not implemented, a write of TRCIMSPEC<n> is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

Bits [40:38]

Reserved, RES0.

TRCCNTVRn, bit [37]

When FEAT_ETMv4 is implemented, TRCCNTVR<n> are implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of TRCCNTVR<n> at EL1 using AArch64 to EL2.

0b0 MSR writes of TRCCNTVR<n> are not affected by this bit.

0b1 If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of TRCCNTVR<n> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.

If Counter n is not implemented, a write of TRCCNTVR<n> is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TRCCLAIM, bit [36]

When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- TRCCLAIMCLR.
- TRCCLAIMSET.
### TRCCLAIM

<table>
<thead>
<tr>
<th>TRCCLAIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or $SCR_EL3.FGTEn == 0b1$, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### TRCUXCTLR, bit [35]

**When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:**

Trap MSR writes of TRCAUXCTLR at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TRCUXCTLR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TRCAUXCTLR are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or $SCR_EL3.FGTEn == 0b1$, then MSR writes of TRCAUXCTLR at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### Bit [34]

Reserved, RES0.

### TRC, bit [33]

**When FEAT_ETMv4 is implemented and System register access to the PE Trace Unit registers is implemented:**

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- TRCACATR<n>.
- TRCACVR<n>.
- TRCBBCCTRL.
- TRCCCCTRL.
- TRCCIDCCTRLR0.
- TRCCIDCCTRLR1.
- TRCCIDCVR<n>.
- TRCCNTCTRLR<n>.
- TRCCNRDLDR<n>.
- TRCCONFIGR.
- TRCEVENTCTRL0R.
- TRCEVENTCTRL1R.
- TRCEXINTSELR.
- TRCQCTRLR.
- TRCSRCTRL<n>.
- TRCSEQEVR
- TRCSEQORSTEVFR
- TRCSSCCR<n>
- TRCSTPLLCTR
- TRCSYNCPR
- TRCTRACEIDR
- TRCTSTCLTR
- TRCVMIDCCTLR0
- TRCVMIDCCTLR1
- TRCVMIDCVR<n>

<table>
<thead>
<tr>
<th>TRC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

A write of an unimplemented register is **UNDEFINED**.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSLATFR_EL1, bit [32]**

When FEAT_SPE is implemented:

Trap MSR writes of **PMSLATFR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSLATFR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>PMSLATFR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of <strong>PMSLATFR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSIRR_EL1, bit [31]**

When FEAT_SPE is implemented:

Trap MSR writes of **PMSIRR_EL1** at EL1 using AArch64 to EL2.
<table>
<thead>
<tr>
<th>PMSIRR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMSIRR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of PMSIRR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [30]

Reserved, RES0.

PMSICR_EL1, bit [29]

When FEAT_SPE is implemented:

Trap MSR writes of PMSICR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSICR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMSICR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of PMSICR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSFCR_EL1, bit [28]

When FEAT_SPE is implemented:

Trap MSR writes of PMSFCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSFCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMSFCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of PMSFCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSEVFR_EL1, bit [27]
When FEAT_SPE is implemented:

Trap MSR writes of **PMSEVFR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSEVFR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>PMSEVFR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>PMSEVFR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMSCR_EL1**, bit [26]

When FEAT_SPE is implemented:

Trap MSR writes of **PMSCR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>PMSCR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>PMSCR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**PMBSR_EL1**, bit [25]

When FEAT_SPE is implemented:

Trap MSR writes of **PMBSR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMBSR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>PMBSR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>PMBSR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
PMBPTR_EL1, bit [24]

When FEAT_SPE is implemented:

Trap MSR writes of PMBPTR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMBPTR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMBPTR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of PMBPTR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMLIMITR_EL1, bit [23]

When FEAT_SPE is implemented:

Trap MSR writes of PMLIMITR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMLIMITR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMLIMITR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of PMLIMITR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [22]

Reserved, RES0.

PMCR_EL0, bit [21]

When FEAT_PMUv3 is implemented:

Trap MSR writes of PMCR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMCR at EL0 using AArch32 when EL1 is using AArch64 to EL2.
PMCR_EL0, bit [0]

When FEAT_PMUv3 is implemented:

<table>
<thead>
<tr>
<th>PMCR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>MSR writes of PMCR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMCR at EL0 using AArch32 are not affected by this bit.</td>
</tr>
<tr>
<td>b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2. {E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MSR writes of PMCR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MCR writes of PMCR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSWINC_EL0, bit [20]

When FEAT_PMUv3 is implemented:

Trap MSR writes of PMSWINC_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMSWINC at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PMSWINC_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>b0</td>
<td>MSR writes of PMSWINC_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMSWINC at EL0 using AArch32 are not affected by this bit.</td>
</tr>
<tr>
<td>b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2. {E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:</td>
</tr>
<tr>
<td></td>
<td>• MSR writes of PMSWINC_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td></td>
<td>• MCR writes of PMSWINC at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

PMSELR_EL0, bit [19]

When FEAT_PMUv3 is implemented:

Trap MSR writes of PMSELR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMSELR at EL0 using AArch32 when EL1 is using AArch64 to EL2.
<table>
<thead>
<tr>
<th>PMSELR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of PMSELR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMSELR at EL0 using AArch32 are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1       | If EL2 is implemented and enabled in the current Security state, \( \text{HCR_EL2} \{ \text{E2H,TGE} \} \neq \{1,1\} \), EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:  
  • MSR writes of PMSELR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.  
  • MCR writes of PMSELR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**PMOVS, bit [18]**

*When FEAT_PMUv3 is implemented:*

Trap MSR writes and MCR writes of multiple System registers.

Enables a trap to EL2 the following operations:

- At EL1 and EL0 using AArch64: MSR writes of PMOVSCLR_EL0 and PMOVSSET_EL0.
- At EL0 using AArch32 when EL1 is using AArch64: MCR writes of PMOVSRSR and PMOVSSET.

<table>
<thead>
<tr>
<th>PMOVS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1   | If EL2 is implemented and enabled in the current Security state, \( \text{HCR_EL2} \{ \text{E2H,TGE} \} \neq \{1,1\} \), EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:  
  • MSR writes at EL1 and EL0 using AArch64 of PMOVSCLR_EL0 and PMOVSSET_EL0 are trapped to EL2 and reported with EC syndrome value 0x18.  
  • MCR writes at EL0 using AArch32 of PMOVSRSR and PMOVSSET are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**PMINTEN, bit [17]**

*When FEAT_PMUv3 is implemented:*

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- PMINTENCLR_EL1.
- PMINTENSET_EL1.
<table>
<thead>
<tr>
<th>PMINTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**PMCNTEN, bit [16]**

**When FEAT_PMUv3 is implemented:**

- Trap MSR writes and MCR writes of multiple System registers.
- Enables a trap to EL2 the following operations:
  - At EL1 and EL0 using AArch64: MSR writes of PMCNTENCLR_EL0 and PMCNTENSET_EL0.
  - At EL0 using Arch32 when EL1 is using AArch64: MCR writes of PMCNTENCLR and PMCNTENSET.

<table>
<thead>
<tr>
<th>PMCNTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1     | If EL2 is implemented and enabled in the current Security state, HCR_EL2.{{E2H,TGE}} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:
  - MSR writes at EL1 and EL0 using AArch64 of PMCNTENCLR_EL0 and PMCNTENSET_EL0 are trapped to EL2 and reported with EC syndrome value 0x18.
  - MCR writes at EL0 using AArch32 of PMCNTENCLR and PMCNTENSET are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**PMCCNTR_EL0, bit [15]**

**When FEAT_PMUv3 is implemented:**

- Trap MSR writes of PMCCNTR_EL0 at EL1 and EL0 using AArch64 and MCR and MCRR writes of PMCCNTR at EL0 using AArch32 when EL1 is using AArch64 to EL2.
Meaning

0b0  MSR writes of PMCCNTR_EL0 at EL1 and EL0 using AArch64 and MCR and MCRR writes of PMCCNTR at EL0 using AArch32 are not affected by this bit.

0b1  If EL2 is implemented and enabled in the current Security state, HCR_EL2 {E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:

• MSR writes of PMCCNTR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.
• MCR and MCRR writes of PMCCNTR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03 (for MCR) or 0x04 (for MCRR).

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Reserved, RES0.

PMCCFILTR_EL0, bit [14]

When FEAT_PMUv3 is implemented:

Trap MSR writes of PMCCFILTR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMCCFILTR at EL0 using AArch32 when EL1 is using AArch64 to EL2.

Meaning

0b0  MSR writes of PMCCFILTR_EL0 at EL1 and EL0 using AArch64 and MCR writes of PMCCFILTR at EL0 using AArch32 are not affected by this bit.

0b1  If EL2 is implemented and enabled in the current Security state, HCR_EL2 {E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the write generates a higher priority exception:

• MSR writes of PMCCFILTR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.
• MCR writes of PMCCFILTR at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03.

PMCCFILTR_EL0 can also be accessed in AArch64 state using PMXEVTYPER_EL0 when PMSELR_EL0.SEL == 31, and PMCCFILTR can also be accessed in AArch32 state using PMXEVTYPER when PMSELR.SEL == 31.

Setting this bit to 1 has no effect on accesses to PMXEVTYPER_EL0 and PMXEVTYPER, regardless of the value of PMSELR_EL0.SEL or PMSELR.SEL.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Reserved, RES0.

PMEVTYPERn_EL0, bit [13]

When FEAT_PMUv3 is implemented:

Trap MSR writes and MCR writes of multiple System registers.

Enables a trap to EL2 the following operations:
• At EL1 and EL0 using AArch64: MSR writes of \texttt{PMEVTYPER<n>\_EL0} and \texttt{PMXEVTYPER\_EL0}
• At EL0 using Arch32 when EL1 is using AArch64: MCR writes of \texttt{PMEVTYPER<n>\_EL0} and \texttt{PMXEVTYPER}.

<table>
<thead>
<tr>
<th>PMEVTYPERn_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The operations listed above are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1              | If EL2 is implemented and enabled in the current Security state, \texttt{HCR\_EL2.E2H,TGE} != \{1,1\}, EL1 is using AArch64, and either EL3 is not implemented or \texttt{SCR\_EL3.FGTEn} == 0b1, then, unless the write generates a higher priority exception:  
• MSR writes at EL1 and EL0 using AArch64 of \texttt{PMEVTYPER<n>\_EL0} and \texttt{PMXEVTYPER\_EL0} are trapped to EL2 and reported with EC syndrome value 0x18.  
• MCR writes at EL0 using AArch32 of \texttt{PMEVTYPER<n>} and \texttt{PMXEVTYPER} are trapped to EL2 and reported with EC syndrome value 0x03. |

When \texttt{FEAT\_FGT} is implemented, then, regardless of the value of this bit, for each value \texttt{n}:

• If event counter \texttt{n} is not implemented, the following accesses are \texttt{UNDEFINED}:
  ◦ In AArch64 state, a write of \texttt{PMEVTYPER<n>\_EL0}, or if \texttt{n} is not 31, a write of \texttt{PMXEVTYPER\_EL0} when \texttt{PMSELR\_EL0.SEL == n}.  
  ◦ In AArch32 state, a write of \texttt{PMEVTYPER<n>}, or if \texttt{n} is not 31, a write of \texttt{PMXEVTYPER} when \texttt{PMSELR.SEL == n}.  
• If event counter \texttt{n} is implemented and EL2 is implemented and enabled in the current Security state, the following generate a Trap exception to EL2 from EL0 or EL1:
  ◦ In AArch64 state, a write of \texttt{PMEVTYPER<n>\_EL0}, or a write of \texttt{PMXEVTYPER\_EL0} when \texttt{PMSELR\_EL0.SEL == n}, reported with EC syndrome value 0x18.  
  ◦ In AArch32 state, a write of \texttt{PMEVTYPER<n>}, or a write of \texttt{PMXEVTYPER} when \texttt{PMSELR.SEL == n}, reported with EC syndrome value 0x03.

See also HDFGWTR\_EL2.PMCCFILTR\_EL0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

\textbf{Otherwise:}

Reserved, \texttt{RES0}.

\textbf{PMEVCNTRn\_EL0, bit [12]}

When \texttt{FEAT\_PMUv3} is implemented:

Trap MSR writes and MCR writes of multiple System registers.

Enables a trap to EL2 the following operations:

• At EL1 and EL0 using AArch64: MSR writes of \texttt{PMEVCNTR<n>\_EL0} and \texttt{PMXEVCNTR\_EL0}.  
• At EL0 using Arch32 when EL1 is using AArch64: MCR writes of \texttt{PMEVCNTR<n>\_EL0} and \texttt{PMXEVCNTR}.  

\texttt{HDFGWTR\_EL2, Hypervisor Debug Fine-Grained Write Trap Register}
Meaning

The operations listed above are not affected by this bit.

If EL2 is implemented and enabled in the current Security state, \( HCR\_{EL2} \{E2H,TGE\} \neq \{1,1\} \), EL1 is using AArch64, and either EL3 is not implemented or \( SCR\_{EL3}.FGTEn == 0b1 \), then, unless the write generates a higher priority exception:

- MSR writes at EL1 and EL0 using AArch64 of \( PMEVCNTR<\text{n}>_{EL0} \) and \( PMXEVCNTR\_EL0 \) are trapped to EL2 and reported with EC syndrome value 0x18.
- MCR writes at EL0 using AArch32 of \( PMEVCNTR<\text{n}> \) and \( PMXEVCNTR \) are trapped to EL2 and reported with EC syndrome value 0x03.

When FEAT\_FGT is implemented, then, regardless of the value of this bit, for each value \( \text{n} \):

- If event counter \( \text{n} \) is not implemented, the following accesses are UNDEFINED:
  - In AArch64 state, a write of \( PMEVCNTR<\text{n}>_{EL0} \) or a write of \( PMXEVCNTR\_EL0 \) when \( PMSELR\_EL0.SEL == \text{n} \).
  - In AArch32 state, a write of \( PMEVCNTR<\text{n}> \), or a write of \( PMXEVCNTR \) when \( PMSELR.SEL == \text{n} \).
- If event counter \( \text{n} \) is implemented, and EL2 is implemented and enabled in the current Security state, the following generate a Trap exception to EL2 from EL0 or EL1:
  - In AArch64 state, a write of \( PMEVCNTR<\text{n}>_{EL0} \), or a write of \( PMXEVCNTR\_EL0 \) when \( PMSELR\_EL0.SEL == \text{n} \), reported with EC syndrome value 0x18.
  - In AArch32 state, a write of \( PMEVCNTR<\text{n}> \), or a write of \( PMXEVCNTR \) when \( PMSELR.SEL == \text{n} \), reported with EC syndrome value 0x03.

On a Warm reset, in a system where the PE resets into EL2, this field resets to \( 0 \).

Otherwise:

Reserved, \( RES0 \).

**OSDLR\_EL1, bit [11]**

When FEAT\_DoubleLock is implemented:

Trap MSR writes of \( OSDLR\_EL1 \) at EL1 using AArch64 to EL2.

Meaning

MSR writes of \( OSDLR\_EL1 \) are not affected by this bit.

If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \( SCR\_{EL3}.FGTEn == 0b1 \), then MSR writes of \( OSDLR\_EL1 \) at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.

On a Warm reset, in a system where the PE resets into EL2, this field resets to \( 0 \).

Otherwise:

Reserved, \( RES0 \).

**OSECCR\_EL1, bit [10]**

Trap MSR writes of \( OSECCR\_EL1 \) at EL1 using AArch64 to EL2.
Bit [9]
Reserved, RES0.

OSLAR_EL1, bit [8]
Trap MSR writes of OSLAR_EL1 at EL1 using AArch64 to EL2.

---

OSLAR_EL1 Meanings

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of OSLAR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of OSLAR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

---

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DBGPRCR_EL1, bit [7]
Trap MSR writes of DBGPRCR_EL1 at EL1 using AArch64 to EL2.

---

DBGPRCR_EL1 Meanings

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of DBGPRCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of DBGPRCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

---

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Bit [6]
Reserved, RES0.

DBGCLAIM, bit [5]
Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- DBGCLAIMCLR_EL1
- DBGCLAIMSET_EL1

---

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
DBGCLAIM

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

MDSCR_EL1, bit [4]

Trap MSR writes of MDSCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>MDSCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of MDSCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DBGWVRn_EL1, bit [3]

Trap MSR writes of DBGWVR<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGWVRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of DBGWVR&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If watchpoint n is not implemented, a write of DBGWVR<n>_EL1 is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DBGWCRL_EL1, bit [2]

Trap MSR writes of DBGWCR<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGWCRL_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of DBGWCR&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If watchpoint n is not implemented, a write of DBGWCR<n>_EL1 is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
**DBGBVRn_EL1, bit [1]**

Trap MSR writes of \texttt{DBGBVR<n> EL1} at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGBVRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of \texttt{DBGBVR&lt;n&gt; EL1} are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \texttt{SCR_EL3.FGTeN == 0b1}, then MSR writes of \texttt{DBGBVR&lt;n&gt; EL1} at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If breakpoint n is not implemented, a write of \texttt{DBGBVR<n> EL1} is \texttt{UNDEFINED}. On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DBGBCRn_EL1, bit [0]**

Trap MSR writes of \texttt{DBGBCR<n> EL1} at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DBGBCRn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of \texttt{DBGBCR&lt;n&gt; EL1} are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \texttt{SCR_EL3.FGTeN == 0b1}, then MSR writes of \texttt{DBGBCR&lt;n&gt; EL1} at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If breakpoint n is not implemented, a write of \texttt{DBGBCR<n> EL1} is \texttt{UNDEFINED}. On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Accessing the HDFGWTR_EL2**

Accesses to this register use the following encodings:

\texttt{MRS <Xt>, HDFGWTR_EL2}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x1D8];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && SCR_EL3.FGTEn == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      HDFGWTR_EL2 = X[t];
  elsif PSTATE.EL == EL3 then
    HDFGWTR_EL2 = X[t];

MSR HDFGWTR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0011</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x1D8] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && SCR_EL3.FGTEn == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      HDFGWTR_EL2 = X[t];
  elsif PSTATE.EL == EL3 then
    HDFGWTR_EL2 = X[t];
HFGITR_EL2, Hypervisor Fine-Grained Instruction Trap Register

The HFGITR_EL2 characteristics are:

**Purpose**

Provides instruction trap controls.

**Configuration**

This register is present only when FEAT_FGT is implemented. Otherwise, direct accesses to HFGITR_EL2 are UNDEFINED.

**Attributes**

HFGITR_EL2 is a 64-bit register.

**Field descriptions**

The HFGITR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>DCCVAC</td>
</tr>
<tr>
<td>61</td>
<td>SVC_EL1</td>
</tr>
<tr>
<td>60</td>
<td>SVC_EL0</td>
</tr>
<tr>
<td>59</td>
<td>ERET</td>
</tr>
<tr>
<td>58</td>
<td>CPPRCTX</td>
</tr>
<tr>
<td>57</td>
<td>DVPRCTX</td>
</tr>
<tr>
<td>56</td>
<td>CFPRCTX</td>
</tr>
<tr>
<td>55</td>
<td>TLBIVAALE1</td>
</tr>
<tr>
<td>54</td>
<td>TLBIVALE1</td>
</tr>
<tr>
<td>53</td>
<td>TLBIVAAE1</td>
</tr>
<tr>
<td>52</td>
<td>TLBIASIDE1</td>
</tr>
<tr>
<td>51</td>
<td>TLBIVMALLE1</td>
</tr>
<tr>
<td>50</td>
<td>TLBIVALE1OS</td>
</tr>
<tr>
<td>49</td>
<td>TLBIRVAE1OS</td>
</tr>
<tr>
<td>48</td>
<td>TLBIVMALLE1OS</td>
</tr>
<tr>
<td>47</td>
<td>TLBIRVAE1OS</td>
</tr>
<tr>
<td>46</td>
<td>TLBIVAALE1OS</td>
</tr>
<tr>
<td>45</td>
<td>TLBIVALE1OS</td>
</tr>
<tr>
<td>44</td>
<td>TLBIVAAE1OS</td>
</tr>
<tr>
<td>43</td>
<td>TLBIASIDE1OS</td>
</tr>
<tr>
<td>42</td>
<td>TLBIVAE1OS</td>
</tr>
<tr>
<td>41</td>
<td>TLBIVMALLE1OS</td>
</tr>
<tr>
<td>40</td>
<td>TLBIRVAE1OS</td>
</tr>
<tr>
<td>39</td>
<td>ATS1E1WP</td>
</tr>
<tr>
<td>38</td>
<td>ATS1E1RP</td>
</tr>
<tr>
<td>37</td>
<td>ATS1E0W</td>
</tr>
<tr>
<td>36</td>
<td>ATS1E0R</td>
</tr>
<tr>
<td>35</td>
<td>ATS1E1W</td>
</tr>
<tr>
<td>34</td>
<td>ATS1E1R</td>
</tr>
<tr>
<td>33</td>
<td>DCZVA</td>
</tr>
<tr>
<td>32</td>
<td>DCCIVAC</td>
</tr>
<tr>
<td>31</td>
<td>DCCVADP</td>
</tr>
<tr>
<td>30</td>
<td>DCCVAP</td>
</tr>
<tr>
<td>29</td>
<td>DCCVAU</td>
</tr>
<tr>
<td>28</td>
<td>DCIVAC</td>
</tr>
<tr>
<td>27</td>
<td>ICIVAU</td>
</tr>
<tr>
<td>26</td>
<td>ICIALLU</td>
</tr>
<tr>
<td>25</td>
<td>ICIALLUIS</td>
</tr>
<tr>
<td>24</td>
<td>TLBIVAAE1IS</td>
</tr>
<tr>
<td>23</td>
<td>TLBIVALE1IS</td>
</tr>
<tr>
<td>22</td>
<td>TLBIVAAE1IS</td>
</tr>
<tr>
<td>21</td>
<td>TLBIASIDE1IS</td>
</tr>
<tr>
<td>20</td>
<td>TLBIVMALLE1IS</td>
</tr>
<tr>
<td>19</td>
<td>TLBIRVAE1IS</td>
</tr>
<tr>
<td>18</td>
<td>TLBIVMALLE1OS</td>
</tr>
<tr>
<td>17</td>
<td>TLBIRVAE1OS</td>
</tr>
<tr>
<td>16</td>
<td>ATS1E1WP</td>
</tr>
<tr>
<td>15</td>
<td>ATS1E1RP</td>
</tr>
<tr>
<td>14</td>
<td>ATS1E0W</td>
</tr>
<tr>
<td>13</td>
<td>ATS1E0R</td>
</tr>
<tr>
<td>12</td>
<td>ATS1E1W</td>
</tr>
<tr>
<td>11</td>
<td>ATS1E1R</td>
</tr>
<tr>
<td>10</td>
<td>DCZVA</td>
</tr>
<tr>
<td>9</td>
<td>DCCIVAC</td>
</tr>
<tr>
<td>8</td>
<td>DCCVADP</td>
</tr>
<tr>
<td>7</td>
<td>DCCVAP</td>
</tr>
<tr>
<td>6</td>
<td>DCCVAU</td>
</tr>
<tr>
<td>5</td>
<td>DCIVAC</td>
</tr>
<tr>
<td>4</td>
<td>ICIVAU</td>
</tr>
<tr>
<td>3</td>
<td>ICIALLU</td>
</tr>
<tr>
<td>2</td>
<td>ICIALLUIS</td>
</tr>
<tr>
<td>1</td>
<td>TLBIVAAE1</td>
</tr>
<tr>
<td>0</td>
<td>TLBIVALE1</td>
</tr>
</tbody>
</table>

**Bits [63:55]**

Reserved, RES0.

**DCCVAC, bit [54]**

Trap execution of multiple instructions. Enables a trap on execution at EL1 and EL0 using AArch64 of any of the following AArch64 instructions to EL2:

- **DC CVAC**, if FEAT_MTE is implemented.
- **DC CGVAC**, if FEAT_MTE is implemented.
- **DC CGDVAC**, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCCVAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, <strong>HCR_EL2, {E2H,TGE} != {1,1}</strong>, and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution at EL1 and EL0 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**SVC_EL1, bit [53]**

Trap execution of SVC at EL1 using AArch64 to EL2.
HFGITR_EL2, Hypervisor Fine-Grained Instruction Trap Register

<table>
<thead>
<tr>
<th>SVC_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of SVC is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of SVC at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x15, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**SVC_EL0, bit [52]**

Trap execution of SVC at EL0 using AArch64 and execution of SVC at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SVC_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of SVC at EL0 using AArch64 and execution of SVC at EL0 using AArch32 is not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1     | If EL2 is implemented and enabled in the current Security state, HCR_EL2.E2H,TGE != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then, unless the instruction generates a higher priority exception:  
  - Execution of SVC at EL0 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x15.  
  - Execution of SVC at EL0 using AArch32 is trapped to EL2 and reported with EC syndrome value 0x11. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**ERET, bit [51]**

Trap execution of multiple instructions. Enables a trap on execution at EL1 using AArch64 of any of the following AArch64 instructions to EL2:

- ERET.
- ERETTA, if FEAT_PAuth is implemented.
- ERETAB, if FEAT_PAuth is implemented.

<table>
<thead>
<tr>
<th>ERET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x1A, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

If EL2 is implemented and enabled in the current Security state, HCR_EL2.API == 0b0, and this bit enables a fine-grained trap on the instruction, then execution at EL1 using AArch64 of ERETTA or ERETTAB instructions is trapped to EL2 and reported with EC syndrome value 0x1A with its associated ISS field, as the fine-grained trap has higher priority than the trap enabled by HCR_EL2.API == 0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CPPRCTX, bit [50]**

When FEAT_SPECRES is implemented:

Trap execution of CPP RCTX at EL1 and EL0 using AArch64 and execution of CPPRCTX at EL0 using AArch32 when EL1 is using AArch64 to EL2.
<table>
<thead>
<tr>
<th>CPPRCTX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <code>CPPRCTX</code> at EL1 and EL0 using AArch64 and execution of <code>CPPRCTX</code> at EL0 using AArch32 is not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1     | If EL2 is implemented and enabled in the current Security state, `HCR_EL2`, `{E2H,TGE}` != `{1,1}`, EL1 is using AArch64, and either EL3 is not implemented or `SCR_EL3`.FGTEn == 0b1, then, unless the instruction generates a higher priority exception:  
  • Execution of `CPPRCTX` at EL1 and EL0 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18.  
  • Execution of `CPPRCTX` at EL0 using AArch32 is trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

<table>
<thead>
<tr>
<th>DVPRCTX, bit [49]</th>
</tr>
</thead>
</table>

When FEAT_SPECRES is implemented:

Trap execution of `DVPRCTX` at EL1 and EL0 using AArch64 and execution of `DVPRCTX` at EL0 using AArch32 when EL1 is using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DVPRCTX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <code>DVPRCTX</code> at EL1 and EL0 using AArch64 and execution of <code>DVPRCTX</code> at EL0 using AArch32 is not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1     | If EL2 is implemented and enabled in the current Security state, `HCR_EL2`, `{E2H,TGE}` != `{1,1}`, EL1 is using AArch64, and either EL3 is not implemented or `SCR_EL3`.FGTEn == 0b1, then, unless the instruction generates a higher priority exception:  
  • Execution of `DVPRCTX` at EL1 and EL0 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18.  
  • Execution of `DVPRCTX` at EL0 using AArch32 is trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

<table>
<thead>
<tr>
<th>CFPRCTX, bit [48]</th>
</tr>
</thead>
</table>

When FEAT_SPECRES is implemented:

Trap execution of `CFPRCTX` at EL1 and EL0 using AArch64 and execution of `CFPRCTX` at EL0 using AArch32 when EL1 is using AArch64 to EL2.
CFPRCTX

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong> Execution of <strong>CFP RCTX</strong> at EL1 and EL0 using AArch64 and execution of <strong>CFPRCTX</strong> at EL0 using AArch32 is not affected by this bit.</td>
</tr>
<tr>
<td><strong>0b1</strong> If EL2 is implemented and enabled in the current Security state, <strong>HCR_EL2</strong> {E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or <strong>SCR_EL3</strong> FGTEn == 0b1, then, unless the instruction generates a higher priority exception:</td>
</tr>
<tr>
<td>• Execution of <strong>CFP RCTX</strong> at EL1 and EL0 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18.</td>
</tr>
<tr>
<td>• Execution of <strong>CFPRCTX</strong> at EL0 using AArch32 is trapped to EL2 and reported with EC syndrome value 0x03.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

TLBIVAALE1, bit [47]

Trap execution of **TLBI VAALE1** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2** FGTnXS == 0b0, this field also traps execution of **TLBI VALE1NXS**.

<table>
<thead>
<tr>
<th>TLBIVAALE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong> Execution of <strong>TLBI VAALE1</strong> is not affected by this bit.</td>
<td></td>
</tr>
<tr>
<td><strong>0b1</strong> If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong> FGTEn == 0b1, then execution of <strong>TLBI VAALE1</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIVALE1, bit [46]

Trap execution of **TLBI VALE1** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2** FGTnXS == 0b0, this field also traps execution of **TLBI VALE1NXS**.

<table>
<thead>
<tr>
<th>TLBIVALE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>0b0</strong> Execution of <strong>TLBI VALE1</strong> is not affected by this bit.</td>
<td></td>
</tr>
<tr>
<td><strong>0b1</strong> If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong> FGTEn == 0b1, then execution of <strong>TLBI VALE1</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIVAAE1, bit [45]

Trap execution of **TLBI VAEE1** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2** FGTnXS == 0b0, this field also traps execution of **TLBI VAAE1NXS**.
TLBIVAE1, bit [43]

Trap execution of TLBI VAE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VAE1NXS.

<table>
<thead>
<tr>
<th>TLBIVAE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI VAE1 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI VAE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIVMALLE1, bit [42]

Trap execution of TLBI VMALLE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VMALLE1NXS.

<table>
<thead>
<tr>
<th>TLBIVMALLE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI VMALLE1 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI VMALLE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVAALE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVAALE1NXS.

<table>
<thead>
<tr>
<th>TLBIRVAALE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAALE1 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAALE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVALE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVALE1NXS.

<table>
<thead>
<tr>
<th>TLBIRVALE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVALE1 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVALE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVAAE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVAAE1NXS.

<table>
<thead>
<tr>
<th>TLBIRVAEE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAAE1 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAAE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Otherwise:
Reserved, RES0.

**TLBIRVAE1, bit [38]**

When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVAE1 at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVAE1NXS.

<table>
<thead>
<tr>
<th>TLBIRVAE1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAE1 is not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of TLBI RVAE1 is not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAE1 at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

**TLBIRVAALE1IS, bit [37]**

When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVAALE1IS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVAALE1ISNXS.

<table>
<thead>
<tr>
<th>TLBIRVAALE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAALE1IS is not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAALE1IS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td>Execution of TLBI RVAALE1IS is not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAALE1IS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

**TLBIRVALE1IS, bit [36]**

When FEAT_TLBIRANGE is implemented:

Trap execution of TLBI RVALE1IS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI RVALE1ISNXS.
TLBIRVALE1IS, bit [35]

When FEAT_TLBIRANGE is implemented:

<table>
<thead>
<tr>
<th>TLBIRVALE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI RVALE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then execution of <strong>TLBI RVALE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TLBIRVAEE1IS, bit [35]

When FEAT_TLBIRANGE is implemented:

Trap execution of **TLBI RVAAE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2**.FGTnXS == 0b0, this field also traps execution of **TLBI RVAAE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIRVAEE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI RVAAE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then execution of <strong>TLBI RVAAE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TLBIRVAE1IS, bit [34]

When FEAT_TLBIRANGE is implemented:

Trap execution of **TLBI RVAE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2**.FGTnXS == 0b0, this field also traps execution of **TLBI RVAE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIRVAE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI RVAE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then execution of <strong>TLBI RVAE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
TLBIVALE1IS, bit [33]

Trap execution of **TLBI VAALE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI VAALE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIVALE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI VAALE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI VAALE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIVALE1IS, bit [32]

Trap execution of **TLBI VALE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI VALE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIVALE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI VALE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI VALE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIVAAE1IS, bit [31]

Trap execution of **TLBI VAAE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI VAAE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIVAAE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI VAAE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI VAAE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TLBIASIDE1IS, bit [30]

Trap execution of **TLBI ASIDE1IS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI ASIDE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIASIDE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI ASIDE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI ASIDE1IS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TLBIVAE1IS, bit [29]**

Trap execution of **TLBI_VAE1IS** at EL1 using AArch64 to EL2.

If **FEAT_XS** is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI_VAE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIVAE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI_VAE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td></td>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td></td>
<td><strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI_VAE1IS</strong></td>
</tr>
<tr>
<td></td>
<td>at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome</td>
</tr>
<tr>
<td></td>
<td>value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TLBIVMALLE1IS, bit [28]**

Trap execution of **TLBI_VMALLE1IS** at EL1 using AArch64 to EL2.

If **FEAT_XS** is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI_VMALLE1ISNXS**.

<table>
<thead>
<tr>
<th>TLBIVMALLE1IS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI_VMALLE1IS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td></td>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td></td>
<td><strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI_VMALLE1IS</strong></td>
</tr>
<tr>
<td></td>
<td>at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome</td>
</tr>
<tr>
<td></td>
<td>value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TLBIRVAALE1OS, bit [27]**

When **FEAT_TLBIRANGE** is implemented and **FEAT_TLBIOS** is implemented:

Trap execution of **TLBI_RVAALE1OS** at EL1 using AArch64 to EL2.

If **FEAT_XS** is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI_RVAALE1OSNXS**.

<table>
<thead>
<tr>
<th>TLBIRVAALE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI_RVAALE1OS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current</td>
</tr>
<tr>
<td></td>
<td>Security state and either EL3 is not implemented or</td>
</tr>
<tr>
<td></td>
<td><strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI_RVAALE1OS</strong></td>
</tr>
<tr>
<td></td>
<td>at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome</td>
</tr>
<tr>
<td></td>
<td>value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, **RES0**.
TLBIRVALE1OS, bit [26]

When FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented:

Trap execution of TLBI RVALE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2 FGTnXS == 0b0, this field also traps execution of TLBI RVALE1OSNXS.

<table>
<thead>
<tr>
<th>TLBIRVALE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVALE1OS is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVALE1OS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TLBIRVAAE1OS, bit [25]

When FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented:

Trap execution of TLBI RVAAE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2 FGTnXS == 0b0, this field also traps execution of TLBI RVAAE1OSNXS.

<table>
<thead>
<tr>
<th>TLBIRVAAE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAAE1OS is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAAE1OS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

TLBIRVAE1OS, bit [24]

When FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented:

Trap execution of TLBI RVAE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2 FGTnXS == 0b0, this field also traps execution of TLBI RVAE1OSNXS.

<table>
<thead>
<tr>
<th>TLBIRVAE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI RVAE1OS is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI RVAE1OS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TLBIVALE1OS, bit [23]**

**When FEAT_TLBIOS is implemented:**

Trap execution of TLBI VAALE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VAALE1OSNXS.

<table>
<thead>
<tr>
<th>TLBIVALE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI VAALE1OS is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI VAALE1OS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TLBIVALE1OS, bit [22]**

**When FEAT_TLBIOS is implemented:**

Trap execution of TLBI VALE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VALE1OSNXS.

<table>
<thead>
<tr>
<th>TLBIVALE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI VALE1OS is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of TLBI VALE1OS at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TLBIVAAE1OS, bit [21]**

**When FEAT_TLBIOS is implemented:**

Trap execution of TLBI VAAE1OS at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VAAE1OSNXS.
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**TLBIASIDE10S, bit [20]**

When FEAT_TLBIS is implemented:

Trap execution of TLBI ASIDE10S at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI ASIDE10SNXS.

<table>
<thead>
<tr>
<th>TLBIASIDE10S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI ASIDE10S is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTeN == 0b1, then execution of TLBI ASIDE10S at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**TLBIVAE10S, bit [19]**

When FEAT_TLBIS is implemented:

Trap execution of TLBI VAE10S at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and HCRX_EL2.FGTnXS == 0b0, this field also traps execution of TLBI VAE10SNXS.

<table>
<thead>
<tr>
<th>TLBIVAE10S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of TLBI VAE10S is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTeN == 0b1, then execution of TLBI VAE10S at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**TLBIVMALLE10S, bit [18]**
When FEAT_TLBIOS is implemented:

Trap execution of **TLBI VMALLE1OS** at EL1 using AArch64 to EL2.

If FEAT_XS is implemented and **HCRX_EL2.FGTnXS == 0b0**, this field also traps execution of **TLBI VMALLE1OSNXS**.

<table>
<thead>
<tr>
<th>TLBIVMALLE1OS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>TLBI VMALLE1OS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>TLBI VMALLE1OS</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**ATS1E1WP, bit [17]**

When FEAT_PAN2 is implemented:

Trap execution of **AT S1E1WP** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ATS1E1WP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E1WP</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>AT S1E1WP</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**ATS1E1RP, bit [16]**

When FEAT_PAN2 is implemented:

Trap execution of **AT S1E1RP** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ATS1E1RP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E1RP</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then execution of <strong>AT S1E1RP</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Otherwise:

Reserved, RES0.

**ATS1E0W, bit [15]**

Trap execution of **AT S1E0W** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>ATS1E0W</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E0W</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of <strong>AT S1E0W</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**ATS1E0R, bit [14]**

Trap execution of **AT S1E0R** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>ATS1E0R</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E0R</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of <strong>AT S1E0R</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**ATS1E1W, bit [13]**

Trap execution of **AT S1E1W** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>ATS1E1W</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E1W</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of <strong>AT S1E1W</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**ATS1E1R, bit [12]**

Trap execution of **AT S1E1R** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>ATS1E1R</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of <strong>AT S1E1R</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of <strong>AT S1E1R</strong> at EL1 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
DCZVA, bit [11]

Trap execution of multiple instructions. Enables a trap on execution at EL1 and EL0 using AArch64 of any of the following AArch64 instructions to EL2:

- **DC ZVA**, if FEAT_MTE is implemented.
- **DC GVA**, if FEAT_MTE is implemented.
- **DC GZVA**, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCZVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 and EL0 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DCCIVAC, bit [10]

Trap execution of multiple instructions. Enables a trap on execution at EL1 and EL0 using AArch64 of any of the following AArch64 instructions to EL2:

- **DC CIVAC**.
- **DC CIGVAC**, if FEAT_MTE is implemented.
- **DC CIGDVAC**, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCCIVAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 and EL0 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DCCVADP, bit [9]

**When FEAT_DP82 is implemented:**

Trap execution of multiple instructions. Enables a trap on execution at EL1 and EL0 using AArch64 of any of the following AArch64 instructions to EL2:

- **DC CVADP**.
- **DC CGVADP**, if FEAT_MTE is implemented.
- **DC CGDVADP**, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCCVADP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.(E2H,TGE) != {1,1}, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 and EL0 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Otherwise:
Reserved, RES0.

**DCCVAP, bit [8]**

Trap execution of multiple instructions. Enables a trap on execution at EL1 and EL0 using AArch64 of any of the following AArch64 instructions to EL2:

- DC_CVAP
- DC_CGVAP, if FEAT_MTE is implemented.
- DC_CGDVAP, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCCVAP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.E2H,TGE != (1,1), and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 and EL0 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DCCVAU, bit [7]**

Trap execution of DC_CVAU at EL1 and EL0 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DCCVAU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of DC_CVAU is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.E2H,TGE != (1,1), and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution of DC_CVAU at EL1 and EL0 using AArch64 is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DCCISW, bit [6]**

Trap execution of multiple instructions. Enables a trap on execution at EL1 using AArch64 of any of the following AArch64 instructions to EL2:

- DC_CISW
- DC_CIGSW, if FEAT_MTE is implemented.
- DC_CIGDSW, if FEAT_MTE is implemented.

<table>
<thead>
<tr>
<th>DCCISW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**DCCSW, bit [5]**

Trap execution of multiple instructions. Enables a trap on execution at EL1 using AArch64 of any of the following AArch64 instructions to EL2:
• **DC CSW**, if FEAT_MTE is implemented.
• **DC CGSW**, if FEAT_MTE is implemented.

### DCCSW

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

### DCISW, bit [4]

Trap execution of multiple instructions. Enables a trap on execution at EL1 using AArch64 of any of the following AArch64 instructions to EL2:

• **DC ISW**.
• **DC IGSW**, if FEAT_MTE is implemented.
• **DC IGDSW**, if FEAT_MTE is implemented.

### DCIVAC

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the instructions listed above is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then execution at EL1 using AArch64 of any of the instructions listed above is trapped to EL2 and reported with EC syndrome value 0x18, unless the instruction generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

### DCIVAC, bit [3]

Trap execution of multiple instructions. Enables a trap on execution at EL1 using AArch64 of any of the following AArch64 instructions to EL2:

• **DC IVAC**.
• **DC IGVAC**, if FEAT_MTE is implemented.
• **DC IGDVAC**, if FEAT_MTE is implemented.

### DCIVAU, bit [2]

Trap execution of **IC IVAU** at EL1 and EL0 using AArch64 to EL2.
ICIVAU

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  Execution of <strong>IC IVAU</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1  If EL2 is implemented and enabled in the current Security state,</td>
</tr>
<tr>
<td><strong>HCR_EL2</strong>.[E2H,TGE] != (1,1), and either EL3 is not</td>
</tr>
<tr>
<td>implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then execution of **IC</td>
</tr>
<tr>
<td>IVAU** at EL1 and EL0 using AArch64 is trapped to EL2 and</td>
</tr>
<tr>
<td>reported with EC syndrome value 0x18, unless the instruction</td>
</tr>
<tr>
<td>generates a higher priority exception.</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>On a Warm reset, in a system where the PE resets into EL2, this field</td>
</tr>
<tr>
<td>resets to 0.</td>
</tr>
</tbody>
</table>

**ICIALLU, bit [1]**

Trap execution of **IC IALLU** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  Execution of <strong>IC IALLU</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1  If EL2 is implemented and enabled in the current Security state</td>
</tr>
<tr>
<td>and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1,</td>
</tr>
<tr>
<td>then execution of <strong>IC IALLU</strong> at EL1 using AArch64 is</td>
</tr>
<tr>
<td>trapped to EL2 and reported with EC syndrome value 0x18, unless</td>
</tr>
<tr>
<td>the instruction generates a higher priority exception.</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>On a Warm reset, in a system where the PE resets into EL2, this field</td>
</tr>
<tr>
<td>resets to 0.</td>
</tr>
</tbody>
</table>

**ICIALLUIS, bit [0]**

Trap execution of **IC IALLUIS** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  Execution of <strong>IC IALLUIS</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1  If EL2 is implemented and enabled in the current Security state</td>
</tr>
<tr>
<td>and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1,</td>
</tr>
<tr>
<td>then execution of <strong>IC IALLUIS</strong> at EL1 using AArch64 is</td>
</tr>
<tr>
<td>trapped to EL2 and reported with EC syndrome value 0x18, unless</td>
</tr>
<tr>
<td>the instruction generates a higher priority exception.</td>
</tr>
<tr>
<td></td>
</tr>
<tr>
<td>On a Warm reset, in a system where the PE resets into EL2, this field</td>
</tr>
<tr>
<td>resets to 0.</td>
</tr>
</tbody>
</table>

**Accessing the HFGITR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, HFGITR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x1C8];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    HFGITR_EL2 = X[t];
  end
elsif PSTATE.EL == EL3 then
  return HFGITR_EL2;
end

MSR HFGITR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x1C8] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    HFGITR_EL2 = X[t];
  end
elsif PSTATE.EL == EL3 then
  HFGITR_EL2 = X[t];
The HFGRTR_EL2 characteristics are:

**Purpose**

Provides controls for traps of MRS and MRC reads of System registers.

**Configuration**

This register is present only when FEAT_FGT is implemented. Otherwise, direct accesses to HFGRTR_EL2 are UNDEFINED.

**Attributes**

HFGRTR_EL2 is a 64-bit register.

**Field descriptions**

The HFGRTR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>nACCDATA_EL1</td>
</tr>
<tr>
<td>61</td>
<td>ERXADDR_EL1</td>
</tr>
<tr>
<td>60</td>
<td>ERXPFGCDN_EL1</td>
</tr>
<tr>
<td>59</td>
<td>ERXPFGCTL_EL1</td>
</tr>
<tr>
<td>58</td>
<td>ERXPFGF_EL1</td>
</tr>
<tr>
<td>57</td>
<td>ERXMISCn_EL1</td>
</tr>
<tr>
<td>56</td>
<td>ERXSTATUS_EL1</td>
</tr>
<tr>
<td>55</td>
<td>ERXCTLR_EL1</td>
</tr>
<tr>
<td>54</td>
<td>ERXFR_EL1</td>
</tr>
<tr>
<td>53</td>
<td>ERRSELR_EL1</td>
</tr>
<tr>
<td>52</td>
<td>ERRIDR_EL1</td>
</tr>
<tr>
<td>51</td>
<td>ICC_IGRPENn_EL1</td>
</tr>
<tr>
<td>50</td>
<td>VBAR_EL1</td>
</tr>
<tr>
<td>49</td>
<td>TTBR1_EL1</td>
</tr>
<tr>
<td>48</td>
<td>TTBR0_EL1</td>
</tr>
<tr>
<td>47</td>
<td>TPIDR_EL0</td>
</tr>
<tr>
<td>46</td>
<td>TPIDRRO_EL0</td>
</tr>
<tr>
<td>45</td>
<td>TPIDR_EL1</td>
</tr>
<tr>
<td>44</td>
<td>TCR_EL1</td>
</tr>
<tr>
<td>43</td>
<td>SCXTNUM_EL0</td>
</tr>
<tr>
<td>42</td>
<td>SCXTNUM_EL1</td>
</tr>
<tr>
<td>41</td>
<td>SCTLR_EL1</td>
</tr>
<tr>
<td>40</td>
<td>REVIDR_EL1</td>
</tr>
<tr>
<td>39</td>
<td>PAR_EL1</td>
</tr>
<tr>
<td>38</td>
<td>MPIDR_EL1</td>
</tr>
<tr>
<td>37</td>
<td>MIDR_EL1</td>
</tr>
<tr>
<td>36</td>
<td>MAIR_EL1</td>
</tr>
<tr>
<td>35</td>
<td>LORN_EL1</td>
</tr>
<tr>
<td>34</td>
<td>LORSA_EL1</td>
</tr>
<tr>
<td>33</td>
<td>LORID_EL1</td>
</tr>
<tr>
<td>32</td>
<td>LOREA_EL1</td>
</tr>
<tr>
<td>31</td>
<td>LORC_EL1</td>
</tr>
<tr>
<td>30</td>
<td>ISR_EL1</td>
</tr>
<tr>
<td>29</td>
<td>FAR_EL1</td>
</tr>
<tr>
<td>28</td>
<td>ESR_EL1</td>
</tr>
<tr>
<td>27</td>
<td>DCZID_EL0</td>
</tr>
<tr>
<td>26</td>
<td>CTR_EL0</td>
</tr>
<tr>
<td>25</td>
<td>CSSELR_EL1</td>
</tr>
<tr>
<td>24</td>
<td>CPACR_EL1</td>
</tr>
<tr>
<td>23</td>
<td>CONTEXTIDR_EL1</td>
</tr>
<tr>
<td>22</td>
<td>CLIDR_EL1</td>
</tr>
<tr>
<td>21</td>
<td>CCSIDR_EL1</td>
</tr>
<tr>
<td>20</td>
<td>APIBKey</td>
</tr>
<tr>
<td>19</td>
<td>APIAKey</td>
</tr>
<tr>
<td>18</td>
<td>APGAKey</td>
</tr>
<tr>
<td>17</td>
<td>APDBKey</td>
</tr>
<tr>
<td>16</td>
<td>APDAKey</td>
</tr>
<tr>
<td>15</td>
<td>AMAIR_EL1</td>
</tr>
<tr>
<td>14</td>
<td>AIDR_EL1</td>
</tr>
<tr>
<td>13</td>
<td>AFSR1_EL1</td>
</tr>
<tr>
<td>12</td>
<td>AFSR0_EL1</td>
</tr>
<tr>
<td>11</td>
<td>0</td>
</tr>
<tr>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>9</td>
<td>0</td>
</tr>
<tr>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:51]**

Reserved, RES0.

**nACCDATA_EL1, bit [50]**

When FEAT_LS64 is implemented:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If EL2 is implemented and enabled in the current Security state then MRS reads of ACCDATA_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td>MRS reads of ACCDATA_EL1 are not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE and treated as zero when EL3 is implemented and SCR_EL3 FGTEn == 0b0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
ERXADDR_EL1, bit [49]

When FEAT_RAS is implemented:

Trap MRS reads of ERXADDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXADDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERXADDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERXADDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Reserved, RES0.

ERXPFGCDN_EL1, bit [48]

When FEAT_RASv1p1 is implemented:

Trap MRS reads of ERXPFGCDN_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXPFGCDN_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERXPFGCDN_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERXPFGCDN_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Reserved, RES0.

ERXPFGCTL_EL1, bit [47]

When FEAT_RASv1p1 is implemented:

Trap MRS reads of ERXPFGCTL_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXPFGCTL_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERXPFGCTL_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERXPFGCTL_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
HFGTR_EL2, Hypervisor Fine-Grained Read Trap Register

Otherwise:
Reserved, RES0.

ERXPFGF_EL1, bit [46]

When FEAT_RAS is implemented:

Trap MRS reads of ERXPFGF_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXPFGF_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERXPFGF_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERXPFGF_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

ERXMISCn_EL1, bit [45]

When FEAT_RAS is implemented:

Trap MRS reads of ERXMISC<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXMISCn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERXMISC&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERXMISC&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

ERXSTATUS_EL1, bit [44]

When FEAT_RAS is implemented:

Trap MRS reads of ERXSTATUS_EL1 at EL1 using AArch64 to EL2.
**ERXSTATUS_EL1**

| Meaning | 
|---|---|
| **0b0** | MRS reads of **ERXSTATUS_EL1** are not affected by this bit. |
| **0b1** | If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \( \text{SCR}_{EL3}.\text{FGTEn} == 0b1 \), then MRS reads of **ERXSTATUS_EL1** at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**ERXCTRLR_EL1, bit [43]**

When FEAT_RAS is implemented:

Trap MRS reads of **ERXCTRLR_EL1** at EL1 using AArch64 to EL2.

| Meaning | 
|---|---|
| **0b0** | MRS reads of **ERXCTRLR_EL1** are not affected by this bit. |
| **0b1** | If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \( \text{SCR}_{EL3}.\text{FGTEn} == 0b1 \), then MRS reads of **ERXCTRLR_EL1** at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**ERXFR_EL1, bit [42]**

When FEAT_RAS is implemented:

Trap MRS reads of **ERXFR_EL1** at EL1 using AArch64 to EL2.

| Meaning | 
|---|---|
| **0b0** | MRS reads of **ERXFR_EL1** are not affected by this bit. |
| **0b1** | If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or \( \text{SCR}_{EL3}.\text{FGTEn} == 0b1 \), then MRS reads of **ERXFR_EL1** at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
ERRSEL_R_EL1, bit [41]

When FEAT_RAS is implemented:

Trap MRS reads of ERRSEL_R_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERRSEL_R_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERRSEL_R_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERRSEL_R_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

ERRIDR_EL1, bit [40]

When FEAT_RAS is implemented:

Trap MRS reads of ERRIDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERRIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ERRIDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ERRIDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

ICC_IGRPENn_EL1, bit [39]

When FEAT_GICv3 is implemented:

Trap MRS reads of ICC_IGRPEN<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ICC_IGRPENn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ICC_IGRPEN&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ICC_IGRPEN&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Reserved, RES0.

**VBAR_EL1, bit [38]**

Trap MRS reads of **VBAR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>VBAR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>VBAR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of <strong>VBAR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TTBR1_EL1, bit [37]**

Trap MRS reads of **TTBR1_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TTBR1_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>TTBR1_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of <strong>TTBR1_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TTBRO_EL1, bit [36]**

Trap MRS reads of **TTBRO_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TTBRO_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>TTBRO_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of <strong>TTBRO_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TPIDR_EL0, bit [35]**

Trap MRS reads of **TPIDR_EL0** at EL1 and EL0 using AArch64 and MRC reads of **TPIDRURW** at EL0 using AArch32 when EL1 is using AArch64 to EL2.
TPIDR_EL0

**Meaning**

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <code>TPIDR_EL0</code> at EL1 and EL0 using AArch64 and MRC reads of <code>TPIDRURW</code> at EL0 using AArch32 are not affected by this bit.</td>
</tr>
</tbody>
</table>
| 0b1       | If EL2 is implemented and enabled in the current Security state, `HCR_EL2`.{E2H,TGE} != {1,1}, EL1 is using AArch64, and either EL3 is not implemented or `SCR_EL3` FGTEn == 0b1, then, unless the read generates a higher priority exception:  
  * MRS reads of `TPIDR_EL0` at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18.  
  * MRC reads of `TPIDRURW` at EL0 using AArch32 are trapped to EL2 and reported with EC syndrome value 0x03. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TPIDR_EL0**, bit [34]

Trap MRS reads of `TPIDR_EL0` at EL1 and EL0 using AArch64 and MRC reads of `TPIDRURW` at EL0 using AArch32 when EL1 is using AArch64 to EL2.

TPIDR_EL1

**Meaning**

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <code>TPIDR_EL1</code> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <code>SCR_EL3</code> FGTEn == 0b1, then MRS reads of <code>TPIDR_EL1</code> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TCR_EL1**, bit [32]

Trap MRS reads of `TCR_EL1` at EL1 using AArch64 to EL2.

**TCR_EL1**

**Meaning**

<table>
<thead>
<tr>
<th>Bit Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <code>TCR_EL1</code> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <code>SCR_EL3</code> FGTEn == 0b1, then MRS reads of <code>TCR_EL1</code> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**SCXTNUM_EL0, bit [31]**

When FEAT_CSV2 is implemented:

Trap MRS reads of SCXTNUM_EL0 at EL1 and EL0 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCXTNUM_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of SCXTNUM_EL0 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2. {E2H,TGE} != {1,1}, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of SCXTNUM_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**SCXTNUM_EL1, bit [30]**

When FEAT_CSV2 is implemented:

Trap MRS reads of SCXTNUM_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCXTNUM_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of SCXTNUM_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of SCXTNUM_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**SCTLR_EL1, bit [29]**

Trap MRS reads of SCTLR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCTLR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of SCTLR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of SCTLR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
**REVIDR_EL1, bit [28]**

Trap MRS reads of **REVIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>REVIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>REVIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>REVIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**PAR_EL1, bit [27]**

Trap MRS reads of **PAR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>PAR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>PAR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>PAR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**MPIDR_EL1, bit [26]**

Trap MRS reads of **MPIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>MPIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>MPIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>MPIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**MIDR_EL1, bit [25]**

Trap MRS reads of **MIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>MIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>MIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>MIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**MAIR_EL1, bit [24]**

Trap MRS reads of **MAIR_EL1** at EL1 using AArch64 to EL2.
**MAIR_EL1**

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>MAIR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>MAIR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**LORSA_EL1**, bit [23]

**When FEAT_LOR is implemented:**

Trap MRS reads of **LORSA_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>LORSA_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>LORSA_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**LORN_EL1**, bit [22]

**When FEAT_LOR is implemented:**

Trap MRS reads of **LORN_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>LORN_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>LORN_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**LORID_EL1**, bit [21]

**When FEAT_LOR is implemented:**

Trap MRS reads of **LORID_EL1** at EL1 using AArch64 to EL2.
<table>
<thead>
<tr>
<th>LORID_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of LORID_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of LORID_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

<table>
<thead>
<tr>
<th>LOREA_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of LOREA_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of LOREA_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

<table>
<thead>
<tr>
<th>LORC_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of LORC_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of LORC_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

<table>
<thead>
<tr>
<th>ISR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ISR_EL1 at EL1 using AArch64 to EL2.</td>
</tr>
</tbody>
</table>

Trap MRS reads of ISR_EL1 at EL1 using AArch64 to EL2.
ISR_EL1, bit [16]

<table>
<thead>
<tr>
<th>ISR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ISR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ISR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

FAR_EL1, bit [17]

Trap MRS reads of FAR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>FAR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of FAR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of FAR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

ESR_EL1, bit [16]

Trap MRS reads of ESR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ESR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of ESR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of ESR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

DCZID_EL0, bit [15]

Trap MRS reads of DCZID_EL0 at EL1 and EL0 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>DCZID_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of DCZID_EL0 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != (1,1), and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of DCZID_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

CTR_EL0, bit [14]

Trap MRS reads of CTR_EL0 at EL1 and EL0 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CTR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of CTR_EL0 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2.{E2H,TGE} != (1,1), and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of CTR_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CSSELR_EL1, bit [13]**

Trap MRS reads of CSSELR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CSSELR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of CSSELR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of CSSELR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CPACR_EL1, bit [12]**

Trap MRS reads of CPACR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CPACR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of CPACR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of CPACR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CONTEXTIDR_EL1, bit [11]**

Trap MRS reads of CONTEXTIDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CONTEXTIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of CONTEXTIDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of CONTEXTIDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CLIDR_EL1, bit [10]**

Trap MRS reads of CLIDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CLIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of CLIDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of CLIDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
**CCSIDR_EL1, bit [9]**

Trap MRS reads of **CCSIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CCSIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>CCSIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MRS reads of <strong>CCSIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**APIBKey, bit [8]**

*When FEAT_PAuth is implemented:*

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APIBKeyHi_EL1**.
- **APIBKeyLo_EL1**.

<table>
<thead>
<tr>
<th>APIBKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**APIAKey, bit [7]**

*When FEAT_PAuth is implemented:*

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APIAKeyHi_EL1**.
- **APIAKeyLo_EL1**.

<table>
<thead>
<tr>
<th>APIAKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
When FEAT_PAuth is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- APGAKeyHi_EL1
- APGAKeyLo_EL1

### APGAKey

<table>
<thead>
<tr>
<th>APGAKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

APDBKey, bit [5]

When FEAT_PAuth is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- APDBKeyHi_EL1
- APDBKeyLo_EL1

### APDBKey

<table>
<thead>
<tr>
<th>APDBKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

APDAKey, bit [4]

When FEAT_PAuth is implemented:

Trap MRS reads of multiple System registers. Enables a trap on MRS reads at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- APDAKeyHi_EL1
- APDAKeyLo_EL1
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Reserved, RES0.

**AMAIR_EL1, bit [3]**

Trap MRS reads of **AMAIR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>AMAIR_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>AMAIR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>AMAIR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**AIDR_EL1, bit [2]**

Trap MRS reads of **AIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>AIDR_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>AIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>AIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**AFSR1_EL1, bit [1]**

Trap MRS reads of **AFSR1_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>AFSR1_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of <strong>AFSR1_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MRS reads of <strong>AFSR1_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**AFSR0_EL1, bit [0]**

Trap MRS reads of **AFSR0_EL1** at EL1 using AArch64 to EL2.
<table>
<thead>
<tr>
<th>AFSR0_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MRS reads of AFSR0_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MRS reads of AFSR0_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the read generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Accessing the HFGTRTR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, HFGTRTR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x1B8];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return HFGTRTR_EL2;
    elsif PSTATE.EL == EL3 then
        return HFGTRTR_EL2;

MSR HFGTRTR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x1B8] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        HFGRTR_EL2 = X[t];
    end
elsif PSTATE.EL == EL3 then
    HFGRTR_EL2 = X[t];
HFGWTR_EL2, Hypervisor Fine-Grained Write Trap Register

The HFGWTR_EL2 characteristics are:

**Purpose**

Provides controls for traps of MSR and MCR writes of System registers.

**Configuration**

This register is present only when FEAT_FGT is implemented. Otherwise, direct accesses to HFGWTR_EL2 are UNDEFINED.

**Attributes**

HFGWTR_EL2 is a 64-bit register.

**Field descriptions**

The HFGWTR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>SCXTNUM_EL0</td>
<td>SCXTNUM_EL1</td>
<td>SCTLR_EL1</td>
<td>RES0</td>
<td>PAR_EL1</td>
<td>RES0</td>
<td>MAIR_EL1</td>
<td>LORSA_EL1</td>
<td>LORN_EL1</td>
<td>RES0</td>
<td>LOREA_EL1</td>
<td>LORC_EL1</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
</tr>
</tbody>
</table>

**Bits [63:51]**

Reserved, RES0.

**nACCDATA_EL1, bit [50]**

When FEAT_LS64 is implemented:

Trap MSR writes of ACCDATA_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>nACCDATA_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If EL2 is implemented and enabled in the current Security state then MSR writes of ACCDATA_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td>MSR writes of ACCDATA_EL1 are not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE and treated as zero when EL3 is implemented and SCR_EL3 FGTEn == 0b0.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
ERTXADD_EL1, bit [48]

When FEAT_RAS is implemented:

Trap MSR writes of ERXADDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXADDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXADDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of ERXADDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

ERXPFGCDN_EL1, bit [48]

When FEAT_RASv1p1 is implemented:

Trap MSR writes of ERXPFGCDN_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXPFGCDN_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXPFGCDN_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of ERXPFGCDN_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

ERXPFGCTL_EL1, bit [47]

When FEAT_RASv1p1 is implemented:

Trap MSR writes of ERXPFGCTL_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXPFGCTL_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXPFGCTL_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of ERXPFGCTL_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
Otherwise:
Reserved, RES0.

Bit [46]
Reserved, RES0.

**ERXMISCn_EL1, bit [45]**

When FEAT_RAS is implemented:

Trap MSR writes of ERXMISC<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXMISCn_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXMISC&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of ERXMISC&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

**ERXSTATUS_EL1, bit [44]**

When FEAT_RAS is implemented:

Trap MSR writes of ERXSTATUS_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>ERXSTATUS_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXSTATUS_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of ERXSTATUS_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:
Reserved, RES0.

**ERXCTLR_EL1, bit [43]**

When FEAT_RAS is implemented:

Trap MSR writes of ERXCTLR_EL1 at EL1 using AArch64 to EL2.
ERXCTRL_EL1

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERXCTRL_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTen == 0b1, then MSR writes of ERXCTRL_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [42]

Reserved, RES0.

ERRSELR_EL1, bit [41]

When FEAT_RAS is implemented:

Trap MSR writes of ERRSELR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ERRSELR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTen == 0b1, then MSR writes of ERRSELR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [40]

Reserved, RES0.

ICC_IGRPEN<n>_EL1, bit [39]

When FEAT_GICv3 is implemented:

Trap MSR writes of ICC_IGRPEN<n>_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of ICC_IGRPEN&lt;n&gt;_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTen == 0b1, then MSR writes of ICC_IGRPEN&lt;n&gt;_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**VBAR_EL1, bit [38]**

Trap MSR writes of **VBAR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>VBAR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>VBAR_EL1</strong> are not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>VBAR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TTBR1_EL1, bit [37]**

Trap MSR writes of **TTBR1_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TTBR1_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>TTBR1_EL1</strong> are not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>TTBR1_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TTBR0_EL1, bit [36]**

Trap MSR writes of **TTBR0_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TTBR0_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>TTBR0_EL1</strong> are not affected by this bit. If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>TTBR0_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**TPIDR_EL0, bit [35]**

Trap MSR writes of **TPIDR_EL0** at EL1 and EL0 using AArch64 and MCR writes of **TPIDRURW** at EL0 using AArch32 when EL1 is using AArch64 to EL2.
TPIDR_EL0, bit [34]

Trap MSR writes of TPIDR_EL0 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TPIDR_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TPIDR_EL0 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, SCR_EL3.FGTEn == 0b1, then MSR writes of TPIDR_EL0 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TPIDR_EL1, bit [33]

Trap MSR writes of TPIDR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TPIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TPIDR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of TPIDR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

TCR_EL1, bit [32]

Trap MSR writes of TCR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>TCR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of TCR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of TCR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
SCXTNUM_EL0, bit [31]

When FEAT_CSV2 is implemented:

Trap MSR writes of SCXTNUM_EL0 at EL1 and EL0 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCXTNUM_EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of SCXTNUM_EL0 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, HCR_EL2, {E2H,TGE} != {1,1}, and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of SCXTNUM_EL0 at EL1 and EL0 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

SCXTNUM_EL1, bit [30]

When FEAT_CSV2 is implemented:

Trap MSR writes of SCXTNUM_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCXTNUM_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of SCXTNUM_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of SCXTNUM_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

SCTLR_EL1, bit [29]

Trap MSR writes of SCTLR_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>SCTLR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of SCTLR_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of SCTLR_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Bit [28]

Reserved, RES0.
**PAR_EL1, bit [27]**

Trap MSR writes of **PAR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>PAR_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>PAR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>PAR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bits [26:25]**

Reserved, RES0.

**MAIR_EL1, bit [24]**

Trap MSR writes of **MAIR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>MAIR_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>MAIR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>MAIR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**LORSA_EL1, bit [23]**

When FEAT_LOR is implemented:

Trap MSR writes of **LORSA_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>LORSA_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>LORSA_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>LORSA_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**LORN_EL1, bit [22]**

When FEAT_LOR is implemented:

Trap MSR writes of **LORN_EL1** at EL1 using AArch64 to EL2.

Otherwise:

Reserved, RES0.
<table>
<thead>
<tr>
<th><strong>LORN_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>LORN_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>LORN_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**Bit [21]**

Reserved, RES0.

**LOREA_EL1, bit [20]**

When FEAT_LOR is implemented:

Trap MSR writes of **LOREA_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>LOREA_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>LOREA_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>LOREA_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**LORC_EL1, bit [19]**

When FEAT_LOR is implemented:

Trap MSR writes of **LORC_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>LORC_EL1</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>LORC_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes of <strong>LORC_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.
Bit [18]

Reserved, RES0.

**FAR_EL1, bit [17]**

Trap MSR writes of **FAR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>FAR_EL1</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>FAR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>FAR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**ESR_EL1, bit [16]**

Trap MSR writes of **ESR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>ESR_EL1</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>ESR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>ESR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bits [15:14]**

Reserved, RES0.

**CSSELR_EL1, bit [13]**

Trap MSR writes of **CSSELR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>CSSELR_EL1</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>CSSELR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>CSSELR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CPACR_EL1, bit [12]**

Trap MSR writes of **CPACR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th><strong>CPACR_EL1</strong></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>CPACR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3</strong>.FGTEn == 0b1, then MSR writes of <strong>CPACR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**CONTEXTIDR_EL1, bit [11]**

Trap MSR writes of **CONTEXTIDR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>CONTEXTIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>CONTEXTIDR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn</strong> == 0b1, then MSR writes of <strong>CONTEXTIDR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bits [10:9]**

Reserved, RES0.

**APIBKey, bit [8]**

When FEAT_PAuth is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APIBKeyHi_EL1**.
- **APIBKeyLo_EL1**.

<table>
<thead>
<tr>
<th>APIBKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn</strong> == 0b1, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**APIAKey, bit [7]**

When FEAT_PAuth is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APIAKeyHi_EL1**.
- **APIAKeyLo_EL1**.

Otherwise:

Reserved, RES0.
APIAKey, bit [6]

When FEAT_PAuth is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APGAKeyHi_EL1.**
- **APGAKeyLo_EL1.**

<table>
<thead>
<tr>
<th>APGAKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

APDBKey, bit [5]

When FEAT_PAuth is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APDBKeyHi_EL1.**
- **APDBKeyLo_EL1.**

<table>
<thead>
<tr>
<th>APDBKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or <strong>SCR_EL3.FGTEn == 0b1</strong>, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.
Otherwise:

Reserved, RES0.

**APDAKey, bit [4]**

When FEAT_PAuth is implemented:

Trap MSR writes of multiple System registers. Enables a trap on MSR writes at EL1 using AArch64 of any of the following AArch64 System registers to EL2:

- **APDAKeyHi_EL1**
- **APDAKeyLo_EL1**

<table>
<thead>
<tr>
<th>APDAKey</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of the System registers listed above are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes at EL1 using AArch64 of any of the System registers listed above are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Otherwise:

Reserved, RES0.

**AMAIR_EL1, bit [3]**

Trap MSR writes of **AMAIR_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>AMAIR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>AMAIR_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of <strong>AMAIR_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bit [2]**

Reserved, RES0.

**AFSR1_EL1, bit [1]**

Trap MSR writes of **AFSR1_EL1** at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>AFSR1_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of <strong>AFSR1_EL1</strong> are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of <strong>AFSR1_EL1</strong> at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.
AFSR0_EL1, bit [0]

Trap MSR writes of AFSR0_EL1 at EL1 using AArch64 to EL2.

<table>
<thead>
<tr>
<th>AFSR0_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSR writes of AFSR0_EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state and either EL3 is not implemented or SCR_EL3.FGTEn == 0b1, then MSR writes of AFSR0_EL1 at EL1 using AArch64 are trapped to EL2 and reported with EC syndrome value 0x18, unless the write generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Accessing the HFGWTR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, HFGWTR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elifs PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '1' then
    return NVMem[0x1c0];
elif EL2Enabled() && HCR_EL2.NV == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && HCR_EL2.<NV2,NV> == '1' then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FGTEn == '0' then
    UNDEFINED;
elif HaveEL(EL3) && SCR_EL3.FGTEn == '0' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
elif PSTATE.EL == EL3 then
    return HFGWTR_EL2;
elif PSTATE.EL == EL2 then
  return HFGWTR_EL2;

MSR HFGWTR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if \( \text{PSTATE.EL} = \text{EL0} \) then
UNDEFINED;
elsif \( \text{PSTATE.EL} = \text{EL1} \) then
  if \( \text{EL2Enabled()} \land \text{HCR.EL2.<NV2,NV>} = \text{'11'} \) then
    \( \text{NVMem[0x1C0]} = \text{X[t]} \);
  elsif \( \text{EL2Enabled()} \land \text{HCR.EL2.NV} = \text{'1'} \) then
    \( \text{AArch64.SystemAccessTrap(EL2, 0x18)} \);
  else
    UNDEFINED;
  endif
elsif \( \text{PSTATE.EL} = \text{EL2} \) then
  if \( \text{Halted()} \land \text{HaveEL(EL3)} \land \text{EDSCR.SDD} = \text{'1'} \land \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'"} \land \text{SCR.EL3.FGTEn} = \text{'0'} \) then
    UNDEFINED;
  elsif \( \text{HaveEL(EL3)} \land \text{SCR.EL3.FGTEn} = \text{'0'} \) then
    if \( \text{Halted()} \land \text{EDSCR.SDD} = \text{'1'} \) then
      UNDEFINED;
    else
      \( \text{AArch64.SystemAccessTrap(EL3, 0x18)} \);
    endif
  else
    \( \text{HFGWTR_EL2} = \text{X[t]} \);
  endif
elsif \( \text{PSTATE.EL} = \text{EL3} \) then
  \( \text{HFGWTR_EL2} = \text{X[t]} \);
HPFAR_EL2, Hypervisor IPA Fault Address Register

The HPFAR_EL2 characteristics are:

**Purpose**

Holds the faulting IPA for some aborts on a stage 2 translation taken to EL2.

**Configuration**

AArch64 System register HPFAR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HPFAR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

The HPFAR_EL2 is written for:

- Translation or Access faults in the second stage of translation.
- An abort in the second stage of translation performed during the translation table walk of a first stage translation, caused by a Translation fault, an Access flag fault, or a Permission fault.
- A stage 2 Address size fault.

For all other exceptions taken to EL2, this register is UNKNOWN.

**Note**

The address held in this register is an address accessed by the instruction fetch or data access that caused the exception that gave rise to the instruction or data abort. It is the lowest address that gave rise to the fault. Where different faults from different addresses arise from the same instruction, such as for an instruction that loads or stores a mis-aligned address that crosses a page boundary, the architecture does not prioritize between those different faults.

**Attributes**

HPFAR_EL2 is a 64-bit register.

**Field descriptions**

The HPFAR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NS |    | RES0 |    | FIPA |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Execution at EL1 or EL0 makes HPFAR_EL2 become UNKNOWN.

**NS, bit [63]**

When FEAT_SEL2 is implemented:

Faulting IPA address space.
Meaning

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Faulting IPA is from the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>Faulting IPA is from the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

For Data Aborts or Instruction Aborts taken to Non-secure EL2, this field is res0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, res0.

Bits [62:44]

Reserved, res0.

FIPA, bits [43:4]

### FIPA encoding when FEAT_LPA is implemented

<table>
<thead>
<tr>
<th>38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIPA</td>
</tr>
</tbody>
</table>

FIPA, bits [38:0]

Faulting Intermediate Physical Address.

When 52-bit addresses and a 64KB translation granule are in use for the stage 1 translation, HPFAR_EL2.FIPA[38:35] forms the upper part of the address value.

For implementations or stage 1 translation granules with fewer than 52 physical address bits the HPFAR_EL2.FIPA[38:35] is res0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

FIPA encoding when FEAT_LPA is not implemented

<table>
<thead>
<tr>
<th>38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>res0 FIPA</td>
</tr>
</tbody>
</table>

Bits [38:35]

Reserved, res0.

FIPA, bits [34:0]

Faulting Intermediate Physical Address.

For implementations with fewer than 48 physical address bits, the corresponding upper bits in this field are res0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [3:0]

Reserved, res0.
## Accessing the HPFAR_EL2

Accesses to this register use the following encodings:

### MRS <Xt>, HPFAR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        return HPFAR_EL2;
    elsif PSTATE.EL == EL3 then
        return HPFAR_EL2;
endif
```  

### MSR HPFAR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        HPFAR_EL2 = X[t];
    elsif PSTATE.EL == EL3 then
        HPFAR_EL2 = X[t];
endif
```
HSTR_EL2, Hypervisor System Trap Register

The HSTR_EL2 characteristics are:

**Purpose**

Controls trapping to EL2 of EL1 or lower AArch32 accesses to the System register in the coproc == 0b1111 encoding space, by the CRn value used to access the register using MCR or MRC instruction. When the register is accessible using an MCRR or MRRC instruction, this is the CRm value used to access the register.

**Configuration**

AArch64 System register HSTR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HSTR[31:0]. If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

HSTR_EL2 is a 64-bit register.

**Field descriptions**

The HSTR_EL2 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>T15</td>
<td>RES0</td>
<td>T13</td>
<td>T12</td>
<td>T11</td>
<td>T10</td>
<td>T9</td>
<td>T8</td>
<td>T7</td>
<td>T6</td>
<td>RES0</td>
<td>T3</td>
<td>T2</td>
<td>T1</td>
<td>T0</td>
<td></td>
<td></td>
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<td>27</td>
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<td>25</td>
<td>24</td>
<td>23</td>
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<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits [63:16, 14, 4]

Reserved, RES0.

\( T<n> \), bit [n], for n = 15, 13 to 5, 3 to 0

The remaining fields control whether EL0 and EL1 accesses, using MCR, MRC, MCRR, and MRRC instructions, to the System registers in the coproc == 0b1111 encoding space, are trapped to EL2 as follows:

- MCR or MRC accesses to these registers that are trapped to EL2 are reported using EC syndrome value 0x03, unless the access is UNDEFINED.
- MCRR or MRRC accesses to these registers that are trapped to EL2 are reported using EC syndrome value 0x04, unless the access is UNDEFINED.
### T<n>

<table>
<thead>
<tr>
<th>T&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on EL0 or EL1 accesses to System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>System registers in the coproc == 0b1111 encoding space and CRn == &lt;n&gt; or CRm == &lt;n&gt; where T&lt;n&gt; is the name of this field, are trapped as follows:</td>
</tr>
<tr>
<td></td>
<td>• An EL1 MCR or MRC access is trapped to EL2.</td>
</tr>
<tr>
<td></td>
<td>• An EL0 MCR or MRC access is trapped to EL2, if the access is not UNDEFINED when the value of this field is 0.</td>
</tr>
<tr>
<td></td>
<td>• An EL1 MCRR or MRRC access is trapped to EL2.</td>
</tr>
<tr>
<td></td>
<td>• An EL0 MCRR or MRRC access is trapped to EL2, if the access is not UNDEFINED when the value of this field is 0.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether an EL0 access using AArch32 is trapped to EL2, or is UNDEFINED. If the access is UNDEFINED, and generates an exception that is taken to EL1 or EL2 using AArch64, this is reported with EC syndrome value 0x00.

#### Note

Arm expects that trapping to EL2 of EL0 accesses to these registers is unusual and used only when the hypervisor must virtualize EL0 operation. Arm recommends that, whenever possible, EL0 accesses to these registers behave as they would if the implementation did not include EL2. This means that, if the architecture does not support the EL0 access, then the register access instruction is treated as UNDEFINED and generates an exception that is taken to EL1.

For example, when HSTR_EL2.T7 is 1, for instructions executed at EL1:

- An MCR or MRC instruction with coproc set to 0b1111 and <CRn> set to c7 is trapped to EL2.
- An MCRR or MRRC instruction with coproc set to 0b1111 and <CRm> set to c7 is trapped to EL2.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Otherwise:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>RES0</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

#### Bits [63:0]

Reserved, RES0.

### Accessing the HSTR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, HSTR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x080];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  return HSTR_EL2;
elsif PSTATE.EL == EL3 then
  return HSTR_EL2;
endif

MSR HSTR_EL2, <Xt>

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x080] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  HSTR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  HSTR_EL2 = X[t];
endif
IC IALLU, Instruction Cache Invalidate All to PoU

The IC IALLU characteristics are:

**Purpose**

Invalidate all instruction caches to Point of Unification.

**Configuration**

AArch64 System instruction IC IALLU performs the same function as AArch32 System instruction ICIALLU.

**Attributes**

IC IALLU is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the IC IALLU instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

IC IALLU{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TOCU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ICIALLU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        IC_IALLUIS();
    else
        IC_IALLU();
    endif
elsif PSTATE.EL == EL2 then
    IC_IALLU();
elsif PSTATE.EL == EL3 then
    IC_IALLU();
else
    IC_IALLU();
```

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The IC IALLUIS characteristics are:

**Purpose**

Invalidate all instruction caches in Inner Shareable domain to Point of Unification.

**Configuration**

AArch64 System instruction IC IALLUIS performs the same function as AArch32 System instruction ICIALLUIS.

**Attributes**

IC IALLUIS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the IC IALLUIS instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

```
IC IALLUIS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.TPU == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && HCR_EL2.TICAB == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ICIALLUIS == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      IC_IALLUIS();
   endif
elsif PSTATE.EL == EL2 then
   IC_IALLUIS();
elsif PSTATE.EL == EL3 then
   IC_IALLUIS();
```
IC IVAU, Instruction Cache line Invalidate by VA to PoU

The IC IVAU characteristics are:

Purpose

Invalidate instruction cache by address to Point of Unification.

Configuration

AArch64 System instruction IC IVAU performs the same function as AArch32 System instruction ICIMVAU.

Attributes

IC IVAU is a 64-bit System instruction.

Field descriptions

The IC IVAU input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Virtual address to use</th>
<th>Virtual address to use</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:0]

Virtual address to use. No alignment restrictions apply to this VA.

Executing the IC IVAU instruction

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'The instruction cache maintenance instruction (IC)'.

If EL0 access is enabled, when executed at EL0, this instruction requires read access permission to the VA, otherwise it is IMPLEMENTATION DEFINED whether it generates a Permission Fault, see 'Permission fault'.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>IC IVAU{, &lt;Xt&gt;}</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b01</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TPU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TOCU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
        HFGITR_EL2.ICIVAU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.UCI == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        IC_IVAU(X[t]);
    end;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TPU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TOCU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.ICIVAU == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        IC_IVAU(X[t]);
    end;
elsif PSTATE.EL == EL2 then
    IC_IVAU(X[t]);
elsif PSTATE.EL == EL3 then
    IC_IVAU(X[t]);
ICC_AP0R<n>_EL1, Interrupt Controller Active Priorities Group 0 Registers, n = 0 - 3

The ICC_AP0R<n>_EL1 characteristics are:

**Purpose**

Provides information about Group 0 active priorities.

**Configuration**

AArch64 System register ICC_AP0R<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICC_AP0R<n>[31:0].

**Attributes**

ICC_AP0R<n>_EL1 is a 64-bit register.

**Field descriptions**

The ICC_AP0R<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
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<tr>
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<td>33</td>
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<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICC_AP0R<n>_EL1**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 0 active priorities) might result in UNPREDICTABLE behavior of the interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICC_AP0R1_EL1 is only implemented in implementations that support 6 or more bits of priority. ICC_AP0R2_EL1 and ICC_AP0R3_EL1 are only implemented in implementations that support 7 or more bits of priority. Unimplemented registers are UNDEFINED.

**Note**

The number of bits of preemption is indicated by ICH_VTR_EL2.PREbits.
Writing to the active priority registers in any order other than the following order will result in UNPREDICTABLE behavior:

- ICC_AP0R<n>_EL1.
- Secure ICC_AP1R<n>_EL1.
- Non-secure ICC_AP1R<n>_EL1.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_AP0R<n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICV_AP0R_EL1[UInt(op2<1:0>)];
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end
endif

MSR ICC_AP0R<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elseif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  else
    ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
else
  ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
else
  ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
ICC_AP1R<n>_EL1, Interrupt Controller Active Priorities Group 1 Registers, n = 0 - 3

The ICC_AP1R<n>_EL1 characteristics are:

**Purpose**

Provides information about Group 1 active priorities.

**Configuration**

AArch64 System register ICC_AP1R<n>_EL1 bits [31:0] (S) are architecturally mapped to AArch32 System register ICC_AP1R<n>[31:0] (S).

AArch64 System register ICC_AP1R<n>_EL1 bits [31:0] (NS) are architecturally mapped to AArch32 System register ICC_AP1R<n>[31:0] (NS).

**Attributes**

ICC_AP1R<n>_EL1 is a 64-bit register.

**Field descriptions**

The ICC_AP1R<n>_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |    |

**Bits [63:32]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICC_AP1R<n>_EL1**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 1 active priorities) might result in UNPREDICTABLE behavior of the interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICC_AP1R1_EL1 is only implemented in implementations that support 6 or more bits of priority. ICC_AP1R2_EL1 and ICC_AP1R3_EL1 are only implemented in implementations that support 7 or more bits of priority. Unimplemented registers are UNDEFINED.

**Note**
The number of bits of preemption is indicated by \texttt{ICH\_VTR\_EL2\_PREbits}.

Writing to the active priority registers in any order other than the following order will result in \texttt{UNPREDICTABLE} behavior:

- \texttt{ICC\_AP0R<n>\_EL1}.
- Secure \texttt{ICC\_AP1R<n>\_EL1}.
- Non-secure \texttt{ICC\_AP1R<n>\_EL1}.

Accesses to this register use the following encodings:

\texttt{MRS <Xt>, ICC\_AP1R<n>\_EL1}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

\texttt{ICC\_AP1R<n>\_EL1, Interrupt Controller Active Priorities Group 1 Registers, n = 0 - 3}
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif SCR_EL3.NS == '0' then
    return ICC_AP1R_EL1_S[UInt(op2<1:0>)];
  else
    return ICC_AP1R_EL1_NS[UInt(op2<1:0>)];
else
  return ICC_AP1R_EL1[UInt(op2<1:0>)];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif SCR_EL3.NS == '0' then
    return ICC_AP1R_EL1_S[UInt(op2<1:0>)];
  else
    return ICC_AP1R_EL1_NS[UInt(op2<1:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  elseif SCR_EL3.NS == '0' then
    return ICC_AP1R_EL1_S[UInt(op2<1:0>)];
  else
    return ICC_AP1R_EL1_NS[UInt(op2<1:0>)];
else
  return ICC_AP1R_EL1[UInt(op2<1:0>)];

MSR ICC_AP1R<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if SCR_EL3.NS == '0' then
      ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
    else
      ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
    else
      ICC_AP1R_EL1[UInt(op2<1:0>)] = X[t];
  else
    if SCR_EL3.NS == '0' then
      ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
    else
      ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
else
  if SCR_EL3.NS == '0' then
    ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
  else
    ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
ICC_ASGI1R_EL1, Interrupt Controller Alias Software Generated Interrupt Group 1 Register

The ICC_ASGI1R_EL1 characteristics are:

**Purpose**

Generates Group 1 SGIs for the Security state that is not the current Security state.

**Configuration**

AArch64 System register ICC_ASGI1R_EL1 performs the same function as AArch32 System register ICC_ASGI1R.

Under certain conditions a write to ICC_ASGI1R_EL1 can generate Group 0 interrupts, see 'Forwarding an SGI to a target PE' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_ASGI1R_EL1 is a 64-bit register.

**Field descriptions**

The ICC_ASGI1R_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Aff3</td>
</tr>
<tr>
<td>61</td>
<td>RS</td>
</tr>
<tr>
<td>60</td>
<td>RES0</td>
</tr>
<tr>
<td>59</td>
<td>Aff1</td>
</tr>
<tr>
<td>58</td>
<td>TargetList</td>
</tr>
<tr>
<td>57</td>
<td>INTID</td>
</tr>
<tr>
<td>56</td>
<td>Aff2</td>
</tr>
<tr>
<td>55</td>
<td>Res0</td>
</tr>
<tr>
<td>54</td>
<td>INTID</td>
</tr>
<tr>
<td>53</td>
<td>Aff1</td>
</tr>
<tr>
<td>52</td>
<td>RS</td>
</tr>
<tr>
<td>51</td>
<td>RES0</td>
</tr>
<tr>
<td>50</td>
<td>Aff2</td>
</tr>
<tr>
<td>49</td>
<td>Res0</td>
</tr>
<tr>
<td>48</td>
<td>INTID</td>
</tr>
<tr>
<td>47</td>
<td>Aff1</td>
</tr>
<tr>
<td>46</td>
<td>RS</td>
</tr>
<tr>
<td>45</td>
<td>RES0</td>
</tr>
<tr>
<td>44</td>
<td>Aff2</td>
</tr>
<tr>
<td>43</td>
<td>Res0</td>
</tr>
<tr>
<td>42</td>
<td>INTID</td>
</tr>
<tr>
<td>41</td>
<td>Aff1</td>
</tr>
<tr>
<td>40</td>
<td>RS</td>
</tr>
<tr>
<td>39</td>
<td>RES0</td>
</tr>
<tr>
<td>38</td>
<td>Aff2</td>
</tr>
<tr>
<td>37</td>
<td>Res0</td>
</tr>
<tr>
<td>36</td>
<td>INTID</td>
</tr>
<tr>
<td>35</td>
<td>Aff1</td>
</tr>
<tr>
<td>34</td>
<td>RS</td>
</tr>
<tr>
<td>33</td>
<td>RES0</td>
</tr>
<tr>
<td>32</td>
<td>Aff2</td>
</tr>
</tbody>
</table>

**Bits [63:56]**

Reserved, RES0.

**Aff3, bits [55:48]**

The affinity 3 value of the affinity path of the luster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**

RangeSelector

Controls which group of 16 values is represented by the TargetList field.

TargetList[n] represents aff0 value ((RS * 16) + n).

When ICC_CTLR_EL1.RSS==0, RS is RES0.

When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a constrained unpredictable choice of:

- The write is ignored.
- The RS field is treated as 0.
**Bits [43:41]**

Reserved, RES0.

**IRM, bit [40]**

Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1. &lt;target list&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding &quot;self&quot;.</td>
</tr>
</tbody>
</table>

**Aff2, bits [39:32]**

The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**Bits [31:28]**

Reserved, RES0.

**INTID, bits [27:24]**

The INTID of the SGI.

**Aff1, bits [23:16]**

The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**TargetList, bits [15:0]**

Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.

If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is IMPLEMENTATION DEFINED whether, in such cases, a Distributor can signal a system error.

**Note**

This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16. If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs. Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.

If the IRM bit is 1, this field is RES0.

**Accessing the ICC_ASGI1R_EL1**

This register allows software executing in a Secure state to generate Non-secure Group 1 SGIs. It will also allow software executing in a Non-secure state to generate Secure Group 1 SGIs, if permitted by the settings of GICR_NSACR in the Redistributor corresponding to the target PE.
When `GICD_CTLR.DS==0`, Non-secure writes do not generate an interrupt for a target PE if not permitted by the `GICR_NSACR` register associated with the target PE. For more information, see 'Use of control registers for SGI forwarding'.

---

**Note**

Accesses at EL3 are treated as Secure regardless of the value of `SCR_EL3.NS`.

---

Accesses to this register use the following encodings:

MSR `ICC_ASGI1R_EL1`, `<Xt>`

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if `PSTATE.EL == EL0` then

**UNDEFINED**;

elsif `PSTATE.EL == EL1` then

if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.<IRQ,FIQ> == '11' then

**UNDEFINED**;

elsif ICC_SRE_EL1.SRE == '0' then

AArch64.SystemAccessTrap(EL1, 0x18);

elsif EL2Enabled() & HCR_EL2.TC == '1' then

AArch64.SystemAccessTrap(EL2, 0x18);

elsif EL2Enabled() & HCR_EL2.FM0 == '1' then

AArch64.SystemAccessTrap(EL2, 0x18);

elsif EL2Enabled() & HCR_EL2.IM0 == '1' then

AArch64.SystemAccessTrap(EL2, 0x18);

elsif HaveEL(EL3) & SCR_EL3.<IRQ,FIQ> == '11' then

if Halted() & EDSCR.SDD == '1' then

**UNDEFINED**;

else

AArch64.SystemAccessTrap(EL3, 0x18);

else

ICC_ASGI1R_EL1 = X[t];

elsif `PSTATE.EL == EL2` then

if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.<IRQ,FIQ> == '11' then

**UNDEFINED**;

elsif ICC_SRE_EL2.SRE == '0' then

AArch64.SystemAccessTrap(EL2, 0x18);

elsif HaveEL(EL3) & SCR_EL3.<IRQ,FIQ> == '11' then

if Halted() & EDSCR.SDD == '1' then

**UNDEFINED**;

else

AArch64.SystemAccessTrap(EL3, 0x18);

else

ICC_ASGI1R_EL1 = X[t];

elsif `PSTATE.EL == EL3` then

if ICC_SRE_EL3.SRE == '0' then

AArch64.SystemAccessTrap(EL3, 0x18);

else

ICC_ASGI1R_EL1 = X[t];
The ICC_BPR0_EL1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 0 interrupt preemption.

**Configuration**

AArch64 System register ICC_BPR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICC_BPR0[31:0].

Virtual accesses to this register update ICH_VMCR_EL2.VBPR0.

**Attributes**

ICC_BPR0_EL1 is a 64-bit register.

**Field descriptions**

The ICC_BPR0_EL1 bit assignments are:

| Bits [63:3] | Reserved, RES0. |
| BinaryPoint, bits [2:0] |

The value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>[7:1]</td>
<td>[0]</td>
<td>ggggggg.s</td>
</tr>
<tr>
<td>1</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>2</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>3</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>gggg.ss</td>
</tr>
<tr>
<td>4</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sss</td>
</tr>
<tr>
<td>5</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>gs.sssss</td>
</tr>
<tr>
<td>6</td>
<td>[7]</td>
<td>[6:0]</td>
<td>ssssssss</td>
</tr>
<tr>
<td>7</td>
<td>No preemption</td>
<td>[7:0]</td>
<td>.ssssssss</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICC_BPR0_EL1**

The minimum binary point value is derived from the number of implemented priority bits. The number of priority bits is IMPLEMENTATION DEFINED, and reported by ICC_CTLR_EL1.PRIbits and ICC_CTLR_EL3.PRIbits.
An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is UNKNOWN.

Accesses to this register use the following encodings:

**MRS <Xt>, ICC_BPR0_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsi
  if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
      UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
      AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
      return ICV_BPR0_EL1;
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    elsif PSTATE.EL == EL2 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
      elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.SystemAccessTrap(EL3, 0x18);
        end
      end
    elsif PSTATE.EL == EL3 then
      if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        return ICC_BPR0_EL1;
      end
    end
  else
    return ICC_BPR0_EL1;
end

**MSR ICC_BPR0_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        ICC_BPR0_EL1 = X[t];
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ICC_BPR0_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ICC_BPR0_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        ICC_BPR0_EL1 = X[t];
    end
The ICC_BPR1_EL1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption.

**Configuration**

AArch64 System register ICC_BPR1_EL1 bits [31:0] (S) are architecturally mapped to AArch32 System register ICC_BPR1[31:0] (S).

AArch64 System register ICC_BPR1_EL1 bits [31:0] (NS) are architecturally mapped to AArch32 System register ICC_BPR1[31:0] (NS).

Virtual accesses to this register update ICH_VMCR_EL2.VBPR1.

**Attributes**

ICC_BPR1_EL1 is a 64-bit register.

**Field descriptions**

The ICC_BPR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RESO | RESO | BinaryPoint |

**Bits [63:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

If the GIC is configured to use separate binary point fields for Group 0 and Group 1 interrupts, the value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. For more information about priorities, see 'Priority grouping' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

The minimum value of the Non-secure copy of this register is the minimum value of ICC_BPR0_EL1 + 1. The minimum value of the Secure copy of this register is the minimum value of ICC_BPR0_EL1.

If EL3 is implemented and ICC_CTLR_EL3.CBPR_EL1S is 1:

- When SCR_EL3.EEL2 is 1 and HCR_EL2.IMO is 1, Secure accesses to this register at EL1 access the state of ICV_BPR1_EL1.
- Otherwise, Secure accesses to this register at EL1 access the state of ICC_BPR0_EL1.

If EL3 is implemented and ICC_CTLR_EL3.CBPR_EL1NS is 1, Non-secure accesses to this register at EL1 or EL2 behave as follows, depending on the values of HCR_EL2.IMO and SCR_EL3.IRQ.
If EL3 is not implemented and ICC_CTLR_EL1.CBPR is 1, Non-secure accesses to this register at EL1 or EL2 behave as follows, depending on the values of HCR_EL2.IMO:

If EL3 is not implemented and ICC_CTLR_EL1.CBPR is 1, Non-secure accesses to this register at EL1 or EL2 behave as follows, depending on the values of HCR_EL2.IMO:

<table>
<thead>
<tr>
<th>HCR_EL2.IMO</th>
<th>SCR_EL3.IRQ</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>Non-secure EL1 and EL2 reads return ICC_BPR0_EL1 + 1 saturated to 0b111. Non-secure EL1 and EL2 writes are ignored.</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>Non-secure EL1 and EL2 accesses trap to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>Non-secure EL1 accesses affect virtual interrupts. Non-secure EL2 reads return ICC_BPR0_EL1 + 1 saturated to 0b111. Non-secure EL2 writes are ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>Non-secure EL1 accesses affect virtual interrupts. Non-secure EL2 accesses trap to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICC_BPR1_EL1**

On a reset, the binary point field is UNKNOWN.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value.

Accesses to this register use the following encodings:

```
MRS <Xt>, ICC_BPR1_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if SCR_EL3.NS == '0' then
            return ICC_BPR1_EL1_S;
        else
            return ICC_BPR1_EL1_NS;
        end if
    end if
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        if SCR_EL3.NS == '0' then
            return ICC_BPR1_EL1_S;
        else
            return ICC_BPR1_EL1_NS;
        end if
    end if
else
    return ICC_BPR1_EL1;
end if

MSR ICC_BPR1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        ICC_BPR1_EL1 = X[t];
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif SCR_EL3.NS == '0' then
        ICC_BPR1_EL1_S = X[t];
    else
        ICC_BPR1_EL1_NS = X[t];
    end if;
elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    if SCR_EL3.NS == '0' then
        ICC_BPR1_EL1_S = X[t];
    else
        ICC_BPR1_EL1_NS = X[t];
    end if;
else
    ICC_BPR1_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
else
    if SCR_EL3.NS == '0' then
        ICC_BPR1_EL1_S = X[t];
    else
        ICC_BPR1_EL1_NS = X[t];
    end if;
else
    ICC_BPR1_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
else
    if SCR_EL3.NS == '0' then
        ICC_BPR1_EL1_S = X[t];
    else
        ICC_BPR1_EL1_NS = X[t];
**ICC_CTLR_EL1, Interrupt Controller Control Register (EL1)**

The ICC_CTLR_EL1 characteristics are:

**Purpose**

Controls aspects of the behavior of the GIC CPU interface and provides information about the features implemented.

**Configuration**

AArch64 System register ICC_CTLR_EL1 bits [31:0] (S) are architecturally mapped to AArch32 System register ICC_CTLR[31:0] (S).

AArch64 System register ICC_CTLR_EL1 bits [31:0] (NS) are architecturally mapped to AArch32 System register ICC_CTLR[31:0] (NS).

**Attributes**

ICC_CTLR_EL1 is a 64-bit register.

**Field descriptions**

The ICC_CTLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>ExtRange, bit [19].</td>
</tr>
<tr>
<td>61</td>
<td>EXTRange, bit [19].</td>
</tr>
<tr>
<td>60</td>
<td>RSS.</td>
</tr>
<tr>
<td>59</td>
<td>RES0.</td>
</tr>
<tr>
<td>58</td>
<td>A3V.</td>
</tr>
<tr>
<td>57</td>
<td>SEIS.</td>
</tr>
<tr>
<td>56</td>
<td>IDbits.</td>
</tr>
<tr>
<td>55</td>
<td>PRIbits.</td>
</tr>
<tr>
<td>54</td>
<td>RES0.</td>
</tr>
<tr>
<td>53</td>
<td>PMHE.</td>
</tr>
<tr>
<td>52</td>
<td>RES0.</td>
</tr>
<tr>
<td>51</td>
<td>EOImode.</td>
</tr>
<tr>
<td>50</td>
<td>CBPR.</td>
</tr>
</tbody>
</table>

**Bits [63:20]**

Reserved, RES0.

**ExtRange, bit [19]**

Extended INTID range (read-only).

<table>
<thead>
<tr>
<th>ExtRange</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0      | CPU interface does not support INTIDs in the range 1024..8191.  
  - Behaviour is **UNPREDICTABLE** if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface. |
| 0b1      | CPU interface supports INTIDs in the range 1024..8191  
  - All INTIDs in the range 1024..8191 are treated as requiring deactivation. |

**Note**

Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them.

If EL3 is implemented, ICC_CTLR_EL1.ExtRange is an alias of ICC_CTLR_EL3.ExtRange.
RSS, bit [18]

Range Selector Support. Possible values are:

<table>
<thead>
<tr>
<th>RSS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 15 are supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 255 are supported.</td>
</tr>
</tbody>
</table>

This bit is read-only.

Bits [17:16]

Reserved, RES0.

A3V, bit [15]

Affinity 3 Valid. Read-only and writes are ignored. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

If EL3 is implemented, this bit is an alias of ICC_CTLR_EL3.A3V.

SEIS, bit [14]

SEI Support. Read-only and writes are ignored. Indicates whether the CPU interface supports local generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support local generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports local generation of SEIs.</td>
</tr>
</tbody>
</table>

If EL3 is implemented, this bit is an alias of ICC_CTLR_EL3.SEIS.

IDbits, bits [13:11]

Identifier bits. Read-only and writes are ignored. The number of physical interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If EL3 is implemented, this field is an alias of ICC_CTLR_EL3.IDbits.

PRIbits, bits [10:8]

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one.

An implementation that supports two Security states must implement at least 32 levels of physical priority (5 priority bits).

An implementation that supports only a single Security state must implement at least 16 levels of physical priority (4 priority bits).

Note

This field always returns the number of priority bits implemented, regardless of the Security state of the access or the value of GICD_CTLR.DS.
For physical accesses, this field determines the minimum value of ICC_BPR0_EL1.

If EL3 is implemented, physical accesses return the value from ICC_CTLR_EL3.PRIbits.

If EL3 is not implemented, physical accesses return the value from this field.

**Bit [7]**

Reserved, RES0.

**PMHE, bit [6]**

Priority Mask Hint Enable. Controls whether the priority mask register is used as a hint for interrupt distribution:

<table>
<thead>
<tr>
<th>PMHE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables use of ICC_PMR_EL1 as a hint for interrupt distribution.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables use of ICC_PMR_EL1 as a hint for interrupt distribution.</td>
</tr>
</tbody>
</table>

If EL3 is implemented, this bit is an alias of ICC_CTLR_EL3.PMHE. Whether this bit can be written as part of an access to this register depends on the value of GICD_CTLR.DS:

- If GICD_CTLR.DS == 0, this bit is read-only.
- If GICD_CTLR.DS == 1, this bit is read/write.

If EL3 is not implemented, it is IMPLEMENTATION DEFINED whether this bit is read-only or read-write:

- If this bit is read-only, an implementation can choose to make this field RAZ/WI or RAO/WI.
- If this bit is read/write, it resets to zero.

**Bits [5:2]**

Reserved, RES0.

**EOImode, bit [1]**

EOI mode for the current Security state. Controls whether a write to an End of Interrupt register also deactivates the interrupt:

<table>
<thead>
<tr>
<th>EOImode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR_EL1 are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide priority drop functionality only. ICC_DIR_EL1 provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

The Secure ICC_CTLR_EL1.EOImode is an alias of ICC_CTLR_EL3.EOImode_EL1S.

The Non-secure ICC_CTLR_EL1.EOImode is an alias of ICC_CTLR_EL3.EOImode_EL1NS.

**CBPR, bit [0]**

Common Binary Point Register. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_BPR0_EL1 determines the preemption group for Group 0 interrupts only. ICC_BPR1_EL1 determines the preemption group for Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_BPR0_EL1 determines the preemption group for both Group 0 and Group 1 interrupts.</td>
</tr>
</tbody>
</table>
If EL3 is implemented:

- This bit is an alias of ICC_CTLR_EL3.CBPR_EL1\{S,NS\} where S or NS corresponds to the current Security state.
- If GICD_CTLR.DS == 0, this bit is read-only.
- If GICD_CTLR.DS == 1, this bit is read/write.

If EL3 is not implemented, this bit is read/write.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICC_CTLR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_CTLR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end
elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    if SCR_EL3.NS == '0' then
        return ICC_CTLR_EL1_S;
    else
        return ICC_CTLR_EL1_NS;
    end
elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
    if SCR_EL3.NS == '0' then
        return ICC_CTLR_EL1_S;
    else
        return ICC_CTLR_EL1_NS;
end

MSR ICC_CTLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
      UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
      AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
      ICV_CTLR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
      ICV_CTLR_EL1 = X[t];
    elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    elsif HaveEL(EL3) then
      if SCR_EL3.NS == '0' then
        ICC_CTLR_EL1_S = X[t];
      else
        ICC_CTLR_EL1_NS = X[t];
      end if
    else
      ICC_CTLR_EL1 = X[t];
  end if
else
  ICC_CTLR_EL1 = X[t];
end if
The ICC_CTLR_EL3 characteristics are:

## Purpose

Controls aspects of the behavior of the GIC CPU interface and provides information about the features implemented.

## Configuration

AArch64 System register ICC_CTLR_EL3 bits [31:0] can be mapped to AArch32 System register ICC_MCTLR[31:0], but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to ICC_CTLR_EL3 are undefined.

## Attributes

ICC_CTLR_EL3 is a 64-bit register.

## Field descriptions

The ICC_CTLR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:20</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31:20</td>
<td><strong>ExtRange</strong> bit [19]</td>
</tr>
<tr>
<td></td>
<td>Extended INTID range (read-only).</td>
</tr>
</tbody>
</table>

**ExtRange**

<table>
<thead>
<tr>
<th>ExtRange</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CPU interface does not support INTIDs in the range 1024..8191.</td>
</tr>
<tr>
<td></td>
<td>• Behaviour is <strong>UNPREDICTABLE</strong> if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface.</td>
</tr>
<tr>
<td></td>
<td><strong>Note</strong></td>
</tr>
<tr>
<td></td>
<td>Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them.</td>
</tr>
<tr>
<td>0b1</td>
<td>CPU interface supports INTIDs in the range 1024..8191.</td>
</tr>
<tr>
<td></td>
<td>• All INTIDs in the range 1024..8191 are treated as requiring deactivation.</td>
</tr>
</tbody>
</table>

**RSS**, bit [18]

Range Selector Support.
Targeted SGIs with affinity level 0 values of 0-15 are supported.

Targeted SGIs with affinity level 0 values of 0-255 are supported.

This bit is read-only.

**nDS, bit [17]**

Disable Security not supported. Read-only and writes are ignored.

<table>
<thead>
<tr>
<th>nDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic supports disabling of security.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic does not support disabling of security, and requires that security is not disabled.</td>
</tr>
</tbody>
</table>

**Bit [16]**

Reserved, RES0.

**A3V, bit [15]**

Affinity 3 Valid. Read-only and writes are ignored.

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support non-zero values of the Aff3 field in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports non-zero values of the Aff3 field in SGI generation System registers.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR_EL1.A3V is an alias of ICC_CTLR_EL3.A3V

**SEIS, bit [14]**

SEI Support. Read-only and writes are ignored. Indicates whether the CPU interface supports generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports generation of SEIs.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR_EL1.SEIS is an alias of ICC_CTLR_EL3.SEIS

**IDbits, bits [13:11]**

Identifier bits. Read-only and writes are ignored. Indicates the number of physical interrupt identifier bits supported.

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b01</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If EL3 is present, ICC_CTLR_EL1.IDbits is an alias of ICC_CTLR_EL3.IDbits

**PRIbits, bits [10:8]**

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one.

An implementation that supports two Security states must implement at least 32 levels of physical priority (5 priority bits).

An implementation that supports only a single Security state must implement at least 16 levels of physical priority (4 priority bits).
Note

This field always returns the number of priority bits implemented, regardless of the value of SCR_EL3.NS or the value of GICD_CTLR.DS.

The division between group priority and subpriority is defined in the binary point registers ICC_BPR0_EL1 and ICC_BPR1_EL1.

This field determines the minimum value of ICC_BPR0_EL1.

Bit [7]

Reserved, RES0.

PMHE, bit [6]

Priority Mask Hint Enable.

<table>
<thead>
<tr>
<th>PMHE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables use of the priority mask register as a hint for interrupt distribution.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables use of the priority mask register as a hint for interrupt distribution.</td>
</tr>
</tbody>
</table>

Software must write ICC_PMR_EL1 to 0xFF before clearing this field to 0.

- An implementation might choose to make this field RAO/WI if priority-based routing is always used
- An implementation might choose to make this field RAZ/WI if priority-based routing is never used

If EL3 is present, ICC_CTLR_EL1.PMHE is an alias of ICC_CTLR_EL3.PMHE.

On a Warm reset, this field resets to 0.

RM, bit [5]

Routing Modifier. For legacy operation of EL1 software with GICC_CTLR.FIQEn set to 1, this bit indicates whether interrupts can be acknowledged or observed as the Highest Priority Pending Interrupt, or whether a special INTID value is returned.

Possible values of this bit are:

<table>
<thead>
<tr>
<th>RM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure Group 0 and Non-secure Group 1 interrupts can be acknowledged and observed as the highest priority interrupt at the Secure Exception level where the interrupt is taken.</td>
</tr>
<tr>
<td>0b1</td>
<td>When accessed at EL3 in AArch64 state:</td>
</tr>
<tr>
<td></td>
<td>• Secure Group 0 interrupts return a special INTID value of 1020. This affects accesses to ICC_IAR0_EL1 and ICC_HPP1R0_EL1.</td>
</tr>
<tr>
<td></td>
<td>• Non-secure Group 1 interrupts return a special INTID value of 1021. This affects accesses to ICC_IAR1_EL1 and ICC_HPP1R1_EL1.</td>
</tr>
</tbody>
</table>

Note

The Routing Modifier bit is supported in AArch64 only. In systems without EL3 the behavior is as if the value is 0. Software must ensure this bit is 0 when the Secure copy of ICC_SRE_EL1.SRE is 1, otherwise system behavior is UNPREDICTABLE. In systems without EL3 or where the Secure copy of ICC_SRE_EL1.SRE is RAO/WI, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
EOImode_EL1NS, bit [4]

EOI mode for interrupts handled at Non-secure EL1 and EL2. Controls whether a write to an End of Interrupt register also deactivates the interrupt.

<table>
<thead>
<tr>
<th>EOImode_EL1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR_EL1 are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide priority drop functionality only. ICC_DIR_EL1 provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR_EL1(NS).EOImode is an alias of ICC_CTLR_EL3.EOImode_EL1NS.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EOImode_EL1S, bit [3]

EOI mode for interrupts handled at Secure EL1 and EL2. Controls whether a write to an End of Interrupt register also deactivates the interrupt.

<table>
<thead>
<tr>
<th>EOImode_EL1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR_EL1 are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide priority drop functionality only. ICC_DIR_EL1 provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR_EL1(S).EOImode is an alias of ICC_CTLR_EL3.EOImode_EL1S.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EOImode_EL3, bit [2]

EOI mode for interrupts handled at EL3. Controls whether a write to an End of Interrupt register also deactivates the interrupt.

<table>
<thead>
<tr>
<th>EOImode_EL3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR_EL1 are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide priority drop functionality only. ICC_DIR_EL1 provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CBPR_EL1NS, bit [1]

Common Binary Point Register, EL1 Non-secure. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 Non-secure interrupts at EL1 and EL2.

<table>
<thead>
<tr>
<th>CBPR_EL1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_BPR0_EL1 determines the preemption group for Group 0 interrupts only. ICC_BPR1_EL1 determines the preemption group for Non-secure Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_BPR0_EL1 determines the preemption group for Group 0 interrupts and Non-secure Group 1 interrupts. Non-secure accesses to GICC_BPR and ICC_BPR1_EL1 access the state of ICC_BPR0_EL1.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR_EL1(NS).CBPR is an alias of ICC_CTLR_EL3.CBPR_EL1NS.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### CBPR_EL1S, bit [0]

Common Binary Point Register, EL1 Secure. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 Secure interrupts at EL1 and EL2.

<table>
<thead>
<tr>
<th>CBPR_EL1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>ICC_BPR0_EL1</strong> determines the preemption group for Group 0 interrupts only.</td>
</tr>
<tr>
<td></td>
<td><strong>ICC_BPR1_EL1</strong> determines the preemption group for Secure Group 1 interrupts.</td>
</tr>
</tbody>
</table>
| 0b1       | **ICC_BPR0_EL1** determines the preemption group for Group 0 interrupts and Secure Group 1 interrupts.  
|           | Secure EL1 accesses to **ICC_BPR1_EL1** access the state of **ICC_BPR0_EL1**. |

If EL3 is present, **ICC_CTLR_EL1(S).CBPR** is an alias of **ICC_CTLR_EL3.CBPR_EL1S**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the ICC_CTLR_EL3

Accesses to this register use the following encodings:

**MRS <Xt>, ICC_CTLR_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_CTLR_EL3;

**MSR ICC_CTLR_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_CTLR_EL3 = X[t];
The ICC_DIR_EL1 characteristics are:

**Purpose**

When interrupt priority drop is separated from interrupt deactivation, a write to this register deactivates the specified interrupt.

**Configuration**

AArch64 System register ICC_DIR_EL1 performs the same function as AArch32 System register ICC_DIR.

**Attributes**

ICC_DIR_EL1 is a 64-bit register.

**Field descriptions**

The ICC_DIR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit 63</th>
<th>Bit 62</th>
<th>Bit 61</th>
<th>Bit 60</th>
<th>Bit 59</th>
<th>Bit 58</th>
<th>Bit 57</th>
<th>Bit 56</th>
<th>Bit 55</th>
<th>Bit 54</th>
<th>Bit 53</th>
<th>Bit 52</th>
<th>Bit 51</th>
<th>Bit 50</th>
<th>Bit 49</th>
<th>Bit 48</th>
<th>Bit 47</th>
<th>Bit 46</th>
<th>Bit 45</th>
<th>Bit 44</th>
<th>Bit 43</th>
<th>Bit 42</th>
<th>Bit 41</th>
<th>Bit 40</th>
<th>Bit 39</th>
<th>Bit 38</th>
<th>Bit 37</th>
<th>Bit 36</th>
<th>Bit 35</th>
<th>Bit 34</th>
<th>Bit 33</th>
<th>Bit 32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
</tr>
</tbody>
</table>

RES0

INTID, bits [23:0]

The INTID of the interrupt to be deactivated.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_DIR_EL1**

There are two cases when writing to ICC_DIR_EL1 that were UNPREDICTABLE for a corresponding GICv2 write to GICC_DIR:

- When EOImode == 0. GICv3 implementations must ignore such writes. In systems supporting system error generation, an implementation might generate an SEI.
- When EOImode == 1 but no EOI has been issued. The interrupt will be de-activated by the Distributor, however the active priority in the CPU interface for the interrupt will remain set (because no EOI was issued).

Accesses to this register use the following encodings:

MSR ICC_DIR_EL1, <Xt>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  else
    ICC_DIR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    ICC_DIR_EL2 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_DIR_EL3 = X[t];
  end if
end if

The ICC_EOIR0_EL1 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified Group 0 interrupt.

**Configuration**

AArch64 System register ICC_EOIR0_EL1 performs the same function as AArch32 System register ICC_EOIR0.

**Attributes**

ICC_EOIR0_EL1 is a 64-bit register.

**Field descriptions**

The ICC_EOIR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23-0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICC_IAR0_EL1 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the EOImode bit for the current Exception level and Security state is 0, a write to this register drops the priority for the interrupt, and also deactivates the interrupt.

If the EOImode bit for the current Exception level and Security state is 1, a write to this register only drops the priority for the interrupt. Software must write to ICC_DIR_EL1 to deactivate the interrupt.

The EOImode bit for the current Exception level and Security state is determined as follows:

- If EL3 is not implemented, the appropriate bit is ICC_CTLR_EL1.EOImode.
- If EL3 is implemented and the software is executing at EL3, the appropriate bit is ICC_CTLR_EL3.EOImode_EL3.
- If EL3 is implemented and the software is not executing at EL3, the bit depends on the current Security state:
  - If the software is executing in Secure state, the bit is ICC_CTLR_EL3.EOImode_EL1S.
  - If the software is executing in Non-secure state, the bit is ICC_CTLR_EL3.EOImode_EL1NS.
Accessing the ICC_EOIR0_EL1

A write to this register must correspond to the most recent valid read by this PE from an Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICC_IAR0_EL1, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

A write of a Special INTID is ignored. For more information, see ‘Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Accesses to this register use the following encodings:

MSR ICC_EOIR0_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICC_EOIR0_EL1 = X[t];
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_EOIR0_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_EOIR0_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_EOIR0_EL1 = X[t];
ICC_EOIR1_EL1, Interrupt Controller End Of Interrupt Register 1

The ICC_EOIR1_EL1 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified Group 1 interrupt.

**Configuration**

AArch64 System register ICC_EOIR1_EL1 performs the same function as AArch32 System register ICC_EOIR1.

**Attributes**

ICC_EOIR1_EL1 is a 64-bit register.

**Field descriptions**

The ICC_EOIR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICC_IAR1_EL1 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTRLR_EL1.IDbits and ICC_CTRLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the EOImode bit for the current Exception level and Security state is 0, a write to this register drops the priority for the interrupt, and also deactivates the interrupt.

If the EOImode bit for the current Exception level and Security state is 1, a write to this register only drops the priority for the interrupt. Software must write to ICC_DIR_EL1 to deactivate the interrupt.

The EOImode bit for the current Exception level and Security state is determined as follows:

- If EL3 is not implemented, the appropriate bit is ICC_CTRLR_EL1.EOImode.
- If EL3 is implemented and the software is executing at EL3, the appropriate bit is ICC_CTRLR_EL3.EOImode_EL3.
- If EL3 is implemented and the software is not executing at EL3, the bit depends on the current Security state:
  - If the software is executing in Secure state, the bit is ICC_CTRLR_EL3.EOImode_EL1S.
  - If the software is executing in Non-secure state, the bit is ICC_CTRLR_EL3.EOImode_EL1NS.
Accessing the ICC_EOIR1_EL1

A write to this register must correspond to the most recent valid read by this PE from an Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICC_IAR1_EL1, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

A write of a Special INTID is ignored. For more information, see ‘Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Accesses to this register use the following encodings:

MSR ICC_EOIR1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_EOIR1_EL1 = X[t];
    AArch64.SystemAccessTrap(EL1, 0x18);
else
  ICC_EOIR1_EL1 = X[t];
else
  ICC_EOIR1_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif ICC_EOIR1_EL1 = X[t];
    AArch64.SystemAccessTrap(EL2, 0x18);
else
  ICC_EOIR1_EL1 = X[t];
else
  ICC_EOIR1_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  elsif ICC_EOIR1_EL1 = X[t];
    AArch64.SystemAccessTrap(EL3, 0x18);
else
  ICC_EOIR1_EL1 = X[t];
```
**ICC_HPPIR0_EL1, Interrupt Controller Highest Priority Pending Interrupt Register 0**

The ICC_HPPIR0_EL1 characteristics are:

**Purpose**

Indicates the highest priority pending Group 0 interrupt on the CPU interface.

**Configuration**

AArch64 System register ICC_HPPIR0_EL1 performs the same function as AArch32 System register ICC_HPPIR0.

**Attributes**

ICC_HPPIR0_EL1 is a 64-bit register.

**Field descriptions**

The ICC_HPPIR0_EL1 bit assignments are:

```
<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23-0</td>
<td>INTID, bits [23:0]</td>
</tr>
</tbody>
</table>
```

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending interrupt, if that interrupt is observable at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_HPPIR0_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, ICC_HPPIR0_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICC_HPPIR0_EL1;
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR0_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR0_EL1;
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_HPPIR0_EL1;
end
The ICC_HPPIR1_EL1 characteristics are:

**Purpose**

Indicates the highest priority pending Group 1 interrupt on the CPU interface.

**Configuration**

AArch64 System register ICC_HPPIR1_EL1 performs the same function as AArch32 System register ICC_HPPIR1.

**Attributes**

ICC_HPPIR1_EL1 is a 64-bit register.

**Field descriptions**

The ICC_HPPIR1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:32</td>
<td>Reserved (RES0)</td>
</tr>
<tr>
<td>31:24</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending interrupt, if that interrupt is observable at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_HPPIR1_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_HPPIR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_HPPIR1_EL1;
    if Halted() && SCR_EL3.IRQ == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR1_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR1_EL1;
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_HPPIR1_EL1;
  end
ICC_IAR0_EL1, Interrupt Controller Interrupt Acknowledge Register 0

The ICC_IAR0_EL1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled Group 0 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch64 System register ICC_IAR0_EL1 performs the same function as AArch32 System register ICC_IAR0.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see 'Observability of the effects of accesses to the GIC registers'.

**Attributes**

ICC_IAR0_EL1 is a 64-bit register.

**Field descriptions**

The ICC_IAR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
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<tr>
<td>62</td>
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<tr>
<td>31</td>
<td>INTID</td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

This is the INTID of the highest priority pending interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see ‘Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_IAR0_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, ICC_IAR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        return ICV_IAR0_EL1;
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return ICC_IAR0_EL1;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return ICC_IAR0_EL1;
    end if
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICC_IAR0_EL1;
    end if
else
    return ICC_IAR0_EL1;
The ICC_IAR1_EL1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled Group 1 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch64 System register ICC_IAR1_EL1 performs the same function as AArch32 System register ICC_IAR1.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_IAR1_EL1 is a 64-bit register.

**Field descriptions**

The ICC_IAR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

This is the INTID of the highest priority pending interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR_EL1.IDbits and ICC_CTLR_EL3.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_IAR1_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, ICC_IAR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
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</tr>
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<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_IAR1_EL1;
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_IAR1_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_IAR1_EL1;
  endif
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_IAR1_EL1;
  endif

The ICC_IGRPEN0_EL1 characteristics are:

**Purpose**

Controls whether Group 0 interrupts are enabled or not.

**Configuration**

AArch64 System register ICC_IGRPEN0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICC_IGRPEN0[31:0].

**Attributes**

ICC_IGRPEN0_EL1 is a 64-bit register.

**Field descriptions**

The ICC_IGRPEN0_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |   0 |

**Bits [63:1]**

Reserved, RES0.

**Enable, bit [0]**

Enables Group 0 interrupts.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

Virtual accesses to this register update ICH_VMCR_EL2.VENG0.

If the highest priority pending interrupt for that PE is a Group 0 interrupt using 1 of N model, then the interrupt will be targeted to another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.

**Accessing the ICC_IGRPEN0_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS &lt;Xt&gt;, ICC_IGRPEN0_EL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ICC_IGRPENn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        return ICV_IGRPEN_EL1;
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return ICC_IGRPEN_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICC_IGRPEN_EL1;
    end
else
    return ICC_IGRPEN_EL1;
end

MSR ICC_IGRPEN0_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elif ICC_SRE_EL1.SRE == '0' then
    ICC_IGRPEN0_EL1 = X[t];
elif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ICC_IGRPENn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_IGRPEN0_EL1 = X[t];
elif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elif ICC_IGRPEN0_EL1 = X[t];
elif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elif ICC_IGRPEN0_EL1 = X[t];
elif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elif ICC_IGRPEN0_EL1 = X[t];
ICC_IGRPEN1_EL1, Interrupt Controller Interrupt Group 1 Enable register

The ICC_IGRPEN1_EL1 characteristics are:

**Purpose**

Controls whether Group 1 interrupts are enabled for the current Security state.

**Configuration**

AArch64 System register ICC_IGRPEN1_EL1 bits [31:0] (S) are architecturally mapped to AArch32 System register ICC_IGRPEN1[31:0] (S).

AArch64 System register ICC_IGRPEN1_EL1 bits [31:0] (NS) are architecturally mapped to AArch32 System register ICC_IGRPEN1[31:0] (NS).

**Attributes**

ICC_IGRPEN1_EL1 is a 64-bit register.

**Field descriptions**

The ICC_IGRPEN1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    | RES0|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**Bits [63:1]**

Reserved, RES0.

**Enable, bit [0]**

Enables Group 1 interrupts for the current Security state.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupts are disabled for the current Security state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupts are enabled for the current Security state.</td>
</tr>
</tbody>
</table>

Virtual accesses to this register update ICH_VMCR_EL2.VENG1.

If EL3 is present:

- The Secure ICC_IGRPEN1_EL1.Enable bit is a read/write alias of the ICC_IGRPEN1_EL3.EnableGrp1S bit.
- The Non-secure ICC_IGRPEN1_EL1.Enable bit is a read/write alias of the ICC_IGRPEN1_EL3.EnableGrp1NS bit.

If the highest priority pending interrupt for that PE is a Group 1 interrupt using 1 of N model, then the interrupt will target another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.
Accessing the ICC_IGRPEN1_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ICC_IGRPEN1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b110</td>
<td>0b110</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    UNDEFINED;
elsf ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elsf EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGTR_EL2.ICC_IGRPENn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsf EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsf EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_IGRPEN1_EL1;
elsf HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elsf HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_S;
elsf SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_NS;
elsf return ICC_IGRPEN1_EL1;
elsf PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    UNDEFINED;
elsf ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsf HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elsf HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_S;
elsf SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_NS;
elsf return ICC_IGRPEN1_EL1;
elsf PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
elsf HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_S;
elsf SCR_EL3.NS == '0' then
      return ICC_IGRPEN1_EL1_NS;
elsf return ICC_IGRPEN1_EL1;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ICC_IGRPENn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        ICC_IGRPEN1_EL1 = X[t];
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            ICC_IGRPEN1_EL1_S = X[t];
        else
            ICC_IGRPEN1_EL1_NS = X[t];
        end if;
    else
        ICC_IGRPEN1_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            ICC_IGRPEN1_EL1_S = X[t];
        else
            ICC_IGRPEN1_EL1_NS = X[t];
        end if;
    else
        ICC_IGRPEN1_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        if SCR_EL3.NS == '0' then
            ICC_IGRPEN1_EL1_S = X[t];
        else
            ICC_IGRPEN1_EL1_NS = X[t];
        end if;
    end if;
The ICC_IGRPEN1_EL3 characteristics are:

**Purpose**

Controls whether Group 1 interrupts are enabled or not.

**Configuration**

AArch64 System register ICC_IGRPEN1_EL3 bits [31:0] can be mapped to AArch32 System register ICC_MGRPEN1[31:0], but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to ICC_IGRPEN1_EL3 are **UNDEFINED**.

**Attributes**

ICC_IGRPEN1_EL3 is a 64-bit register.

**Field descriptions**

The ICC_IGRPEN1_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>EnableGrp1S</td>
<td></td>
<td>Enables Group 1 interrupts for the Secure state.</td>
</tr>
<tr>
<td>30</td>
<td>EnableGrp1NS</td>
<td></td>
<td>Enables Group 1 interrupts for the Non-secure state.</td>
</tr>
</tbody>
</table>

**Bits [63:2]**

Reserved, RES0.

**EnableGrp1S, bit [1]**

Enables Group 1 interrupts for the Secure state.

<table>
<thead>
<tr>
<th>EnableGrp1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

The Secure ICC_IGRPEN1_EL1.Enable bit is a read/write alias of the ICC_IGRPEN1_EL3.EnableGrp1S bit.

If the highest priority pending interrupt for that PE is a Group 1 interrupt using 1 of N model, then the interrupt will target another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.

**EnableGrp1NS, bit [0]**

Enables Group 1 interrupts for the Non-secure state.

<table>
<thead>
<tr>
<th>EnableGrp1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>
The Non-secure ICC_IGRPEN1_EL1.Enable bit is a read/write alias of the ICC_IGRPEN1_EL3.EnableGrp1NS bit.

If the highest priority pending interrupt for that PE is a Group 1 interrupt using 1 of N model, then the interrupt will target another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.

**Accessing the ICC_IGRPEN1_EL3**

Accesses to this register use the following encodings:

**MRS <Xt>, ICC_IGRPEN1_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICC_IGRPEN1_EL3;
    end

**MSR ICC_IGRPEN1_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        ICC_IGRPEN1_EL3 = X[t];
    end
ICC_PMRE1, Interrupt Controller Interrupt Priority Mask Register

The ICC_PMRE1 characteristics are:

**Purpose**

Provides an interrupt priority filter. Only interrupts with a higher priority than the value in this register are signaled to the PE.

Writes to this register must be high performance and must ensure that no interrupt of lower priority than the written value occurs after the write, without requiring an ISB or an exception boundary.

**Configuration**

AArch64 System register ICC_PMRE1 bits [31:0] are architecturally mapped to AArch32 System register ICC_PMRE[31:0].

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that writes to this register are self-synchronising. This ensures that no interrupts below the written PMR value will be taken after a write to this register is architecturally executed. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_PMRE1 is a 64-bit register.

**Field descriptions**

The ICC_PMRE1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**Bits [63:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The priority mask level for the CPU interface. If the priority of an interrupt is higher than the value indicated by this field, the interface signals the interrupt to the PE.

The possible priority field values are as follows:
Implemented priority bits | Possible priority field values | Number of priority levels
---|---|---
[7:0] | 0x00-0xFF (0-255), all values | 256
[7:1] | 0x00-0xFE (0-254), even values only | 128
[7:2] | 0x00-0xFC (0-252), in steps of 4 | 64
[7:3] | 0x00-0xF8 (0-248), in steps of 8 | 32
[7:4] | 0x00-0xF0 (0-240), in steps of 16 | 16

Unimplemented priority bits are RAZ/WI.

On a Warm reset, this field resets to 0.

**Accessing the ICC_PMR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_PMR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICV_PMR_EL1;
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_PMR_EL1;
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_PMR_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_PMR_EL1;
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_PMR_EL1;
  end
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif ICC_SRE_EL2.SRE == '0' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif ICC_SRE_EL3.SRE == '0' then
  AArch64.SystemAccessTrap(EL3, 0x18);
else
  ICC_PMR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL2.SRE == '0' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif ICC_SRE_EL3.SRE == '0' then
  AArch64.SystemAccessTrap(EL3, 0x18);
else
  ICC_PMR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
  ICC_PMR_EL1 = X[t];
ICC_RPR_EL1, Interrupt Controller Running Priority Register

The ICC_RPR_EL1 characteristics are:

**Purpose**

Indicates the Running priority of the CPU interface.

**Configuration**

AArch64 System register ICC_RPR_EL1 performs the same function as AArch32 System register ICC_RPR.

**Attributes**

ICC_RPR_EL1 is a 64-bit register.

**Field descriptions**

The ICC_RPR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7:0</td>
<td>Priority, bits [7:0]</td>
</tr>
</tbody>
</table>

**Priority, bits [7:0]**

The current running priority on the CPU interface. This is the group priority of the current active interrupt.

If there are no active interrupts on the CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

The priority returned is the group priority as if the BPR for the current Exception level and Security state was set to the minimum value of BPR for the number of implemented priority bits.

**Note**

If 8 bits of priority are implemented the group priority is bits[7:1] of the priority.

**Accessing the ICC_RPR_EL1**

Software cannot determine the number of implemented priority bits from a read of this register.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_RPR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICC_RPR_EL1;
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICC_RPR_EL1;
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_RPR_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return ICC_RPR_EL1;
  endif
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_RPR_EL1;
  endif
The ICC_SGI0R_EL1 characteristics are:

**Purpose**

Generates Secure Group 0 SGIs.

**Configuration**

AArch64 System register ICC_SGI0R_EL1 performs the same function as AArch32 System register ICC_SGI0R.

**Attributes**

ICC_SGI0R_EL1 is a 64-bit register.

**Field descriptions**

The ICC_SGI0R_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-56</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55-48</td>
<td>Aff3</td>
<td>The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated. If the IRM bit is 1, this field is RES0.</td>
</tr>
<tr>
<td>47-44</td>
<td>RS</td>
<td>RangeSelector</td>
</tr>
<tr>
<td>43-41</td>
<td>INTID</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>42-11</td>
<td>Aff2</td>
<td>Reserved.</td>
</tr>
<tr>
<td>10-0</td>
<td>TargetList</td>
<td>Controls which group of 16 values is represented by the TargetList field. TargetList[n] represents aff0 value ((RS * 16) + n). When ICC_CTLR_EL1.RSS==0, RS is RES0. When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a constrained unpredictable choice of:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The write is ignored.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• The RS field is treated as 0.</td>
</tr>
</tbody>
</table>

**Bits [63:56]**

Reserved, RES0.

**Aff3, bits [55:48]**

The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated. If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**

RangeSelector

Controls which group of 16 values is represented by the TargetList field. TargetList[n] represents aff0 value ((RS * 16) + n). When ICC_CTLR_EL1.RSS==0, RS is RES0.

When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a constrained unpredictable choice of:

• The write is ignored.
• The RS field is treated as 0.

**Bits [43:41]**

Reserved, RES0.
Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1.&lt;target list&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding “self”.</td>
</tr>
</tbody>
</table>

**Aff2, bits [39:32]**

The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**Bits [31:28]**

Reserved, RES0.

**INTID, bits [27:24]**

The INTID of the SGI.

**Aff1, bits [23:16]**

The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**TargetList, bits [15:0]**

Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.

If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is IMPLEMENTATION DEFINED whether, in such cases, a Distributor can signal a system error.

**Note**

This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16.

If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs. Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.

If the IRM bit is 1, this field is RES0.

**Accessing the ICC_SGI0R_EL1**

This register allows software executing in a Secure state to generate Group 0 SGIs. It will also allow software executing in a Non-secure state to generate Group 0 SGIs, if permitted by the settings of GICR_NSACR in the Redistributor corresponding to the target PE.

When GICD_CTLR.DS==0, Non-secure writes do not generate an interrupt for a target PE if not permitted by the GICR_NSACR register associated with the target PE. For more information, see ‘Use of control registers for SGI forwarding’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**
Accesses at EL3 are treated as Secure regardless of the value of SCR_EL3.NS.

Accesses to this register use the following encodings:

MSR ICC_SGI0R_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SGI0R_EL1 = X[t];
else
  ICC_SGI0R_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif ICC_SGI0R_EL2 = X[t];
else
  ICC_SGI0R_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  elseif ICC_SGI0R_EL3 = X[t];
ICC_SGI1R_EL1, Interrupt Controller Software Generated Interrupt Group 1 Register

The ICC_SGI1R_EL1 characteristics are:

**Purpose**

Generates Group 1 SGIs for the current Security state.

**Configuration**

AArch64 System register ICC_SGI1R_EL1 performs the same function as AArch32 System register ICC_SGI1R.

Under certain conditions a write to ICC_SGI1R_EL1 can generate Group 0 interrupts, see ‘Forwarding an SGI to a target PE’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_SGI1R_EL1 is a 64-bit register.

**Field descriptions**

The ICC_SGI1R_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| INTID | Aff3 | RES0 | IRM | Aff2 | RS  | RES0 | TargetList |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 09  | 08  | 07  | 06  | 05  | 04  | 03  | 02  | 01  | 00  |

**Bits [63:56]**

Reserved, RES0.

**Aff3, bits [55:48]**

The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**

RangeSelector

Controls which group of 16 values is represented by the TargetList field.

TargetList[n] represents aff0 value ((RS * 16) + n).

When ICC_CTLR_EL1.RSS==0, RS is RES0.

When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a constrained unpredictable choice of:

- The write is ignored.
- The RS field is treated as 0.
Bits [43:41]
Reserved, RES0.

IRM, bit [40]
Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1.&lt;target list&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding &quot;self&quot;.</td>
</tr>
</tbody>
</table>

Aff2, bits [39:32]
The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

Bits [31:28]
Reserved, RES0.

INTID, bits [27:24]
The INTID of the SGI.

Aff1, bits [23:16]
The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

TargetList, bits [15:0]
Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.
If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is IMPLEMENTATION DEFINED whether, in such cases, a Distributor can signal a system error.

Note
This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16.
If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs. Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.

If the IRM bit is 1, this field is RES0.

Accessing the ICC_SGI1R_EL1

Note
Accesses at EL3 are treated as Secure regardless of the value of SCR_EL3.NS.
Accesses to this register use the following encodings:

**MSR ICC_SGI1R_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elsif EL2Enabled() && HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif Halted() && HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SGI1R_EL1 = X[t];
else
  if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
      UNDEFINED;
elsif ICC_SRE_EL2.SRE == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
elsif ICC_SRI_EL3 == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elsif ICC_SGI1R_EL1 = X[t];
else
  if PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
      AArch64.SystemAccessTrap(EL3, 0x18);
elsif ICC_SGI1R_EL1 = X[t];
The ICC_SRE_EL1 characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL1.

**Configuration**

AArch64 System register ICC_SRE_EL1 bits [31:0] (S) are architecturally mapped to AArch32 System register ICC_SRE[31:0] (S).

AArch64 System register ICC_SRE_EL1 bits [31:0] (NS) are architecturally mapped to AArch32 System register ICC_SRE[31:0] (NS).

**Attributes**

ICC_SRE_EL1 is a 64-bit register.

**Field descriptions**

The ICC_SRE_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>DIB</td>
</tr>
<tr>
<td>61</td>
<td>Disable IRQ bypass</td>
</tr>
<tr>
<td>60</td>
<td>IRQ bypass enabled</td>
</tr>
<tr>
<td>59</td>
<td>IRQ bypass disabled</td>
</tr>
<tr>
<td>58</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
</tr>
<tr>
<td>56</td>
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<td>44</td>
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<td>42</td>
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<td>41</td>
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<td>40</td>
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<td>39</td>
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<td>38</td>
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<td>37</td>
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<tr>
<td>36</td>
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<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**DIB, bit [2]**

Disable IRQ bypass.

<table>
<thead>
<tr>
<th>DIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRQ bypass enabled</td>
</tr>
<tr>
<td>0b1</td>
<td>IRQ bypass disabled</td>
</tr>
</tbody>
</table>

If EL3 is implemented and GICD_CTLR.DS == 0, this field is a read-only alias of ICC_SRE_EL3.DIB.

If EL3 is implemented and GICD_CTLR.DS == 1, and EL2 is not implemented, this field is a read-write alias of ICC_SRE_EL3.DIB.

If EL3 is not implemented and EL2 is implemented, this field is a read-only alias of ICC_SRE_EL2.DIB.

If GICD_CTLR.DS == 1 and EL2 is implemented, this field is a read-only alias of ICC_SRE_EL2.DIB.

In systems that do not support IRQ bypass, this field is RAO/WI.

On a Warm reset, this field resets to 0.
DFB, bit [1]

Disable FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and \texttt{GICD_CTLR.DS == 0}, this field is a read-only alias of \texttt{ICC_SRE_EL3.DFB}.

If EL3 is implemented and \texttt{GICD_CTLR.DS == 1}, and EL2 is not implemented, this field is a read-write alias of \texttt{ICC_SRE_EL3.DFB}.

If EL3 is not implemented and EL2 is implemented, this field is a read-only alias of \texttt{ICC_SRE_EL2.DFB}.

If \texttt{GICD_CTLR.DS == 1} and EL2 is implemented, this field is a read-only alias of \texttt{ICC_SRE_EL2.DFB}.

In systems that do not support FIQ bypass, this field is RAO/WI.

On a Warm reset, this field resets to 0.

SRE, bit [0]

System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used. Access at EL1 to any ICC_* System register other than ICC_SRE_EL1 is trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface for the current Security state is enabled.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0 in the Secure instance of this register, the results are \textbf{UNPREDICTABLE}.

If an implementation supports only a System register interface to the GIC CPU interface, this bit is RAO/WI.

If EL3 is implemented and \texttt{ICC_SRE_EL3.SRE==0} the Secure copy of this bit is RAZ/WI. If \texttt{ICC_SRE_EL3.SRE} is changed from zero to one, the Secure copy of this bit becomes \textbf{UNKNOWN}.

If EL2 is implemented and \texttt{ICC_SRE_EL2.SRE==0} the Non-secure copy of this bit is RAZ/WI. If \texttt{ICC_SRE_EL2.SRE} is changed from zero to one, the Non-secure copy of this bit becomes \textbf{UNKNOWN}.

If EL3 is implemented and \texttt{ICC_SRE_EL3.SRE==0} the Non-secure copy of this bit is RAZ/WI. If \texttt{ICC_SRE_EL3.SRE} is changed from zero to one, the Non-secure copy of this bit becomes \textbf{UNKNOWN}.

GICv3 implementations that do not require GICv2 compatibility might choose to make this bit RAO/WI. The following options are supported:

- The Non-secure copy of \texttt{ICC_SRE_EL1.SRE} can be RAO/WI if \texttt{ICC_SRE_EL2.SRE} is also RAO/WI. This means all Non-secure software, including VMs using only virtual interrupts, must access the GIC using System registers.
- The Secure copy of \texttt{ICC_SRE_EL1.SRE} can be RAO/WI if \texttt{ICC_SRE_EL3.SRE} and \texttt{ICC_SRE_EL2.SRE} are also RAO/WI. This means that all Secure software must access the GIC using System registers and all Non-secure accesses to registers for physical interrupts must use System registers.

\textbf{Note}

A VM using only virtual interrupts might still use memory-mapped access if the Non-secure copy of \texttt{ICC_SRE_EL1.SRE} is not RAO/WI.

On a Warm reset, this field resets to 0.

\textbf{Accessing the ICC_SRE_EL1}

Execution with \texttt{ICC_SRE_EL1.SRE set to 0} might make some System registers \textbf{UNKNOWN}.

Accesses to this register use the following encodings:
MRS <Xt>, ICC_SRE_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && haveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif EL2Enabled() && ICC_SRE_EL2.Enable == '0' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif haveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x10);
    end if
  else
    return ICC_SRE_EL1_NS;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && haveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif haveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x10);
    end if
  else
    return ICC_SRE_EL1_NS;
  end if
elsif PSTATE.EL == EL3 then
  if SCR_EL3.NS == '0' then
    return ICC_SRE_EL1_S;
  else
    return ICC_SRE_EL1_NS;
  end if
else
  return ICC_SRE_EL1;
end if

MSR ICC_SRE_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    and ICC_SRE_EL1.Enable == '0' then
        UNDEFINED;
    elsif EL2Enabled() && ICC_SRE_EL2.Enable == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    and ICC_SRE_EL3.Enable == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
        if SCR_EL3.NS == '0' then
            ICC_SRE_EL1_S = X[t];
        else
            ICC_SRE_EL1_NS = X[t];
        end if
    else
        ICC_SRE_EL1 = X[t];
    end if
else
    ICC_SRE_EL1 = X[t];
end if
if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    and ICC_SRE_EL3.Enable == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
        if SCR_EL3.NS == '0' then
            ICC_SRE_EL1_S = X[t];
        else
            ICC_SRE_EL1_NS = X[t];
        end if
    else
        ICC_SRE_EL1 = X[t];
    end if
else
    ICC_SRE_EL1 = X[t];
end if
if PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        ICC_SRE_EL1_S = X[t];
    else
        ICC_SRE_EL1_NS = X[t];
    end if
else
    ICC_SRE_EL1 = X[t];
end if
The ICC_SRE_EL2 characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL2.

**Configuration**

AArch64 System register ICC_SRE_EL2 is architecturally mapped to AArch32 System register ICC_HSRE.

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICC_SRE_EL2 is a 64-bit register.

**Field descriptions**

The ICC_SRE_EL2 bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Enable, bit [3]**

Enable. Enables lower Exception level access to ICC_SRE_EL1.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When EL2 is implemented and enabled in the current Security state, EL1 accesses to ICC_SRE_EL1 trap to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to ICC_SRE_EL1 do not trap to EL2.</td>
</tr>
</tbody>
</table>

If ICC_SRE_EL2.SRE is RAO/WI, an implementation is permitted to make the Enable bit RAO/WI.

If ICC_SRE_EL2.SRE is 0, the Enable bit behaves as 1 for all purposes other than reading the value of the bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DIB, bit [2]**

Disable IRQ bypass.

<table>
<thead>
<tr>
<th>DIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>IRQ bypass disabled.</td>
</tr>
</tbody>
</table>
If EL3 is implemented and GICD_CTLR.DS is 0, this field is a read-only alias of ICC_SRE_EL3.DIB.

If EL3 is implemented and GICD_CTLR.DS is 1, this field is a read-write alias of ICC_SRE_EL3.DIB.

In systems that do not support IRQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

**DFB, bit [1]**

Disable FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and GICD_CTLR.DS is 0, this field is a read-only alias of ICC_SRE_EL3.DFB.

If EL3 is implemented and GICD_CTLR.DS is 1, this field is a read-write alias of ICC_SRE_EL3.DFB.

In systems that do not support FIQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

**SRE, bit [0]**

System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used. Access at EL2 to any ICH_* or ICC_* register other than ICC_SRE_EL1 or ICC_SRE_EL2, is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface to the ICH_* registers and the EL1 and EL2 ICC_* registers is enabled for EL2.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0, the results are UNPREDICTABLE.

If an implementation supports only a System register interface to the GIC CPU interface, this bit is RAO/WI.

If EL3 is implemented and ICC_SRE_EL3.SRE==0 this bit is RAZ/WI. If ICC_SRE_EL3.SRE is changed from zero to one, this bit becomes UNKNOWN.

FEAT_GICv3 implementations that do not require GICv2 compatibility might choose to make this bit RAO/WI, but this is only allowed if ICC_SRE_EL3.SRE is also RAO/WI.

On a Warm reset, this field resets to 0.

**Accessing the ICC_SRE_EL2**

Execution with ICC_SRE_EL2.SRE set to 0 might make some System registers UNKNOWN.

Accesses to this register use the following encodings:

\[
\text{MRS <Xt>, ICC_SRE_EL2}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return ICC_SRE_EL2;
  end if;
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    ICC_SRE_EL2 = X[t];
  end if;
end if;

MSR ICC_SRE_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    ICC_SRE_EL2 = X[t];
  end if;
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    ICC_SRE_EL2 = X[t];
  end if;
ICC_SRE_EL3, Interrupt Controller System Register Enable register (EL3)

The ICC_SRE_EL3 characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL3.

**Configuration**

AArch64 System register ICC_SRE_EL3 bits [31:0] can be mapped to AArch32 System register ICC_MSRE[31:0], but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to ICC_SRE_EL3 are UNDEFINED.

**Attributes**

ICC_SRE_EL3 is a 64-bit register.

**Field descriptions**

The ICC_SRE_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | Enable | DIB | DFB | SRE |

**Bits [63:4]**

Reserved, RES0.

**Enable, bit [3]**

Enable. Enables lower Exception level access to ICC_SRE_EL1 and ICC_SRE_EL2.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 accesses to ICC_SRE_EL1 trap to EL3, unless these accesses are trapped to EL2 as a result of ICC_SRE_EL2.Enable == 0. EL2 accesses to ICC_SRE_EL1 and ICC_SRE_EL2 trap to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to ICC_SRE_EL1 do not trap to EL3. EL2 accesses to ICC_SRE_EL1 and ICC_SRE_EL2 do not trap to EL3.</td>
</tr>
</tbody>
</table>

If ICC_SRE_EL3.SRE is RAO/WI, an implementation is permitted to make the Enable bit RAO/WI.

If ICC_SRE_EL3.SRE is 0, the Enable bit behaves as 1 for all purposes other than reading the value of the bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DIB, bit [2]**

Disable IRQ bypass.
DIB, bit [2]

Disable IRQ bypass.

<table>
<thead>
<tr>
<th>DIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>IRQ bypass disabled.</td>
</tr>
</tbody>
</table>

In systems that do not support IRQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

DFB, bit [1]

Disable FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

In systems that do not support FIQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

SRE, bit [0]

System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used. Access at EL3 to any ICH * or</td>
</tr>
<tr>
<td></td>
<td>ICC * register other than ICC_SRE_EL1, ICC_SRE_EL2, or ICC_SRE_EL3 is</td>
</tr>
<tr>
<td></td>
<td>trapped to EL3</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface to the ICH * registers and the EL1, EL2,</td>
</tr>
<tr>
<td></td>
<td>and EL3 ICC * registers is enabled for EL3.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0, the results are UNPREDICTABLE.

FEAT_GICv3 implementations that do not require GICv2 compatibility might choose to make this bit RAO/WI.

On a Warm reset, this field resets to 0.

Accessing the ICC_SRE_EL3

This register is always System register accessible.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_SRE_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b110</td>
<td>0b110</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return ICC_SRE_EL3;

MSR ICC_SRE_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b110</td>
<td>0b110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    ICC_SRE_EL3 = X[t];
ICH_AP0R<n>_EL2, Interrupt Controller Hyp Active Priorities Group 0 Registers, n = 0 - 3

The ICH_AP0R<n>_EL2 characteristics are:

**Purpose**

Provides information about Group 0 virtual active priorities for EL2.

**Configuration**

AArch64 System register ICH_AP0R<n>_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_AP0R<n>[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_AP0R<n>_EL2 is a 64-bit register.

**Field descriptions**

The ICH_AP0R<n>_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>P31</td>
</tr>
<tr>
<td>61</td>
<td>P30</td>
</tr>
<tr>
<td>60</td>
<td>P29</td>
</tr>
<tr>
<td>59</td>
<td>P28</td>
</tr>
<tr>
<td>58</td>
<td>P27</td>
</tr>
<tr>
<td>57</td>
<td>P26</td>
</tr>
<tr>
<td>56</td>
<td>P25</td>
</tr>
<tr>
<td>55</td>
<td>P24</td>
</tr>
<tr>
<td>54</td>
<td>P23</td>
</tr>
<tr>
<td>53</td>
<td>P22</td>
</tr>
<tr>
<td>52</td>
<td>P21</td>
</tr>
<tr>
<td>51</td>
<td>P20</td>
</tr>
<tr>
<td>50</td>
<td>P19</td>
</tr>
<tr>
<td>49</td>
<td>P18</td>
</tr>
<tr>
<td>48</td>
<td>P17</td>
</tr>
<tr>
<td>47</td>
<td>P16</td>
</tr>
<tr>
<td>46</td>
<td>P15</td>
</tr>
<tr>
<td>45</td>
<td>P14</td>
</tr>
<tr>
<td>44</td>
<td>P13</td>
</tr>
<tr>
<td>43</td>
<td>P12</td>
</tr>
<tr>
<td>42</td>
<td>P11</td>
</tr>
<tr>
<td>41</td>
<td>P10</td>
</tr>
<tr>
<td>40</td>
<td>P9</td>
</tr>
<tr>
<td>39</td>
<td>P8</td>
</tr>
<tr>
<td>38</td>
<td>P7</td>
</tr>
<tr>
<td>37</td>
<td>P6</td>
</tr>
<tr>
<td>36</td>
<td>P5</td>
</tr>
<tr>
<td>35</td>
<td>P4</td>
</tr>
<tr>
<td>34</td>
<td>P3</td>
</tr>
<tr>
<td>33</td>
<td>P2</td>
</tr>
<tr>
<td>32</td>
<td>P1</td>
</tr>
<tr>
<td>31</td>
<td>P0</td>
</tr>
<tr>
<td>30</td>
<td>Bits [63:32] Reserved, RES0.</td>
</tr>
</tbody>
</table>

**P<x>, bit [x], for x = 31 to 0**

Provides the access to the virtual active priorities for Group 0 interrupts. Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no Group 0 interrupt active with this priority level, or all active Group 0 interrupts with this priority level have undergone priority-drop.</td>
</tr>
<tr>
<td>0b1</td>
<td>There is a Group 0 interrupt active with this priority level which has not undergone priority drop.</td>
</tr>
</tbody>
</table>

The correspondence between priority levels and bits depends on the number of bits of priority that are implemented.

If 5 bits of preemption are implemented (bits [7:3] of priority), then there are 32 preemption levels, and the active state of these preemption levels are held in ICH_AP0R0_EL2 in the bits corresponding to Priority[7:3].

If 6 bits of preemption are implemented (bits [7:2] of priority), then there are 64 preemption levels, and:

- The active state of preemption levels 0 - 124 are held in ICH_AP0R0_EL2 in the bits corresponding to 0:Priority[6:2].
- The active state of preemption levels 128 - 252 are held in ICH_AP0R1_EL2 in the bits corresponding to 1:Priority[6:2].
If 7 bits of preemption are implemented (bits [7:1] of priority), then there are 128 preemption levels, and:

- The active state of preemption levels 0 - 62 are held in ICH_AP0R0_EL2 in the bits corresponding to 00:Priority[5:1].
- The active state of preemption levels 64 - 126 are held in ICH_AP0R1_EL2 in the bits corresponding to 01:Priority[5:1].
- The active state of preemption levels 128 - 190 are held in ICH_AP0R2_EL2 in the bits corresponding to 10:Priority[5:1].
- The active state of preemption levels 192 - 254 are held in ICH_AP0R3_EL2 in the bits corresponding to 11:Priority[5:1].

Note

Having the bit corresponding to a priority set to 1 in both ICH_AP0R<n>_EL2 and ICH_AP1R<n>_EL2 might result in UNPREDICTABLE behavior of the interrupt prioritization system for virtual interrupts.

On a Warm reset, this field resets to 0.

Software must ensure that ICH_AP0R<n>_EL2 is 0 for legacy VMs otherwise behaviour is UNPREDICTABLE. For more information about support for legacy VMs, see ‘Support for legacy operation of VMs’ in ARM Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

The active priorities for Group 0 and Group 1 interrupts for legacy VMs are held in ICH_AP1R<n>_EL2 and reads and writes to GICV_APR access ICH_AP1R<n>_EL2. This means that ICH_AP0R<n>_EL2 is inaccessible to legacy VMs.

Accessing the ICH_AP0R<n>_EL2

ICH_AP0R1_EL2 is only implemented in implementations that support 6 or more bits of preemption. ICH_AP0R2_EL2 and ICH_AP0R3_EL2 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are UNDEFINED.

Note

The number of bits of preemption is indicated by ICH_VTR_EL2.PREbits

Writing to these registers with any value other than the last read value of the register (or 0x00000000 for a newly set up virtual machine) can result in UNPREDICTABLE behavior of the virtual interrupt prioritization system allowing either:

- Virtual interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution at EL1 or EL0.

Writing to the active priority registers in any order other than the following order will result in UNPREDICTABLE behavior:

- ICH_AP0R<n>_EL2.
- ICH_AP1R<n>_EL2.

Having the bit corresponding to a priority set in both ICH_AP0R<n>_EL2 and ICH_AP1R<n>_EL2 can result in UNPREDICTABLE behavior of the interrupt prioritization system for virtual interrupts.

Accesses to this register use the following encodings:

MRS <Xt>, ICH_AP0R<n>_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x480+8*UInt(op2<1:0>)];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_AP0R_EL2[UInt(op2<1:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_AP0R_EL2[UInt(op2<1:0>)];

ICH_AP0R<n>_EL2, Interrupt Controller Hyp Active Priorities Group 0 Registers, n = 0 - 3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x480+8*UInt(op2<1:0>)] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    ICH_AP0R_EL2[UInt(op2<1:0>)] = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICH_AP0R_EL2[UInt(op2<1:0>)] = X[t];
ICH_AP1R<n>_EL2, Interrupt Controller Hyp Active Priorities Group 1 Registers, \( n = 0 - 3 \)

The ICH_AP1R<n>_EL2 characteristics are:

**Purpose**

Provides information about Group 1 virtual active priorities for EL2.

**Configuration**

AArch64 System register ICH_AP1R<n>_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_AP1R<n>[31:0].

If EL2 is not implemented, this register is \texttt{RES0}\( \text{ from EL3} \).

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_AP1R<n>_EL2 is a 64-bit register.

**Field descriptions**

The ICH_AP1R<n>_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bits (31:20)</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>P&lt;31&gt;, bit [31], for x = 0 to 31</td>
<td>Group 1 interrupt active priorities. Possible values of each bit are:</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P&lt;31&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0}</td>
<td>There is no Group 1 interrupt active with this priority level, or all active Group 1 interrupts with this priority level have undergone priority-drop.</td>
</tr>
<tr>
<td>\texttt{0b1}</td>
<td>There is a Group 1 interrupt active with this priority level which has not undergone priority drop.</td>
</tr>
</tbody>
</table>

The correspondence between priority levels and bits depends on the number of bits of priority that are implemented.

If 5 bits of preemption are implemented (bits [7:3] of priority), then there are 32 preemption levels, and the active state of these preemption levels are held in ICH_AP1R0_EL2 in the bits corresponding to Priority[7:3].

If 6 bits of preemption are implemented (bits [7:2] of priority), then there are 64 preemption levels, and:

- The active state of preemption levels 0 - 124 are held in ICH_AP1R0_EL2 in the bits corresponding to 0:Priority[6:2].
- The active state of preemption levels 128 - 252 are held in ICH_AP1R1_EL2 in the bits corresponding to 1:Priority[6:2].
If 7 bits of preemption are implemented (bits [7:1] of priority), then there are 128 preemption levels, and:

- The active state of preemption levels 0 - 62 are held in ICH_AP1R0_EL2 in the bits corresponding to 00:Priority[5:1].
- The active state of preemption levels 64 - 126 are held in ICH_AP1R1_EL2 in the bits corresponding to 01:Priority[5:1].
- The active state of preemption levels 128 - 190 are held in ICH_AP1R2_EL2 in the bits corresponding to 10:Priority[5:1].
- The active state of preemption levels 192 - 254 are held in ICH_AP1R3_EL2 in the bits corresponding to 11:Priority[5:1].

**Note**

Having the bit corresponding to a priority set to 1 in both ICH_AP0R<n>_EL2 and ICH_AP1R<n>_EL2 might result in UNPREDICTABLE behavior of the interrupt prioritization system for virtual interrupts.

On a Warm reset, this field resets to 0.

This register is always used for legacy VMs, regardless of the group of the virtual interrupt. Reads and writes to GICV_APR<n> access ICH_AP1R<n>_EL2. For more information about support for legacy VMs, see ‘Support for legacy operation of VMs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

### Accessing the ICH_AP1R<n>_EL2

ICH_AP1R1_EL2 is only implemented in implementations that support 6 or more bits of preemption. ICH_AP1R2_EL2 and ICH_AP1R3_EL2 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are UNDEFINED.

**Note**

The number of bits of preemption is indicated by ICH_VTR_EL2.PREbits

Writing to these registers with any value other than the last read value of the register (or 0x00000000 for a newly set up virtual machine) can result in UNPREDICTABLE behavior of the virtual interrupt prioritization system allowing either:

Writing to the active priority registers in any order other than the following order will result in UNPREDICTABLE behavior:

Accesses to this register use the following encodings:

```
MRS <Xt>, ICH_AP1R<n>_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x4A0+8*UInt(op2<1:0>)];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_AP1R_EL2[UInt(op2<1:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_AP1R_EL2[UInt(op2<1:0>)];

MSR ICH_AP1R<n>_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x4A0+8*UInt(op2<1:0>)] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    ICH_AP1R_EL2[UInt(op2<1:0>)] = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICH_AP1R_EL2[UInt(op2<1:0>)] = X[t];
ICH_EISR_EL2, Interrupt Controller End of Interrupt Status Register

The ICH_EISR_EL2 characteristics are:

**Purpose**

Indicates which List registers have outstanding EOI maintenance interrupts.

**Configuration**

AArch64 System register ICH_EISR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_EISR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_EISR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_EISR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:16]</th>
<th>Status&lt;n&gt;, bit [n], for n = 15 to 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>636261605958857565554535251504948</td>
<td>RES0</td>
</tr>
<tr>
<td>31302928272625242322212019181716</td>
<td>Status15Status14Status13Status12Status11Status10Status9Status8Status7Status6Status5Status4Status3Status2Status1Status0</td>
</tr>
</tbody>
</table>

**Bits [63:16]**

Reserved, RES0.

**Status<n>, bit [n], for n = 15 to 0**

EOI maintenance interrupt status bit for List register <n>:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List register &lt;n&gt;, ICH_LR&lt;n&gt;_EL2, does not have an EOI maintenance interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>List register &lt;n&gt;, ICH_LR&lt;n&gt;_EL2, has an EOI maintenance interrupt that has not been handled.</td>
</tr>
</tbody>
</table>

For any ICH_LR<n>_EL2, the corresponding status bit is set to 1 if all of the following are true:

- ICH_LR<n>_EL2.State is 0b00.
- ICH_LR<n>_EL2.HW is 0.
- ICH_LR<n>_EL2.EOI (bit [41]) is 1, indicating that when the interrupt corresponding to that List register is deactivated, a maintenance interrupt is asserted.

Otherwise the status bit takes the value 0.

**Accessing the ICH_EISR_EL2**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_EISR_EL2;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_EISR_EL2;
ICH_ELRSR_EL2, Interrupt Controller Empty List Register Status Register

The ICH_ELRSR_EL2 characteristics are:

**Purpose**

These registers can be used to locate a usable List register when the hypervisor is delivering an interrupt to a VM.

**Configuration**

AArch64 System register ICH_ELRSR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_ELRSR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_ELRSR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_ELRSR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Status0</th>
<th>Status1</th>
<th>Status2</th>
<th>Status3</th>
<th>Status4</th>
<th>Status5</th>
<th>Status6</th>
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<th>Status10</th>
<th>Status11</th>
<th>Status12</th>
<th>Status13</th>
<th>Status14</th>
<th>Status15</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES</td>
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</tr>
</tbody>
</table>

**Bits [63:16]**

Reserved, RES0.

**Status<n>, bit [n], for n = 15 to 0**

Status bit for List register <n>, ICH_LR<n>_EL2:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List register ICH_LR&lt;n&gt;_EL2, if implemented, contains a valid interrupt. Using this List register can result in overwriting a valid interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>List register ICH_LR&lt;n&gt;_EL2 does not contain a valid interrupt. The List register is empty and can be used without overwriting a valid interrupt or losing an EOI maintenance interrupt.</td>
</tr>
</tbody>
</table>

For any List register <n>, the corresponding status bit is set to 1 if ICH_LR<n>_EL2.State is 0b00 and either ICH_LR<n>_EL2.HW is 1 or ICH_LR<n>_EL2.EOI (bit [41]) is 0.

Otherwise the status bit takes the value 0.

**Accessing the ICH_ELRSR_EL2**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ICH_ELRSR_EL2;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICH_ELRSR_EL2;

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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ICH_HCR_EL2, Interrupt Controller Hyp Control Register

The ICH_HCR_EL2 characteristics are:

**Purpose**

Controls the environment for VMs.

**Configuration**

AArch64 System register ICH_HCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_HCR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_HCR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_HCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31-27</td>
<td>EOIcount, bits [31:27]</td>
</tr>
<tr>
<td>26-16</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15-0</td>
<td>Bits [63:32]</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**EOIcount, bits [31:27]**

This field is incremented whenever a successful write to a virtual EOIR or DIR register would have resulted in a virtual interrupt deactivation. That is either:

- A virtual write to EOIR with a valid interrupt identifier that is not in the LPI range (that is < 8192) when EOI mode is zero and no List Register was found.
- A virtual write to DIR with a valid interrupt identifier that is not in the LPI range (that is < 8192) when EOI mode is one and no List Register was found.

This allows software to manage more active interrupts than there are implemented List Registers.

It is **CONSTRAINED UNPREDICTABLE** whether a virtual write to EOIR that does not clear a bit in the Active Priorities registers (ICH_AP0R<n>_EL2/ICH_AP1R<n>_EL2) increments EOIcount. Permitted behaviors are:

- Increment EOIcount.
- Leave EOIcount unchanged.

On a Warm reset, this field resets to 0.

**Bits [26:16]**

Reserved, RES0.
**DVIM, bit [15]**

When `ICH_VTR_EL2.DVIM == 1`:

Directly-injected Virtual Interrupt Mask.

<table>
<thead>
<tr>
<th>DVIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the signalling of virtual interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual interrupts received via direct-injection are not presented to the virtual CPU interface and not considered when determining the highest priority pending virtual interrupt.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**TDIR, bit [14]**

Trap EL1 writes to `ICC_DIR_EL1` and `ICV_DIR_EL1`.

<table>
<thead>
<tr>
<th>TDIR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 writes of <code>ICC_DIR_EL1</code> and <code>ICV_DIR_EL1</code> are not trapped to EL2, unless trapped by other mechanisms.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 writes of <code>ICV_DIR_EL1</code> are trapped to EL2. It is IMPLEMENTATIONDEFINED whether writes of <code>ICC_DIR_EL1</code> are trapped. Not trapping <code>ICC_DIR_EL1</code> writes is DEPRECATED.</td>
</tr>
</tbody>
</table>

Support for this bit is OPTIONAL, with support indicated by `ICH_VTR_EL2`.

If the implementation does not support this trap, this bit is RES0.

Arm deprecates not including this trap bit.

On a Warm reset, this field resets to 0.

**TSEI, bit [13]**

Trap all locally generated SEIs. This bit allows the hypervisor to intercept locally generated SEIs that would otherwise be taken at EL1.

<table>
<thead>
<tr>
<th>TSEI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Locally generated SEIs do not cause a trap to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Locally generated SEIs trap to EL2.</td>
</tr>
</tbody>
</table>

If `ICH_VTR_EL2.SEIS` is 0, this bit is RES0.

On a Warm reset, this field resets to 0.

**TALL1, bit [12]**

Trap all EL1 accesses to ICC_* and ICV_* System registers for Group 1 interrupts to EL2.

<table>
<thead>
<tr>
<th>TALL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 accesses to ICC_* and ICV_* registers for Group 1 interrupts proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to ICC_* and ICV_* registers for Group 1 interrupts trap to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.
TALL0, bit [11]

Trap all EL1 accesses to ICC_* and ICV_* System registers for Group 0 interrupts to EL2.

<table>
<thead>
<tr>
<th>TALL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 accesses to ICC_* and ICV_* registers for Group 0 interrupts proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to ICC_* and ICV_* registers for Group 0 interrupts trap to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

TC, bit [10]

Trap all EL1 accesses to System registers that are common to Group 0 and Group 1 to EL2.

<table>
<thead>
<tr>
<th>TC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 accesses to common registers proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 accesses to common registers trap to EL2.</td>
</tr>
</tbody>
</table>

This affects accesses to ICC_SGIO_R_EL1, ICC_SGI1R_EL1, ICC_ASGI1R_EL1, ICC_CTLR_EL1, ICC_DIR_EL1, ICC_PMR_EL1, ICC_RPR_EL1, ICC_CTLR_EL1, ICC_DIR_EL1, ICC_PMR_EL1, and ICV_RPR_EL1.

On a Warm reset, this field resets to 0.

Bit [9]

Reserved, RES0.

vSGIEOICount, bit [8]

When FEAT_GICv4p1 is implemented:

Controls whether deactivation of virtual SGIs can increment ICH_HCR_EL2.EOIcount

<table>
<thead>
<tr>
<th>vSGIEOICount</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Deactivation of virtual SGIs can increment ICH_HCR_EL2.EOIcount.</td>
</tr>
<tr>
<td>0b1</td>
<td>Deactivation of virtual SGIs does not increment ICH_HCR_EL2.EOIcount.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

VGrp1DIE, bit [7]

VM Group 1 Disabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected vPE is disabled:

<table>
<thead>
<tr>
<th>VGrp1DIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR_EL2.VENG1 is 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

VGrp1EIE, bit [6]

VM Group 1 Enabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected vPE is enabled:
ICH_HCR_EL2, Interrupt Controller Hyp Control Register

<table>
<thead>
<tr>
<th>VGrp1EIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR_EL2.VENG1 is 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**VGrp0DIE, bit [5]**

VM Group 0 Disabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 0 interrupts from the virtual CPU interface to the connected vPE is disabled:

<table>
<thead>
<tr>
<th>VGrp0DIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR_EL2.VENG0 is 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**VGrp0EIE, bit [4]**

VM Group 0 Enabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 0 interrupts from the virtual CPU interface to the connected vPE is enabled:

<table>
<thead>
<tr>
<th>VGrp0EIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR_EL2.VENG0 is 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**NPIE, bit [3]**

No Pending Interrupt Enable. Enables the signaling of a maintenance interrupt when there are no List registers with the State field set to 0b01 (pending):

<table>
<thead>
<tr>
<th>NPIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled while the List registers contain no interrupts in the pending state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**LRENPIE, bit [2]**

List Register Entry Not Present Interrupt Enable. Enables the signaling of a maintenance interrupt while the virtual CPU interface does not have a corresponding valid List register entry for an EOI request:

<table>
<thead>
<tr>
<th>LRENPIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt is asserted while the EOICount field is not 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**UIE, bit [1]**

Underflow Interrupt Enable. Enables the signaling of a maintenance interrupt when the List registers are empty, or hold only one valid entry:

<table>
<thead>
<tr>
<th>UIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt is asserted if none, or only one, of the List register entries is marked as a valid interrupt.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to 0.

**En, bit [0]**

Enable. Global enable bit for the virtual CPU interface:

<table>
<thead>
<tr>
<th>En</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Virtual CPU interface operation disabled.</td>
</tr>
<tr>
<td>01</td>
<td>Virtual CPU interface operation enabled.</td>
</tr>
</tbody>
</table>

When this field is set to 0:

- The virtual CPU interface does not signal any maintenance interrupts.
- The virtual CPU interface does not signal any virtual interrupts.
- A read of ICV_IAR0_EL1, ICV_IAR1_EL1, GICV_IAR or GICV_AIAR returns a spurious interrupt ID.

**Note**

This field is RES0 when SCR_EL3.{NS,EEL2}=={0,0}

On a Warm reset, this field resets to 0.

**Accessing the ICH_HCR_EL2**

Accesses to this register use the following encodings:

**MRS <Xt>, ICH_HCR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```cpp
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x4C0];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_HCR_EL2;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_HCR_EL2;

MSR ICH_HCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
     UNDEFINED;
elsif PSTATE.EL == EL1 then
     if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
         NVMem[0x4C0] = X[t];
     elsif EL2Enabled() && HCR_EL2.NV == '1' then
         AArch64.SystemAccessTrap(EL2, 0x18);
     else
         UNDEFINED;
     end
elsif PSTATE.EL == EL2 then
     if ICC_SRE_EL2.SRE == '0' then
         AArch64.SystemAccessTrap(EL2, 0x18);
     else
         ICH_HCR_EL2 = X[t];
     end
elsif PSTATE.EL == EL3 then
     if ICC_SRE_EL3.SRE == '0' then
         AArch64.SystemAccessTrap(EL3, 0x18);
     else
         ICH_HCR_EL2 = X[t];
end
ICH_LR<n>_EL2, Interrupt Controller List Registers, n = 0 - 15

The ICH_LR<n>_EL2 characteristics are:

**Purpose**

Provides interrupt context information for the virtual CPU interface.

**Configuration**

AArch64 System register ICH_LR<n>_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_LR<n>[31:0].

AArch64 System register ICH_LR<n>_EL2 bits [63:32] are architecturally mapped to AArch32 System register ICH_LRC<n>[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

If list register n is not implemented, then accesses to this register are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_LR<n>_EL2 is a 64-bit register.

**Field descriptions**

The ICH_LR<n>_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>State</th>
<th>HW</th>
<th>Group</th>
<th>RES0</th>
<th>Priority</th>
<th>RES0</th>
<th>pINTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60</td>
<td>59 58 57 56</td>
<td>55 54 53 52</td>
<td>51 50 49 48</td>
<td>47 46 45 44</td>
<td>43 42 41 40</td>
<td>39 38 37 36</td>
</tr>
<tr>
<td>31 30 29 28</td>
<td>27 26 25 24</td>
<td>23 22 21 20</td>
<td>19 18 17 16</td>
<td>15 14 13 12</td>
<td>11 10 9 8</td>
<td>7 6 5 4</td>
</tr>
<tr>
<td>vINTID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**State, bits [63:62]**

The state of the interrupt:

<table>
<thead>
<tr>
<th>State</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Invalid (Inactive).</td>
</tr>
<tr>
<td>0b01</td>
<td>Pending.</td>
</tr>
<tr>
<td>0b10</td>
<td>Active.</td>
</tr>
<tr>
<td>0b11</td>
<td>Pending and active.</td>
</tr>
</tbody>
</table>

The GIC updates these state bits as virtual interrupts proceed through the interrupt life cycle. Entries in the invalid state are ignored, except for the purpose of generating virtual maintenance interrupts.

For hardware interrupts, the pending and active state is held in the physical Distributor rather than the virtual CPU interface. A hypervisor must only use the pending and active state for software originated interrupts, which are typically associated with virtual devices, or SGIs.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
HW, bit [61]

Indicates whether this virtual interrupt maps directly to a hardware interrupt, meaning that it corresponds to a physical interrupt. Deactivation of the virtual interrupt also causes the deactivation of the physical interrupt with the ID that the pINTID field indicates.

<table>
<thead>
<tr>
<th>HW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The interrupt is triggered entirely by software. No notification is sent to the Distributor when the virtual interrupt is deactivated.</td>
</tr>
<tr>
<td>0b1</td>
<td>The interrupt maps directly to a hardware interrupt. A deactivate interrupt request is sent to the Distributor when the virtual interrupt is deactivated, using the pINTID field from this register to indicate the physical interrupt ID. If \texttt{ICH_VMCR_EL2.VEOIM} is 0, this request corresponds to a write to \texttt{ICC_EOIR0_EL1} or \texttt{ICC_EOIR1_EL1}. Otherwise, it corresponds to a write to \texttt{ICC_DIR_EL1}.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Group, bit [60]

Indicates the group for this virtual interrupt.

<table>
<thead>
<tr>
<th>Group</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This is a Group 0 virtual interrupt. \texttt{ICH_VMCR_EL2.VFIQEn} determines whether it is signaled as a virtual IRQ or as a virtual FIQ, and \texttt{ICH_VMCR_EL2.VENG0} enables signaling of this interrupt to the virtual machine.</td>
</tr>
<tr>
<td>0b1</td>
<td>This is a Group 1 virtual interrupt, signaled as a virtual IRQ. \texttt{ICH_VMCR_EL2.VENG1} enables the signaling of this interrupt to the virtual machine. If \texttt{ICH_VMCR_EL2.VCBPR} is 0, then \texttt{ICC_BPR1_EL1} determines if a pending Group 1 interrupt has sufficient priority to preempt current execution. Otherwise, \texttt{ICH_LR&lt;n&gt;_EL2} determines preemption.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [59:56]

Reserved, RES0.

Priority, bits [55:48]

The priority of this interrupt.

It is IMPLEMENTATION DEFINED how many bits of priority are implemented, though at least five bits must be implemented. Unimplemented bits are RES0 and start from bit[48] up to bit[50]. The number of implemented bits can be discovered from \texttt{ICH_VTR_EL2.PRIbits}. On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [47:45]

Reserved, RES0.

pINTID, bits [44:32]

Physical INTID, for hardware interrupts.

When \texttt{ICH_LR<n>_EL2.HW} is 0 (there is no corresponding physical interrupt), this field has the following meaning:

- Bits[44:42] : RES0.
- Bit[41] : EOI. If this bit is 1, then when the interrupt identified by vINTID is deactivated, a maintenance interrupt is asserted.
When ICH_LR<n>_EL2.HW is 1 (there is a corresponding physical interrupt):

- This field indicates the physical INTID. This field is only required to implement enough bits to hold a valid value for the implemented INTID size. Any unused higher order bits are RES0.
- When ICC_CTLR EL1.ExtRange is 0, then bits[44:42] of this field are RES0.
- If the value of pINTID is not a valid INTID, behavior is UNPREDICTABLE. If the value of pINTID indicates a PPI, this field applies to the PPI associated with this same physical PE ID as the virtual CPU interface requesting the deactivation.

A hardware physical identifier is only required in List Registers for interrupts that require deactivation. This means only 13 bits of Physical INTID are required, regardless of the number specified by ICC_CTLR_EL1.IDbits.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**vINTID, bits [31:0]**

Virtual INTID of the interrupt.

If the value of vINTID is 1020-1023 and ICH_LR<n>_EL2.State!=0b00 (Inactive), behavior is UNPREDICTABLE.

Behavior is UNPREDICTABLE if two or more List Registers specify the same vINTID when:

- ICH_LR<n>_EL2.State == 0b01.
- ICH_LR<n>_EL2.State == 0b10.
- ICH_LR<n>_EL2.State == 0b11.

It is IMPLEMENTATION DEFINED how many bits are implemented, though at least 16 bits must be implemented. Unimplemented bits are RES0. The number of implemented bits can be discovered from ICH_VTR_EL2.IDbits.

When ICC_SRE_EL1.SRE == 0, specifying a vINTID in the LPI range is UNPREDICTABLE.

---

**Note**

When a VM is using memory-mapped access to the GIC, software must ensure that the correct source PE ID is provided in bits[12:10].

---

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICH_LR<n>_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, ICH_LR<n>_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b110:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x400+8*UInt(CRm<0>:op2<2:0>)] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_LR_EL2[UInt(CRm<0>:op2<2:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_LR_EL2[UInt(CRm<0>:op2<2:0>)];
end if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x400+8*UInt(CRm<0>:op2<2:0>)] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ICH_LR_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICH_LR_EL2[UInt(CRm<0>:op2<2:0>)] = X[t];
end

MSR ICH_LR<n>_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b110:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

30/09/2020 15:06; ccead0cb9f08f99cece050268e82ae9e71047211
Copyright © 2010-2020 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.
ICH_MISR_EL2, Interrupt Controller Maintenance Interrupt State Register

The ICH_MISR_EL2 characteristics are:

**Purpose**

Indicates which maintenance interrupts are asserted.

**Configuration**

AArch64 System register ICH_MISR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_MISR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_MISR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_MISR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-8</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**VGrp1D, bit [7]**

vPE Group 1 Disabled.

<table>
<thead>
<tr>
<th>VGrp1D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>vPE Group 1 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>01</td>
<td>vPE Group 1 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when ICH_HCR_EL2.VGrp1DIE==1 and ICH_VMCR_EL2.VENG1==is 0.

On a Warm reset, this field resets to 0.

**VGrp1E, bit [6]**

vPE Group 1 Enabled.

<table>
<thead>
<tr>
<th>VGrp1E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>vPE Group 1 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>01</td>
<td>vPE Group 1 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when ICH_HCR_EL2.VGrp1EIE==1 and ICH_VMCR_EL2.VENG1==is 1.
On a Warm reset, this field resets to 0.

**VGrp0D, bit [5]**

vPE Group 0 Disabled.

<table>
<thead>
<tr>
<th>VGrp0D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when $ICH_HCR_EL2.VGrp0DIE==1$ and $ICH_VMCR_EL2.VENG0==0$.

On a Warm reset, this field resets to 0.

**VGrp0E, bit [4]**

vPE Group 0 Enabled.

<table>
<thead>
<tr>
<th>VGrp0E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when $ICH_HCR_EL2.VGrp0EIE==1$ and $ICH_VMCR_EL2.VENG0==1$.

On a Warm reset, this field resets to 0.

**NP, bit [3]**

No Pending.

<table>
<thead>
<tr>
<th>NP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Pending maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>No Pending maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when $ICH_HCR_EL2.NPIE==1$ and no List register is in pending state.

On a Warm reset, this field resets to 0.

**LRENP, bit [2]**

List Register Entry Not Present.

<table>
<thead>
<tr>
<th>LRENP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List Register Entry Not Present maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>List Register Entry Not Present maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when $ICH_HCR_EL2.LRENPIE==1$ and $ICH_HCR_EL2.EOIcount$ is non-zero.

On a Warm reset, this field resets to 0.

**U, bit [1]**

Underflow.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when $ICH_HCR_EL2.UIE==1$ and zero or one of the List register entries are marked as a valid interrupt, that is, if the corresponding $ICH_LR<n>_EL2.State$ bits do not equal $0x0$.

On a Warm reset, this field resets to 0.
**EOI, bit [0]**

End Of Interrupt.

<table>
<thead>
<tr>
<th>EOI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>End Of Interrupt maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>End Of Interrupt maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when at least one bit in **ICH_EISR_EL2** is 1.

On a Warm reset, this field resets to 0.

The U and NP bits do not include the status of any pending/active 'VSet (IRI)' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069) packets because these bits control generation of interrupts that allow software management of the contents of the List Registers (which are not affected by 'VSet (IRI)' packets).

**Accessing the ICH_MISR_EL2**

Accesses to this register use the following encodings:

```
MRS <Xt>, ICH_MISR_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```java
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ICH_MISR_EL2;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICH_MISR_EL2;
```

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ICH_VMCR_EL2, Interrupt Controller Virtual Machine Control Register

The ICH_VMCR_EL2 characteristics are:

**Purpose**

Enables the hypervisor to save and restore the virtual machine view of the GIC state.

**Configuration**

AArch64 System register ICH_VMCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_VMCR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_VMCR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_VMCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**VPMR, bits [31:24]**

Virtual Priority Mask. The priority mask level for the virtual CPU interface. If the priority of a pending virtual interrupt is higher than the value indicated by this field, the interface signals the virtual interrupt to the PE.

This field is an alias of ICV_PMR_EL1.Priority.

**VBPR0, bits [23:21]**

Virtual Binary Point Register, Group 0. Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 0 interrupt preemption, and also determines Group 1 interrupt preemption if ICH_VMCR_EL2.VCBPR == 1.

This field is an alias of ICV_BPR0_EL1.BinaryPoint.

The minimum value of this field is determined by ICH_VTR_EL2.PREbits. An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value.
**VBPR1, bits [20:18]**

Virtual Binary Point Register, Group 1. Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption if `ICH_VMCR_EL2.VCBPR == 0`.

This field is an alias of `ICV_BPR1_EL1.BinaryPoint`.

This field is always accessible to EL2 accesses, regardless of the setting of the `ICH_VMCR_EL2.VCBPR` field.

For Non-secure writes, the minimum value of this field is the minimum value of `ICH_VMCR_EL2.VBPR0` plus one.

For Secure writes, the minimum value of this field is the minimum value of `ICH_VMCR_EL2.VBPR0`.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value.

**Bits [17:10]**

Reserved, `RES0`.

**VEOIM, bit [9]**

Virtual EOI mode. Controls whether a write to an End of Interrupt register also deactivates the virtual interrupt:

<table>
<thead>
<tr>
<th>VEOIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>ICV_EOIR0_EL1</code> and <code>ICV_EOIR1_EL1</code> provide both priority drop and interrupt deactivation functionality. Accesses to <code>ICV_DIR_EL1</code> are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>ICV_EOIR0_EL1</code> and <code>ICV_EOIR1_EL1</code> provide priority drop functionality only. <code>ICV_DIR_EL1</code> provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

This bit is an alias of `ICV_CTLR_EL1.EOImode`.

**Bits [8:5]**

Reserved, `RES0`.

**VCBPR, bit [4]**

Virtual Common Binary Point Register. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VCBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>ICV_BPR1_EL1</code> determines the preemption group for virtual Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reads of <code>ICV_BPR1_EL1</code> return <code>ICV_BPR0_EL1</code> plus one, saturated to <code>0b11</code>. Writes to <code>ICV_BPR1_EL1</code> are ignored.</td>
</tr>
</tbody>
</table>

This field is an alias of `ICV_CTLR_EL1.CBPR`.

**VFIQEn, bit [3]**

Virtual FIQ enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VFIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupts are presented as virtual IRQs.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 virtual interrupts are presented as virtual FIQs.</td>
</tr>
</tbody>
</table>

This bit is an alias of `GICV_CTLR.FIQEn`.

In implementations where the Non-secure copy of `ICC_SRE_EL1.SRE` is always 1, this bit is `RES1`. 
VAckCtl, bit [2]

Virtual AckCtl. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VAckCtl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns an INTID of 1022.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns the INTID of the corresponding interrupt.</td>
</tr>
</tbody>
</table>

This bit is an alias of GICV_CTLR.AckCtl.

This field is supported for backwards compatibility with GICv2. Arm deprecates the use of this field.

In implementations where the Non-secure copy of ICC_SRE_EL1.SRE is always 1, this bit is RES0.

VENG1, bit [1]

Virtual Group 1 interrupt enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

This bit is an alias of ICV_IGRPEN1_EL1.Enable.

VENG0, bit [0]

Virtual Group 0 interrupt enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

This bit is an alias of ICV_IGRPEN0_EL1.Enable.

Accessing the ICH_VMCR_EL2

When EL2 is using System register access, EL1 using either System register or memory-mapped access must be supported.

Accesses to this register use the following encodings:

MRS <Xt>, ICH_VMCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
      return NVMem[0x4C8];
   elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
endif
elsif PSTATE.EL == EL2 then
   if ICC_SRE_EL2.SRE == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      return ICH_VMCR_EL2;
endif
elsif PSTATE.EL == EL3 then
   if ICC_SRE_EL3.SRE == '0' then
      AArch64.SystemAccessTrap(EL3, 0x18);
   else
      return ICH_VMCR_EL2;
endif
endif

ICH_VMCR_EL2, Interrupt Controller Virtual Machine Control Register

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
      NVMem[0x4C8] = X[t];
   elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
endif
elsif PSTATE.EL == EL2 then
   if ICC_SRE_EL2.SRE == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      ICH_VMCR_EL2 = X[t];
endif
elsif PSTATE.EL == EL3 then
   if ICC_SRE_EL3.SRE == '0' then
      AArch64.SystemAccessTrap(EL3, 0x18);
   else
      ICH_VMCR_EL2 = X[t];
endif
ICH_VTR_EL2, Interrupt Controller VGIC Type Register

The ICH_VTR_EL2 characteristics are:

**Purpose**

Reports supported GIC virtualization features.

**Configuration**

AArch64 System register ICH_VTR_EL2 bits [31:0] are architecturally mapped to AArch32 System register ICH_VTR[31:0].

If EL2 is not implemented, all bits in this register are RES0 from EL3, except for nV4, which is RES1 from EL3. This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ICH_VTR_EL2 is a 64-bit register.

**Field descriptions**

The ICH_VTR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | PRIbits | PREbits | IDbits | SEISA3V | TDSDVIM | RES0 | ListRegs |

**Bits [63:32]**

Reserved, RES0.

**PRIbits, bits [31:29]**

Priority bits. The number of virtual priority bits implemented, minus one.

An implementation must implement at least 32 levels of virtual priority (5 priority bits).

This field is an alias of ICV_CTLR_EL1.PRIbits.

**PREbits, bits [28:26]**

The number of virtual preemption bits implemented, minus one.

An implementation must implement at least 32 levels of virtual preemption priority (5 preemption bits).

The value of this field must be less than or equal to the value of ICH_VTR_EL2.PRIbits.

The maximum value of this field is 6, indicating 7 bits of preemption.

This field determines the minimum value of ICH_VMCR_EL2.VBPR0.

**IDbits, bits [25:23]**

The number of virtual interrupt identifier bits supported:
### IDbits

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is an alias of `ICV_CTLR_EL1.IDbits`.

### SEIS, bit [22]

SEI Support. Indicates whether the virtual CPU interface supports generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic does not support generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports generation of SEIs.</td>
</tr>
</tbody>
</table>

This bit is an alias of `ICV_CTLR_EL1.SEIS`.

### A3V, bit [21]

Affinity 3 Valid. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

This bit is an alias of `ICV_CTLR_EL1.A3V`.

### nV4, bit [20]

Direct injection of virtual interrupts not supported. Possible values are:

<table>
<thead>
<tr>
<th>nV4</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic supports direct injection of virtual interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic does not support direct injection of virtual interrupts.</td>
</tr>
</tbody>
</table>

If FEAT_GICv4 is not implemented, this bit is `RES1`.

### TDS, bit [19]

Separate trapping of EL1 writes to `ICV_DIR_EL1` supported.

<table>
<thead>
<tr>
<th>TDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Implementation does not support <code>ICH_HCR_EL2.TDIR</code>.</td>
</tr>
<tr>
<td>0b1</td>
<td>Implementation supports <code>ICH_HCR_EL2.TDIR</code>.</td>
</tr>
</tbody>
</table>

### DVIM, bit [18]

Masking of directly-injected virtual interrupts.

<table>
<thead>
<tr>
<th>DVIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Masking of Directly-injected Virtual Interrupts not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Masking of Directly-injected Virtual Interrupts is supported.</td>
</tr>
</tbody>
</table>

### Bits [17:5]

Reserved, `RES0`. 

ICH_VTR_EL2, Interrupt Controller VGIC Type Register

Page 902
ListRegs, bits [4:0]

The number of implemented List registers, minus one. For example, a value of 0b01111 indicates that the maximum of 16 List registers are implemented.

Accessing the ICH_VTR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, ICH_VTR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ICH_VTR_EL2;
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICH_VTR_EL2;
ICV_AP0R<n>_EL1, Interrupt Controller Virtual Active Priorities Group 0 Registers, n = 0 - 3

The ICV_AP0R<n>_EL1 characteristics are:

**Purpose**

Provides information about virtual Group 0 active priorities.

**Configuration**

AArch64 System register ICV_AP0R<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_AP0R<n>[31:0].

**Attributes**

ICV_AP0R<n>_EL1 is a 64-bit register.

**Field descriptions**

The ICV_AP0R<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED, bits [31:0]</td>
</tr>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED, bits [31:0]</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICV_AP0R<n>_EL1**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 0 active priorities) might result in UNPREDICTABLE behavior of the virtual interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICV_AP0R1_EL1 is only implemented in implementations that support 6 or more bits of priority. ICV_AP0R2_EL1 and ICV_AP0R3_EL1 are only implemented in implementations that support 7 bits of priority. Unimplemented registers are UNDEFINED.

Writing to the active priority registers in any order other than the following order might result in UNPREDICTABLE behavior of the interrupt prioritization system:

- ICV_AP0R<n>_EL1.
• **ICV_AP0R<n>_EL1**.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_AP0R<n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_AP0R_EL1[UInt(op2<1:0>)];
  end

MSR ICC_AP0R<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TALL == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_AP0R_EL1[UInt(op2<1:0>)] = X[t];
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_AP0R_EL1[UInt(op2<1:0>)] = X[t];
ICV_AP1R<n>_EL1, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3

The ICV_AP1R<n>_EL1 characteristics are:

**Purpose**

Provides information about virtual Group 1 active priorities.

**Configuration**

AArch64 System register ICV_AP1R<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_AP1R<n>[31:0].

**Attributes**

ICV_AP1R<n>_EL1 is a 64-bit register.

**Field descriptions**

The ICV_AP1R<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td></td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>0</td>
<td>The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.</td>
</tr>
</tbody>
</table>

**Accessing the ICV_AP1R<n>_EL1**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 1 active priorities) might result in UNPREDICTABLE behavior of the virtual interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICV_AP1R1_EL1 is only implemented in implementations that support 6 or more bits of priority. ICV_AP1R2_EL1 and ICV_AP1R3_EL1 are only implemented in implementations that support 7 bits of priority. Unimplemented registers are UNDEFINED.

Writing to the active priority registers in any order other than the following order might result in UNPREDICTABLE behavior of the interrupt prioritization system:

- **ICV_AP0R<n>_EL1**.
ICV_APB<n>_EL1, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3

- ICV_APB<n>_EL1.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_APB<n>_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() & ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif SCR_EL3.IRQ == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  endif
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif SCR_EL3.IRQ == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  endif
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if SCR_EL3.IRQ == '1' then
      return ICC_APB_EL1_S[UInt(op2<1:0>)];
    else
      return ICC_APB_EL1_NS[UInt(op2<1:0>)];
    endif
  endif
else
  return ICC_APB_EL1[UInt(op2<1:0>)];
endif

MSR ICC_APB<n>_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        ICV_AP1R_EL1[UInt(op2<1:0>)] = X[t];
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
        else
            ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
        endif
    else
        ICC_AP1R_EL1[UInt(op2<1:0>)] = X[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
        else
            ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
        endif
    else
        ICC_AP1R_EL1[UInt(op2<1:0>)] = X[t];
    endif
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        if SCR_EL3.NS == '0' then
            ICC_AP1R_EL1_S[UInt(op2<1:0>)] = X[t];
        else
            ICC_AP1R_EL1_NS[UInt(op2<1:0>)] = X[t];
        endif
    endif

The ICV_BPR0_EL1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines virtual Group 0 interrupt preemption.

**Configuration**

AArch64 System register ICV_BPR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_BPR0[31:0].

**Attributes**

ICV_BPR0_EL1 is a 64-bit register.

**Field descriptions**

The ICV_BPR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>BinaryPoint</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>57</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, RES0</td>
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<tr>
<td>48</td>
<td>Reserved, RES0</td>
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<tr>
<td>47</td>
<td>Reserved, RES0</td>
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<tr>
<td>46</td>
<td>Reserved, RES0</td>
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<td>45</td>
<td>Reserved, RES0</td>
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<td>44</td>
<td>Reserved, RES0</td>
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<td>43</td>
<td>Reserved, RES0</td>
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<td>42</td>
<td>Reserved, RES0</td>
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<td>41</td>
<td>Reserved, RES0</td>
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<td>40</td>
<td>Reserved, RES0</td>
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<tr>
<td>39</td>
<td>Reserved, RES0</td>
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<tr>
<td>38</td>
<td>Reserved, RES0</td>
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<tr>
<td>37</td>
<td>Reserved, RES0</td>
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<tr>
<td>36</td>
<td>Reserved, RES0</td>
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<tr>
<td>35</td>
<td>Reserved, RES0</td>
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<tr>
<td>34</td>
<td>Reserved, RES0</td>
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<tr>
<td>33</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>Res0</td>
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<tr>
<td>30</td>
<td>Res0</td>
</tr>
<tr>
<td>29</td>
<td>Res0</td>
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<tr>
<td>28</td>
<td>Res0</td>
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<tr>
<td>27</td>
<td>Res0</td>
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<tr>
<td>26</td>
<td>Res0</td>
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<tr>
<td>25</td>
<td>Res0</td>
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<tr>
<td>24</td>
<td>Res0</td>
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<tr>
<td>23</td>
<td>Res0</td>
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<tr>
<td>22</td>
<td>Res0</td>
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<tr>
<td>21</td>
<td>Res0</td>
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<tr>
<td>20</td>
<td>Res0</td>
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<tr>
<td>19</td>
<td>Res0</td>
</tr>
<tr>
<td>18</td>
<td>Res0</td>
</tr>
<tr>
<td>17</td>
<td>Res0</td>
</tr>
<tr>
<td>16</td>
<td>Res0</td>
</tr>
<tr>
<td>15</td>
<td>Res0</td>
</tr>
<tr>
<td>14</td>
<td>Res0</td>
</tr>
<tr>
<td>13</td>
<td>Res0</td>
</tr>
<tr>
<td>12</td>
<td>Res0</td>
</tr>
<tr>
<td>11</td>
<td>Res0</td>
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<tr>
<td>10</td>
<td>Res0</td>
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<tr>
<td>9</td>
<td>Res0</td>
</tr>
<tr>
<td>8</td>
<td>Res0</td>
</tr>
<tr>
<td>7</td>
<td>Res0</td>
</tr>
<tr>
<td>6</td>
<td>Res0</td>
</tr>
<tr>
<td>5</td>
<td>Res0</td>
</tr>
<tr>
<td>4</td>
<td>Res0</td>
</tr>
<tr>
<td>3</td>
<td>Res0</td>
</tr>
<tr>
<td>2</td>
<td>Res0</td>
</tr>
<tr>
<td>1</td>
<td>Res0</td>
</tr>
<tr>
<td>0</td>
<td>Res0</td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

The value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>[7:1]</td>
<td>[0]</td>
<td>ggggggg.s</td>
</tr>
<tr>
<td>1</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>2</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>gggggg.sss</td>
</tr>
<tr>
<td>3</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>ggggg.ssss</td>
</tr>
<tr>
<td>4</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sssss</td>
</tr>
<tr>
<td>5</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>gg.sssssss</td>
</tr>
<tr>
<td>6</td>
<td>[7]</td>
<td>[6:0]</td>
<td>g.ssssssss</td>
</tr>
<tr>
<td>7</td>
<td>No preemption</td>
<td>[7:0]</td>
<td>sssssss</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ICV_BPR0_EL1**

The minimum binary point value is derived from the number of implemented preemption bits, as shown in the following table:
The number of implemented preemption bits is indicated by `ICH_VTR_EL2.PREbits`.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is `UNKNOWN`.

Accesses to this register use the following encodings:

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\text{0b11} & \text{0b000} & \text{0b1100} & \text{0b1000} & \text{0b011} \\
\hline
\end{array}
\]

if `PSTATE.EL == EL0` then
    UNDEFINED;
elsif `PSTATE.EL == EL1` then
    if `Halted()` \&\& `HaveEL(EL3)` \&\& `EDSCR.SDD == '1'` \&\& boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" \&\& `SCR_EL3.FIQ == '1'` then
        UNDEFINED;
    elsif `ICC_SRE_EL1.SRE == '0'` then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif `EL2Enabled()` \&\& `ICH_HCR_EL2.TALL0 == '1'` then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif `EL2Enabled()` \&\& `HCR_EL2.FMO == '1'` then
        return `ICV_BPR0_EL1`;
    elsif `HaveEL(EL3)` \&\& `SCR_EL3.FIQ == '1'` then
        if `Halted()` \&\& `EDSCR.SDD == '1'` then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return `ICC_BPR0_EL1`;
    end
elsif `PSTATE.EL == EL2` then
    if `Halted()` \&\& `HaveEL(EL3)` \&\& `EDSCR.SDD == '1'` \&\& boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" \&\& `SCR_EL3.FIQ == '1'` then
        UNDEFINED;
    elsif `ICC_SRE_EL2.SRE == '0'` then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif `HaveEL(EL3)` \&\& `SCR_EL3.FIQ == '1'` then
        if `Halted()` \&\& `EDSCR.SDD == '1'` then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return `ICC_BPR0_EL1`;
    end
elsif `PSTATE.EL == EL3` then
    if `ICC_SRE_EL3.SRE == '0'` then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return `ICC_BPR0_EL1`;
    end
else
    return `ICC_BPR0_EL1`;
end

MSR `ICC_BPR0_EL1`, `<Xt>`

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\text{0b11} & \text{0b000} & \text{0b1100} & \text{0b1000} & \text{0b011} \\
\hline
\end{array}
\]
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_BPR0_EL1 = X[t];
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_BPR0_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HCR_EL2.TALL0 == '1' then
    if ICC_BPR0_EL1 = X[t];
  elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_BPR0_EL1 = X[t];
else
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_BPR0_EL1 = X[t];
end
ICV_BPR1_EL1, Interrupt Controller Virtual Binary Point Register 1

The ICV_BPR1_EL1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines virtual Group 1 interrupt preemption.

**Configuration**

AArch64 System register ICV_BPR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_BPR1[31:0].

**Attributes**

ICV_BPR1_EL1 is a 64-bit register.

**Field descriptions**

The ICV_BPR1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-3</td>
<td>RES0</td>
</tr>
<tr>
<td>2-0</td>
<td>BinaryPoint</td>
</tr>
</tbody>
</table>

**Bits [63:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

If the GIC is configured to use separate binary point fields for virtual Group 0 and virtual Group 1 interrupts, the value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>1</td>
<td>[7:1]</td>
<td>[0]</td>
<td>ggggggg.s</td>
</tr>
<tr>
<td>2</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.sss</td>
</tr>
<tr>
<td>3</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>gggggg.sss</td>
</tr>
<tr>
<td>4</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>gggg.sssss</td>
</tr>
<tr>
<td>5</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sssssss</td>
</tr>
<tr>
<td>6</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>gg.sssssss</td>
</tr>
<tr>
<td>7</td>
<td>[7]</td>
<td>[6:0]</td>
<td>g.sssssssss</td>
</tr>
</tbody>
</table>

Writing 0 to this field will set this field to its reset value.

If ICV_CTLR_EL1_CBPR is set to 1, Non-secure EL1 reads return ICV_BPR0_EL1 + 1 saturated to 0b111. Non-secure EL1 writes are ignored.

If ICV_CTLR_EL1_CBPR is set to 1, Secure EL1 reads return ICV_BPR0_EL1. Secure EL1 writes modify ICV_BPR0_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the ICV_BPR1_EL1

For Non-secure writes, the minimum value of this field is the minimum value of ICH_VMCR_EL2.VBPR0 plus one.

For Secure writes, the minimum value of this field is the minimum value of ICH_VMCR_EL2.VBPR0.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is UNKNOWN.

Accesses to this register use the following encodings:

MRS <Xt>, ICC_BPR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_BPR1_EL1;
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_BPR1_EL1_S;
    else
      return ICC_BPR1_EL1_NS;
  else
    return ICC_BPR1_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_BPR1_EL1_S;
    else
      return ICC_BPR1_EL1_NS;
  else
    return ICC_BPR1_EL1;
  endif
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if SCR_EL3.NS == '0' then
      return ICC_BPR1_EL1_S;
    else
      return ICC_BPR1_EL1_NS;
  endif
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  if SCR_EL3.NS == '0' then
    ICC_BPR1_EL1_S = X[t];
  else
    ICC_BPR1_EL1_NS = X[t];
  endif
endif

if PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  if SCR_EL3.NS == '0' then
    ICC_BPR1_EL1_S = X[t];
  else
    ICC_BPR1_EL1_NS = X[t];
  endif
endif

if PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if SCR_EL3.NS == '0' then
      ICC_BPR1_EL1_S = X[t];
    else
      ICC_BPR1_EL1_NS = X[t];
    endif
  endif
else
  if SCR_EL3.NS == '0' then
    ICC_BPR1_EL1_S = X[t];
  else
    ICC_BPR1_EL1_NS = X[t];
  endif
endif
ICV_CTLR_EL1, Interrupt Controller Virtual Control Register

The ICV_CTLR_EL1 characteristics are:

**Purpose**

Controls aspects of the behavior of the GIC virtual CPU interface and provides information about the features implemented.

**Configuration**

AArch64 System register ICV_CTLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_CTLR[31:0].

**Attributes**

ICV_CTLR_EL1 is a 64-bit register.

**Field descriptions**

The ICV_CTLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>62</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>61</td>
<td><code>ExtRange</code></td>
</tr>
<tr>
<td>60</td>
<td><code>RSS</code></td>
</tr>
<tr>
<td>59</td>
<td><code>A3V</code></td>
</tr>
<tr>
<td>58</td>
<td><code>SEIS</code></td>
</tr>
<tr>
<td>57</td>
<td><code>IDbits</code></td>
</tr>
<tr>
<td>56</td>
<td><code>PRbits</code></td>
</tr>
<tr>
<td>55</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>54</td>
<td><code>EOImode</code></td>
</tr>
<tr>
<td>53</td>
<td><code>CBPR</code></td>
</tr>
<tr>
<td>52</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>51</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>50</td>
<td><code>RES0</code></td>
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<tr>
<td>49</td>
<td><code>RES0</code></td>
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<tr>
<td>48</td>
<td><code>RES0</code></td>
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<td>47</td>
<td><code>RES0</code></td>
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<td>46</td>
<td><code>RES0</code></td>
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<td>45</td>
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<td>43</td>
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<td><code>RES0</code></td>
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<td>39</td>
<td><code>RES0</code></td>
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<td>38</td>
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<td>37</td>
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<td>31</td>
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<tr>
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<td>15</td>
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<td>11</td>
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<td>10</td>
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<td>9</td>
<td><code>RES0</code></td>
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<td>8</td>
<td><code>RES0</code></td>
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<tr>
<td>7</td>
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</tr>
<tr>
<td>6</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>5</td>
<td><code>RES0</code></td>
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<tr>
<td>4</td>
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<td>3</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>2</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>1</td>
<td><code>RES0</code></td>
</tr>
<tr>
<td>0</td>
<td><code>RES0</code></td>
</tr>
</tbody>
</table>

**Bits [63:20]**

Reserved, RES0.

**ExtRange, bit [19]**

Extended INTID range (read-only).

<table>
<thead>
<tr>
<th>ExtRange</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0      | CPU interface does not support INTIDs in the range 1024..8191.  
- Behaviour is **UNPREDICTABLE** if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface.  
  
  **Note**  
  Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them. |
| 0b1      | CPU interface supports INTIDs in the range 1024..8191  
- All INTIDs in the range 1024..8191 are treated as requiring deactivation. |

ICV_CTLR_EL1.ExtRange is an alias of ICC_CTLR_EL1.ExtRange.

**RSS, bit [18]**

Range Selector Support. Possible values are:
Targeted SGIs with affinity level 0 values of 0 - 15 are supported.

Targeted SGIs with affinity level 0 values of 0 - 255 are supported.

This bit is read-only.

Bits [17:16]

Reserved, RES0.

A3V, bit [15]

Affinity 3 Valid. Read-only and writes are ignored. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

SEIS, bit [14]

SEI Support. Read-only and writes are ignored. Indicates whether the virtual CPU interface supports local generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic does not support local generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports local generation of SEIs.</td>
</tr>
</tbody>
</table>

IDbits, bits [13:11]

Identifier bits. Read-only and writes are ignored. The number of virtual interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

PRibits, bits [10:8]

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one. An implementation must implement at least 32 levels of physical priority (5 priority bits).

Note

This field always returns the number of priority bits implemented.

The division between group priority and subpriority is defined in the binary point registers ICV_BPR0_EL1 and ICV_BPR1_EL1.

Bits [7:2]

Reserved, RES0.

EOImode, bit [1]

Virtual EOI mode. Controls whether a write to an End of Interrupt register also deactivates the virtual interrupt:
**EOImode**

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 ICV_EOIR0_EL1 and ICV_EOIR1_EL1 provide both priority drop and interrupt deactivation functionality. Accesses to ICV_DIR_EL1 are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1 ICV_EOIR0_EL1 and ICV_EOIR1_EL1 provide priority drop functionality only. ICV_DIR_EL1 provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CBPR, bit [0]**

Common Binary Point Register. Controls whether the same register is used for interrupt preemption of both virtual Group 0 and virtual Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 ICV_BPR1_EL1 determines the preemption group for virtual Group 1 interrupts.</td>
<td></td>
</tr>
<tr>
<td>0b1 Reads of ICV_BPR1_EL1 return ICV_BPR0_EL1 plus one, saturated to 0b111. Writes to ICV_BPR1_EL1 are ignored.</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICV_CTLR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, ICC_CTLR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        return ICV_CTLR_EL1;
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        return ICV_CTLR_EL1;
    elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            return ICC_CTLR_EL1_S;
        else
            return ICC_CTLR_EL1_NS;
        end
    else
        return ICC_CTLR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            return ICC_CTLR_EL1_S;
        else
            return ICC_CTLR_EL1_NS;
        end
    else
        return ICC_CTLR_EL1;
    end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif SCR_EL3.NS == '0' then
        return ICC_CTLR_EL1_S;
    else
        return ICC_CTLR_EL1_NS;
    else
        return ICC_CTLR_EL1_NS;
    end

MSR ICC_CTLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>
| 0b11| 0b000| 0b1100  | 0b1100 | 0b100
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
elsif EL2Enabled() && ICH_HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_CTLR_EL1 = X[t];
elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    ICV_CTLR_EL1 = X[t];
elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
elsif HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      ICC_CTLR_EL1_S = X[t];
else
      ICC_CTLR_EL1_NS = X[t];
else
      ICC_CTLR_EL1 = X[t];
else
  AArch64.SystemAccessTrap(EL3, 0x18);
elsif ICC_SRE_EL2.SRE == '0' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch64.SystemAccessTrap(EL3, 0x18);
elsif HaveEL(EL3) then
  if SCR_EL3.NS == '0' then
    ICC_CTLR_EL1_S = X[t];
else
    ICC_CTLR_EL1_NS = X[t];
else
    ICC_CTLR_EL1 = X[t];
else
  ICC_CTLR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL2.SRE == '0' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
eselse
  AArch64.SystemAccessTrap(EL3, 0x18);
elsif ICC_SRE_EL3.SRE == '0' then
  AArch64.SystemAccessTrap(EL3, 0x18);
else
  if SCR_EL3.NS == '0' then
    ICC_CTLR_EL1_S = X[t];
eelse
    ICC_CTLR_EL1_NS = X[t];
ICV_DIR_EL1, Interrupt Controller Deactivate Virtual Interrupt Register

The ICV_DIR_EL1 characteristics are:

**Purpose**

When interrupt priority drop is separated from interrupt deactivation, a write to this register deactivates the specified virtual interrupt.

**Configuration**

AArch64 System register ICV_DIR_EL1 bits [31:0] performs the same function as AArch32 System register ICV_DIR[31:0].

**Attributes**

ICV_DIR_EL1 is a 64-bit register.

**Field descriptions**

The ICV_DIR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | RES0 | INTID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the virtual interrupt to be deactivated.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_DIR_EL1**

When EOiMode == 0, writes are ignored. In systems supporting system error generation, an implementation might generate an SEI.

Accesses to this register use the following encodings:

MSR ICC_DIR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
        && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TDIR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        ICV_DIR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        ICV_DIR_EL1 = X[t];
    elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ICC_DIR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
        && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        ICC_DIR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        ICC_DIR_EL1 = X[t];
    end
end
ICV_EOIR0_EL1, Interrupt Controller Virtual End Of Interrupt Register 0

The ICV_EOIR0_EL1 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified virtual Group 0 interrupt.

**Configuration**

AArch64 System register ICV_EOIR0_EL1 performs the same function as AArch32 System register ICV_EOIR0.

**Attributes**

ICV_EOIR0_EL1 is a 64-bit register.

**Field descriptions**

The ICV_EOIR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
</tr>
<tr>
<td>61</td>
<td>INTID</td>
</tr>
<tr>
<td>60</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>...</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICV_IAR0_EL1 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the ICV_CTLR.EOImode bit is 0, a write to this register drops the priority for the virtual interrupt, and also deactivates the virtual interrupt.

If the ICV_CTLR.EOImode bit is 1, a write to this register only drops the priority for the virtual interrupt. Software must write to ICV_DIR_EL1 to deactivate the virtual interrupt.

**Accessing the ICV_EOIR0_EL1**

A write to this register must correspond to the most recent valid read by this vPE from a Virtual Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICV_IAR0_EL1, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

Accesses to this register use the following encodings:

```
MSR ICC_EOIR0_EL1, <Xt>
```

```
op0 | op1 | CRn | CRm | op2
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elseif EL2Enabled() && HCR_EL2.TALL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && HCR_EL2.FM0 == '1' then
        ICC_EOIR0_EL1 = X[t];
    elseif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        ICC_EOIR0_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        ICC_EOIR0_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        ICC_EOIR0_EL1 = X[t];
    end
else
    ICC_EOIR0_EL1 = X[t];
end if

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ICV_EOIR1_EL1, Interrupt Controller Virtual End Of Interrupt Register 1

The ICV_EOIR1_EL1 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified virtual Group 1 interrupt.

**Configuration**

AArch64 System register ICV_EOIR1_EL1 performs the same function as AArch32 System register ICV_EOIR1.

**Attributes**

ICV_EOIR1_EL1 is a 64-bit register.

**Field descriptions**

The ICV_EOIR1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICV_IAR1_EL1 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the ICV_CTLR.EOImode bit is 0, a write to this register drops the priority for the virtual interrupt, and also deactivates the virtual interrupt.

If the ICV_CTLR.EOImode bit is 1, a write to this register only drops the priority for the virtual interrupt. Software must write to ICV_DIR_EL1 to deactivate the virtual interrupt.

**Accessing the ICV_EOIR1_EL1**

A write to this register must correspond to the most recent valid read by this vPE from a Virtual Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICV_IAR1_EL1, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

Accesses to this register use the following encodings:

MSR ICC_EOIR1_EL1, <Xt>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    ICV_EOIR1_EL1 = X[t];
  elsif ICC_HCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_EOIR1_EL1 = X[t];
else
  ICC_EOIR1_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_EOIR1_EL1 = X[t];
else
  ICC_EOIR1_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_EOIR1_EL1 = X[t];
ICV_HPPIR0_EL1, Interrupt Controller Virtual Highest Priority Pending Interrupt Register 0

The ICV_HPPIR0_EL1 characteristics are:

**Purpose**

Indicates the highest priority pending virtual Group 0 interrupt on the virtual CPU interface.

**Configuration**

AArch64 System register ICV_HPPIR0_EL1 performs the same function as AArch32 System register ICV_HPPIR0.

**Attributes**

ICV_HPPIR0_EL1 is a 64-bit register.

**Field descriptions**

The ICV_HPPIR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>RES0</td>
<td>RES0</td>
<td>INTID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
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<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
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<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending virtual interrupt.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_HPPIR0_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_HPPIR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.TALL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        return ICV_HPPIR0_EL1;
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return ICC_HPPIR0_EL1;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end if
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICC_HPPIR0_EL1;
    end if
The ICV_HPPIR1_EL1 characteristics are:

**Purpose**

Indicates the highest priority pending virtual Group 1 interrupt on the virtual CPU interface.

**Configuration**

AArch64 System register ICV_HPPIR1_EL1 performs the same function as AArch32 System register ICV_HPPIR1.

**Attributes**

ICV_HPPIR1_EL1 is a 64-bit register.

**Field descriptions**

The ICV_HPPIR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending virtual interrupt.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_HPPIR1_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_HPPIR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_HPPIR1_EL1;
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR1_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_HPPIR1_EL1;
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_HPPIR1_EL1;
end
ICV_IAR0_EL1, Interrupt Controller Virtual Interrupt Acknowledge Register 0

The ICV_IAR0_EL1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled virtual Group 0 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch64 System register ICV_IAR0_EL1 performs the same function as AArch32 System register ICV_IAR0.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_IAR0_EL1 is a 64-bit register.

**Field descriptions**

The ICV_IAR0_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RES0 | RES0 | INTID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled virtual interrupt.

This is the INTID of the highest priority pending virtual interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_IAR0_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, ICC_IAR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICV_IAR0_EL1;
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_IAR0_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return ICC_IAR0_EL1;
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_IAR0_EL1;
  end
ICV_IAR1_EL1, Interrupt Controller Virtual Interrupt Acknowledge Register 1

The ICV_IAR1_EL1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled virtual Group 1 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch64 System register ICV_IAR1_EL1 performs the same function as AArch32 System register ICV_IAR1.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see ‘Observability of the effects of accesses to the GIC registers’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_IAR1_EL1 is a 64-bit register.

**Field descriptions**

The ICV_IAR1_EL1 bit assignments are:

<p>| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|</p>
<table>
<thead>
<tr>
<th>RES0</th>
<th>RES0</th>
<th>INTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled virtual interrupt.

This is the INTID of the highest priority pending virtual interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_EL1.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_IAR1_EL1**

Accesses to this register use the following encodings:
### MRS <Xt>, ICC_IAR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && HCR_EL2.TALL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.IMO == '1' then
        return ICV_IAR1_EL1;
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return ICC_IAR1_EL1;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return ICC_IAR1_EL1;
    end if
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        return ICC_IAR1_EL1;
    end if
```

---

**ICV_IAR1_EL1, Interrupt Controller Virtual Interrupt Acknowledge Register 1**

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ICV_IGRPEN0_EL1, Interrupt Controller Virtual Interrupt Group 0 Enable register

The ICV_IGRPEN0_EL1 characteristics are:

**Purpose**

Controls whether virtual Group 0 interrupts are enabled or not.

**Configuration**

AArch64 System register ICV_IGRPEN0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_IGRPEN0[31:0].

**Attributes**

ICV_IGRPEN0_EL1 is a 64-bit register.

**Field descriptions**

The ICV_IGRPEN0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Enable</td>
</tr>
<tr>
<td>0</td>
<td>Virtual Group 0 interrupts are enabled.</td>
</tr>
<tr>
<td>0</td>
<td>Virtual Group 0 interrupts are disabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICV_IGRPEN0_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.ICC_IGRPENn_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FMO == '1' then
        return ICV_IGRPEN0_EL1;
    elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return ICC_IGRPEN0_EL1;
        end
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
            UNDEFINED;
        elsif ICC_SRE_EL2.SRE == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                return ICV_IGRPEN0_EL1;
            end
        elsif PSTATE.EL == EL3 then
            if ICC_SRE_EL3.SRE == '0' then
                AArch64.SystemAccessTrap(EL3, 0x18);
            else
                return ICC_IGRPEN0_EL1;
            end
        elsif PSTATE.EL == EL4 then
            if ICC_SRE_EL4.SRE == '0' then
                AArch64.SystemAccessTrap(EL4, 0x18);
            else
                return ICC_IGRPEN0_EL1;
            end
        else
            return ICC_IGRPEN0_EL1;
        end
    else
        return ICC_IGRPEN0_EL1;
    end
end

MSR ICC_IGRPEN0_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ICC_IGRPEn_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_IGRPEN0_EL1 = X[t];
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_IGRPEN0_EL1 = X[t];
  end
else
  ICC_IGRPEN0_EL1 = X[t];
endif

if PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_IGRPEN0_EL1 = X[t];
  endif
else
  ICC_IGRPEN0_EL1 = X[t];
endif

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ICV_IGRPEN1_EL1, Interrupt Controller Virtual Interrupt Group 1 Enable register

The ICV_IGRPEN1_EL1 characteristics are:

**Purpose**

Controls whether virtual Group 1 interrupts are enabled for the current Security state.

**Configuration**

AArch64 System register ICV_IGRPEN1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_IGRPEN1[31:0].

**Attributes**

ICV_IGRPEN1_EL1 is a 64-bit register.

**Field descriptions**

The ICV_IGRPEN1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Enable</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:1]**

Reserved, RES0.

**Enable, bit [0]**

Enables virtual Group 1 interrupts.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ICV_IGRPEN1_EL1**

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ ICV_IGRPEN1_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    elsif ICC_SRE_EL1.SRE == '0' then
        AArch64.SystemAccessTrap(EL1, 0x18);
    end
else
    return ICC_IGRPEN1_EL1;
end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif ICC_SRE_EL2.SRE == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    end
else
    return ICC_IGRPEN1_EL1;
end
elsif PSTATE.EL == EL3 then
    if ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    elsif ICC_SRE_EL3.SRE == '0' then
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
else
    return ICC_IGRPEN1_EL1;
end
else
    return ICC_IGRPEN1_EL1;
end

ICV_IGRPEN1_EL1, Interrupt Controller Virtual Interrupt Group 1 Enable register

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.ICC_IGRPEN_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    ICV_IGRPEN1_EL1 = X[t];
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif ICC_IGRPEN1_EL1 == '1' then
    if SCR_EL3.FGTEn == '1' && SCR_EL3.IRQ == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif SCR_EL3.NS == '0' then
    ICC_IGRPEN1_EL1_S = X[t];
  else
    ICC_IGRPEN1_EL1_NS = X[t];
  else
    ICC_IGRPEN1_EL1 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif ICC_IGRPEN1_EL1 == '1' then
    if SCR_EL3.FGTEn == '1' && SCR_EL3.IRQ == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif SCR_EL3.NS == '0' then
    ICC_IGRPEN1_EL1_S = X[t];
  else
    ICC_IGRPEN1_EL1_NS = X[t];
  else
    ICC_IGRPEN1_EL1 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if SCR_EL3.FGTEn == '1' && SCR_EL3.IRQ == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  end if
else
  ICC_IGRPEN1_EL1_S = X[t];
else
  ICC_IGRPEN1_EL1_NS = X[t];
The ICV_PMR_EL1 characteristics are:

**Purpose**

Provides a virtual interrupt priority filter. Only virtual interrupts with a higher priority than the value in this register are signaled to the PE.

**Configuration**

AArch64 System register ICV_PMR_EL1 bits [31:0] are architecturally mapped to AArch32 System register ICV_PMR[31:0].

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that writes to this register are self-synchronising. This ensures that no interrupts below the written PMR value will be taken after a write to this register is architecturally executed. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_PMR_EL1 is a 64-bit register.

**Field descriptions**

The ICV_PMR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:8]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Priority, bits [7:0]</td>
<td>The priority mask level for the virtual CPU interface. If the priority of a virtual interrupt is higher than the value indicated by this field, the interface signals the virtual interrupt to the PE.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Implemented priority bits</th>
<th>Possible priority field values</th>
<th>Number of priority levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>0x00-0xFF (0-255), all values</td>
<td>256</td>
</tr>
<tr>
<td>[7:1]</td>
<td>0x00-0xFE (0-254), even values only</td>
<td>128</td>
</tr>
<tr>
<td>[7:2]</td>
<td>0x00-0xFC (0-252), in steps of 4</td>
<td>64</td>
</tr>
<tr>
<td>[7:3]</td>
<td>0x00-0xF8 (0-248), in steps of 8</td>
<td>32</td>
</tr>
<tr>
<td>[7:4]</td>
<td>0x00-0xF0 (0-240), in steps of 16</td>
<td>16</td>
</tr>
</tbody>
</table>
Unimplemented priority bits are RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICV_PMR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ICC_PMR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    return ICV_PMR_EL1;
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    return ICV_PMR_EL1;
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end else
  return ICC_PMR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end else
  return ICC_PMR_EL1;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return ICC_PMR_EL1;
  end if

MSR ICC_PMR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL1.SRE == '0' then
    AArch64.SystemAccessTrap(EL1, 0x18);
  elsif EL2Enabled() && ICH_HCR_EL2.TC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FMO == '1' then
    ICV_PMR_EL1 = X[t];
  elsif EL2Enabled() && HCR_EL2.IMO == '1' then
    ICV_PMR_EL1 = X[t];
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_PMR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE_EL2.SRE == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    ICC_PMR_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    ICC_PMR_EL1 = X[t];
ICV_RPR_EL1, Interrupt Controller Virtual Running Priority Register

The ICV_RPR_EL1 characteristics are:

**Purpose**

Indicates the Running priority of the virtual CPU interface.

**Configuration**

AArch64 System register ICV_RPR_EL1 performs the same function as AArch32 System register ICV_RPR.

**Attributes**

ICV_RPR_EL1 is a 64-bit register.

**Field descriptions**

The ICV_RPR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0-62</td>
<td>Priority</td>
<td>The current running priority on the virtual CPU interface. This is the group priority of the current active virtual interrupt. If there are no active interrupts on the virtual CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority. The priority returned is the group priority as if the BPR for the current Exception level and Security state was set to the minimum value of BPR for the number of implemented priority bits.</td>
</tr>
</tbody>
</table>

**Bits [63:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The current running priority on the virtual CPU interface. This is the group priority of the current active virtual interrupt.

If there are no active interrupts on the virtual CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

The priority returned is the group priority as if the BPR for the current Exception level and Security state was set to the minimum value of BPR for the number of implemented priority bits.

**Note**

If 8 bits of priority are implemented the group priority is bits[7:1] of the priority.

**Accessing the ICV_RPR_EL1**

If there are no active interrupts on the virtual CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

Software cannot determine the number of implemented priority bits from a read of this register.

Accesses to this register use the following encodings:
MRS <Xt>, ICC_RPR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && ESCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL1.SRE == '0' then
  AArch64.SystemAccessTrap(EL1, 0x18);
elsif EL2Enabled() && HCR_EL2.TC == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.IMO == '1' then
  return ICC_RPR_EL1;
elsif EL2Enabled() && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && ESCR.SDD == '1' then
    UNDEFINED;
  else
    return ICC_RPR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && ESCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_SRE_EL2.SRE == '0' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && ESCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
else
  return ICC_RPR_EL1;
elsif PSTATE.EL == EL3 then
  if ICC_SRE_EL3.SRE == '0' then
    AArch64.SystemAccessTrap(EL3, 0x18);
else
  return ICC_RPR_EL1;

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The ID_AA64AFR0_EL1 characteristics are:

**Purpose**

Provides information about the `IMPLEMENTATION DEFINED` features of the PE in AArch64 state.

For general information about the interpretation of the ID registers, see ‘Principles of the ID scheme for fields in ID registers’.

**Configuration**

There are no configuration notes.

**Attributes**

ID_AA64AFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64AFR0_EL1 bit assignments are:

```
       Bits [63:32]  
0   63  62  61  60  59  58  57  56  55  54  53  52  51  50  49  48  47  46  45  44  43  42  41  40  39  38  37  36  35  34  33  32  31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0  
RES0 `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` `IMPLEMENTATION DEFINED` 
```

**Bits [63:32]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [31:28]**

`IMPLEMENTATION DEFINED`.

**IMPLEMENTATION DEFINED, bits [27:24]**

`IMPLEMENTATION DEFINED`.

**IMPLEMENTATION DEFINED, bits [23:20]**

`IMPLEMENTATION DEFINED`.

**IMPLEMENTATION DEFINED, bits [19:16]**

`IMPLEMENTATION DEFINED`.

**IMPLEMENTATION DEFINED, bits [15:12]**

`IMPLEMENTATION DEFINED`. 
IMPLEMENTATION DEFINED, bits [11:8]

IMPLEMENTATION DEFINED.

IMPLEMENTATION DEFINED, bits [7:4]

IMPLEMENTATION DEFINED.

IMPLEMENTATION DEFINED, bits [3:0]

IMPLEMENTATION DEFINED.

Accessing the ID_AA64AFR0_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_AA64AFR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0101</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64AFR0_EL1;
elsif PSTATE.EL == EL2 then
  return ID_AA64AFR0_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64AFR0_EL1;
The ID_AA64AFR1_EL1 characteristics are:

### Purpose

Reserved for future expansion of information about the IMPLEMENTATION DEFINED features of the PE in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

### Configuration

There are no configuration notes.

### Attributes

ID_AA64AFR1_EL1 is a 64-bit register.

### Field descriptions

The ID_AA64AFR1_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

### Bits [63:0]

Reserved, RES0.

### Accessing the ID_AA64AFR1_EL1

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{ID\_AA64AFR1\_EL1}
\]

<table>
<thead>
<tr>
<th>(op0)</th>
<th>(op1)</th>
<th>(CRn)</th>
<th>(CRm)</th>
<th>(op2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(Feat_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_AA64AFR1_EL1;
elsif PSTATE.EL == EL2 then
    return ID_AA64AFR1_EL1;
elsif PSTATE.EL == EL3 then
    return ID_AA64AFR1_EL1;
The ID_AA64DFR0_EL1 characteristics are:

**Purpose**

Provides top level information about the debug system in AArch64 state.

For general information about the interpretation of the ID registers, see Principles of the ID scheme for fields in ID registers.

**Configuration**

The external register EDDFR gives information from this register.

**Attributes**

ID_AA64DFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64DFR0_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | MTPMU | RES0 | TraceFilt | DoubleLock | PMSVer |
| CTX_CMPs | RES0 | WRPs | RES0 | BRPs | PMUVer | TraceVer | DebugVer |

**Bits [63:52]**

Reserved, RES0.

**MTPMU, bits [51:48]**

Multi-threaded PMU extension. Defined values are:

<table>
<thead>
<tr>
<th>MTPMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, it is IMPLEMENTATION DEFINED whether PMEVTYPE&lt;n&gt;_EL0_MT and PMEVTYPE&lt;n&gt;_MT are read/write or RES0.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_MTPMU and FEAT_PMUv3 implemented. PMEVTYPE&lt;n&gt;_EL0_MT and PMEVTYPE&lt;n&gt;_MT are read/write. When FEAT_MTPMU is disabled, the Effective values of PMEVTYPE&lt;n&gt;_EL0_MT and PMEVTYPE&lt;n&gt;_MT are 0.</td>
</tr>
<tr>
<td>0b1111</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, PMEVTYPE&lt;n&gt;_EL0_MT and PMEVTYPE&lt;n&gt;_MT are RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_MTPMU implements the functionality identified by the value 0b0001.

From Armv8.6, in an implementation that includes FEAT_PMUv3, the value 0b0000 is not permitted.

In an implementation that does not include FEAT_PMUv3, the value 0b0001 is not permitted.
Bits [47:44]

Reserved, RES0.

**TraceFilt, bits [43:40]**

Armv8.4 Self-hosted Trace Extension version. Defined values are:

<table>
<thead>
<tr>
<th>TraceFilt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Armv8.4 Self-hosted Trace Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Armv8.4 Self-hosted Trace Extension implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TRF implements the functionality identified by the value 0b0001.

From Armv8.4, if an Embedded Trace Macrocell Architecture PE Trace Unit is implemented, the value 0b0000 is not permitted.

**DoubleLock, bits [39:36]**

OS Double Lock implemented. Defined values are:

<table>
<thead>
<tr>
<th>DoubleLock</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>OS Double Lock implemented. OSDLR_EL1 is RW.</td>
</tr>
<tr>
<td>0b1111</td>
<td>OS Double Lock not implemented. OSDLR_EL1 is RAZ/WI.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DoubleLock implements the functionality identified by the value 0b0000.

In Armv8.0, the only permitted value is 0b0000.

If FEAT_Debugv8p2 is implemented and FEAT_DoPD is not implemented, the permitted values are 0b0000 and 0b1111.

If FEAT_DoPD is implemented, the only permitted value is 0b1111.

**PMSVer, bits [35:32]**

Statistical Profiling Extension version. Defined values are:

<table>
<thead>
<tr>
<th>PMSVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Statistical Profiling Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Statistical Profiling Extension implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Support for the Event packet Alignment flag.</td>
</tr>
<tr>
<td></td>
<td>• If FEAT_SVE is implemented, support for the Scalable Vector extensions to Statistical Profiling.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• The last branch target Address packet.</td>
</tr>
<tr>
<td></td>
<td>• Discard mode.</td>
</tr>
<tr>
<td></td>
<td>• Extended event filtering, including the PMSNEVFR_EL1 System register.</td>
</tr>
<tr>
<td></td>
<td>• If FEAT_PMUv3 is implemented, controls to freeze the PMU event counters after an SPE buffer management event occurs.</td>
</tr>
<tr>
<td></td>
<td>• If FEAT_PMUv3 is implemented, the SAMPLE_FEED_BR,</td>
</tr>
<tr>
<td></td>
<td>SAMPLE_FEED_EVENT, SAMPLE_FEED_LAT,</td>
</tr>
<tr>
<td></td>
<td>SAMPLE_FEED_LD, SAMPLE_FEED_OP, and</td>
</tr>
<tr>
<td></td>
<td>SAMPLE_FEED_ST PMU events.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SPE implements the functionality identified by the value 0b0001.

FEAT_SPEv1p1 implements the functionality identified by the value 0b0010.
FEAT_SPEv1p2 implements the functionality identified by the value 0b0011.

In Armv8.5, if FEAT_SPE is implemented, the value 0b0001 is not permitted.

From Armv8.7, if FEAT_SPE is implemented, the value 0b0010 is not permitted.

**CTX_CMPs, bits [31:28]**

Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.

**Bits [27:24]**

Reserved, RES0.

**WRPs, bits [23:20]**

Number of watchpoints, minus 1. The value of 0b0000 is reserved.

**Bits [19:16]**

Reserved, RES0.

**BRPs, bits [15:12]**

Number of breakpoints, minus 1. The value of 0b0000 is reserved.

**PMU Ver, bits [11:8]**

Performance Monitors Extension version.

This field does not follow the standard ID scheme, but uses the alternative ID scheme described in 'Alternative ID scheme used for the Performance Monitors Extension version'

Defined values are:

<table>
<thead>
<tr>
<th>PMUVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Performance Monitors Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Performance Monitors Extension, PMUv3 implemented.</td>
</tr>
<tr>
<td>0b0100</td>
<td>PMUv3 for Armv8.1. As 0b0001, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• Extended 16-bit PMEVTYPE&lt;\n&gt;_{EL0}.evtCount field.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the MDCR_EL2.HPMD control bit.</td>
</tr>
<tr>
<td>0b0101</td>
<td>PMUv3 for Armv8.4. As 0b0100, and also includes support for the PMMIR_EL1 registers.</td>
</tr>
<tr>
<td>0b0110</td>
<td>PMUv3 for Armv8.5. As 0b0101, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• 64-bit event counters.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the MDCR_EL2.HCCD control bit.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.SCCD control bit.</td>
</tr>
<tr>
<td>0b0111</td>
<td>PMUv3 for Armv8.7. As 0b0110, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• The PMCR_EL0.FZO and, if EL2 is implemented, MDCR_EL2.HPMFZO control bits.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.{MPMX,MCCD} control bits.</td>
</tr>
<tr>
<td>0b1111</td>
<td>IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. Arm does not recommend this value for new implementations.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PMUv3 implements the functionality identified by the value 0b0001.
FEAT_PMUv3p1 implements the functionality identified by the value 0b0100.

FEAT_PMUv3p4 implements the functionality identified by the value 0b0101.

FEAT_PMUv3p5 implements the functionality identified by the value 0b0110.

FEAT_PMUv3p7 implements the functionality identified by the value 0b0111.

In Armv8.1, if FEAT_PMUv3 is implemented, the value 0b0001 is not permitted.

In Armv8.4, if FEAT_PMUv3 is implemented, the value 0b0100 is not permitted.

In Armv8.5, if FEAT_PMUv3 is implemented, the value 0b0101 is not permitted.

From Armv8.7, if FEAT_PMUv3 is implemented, the value 0b0110 is not permitted.

**TraceVer, bits [7:4]**

Trace support. Indicates whether System register interface to a PE trace unit is implemented. Defined values are:

<table>
<thead>
<tr>
<th>TraceVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PE trace unit System registers not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PE trace unit System registers implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

See the ETM Architecture Specification for more information.

A value of 0b0000 only indicates that no System register interface to a PE trace unit is implemented. A PE trace unit might nevertheless be implemented without a System register interface.

**DebugVer, bits [3:0]**

Debug architecture version. Indicates presence of Armv8 debug architecture. Defined values are:

<table>
<thead>
<tr>
<th>DebugVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0110</td>
<td>Armv8 debug architecture.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv8 debug architecture with Virtualization Host Extensions.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Armv8.2 debug architecture.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Armv8.4 debug architecture.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_Debugv8p2 adds the functionality identified by the value 0b1000.

FEAT_Debugv8p4 adds the functionality identified by the value 0b1001.

In Armv8.1, the value 0b0110 is not permitted.

In Armv8.2, the value 0b0111 is not permitted.

From Armv8.4, the value 0b1000 is not permitted.

**Accessing the ID_AA64DFR0_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, ID_AA64DFR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0101</td>
<td>0b00</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_AA64DFR0_EL1;
elsif PSTATE.EL == EL2 then
    return ID_AA64DFR0_EL1;
elsif PSTATE.EL == EL3 then
    return ID_AA64DFR0_EL1;
ID_AA64DFR1_EL1, AArch64 Debug Feature Register 1

The ID_AA64DFR1_EL1 characteristics are:

Purpose

Reserved for future expansion of top level information about the debug system in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

Configuration

There are no configuration notes.

Attributes

ID_AA64DFR1_EL1 is a 64-bit register.

Field descriptions

The ID_AA64DFR1_EL1 bit assignments are:

Accessing the ID_AA64DFR1_EL1

Accesses to this register use the following encodings:

```
MRS <Xt>, ID_AA64DFR1_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_AA64DFR1_EL1;
    end if
elsif PSTATE.EL == EL2 then
    return ID_AA64DFR1_EL1;
elsif PSTATE.EL == EL3 then
    return ID_AA64DFR1_EL1;
The ID_AA64ISAR0_EL1 characteristics are:

**Purpose**

Provides information about the instructions implemented in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

There are no configuration notes.

**Attributes**

ID_AA64ISAR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64ISAR0_EL1 bit assignments are:

| Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  | Bit  |
|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
| 63   | 62   | 61   | 60   | 59   | 58   | 57   | 56   | 55   | 54   | 53   | 52   | 51   | 50   | 49   | 48   | 47   | 46   | 45   | 44   | 43   | 42   | 41   | 40   | 39   | 38   | 37   | 36   | 35   | 34   | 33   | 32   |
| RNDR | TLB  | TS   | FHM  | DP   | SM4  | SM3  | SHA3 | RDM  | RES0 | Atomic| CRC32 | SHA2  | SHA1  | AES  | RES0 |

**RNDR, bits [63:60]**

Indicates support for Random Number instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>RNDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No Random Number instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>RNDR and RNDRRS registers are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RNG implements the functionality identified by the value 0b0001.

From Armv8.5, the permitted values are 0b0000 and 0b0001.

**TLB, bits [59:56]**

Indicates support for Outer shareable and TLB range maintenance instructions. Defined values are:

<table>
<thead>
<tr>
<th>TLB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Outer shareable and TLB range maintenance instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Outer shareable TLB maintenance instructions are implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Outer shareable and TLB range maintenance instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TLBIOS implements the functionality identified by the values 0b0001 and 0b0010.
FEAT_TLBIRANGE implements the functionality identified by the value 0b0010.

From Armv8.4, the only permitted value is 0b0010.

**TS, bits [55:52]**

Indicates support for flag manipulation instructions. Defined values are:

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No flag manipulation instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CFINV, RMIF, SETF16, and SETF8 instructions are implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>CFINV, RMIF, SETF16, SETF8, AXFLAG, and XAFLAG instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FlagM implements the functionality identified by the value 0b0001.

FEAT_FlagM2 implements the functionality identified by the value 0b0010.

In Armv8.2, the permitted values are 0b0000 and 0b0001.

In Armv8.4, the only permitted value is 0b0001.

From Armv8.5, the only permitted value is 0b0010.

**FHM, bits [51:48]**

Indicates support for FMLAL and FMLSL instructions. Defined values are:

<table>
<thead>
<tr>
<th>FHM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FMLAL and FMLSL instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FMLAL and FMLSL instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FHM implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

**DP, bits [47:44]**

Indicates support for Dot Product instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No Dot Product instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>UDOT and SDOT instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DotProd implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

**SM4, bits [43:40]**

Indicates support for SM4 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SM4</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SM4 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SM4E and SM4EKEY instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If FEAT_SM4 is not implemented, the value 0b0001 is reserved.
From Armv8.2, the permitted values are 0b0000 and 0b0001.

This field must have the same value as ID_AA64ISAR0_EL1.SM3.

**SM3, bits [39:36]**

Indicates support for SM3 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SM3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SM3 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SM3SS1, SM3TT1A, SM3TT1B, SM3TT2A, SM3TT2B, SM3PARTW1, and SM3PARTW2 instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If FEAT_SM3 is not implemented, the value 0b0001 is reserved.

FEAT_SM3 implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

This field must have the same value as ID_AA64ISAR0_EL1.SM4.

**SHA3, bits [35:32]**

Indicates support for SHA3 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SHA3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA3 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EOR3, RAX1, XAR, and BCAX instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If FEAT_SHA3 is not implemented, the value 0b0001 is reserved.

FEAT_SHA3 implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

If the value of ID_AA64ISAR0_EL1.SHA1 is 0b0000, this field must have the value 0b0000.

If the value of this field is 0b0001, ID_AA64ISAR0_EL1.SHA2 must have the value 0b0010.

**RDM, bits [31:28]**

Indicates support for SQRDMLAH and SQRDMLSH instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>RDM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No RDMA instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SQRDMLAH and SQRDMLSH instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RDM implements the functionality identified by the value 0b0001.

From Armv8.1, the only permitted value is 0b0001.

**Bits [27:24]**

Reserved, RES0.

**Atomic, bits [23:20]**

Indicates support for Atomic instructions in AArch64 state. Defined values are:
Atomic

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
</tr>
<tr>
<td>No Atomic instructions implemented.</td>
</tr>
<tr>
<td>0b0010</td>
</tr>
<tr>
<td>LDADD, LDCLR, LDOR, LDSET, LDSMAX, LDSMIN, LDUMAX, LDUMIN, CAS, CASP, and SWP instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LSE implements the functionality identified by the value 0b0010.

From Armv8.1, the only permitted value is 0b0010.

CRC32, bits [19:16]

Indicates support for CRC32 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>CRC32</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No CRC32 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CRC32B, CRC32H, CRC32W, CRC32X, CRC32CB, CRC32CH, CRC32CW, and CRC32CX instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.1, the only permitted value is 0b0001.

SHA2, bits [15:12]

Indicates support for SHA2 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SHA2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA2 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implements instructions: SHA256H, SHA256H2, SHA256SU0, and SHA256SU1.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Implements instructions:</td>
</tr>
<tr>
<td></td>
<td>• SHA256H, SHA256H2, SHA256SU0, and SHA256SU1.</td>
</tr>
<tr>
<td></td>
<td>• SHA512H, SHA512H2, SHA512SU0, and SHA512SU1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SHA256 implements the functionality identified by the value 0b0001.

FEAT_SHA512 implements the functionality identified by the value 0b0010.

In Armv8, the permitted values are 0b0000 and 0b0001.

From Armv8.2, the permitted values are 0b0000, 0b0001, and 0b0010.

If the value of ID_AA64ISAR0_EL1.SHA1 is 0b0000, this field must have the value 0b0000.

If the value of this field is 0b0010, ID_AA64ISAR0_EL1.SHA3 must have the value 0b0001.

SHA1, bits [11:8]

Indicates support for SHA1 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SHA1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA1 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SHA1 implements the functionality identified by the value 0b0001.

From Armv8, the permitted values are 0b0000 and 0b0001.
If the value of ID_AA64ISAR0_EL1.SHA2 is 0b0000, this field must have the value 0b0000.

**AES, bits [7:4]**

Indicates support for AES instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>AES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No AES instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AESE, AESD, AESMC, and AESIMC instructions implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, plus PMULL/PMULL2 instructions operating on 64-bit data quantities.</td>
</tr>
</tbody>
</table>

FEAT_AES implements the functionality identified by the value 0b0001.

FEAT_PMULL implements the functionality identified by the value 0b0010.

All other values are reserved.

From Armv8, the permitted values are 0b0000 and 0b0010.

**Bits [3:0]**

Reserved, RES0.

**Accessing the ID_AA64ISAR0_EL1**

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, ID_AA64ISAR0_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b0000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64ISAR0_EL1;
elsif PSTATE.EL == EL2 then
  return ID_AA64ISAR0_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64ISAR0_EL1;
ID_AA64ISAR1_EL1, AArch64 Instruction Set Attribute Register 1

The ID_AA64ISAR1_EL1 characteristics are:

**Purpose**

Provides information about the features and instructions implemented in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

If ID_AA64ISAR1_EL1.{API, APA} == {0000, 0000}, then:

- The TCR_EL1.{TBID,TBID0}, TCR_EL2.{TBID0,TBID1}, TCR_EL3.TBID and TCR_EL3.TBID bits are **RES0**.
- APIAKeyHi_EL1, APIAKeyLo_EL1, APIBKeyHi_EL1, APIBKeyLo_EL1, APDKeyHi_EL1, APDKeyLo_EL1, APDBKeyHi_EL1, APDBKeyLo_EL1 are not allocated.
- SCTLR_ELx.EnIA, SCTLR_ELx.EnIB, SCTLR_ELx.EnDA, SCTLR_ELx.EnDB are all **RES0**.

If ID_AA64ISAR1_EL1.{GPI, GPA, API, APA} == {0000, 0000, 0000, 0000}, then:

- HCR_EL2.APK and HCR_EL2.API are **RES0**.
- SCR_EL3.APK and SCR_EL3.API are **RES0**.

**Attributes**

ID_AA64ISAR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64ISAR1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>LS64</th>
<th>XS</th>
<th>I8MM</th>
<th>DGH</th>
<th>BF16</th>
<th>SPECRES</th>
<th>SB</th>
<th>FRINTTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>GPI</td>
<td>GPA</td>
<td>LRPMC</td>
<td>FCMA</td>
<td>JSCVT</td>
<td>API</td>
<td>APA</td>
<td>DPB</td>
</tr>
</tbody>
</table>

**LS64, bits [63:60]**

Indicates support for LD64B and ST64B* instructions, and the **ACCDATA_EL1** register. Defined values of this field are:

<table>
<thead>
<tr>
<th>LS64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>The LD64B and ST64B* instructions, the <strong>ACCDATA_EL1</strong> register, and associated traps are not supported.</td>
</tr>
<tr>
<td>000001</td>
<td>The LD64B and ST64B instructions are supported.</td>
</tr>
<tr>
<td>000010</td>
<td>The LD64B, ST64B, and ST64BV instructions, and their associated traps are supported.</td>
</tr>
<tr>
<td>000011</td>
<td>The LD64 and ST64B* instructions, the <strong>ACCDATA_EL1</strong> register, and their associated traps are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LS64 implements the functionality identified by 0b0001.

FEAT_LS64_V implements the functionality identified by 0b0010.

FEAT_LS64_ACCDATA implements the functionality identified by 0b0011.
From Armv8.7, the permitted values are 0b0000, 0b0010, and 0b0011.

**XS, bits [59:56]**

Indicates support for the XS attribute, the TLBI and DSB instructions with the nXS qualifier, and the HCRX_EL2.\{FGtnXS, FnXS\} fields in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>XS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The XS attribute, the TLBI and DSB instructions with the nXS qualifier, and the HCRX_EL2.{FGtnXS, FnXS} fields are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The XS attribute, the TLBI and DSB instructions with the nXS qualifier, and the HCRX_EL2.{FGtnXS, FnXS} fields are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_XS implements the functionality identified by 0b0001.

From Armv8.7, the only permitted value is 0b0001.

**I8MM, bits [55:52]**

Indicates support for Advanced SIMD and Floating-point Int8 matrix multiplication instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>I8MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Int8 matrix multiplication instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SMMLA, SUDOT, UMMLA, USMMLA, and USDOT instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_I8MM implements the functionality identified by 0b0001.

When Advanced SIMD and SVE are both implemented, this field must return the same value as ID_AA64ZFR0_EL1.I8MM.

From Armv8.6, the only permitted value is 0b0001.

**DGH, bits [51:48]**

Indicates support for the Data Gathering Hint instruction. Defined values are:

<table>
<thead>
<tr>
<th>DGH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Data Gathering Hint is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Data Gathering Hint is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DGH implements the functionality identified by 0b0001.

From ARMv8.0, the permitted values are 0b0000 and 0b0001.

If the DGH instruction has no effect in preventing the merging of memory accesses, the value of this field is 0b0000.

**BF16, bits [47:44]**

Indicates support for Advanced SIMD and Floating-point BFloat16 instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>BF16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>BFloat16 instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>BFCVT, BFCVTN, BFCVTN2, BFDOT, BFMLALB, BFMLALT, and BFMLA instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.
FEAT_BF16 implements the functionality identified by 0b0001.

When Advanced SIMD and SVE are both implemented, this field must return the same value as ID_AA64ZFR0_EL1.BF16.

From Armv8.6, the only permitted value is 0b0001.

**SPECRES, bits [43:40]**

Indicates support for prediction invalidation instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SPECRES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>CFP RCTX, DVP RCTX, and CPP RCTX instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CFP RCTX, DVP RCTX, and CPP RCTX instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SPECRES implements the functionality identified by 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**SB, bits [39:36]**

Indicates support for SB instruction in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SB instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SB instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SB implements the functionality identified by 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**FRINTTS, bits [35:32]**

Indicates support for the FRINT32Z, FRINT32X, FRINT64Z, and FRINT64X instructions are implemented. Defined values are:

<table>
<thead>
<tr>
<th>FRINTTS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FRINT32Z, FRINT32X, FRINT64Z, and FRINT64X instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FRINT32Z, FRINT32X, FRINT64Z, and FRINT64X instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FRINTTS implements the functionality identified by 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**GPI, bits [31:28]**

Indicates support for an IMPLEMENTATION DEFINED algorithm is implemented in the PE for generic code authentication in AArch64 state. Defined values are:
**GPI**, bits [27:24]

Indicates whether QARMA or Architected algorithm is implemented in the PE for generic code authentication in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>GPA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Generic Authentication using an Architected algorithm is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Generic Authentication using the QARMA algorithm is implemented. This includes the PACGA instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

If the value of ID_AA64ISAR1_EL1.GPA is non-zero, this field must have the value 0b0000.

**LRCPC**, bits [23:20]

Indicates support for weaker release consistency, RCpc, based model. Defined values are:

<table>
<thead>
<tr>
<th>LRCPC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The LDAPR*, LDAPUR*, and STLUR* instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The LDAPR* instructions are implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>The LDAPR*, LDAPUR*, and STLUR* instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

If the value of ID_AA64ISAR1_EL1.GPI is non-zero, this field must have the value 0b0000.

**FCMA**, bits [19:16]

Indicates support for complex number addition and multiplication, where numbers are stored in vectors. Defined values are:

<table>
<thead>
<tr>
<th>FCMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The FCMLA and FCADD instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The FCMLA and FCADD instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FCMA implements the functionality identified by the value 0b0001.

In Armv8.0, Armv8.1, and Armv8.2, the only permitted value is 0b0000.
From Armv8.3, if Advanced SIMD or Floating-point is implemented, the only permitted value is 0b0001.

From Armv8.3, if Advanced SIMD or Floating-point is not implemented, the only permitted value is 0b0000.

**JSCVT, bits [15:12]**

Indicates support for JavaScript conversion from double precision floating point values to integers in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>JSCVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The FJCVTZS instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The FJCVTZS instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_JSCVT implements the functionality identified by 0b0001.

In Armv8.0, Armv8.1, and Armv8.2, the only permitted value is 0b0000.

From Armv8.3, if Advanced SIMD or Floating-point is implemented, the only permitted value is 0b0001.

From Armv8.3, if Advanced SIMD or Floating-point is not implemented, the only permitted value is 0b0000.

**API, bits [11:8]**

Indicates whether an IMPLEMENTATION DEFINED algorithm is implemented in the PE for address authentication, in AArch64 state. This applies to all Pointer Authentication instructions other than the PACGA instruction. Defined values are:

<table>
<thead>
<tr>
<th>API</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is implemented, with the HaveEnhancedPAC() and HaveEnhancedPAC2() functions returning FALSE.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is implemented, with the HaveEnhancedPAC() function returning TRUE, and the HaveEnhancedPAC2() function returning FALSE.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, the HaveFPAC() function returning TRUE, the HaveFPACCombined() function returning FALSE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Address Authentication using an IMPLEMENTATION DEFINED algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, the HaveFPAC() function returning TRUE, the HaveFPACCombined() function returning TRUE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PAuth implements the functionality added by the values 0b0000, 0b0001, and 0b0010.

FEAT_PAuth2 implements the functionality added by the value 0b0011.

FEAT_FPAC implements the functionality added by the values 0b0100 and 0b0101.

From Armv8.6, the permitted values are 0b0011, 0b0100, and 0b0101.

If the value of ID_AA64ISAR1_EL1.APA is non-zero, this field must have the value 0b0000.
APA, bits [7:4]

Indicates whether QARMA or Architected algorithm is implemented in the PE for address authentication, in AArch64 state. This applies to all Pointer Authentication instructions other than the PACGA instruction. Defined values are:

<table>
<thead>
<tr>
<th>APA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Address Authentication using an Architected algorithm is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Address Authentication using the QARMA algorithm is implemented, with the HaveEnhancedPAC() and HaveEnhancedPAC2() functions returning FALSE.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Address Authentication using the QARMA algorithm is implemented, with the HaveEnhancedPAC() function returning TRUE and the HaveEnhancedPAC2() function returning FALSE.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Address Authentication using the QARMA algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, the HaveFPAC() function returning FALSE, the HaveFPACCombined() function returning FALSE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Address Authentication using the QARMA algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, the HaveFPAC() function returning TRUE, the HaveFPACCombined() function returning FALSE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Address Authentication using the QARMA algorithm is implemented, with the HaveEnhancedPAC2() function returning TRUE, the HaveFPAC() function returning TRUE, the HaveFPACCombined() function returning TRUE, the HaveFPACCombined() function returning FALSE, and the HaveEnhancedPAC() function returning FALSE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PAuth implements the functionality added by the values 0b0000, 0b0001, and 0b0010.

FEAT_PAuth2 implements the functionality added by the value 0b0011.

FEAT_FPAC implements the functionality added by the values 0b0100 and 0b0101.

From Armv8.6, the permitted values are 0b0011, 0b0100, and 0b0101.

If the value of the ID_AA64ISAR1_EL1.API is non-zero, this field must have the value 0b0000.

DPB, bits [3:0]

Data Persistence writeback. Indicates support for the DC CVAP and DC CVADP instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>DPB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>DC CVAP not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>DC CVAP supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>DC CVAP and DC CVADP supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DPB implements the functionality identified by the value 0b0001.

FEAT_DPB2 implements the functionality identified by the value 0b0010.

In Armv8.2, the permitted values are 0b0001 and 0b0010.

From Armv8.5, the only permitted value is 0b0010.

**Accessing the ID_AA64ISAR1_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, ID_AA64ISAR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64ISAR1_EL1;
elsif PSTATE.EL == EL2 then
  return ID_AA64ISAR1_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64ISAR1_EL1;
ID_AA64ISAR2_EL1, AArch64 Instruction Set Attribute Register 2

The ID_AA64ISAR2_EL1 characteristics are:

**Purpose**

Provides information about the features and instructions implemented in AArch64 state.

For general information about the interpretation of the ID registers, see Principles of the ID scheme for fields in ID registers.

**Configuration**

This register is present only from Armv8.7. Otherwise, direct accesses to ID_AA64ISAR2_EL1 are **UNDEFINED**.

**Attributes**

ID_AA64ISAR2_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64ISAR2_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-8</td>
<td>RES0</td>
</tr>
<tr>
<td>7-4</td>
<td>RPRES</td>
</tr>
<tr>
<td>3-0</td>
<td>WFxT</td>
</tr>
</tbody>
</table>

**Bits [63:8]**

Reserved, RES0.

**RPRES, bits [7:4]**

When FPCR.AH is 1, indicates support for 12 bits of mantissa in reciprocal and reciprocal square root instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>RPRES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Reciprocal and reciprocal square root estimates give 8 bits of mantissa.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Reciprocal and reciprocal square root estimates give 12 bits of mantissa.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RPRES implements the functionality identified by the value 0b0001.

From Armv8.7, if Advanced SIMD and floating-point is implemented, the only permitted value is 0b0001.

**WFxT, bits [3:0]**

Indicates support for the WFET and WFIT instructions in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>WFxT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>WFET and WFIT are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>WFET and WFIT are supported.</td>
</tr>
</tbody>
</table>
All other values are reserved.

FEAT_WFxT implements the functionality identified by the value 0b0001.

From Armv8.7, the only permitted value is 0b0001.

**Accessing the ID_AA64ISAR2_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, ID_AA64ISAR2_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        else
            UNDEFINED;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TID3 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return ID_AA64ISAR2_EL1;
    elsif PSTATE.EL == EL2 then
        return ID_AA64ISAR2_EL1;
    elsif PSTATE.EL == EL3 then
        return ID_AA64ISAR2_EL1;
The ID_AA64MMFR0_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

There are no configuration notes.

**Attributes**

ID_AA64MMFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64MMFR0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>ECV</th>
<th>FGT</th>
<th>RES0</th>
<th>ExS</th>
<th>TGran4</th>
<th>TGran64</th>
<th>TGran16</th>
<th>BigEndEL0</th>
<th>SNSMem</th>
<th>BigEnd</th>
<th>ASIDBits</th>
<th>PARange</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
</tr>
<tr>
<td>TGran4</td>
<td>TGran64</td>
<td>TGran16</td>
<td>BigEndEL0</td>
<td>SNSMem</td>
<td>BigEnd</td>
<td>ASIDBits</td>
<td>PARange</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
</tr>
</tbody>
</table>

**ECV, bits [63:60]**

Indicates presence of Enhanced Counter Virtualization. Defined values are:

<table>
<thead>
<tr>
<th>ECV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Enhanced Counter Virtualization is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Enhanced Counter Virtualization is implemented. Supports CNTHCTL_EL2, (EL1TVT, EL1TVCT, EL1NVPT, EL1NVVCT, EVNTIS), CNTKCTL_EL1, EVNTIS, CNTPCTSS_EL0 counter views, and CNTVCTSS_EL0 counter views. Extends the PMSR_EL1.PCT, PMSR_EL2.PCT, TRFCR_EL1.TS, and TRFCR_EL2.TS fields.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and also includes support for CNTHCTL_EL2.ECV and CNTPOFF_EL2.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ECV implements the functionality identified by the values 0b0001 and 0b0010.

From Armv8.6, the only permitted values are 0b0001 and 0b0010.

**FGT, bits [59:56]**

Indicates presence of the Fine-Grained Trap controls:

- If EL2 is implemented, the HAFGRTR_EL2, HDFGRTR_EL2, HDFGWTR_EL2, HFRGRTR_EL2, HFGITR_EL2, and HFGWTR_EL2 registers, and their associated traps.
- If EL2 is implemented, MDCR_EL2.TDCC.
- If EL3 is implemented, MDCR_EL3.TDCC.
• If both EL2 and EL3 are implemented, SCR_EL3.FGTEn.

Defined values are:

<table>
<thead>
<tr>
<th>FGT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The fine-grained trap controls are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The fine-grained trap controls are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FGT implements the functionality identified by the value 0b0001.

From Armv8.6, the only permitted value is 0b0001.

**Bits [55:48]**

Reserved, RES0.

**ExS, bits [47:44]**

Indicates support for disabling context synchronizing exception entry and exit. Defined values are:

<table>
<thead>
<tr>
<th>ExS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>All exception entries and exits are context synchronization events.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Non-context synchronizing exception entry and exit are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ExS implements the functionality identified by the value 0b0001.

**TGran4_2, bits [43:40]**

Indicates support for 4KB memory granule size at stage 2. Defined values are:

<table>
<thead>
<tr>
<th>TGran4_2</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Support for 4KB granule at stage 2 is identified in the ID_AArch64MMFR0_EL1.TGran4 field.</td>
<td></td>
</tr>
<tr>
<td>0b0001</td>
<td>4KB granule not supported at stage 2.</td>
<td></td>
</tr>
<tr>
<td>0b0010</td>
<td>4KB granule supported at stage 2.</td>
<td></td>
</tr>
<tr>
<td>0b0011</td>
<td>4KB granule at stage 2 supports 52-bit input and output addresses. When FEAT_LPA2 is implemented</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

The 0b0000 value is deprecated.

**TGran64_2, bits [39:36]**

Indicates support for 64KB memory granule size at stage 2. Defined values are:

<table>
<thead>
<tr>
<th>TGran64_2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Support for 64KB granule at stage 2 is identified in the ID_AArch64MMFR0_EL1.TGran64 field.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64KB granule not supported at stage 2.</td>
</tr>
<tr>
<td>0b0010</td>
<td>64KB granule supported at stage 2.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The 0b0000 value is deprecated.
### TGran16_2, bits [35:32]

Indicates support for 16KB memory granule size at stage 2. Defined values are:

<table>
<thead>
<tr>
<th>TGran16_2</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Support for 16KB granule at stage 2 is identified in the ID_AA64MMFR0_EL1.TGran16 field.</td>
<td></td>
</tr>
<tr>
<td>0b0001</td>
<td>16KB granule not supported at stage 2.</td>
<td></td>
</tr>
<tr>
<td>0b0010</td>
<td>16KB granule supported at stage 2.</td>
<td></td>
</tr>
<tr>
<td>0b0011</td>
<td>16KB granule at stage 2 supports 52-bit input and output addresses.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

The 0b0000 value is deprecated.

### TGran4, bits [31:28]

Indicates support for 4KB memory translation granule size. Defined values are:

<table>
<thead>
<tr>
<th>TGran4</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>4KB granule supported.</td>
<td></td>
</tr>
<tr>
<td>0b0001</td>
<td>4KB granule supports 52-bit input and output addresses.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b1111</td>
<td>4KB granule not supported.</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

### TGran64, bits [27:24]

Indicates support for 64KB memory translation granule size. Defined values are:

<table>
<thead>
<tr>
<th>TGran64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>64KB granule supported.</td>
</tr>
<tr>
<td>0b1111</td>
<td>64KB granule not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

### TGran16, bits [23:20]

Indicates support for 16KB memory translation granule size. Defined values are:

<table>
<thead>
<tr>
<th>TGran16</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>16KB granule not supported.</td>
<td></td>
</tr>
<tr>
<td>0b0001</td>
<td>16KB granule supported.</td>
<td></td>
</tr>
<tr>
<td>0b0010</td>
<td>16KB granule supports 52-bit input and output addresses.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

### BigEndEL0, bits [19:16]

Indicates support for mixed-endian at EL0 only. Defined values are:

<table>
<thead>
<tr>
<th>BigEndEL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No mixed-endian support at EL0. The SCTLR_EL1.E0E bit has a fixed value.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Mixed-endian support at EL0. The SCTLR_EL1.E0E bit can be configured.</td>
</tr>
</tbody>
</table>

All other values are reserved.
This field is invalid and is RES0 if ID_AA64MMFR0_EL1.BigEnd is not 0b0000.

**SNSMem, bits [15:12]**

Indicates support for a distinction between Secure and Non-secure Memory. Defined values are:

<table>
<thead>
<tr>
<th>SNSMem</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Does not support a distinction between Secure and Non-secure Memory.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Does support a distinction between Secure and Non-secure Memory.</td>
</tr>
</tbody>
</table>

**Note**

If EL3 is implemented, the value 0b0000 is not permitted.

All other values are reserved.

**BigEnd, bits [11:8]**

Indicates support for mixed-endian configuration. Defined values are:

<table>
<thead>
<tr>
<th>BigEnd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No mixed-endian support. The 'SCTLR_ELx'.EE bits have a fixed value. See the BigEndEL0 field, bits[19:16], for whether EL0 supports mixed-endian.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Mixed-endian support. The 'SCTLR_ELx'.EE and SCTLR_EL1.E0E bits can be configured.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**ASIDBits, bits [7:4]**

Number of ASID bits. Defined values are:

<table>
<thead>
<tr>
<th>ASIDBits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>8 bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>16 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**PARange, bits [3:0]**

Physical Address range supported. Defined values are:

<table>
<thead>
<tr>
<th>PARange</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>32 bits, 4GB.</td>
</tr>
<tr>
<td>0b0001</td>
<td>36 bits, 64GB.</td>
</tr>
<tr>
<td>0b0010</td>
<td>40 bits, 1TB.</td>
</tr>
<tr>
<td>0b0011</td>
<td>42 bits, 4TB.</td>
</tr>
<tr>
<td>0b0100</td>
<td>44 bits, 16TB.</td>
</tr>
<tr>
<td>0b0101</td>
<td>48 bits, 256TB.</td>
</tr>
<tr>
<td>0b0110</td>
<td>52 bits, 4PB.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The value 0b0110 is permitted only if the implementation includes FEAT_LPA, otherwise it is reserved.

**Accessing the ID_AA64MMFR0_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, ID_AA64MMFR0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return ID_AA64MMFR0_EL1;
  elsif PSTATE.EL == EL2 then
    return ID_AA64MMFR0_EL1;
  elsif PSTATE.EL == EL3 then
    return ID_AA64MMFR0_EL1;
The ID_AA64MMFR1_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

There are no configuration notes.

**Attributes**

ID_AA64MMFR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64MMFR1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
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<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>AFP</td>
<td>HCX</td>
<td>ETS</td>
<td>TWED</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>XNX</td>
<td>SpecSEI</td>
<td>PAN</td>
<td>LO</td>
<td>HPDS</td>
<td>VH</td>
<td>VMIDBits</td>
<td>HAFDBS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**AFP, bits [47:44]**

Indicates support for FPCR.\{AH, FIZ, NEP\}. Defined values are:

<table>
<thead>
<tr>
<th>AFP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The FPCR.{AH, FIZ, NEP} fields are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The FPCR.{AH, FIZ, NEP} fields are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AFP implements the functionality identified by the value 0b0001.

From Armv8.7, if Advanced SIMD and floating-point is implemented, the only permitted value is 0b0001.

**HCX, bits [43:40]**

Indicates support for HCRX_EL2 and its associated EL3 trap. Defined values are:

<table>
<thead>
<tr>
<th>HCX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>HCRX_EL2 and its associated EL3 trap are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>HCRX_EL2 and its associated EL3 trap are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.
FEAT_HCX implements the functionality identified by the value 0b0001.

From Armv8.7, if EL2 is implemented, the only permitted value is 0b0001.

ETS, bits [39:36]

Indicates support for Enhanced Translation Synchronization. Defined values are:

<table>
<thead>
<tr>
<th>ETS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Enhanced Translation Synchronization is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Enhanced Translation Synchronization is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ETS implements the functionality identified by the value 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.7, the only permitted value is 0b0001.

TWED, bits [35:32]

Indicates support for the configurable delayed trapping of WFE. Defined values are:

<table>
<thead>
<tr>
<th>TWED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Configurable delayed trapping of WFE is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Configurable delayed trapping of WFE is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TWED implements the functionality identified by the value 0b0001.

From Armv8.6, the permitted values are 0b0000 and 0b0001.

XNX, bits [31:28]

Indicates support for execute-never control distinction by Exception level at stage 2. Defined values are:

<table>
<thead>
<tr>
<th>XNX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_XNX implements the functionality identified by the value 0b0001.

From Armv8.2, the only permitted value is 0b0001.

SpecSEI, bits [27:24]

Describes whether the PE can generate SError interrupt exceptions from speculative reads of memory, including speculative instruction fetches. The defined values of this field are:

<table>
<thead>
<tr>
<th>SpecSEI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The PE never generates an SError interrupt due to an External abort on a speculative read.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The PE might generate an SError interrupt due to an External abort on a speculative read.</td>
</tr>
</tbody>
</table>

All other values are reserved.
PAN, bits [23:20]

Privileged Access Never. Indicates support for the PAN bit in PSTATE, SPSR_EL1, SPSR_EL2, SPSR_EL3, and DSPSR_EL0. Defined values are:

<table>
<thead>
<tr>
<th>PAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PAN not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PAN supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>PAN supported and AT_S1E1RP and AT_S1E1WP instructions supported.</td>
</tr>
<tr>
<td>0b0011</td>
<td>PAN supported, AT_S1E1RP and AT_S1E1WP instructions supported, and SCTLR_EL1.EPAN and SCTLR_EL2.EPAN bits supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PAN implements the functionality identified by the value 0b0001.

FEAT_PAN2 implements the functionality added by the value 0b0010.

FEAT_PAN3 implements the functionality added by the value 0b0011.

In Armv8.1, the permitted values are 0b0001 and 0b0011.

From Armv8.2, the permitted values are 0b0010 and 0b0011.

From Armv8.7, the only permitted value is 0b0011.

LO, bits [19:16]

LORegions. Indicates support for LORegions. Defined values are:

<table>
<thead>
<tr>
<th>LO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>LORegions not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LORegions supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LOR implements the functionality identified by the value 0b0001.

From Armv8.1, the only permitted value is 0b0001.

HPDS, bits [15:12]

Hierarchical Permission Disables. Indicates support for disabling hierarchical controls in translation tables. Defined values are:

<table>
<thead>
<tr>
<th>HPDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Disabling of hierarchical controls not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Disabling of hierarchical controls supported with the TCR_EL1. (HPD1, HPD0), TCR_EL2. HPD or TCR_EL2. (HPD1, HPD0), and TCR_EL3. HPD bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for value 0b0001, and adds possible hardware allocation of bits[62:59] of the translation table descriptors from the final lookup level for IMPLEMENTATION DEFINED use.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_HPDS implements the functionality identified by the value 0b0001.

FEAT_HPDS2 implements the functionality identified by the value 0b0010.

From Armv8.1, the value 0b0000 is not permitted.

VH, bits [11:8]

Virtualization Host Extensions. Defined values are:
<table>
<thead>
<tr>
<th>VH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Virtualization Host Extensions not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Virtualization Host Extensions supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_VHE implements the functionality identified by the value 0b0001.

From Armv8.1, the only permitted value is 0b0001.

**VMIDBits, bits [7:4]**

Number of VMID bits. Defined values are:

<table>
<thead>
<tr>
<th>VMIDBits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>8 bits</td>
</tr>
<tr>
<td>0b0010</td>
<td>16 bits</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_VMID16 implements the functionality identified by the value 0b0010.

From Armv8.1, the permitted values are 0b0000 and 0b0010.

**HAFDBS, bits [3:0]**

Hardware updates to Access flag and Dirty state in translation tables. Defined values are:

<table>
<thead>
<tr>
<th>HAFDBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Hardware update of the Access flag and dirty state are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Hardware update of the Access flag is supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Hardware update of both the Access flag and dirty state is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_HAFDBS implements the functionality identified by the values 0b0001 and 0b0010.

From Armv8.1, the permitted values are 0b0000, 0b0001, and 0b0010.

**Accessing the ID_AA64MMFR1_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ID_AA64MMFR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  else
    UNDEFINED;
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64MMFR1_EL1;
  end
elsif PSTATE.EL == EL2 then
  return ID_AA64MMFR1_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64MMFR1_EL1;
ID_AA64MMFR2_EL1, AArch64 Memory Model Feature Register 2

The ID_AA64MMFR2_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

Note

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_AA64MMFR2_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64MMFR2_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>E0PD</th>
<th>EVT</th>
<th>BBM</th>
<th>TTL</th>
<th>RES0</th>
<th>FWB</th>
<th>IDS</th>
<th>AT</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ST</td>
<td>NV</td>
<td>CCIDX</td>
<td>VARange</td>
<td>IESB</td>
<td>LSM</td>
<td>UAO</td>
<td>CnP</td>
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<td>62</td>
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</tbody>
</table>

**E0PD, bits [63:60]**

Indicates support for the E0PD mechanism. Defined values are:

<table>
<thead>
<tr>
<th>E0PD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>E0PD mechanism is not implemented.</td>
</tr>
<tr>
<td>0001</td>
<td>E0PD mechanism is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_E0PD implements the functionality identified by the value 0b0001.

In Armv8.4, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

If FEAT_E0PD is implemented, FEAT_CSV3 must be implemented.

**EVT, bits [59:56]**

Enhanced Virtualization Traps. If EL2 is implemented, indicates support for the HCR_EL2, {TTLBOS, TTLBIS, TOCU, TICAB, TID4} traps. Defined values are:
<table>
<thead>
<tr>
<th>EVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td><code>HCR_EL2</code> <code>{TTLBOS, TTLBIS, TOCU, TICAB, TID4}</code> traps are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td><code>HCR_EL2</code> <code>{TOCU, TICAB, TID4}</code> traps supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td><code>HCR_EL2</code> <code>{TTLBOS, TTLBIS}</code> traps are not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_EVT implements the functionality identified by the values 0b0001 and 0b010.

If EL2 is not implemented, the only permitted value is 0b0000.

In Armv8.2, the permitted values are 0b0000, 0b0001, and 0b010.

From Armv8.5, the permitted values are:

- 0b0000 when EL2 is not implemented.
- 0b0010 when EL2 is implemented.

**BBM, bits [55:52]**

Allows identification of the requirements of the hardware to have break-before-make sequences when changing block size for a translation.

<table>
<thead>
<tr>
<th>BBM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Level 0 support for changing block size is supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Level 1 support for changing block size is supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Level 2 support for changing block size is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_BBM implements the functionality identified by the values 0b0000, 0b0001, and 0b010.

From Armv8.4, the permitted values are 0b0000, 0b0001, and 0b010.

**TTL, bits [51:48]**

Indicates support for TTL field in address operations. Defined values are:

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>TLB maintenance instructions by address have bits[47:44] as RES0.</td>
</tr>
<tr>
<td>0b0001</td>
<td>TLB maintenance instructions by address have bits[47:44] holding the TTL field.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TTL implements the functionality identified by the value 0b0001.

This field affects TLBI IPAS2E1, TLBI IPAS2E1IS, TLBI IPAS2E1OS, TLBI IPAS2LE1, TLBI IPAS2LE1IS, TLBI IPAS2LE1OS, TLBI VAE1, TLBI VAE1IS, TLBI VAE1OS, TLBI VAAE1, TLBI VAAE1IS, TLBI VAAE1OS, TLBI VAAE1OS, TLBI VAAE2, TLBI VAAE2IS, TLBI VAAE2OS, TLBI VALE1, TLBI VALE1IS, TLBI VALE1OS, TLBI VALE2, TLBI VALE2IS, TLBI VALE2OS, TLBI VALE3, TLBI VALE3IS, TLBI VALE3OS.

From Armv8.4, the only permitted value is 0b0001.

**Bits [47:44]**

Reserved, RES0.

**FWB, bits [43:40]**

Indicates support for `HCR_EL2`.FWB. Defined values are:
### FWB

<table>
<thead>
<tr>
<th>FWB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>HCR_EL2.FWB bit is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>HCR_EL2.FWB is supported.</td>
</tr>
</tbody>
</table>

All other values reserved.

FEAT_S2FWB implements the functionality identified by the value 0b0001.

From Armv8.4, the only permitted value is 0b0001.

### IDS, bits [39:36]

Indicates the value of ESR_ELx.EC that reports an exception generated by a read access to the feature ID space. Defined values are:

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<tr>
<th>IDS</th>
<th>Meaning</th>
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<tbody>
<tr>
<td>0b0000</td>
<td>An exception which is generated by a read access to the feature ID space, other than a trap caused by HCR_EL2.TIDx, SCTLR_EL1.UCT, or SCTLR_EL2.UCT, is reported by ESR_ELx.EC == 0x0.</td>
</tr>
<tr>
<td>0b0001</td>
<td>All exceptions generated by an AArch64 read access to the feature ID space are reported by ESR_ELx.EC == 0x18.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The Feature ID space is defined as the System register space in AArch64 with op0==3, op1=={0, 1, 3}, CRn==0, CRm=={0-7}, op2=={0-7}.

FEAT_IDST implements the functionality identified by the value 0b0001.

From Armv8.4, the only permitted value is 0b0001.

### AT, bits [35:32]

Identifies support for unaligned single-copy atomicity and atomic functions. Defined values are:

<table>
<thead>
<tr>
<th>AT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Unaligned single-copy atomicity and atomic functions are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Unaligned single-copy atomicity and atomic functions with a 16-byte address range aligned to 16-bytes are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LSE2 implements the functionality identified by the value 0b0001.

In Armv8.2, the permitted values are 0b0000 and 0b0001.

From Armv8.4, the only permitted value is 0b0001.

### ST, bits [31:28]

Identifies support for small translation tables. Defined values are:

<table>
<thead>
<tr>
<th>ST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The maximum value of the TCR_ELx.{T0SZ,T1SZ} and VTCR_EL2.T0SZ fields is 39.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The maximum value of the TCR_ELx.{T0SZ,T1SZ} and VTCR_EL2.T0SZ fields is 48 for 4KB and 16KB granules, and 47 for 64KB granules.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TTST implements the functionality identified by the value 0b0001.

If FEAT_SEL2 is implemented, the only permitted value is 0b0001.

In an implementation which does not support FEAT_SEL2, the permitted values are 0b0000 and 0b0001.
**NV, bits [27:24]**

Nested Virtualization. If EL2 is implemented, indicates support for the use of nested virtualization. Defined values are:

<table>
<thead>
<tr>
<th>NV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Nested virtualization is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The HCR_EL2.NV, HCR_EL2.NV1, HCR_EL2.AT bits are implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>The VNCR_EL2 register and the HCR_EL2.{AT, NV, NV1, NV2} bits are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If EL2 is not implemented, the only permitted value is 0b0000.

FEAT_NV implements the functionality identified by the value 0b0001.

FEAT_NV2 implements the functionality identified by the value 0b0010.

In Armv8.3, if EL2 is implemented, the permitted values are 0b0000 and 0b0001.

From Armv8.4, if EL2 is implemented, the permitted values are 0b0000, 0b0001, and 0b0010.

**CCIDX, bits [23:20]**

Support for the use of revised CCSIDR_EL1 register format. Defined values are:

<table>
<thead>
<tr>
<th>CCIDX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>32-bit format implemented for all levels of the CCSIDR_EL1.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64-bit format implemented for all levels of the CCSIDR_EL1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CCIDX implements the functionality identified by the value 0b0001.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

**VARange, bits [19:16]**

Indicates support for a larger virtual address. Defined values are:

<table>
<thead>
<tr>
<th>VARange</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>VMSAv8-64 supports 48-bit VAs.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VMSAv8-64 supports 52-bit VAs when using the 64KB translation granule. The other translation granules support 48-bit VAs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LVA implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

**IESB, bits [15:12]**

Indicates support for the IESB bit in the SCTLR_ELx registers. Defined values are:

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>IESB bit in the SCTLR_ELx registers is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>IESB bit in the SCTLR_ELx registers is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_IESB implements the functionality identified by the value 0b0001.
LSM, bits [11:8]
Indicates support for LSMAOE and nTLSMD bits in \texttt{SCTLR\_EL1} and \texttt{SCTLR\_EL2}. Defined values are:

<table>
<thead>
<tr>
<th>LSM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>LSMAOE and nTLSMD bits not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LSMAOE and nTLSMD bits supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

\texttt{FEAT\_LSMAOC} implements the functionality identified by the value 0b0001.

UAO, bits [7:4]
User Access Override. Defined values are:

<table>
<thead>
<tr>
<th>UAO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>UAO not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>UAO supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

\texttt{FEAT\_UAO} implements the functionality identified by the value 0b0001.

From Armv8.2, the only permitted value is 0b0001.

CnP, bits [3:0]
Indicates support for Common not Private translations. Defined values are:

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Common not Private translations not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Common not Private translations supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

\texttt{FEAT\_TTCNP} implements the functionality identified by the value 0b0001.

From Armv8.2, the only permitted value is 0b0001.

**Accessing the ID\_AA64MMFR2\_EL1**
Accesses to this register use the following encodings:

\texttt{MRS <Xt>, ID\_AA64MMFR2\_EL1}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!IsZero(ID_AA64MMFR2_EL1) || boolean IMPLEMENTATION_DEFINED “ID_AA64MMFR2 trapped by HCR_EL2.TID3”) && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64MMFR2_EL1;
elsif PSTATE.EL == EL2 then
  return ID_AA64MMFR2_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64MMFR2_EL1;
The ID_AA64PFR0_EL1 characteristics are:

**Purpose**

Provides additional information about implemented PE features in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

The external register EDPFR gives information from this register.

**Attributes**

ID_AA64PFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64PFR0_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CSV3 | CSV2 | RES0 | DIT | AMU | MPAM | SEL2 | SVE |
| RAS | GIC | AdvSIMD | FP | EL3 | EL2 | EL1 | EL0 |

**CSV3, bits [63:60]**

Speculative use of faulting data. Defined values are:

<table>
<thead>
<tr>
<th>CSV3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>This Device does not disclose whether data loaded under speculation with a permission or domain fault can be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence</td>
</tr>
<tr>
<td>0b0001</td>
<td>Data loaded under speculation with a permission or domain fault cannot be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CSV3 implements the functionality identified by the value 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

If FEAT_E0PD is implemented, FEAT_CSV3 must be implemented.

**CSV2, bits [59:56]**

Speculative use of out of context branch targets. Defined values are:
This Device does not disclose whether branch targets trained in one hardware described context can affect speculative execution in a different hardware described context.

Branch targets trained in one hardware described context can only affect speculative execution in a different hardware described context in a hard-to-determine way. Contexts do not include the SCXTNUM_ELx register contexts, and these registers are not supported.

Branch targets trained in one hardware described context can only affect speculative execution in a different hardware described context in a hard-to-determine way. Contexts include the SCXTNUM_ELx register contexts, and these registers are supported.

All other values are reserved.

In Armv8.0, the permitted values are 0b0000, 0b0001, and 0b0010.

From Armv8.5, the permitted values are 0b0001 and 0b0010.

Bits [55:52]

Reserved, RES0.

DIT, bits [51:48]

Data Independent Timing. Defined values are:

<table>
<thead>
<tr>
<th>DIT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>AArch64 does not guarantee constant execution time of any instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AArch64 provides the PSTATE.DIT mechanism to guarantee constant execution time of certain instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DIT implements the functionality identified by the value 0b0001.

From Armv8.4, the only permitted value is 0b0001.

AMU, bits [47:44]

Indicates support for Activity Monitors Extension. Defined values are:

<table>
<thead>
<tr>
<th>AMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Activity Monitors Extension is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_AMUv1 is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_AMUv1p1 is implemented. As 0b0001 and adds support for virtualization of the activity monitor event counters.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AMUv1 implements the functionality identified by the value 0b0001.

FEAT_AMUv1p1 implements the functionality identified by the value 0b0010.

In Armv8.0, the only permitted value is 0b0000.

In Armv8.4, the permitted values are 0b0000 and 0b0001.

From Armv8.6, the permitted values are 0b0000, 0b0001, and 0b0010.

MPAM, bits [43:40]

Indicates support for MPAM Extension. Defined values are:
MPAM

<table>
<thead>
<tr>
<th>MPAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If ID_AA64PFR1_EL1.MPAM_frac == 0b0000, MPAM Extension is not implemented. If ID_AA64PFR1_EL1.MPAM_frac == 0b0001, MPAM Extension version 0.1 is implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If ID_AA64PFR1_EL1.MPAM_frac == 0b0000, MPAM Extension version 1.0 is implemented. If ID_AA64PFR1_EL1.MPAM_frac == 0b0001, MPAM Extension version 1.1 is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

SEL2, bits [39:36]

Secure EL2. Defined values are:

<table>
<thead>
<tr>
<th>SEL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Secure EL2 is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Secure EL2 is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SEL2 implements the functionality identified by the value 0b0001.

SVE, bits [35:32]

Scalable Vector Extension. Defined values are:

<table>
<thead>
<tr>
<th>SVE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SVE architectural state and programmers’ model are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SVE architectural state and programmers’ model are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If implemented, refer to ID_AA64ZFR0_EL1 for information about which SVE instructions are available.

RAS, bits [31:28]

RAS Extension version. Defined values are:

<table>
<thead>
<tr>
<th>RAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No RAS Extension.</td>
</tr>
<tr>
<td>0b0001</td>
<td>RAS Extension present.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_RASv1p1 present. As 0b0001, and adds support for:</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, FEAT_DoubleFault.</td>
</tr>
<tr>
<td></td>
<td>• Additional ERX_MISC&lt;m&gt; EL1 System registers.</td>
</tr>
<tr>
<td></td>
<td>• Additional System registers ERXPFGCDN_EL1, ERXPFGCTL_EL1, and ERXPFGF_EL1, and the SCR_EL3, FIEN and HCR_EL2, FIEN trap controls, to support the optional RAS Common Fault Injection Model Extension.</td>
</tr>
<tr>
<td></td>
<td>Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ERR&lt;n&gt;STATUS and support for the optional RAS Timestamp and RAS Common Fault Injection Model Extensions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RAS implements the functionality identified by the value 0b0001.

FEAT_RASv1p1 and FEAT_DoubleFault implement the functionality identified by the value 0b0010.

In Armv8.0 and Armv8.1, the permitted values are 0b0000 and 0b0001.

In Armv8.2, the only permitted value is 0b0001.
From Armv8.4, if FEAT_DoubleFault is implemented, the only permitted value is 0b0010.

From Armv8.4, when FEAT_DoubleFault is not implemented, and ERRIDR_EL1 is 0, the permitted values are IMPLEMENTATION DEFINED 0b0001 or 0b0010.

---

**Note**

When the value of this field is 0b0001, ID_AA64PFR1_EL1.RAS_frac indicates whether FEAT_RASv1p1 is implemented.

---

**GIC, bits [27:24]**

System register GIC CPU interface. Defined values are:

<table>
<thead>
<tr>
<th>GIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>GIC CPU interface system registers not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>System register interface to versions 3.0 and 4.0 of the GIC CPU interface is supported.</td>
</tr>
<tr>
<td>0b0011</td>
<td>System register interface to version 4.1 of the GIC CPU interface is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**AdvSIMD, bits [23:20]**

Advanced SIMD. Defined values are:

<table>
<thead>
<tr>
<th>AdvSIMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Advanced SIMD is implemented, including support for the following SISD and SIMD operations:</td>
</tr>
<tr>
<td></td>
<td>• Integer byte, halfword, word and doubleword element operations.</td>
</tr>
<tr>
<td></td>
<td>• Single-precision and double-precision floating-point arithmetic.</td>
</tr>
<tr>
<td></td>
<td>• Conversions between single-precision and half-precision data types, and double-precision and half-precision data types.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As for 0b0000, and also includes support for half-precision floating-point arithmetic.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Advanced SIMD is not implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field must have the same value as the FP field.

The permitted values are:

- 0b0000 in an implementation with Advanced SIMD support that does not include the FEAT_FP16 extension.
- 0b0001 in an implementation with Advanced SIMD support that includes the FEAT_FP16 extension.
- 0b1111 in an implementation without Advanced SIMD support.

**FP, bits [19:16]**

Floating-point. Defined values are:

<table>
<thead>
<tr>
<th>FP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Floating-point is implemented, and includes support for:</td>
</tr>
<tr>
<td></td>
<td>• Single-precision and double-precision floating-point types.</td>
</tr>
<tr>
<td></td>
<td>• Conversions between single-precision and half-precision data types, and double-precision and half-precision data types.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As for 0b0000, and also includes support for half-precision floating-point arithmetic.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Floating-point is not implemented.</td>
</tr>
</tbody>
</table>
All other values are reserved.

This field must have the same value as the AdvSIMD field.

The permitted values are:

- \(0b0000\) in an implementation with floating-point support that does not include the FEAT_FP16 extension.
- \(0b0001\) in an implementation with floating-point support that includes the FEAT_FP16 extension.
- \(0b1111\) in an implementation without floating-point support.

**EL3, bits [15:12]**

EL3 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL3 is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL3 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL3 can be executed in either AArch64 or AArch32 state.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**EL2, bits [11:8]**

EL2 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL2 is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL2 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL2 can be executed in either AArch64 or AArch32 state.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**EL1, bits [7:4]**

EL1 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>EL1 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL1 can be executed in either AArch64 or AArch32 state.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**EL0, bits [3:0]**

EL0 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>EL0 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL0 can be executed in either AArch64 or AArch32 state.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Accessing the ID_AA64PFR0_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, ID_AA64PFR0_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0100</td>
<td>0b00</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  else
    UNDEFINED;
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AA64PFR0_EL1;
  end
elsif PSTATE.EL == EL2 then
  return ID_AA64PFR0_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AA64PFR0_EL1;

The ID_AA64PFR1_EL1 characteristics are:

**Purpose**

Reserved for future expansion of information about implemented PE features in AArch64 state.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

There are no configuration notes.

**Attributes**

ID_AA64PFR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64PFR1_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| MPAM_frac | RAS_frac | MTE | SSBS | BT |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:20]**

Reserved, RES0.

**MPAM_frac, bits [19:16]**

MPAM Extension fractional field. Defined values are:

<table>
<thead>
<tr>
<th>MPAM_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If ID_AA64PFR0_EL1.MPAM == 0b0000, MPAM Extension not implemented. If ID_AA64PFR0_EL1.MPAM == 0b0001, MPAM Extension v1.0 is implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If ID_AA64PFR0_EL1.MPAM == 0b0000, implements MPAM v0.1, which is like v1.1 but reduces support for Secure PARTIDs. If ID_AA64PFR0_EL1.MPAM == 0b0001, implements MPAM v1.1 and adds support for MPAM2_EL2.TIDR to provide trapping of MPAMIDR_EL1 when MPAMHCR_EL2 is not present.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**RAS_frac, bits [15:12]**

RAS Extension fractional field. Defined values are:
<table>
<thead>
<tr>
<th>RAS_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If ( \text{ID_AA64PFR0_EL1_RAS} == 0b0001 ), RAS Extension implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If ( \text{ID_AA64PFR0_EL1_RAS} == 0b0001 ), as 0b0000 and adds support for:</td>
</tr>
<tr>
<td></td>
<td>- Additional ERXMISC(&lt;m&gt;) EL1 System registers.</td>
</tr>
<tr>
<td></td>
<td>- Additional System registers ( \text{ERXPFGCDN_EL1} ), ( \text{ERXPFGCTL_EL1} ), and ( \text{ERXPFGF_EL1} ), and the ( \text{SCR_EL3} ), ( \text{FIEN} ) and ( \text{HCR_EL2} ), ( \text{FIEN} ) trap controls, to support the optional RAS Common Fault Injection Model Extension.</td>
</tr>
<tr>
<td></td>
<td>Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ( \text{ERR&lt;n&gt;STATUS} ), and support for the optional RAS Timestamp and RAS Common Fault Injection Model Extensions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RASv1p1 implements the functionality identified by the value 0b0001.

This field is valid only if \( \text{ID\_AA64PFR0\_EL1\_RAS} == 0b0001 \).

### MTE, bits [11:8]

Support for the Memory Tagging Extension. Defined values are:

<table>
<thead>
<tr>
<th>MTE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Memory Tagging Extension is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Instruction-only Memory Tagging Extension is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Full Memory Tagging Extension is implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Memory Tagging Extension is implemented with support for asymmetric Tag Check Fault handling.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_MTE implements the functionality identified by the value 0b0001.

FEAT_MTE2 implements the functionality identified by the value 0b0010

FEAT_MTE3 implements the functionality identified by the value 0b0011.

In Armv8.5, the permitted values are 0b0000, 0b0001 and 0b0010.

From Armv8.7, the value 0b0001 is not permitted.

### SSBS, bits [7:4]

Speculative Store Bypasing controls in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>AArch64 provides no mechanism to control the use of Speculative Store Bypasing.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AArch64 provides the PSTATE.SBSB mechanism to mark regions that are Speculative Store Bypasing Safe.</td>
</tr>
<tr>
<td>0b0010</td>
<td>AArch64 provides the PSTATE.SBSB mechanism to mark regions that are Speculative Store Bypasing Safe, and the MSR and MRS instructions to directly read and write the PSTATE.SBSB field.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SSBS implements the functionality identified by the value 0b0001.

FEAT_SSBS2 implements the functionality identified by the value 0b0010.
**BT, bits [3:0]**

Branch Target Identification mechanism support in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The Branch Target Identification mechanism is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The Branch Target Identification mechanism is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_BTI implements the functionality identified by the value 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**Accessing the ID_AA64PFR1_EL1**

Accesses to this register use the following encodings:

```c
MRS <Xt>, ID_AA64PFR1_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_AA64PFR1_EL1;
elsif PSTATE.EL == EL2 then
    return ID_AA64PFR1_EL1;
elsif PSTATE.EL == EL3 then
    return ID_AA64PFR1_EL1;
```

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ID_AA64ZFR0_EL1, SVE Feature ID register 0

The ID_AA64ZFR0_EL1 characteristics are:

**Purpose**

Provides additional information about the implemented features of the AArch64 Scalable Vector Extension, when the ID_AA64PFR0_EL1.SVE field is not zero.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

**Note**

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_AA64ZFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AA64ZFR0_EL1 bit assignments are:

```
  | 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
---|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
 RES0|  F64MM|  F32MM| RES0|  I8MM| RES0|  SVEver |
 RES0|  BF16| RES0| RES0| RES0| RES0|      |
 31 | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
```

Bits [63:60]

Reserved, RES0.

**F64MM, bits [59:56]**

Indicates support for SVE FP64 double-precision floating-point matrix multiplication instructions. Defined values are:

<table>
<thead>
<tr>
<th>F64MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FP64 matrix multiplication and related instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FP64 variant of the FMMLA instruction, and LD1RO* instructions are implemented. The 128-bit element variations of TRN1, TRN2, UZP1, UZP2, ZIP1, and ZIP2 are also implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_F64MM implements the functionality identified by 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.
### F32MM, bits [55:52]

Indicates support for the SVE FP32 single-precision floating-point matrix multiplication instruction. Defined values are:

<table>
<thead>
<tr>
<th>F32MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FP32 matrix multiplication instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FP32 variant of the FMMLA instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_F32MM implements the functionality identified by 0b0001.

From Arm v8.2, the permitted values are 0b0000 and 0b0001.

### Bits [51:48]

Reserved, RES0.

### I8MM, bits [47:44]

Indicates support for SVE Int8 matrix multiplication instructions. Defined values are:

<table>
<thead>
<tr>
<th>I8MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Int8 matrix multiplication instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SMMLA, SUDOT, UMMLA, USMMLA, and USDOT instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_I8MM implements the functionality identified by 0b0001.

When Advanced SIMD and SVE are both implemented, this field must return the same value as ID_AA64ISAR1_EL1.I8MM.

From Armv8.6, the only permitted value is 0b0001.

### Bits [43:24]

Reserved, RES0.

### BF16, bits [23:20]

Indicates support for SVE BFloat16 instructions. Defined values are:

<table>
<thead>
<tr>
<th>BF16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>BFloat16 instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>BFCVT, BFCVTNT, BFDOT, BFMLALB, BFMLALT, and BFMLMA instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_BF16 implements the functionality identified by 0b0001.

When Advanced SIMD and SVE are both implemented, this field must return the same value as ID_AA64ISAR1_EL1.BF16.

From Armv8.6, the only permitted value is 0b0001.

### Bits [19:4]

Reserved, RES0.
**SVEver, bits [3:0]**

Indicates support for SVE version 2. Defined values are:

<table>
<thead>
<tr>
<th>SVEver</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SVE instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved. This field is valid only if the ID_AA64PFR0_EL1.SVE field is not zero.

**Accessing the ID_AA64ZFR0_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, ID_AA64ZFR0_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && (!IsZero(ID_AA64ZFR0_EL1) || boolean IMPLEMENTATION_DEFINED
            "ID_AA64ZFR0_EL1 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return ID_AA64ZFR0_EL1;
    elsif PSTATE.EL == EL2 then
        return ID_AA64ZFR0_EL1;
    elsif PSTATE.EL == EL3 then
        return ID_AA64ZFR0_EL1;
```
**ID_AFR0_EL1, AArch32 Auxiliary Feature Register 0**

The ID_AFR0_EL1 characteristics are:

**Purpose**

Provides information about the IMPLEMENTATION DEFINED features of the PE in AArch32 state.

Must be interpreted with the Main ID Register, MIDR_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_AFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_AFR0[31:0].

**Attributes**

ID_AFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_AFR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bits [63:16]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMPLEMENTATION DEFINED, bits [15:12]</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>IMPLEMENTATION DEFINED, bits [11:8]</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>IMPLEMENTATION DEFINED, bits [7:4]</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>IMPLEMENTATION DEFINED, bits [3:0]</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
</tbody>
</table>
Otherwise:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_AFR0_EL1

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ ID_AFR0_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_AFR0_EL1;
elsif PSTATE.EL == EL2 then
  return ID_AFR0_EL1;
elsif PSTATE.EL == EL3 then
  return ID_AFR0_EL1;
The ID_DFR0_EL1 characteristics are:

**Purpose**

Provides top level information about the debug system in AArch32 state.

Must be interpreted with the Main ID Register, MIDR_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_DFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_DFR0[31:0].

**Attributes**

ID_DFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_DFR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TraceFilt | PerfMon | MProfDbg | MMapTrc | CopTrc | MMapDbg | CopSDbg | CopDbg |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**TraceFilt, bits [31:28]**

Armv8.4 Self-hosted Trace Extension version. Defined values are:

<table>
<thead>
<tr>
<th>TraceFilt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Armv8.4 Self-hosted Trace Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Armv8.4 Self-hosted Trace Extension implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TRF implements the functionality added by the value 0b0001.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

**PerfMon, bits [27:24]**

Performance Monitors Extension version.

This field does not follow the standard ID scheme, but uses the alternative ID scheme described in 'Alternative ID scheme used for the Performance Monitors Extension version'
Defined values are:

<table>
<thead>
<tr>
<th>PerfMon</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Performance Monitors Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Performance Monitors Extension, PMUv1 implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Performance Monitors Extension, PMUv2 implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Performance Monitors Extension, PMUv3 implemented.</td>
</tr>
<tr>
<td>0b0100</td>
<td>PMUv3 for Armv8.1. As 0b0011, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• Extended 16-bit PMEVTYPER\langle n\rangle.evCount field.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the HDCR.HPMD control bit.</td>
</tr>
<tr>
<td>0b0101</td>
<td>PMUv3 for Armv8.4. As 0b0100, and also includes support for the PMMIR register.</td>
</tr>
<tr>
<td>0b0110</td>
<td>PMUv3 for Armv8.5. As 0b0101, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• 64-bit event counters.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the HDCR.HCCD control bit.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.SCCD control bit.</td>
</tr>
<tr>
<td>0b0111</td>
<td>PMUv3 for Armv8.7. As 0b0110, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• The PMCR.FZO and, if EL2 is implemented, HDCR.HPMFZO control bits.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.{MPMX,MCCD} control bits.</td>
</tr>
<tr>
<td>0b1111</td>
<td>IMPLEMENTATION DEFINED form of performance monitors supported. PMUv3 not supported. Arm does not recommend this value for new implementations.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PMUv3 implements the functionality identified by the value 0b0011.

FEAT_PMUv3p1 implements the functionality identified by the value 0b0100.

FEAT_PMUv3p4 implements the functionality identified by the value 0b0101.

FEAT_PMUv3p5 implements the functionality identified by the value 0b0110.

FEAT_PMUv3p7 implements the functionality identified by the value 0b0111.

In any Armv8 implementation, the values 0b0001 and 0b0010 are not permitted.

From Armv8.1, if FEAT_PMUv3 is implemented, the value 0b0011 is not permitted.

From Armv8.4, if FEAT_PMUv3 is implemented, the value 0b0100 is not permitted.

From Armv8.5, if FEAT_PMUv3 is implemented, the value 0b0101 is not permitted.

From Armv8.7, if FEAT_PMUv3 is implemented, the value 0b0110 is not permitted.

**Note**

In Armv7, the value 0b0000 can mean that PMUv1 is implemented. PMUv1 is not permitted in an Armv8 implementation.

**MProfDbg, bits [23:20]**

M Profile Debug. Support for memory-mapped debug model for M profile processors. Defined values are:

<table>
<thead>
<tr>
<th>MProfDbg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for M profile Debug architecture, with memory-mapped access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.
MMapTrc, bits [19:16]

Memory Mapped Trace. Support for memory-mapped trace model. Defined values are:

<table>
<thead>
<tr>
<th>MMapTrc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Arm trace architecture, with memory-mapped access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

See the ETM Architecture Specification for more information.

CopTrc, bits [15:12]

Support for System registers-based trace model, using registers in the coproc == 0b1110 encoding space. Defined values are:

<table>
<thead>
<tr>
<th>CopTrc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Arm trace architecture, with System registers access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

See the ETM Architecture Specification for more information.

MMapDbg, bits [11:8]

Memory Mapped Debug. Support for v7 memory-mapped debug model, for A and R profile processors.

In Armv8-A, this field is RES0.

The optional memory map defined by Armv8 is not compatible with Armv7.

CopSDbg, bits [7:4]

Support for a System registers-based Secure debug model, using registers in the coproc = 0b1110 encoding space, for an A profile processor that includes EL3.

If EL3 is not implemented and the implemented Security state is Non-secure state, this field is RES0. Otherwise, this field reads the same as bits [3:0].

CopDbg, bits [3:0]

Support for System registers-based debug model, using registers in the coproc == 0b1110 encoding space, for A and R profile processors. Defined values are:
CopDbg | Meaning
---|---
0b0000 | Not supported.
0b0010 | Support for Armv6, v6 Debug architecture, with System registers access.
0b0011 | Support for Armv6, v6.1 Debug architecture, with System registers access.
0b0100 | Support for Armv7, v7 Debug architecture, with System registers access.
0b0101 | Support for Armv7, v7.1 Debug architecture, with System registers access.
0b0110 | Support for Armv8 debug architecture, with System registers access.
0b0111 | Support for Armv8 debug architecture, with System registers access, and Virtualization Host Extensions.
0b1000 | Support for Armv8.2 debug architecture.
0b1001 | Support for Armv8.4 debug architecture.

All other values are reserved.

FEAT_Debugv8p2 adds the functionality identified by the value 0b1000.

FEAT_Debugv8p4 adds the functionality identified by the value 0b1001.

In Armv8.0, the only permitted value is 0b0110.

In Armv8.1, the only permitted value is 0b0111.

In Armv8.2, the only permitted value is 0b1000.

From Armv8.4, the only permitted value is 0b1001.

**Otherwise:**

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
</tr>
<tr>
<td><strong>UNKNOWN</strong></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Reserved, UNKNOWN.

**Accessing the ID_DFR0_EL1**

Accesses to this register use the following encodings:

\[
\text{MRS } \langle Xt \rangle, \text{ ID_DFR0_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_DFR0_EL1;
else if PSTATE.EL == EL2 then
    return ID_DFR0_EL1;
else if PSTATE.EL == EL3 then
    return ID_DFR0_EL1;
The ID_DFR1_EL1 characteristics are:

**Purpose**

Provides top level information about the debug system in AArch32.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_DFR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_DFR1[31:0].

**Note**

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_DFR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_DFR1_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**MTPMU, bits [3:0]**

Multi-threaded PMU extension. Defined values are:

<table>
<thead>
<tr>
<th>MTPMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, it is IMPLEMENTATION DEFINED whether PMEVTYPER&lt;n&gt;.MT are read/write or RES0.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_MTPMU and FEAT_PMUv3 implemented. PMEVTYPER&lt;n&gt;.MT are read/write. When FEAT_MTPMU is disabled, the Effective values of PMEVTYPER&lt;n&gt;.MT are 0.</td>
</tr>
<tr>
<td>0b1111</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, PMEVTYPER&lt;n&gt;.MT are RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_MTPMU implements the functionality identified by the value 0b0001.
From Armv8.6, in an implementation that includes FEAT_PMUv3, the value 0b0000 is not permitted. In an implementation that does not include FEAT_PMUv3, the value 0b0001 is not permitted.

**Otherwise:**

| Bits [63:0] | Reserved, UNKNOWN. |

### Accessing the ID_DFR1_EL1

Accesses to this register use the following encodings:

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b0000 & 0b0011 & 0b101 \\
\hline
\end{array}
\]

```plaintext
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && (!IsZero(ID_DFR1_EL1) || boolean IMPLEMENTATION_DEFINED "ID_DFR1 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return ID_DFR1_EL1;
  elsif PSTATE.EL == EL2 then
    return ID_DFR1_EL1;
  elsif PSTATE.EL == EL3 then
    return ID_DFR1_EL1;
```
The ID_ISAR0_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with `ID_ISAR1_EL1`, `ID_ISAR2_EL1`, `ID_ISAR3_EL1`, `ID_ISAR4_EL1`, and `ID_ISAR5_EL1`.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register `ID_ISAR0[31:0]`.

**Attributes**

ID_ISAR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Divide</td>
<td>Indicates the implemented Divide instructions. Defined values are:</td>
</tr>
<tr>
<td>61</td>
<td>Debug</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Coproc</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td>CmpBranch</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>BitField</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>BitCount</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>Swap</td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:28]

Reserved, RES0.

**Divide, bits [27:24]**

Indicates the implemented Divide instructions. Defined values are:

<table>
<thead>
<tr>
<th>Divide</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds SDIV and UDIV in the T32 instruction set.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds SDIV and UDIV in the A32 instruction set.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**Debug, bits [23:20]**

Indicates the implemented Debug instructions. Defined values are:
### Debug, bits [0x0]

- **0b0000**: None implemented.
- **0b0001**: Adds BKPT.

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### Coproc, bits [19:16]

Indicates the implemented System register access instructions. Defined values are:

<table>
<thead>
<tr>
<th>Coproc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented, except for instructions separately attributed by the architecture to provide access to AArch32 System registers and System instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds generic CDP, LDC, MCR, MRC, and STC.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds generic CDP2, LDC2, MCR2, MRC2, and STC2.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds generic MCRR and MRRC.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds generic MCRR2 and MRRC2.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### CmpBranch, bits [15:12]

Indicates the implemented combined Compare and Branch instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>CmpBranch</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds CBNZ and CBZ.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### BitField, bits [11:8]

Indicates the implemented BitField instructions. Defined values are:

<table>
<thead>
<tr>
<th>BitField</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds BFC, BFI, SBFX, and UBFX.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### BitCount, bits [7:4]

Indicates the implemented Bit Counting instructions. Defined values are:

<table>
<thead>
<tr>
<th>BitCount</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds CLZ.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### Swap, bits [3:0]

Indicates the implemented Swap instructions in the A32 instruction set. Defined values are:
All other values are reserved.

In Armv8-A, the only permitted value is `0b0000`.

### Otherwise:

<p>| | | | | | | | | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
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<td>47</td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Reserved, `UNKNOWN`.

### Accessing the ID_ISAR0_EL1

Accesses to this register use the following encodings:

```
MRS <Xt>, ID_ISAR0_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return ID_ISAR0_EL1;
  elsif PSTATE.EL == EL2 then
    return ID_ISAR0_EL1;
  elsif PSTATE.EL == EL3 then
    return ID_ISAR0_EL1;
```
The ID_ISAR1_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR2_EL1, ID_ISAR3_EL1, ID_ISAR4_EL1, and ID_ISAR5_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR1[31:0].

**Attributes**

ID_ISAR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR1_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Jazelle | Interwork | Immediate | IfThen | Extend | Except AR | Except | Endian |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**Jazelle, bits [31:28]**

Indicates the implemented Jazelle extension instructions. Defined values are:

<table>
<thead>
<tr>
<th>Jazelle</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No support for Jazelle.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the BXJ instruction and the J bit in the PSR. This setting might indicate a trivial implementation of the Jazelle extension.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Interwork, bits [27:24]**

Indicates the implemented Interworking instructions. Defined values are:
## Interwork

<table>
<thead>
<tr>
<th>Interwork</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the BX instruction, and the T bit in the PSR.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the BLX instruction. PC loads have BX-like behavior.</td>
</tr>
<tr>
<td>0b0110</td>
<td>As for 0b0010, and guarantees that data-processing instructions in the A32 instruction set with the PC as the destination and the S bit clear have BX-like behavior.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0110.

## Immediate, bits [23:20]

Indicates the implemented data-processing instructions with long immediates. Defined values are:

<table>
<thead>
<tr>
<th>Immediate</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
</tbody>
</table>
| 0b0001    | Adds:  
  - The MOVT instruction.  
  - The MOV instruction encodings with zero-extended 16-bit immediates.  
  - The T32 ADD and SUB instruction encodings with zero-extended 12-bit immediates, and the other ADD, ADR, and SUB encodings cross-referenced by the pseudocode for those encodings. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

## IfThen, bits [19:16]

Indicates the implemented If-Then instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>IfThen</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the IT instructions, and the IT bits in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

## Extend, bits [15:12]

Indicates the implemented Extend instructions. Defined values are:

<table>
<thead>
<tr>
<th>Extend</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No scalar sign-extend or zero-extend instructions are implemented, where scalar instructions means non-Advanced SIMD instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SXTB, SXTH, UXTB, and UXTH instructions.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0001, and adds the SXTB16, SXTAB, SXTAB16, SXTAH, UXTOB16, UXTOB, UXTOB16, and UXTOAH instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

## Except_AR, bits [11:8]

Indicates the implemented A and R profile exception-handling instructions. Defined values are:
Except, bits [7:4]

Indicates the implemented exception-handling instructions in the A32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>Except</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented. This indicates that the User bank and Exception return forms of the LDM and STM instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the LDM (exception return), LDM (user registers), and STM (user registers) instruction versions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

Endian, bits [3:0]

Indicates the implemented Endian instructions. Defined values are:

<table>
<thead>
<tr>
<th>Endian</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SETEND instruction, and the E bit in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

Otherwise:

Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_ISAR1_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_ISAR1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_ISAR1_EL1;
elsif PSTATE.EL == EL2 then
  return ID_ISAR1_EL1;
elsif PSTATE.EL == EL3 then
  return ID_ISAR1_EL1;
The ID_ISAR2_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR1_EL1, ID_ISAR3_EL1, ID_ISAR4_EL1, and ID_ISAR5_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR2_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR2[31:0].

**Attributes**

ID_ISAR2_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR2_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Reversal</th>
<th>PSR_AR</th>
<th>MultiU</th>
<th>MultiS</th>
<th>Mult</th>
<th>MultiAccessInt</th>
<th>MemHint</th>
<th>LoadStore</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Reversal, bits [31:28]**

Indicates the implemented Reversal instructions. Defined values are:

<table>
<thead>
<tr>
<th>Reversal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the REV, REV16, and REVSH instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the RBIT instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**PSR_AR, bits [27:24]**

Indicates the implemented A and R profile instructions to manipulate the PSR. Defined values are:
PSR_AR | Meaning
---|---
0b0000 | None implemented.
0b0001 | Adds the MRS and MSR instructions, and the exception return forms of data-processing instructions.

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

The exception return forms of the data-processing instructions are:

- In the A32 instruction set, data-processing instructions with the PC as the destination and the S bit set. These instructions might be affected by the WithShifts attribute.
- In the T32 instruction set, the SUBS PC,LR,#N instruction.

**MultU, bits [23:20]**

Indicates the implemented advanced unsigned Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>MultU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the UMULL and UMLAL instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the UMAAL instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**MultS, bits [19:16]**

Indicates the implemented advanced signed Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>MultS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SMULL and SMLAL instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the SMLABB, SMLABT, SMLALBB, SMLALBT, SMLALT, SMLATB, SMLATT, SMLAWB, SMLAWT, SMULBB, SMULBT, SMULTB, SMULTT, SMULWB, and SMULWT instructions. Also adds the Q bit in the PSRs.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds the SMLAD, SMLADX, SMLALD, SMLALDX, SMLS, SMLSD, SMLSDX, SMLS, SMML, SMLAR, SMMLS, SMMLSR, SMMUL, SMMULR, SMUAD, SMUADX, SMUSD, and SMUSDX instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0011.

**Mult, bits [15:12]**

Indicates the implemented additional Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>Mult</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No additional instructions implemented. This means only MUL is implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the MLA instruction.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the MLS instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**MultiAccessInt, bits [11:8]**

Indicates the support for interruptible multi-access instructions. Defined values are:
### MultiAccessInt

<table>
<thead>
<tr>
<th>MultiAccessInt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No support. This means the LDM and STM instructions are not interruptible.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LDM and STM instructions are restartable.</td>
</tr>
<tr>
<td>0b0010</td>
<td>LDM and STM instructions are continuable.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### MemHint, bits [7:4]

Indicates the implemented Memory Hint instructions. Defined values are:

<table>
<thead>
<tr>
<th>MemHint</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the PLD instruction.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Adds the PLD instruction. (0b0001 and 0b0010 have identical effects.)</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001 (or 0b0010), and adds the PLI instruction.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds the PLDW instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0100.

### LoadStore, bits [3:0]

Indicates the implemented additional load/store instructions. Defined values are:

<table>
<thead>
<tr>
<th>LoadStore</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No additional load/store instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the LDRD and STRD instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the Load Acquire (LDAB, LDAH, LDA, LDAEXB, LDAEXH, LDAEX, LDAEXD) and Store Release (STLB, STLH, STL, STLEXB, STLEXH, STLEX, STLEXD) instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

### Otherwise:

<table>
<thead>
<tr>
<th></th>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
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<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
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</tbody>
</table>

**Bits [63:0]**

Reserved, UNKNOWN.

### Accessing the ID_ISAR2_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_ISAR2_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return ID_ISAR2_EL1;
  elsif PSTATE.EL == EL2 then
    return ID_ISAR2_EL1;
  elsif PSTATE.EL == EL3 then
    return ID_ISAR2_EL1;
The ID_ISAR3_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR1_EL1, ID_ISAR2_EL1, ID_ISAR4_EL1, and ID_ISAR5_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR3_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR3[31:0].

**Attributes**

ID_ISAR3_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR3_EL1 bit assignments are:

### When AArch32 is supported at any Exception level:

<table>
<thead>
<tr>
<th>Bit</th>
<th>T32EE</th>
<th>TrueNOP</th>
<th>T32Copy</th>
<th>TabBranch</th>
<th>SynchPrim</th>
<th>SVC</th>
<th>SIMD</th>
<th>Saturate</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
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</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**T32EE, bits [31:28]**

Indicates the implemented T32EE instructions. Defined values are:

<table>
<thead>
<tr>
<th>T32EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>000000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>000001</td>
<td>Adds the ENTERX and LEAVEX instructions, and modifies the load behavior to include null checking.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**TrueNOP, bits [27:24]**

Indicates the implemented true NOP instructions. Defined values are:
TrueNOP, bits [47:44]

Indicates the meaning of TrueNOP. Defined values are:

<table>
<thead>
<tr>
<th>TrueNOP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. This means there are no NOP instructions that do not have any register dependencies.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds true NOP instructions in both the T32 and A32 instruction sets. This also permits additional NOP-compatible hints.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

T32Copy, bits [23:20]

Indicates the support for T32 non flag-setting MOV instructions. Defined values are:

<table>
<thead>
<tr>
<th>T32Copy</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported. This means that in the T32 instruction set, encoding T1 of the MOV (register) instruction does not support a copy from a low register to a low register.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for T32 instruction set encoding T1 of the MOV (register) instruction, copying from a low register to a low register.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

TabBranch, bits [19:16]

Indicates the implemented Table Branch instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>TabBranch</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the TBB and TBH instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

SynchPrim, bits [15:12]

Used in conjunction with ID_ISAR4.SynchPrim_frac to indicate the implemented Synchronization Primitive instructions. Defined values are:

<table>
<thead>
<tr>
<th>SynchPrim</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If SynchPrim_frac == 0b0000, no Synchronization Primitives implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If SynchPrim_frac == 0b0000, adds the LDREX and STREX instructions.</td>
</tr>
<tr>
<td></td>
<td>If SynchPrim_frac == 0b0011, also adds the CLREX, LDREXB, STREXB, and STREXH instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>If SynchPrim_frac == 0b0000, as for [0b0001, 0b0011] and also adds the LDREXD and STREXD instructions.</td>
</tr>
</tbody>
</table>

All other combinations of SynchPrim and SynchPrim_frac are reserved.

In Armv8-A, the only permitted value is 0b0010.

SVC, bits [11:8]

Indicates the implemented SVC instructions. Defined values are:

<table>
<thead>
<tr>
<th>SVC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SVC instruction.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In Armv8-A, the only permitted value is **0b0001**.

**SIMD, bits [7:4]**

Indicates the implemented SIMD instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SSAT and USAT instructions, and the Q bit in the PSRs.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001, and adds the PKHBT, PKHTB, QADD16, QADD8, QASX, QSUB16, QSUB8, QAX, SADD16, SADD8, SASX, SEL, SHADD16, SHADD8, SHASX, SHSUB16, SHSUB8, SHAX, SSAT16, SSUB16, SSUB8, SSAX, SXTAB16, SXTB16, UADD16, UADD8, USAX, UHADD16, UHADD8, UHASX, UHSUB16, UHSUB8, UHASX, UQADD16, UQADD8, UQASX, UQSUB16, UQSUB8, UQASX, USAD8, USADA8, USAT16, USUB16, USUB8, USAX, UXTAB16, and UXTB16 instructions. Also adds support for the GE[3:0] bits in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is **0b0001**.

The SIMD field relates only to implemented instructions that perform SIMD operations on the general-purpose registers. In an implementation that supports floating-point and Advanced SIMD instructions, MVFR0, MVFR1, and MVFR2 give information about the implemented Advanced SIMD instructions.

**Saturate, bits [3:0]**

Indicates the implemented Saturate instructions. Defined values are:

<table>
<thead>
<tr>
<th>Saturate</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. This means no non-Advanced SIMD saturate instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the QADD, QDADD, QDSUB, and QSUB instructions, and the Q bit in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is **0b0001**.

** Otherwise:**

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is **0b0001**.

**Accessing the ID_ISAR3_EL1**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS &lt;Xt&gt;, ID_ISAR3_EL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_ISAR3_EL1;
    end if
elsif PSTATE.EL == EL2 then
    return ID_ISAR3_EL1;
elsif PSTATE.EL == EL3 then
    return ID_ISAR3_EL1;
The ID_ISAR4_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR1_EL1, ID_ISAR2_EL1, ID_ISAR3_EL1, and ID_ISAR5_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR4_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR4[31:0].

**Attributes**

ID_ISAR4_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR4_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| SWP_frac | PSR_M | SynchPrim_frac | Barrier | SMC | Writeback | WithShifts | Unpriv |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**SWP_frac, bits [31:28]**

Indicates support for the memory system locking the bus for SWP or SWPB instructions. Defined values are:

<table>
<thead>
<tr>
<th>SWP_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SWP or SWPB instructions not implemented. SWP or SWPB implemented but only in a uniprocessor context. SWP and SWPB do not guarantee whether memory accesses from other Requesters can come between the load memory access and the store memory access of the SWP or SWPB.</td>
</tr>
<tr>
<td>0b0001</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved. This field is valid only if ID_ISAR0.Swap is 0b0000.

In Armv8-A, the only permitted value is 0b0000.
**PSR_M, bits [27:24]**

Indicates the implemented M profile instructions to modify the PSRs. Defined values are:

<table>
<thead>
<tr>
<th>PSR_M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the M profile forms of the CPS, MRS, and MSR instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**SynchPrim_frac, bits [23:20]**

Used in conjunction with ID_ISAR3, SynchPrim to indicate the implemented Synchronization Primitive instructions. Possible values are:

<table>
<thead>
<tr>
<th>SynchPrim_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If SynchPrim == 0b0000, no Synchronization Primitives implemented. If SynchPrim == 0b0001, adds the LDREX and STREX instructions. If SynchPrim == 0b0010, also adds the CLREX, LDREXB, LDREXH, STREXB, STREXH, LDREXD, and STREXD instructions.</td>
</tr>
<tr>
<td>0b0011</td>
<td>If SynchPrim == 0b0001, adds the LDREX, STREX, CLREX, LDREXB, LDREXH, STREXB, and STREXH instructions.</td>
</tr>
</tbody>
</table>

All other combinations of SynchPrim and SynchPrim_frac are reserved.

In Armv8-A, the only permitted value is 0b0000.

**Barrier, bits [19:16]**

Indicates the implemented Barrier instructions in the A32 and T32 instruction sets. Defined values are:

<table>
<thead>
<tr>
<th>Barrier</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. Barrier operations are provided only as System instructions in the (coproc==0b1111) encoding space.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the DMB, DSB, and ISB barrier instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**SMC, bits [15:12]**

Indicates the implemented SMC instructions. Defined values are:

<table>
<thead>
<tr>
<th>SMC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SMC instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0001 and 0b0000.

If EL1 cannot use AArch32, then this field has the value 0b0000.

**Writeback, bits [11:8]**

Indicates the support for Writeback addressing modes. Defined values are:
### Writeback

<table>
<thead>
<tr>
<th>Writeback</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Basic support. Only the LDM, STM, PUSH, POP, SRS, and RFE instructions support writeback addressing modes. These instructions support all of their writeback addressing modes.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for all of the writeback addressing modes.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### WithShifts, bits [7:4]

Indicates the support for instructions with shifts. Defined values are:

<table>
<thead>
<tr>
<th>WithShifts</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Nonzero shifts supported only in MOV and shift instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for shifts of loads and stores over the range LSL 0-3.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001, and adds support for other constant shift options, both on load/store and other instructions.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds support for register-controlled shift options.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0100.

### Unpriv, bits [3:0]

Indicates the implemented unprivileged instructions. Defined values are:

<table>
<thead>
<tr>
<th>Unpriv</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. No T variant instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the LDRBT, LDRT, STRBT, and STRT instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the LDRHT, LDRSBT, LDRSHT, and STRHT instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

### Otherwise:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>

### Bits [63:0]

Reserved, UNKNOWN.

### Accessing the ID_ISAR4_EL1

Accesses to this register use the following encodings:

\[
\text{MRS <Xt>, ID_ISAR4_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_ISAR4_EL1;
elsif PSTATE.EL == EL2 then
  return ID_ISAR4_EL1;
elsif PSTATE.EL == EL3 then
  return ID_ISAR4_EL1;
The ID_ISAR5_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR1_EL1, ID_ISAR2_EL1, ID_ISAR3_EL1, and ID_ISAR4_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR5_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR5[31:0].

**Attributes**

ID_ISAR5_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR5_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<p>| | | | | | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
</tr>
<tr>
<td>VCMA</td>
<td>RDM</td>
<td>RES0</td>
<td>CRC32</td>
<td>SHA2</td>
<td>SHA1</td>
<td>AES</td>
<td>SEVL</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**VCMA, bits [31:28]**

Indicates AArch32 support for complex number addition and multiplication where numbers are stored in vectors. Defined values are:

<table>
<thead>
<tr>
<th>VCMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The VCMLA and VCADD instructions are not implemented in AArch32.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The VCMLA and VCADD instructions are implemented in AArch32.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FCMA implements the functionality identified by 0b0001.

In Armv8.0, Armv8.1, and Armv8.2, the only permitted value is 0b0000.

From Armv8.3, the only permitted value is 0b0001.
RDM, bits [27:24]
Indicates whether the VQRDMLAH and VQRDMLSH instructions are implemented in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>RDM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No VQRDMLAH and VQRDMLSH instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VQRDMLAH and VQRDMLSH instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RDM implements the functionality identified by the value 0b0001.

In Armv8.0, the only permitted value is 0b0000.
From Armv8.1, the only permitted value is 0b0001.

Bits [23:20]
Reserved, RES0.

CRC32, bits [19:16]
Indicates whether the CRC32 instructions are implemented in AArch32 state.

<table>
<thead>
<tr>
<th>CRC32</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No CRC32 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CRC32B, CRC32H, CRC32W, CRC32CEB, CRC32CH, and CRC32CW instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8.0, the permitted values are 0b0000 and 0b0001.
From Armv8.1, the only permitted value is 0b0001.

SHA2, bits [15:12]
Indicates whether the SHA2 instructions are implemented in AArch32 state.

<table>
<thead>
<tr>
<th>SHA2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA2 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the permitted values are 0b0000 and 0b0001.

SHA1, bits [11:8]
Indicates whether the SHA1 instructions are implemented in AArch32 state.

<table>
<thead>
<tr>
<th>SHA1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA1 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the permitted values are 0b0000 and 0b0001.

AES, bits [7:4]
Indicates whether the AES instructions are implemented in AArch32 state.
AES

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No AES instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AESE, AESD, AESMC, and AESIMC implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, plus VMULL (polynomial) instructions operating on 64-bit data quantities.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0010.

SEVL, bits [3:0]

Indicates whether the SEVL instruction is implemented in AArch32 state.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SEVL is implemented as a NOP.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SEVL is implemented as Send Event Local.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

Otherwise:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>0b11</td>
</tr>
<tr>
<td>62</td>
<td>0b0000</td>
</tr>
<tr>
<td>61</td>
<td>0b0000</td>
</tr>
<tr>
<td>60</td>
<td>0b0010</td>
</tr>
<tr>
<td>59</td>
<td>0b101</td>
</tr>
<tr>
<td>58</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>57</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>56</td>
<td>0b0000</td>
</tr>
<tr>
<td>55</td>
<td>0b0000</td>
</tr>
<tr>
<td>54</td>
<td>0b0010</td>
</tr>
<tr>
<td>53</td>
<td>0b101</td>
</tr>
<tr>
<td>52</td>
<td>0b11</td>
</tr>
<tr>
<td>51</td>
<td>0b0000</td>
</tr>
<tr>
<td>50</td>
<td>0b0000</td>
</tr>
<tr>
<td>49</td>
<td>0b0010</td>
</tr>
<tr>
<td>48</td>
<td>0b101</td>
</tr>
<tr>
<td>47</td>
<td>0b11</td>
</tr>
<tr>
<td>46</td>
<td>0b0000</td>
</tr>
<tr>
<td>45</td>
<td>0b0000</td>
</tr>
<tr>
<td>44</td>
<td>0b0010</td>
</tr>
<tr>
<td>43</td>
<td>0b101</td>
</tr>
<tr>
<td>42</td>
<td>0b11</td>
</tr>
<tr>
<td>41</td>
<td>0b0000</td>
</tr>
<tr>
<td>40</td>
<td>0b0000</td>
</tr>
<tr>
<td>39</td>
<td>0b0010</td>
</tr>
<tr>
<td>38</td>
<td>0b101</td>
</tr>
<tr>
<td>37</td>
<td>0b11</td>
</tr>
<tr>
<td>36</td>
<td>0b0000</td>
</tr>
<tr>
<td>35</td>
<td>0b0000</td>
</tr>
<tr>
<td>34</td>
<td>0b0010</td>
</tr>
<tr>
<td>33</td>
<td>0b101</td>
</tr>
<tr>
<td>32</td>
<td>0b11</td>
</tr>
<tr>
<td>31</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>30</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>29</td>
<td>0b0000</td>
</tr>
<tr>
<td>28</td>
<td>0b0000</td>
</tr>
<tr>
<td>27</td>
<td>0b0010</td>
</tr>
<tr>
<td>26</td>
<td>0b101</td>
</tr>
<tr>
<td>25</td>
<td>0b11</td>
</tr>
<tr>
<td>24</td>
<td>0b0000</td>
</tr>
<tr>
<td>23</td>
<td>0b0000</td>
</tr>
<tr>
<td>22</td>
<td>0b0010</td>
</tr>
<tr>
<td>21</td>
<td>0b101</td>
</tr>
<tr>
<td>20</td>
<td>0b11</td>
</tr>
<tr>
<td>19</td>
<td>0b0000</td>
</tr>
<tr>
<td>18</td>
<td>0b0000</td>
</tr>
<tr>
<td>17</td>
<td>0b0010</td>
</tr>
<tr>
<td>16</td>
<td>0b101</td>
</tr>
<tr>
<td>15</td>
<td>0b11</td>
</tr>
<tr>
<td>14</td>
<td>0b0000</td>
</tr>
<tr>
<td>13</td>
<td>0b0000</td>
</tr>
<tr>
<td>12</td>
<td>0b0010</td>
</tr>
<tr>
<td>11</td>
<td>0b101</td>
</tr>
<tr>
<td>10</td>
<td>0b11</td>
</tr>
<tr>
<td>9</td>
<td>0b0000</td>
</tr>
<tr>
<td>8</td>
<td>0b0000</td>
</tr>
<tr>
<td>7</td>
<td>0b0010</td>
</tr>
<tr>
<td>6</td>
<td>0b101</td>
</tr>
<tr>
<td>5</td>
<td>0b11</td>
</tr>
<tr>
<td>4</td>
<td>0b0000</td>
</tr>
<tr>
<td>3</td>
<td>0b0000</td>
</tr>
<tr>
<td>2</td>
<td>0b0010</td>
</tr>
<tr>
<td>1</td>
<td>0b101</td>
</tr>
<tr>
<td>0</td>
<td>0b11</td>
</tr>
</tbody>
</table>

Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_ISAR5_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_ISAR5_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() & HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return ID_ISAR5_EL1;
  elsif PSTATE.EL == EL2 then
    return ID_ISAR5_EL1;
  elsif PSTATE.EL == EL3 then
    return ID_ISAR5_EL1;
**ID_ISAR6_EL1, AArch32 Instruction Set Attribute Register 6**

The ID_ISAR6_EL1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0_EL1, ID_ISAR1_EL1, ID_ISAR2_EL1, ID_ISAR3_EL1, ID_ISAR4_EL1 and ID_ISAR5_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_ISAR6_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_ISAR6[31:0].

**Note**

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_ISAR6_EL1 is a 64-bit register.

**Field descriptions**

The ID_ISAR6_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | I8MM | BF16 | SPECRES | SB | FHM | DP | JSCVT |

**Bits [63:28]**

Reserved, RES0.

**I8MM, bits [27:24]**

Indicates support for Advanced SIMD and floating-point Int8 matrix multiplication instructions in AArch32 state. Defined values of this field are:

<table>
<thead>
<tr>
<th>I8MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Int8 matrix multiplication instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VSMMLA, VSUDOT, VUMMLA, VUSMMLA, and VUSDOT instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.
FEAT AA32I8MM implements the functionality identified by 0b0001.

**BF16, bits [23:20]**

Indicates support for Advanced SIMD and floating-point BF16 instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>BF16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>BF16 instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VCVT, VCVTB, VCVTT, VDOT, VFMAB, VFMAT, and VMMLA instructions with BF16 operand or result types are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AA32BF16 implements the functionality identified by 0b0001.

**SPECRES, bits [19:16]**

Indicates support for Speculation invalidation instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>SPECRES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Prediction invalidation instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CFPRCTX, DVPRCTX, and CPRPRCTX instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SPECRES implements the functionality identified by 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**SB, bits [15:12]**

Indicates support for the SB instruction in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>SB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SB instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SB instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_SB implements the functionality identified by 0b0001.

From Armv8.5, the only permitted value is 0b0001.

**FHM, bits [11:8]**

Indicates support for Advanced SIMD and floating-point VFMAL and VFMSL instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>FHM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>VFMAL and VMFSL instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VFMAL and VMFSL instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FHM implements the functionality identified by 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

**DP, bits [7:4]**

Indicates support for Advanced SIMD and floating-point VFMAL and VFMSL instructions in AArch32 state. Defined values are:
<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Dot product instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>UDOT and VSDOT instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DotProd implements the functionality identified by 0b0001.

In Armv8.2, the permitted values are 0b0000 and 0b0001.

From Armv8.4, the only permitted value is 0b0001.

**JSCVT, bits [3:0]**

Indicates support for the VJCVT instruction in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>JSCVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The VJCVT instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The VJCVT instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_JSCVT implements the functionality identified by 0b0001.

In Armv8.0, Armv8.1, and Armv8.2, the only permitted value is 0b0000.

From Armv8.3, if Advanced SIMD or Floating-point is implemented, the only permitted value is 0b0001.

From Armv8.3, if Advanced SIMD or Floating-point is not implemented, the only permitted value is 0b0000.

**Otherwise:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, UNKNOWN.</td>
<td></td>
</tr>
</tbody>
</table>

**Accessing the ID_ISAR6_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ID_ISAR6_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!IsZero(ID_ISAR6_EL1) || boolean IMPLEMENTATION_DEFINED "ID_ISAR6_EL1
trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_ISAR6_EL1;
elsif PSTATE.EL == EL2 then
  return ID_ISAR6_EL1;
elsif PSTATE.EL == EL3 then
  return ID_ISAR6_EL1;
The ID_MMFR0_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with ID_MMFR1_EL1, ID_MMFR2_EL1, ID_MMFR3_EL1, and ID_MMFR4_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_MMFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR0[31:0].

**Attributes**

ID_MMFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_MMFR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Reserved, RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>InnerShr</td>
<td>FCSE</td>
</tr>
<tr>
<td>31 30 29</td>
<td>28 27 26 25</td>
</tr>
</tbody>
</table>

**InnerShr, bits [31:28]**

Innermost Shareability. Indicates the innermost shareability domain implemented. Defined values are:

<table>
<thead>
<tr>
<th>InnerShr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Implemented as Non-cacheable.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented with hardware coherency support.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Shareability ignored.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8 the permitted values are 0b0000, 0b0001, and 0b1111.

This field is valid only if the implementation supports two levels of shareability, as indicated by ID_MMFR0_EL1.ShareLvl having the value 0b0001.

When ID_MMFR0_EL1.ShareLvl is zero, this field is UNKNOWN.
FCSE, bits [27:24]

Indicates whether the implementation includes the FCSE. Defined values are:

<table>
<thead>
<tr>
<th>FCSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for FCSE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8 the only permitted value is 0b0000.

AuxReg, bits [23:20]

Auxiliary Registers. Indicates support for Auxiliary registers. Defined values are:

<table>
<thead>
<tr>
<th>AuxReg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Auxiliary Control Register only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for Auxiliary Fault Status Registers (AIFSR and ADFSR)</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8 the only permitted value is 0b0010.

Note

Accesses to unimplemented Auxiliary registers are UNDEFINED.

TCM, bits [19:16]

Indicates support for TCMs and associated DMAs. Defined values are:

<table>
<thead>
<tr>
<th>TCM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support is IMPLEMENTATION DEFINED. Armv7 requires this setting.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for TCM only. Armv6 implementation.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for TCM and DMA, Armv6 implementation.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the only permitted value is 0b0000.

ShareLvl, bits [15:12]

Shareability Levels. Indicates the number of shareability levels implemented. Defined values are:

<table>
<thead>
<tr>
<th>ShareLvl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>One level of shareability implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Two levels of shareability implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8 the only permitted value is 0b0001.

OuterShr, bits [11:8]

Outermost Shareability. Indicates the outermost shareability domain implemented. Defined values are:
OuterShr | Meaning
--- | ---
0b0000 | Implemented as Non-cacheable.
0b0001 | Implemented with hardware coherency support.
0b1111 | Shareability ignored.

All other values are reserved.

From Armv8 the permitted values are 0b0000, 0b0001, and 0b1111.

**PMSA, bits [7:4]**

Indicates support for a PMSA. Defined values are:

<table>
<thead>
<tr>
<th>PMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for IMPLEMENTATION DEFINED PMSA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for PMSAv6, with a Cache Type Register implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for PMSAv7, with support for memory subsections. Armv7-R profile.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the only permitted value is 0b0000.

**VMSA, bits [3:0]**

Indicates support for a VMSA. Defined values are:

<table>
<thead>
<tr>
<th>VMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for IMPLEMENTATION DEFINED VMSA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for VMSAv6, with Cache and TLB Type Registers implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for VMSAv7, with support for remapping and the Access flag. Armv7-A profile.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds support for the PXN bit in the Short-descriptor translation table format descriptors.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As for 0b0100, and adds support for the Long-descriptor translation table format.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the only permitted value is 0b0101.

**Otherwise:**

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Reserved, UNKNOWN.

**Accessing the ID_MMFR0_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, ID_MMFR0_EL1

| op0 | op1 | CRn | CRm | op2 |
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if;
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_MMFR0_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    return ID_MMFR0_EL1;
elsif PSTATE.EL == EL3 then
    return ID_MMFR0_EL1;
The ID_MMFR1_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with ID_MMFR0_EL1, ID_MMFR2_EL1, ID_MMFR3_EL1, and ID_MMFR4_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_MMFR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR1[31:0].

**Attributes**

ID_MMFR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_MMFR1_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | BPred | L1TstCln | L1Uni | L1Hvd | L1UniSW | L1HvdSW | L1UniVA | L1HvdVA |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**BPred, bits [31:28]**

Branch Predictor. Indicates branch predictor management requirements. Defined values are:
### BPred

<table>
<thead>
<tr>
<th>BPred</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No branch predictor, or no MMU present. Implies a fixed MPU configuration.</td>
</tr>
</tbody>
</table>
| 0b0001 | Branch predictor requires flushing on:  
  - Enabling or disabling a stage of address translation.  
  - Writing new data to instruction locations.  
  - Writing new mappings to the translation tables.  
  - Changes to the TTBR0, TTBR1, or TTBCR registers.  
  - Changes to the ContextID or ASID, or to the FCSE ProcessID if this is supported. |
| 0b0010 | Branch predictor requires flushing on:  
  - Enabling or disabling a stage of address translation.  
  - Writing new data to instruction locations.  
  - Writing new mappings to the translation tables.  
  - Any change to the TTBR0, TTBR1, or TTBCR registers without a change to the corresponding ContextID or ASID, or FCSE ProcessID if this is supported. |
| 0b0011 | Branch predictor requires flushing only on writing new data to instruction locations. |
| 0b0100 | For execution correctness, branch predictor requires no flushing at any time. |

All other values are reserved.

In Armv8-A, the permitted values are 0b0010, 0b0011, and 0b0100. For values other than 0b0000 and 0b0100 the Arm Architecture Reference Manual, or the product documentation, might give more information about the required maintenance.

### L1TstCln, bits [27:24]

Level 1 cache Test and Clean. Indicates the supported Level 1 data cache test and clean operations, for Harvard or unified cache implementations. Defined values are:

<table>
<thead>
<tr>
<th>L1TstCln</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
</tbody>
</table>
| 0b0001   | Supported Level 1 data cache test and clean operations are:  
  - Test and clean data cache. |
| 0b0010   | As for 0b0001, and adds:  
  - Test, clean, and invalidate data cache. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### L1Uni, bits [23:20]

Level 1 Unified cache. Indicates the supported entire Level 1 cache maintenance operations for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1Uni</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
</tbody>
</table>
| 0b0001  | Supported entire Level 1 cache operations are:  
  - Invalidate cache, including branch predictor if appropriate.  
  - Invalidate branch predictor, if appropriate. |
| 0b0010  | As for 0b0001, and adds:  
  - Clean cache, using a recursive model that uses the cache dirty status bit.  
  - Clean and invalidate cache, using a recursive model that uses the cache dirty status bit. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.
L1Hvd, bits [19:16]

Level 1 Harvard cache. Indicates the supported entire Level 1 cache maintenance operations for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1Hvd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported entire Level 1 cache operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache, including branch predictor if appropriate.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor, if appropriate.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache and instruction cache, including branch predictor if appropriate.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

L1UniSW, bits [15:12]

Level 1 Unified cache by Set/Way. Indicates the supported Level 1 cache line maintenance operations by set/way, for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1UniSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 unified cache line maintenance operations by set/way are:</td>
</tr>
<tr>
<td></td>
<td>• Clean cache line by set/way.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate cache line by set/way.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate cache line by set/way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

L1HvdSW, bits [11:8]

Level 1 Harvard cache by Set/Way. Indicates the supported Level 1 cache line maintenance operations by set/way, for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache line maintenance operations by set/way are:</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache line by set/way.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache line by set/way.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache line by set/way.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache line by set/way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.
L1UniVA, bits [7:4]

Level 1 Unified cache by Virtual Address. Indicates the supported Level 1 cache line maintenance operations by VA, for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1UniVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 unified cache line maintenance operations by VA are:</td>
</tr>
<tr>
<td></td>
<td>• Clean cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate cache line by VA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor by VA, if branch predictor is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

L1HvdVA, bits [3:0]

Level 1 Harvard cache by Virtual Address. Indicates the supported Level 1 cache line maintenance operations by VA, for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache line maintenance operations by VA are:</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean instruction cache line by VA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor by VA, if branch predictor is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

Otherwise:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
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<tr>
<td>58</td>
<td></td>
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<td>57</td>
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<td>56</td>
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<td>53</td>
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<td>52</td>
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<td>51</td>
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<td>49</td>
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<td>47</td>
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<td>46</td>
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<td>45</td>
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<td>44</td>
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<td>43</td>
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<td>42</td>
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<td>37</td>
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<td>36</td>
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<td>33</td>
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<tr>
<td>32</td>
<td></td>
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<tr>
<td>31</td>
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<td>30</td>
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<td>29</td>
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<td>28</td>
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<td>27</td>
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<td>26</td>
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<td>25</td>
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<td>24</td>
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<td>23</td>
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<td>22</td>
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<td>21</td>
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<td>20</td>
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<td>19</td>
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<tr>
<td>17</td>
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<tr>
<td>16</td>
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<tr>
<td>15</td>
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<tr>
<td>14</td>
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<td>13</td>
<td></td>
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<tr>
<td>12</td>
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<td>11</td>
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<tr>
<td>10</td>
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<tr>
<td>9</td>
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<tr>
<td>8</td>
<td></td>
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<tr>
<td>7</td>
<td></td>
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<tr>
<td>6</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Reserved, UNKNOWN.

Accessing the ID_MMFR1_EL1

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS &lt;Xt&gt;, ID_MMFR1_EL1</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_MMFR1_EL1;
elsif PSTATE.EL == EL2 then
  return ID_MMFR1_EL1;
elsif PSTATE.EL == EL3 then
  return ID_MMFR1_EL1;
The ID_MMFR2_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with ID_MMFR0_EL1, ID_MMFR1_EL1, ID_MMFR3_EL1, and ID_MMFR4_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_MMFR2_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR2[31:0].

**Attributes**

ID_MMFR2_EL1 is a 64-bit register.

**Field descriptions**

The ID_MMFR2_EL1 bit assignments are:

### When AArch32 is supported at any Exception level:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | HWAccFlg | WFIStall | MemBarr | UniTLB | HvdTLB | L1HvdRng | L1HvdBG | L1HvdFG |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:32]

Reserved, RES0.

**HWAccFlg, bits [31:28]**

Hardware Access Flag. In earlier versions of the Arm Architecture, this field indicates support for a Hardware Access flag, as part of the VMSAv7 implementation. Defined values are:

<table>
<thead>
<tr>
<th>HWAccFlg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for VMSAv7 Access flag, updated in hardware.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the only permitted value is 0b0000.

**WFIStall, bits [27:24]**

Wait For Interrupt Stall. Indicates the support for Wait For Interrupt (WFI) stalling. Defined values are:
### WFIStall

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for WFI stalling.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the permitted values are 0b0000 and 0b0001.

### MemBarr, bits [23:20]

Memory Barrier. Indicates the supported memory barrier System instructions in the (coproc==0b1111) encoding space:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported memory barrier System instructions are:</td>
</tr>
<tr>
<td></td>
<td>• Data Synchronization Barrier (DSB).</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Instruction Synchronization Barrier (ISB).</td>
</tr>
<tr>
<td></td>
<td>• Data Memory Barrier (DMB).</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the only permitted value is 0b0010.

Arm deprecates the use of these operations. ID_ISAR4.Barrier_intrs indicates the level of support for the preferred barrier instructions.

### UniTLB, bits [19:16]

Unified TLB. Indicates the supported TLB maintenance operations, for a unified TLB implementation. Defined values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported unified TLB maintenance operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate all entries in the TLB.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate TLB entry by VA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate TLB entries by ASID match.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction TLB and data TLB entries by VA All ASID. This is a shared unified TLB operation.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate Hyp mode unified TLB entry by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate entire Non-secure PL1&amp;0 unified TLB.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate entire Hyp mode unified TLB.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As for 0b0100, and adds the following operations:</td>
</tr>
<tr>
<td></td>
<td>TLBIMVALIS, TLBIMVAALIS, TLBIMVALHIS, TLBIMVAL, TLBIMVAAL, TLBIMVALH.</td>
</tr>
<tr>
<td>0b0110</td>
<td>As for 0b0101, and adds the following operations:</td>
</tr>
<tr>
<td></td>
<td>TLBIIIPAS2IS, TLBIIIPAS2LIS, TLBIIIPAS2, TLBIIIPAS2L.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0110.

### HvdTLB, bits [15:12]

If the Unified TLB field (UniTLB, bits [19:16]) is not 0000, then the meaning of this field is IMPLEMENTATION DEFINED. Arm deprecates the use of this field by software.

### L1HvdRng, bits [11:8]

Level 1 Harvard cache Range. Indicates the supported Level 1 cache maintenance range operations, for a Harvard cache implementation. Defined values are:
Meaning

<table>
<thead>
<tr>
<th>L1HvdRng</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache maintenance range operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache range by VA.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the only permitted value is 0b0000.

L1HvdBG, bits [7:4]

Level 1 Harvard cache Background fetch. Indicates the supported Level 1 cache background fetch operations, for a Harvard cache implementation. When supported, background fetch operations are non-blocking operations. Defined values are:

Meaning

<table>
<thead>
<tr>
<th>L1HvdBG</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache background fetch operations are:</td>
</tr>
<tr>
<td></td>
<td>• Fetch instruction cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Fetch data cache range by VA.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the only permitted value is 0b0000.

L1HvdFG, bits [3:0]

Level 1 Harvard cache Foreground fetch. Indicates the supported Level 1 cache foreground fetch operations, for a Harvard cache implementation. When supported, foreground fetch operations are blocking operations. Defined values are:

Meaning

<table>
<thead>
<tr>
<th>L1HvdFG</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache foreground fetch operations are:</td>
</tr>
<tr>
<td></td>
<td>• Fetch instruction cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Fetch data cache range by VA.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8, the only permitted value is 0b0000.

Otherwise:

63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32

UNKNOWN

UNKNOWN

Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_MMFR2_EL1

Accesses to this register use the following encodings:
MRS <Xt>, ID.MMFR2_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID.MMFR2_EL1;
    end
elsif PSTATE.EL == EL2 then
    return ID.MMFR2_EL1;
else PSTATE.EL == EL3 then
    return ID.MMFR2_EL1;
```
The ID_MMFR3_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state. Must be interpreted with ID_MMFR0_EL1, ID_MMFR1_EL1, ID_MMFR2_EL1, and ID_MMFR4_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_MMFR3_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR3[31:0].

**Attributes**

ID_MMFR3_EL1 is a 64-bit register.

**Field descriptions**

The ID_MMFR3_EL1 bit assignments are:

When AArch32 is supported at any Exception level:

<table>
<thead>
<tr>
<th></th>
<th>RES0</th>
<th>Supersec</th>
<th>CMemSz</th>
<th>CohWalk</th>
<th>PAN</th>
<th>MaintBcst</th>
<th>BPMaint</th>
<th>CMaintSW</th>
<th>CMaintVA</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:32</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:32]

Reserved, RES0.

**Supersec, bits [31:28]**

Supersections. On a VMSA implementation, indicates whether Supersections are supported. Defined values are:

<table>
<thead>
<tr>
<th>Supersec</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Supersections supported.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Supersections not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b1111.

**CMemSz, bits [27:24]**

Cached Memory Size. Indicates the physical memory size supported by the caches. Defined values are:
<table>
<thead>
<tr>
<th>CMemSz</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>4GB, corresponding to a 32-bit physical address range.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64GB, corresponding to a 36-bit physical address range.</td>
</tr>
<tr>
<td>0b0010</td>
<td>1TB or more, corresponding to a 40-bit or larger physical address range.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000, 0b0001, and 0b0010.

**CohWalk, bits [23:20]**

Coherent Walk. Indicates whether Translation table updates require a clean to the Point of Unification. Defined values are:

<table>
<thead>
<tr>
<th>CohWalk</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Updates to the translation tables require a clean to the Point of Unification to ensure visibility by subsequent translation table walks.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Updates to the translation tables do not require a clean to the Point of Unification to ensure visibility by subsequent translation table walks.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**PAN, bits [19:16]**

Privileged Access Never. Indicates support for the PAN bit in CPSR, SPSR, and DSPSR in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>PAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PAN not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PAN supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>PAN supported and ATS1CPRP and ATS1CPWP instructions supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PAN implements the functionality identified by the value 0b0001.

FEAT_PAN2 implements the functionality added by the value 0b0010.

In Armv8.1, the value 0b0000 is not permitted.

From Armv8.2, the only permitted value is 0b0010.

**MaintBcst, bits [15:12]**

Maintenance Broadcast. Indicates whether Cache, TLB, and branch predictor operations are broadcast. Defined values are:

<table>
<thead>
<tr>
<th>MaintBcst</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Cache, TLB, and branch predictor operations only affect local structures.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Cache and branch predictor operations affect structures according to shareability and defined behavior of instructions. TLB operations only affect local structures.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Cache, TLB, and branch predictor operations affect structures according to shareability and defined behavior of instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.
BPMaint, bits [11:8]

Branch Predictor Maintenance. Indicates the supported branch predictor maintenance operations in an implementation with hierarchical cache maintenance operations. Defined values are:

<table>
<thead>
<tr>
<th>BPMaint</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported branch predictor maintenance operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate all branch predictors.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictors by VA.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

CMaintSW, bits [7:4]

Cache Maintenance by Set/Way. Indicates the supported cache maintenance operations by set/way, in an implementation with hierarchical caches. Defined values are:

<table>
<thead>
<tr>
<th>CMaintSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported hierarchical cache maintenance instructions by set/way are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache by set/way.</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache by set/way.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache by set/way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

In a unified cache implementation, the data cache maintenance operations apply to the unified caches.

CMaintVA, bits [3:0]

Cache Maintenance by Virtual Address. Indicates the supported cache maintenance operations by VA, in an implementation with hierarchical caches. Defined values are:

<table>
<thead>
<tr>
<th>CMaintVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported hierarchical cache maintenance operations by VA are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate all instruction cache entries.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

In a unified cache implementation, data cache maintenance operations apply to the unified caches, and the instruction cache maintenance instructions are not implemented.

Otherwise:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNKNOWN</td>
</tr>
<tr>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>
Bits [63:0]

Reserved, UNKNOWN.

### Accessing the ID_MMFR3_EL1

Accesses to this register use the following encodings:

```
MRS <Xt>, ID_MMFR3_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```java
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_MMFR3_EL1;
elsif PSTATE.EL == EL2 then
  return ID_MMFR3_EL1;
elsif PSTATE.EL == EL3 then
  return ID_MMFR3_EL1;
```

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The ID_MMFR4_EL1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state. Must be interpreted with ID_MMFR0_EL1, ID_MMFR1_EL1, ID_MMFR2_EL1, and ID_MMFR3_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_MMFR4_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR4[31:0].

**Attributes**

ID_MMFR4_EL1 is a 64-bit register.

**Field descriptions**

The ID_MMFR4_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th></th>
<th>EVT</th>
<th>CCIDX</th>
<th>LSM</th>
<th>HPDS</th>
<th>CnP</th>
<th>XNX</th>
<th>AC2</th>
<th>SpecSEI</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
</tr>
<tr>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
</tr>
<tr>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:32]

Reserved, RES0.

**EVT, bits [31:28]**

Enhanced Virtualization Traps. If EL2 is implemented, indicates support for the HCR2\{TTLBIS, TOCU, TICAB, TID4\} traps. Defined values are:

<table>
<thead>
<tr>
<th>EVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>HCR2{TTLBIS, TOCU, TICAB, TID4} traps are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>HCR2{TOCU, TICAB, TID4} traps are supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>HCR2{TTLBIS, TOCU, TICAB, TID4} trap is not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT EVT implements the functionality identified by the values 0b0001 and 0b0010.

If EL2 is not implemented supporting AArch32, the only permitted value is 0b0000.

In Armv8.2, the permitted values are 0b0000, 0b0001, and 0b0010.
From Armv8.5, the permitted values are:
- 0b0000 when EL2 is not implemented.
- 0b0010 when EL2 is implemented.

**CCIDX, bits [27:24]**

Support for use of the revised CCSIDR format and the presence of the CCSIDR2 is indicated. Defined values are:

<table>
<thead>
<tr>
<th>CCIDX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>32-bit format implemented for all levels of the CCSIDR, and the CCSIDR2 register is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64-bit format implemented for all levels of the CCSIDR, and the CCSIDR2 register is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CCIDX implements the functionality identified by 0b0001.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

**LSM, bits [23:20]**

Indicates support for LSMAOE and nTLSMD bits in HSCTL.R and SCTLR. Defined values are:

<table>
<thead>
<tr>
<th>LSM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>LSMAOE and nTLSMD bits not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LSMAOE and nTLSMD bits supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LSMAOC implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

**HPDS, bits [19:16]**

Hierarchical permission disables bits in translation tables. Defined values are:

<table>
<thead>
<tr>
<th>HPDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Disabling of hierarchical controls not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supports disabling of hierarchical controls using the TTBCR2,HPD0, TTBCR2,HPD1, and HTCR,HPD bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for value 0b0001, and adds possible hardware allocation of bits[62:59] of the translation table descriptors from the final lookup level for IMPLEMENTATION DEFINED use.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AA32HPD implements the functionality identified by the value 0b0001.

FEAT_HPDS2 implements the functionality added by the value 0b0010.

**Note**

The value 0b0000 implies that the encoding for TTBCR2 is UNDEFINED.

**CnP, bits [15:12]**

Common not Private translations. Defined values are:

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Common not Private translations not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Common not Private translations supported.</td>
</tr>
</tbody>
</table>
All other values are reserved.

FEAT_TTCNP implements the functionality identified by the value 0b0001.

From Armv8.2 the only permitted value is 0b0001.

**XNX, bits [11:8]**

Support for execute-never control distinction by Exception level at stage 2. Defined values are:

<table>
<thead>
<tr>
<th>XNX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_XNX implements the functionality identified by the value 0b0001.

When FEAT_XNX is implemented:

- If all of the following conditions are true, it is IMPLEMENTATION DEFINED whether the value of ID_MMFR4_EL1.XNX is 0b0000 or 0b0001:
  - ID_AA64MMFR1_EL1.XNX ==1.
  - EL2 cannot use AArch32.
  - EL1 can use AArch32.
- If EL2 can use AArch32 then the only permitted value is 0b0001.

**AC2, bits [7:4]**

Indicates the extension of the ACTLR and HACTLR registers using ACTLR2 and HACTLR2. Defined values are:

<table>
<thead>
<tr>
<th>AC2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>ACTLR2 and HACTLR2 are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>ACTLR2 and HACTLR2 are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8.0 and Armv8.1 the permitted values are 0b0000 and 0b0001.

From Armv8.2, the only permitted value is 0b0001.

**SpecSEI, bits [3:0]**

Describes whether the PE can generate SError interrupt exceptions from speculative reads of memory, including speculative instruction fetches. The defined values of this field are:

<table>
<thead>
<tr>
<th>SpecSEI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The PE never generates an SError interrupt due to an External abort on a speculative read.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The PE might generate an SError interrupt due to an External abort on a speculative read.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Otherwise:**

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
<th>UNKNOWN</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>
Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_MMFR4_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_MMFR4_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!IsZero(ID_MMFR4_EL1) || boolean IMPLEMENTATION_DEFINED "ID_MMFR4_EL1 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_MMFR4_EL1;
elsif PSTATE.EL == EL2 then
  return ID_MMFR4_EL1;
else if PSTATE.EL == EL3 then
  return ID_MMFR4_EL1;
The ID_MMFR5_EL1 characteristics are:

Purpose

Provides information about the implemented memory model and memory management support in AArch32 state.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

Configuration

AArch64 System register ID_MMFR5_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_MMFR5[31:0].

Attributes

ID_MMFR5_EL1 is a 64-bit register.

Field descriptions

The ID_MMFR5_EL1 bit assignments are:

When AArch32 is supported at any Exception level:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    | RES0|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Bits [63:4]

Reserved, RES0.

ETS, bits [3:0]

Support for Enhanced Translation Synchronization. Defined values are:

<table>
<thead>
<tr>
<th>ETS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Enhanced Translation Synchronization is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Enhanced Translation Synchronization is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ETS implements the functionality identified by the value 0b0001.

From Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.7, the only permitted value is 0b0001.
Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_MMFR5_EL1

Accesses to this register use the following encodings:

\[
\text{MRS <Xt>, ID_MMFR5_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
else
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && (!IsZero(ID_MMFR5_EL1) || boolean IMPLEMENTATION_DEFINED "ID_MMFR5_EL1 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return ID_MMFR5_EL1;
    elsif PSTATE.EL == EL2 then
        return ID_MMFR5_EL1;
    elsif PSTATE.EL == EL3 then
        return ID_MMFR5_EL1;
The ID_PFR0_EL1 characteristics are:

**Purpose**

Gives top-level information about the instruction sets supported by the PE in AArch32 state.

Must be interpreted with ID_PFR1_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_PFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_PFR0[31:0].

**Attributes**

ID_PFR0_EL1 is a 64-bit register.

**Field descriptions**

The ID_PFR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Reserved, RES0</th>
</tr>
</thead>
</table>

**RAS, bits [31:28]**

RAS Extension version. Defined values are:

<table>
<thead>
<tr>
<th>RAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No RAS Extension.</td>
</tr>
<tr>
<td>0b0001</td>
<td>RAS Extension present.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_RASv1p1 present. As 0b0001, and adds support for additional ERXMISC&lt;m&gt; System registers. Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ERR&lt;n&gt;STATUS and support for the optional RAS Timestamp Extension.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RAS implements the functionality identified by the value 0b0001.

FEAT_RASv1p1 implements the functionality identified by the value 0b0010.

In Armv8.0 and Armv8.1, the permitted values are 0b0000 and 0b0001.
In Armv8.2, the only permitted value is 0b0001.

From Armv8.4, if FEAT_DoubleFault is implemented, the only permitted value is 0b0010.

From Armv8.4, when FEAT_DoubleFault is not implemented, and ERRIDR_EL1.NUM is 0, the permitted values are IMPLEMENTATION DEFINED 0b0001 or 0b0010.

---

**Note**

When the value of this field is 0b0001, ID_PFR2_EL1.RAS_frac indicates whether FEAT_RASv1p1 is implemented.

---

**DIT, bits [27:24]**

Data Independent Timing. Defined values are:

<table>
<thead>
<tr>
<th>DIT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>AArch32 does not guarantee constant execution time of any instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AArch32 provides the PSTATE.DIT mechanism to guarantee constant execution time of certain instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DIT implements the functionality identified by the value 0b0001.

From Armv8.4, the only permitted value is 0b0001.

**AMU, bits [23:20]**

Indicates support for Activity Monitors Extension. Defined values are:

<table>
<thead>
<tr>
<th>AMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Activity Monitors Extension is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_AMUv1 is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_AMUv1p1 is implemented. As 0b0001 and adds support for virtualization of the activity monitor event counters.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AMUv1 implements the functionality identified by the value 0b0001.

FEAT_AMUv1p1 implements the functionality identified by the value 0b0010.

In Armv8.0, the only permitted value is 0b0000.

In Armv8.4, the permitted values are 0b0000 and 0b0001.

From Armv8.6, the permitted values are 0b0000, 0b0001, and 0b0010.

**CSV2, bits [19:16]**

Speculative use of out of context branch targets. Defined values are:

<table>
<thead>
<tr>
<th>CSV2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>This Device does not disclose whether branch targets trained in one hardware described context can affect speculative execution in a different hardware described context.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Branch targets trained in one hardware described context can only affect speculative execution in a different hardware described context in a hard-to-determine way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CSV2 implements the functionality identified by 0b0001.
From Armv8.5, the only permitted value is \texttt{0b0001}.

**State3, bits [15:12]**

T32EE instruction set support. Defined values are:

<table>
<thead>
<tr>
<th>State3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>T32EE instruction set implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0000}.

**State2, bits [11:8]**

Jazelle extension support. Defined values are:

<table>
<thead>
<tr>
<th>State2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Jazelle extension implemented, without clearing of JOSCR.CV on exception entry.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Jazelle extension implemented, with clearing of JOSCR.CV on exception entry.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0001}.

**State1, bits [7:4]**

T32 instruction set support. Defined values are:

<table>
<thead>
<tr>
<th>State1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>T32 instruction set not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>T32 encodings before the introduction of Thumb-2 technology implemented:</td>
</tr>
<tr>
<td></td>
<td>• All instructions are 16-bit.</td>
</tr>
<tr>
<td></td>
<td>• A BL or BLX is a pair of 16-bit instructions.</td>
</tr>
<tr>
<td></td>
<td>• 32-bit instructions other than BL and BLX cannot be encoded.</td>
</tr>
<tr>
<td>0b0011</td>
<td>T32 encodings after the introduction of Thumb-2 technology implemented, for all 16-bit and 32-bit T32 basic instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0011}.

**State0, bits [3:0]**

A32 instruction set support. Defined values are:

<table>
<thead>
<tr>
<th>State0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>A32 instruction set not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>A32 instruction set implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0001}. 
Otherwise:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
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<th>38</th>
<th>37</th>
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<th>35</th>
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<th>33</th>
<th>32</th>
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<td>31</td>
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<td>24</td>
<td>23</td>
<td>22</td>
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<td>16</td>
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<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits [63:0]

Reserved, UNKNOWN.

**Accessing the ID_PFR0_EL1**

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ ID_PFR0_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ID_PFR0_EL1;
elsif PSTATE.EL == EL2 then
  return ID_PFR0_EL1;
elsif PSTATE.EL == EL3 then
  return ID_PFR0_EL1;
ID_PFR1_EL1, AArch32 Processor Feature Register 1

The ID_PFR1_EL1 characteristics are:

**Purpose**

Gives information about the AArch32 programmers' model.

Must be interpreted with ID_PFR0_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_PFR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_PFR1[31:0].

**Attributes**

ID_PFR1_EL1 is a 64-bit register.

**Field descriptions**

The ID_PFR1_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>GIC</td>
</tr>
<tr>
<td>61</td>
<td>Virt_frac, bits [27:24]</td>
</tr>
<tr>
<td>60</td>
<td>Sec_frac, bits [23:20]</td>
</tr>
<tr>
<td>59</td>
<td>GenTimer</td>
</tr>
<tr>
<td>58</td>
<td>Virtualization, bits [15:12]</td>
</tr>
<tr>
<td>57</td>
<td>MProgMod</td>
</tr>
<tr>
<td>56</td>
<td>Security</td>
</tr>
<tr>
<td>55</td>
<td>ProgMod</td>
</tr>
</tbody>
</table>

GIC, bits [31:28]

System register GIC CPU interface. Defined values are:

<table>
<thead>
<tr>
<th>GIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>GIC CPU interface system registers not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>System register interface to versions 3.0 and 4.0 of the GIC CPU interface is supported.</td>
</tr>
<tr>
<td>0b0011</td>
<td>System register interface to version 4.1 of the GIC CPU interface is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Virt_frac, bits [27:24]

Virtualization fractional field. When the Virtualization field is 0b0000, determines the support for features from the ARMv7 Virtualization Extensions. Defined values are:
**Virt_frac**

<table>
<thead>
<tr>
<th>Virt_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No features from the ARMv7 Virtualization Extensions are implemented.</td>
</tr>
</tbody>
</table>
| 0b0001    | The following features of the ARMv7 Virtualization Extensions are implemented:  
          | • The SCR.SIF bit, if EL3 is implemented.  
          | • The modifications to the SCR.AW and SCR.FW bits described in the Virtualization Extensions, if EL3 is implemented.  
          | • The MSR (banked register) and MRS (banked register) instructions.  
          | • The ERET instruction. |

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL2 is implemented.
- 0b0001 when EL2 is not implemented.

This field is only valid when the value of ID_PFR1_EL1.Virtualization is 0, otherwise it holds the value 0b0000.

**Note**

The ID_ISAR registers do not identify whether the instructions added by the ARMv7 Virtualization Extensions are implemented.

---

**Sec_frac, bits [23:20]**

Security fractional field. When the Security field is 0b0000, determines the support for features from the ARMv7 Security Extensions. Defined values are:

<table>
<thead>
<tr>
<th>Sec_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No features from the ARMv7 Security Extensions are implemented.</td>
</tr>
</tbody>
</table>
| 0b0001   | The following features from the ARMv7 Security Extensions are implemented:  
          | • The VBAR register.  
          | • The TTBCR.PD0 and TTBCR.PD1 bits. |
| 0b0010   | As for 0b0001, plus the ability to access Secure or Non-secure physical memory is supported. |

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL3 is implemented.
- 0b0001 or 0b0010 when EL3 is not implemented.

This field is only valid when the value of ID_PFR1_EL1.Security is 0, otherwise it holds the value 0b0000.

**GenTimer, bits [19:16]**

Generic Timer support. Defined values are:

<table>
<thead>
<tr>
<th>GenTimer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Generic Timer is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Generic Timer is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Generic Timer is implemented, and also includes support for CNTHCTL.EVNTIS and CNTKCTL.EVNTIS fields, and CNTPTCSS and CNTVCTSS counter views.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ECV implements the functionality identified by the value 0b0010.

In Armv8.0, Armv8.1, Armv8.2, Armv8.3, Armv8.4, and Armv8.5, the only permitted value is 0b0001.
From Armv8.6, the only permitted value is 0b0010.

**Virtualization, bits [15:12]**

Virtualization support. Defined values are:

<table>
<thead>
<tr>
<th>Virtualization</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL2, Hyp mode, and the HVC instruction not</td>
</tr>
<tr>
<td></td>
<td>implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL2, Hyp mode, the HVC instruction, and all the</td>
</tr>
<tr>
<td></td>
<td>features described by Virt_frac == 0b0001</td>
</tr>
<tr>
<td></td>
<td>implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL2 is not implemented.
- 0b0001 when EL2 is implemented.

In an implementation that includes EL2, if EL2 cannot use AArch32 but EL1 can use AArch32 then this field has the value 0b0001.

If EL1 cannot use AArch32 then this field has the value 0b0000.

**Note**

The ID-ISARs do not identify whether the HVC instruction is implemented.

**MProgMod, bits [11:8]**

M profile programmers' model support. Defined values are:

<table>
<thead>
<tr>
<th>MProgMod</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for two-stack programmers' model.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the only permitted value is 0b0000.

**Security, bits [7:4]**

Security support. Defined values are:

<table>
<thead>
<tr>
<th>Security</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL3, Monitor mode, and the SMC instruction not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL3, Monitor mode, the SMC instruction, and all the features</td>
</tr>
<tr>
<td></td>
<td>described by Sec_frac == 0b0001 implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the ability to set the NSACR.RFR bit.</td>
</tr>
<tr>
<td></td>
<td>Not permitted in Armv8 as the NSACR.RFR bit is RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL3 is not implemented.
- 0b0001 when EL3 is implemented.

In an implementation that includes EL3, if EL3 cannot use AArch32 but EL1 can use AArch32 then this field has the value 0b0001.

If EL1 cannot use AArch32 then this field has the value 0b0000.
ProgMod, bits [3:0]

Support for the standard programmers' model for Armv4 and later. Model must support User, FIQ, IRQ, Supervisor, Abort, Undefined, and System modes. Defined values are:

<table>
<thead>
<tr>
<th>ProgMod</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0001 and 0b0000.

If EL1 cannot use AArch32 then this field has the value 0b0000.

Otherwise:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
</tr>
</thead>
<tbody>
<tr>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
</tr>
<tr>
<td>55</td>
<td>54</td>
<td>53</td>
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<td>9</td>
<td>8</td>
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<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits [63:0]

Reserved, UNKNOWN.

Accessing the ID_PFR1_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ID_PFR1_EL1

```
if PSTATE_EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
    elsif PSTATE_EL == EL1 then
        if EL2Enabled() && HCR_EL2.TID3 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            return ID_PFR1_EL1;
    elsif PSTATE_EL == EL2 then
        return ID_PFR1_EL1;
    elsif PSTATE_EL == EL3 then
        return ID_PFR1_EL1;
```
The ID_PFR2_EL1 characteristics are:

**Purpose**

Gives information about the AArch32 programmers' model.

Must be interpreted with ID_PFR0_EL1 and ID_PFR1_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register ID_PFR2_EL1 bits [31:0] are architecturally mapped to AArch32 System register ID_PFR2[31:0].

**Attributes**

ID_PFR2_EL1 is a 64-bit register.

**Field descriptions**

The ID_PFR2_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>RAS_frac</td>
</tr>
<tr>
<td>61</td>
<td>SSBS</td>
</tr>
<tr>
<td>60</td>
<td>CSV3</td>
</tr>
</tbody>
</table>

**Bits [63:12]**

Reserved, RES0.

**RAS_frac, bits [11:8]**

RAS Extension fractional field. Defined values are:

<table>
<thead>
<tr>
<th>RAS_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If ID_PFR0_EL1.RAS == 0b0001, RAS Extension implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If ID_PFR0_EL1.RAS == 0b0001, as 0b0000 and adds support for additional ERXMISC&lt;m&gt; System registers. Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ERR&lt;n&gt;STATUS and support for the optional RAS Timestamp Extension.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is valid only if ID_PFR0_EL1.RAS == 0b0001.
**SSBS, bits [7:4]**

Speculative Store Bypassing controls in AArch64 state. Defined values are:

<table>
<thead>
<tr>
<th>SSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>AArch32 provides no mechanism to control the use of Speculative Store Bypassing.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AArch32 provides the PSTATE.SSBS mechanism to mark regions that are Speculative Store Bypass Safe.</td>
</tr>
</tbody>
</table>

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

All other values are reserved.

**CSV3, bits [3:0]**

Speculative use of faulting data. Defined values are:

<table>
<thead>
<tr>
<th>CSV3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>This Device does not disclose whether data loaded under speculation with a permission or domain fault can be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence</td>
</tr>
<tr>
<td>0b0001</td>
<td>Data loaded under speculation with a permission or domain fault cannot be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CSV3 implements the functionality identified by the value 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

If FEAT_E0PD is implemented, FEAT_CSV3 must be implemented.

**Otherwise:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>0000</td>
</tr>
<tr>
<td>62</td>
<td>0000</td>
</tr>
<tr>
<td>61</td>
<td>0000</td>
</tr>
<tr>
<td>60</td>
<td>0000</td>
</tr>
<tr>
<td>59</td>
<td>0000</td>
</tr>
<tr>
<td>58</td>
<td>0000</td>
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<tr>
<td>57</td>
<td>0000</td>
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<tr>
<td>56</td>
<td>0000</td>
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<td>55</td>
<td>0000</td>
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<tr>
<td>54</td>
<td>0000</td>
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<tr>
<td>53</td>
<td>0000</td>
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<tr>
<td>52</td>
<td>0000</td>
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<tr>
<td>51</td>
<td>0000</td>
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<tr>
<td>50</td>
<td>0000</td>
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<tr>
<td>49</td>
<td>0000</td>
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<tr>
<td>48</td>
<td>0000</td>
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<tr>
<td>47</td>
<td>0000</td>
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<tr>
<td>46</td>
<td>0000</td>
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<tr>
<td>45</td>
<td>0000</td>
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<tr>
<td>44</td>
<td>0000</td>
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<tr>
<td>43</td>
<td>0000</td>
</tr>
<tr>
<td>42</td>
<td>0000</td>
</tr>
<tr>
<td>41</td>
<td>0000</td>
</tr>
<tr>
<td>40</td>
<td>0000</td>
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<tr>
<td>39</td>
<td>0000</td>
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<tr>
<td>38</td>
<td>0000</td>
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<tr>
<td>37</td>
<td>0000</td>
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<tr>
<td>36</td>
<td>0000</td>
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<td>35</td>
<td>0000</td>
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<td>34</td>
<td>0000</td>
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<tr>
<td>33</td>
<td>0000</td>
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<tr>
<td>32</td>
<td>0000</td>
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<tr>
<td>31</td>
<td>0000</td>
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<tr>
<td>30</td>
<td>0000</td>
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<tr>
<td>29</td>
<td>0000</td>
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<tr>
<td>28</td>
<td>0000</td>
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<tr>
<td>27</td>
<td>0000</td>
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<tr>
<td>26</td>
<td>0000</td>
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<tr>
<td>25</td>
<td>0000</td>
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<tr>
<td>24</td>
<td>0000</td>
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<tr>
<td>23</td>
<td>0000</td>
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<tr>
<td>22</td>
<td>0000</td>
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<tr>
<td>21</td>
<td>0000</td>
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<tr>
<td>20</td>
<td>0000</td>
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<tr>
<td>19</td>
<td>0000</td>
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<tr>
<td>18</td>
<td>0000</td>
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<tr>
<td>17</td>
<td>0000</td>
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<tr>
<td>16</td>
<td>0000</td>
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<tr>
<td>15</td>
<td>0000</td>
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<tr>
<td>14</td>
<td>0000</td>
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<tr>
<td>13</td>
<td>0000</td>
</tr>
<tr>
<td>12</td>
<td>0000</td>
</tr>
<tr>
<td>11</td>
<td>0000</td>
</tr>
<tr>
<td>10</td>
<td>0000</td>
</tr>
<tr>
<td>9</td>
<td>0000</td>
</tr>
<tr>
<td>8</td>
<td>0000</td>
</tr>
<tr>
<td>7</td>
<td>0000</td>
</tr>
<tr>
<td>6</td>
<td>0000</td>
</tr>
<tr>
<td>5</td>
<td>0000</td>
</tr>
<tr>
<td>4</td>
<td>0000</td>
</tr>
<tr>
<td>3</td>
<td>0000</td>
</tr>
<tr>
<td>2</td>
<td>0000</td>
</tr>
<tr>
<td>1</td>
<td>0000</td>
</tr>
<tr>
<td>0</td>
<td>0000</td>
</tr>
</tbody>
</table>

Reserved, UNKNOWN.

**Accessing the ID_PFR2_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, ID_PFR2_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return ID_PFR2_EL1;
elsif PSTATE.EL == EL2 then
    return ID_PFR2_EL1;
elsif PSTATE.EL == EL3 then
    return ID_PFR2_EL1;
**IFSR32_EL2, Instruction Fault Status Register (EL2)**

The IFSR32_EL2 characteristics are:

**Purpose**

Allows access to the AArch32 IFSR register from AArch64 state only. Its value has no effect on execution in AArch64 state.

**Configuration**

AArch64 System register IFSR32_EL2 bits [31:0] are architecturally mapped to AArch32 System register IFSR[31:0].

This register is present only when EL1 is capable of using AArch32. Otherwise, direct accesses to IFSR32_EL2 are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, and EL1 is capable of using AArch32, then this register is not RES0.

**Attributes**

IFSR32_EL2 is a 64-bit register.

**Field descriptions**

The IFSR32_EL2 bit assignments are:

**When TTBCR.EAE == 0:**

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | FS[3:0] |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:17]**

Reserved, RES0.

**FnV, bit [16]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>IFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is RES0 for all other Prefetch Abort exceptions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:13]**

Reserved, RES0.
External abort type. This bit can be used to provide an **IMPLEMENTATION DEFINED** classification of External aborts. In an implementation that does not provide any classification of External aborts, this bit is **RES0**. For aborts other than External aborts this bit always returns 0. On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Bit [11]

Reserved, **RES0**.


<table>
<thead>
<tr>
<th>FS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00001</td>
<td>PC alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b00010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b00011</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00110</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b00111</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b01001</td>
<td>Domain fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01011</td>
<td>Domain fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01100</td>
<td>Synchronous External abort, on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01110</td>
<td>Synchronous External abort, on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01111</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b10000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b10100</td>
<td><strong>IMPLEMENTATION DEFINED</strong> fault (Lockdown fault).</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11001</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11100</td>
<td>Synchronous parity or ECC error on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11110</td>
<td>Synchronous parity or ECC error on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Short-descriptor translation table lookup'.

The FS field is split as follows:

- FS[4] is IFSR32_EL2[10].
- FS[3:0] is IFSR32_EL2[3:0].

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>
Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [8:4]**

Reserved, **RES0**.

**When TTBCR.EAE == 1:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| **RES0** | **FnV** | **RES0** | **ExT** | **RES0** | **LPAE** | **RES0** | **STATUS** |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:17]**

Reserved, **RES0**.

**FnV, bit [16]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>IFAR</strong> is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>IFAR</strong> is not valid, and holds a <strong>UNKNOWN</strong> value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is **RES0** for all other Prefetch Abort exceptions.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [15:13]**

Reserved, **RES0**.

**ExT, bit [12]**

External abort type. This bit can be used to provide an **IMPLEMENTATION DEFINED** classification of External aborts.

In an implementation that does not provide any classification of External aborts, this bit is **RES0**.

For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [11:10]**

Reserved, **RES0**.

**LPAE, bit [9]**

On taking a Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>

Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [8:6]**

Reserved, RES0.

**STATUS, bits [5:0]**

Fault status bits. Possible values of this field are:

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault in translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011010</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b100001</td>
<td>PC alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

When FEAT_RAS is implemented, 0b011000, 0b011101, 0b011110, and 0b011111 are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Long-descriptor translation table lookup'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the IFSR32_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, IFSR32_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elseif PSTATE.EL == EL2 then
    return IFSR32_EL2;
elsif PSTATE.EL == EL3 then
    return IFSR32_EL2;

MSR IFSR32_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elseif PSTATE.EL == EL2 then
    IFSR32_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    IFSR32_EL2 = X[t];
The ISR_EL1 characteristics are:

### Purpose

Shows the pending status of the IRQ, FIQ, or SError interrupt.

When executing at EL2, EL3 or Secure EL1 when SCR_EL3.EEL2 == 0b0, this shows the pending status of the physical IRQ, FIQ, or SError interrupts.

When executing at either Non-secure EL1 or at Secure EL1 when SCR_EL3.EEL2 == 0b1:

- If the HCR_EL2.{IMO,FMO,AMO} bit has a value of 1, the corresponding ISR_EL1.{I,F,A} bit shows the pending status of the virtual IRQ, FIQ, or SError.
- If the HCR_EL2.{IMO,FMO,AMO} bit has a value of 0, the corresponding ISR_EL1.{I,F,A} bit shows the pending status of the physical IRQ, FIQ, or SError.

### Configuration

AArch64 System register ISR_EL1 bits [31:0] are architecturally mapped to AArch32 System register ISR[31:0].

### Attributes

ISR_EL1 is a 64-bit register.

### Field descriptions

The ISR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-9</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>SError interrupt pending bit</td>
</tr>
<tr>
<td>7</td>
<td>IRQ pending bit</td>
</tr>
</tbody>
</table>

#### Bits [63:9]

- Reserved, RES0.

#### A, bit [8]

- SError interrupt pending bit.

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending SError</td>
</tr>
<tr>
<td>0b1</td>
<td>An SError interrupt is pending</td>
</tr>
</tbody>
</table>

If the SError interrupt is edge-triggered, this field is cleared to zero when the physical SError interrupt is taken.

#### I, bit [7]

- IRQ pending bit. Indicates whether an IRQ interrupt is pending.

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending IRQ</td>
</tr>
<tr>
<td>0b1</td>
<td>An IRQ interrupt is pending</td>
</tr>
</tbody>
</table>
F, bit [6]

FIQ pending bit. Indicates whether an FIQ interrupt is pending.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending FIQ.</td>
</tr>
<tr>
<td>0b1</td>
<td>An FIQ interrupt is pending.</td>
</tr>
</tbody>
</table>

Bits [5:0]

Reserved, RES0.

Accessing the ISR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, ISR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGTR_EL2.ISR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return ISR_EL1;
elsif PSTATE.EL == EL2 then
  return ISR_EL1;
elsif PSTATE.EL == EL3 then
  return ISR_EL1;
LORC_EL1, LORegion Control (EL1)

The LORC_EL1 characteristics are:

**Purpose**

Enables and disables LORegions, and selects the current LORegion descriptor.

**Configuration**

This register is present only when FEAT_LOR is implemented. Otherwise, direct accesses to LORC_EL1 are UNDEFINED.

If no LORegion descriptors are supported by the PE, then this register is RES0.

**Attributes**

LORC_EL1 is a 64-bit register.

**Field descriptions**

The LORC_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
</tr>
<tr>
<td>62</td>
</tr>
<tr>
<td>61</td>
</tr>
<tr>
<td>60</td>
</tr>
<tr>
<td>59</td>
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<td>58</td>
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<tr>
<td>57</td>
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<td>53</td>
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<td>51</td>
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<tr>
<td>50</td>
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<tr>
<td>49</td>
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<tr>
<td>48</td>
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<tr>
<td>47</td>
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<tr>
<td>46</td>
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<tr>
<td>45</td>
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<tr>
<td>44</td>
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<tr>
<td>43</td>
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<tr>
<td>42</td>
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<tr>
<td>41</td>
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<tr>
<td>40</td>
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<tr>
<td>39</td>
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<tr>
<td>38</td>
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<tr>
<td>37</td>
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<tr>
<td>36</td>
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<tr>
<td>35</td>
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<tr>
<td>34</td>
</tr>
<tr>
<td>33</td>
</tr>
<tr>
<td>32</td>
</tr>
<tr>
<td>31</td>
</tr>
<tr>
<td>30</td>
</tr>
<tr>
<td>29</td>
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<tr>
<td>28</td>
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<tr>
<td>27</td>
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<tr>
<td>26</td>
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<tr>
<td>25</td>
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<tr>
<td>24</td>
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<tr>
<td>23</td>
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<tr>
<td>22</td>
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<tr>
<td>21</td>
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<tr>
<td>20</td>
</tr>
<tr>
<td>19</td>
</tr>
<tr>
<td>18</td>
</tr>
<tr>
<td>17</td>
</tr>
<tr>
<td>16</td>
</tr>
<tr>
<td>15</td>
</tr>
<tr>
<td>14</td>
</tr>
<tr>
<td>13</td>
</tr>
<tr>
<td>12</td>
</tr>
<tr>
<td>11</td>
</tr>
<tr>
<td>10</td>
</tr>
<tr>
<td>9</td>
</tr>
<tr>
<td>8</td>
</tr>
<tr>
<td>7</td>
</tr>
<tr>
<td>6</td>
</tr>
<tr>
<td>5</td>
</tr>
<tr>
<td>4</td>
</tr>
<tr>
<td>3</td>
</tr>
<tr>
<td>2</td>
</tr>
<tr>
<td>1</td>
</tr>
<tr>
<td>0</td>
</tr>
</tbody>
</table>

Reserved, RES0.

**DS, bits [9:2]**

Descriptor Select. Selects the current LORegion descriptor accessed by LORSA_EL1, LOREA_EL1, and LORN_EL1.

The number of LORegion descriptors in IMPLEMENTATION DEFINED. The maximum number of LORegion descriptors supported is 256. If the number is less than 256, then bits[63:M+2] are RES0, where M is Log2(Number of LORegion descriptors supported by the implementation).

If this field points to an LORegion descriptor that is not supported by an implementation, then the registers LORN_EL1, LOREA_EL1, and LORSA_EL1 are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [1]**

Reserved, RES0.

**EN, bit [0]**

Enable. Indicates whether LORegions are enabled.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled. Memory accesses do not match any LORegions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enabled. Memory accesses may match a LORegion.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.
On a Warm reset, this field resets to 0.

### Accessing the LORC_EL1

Accesses to this register use the following encodings:

MRS <Xt>, LORC_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif SCR_EL3.NS == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.LORC_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return LORC_EL1;
  end if
elsif PSTATE.EL == EL2 then
  if SCR_EL3.NS == '0' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return LORC_EL1;
  end if
elsif PSTATE.EL == EL3 then
  if SCR_EL3.NS == '0' then
    return LORC_EL1;
  else
    return LORC_EL1;
  end if

MSR LORC_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif SCR_EL3.NS == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.LORC_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      LORC_EL1 = X[t];
  elsif SCR_EL3.NS == '0' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      LORC_EL1 = X[t];
  endif
else
  LORC_EL1 = X[t];
endif
LOREA_EL1, LORegion End Address (EL1)

The LOREA_EL1 characteristics are:

**Purpose**

Holds the physical address of the end of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.

**Configuration**

This register is present only when FEAT_LOR is implemented. Otherwise, direct accesses to LOREA_EL1 are UNDEFINED.

This register is RES0 if any of the following apply:

- No LORegion descriptors are supported by the PE.
- LORC_EL1.DS points to a LORegion that is not supported by the PE.

**Attributes**

LOREA_EL1 is a 64-bit register.

**Field descriptions**

The LOREA_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     | EA[51:48]|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| EA[47:16]|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

Any of the fields in this register are permitted to be cached in a TLB.

**Bits [63:52]**

Reserved, RES0.

**EA[51:48], bits [51:48]**

When FEAT_LPA is implemented:


On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**EA[47:16], bits [47:16]**

Bits [47:16] of the end physical address of an LORegion described in the current LORegion descriptor selected by LORC_EL1.DS. Bits[15:0] of this address are defined to be 0xFFFF. For implementations with fewer than 48 bits, the upper bits of this field are RES0.
When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, EA[51:48] form the upper part of the address value. Otherwise, for implementations with fewer than 52 physical address bits, EA[51:48] are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:0]**

Reserved, RES0.

### Accessing the LOREA_EL1

Accesses to this register use the following encodings:

**MRS \(<Xt>, \text{LOREA_EL1}\)**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```diff
if PSTATE.EL == EL0 then
    UNDEFINED;
elsf PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
elsf SCR_EL3.NS == '0' then
            UNDEFINED;
elsf EL2Enabled() && HCR_EL2.TLOR == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
elsf EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HGFTR_EL2.LOREA_EL1 == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
elsf HaveEL(EL3) && SCR_EL3.TLOR == '1' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
elsf SCR_EL3.NS == '0' then
                elsif Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
elsf SCR_EL3.NS == '0' then
                elsif Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
elsf SCR_EL3.NS == '0' then
                elsif Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
elsf SCR_EL3.NS == '0' then
                elsif Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
elsf SCR_EL3.NS == '0' then
                return LOREA_EL1;
elsf PSTATE.EL == EL2 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
elsf Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
elsf HaveEL(EL3) && SCR_EL3.TLOR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elsf SCR_EL3.NS == '0' then
        elsif SCR_EL3.NS == '0' then
    else
        return LOREA_EL1;
elsf PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
elsf SCR_EL3.NS == '0' then
    else
        return LOREA_EL1;

**MSR LOREA_EL1, \(<Xt>\)**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
      UNDEFINED;
   elsif SCR_EL3.NS == '0' then
      UNDEFINED;
   elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.LOREA_EL1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      AArch64.SystemAccessTrap(EL3, 0x18);
   else
      LOREA_EL1 = X[t];
   elsif PSTATE.EL == EL2 then
      if SCR_EL3.NS == '0' then
         UNDEFINED;
      elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
         UNDEFINED;
      elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
         if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
         else
            AArch64.SystemAccessTrap(EL3, 0x18);
         else
            LOREA_EL1 = X[t];
      elsif PSTATE.EL == EL3 then
         if SCR_EL3.NS == '0' then
            UNDEFINED;
         else
            LOREA_EL1 = X[t];
      else
         LOREA_EL1 = X[t];
The LORID_EL1 characteristics are:

**Purpose**

Indicates the number of LORegions and LORegion descriptors supported by the PE.

**Configuration**

This register is present only when FEAT_LOR is implemented. Otherwise, direct accesses to LORID_EL1 are UNDEFINED.

If no LORegion descriptors are implemented, then the registers LORC_EL1, LORN_EL1, LOREA_EL1, and LORSA_EL1 are RES0.

**Attributes**

LORID_EL1 is a 64-bit register.

**Field descriptions**

The LORID_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>LD</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>LR</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**LD, bits [23:16]**

Number of LORegion descriptors supported by the PE. This is an 8-bit binary number.

**Bits [15:8]**

Reserved, RES0.

**LR, bits [7:0]**

Number of LORegions supported by the PE. This is an 8-bit binary number.

---

**Note**

If LORID_EL1 indicates that no LORegions are implemented, then LoadLOAcquire and StoreLORelease will behave as LoadAcquire and StoreRelease.

---

**Accessing the LORID_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, LORID_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.LORID_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return LORID_EL1;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return LORID_EL1;
  end
elsif PSTATE.EL == EL3 then
  return LORID_EL1;
LORN_EL1, LORegion Number (EL1)

The LORN_EL1 characteristics are:

**Purpose**

Holds the number of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.

**Configuration**

This register is present only when FEAT_LOR is implemented. Otherwise, direct accesses to LORN_EL1 are UNDEFINED.

This register is RES0 if any of the following apply:

- No LORegion descriptors are supported by the PE.
- LORC_EL1.DS points to a LORegion that is not supported by the PE.

**Attributes**

LORN_EL1 is a 64-bit register.

**Field descriptions**

The LORN_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>57</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>45</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>43</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31</td>
<td>Number of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

Any of the fields in this register are permitted to be cached in a TLB.

**Bits [63:8]**

Reserved, RES0.

**Num, bits [7:0]**

Number of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.

The maximum number of LORegions supported by the PE is 256. If the maximum number is less than 256, then bits[8:N] are RES0, where N is (Log₂(Number of LORegions supported by the PE)).

If this field points to a LORegion that is not supported by the PE, then the current LORegion descriptor does not match any LORegion.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the LORN_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, LORN_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

Page 1084
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
elseif SCR_EL3.NS == '0' then
        UNDEFINED;
elseif EL2Enabled() && HCR_EL2.TLOR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.LORN_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elseif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return LORN_EL1;
elseif PSTATE.EL == EL2 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
elseif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return LORN_EL1;
elseif PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
else
    return LORN_EL1;
else
    return LORN_EL1;

MSR LORN_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
    elsif SCR_EL3.NS == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.LORN_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif PSTATE.EL == EL2 then
        if SCR_EL3.NS == '0' then
            UNDEFINED;
        else
            LORN_EL1 = X[t];
        end if
    elsif PSTATE.EL == EL3 then
        if SCR_EL3.NS == '0' then
            UNDEFINED;
        else
            LORN_EL1 = X[t];
        end if
elsif PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
    else
        LORN_EL1 = X[t];
    end if
else
    LORN_EL1 = X[t];
end if
The LORSA_EL1 characteristics are:

### Purpose

Indicates whether the current LORegion descriptor selected by LORC_EL1.DS is enabled, and holds the physical address of the start of the LORegion.

### Configuration

This register is present only when FEAT_LOR is implemented. Otherwise, direct accesses to LORSA_EL1 are UNDEFINED.

This register is RES0 if any of the following apply:

- No LORegion descriptors are supported by the PE.
- LORC_EL1.DS points to a LORegion that is not supported by the PE.

### Attributes

LORSA_EL1 is a 64-bit register.

### Field descriptions

The LORSA_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SA | RES0 | Valid |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Any of the fields in this register are permitted to be cached in a TLB.

**Bits [63:52]**

Reserved, RES0.

**SA, bits [51:16]**

**SA encoding when FEAT_LPA is implemented**

| 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 10 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| SA |

**SA, bits [35:0]**

The start physical address of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.

Bits[15:0] of this address are defined to be 0x0000.

When 52-bit addresses and a 64KB translation granule are in use, LORSA_EL1.SA[35:32] forms the upper part of the address value.

For implementations with fewer than 52 physical address bits, LORSA_EL1.SA[35:32] is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
SA encoding when FEAT_LPA is not implemented

| 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |  
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SA |

**Bits [35:32]**

Reserved, RES0.

**SA, bits [31:0]**

The start physical address of the LORegion described in the current LORegion descriptor selected by LORC_EL1.DS.

Bits [15:0] of this address are defined to be 0x0000.

For implementations with fewer than 48 bits, the upper bits of this field are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:1]**

Reserved, RES0.

**Valid, bit [0]**

Indicates whether the current LORegion Descriptor is enabled.

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled</td>
</tr>
<tr>
<td>0b1</td>
<td>Enabled</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the LORSA_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, LORSA_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && SCR_EL3.TLOR == '1' then
    UNDEFINED;
  elsif SCR_EL3.NS == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.LORSA_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      return LORSA_EL1;
  elsif PSTATE.EL == EL2 then
    if SCR_EL3.NS == '0' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && SCR_EL3.TLOR == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        return LORSA_EL1;
    elsif PSTATE.EL == EL3 then
      if SCR_EL3.NS == '0' then
        return LORSA_EL1;
    else
      return LORSA_EL1;
    endif
  endif
endif

MSR LORSA_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
    elsif SCR_EL3.NS == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.TLOR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.LORSA_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
        LORSA_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.TLOR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.TLOR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            LORSA_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        UNDEFINED;
    else
        LORSA_EL1 = X[t];
The MAIR_EL1 characteristics are:

**Purpose**

Provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations at EL1.

**Configuration**

AArch64 System register MAIR_EL1 bits [31:0] are architecturally mapped to AArch32 System register PRRR[31:0] when TTBCR.EAE == 0.

AArch64 System register MAIR_EL1 bits [31:0] are architecturally mapped to AArch32 System register MAIR0[31:0] when TTBCR.EAE == 1.

AArch64 System register MAIR_EL1 bits [63:32] are architecturally mapped to AArch32 System register NMRR[31:0] when TTBCR.EAE == 0.

AArch64 System register MAIR_EL1 bits [63:32] are architecturally mapped to AArch32 System register MAIR1[31:0] when TTBCR.EAE == 1.

**Attributes**

MAIR_EL1 is a 64-bit register.

**Field descriptions**

The MAIR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Attr7 |     | Attr6 |     | Attr5 |     | Attr4 |     | Attr3 |     | Attr2 |     | Attr1 |     | Attr0 |     |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

MAIR_EL1 is permitted to be cached in a TLB.

**Attr<n>, bits [8n+7:8n], for n = 7 to 0**


Attr is encoded as follows:
### Attr | Meaning
--- | ---
0b0000dd00 | Device memory. See encoding of 'dd' for the type of Device memory.
0b0000dd01 | If FEAT_XS is implemented: Device memory with the XS attribute set to 0. See encoding of 'dd' for the type of Device memory. Otherwise, UNPREDICTABLE.
0b0000dd1x | UNPREDICTABLE.
0b00000000, (oooo != 0000 and iiii != 0000) | Normal memory. See encoding of 'oooo' and 'iiii' for the type of Normal Memory.
0b01000000 | If FEAT_XS is implemented: Normal Inner Non-cacheable, Outer Non-cacheable memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.
0b10100000 | If FEAT_XS is implemented: Normal Inner Write-through Cacheable, Outer Write-through Cacheable, Read-Allocate, No-Write Allocate, Non-transient memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.
0b11110000 | If FEAT_MTE is implemented: Tagged Normal Inner Write-Back, Outer Write-Back, Read-Allocate, Write-Allocate Non-transient memory. Otherwise, UNPREDICTABLE.
0bxxxx0000, (xxxx != 0000, xxxx != 0100, xxxx != 1010, xxxx != 1111) | UNPREDICTABLE.

'dd' is encoded as follows:

| dd | Meaning |
--- | ---|
0b00 | Device-nGnRnE memory |
0b01 | Device-nGnRE memory |
0b10 | Device-nGRE memory |
0b11 | Device-GRE memory |

'oooo' is encoded as follows:

| 'oooo' | Meaning |
--- | ---|
0b0000 | See encoding of Attr |
0b00RW, RW | Normal memory, Outer Write-Through Transient |
not0b0 | |
0b0100 | Normal memory, Outer Non-cacheable |
0b01RW, RW | Normal memory, Outer Write-Back Transient |
not0b0 | |
0b10RW | Normal memory, Outer Write-Through Non-transient |
0b11RW | Normal memory, Outer Write-Back Non-transient |

R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

'iiii' is encoded as follows:

| 'iiii' | Meaning |
--- | ---|
0b0000 | See encoding of Attr |
0b00RW, RW | Normal memory, Inner Write-Through Transient |
not0b0 | |
0b0100 | Normal memory, Inner Non-cacheable |
0b01RW, RW | Normal memory, Inner Write-Back Transient |
not0b0 | |
0b10RW | Normal memory, Inner Write-Through Non-transient |
0b11RW | Normal memory, Inner Write-Back Non-transient |

R = Inner Read-Allocate policy, W = Inner Write-Allocate policy.

The R and W bits in 'oooo' and 'iiii' fields have the following meanings:
<table>
<thead>
<tr>
<th>R or W</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Allocate</td>
</tr>
<tr>
<td>0b1</td>
<td>Allocate</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally \textit{UNKNOWN} value.

**Accessing the MAIR\_EL1**

When \texttt{HCR\_EL2.E2H} is 1, without explicit synchronization, access from EL3 using the mnemonic MAIR\_EL1 or MAIR\_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

\[
\text{MRS} <Xt>, \text{MAIR\_EL1}
\]

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b1010 & 0b0010 & 0b000 \\
\hline
\end{array}
\]

\[
\text{if PSTATE.EL == EL0 then} \\
\quad \text{UNDEFINED;}
\]

\[
\text{elsif PSTATE.EL == EL1 then} \\
\quad \text{if EL2Enabled()} \&\& \text{HCR\_EL2.TVM} == '1' then \\
\quad \quad \text{AArch64.SystemAccessTrap(EL2, 0x18);} \\
\quad \text{elsif EL2Enabled()} \&\& (!HaveEL(EL3) || SCR\_EL3.FGTEn == '1') \&\& \text{HFGWTR\_EL2.MAIR\_EL1} == '1' then \\
\quad \quad \text{AArch64.SystemAccessTrap(EL2, 0x18);} \\
\quad \text{elsif EL2Enabled()} \&\& \text{HCR\_EL2.<NV2,NV1,NV>} == '111' then \\
\quad \quad \text{return NVMem[0x140];} \\
\quad \text{else} \\
\quad \quad \text{return MAIR\_EL1;} \\
\text{elsif PSTATE.EL == EL2 then} \\
\quad \text{if HCR\_EL2.E2H} == '1' then \\
\quad \quad \text{return MAIR\_EL2;} \\
\quad \text{else} \\
\quad \quad \text{return MAIR\_EL1;} \\
\text{elsif PSTATE.EL == EL3 then} \\
\quad \text{return MAIR\_EL1;} \\
\]

\[
\text{MSR MAIR\_EL1, <Xt>}
\]

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b1010 & 0b0010 & 0b000 \\
\hline
\end{array}
\]

\[
\text{if PSTATE.EL == EL0 then} \\
\quad \text{UNDEFINED;} \\
\text{elsif PSTATE.EL == EL1 then} \\
\quad \text{if EL2Enabled()} \&\& \text{HCR\_EL2.TVM} == '1' then \\
\quad \quad \text{AArch64.SystemAccessTrap(EL2, 0x18);} \\
\quad \text{elsif EL2Enabled()} \&\& (!HaveEL(EL3) || SCR\_EL3.FGTEn == '1') \&\& \text{HFGWTR\_EL2.MAIR\_EL1} == '1' then \\
\quad \quad \text{AArch64.SystemAccessTrap(EL2, 0x18);} \\
\quad \text{elsif EL2Enabled()} \&\& \text{HCR\_EL2.<NV2,NV1,NV>} == '111' then \\
\quad \quad \text{NVMem[0x140]} = X[t]; \\
\quad \text{else} \\
\quad \quad \text{MAIR\_EL1} = X[t]; \\
\quad \text{elsif PSTATE.EL == EL2 then} \\
\quad \quad \text{if HCR\_EL2.E2H} == '1' then \\
\quad \quad \quad \text{MAIR\_EL2} = X[t]; \\
\quad \quad \text{elsif PSTATE.EL == EL3 then} \\
\quad \quad \quad \text{MAIR\_EL1} = X[t]; \\
\text{elsif PSTATE.EL == EL3 then} \\
\quad \quad \text{MAIR\_EL1} = X[t];
\]
MRS <Xt>, MAIR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x140];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return MAIR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return MAIR_EL1;
  else
    UNDEFINED;

MSR MAIR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x140] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    MAIR_EL1 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    MAIR_EL1 = X[t];
  else
    UNDEFINED;

The MAIR_EL2 characteristics are:

**Purpose**

Provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations at EL2.

**Configuration**

AArch64 System register MAIR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HMAIR0[31:0].

AArch64 System register MAIR_EL2 bits [63:32] are architecturally mapped to AArch32 System register HMAIR1[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MAIR_EL2 is a 64-bit register.

**Field descriptions**

The MAIR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Attr7 | Attr6 | Attr5 | Attr4 |
| Attr3 | Attr2 | Attr1 | Attr0 |

MAIR_EL2 is permitted to be cached in a TLB.

Attr<\(n\)>, bits [8\(n+7:8\)n], for \(n = 7\) to \(0\)

The memory attribute encoding for an AttrIndx[2:0] entry in a Long descriptor format translation table entry, where AttrIndx[2:0] gives the value of \(<n>\) in Attr<\(n\)>.

Attr is encoded as follows:
### Attr and Meaning

<table>
<thead>
<tr>
<th>Attr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000dd00</td>
<td>Device memory. See encoding of 'dd' for the type of Device memory.</td>
</tr>
<tr>
<td>0b0000dd01</td>
<td>If FEAT_XS is implemented: Device memory with the XS attribute set to 0. See encoding of 'dd' for the type of Device memory. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b0000dd1x</td>
<td>UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b0000iiii, (oooo != 0000 and iii != 0000)</td>
<td>Normal memory. See encoding of 'oooo' and 'iiii' for the type of Normal Memory.</td>
</tr>
<tr>
<td>0b01000000</td>
<td>If FEAT_XS is implemented: Normal Inner Non-cacheable, Outer Non-cacheable memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b10100000</td>
<td>If FEAT_XS is implemented: Normal Inner Write-through Cacheable, Outer Write-through Cacheable, Read-Allocate, No-Write Allocate, Non-transient memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b11110000</td>
<td>If FEAT_MTE is implemented: Tagged Normal Inner Write-Back, Outer Write-Back, Read-Allocate, Write-Allocate Non-transient memory. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0bxxxx0000, (xxxx != 0000, xxxx != 0100, xxxx != 1010, xxxx != 1111)</td>
<td>UNPREDICTABLE.</td>
</tr>
</tbody>
</table>

'dd' is encoded as follows:

<table>
<thead>
<tr>
<th>dd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Device-nGnRnE memory</td>
</tr>
<tr>
<td>0b01</td>
<td>Device-nGnRE memory</td>
</tr>
<tr>
<td>0b10</td>
<td>Device-ngRE memory</td>
</tr>
<tr>
<td>0b11</td>
<td>Device-GRE memory</td>
</tr>
</tbody>
</table>

'oooo' is encoded as follows:

<table>
<thead>
<tr>
<th>'oooo'</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>See encoding of Attr</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Outer Write-Through Transient</td>
</tr>
<tr>
<td>not0b0</td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Outer Non-cacheable</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Outer Write-Back Transient</td>
</tr>
<tr>
<td>not0b0</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Outer Write-Through Non-transient</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Outer Write-Back Non-transient</td>
</tr>
</tbody>
</table>

R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

'iiii' is encoded as follows:

<table>
<thead>
<tr>
<th>'iiii'</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>See encoding of Attr</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Inner Write-Through Transient</td>
</tr>
<tr>
<td>not0b0</td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Inner Non-cacheable</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Inner Write-Back Transient</td>
</tr>
<tr>
<td>not0b0</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Inner Write-Through Non-transient</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Inner Write-Back Non-transient</td>
</tr>
</tbody>
</table>

R = Inner Read-Allocate policy, W = Inner Write-Allocate policy.

The R and W bits in 'oooo' and 'iiii' fields have the following meanings:
### Accessing the MAIR_EL2

When \texttt{HCR\_EL2.E2H} is 1, without explicit synchronization, access from EL2 using the mnemonic \texttt{MAIR\_EL2} or \texttt{MAIR\_EL1} is not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, MAIR\_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b00</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR\_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return MAIR\_EL2;
elsif PSTATE.EL == EL3 then
    return MAIR\_EL2;
```

**MSR MAIR\_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b00</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR\_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    MAIR\_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    MAIR\_EL2 = X[t];
```

**MRS <Xt>, MAIR\_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.MAIR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x140];
    else
        return MAIR_EL1;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return MAIR_EL2;
    else
        return MAIR_EL1;
elsif PSTATE.EL == EL3 then
    return MAIR_EL1;

MSR MAIR_EL1, <Xt> 

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.MAIR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x140] = X[t];
    else
        MAIR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        MAIR_EL2 = X[t];
    else
        MAIR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    MAIR_EL1 = X[t];
MAIR_EL3, Memory Attribute Indirection Register (EL3)

The MAIR_EL3 characteristics are:

**Purpose**

Provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations at EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to MAIR_EL3 are UNDEFINED.

**Attributes**

MAIR_EL3 is a 64-bit register.

**Field descriptions**

The MAIR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Attr7 | Attr6 | Attr5 | Attr4 |
| Attr3 | Attr2 | Attr1 | Attr0 |

MAIR_EL3 is permitted to be cached in a TLB.

**Attr<n>, bits [8n+7:8n], for n = 7 to 0**


Attr is encoded as follows:
MAIR_EL3, Memory Attribute Indirection Register (EL3)

<table>
<thead>
<tr>
<th>Attr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000dd00</td>
<td>Device memory. See encoding of 'dd' for the type of Device memory.</td>
</tr>
<tr>
<td>0b0000dd01</td>
<td>If FEAT_XS is implemented: Device memory with the XS attribute set to 0. See encoding of 'dd' for the type of Device memory. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b0000dd1x</td>
<td>UNPREDICTABLE.</td>
</tr>
<tr>
<td>0booooiiii, (oooo != 0000 and iii i != 0000)</td>
<td>Normal memory. See encoding of 'oooo' and 'iiii' for the type of Normal Memory.</td>
</tr>
<tr>
<td>0b01000000</td>
<td>If FEAT_XS is implemented: Normal Inner Non-cacheable, Outer Non-cacheable memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b10100000</td>
<td>If FEAT_XS is implemented: Normal Inner Write-through Cacheable, Outer Write-through Cacheable, Read-Allocate, No-Write Allocate, Non-transient memory with the XS attribute set to 0. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b11110000</td>
<td>If FEAT_MTE is implemented: Tagged Normal Inner Write-Back, Outer Write-Back, Read-Allocate, Write-Allocate Non-transient memory. Otherwise, UNPREDICTABLE.</td>
</tr>
<tr>
<td>0bxxxx0000, (xxxx != 0000, xxxx != 0100, xxxx != 1010, xxxx != 1111)</td>
<td>UNPREDICTABLE.</td>
</tr>
</tbody>
</table>

'dd' is encoded as follows:

<table>
<thead>
<tr>
<th>dd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Device-nGnRnE memory</td>
</tr>
<tr>
<td>0b01</td>
<td>Device-nGnRE memory</td>
</tr>
<tr>
<td>0b10</td>
<td>Device-NGRE memory</td>
</tr>
<tr>
<td>0b11</td>
<td>Device-GRE memory</td>
</tr>
</tbody>
</table>

'oooo' is encoded as follows:

<table>
<thead>
<tr>
<th>'oooo'</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>See encoding of Attr</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Outer Write-Through Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Outer Non-cacheable</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Outer Write-Back Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Outer Write-Through Non-transient</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Outer Write-Back Non-transient</td>
</tr>
</tbody>
</table>

'R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

'iiii' is encoded as follows:

<table>
<thead>
<tr>
<th>'iiii'</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>See encoding of Attr</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Inner Write-Through Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Inner Non-cacheable</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Inner Write-Back Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Inner Write-Through Non-transient</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Inner Write-Back Non-transient</td>
</tr>
</tbody>
</table>

'R = Inner Read-Allocate policy, W = Inner Write-Allocate policy.

The R and W bits in 'oooo' and 'iiii' fields have the following meanings:

MAIR_EL3, Memory Attribute Indirection Register (EL3)
<table>
<thead>
<tr>
<th>R or W</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Allocate</td>
</tr>
<tr>
<td>0b1</td>
<td>Allocate</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the MAIR_EL3

Accesses to this register use the following encodings:

**MRS <Xt>, MAIR_EL3**

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return MAIR_EL3;
```

**MSR MAIR_EL3, <Xt>**

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    MAIR_EL3 = X[t];
```
**MDCCINT_EL1, Monitor DCC Interrupt Enable Register**

The MDCCINT_EL1 characteristics are:

**Purpose**

Enables interrupt requests to be signaled based on the DCC status flags.

**Configuration**

AArch64 System register MDCCINT_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGDCCINT[31:0].

**Attributes**

MDCCINT_EL1 is a 64-bit register.

**Field descriptions**

The MDCCINT_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>60</td>
<td>RX, bit [30] DCC interrupt request enable control for DTRRX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.</td>
</tr>
<tr>
<td>59</td>
<td>Meaning</td>
</tr>
<tr>
<td>58</td>
<td>No interrupt request generated by DTRRX.</td>
</tr>
<tr>
<td>57</td>
<td>Interrupt request will be generated on RXfull == 1.</td>
</tr>
<tr>
<td>28</td>
<td>TX, bit [29] DCC interrupt request enable control for DTRTX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.</td>
</tr>
<tr>
<td>27</td>
<td>Meaning</td>
</tr>
<tr>
<td>26</td>
<td>No interrupt request generated by DTRTX.</td>
</tr>
<tr>
<td>25</td>
<td>Interrupt request will be generated on TXfull == 0.</td>
</tr>
</tbody>
</table>

If legacy COMMRX and COMMTX signals are implemented, then these are not affected by the value of this bit.

On a Warm reset, this field resets to 0.
Bits [28:0]

Reserved, RES0.

**Accessing the MDCCINT_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, MDCCINT_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC != '00' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA != '00' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  AArch64.SystemAccessTrap(EL3, 0x18);
endif
else
  return MDCCINT_EL1;
endif

MSR MDCCINT_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

AArch64.SystemAccessTrap(EL3, 0x18);
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MDCCINT_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MDCCINT_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    MDCCINT_EL1 = X[t];
else
    MDCCINT_EL1 = X[t];
end
MDCCSR_EL0, Monitor DCC Status Register

The MDCCSR_EL0 characteristics are:

**Purpose**

Read-only register containing control status flags for the DCC.

**Configuration**

AArch64 System register MDCCSR_EL0 bits [30:29] are architecturally mapped to External register [EDSCR][30:29].

AArch64 System register MDCCSR_EL0 bits [30:29] are architecturally mapped to AArch32 System register [DBGDSCR][30:29].

**Attributes**

MDCCSR_EL0 is a 64-bit register.

**Field descriptions**

The MDCCSR_EL0 bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| RES0   | RXfull | TXfull | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    | RES0   | RAZ    |
| 31     | 30     | 29     | 28     | 27     | 26     | 25     | 24     | 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     | 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |

**Bits [63:31]**

Reserved, RES0.

**RXfull, bit [30]**

DTRRX full. Read-only view of the equivalent bit in the EDSCR.

**TXfull, bit [29]**

DTRTX full. Read-only view of the equivalent bit in the EDSCR.

**Bits [28:19]**

Reserved, RES0.

**Bits [18:15]**

Reserved, RAZ.

**Bits [14:13]**

Reserved, RES0.
Bit [12]
Reserved, RAZ.

Bits [11:6]
Reserved, RES0.

Bits [5:2]
Reserved, RAZ.

Bits [1:0]
Reserved, RES0.

**Accessing the MDCCSR_EL0**

Accesses to this register use the following encodings:

```
MRS <Xt>, MDCCSR_EL0
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b11</td>
<td>0b000</td>
<td>0b001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then UNDEFINED;
    elsif MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDA> != '00') then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    else
        return MDCCSR_EL0;
    end if;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then UNDEFINED;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    else
        return MDCCSR_EL0;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    else
        return MDCCSR_EL0;
    end if;
elsif PSTATE.EL == EL3 then
  return MDCCSR_EL0;
The MDCR_EL2 characteristics are:

**Purpose**
Provides EL2 configuration options for self-hosted debug and the Performance Monitors Extension.

**Configuration**
AArch64 System register MDCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HDCR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**
MDCR_EL2 is a 64-bit register.

**Field descriptions**
The MDCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>HPMFZS</td>
<td>TPM</td>
<td>TDCC</td>
<td>HLP</td>
<td>RES0</td>
<td>HCCD</td>
<td>RES0</td>
<td>TTRF</td>
<td>RES0</td>
<td>HPMDR</td>
<td>RES0</td>
<td>TPMSE</td>
<td>E2PB</td>
<td>TDRA</td>
<td>TDOSA</td>
<td>TDAT</td>
<td>TDE</td>
<td>HPME</td>
<td>TPM</td>
<td>RES0</td>
<td>HPMD</td>
<td>RES0</td>
<td>TPM</td>
<td>E2PB</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:37]**
Reserved, RES0.

**HPMFZS, bit [36]**
When FEAT_SPEv1p2 is implemented:

Hyp Performance Monitors Freeze-on-SPE event. Stop counters when PMBLIMITER_EL1.(PMFZ, E) == {1, 1} and PMBSR_EL1.S == 0b1.

<table>
<thead>
<tr>
<th>HPMFZS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on Statistical Profiling Buffer Management event.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters do not count following a Statistical Profiling Buffer Management event.</td>
</tr>
</tbody>
</table>

If MDCR_EL2.HPMN is less than PMCR_EL0.N, this bit affects the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].

If MDCR_EL2.HPMN is equal to PMCR_EL0.N, this bit has no effect.

This bit does not affect the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)] and PMCCNTR_EL0.

The operation of this bit applies even when EL2 is disabled in the current Security state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:
Reserved, RES0.

**Bits [35:30]**
Reserved, RES0.

**HPMFZO, bit [29]**

When FEAT_PMUv3p7 is implemented:

Hyp Performance Monitors Freeze-on-overflow. Stop event counters on overflow.

<table>
<thead>
<tr>
<th>HPMFZO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on overflow. Event counters do not count when PMOVSCLR_EL0((PMCR_EL0.N-1):MDCR_EL2.HPMN) is nonzero.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

If MDCR_EL2.HPMN is less than PMCR_EL0.N, this bit affects the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].

If MDCR_EL2.HPMN is equal to PMCR_EL0.N, this bit has no effect.

This bit does not affect the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)] and PMCCNTR_EL0.

The operation of this bit ignores the values of PMOVSCLR_EL0((MDCR_EL2.HPMN-1):0].

The operation of this bit applies even when EL2 is disabled in the current Security state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

**MTPME, bit [28]**

When FEAT_MTPMU is implemented and EL3 is not implemented:

Multi-threaded PMU Enable. Enables use of the PMEVTYPER<n>_EL0.MT bits.

<table>
<thead>
<tr>
<th>MTPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FEAT_MTPMU is disabled. The Effective value of PMEVTYPER&lt;n&gt;_EL0.MT is zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMEVTYPER&lt;n&gt;_EL0.MT bits not affected by this bit.</td>
</tr>
</tbody>
</table>

If FEAT_MTPMU is disabled for any other PE in the system that has the same level 1 Affinity as the PE, it is IMPLEMENTATION DEFINED whether the PE behaves as if this bit is 0b0.

On a Cold reset, this field resets to 1.

Otherwise:
Reserved, RES0.

**TDCC, bit [27]**

When FEAT_FGT is implemented:

Trap DCC. Traps use of the Debug Comms Channel at EL1 and EL0 to EL2.
The DCC registers trapped by this control are:

AArch64: OSDTRRX_EL1, OSDTRTX_EL1, MDCCSR_EL0, MDCCINT_EL1, and, when the PE is in Non-debug state, DBGDTR_EL0, DBGDTRRX_EL0, and DBGDTRTX_EL0.

AArch32: DBGDTRRXext, DBGDTRTXext, DBGDSCRint, DBGDCCINT, and, when the PE is in Non-debug state, DBGDTRRXint and DBGDTRTXint.

The traps are reported with EC syndrome value:

- 0x05 for trapped AArch32 MRC and MCR accesses with coproc == 0b1110.
- 0x06 for trapped AArch32 LDC to DBGDTRTXint and STC from DBGDTRRXint.
- 0x18 for trapped AArch64 MRS and MSR accesses.

When the PE is in Debug state, MDCR_EL2.TDCC does not trap any accesses to:

AArch64: DBGDTR_EL0, DBGDTRRX_EL0, and DBGDTRTX_EL0.

AArch32: DBGDTRRXint and DBGDTRTXint.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HLP, bit [26]

When FEAT_PMUv3p5 is implemented:

Hypervisor Long event counter enable. Determines when unsigned overflow is recorded by a counter overflow bit.

<table>
<thead>
<tr>
<th>HLP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;np&gt; EL0[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;np&gt; EL0[63:0].</td>
</tr>
</tbody>
</table>

If MDCR_EL2.HPMN is less than PMCR_EL0.N or PMCR_N, this bit affects the operation of event counters in the range [MDCR_EL2.HPMN..(PMCR_EL0.N-1)] or [MDCR_EL2.HPMN..(PMCR_N-1)]. Otherwise this bit has no effect on the operation of the event counters.

Note

The effect of MDCR_EL2.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state.

For more information see the description of the MDCR_EL2.HPMN field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
Bits [25:24]

Reserved, RES0.

**HCCD, bit [23]**

*When FEAT_PMUv3p5 is implemented:*

Hypervisor Cycle Counter Disable. Prohibits PMCCNTR_EL0 from counting at EL2.

<table>
<thead>
<tr>
<th>HCCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR_EL0 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counting by PMCCNTR_EL0 is prohibited at EL2.</td>
</tr>
</tbody>
</table>

This bit does not affect the CPU_CYCLES event or any other event that counts cycles.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**Bits [22:20]**

Reserved, RES0.

**TTRF, bit [19]**

*When FEAT_TRF is implemented:*

Traps use of the Trace Filter Control registers at EL1 to EL2, as follows:

- Access to TRFCR_EL1 is trapped to EL2, reported using EC syndrome value 0x18.
- Access to TRFCR is trapped to EL2, reported using EC syndrome value 0x03.

<table>
<thead>
<tr>
<th>TTRF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to TRFCR_EL1 and TRFCR at EL1 are not affected by this control.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to TRFCR_EL1 and TRFCR at EL1 generate a trap exception to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

**Bit [18]**

Reserved, RES0.

**HPMD, bit [17]**

*When FEAT_PMUv3p1 is implemented:*

Guest Performance Monitors Disable. This control prohibits event counting at EL2.
### HPMD

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting allowed at EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting prohibited at EL2. If FEAT_Debugv8p2 is not implemented, event counting is prohibited unless enabled by the IMPLEMENTATION DEFINED authentication interface <code>ExternalSecureNoninvasiveDebugEnabled()</code>.</td>
</tr>
</tbody>
</table>

This control applies only to:

- The event counters in the range [0..(MDCR_EL2.HPMN-1)].
- If `PMCR_EL0.DP` is set to 1, `PMCCNTR_EL0`.

The other event counters are unaffected, and when `PMCR_EL0.DP` is set to 0, `PMCCNTR_EL0` is unaffected.

On a Warm reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### Bits [16:15]

Reserved, RES0.

### TPMS, bit [14]

**When FEAT_SPE is implemented:**

Trap Performance Monitor Sampling. If EL2 is implemented and enabled in the current Security state, controls access to Statistical Profiling control registers from EL1.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not trap Statistical Profiling controls to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, accesses to Statistical Profiling control registers at EL1 generate a Trap exception to EL2.</td>
</tr>
</tbody>
</table>

The Statistical Profiling control registers trapped by this control are:

- `PMSCR_EL1`, `PMSEVFR_EL1`, `PMSFCR_EL1`, `PMSICR_EL1`, `PMSIDR_EL1`, `PMSIRR_EL1`, and `PMSLATFR_EL1`.
- If FEAT_SPEv1p2 is implemented, `PMSNEVFR_EL1`.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

### E2PB, bits [13:12]

**When FEAT_SPE is implemented:**

EL2 Profiling Buffer. If EL2 is implemented and enabled in the Profiling Buffer owning Security state, this field controls the owning translation regime. If EL2 is implemented and enabled in the current Security state, this field controls access to Profiling Buffer control registers from EL1.
Meaning

0b00 If EL2 is implemented and enabled in the Profiling Buffer owning Security state, the Profiling Buffer uses the EL2 or EL2&0 stage 1 translation regime. Otherwise the Profiling Buffer uses the EL1&0 stage 1 translation regime. If EL2 is implemented and enabled in the current Security state, accesses to Profiling Buffer control registers at EL1 generate a Trap exception to EL2.

0b10 Profiling Buffer uses the EL1&0 stage 1 translation regime. If EL2 is implemented and enabled in the current Security state, accesses to Profiling Buffer control registers at EL1 generate a Trap exception to EL2.

0b11 Profiling Buffer uses the EL1&0 stage 1 translation regime. Accesses to Profiling Buffer control registers at EL1 are not trapped to EL2.

All other values are reserved.

The Profiling Buffer control registers trapped by this control are: PMBLIMITR_EL1, PMBPTR_EL1, and PMBSR_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TDRA, bit [11]

Trap Debug ROM Address register access. Traps System register accesses to the Debug ROM registers to EL2 when EL2 is enabled in the current Security state as follows:

- If EL1 is using AArch64 state, accesses to MDRAR_EL1 are trapped to EL2, reported using EC syndrome value 0x18.
- If EL0 or EL1 is using AArch32 state, MRC or MCR accesses to the following registers are trapped to EL2, reported using EC syndrome value 0x05 and MRRC or MCRR accesses are trapped to EL2, reported using EC syndrome value 0x0C:
  - DBGDRAR, DBGDSAR.

This field is treated as being 1 for all purposes other than a direct read when one or more of the following are true:

- MDCR_EL2.TDE == 1.
- HCR_EL2.TGE == 1.

Note

EL2 does not provide traps on debug register accesses through the optional memory-mapped external debug interfaces.

System register accesses to the debug registers might have side-effects. When a System register access is trapped to EL2, no side-effects occur before the exception is taken to EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TDOSA, bit [10]

When FEAT_DoubleLock is implemented:

Trap debug OS-related register access. Traps EL1 System register accesses to the powerdown debug registers to EL2, from both Execution states as follows:
In AArch64 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value \(0x18\):

- OSLAR_EL1, OSLSR_EL1, OSDLR_EL1, and DBGPRCR_EL1.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

In AArch32 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value \(0x05\):

- DBGOSLSR, DBGOSLAR, DBGOSDLR, and DBGPRCR.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 System register accesses to the powerdown debug registers are trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

**Note**

These registers are not accessible at EL0.

This field is treated as being 1 for all purposes other than a direct read when one or more of the following are true:

- **MDCR_EL2.TDE == 1.**
- **HCR_EL2.TGE == 1.**

System register accesses to the debug registers might have side-effects. When a System register access is trapped to EL2, no side-effects occur before the exception is taken to EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Trap debug OS-related register access. Traps EL1 System register accesses to the powerdown debug registers to EL2, from both Execution states as follows:

In AArch64 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value \(0x18\):

- OSLAR_EL1, OSLSR_EL1, and DBGPRCR_EL1.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

In AArch32 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value \(0x05\):

- DBGOSLSR, DBGOSLAR, and DBGPRCR.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

It is IMPLEMENTATION DEFINED whether accesses to OSDLR_EL1 are trapped.

It is IMPLEMENTATION DEFINED whether accesses to DBGOSDLR are trapped.

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 System register accesses to the powerdown debug registers are trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>

**Note**

These registers are not accessible at EL0.

This field is treated as being 1 for all purposes other than a direct read when one or more of the following are true:
Note

EL2 does not provide traps on debug register accesses through the optional memory-mapped external debug interfaces.

System register accesses to the debug registers might have side-effects. When a System register access is trapped to EL2, no side-effects occur before the exception is taken to EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TDA, bit [9]**

Trap Debug Access. Traps EL0 and EL1 System register accesses to debug System registers that are not trapped by MDCR_EL2.TDRA or MDCR_EL2.TDOSA, as follows:

- In AArch64 state, accesses to the following registers are trapped to EL2 reported using EC syndrome value 0x18:
  - MDCCSR_EL0, MDCCINT_EL1, OSDTRRX_EL1, MDSCR_EL1, OSDTRTX_EL1, OSECCR_EL1, DBGVR<n>_EL1, DBGCR<n>_EL1, DBGWVR<n>_EL1, DBGWCR<n>_EL1, DBGCLAIMCLR_EL1, DBGAUTHSTATUS_EL1,
  - When not in Debug state, DBGDTR_EL0, DBGDTRRX_EL0, DBGDTRTX_EL0.
- In AArch32 state, MRC or MCR accesses to the following registers are trapped to EL2, reported using EC syndrome value 0x05:
  - DBGDIDR, DBGDCINT, DBGWFAR, DBGVCR, DBGDCRext, DBGDTRXext, DBGDTRRXext, DBGVR<n>, DBGCR<n>, DBGXVR<n>, DBGWCR<n>, DBGWVR<n>, DBGCLAIMCLR, DBGAUTHSTATUS, DBGDEVID, DBGDEVID1, DBGDEVID2, DBGSECCR,
  - When not in Debug state, DBGDTRRXint and DBGDTRTXint.
- In AArch32 state, STC accesses to DBGDTRRXint and LDC accesses to DBGDTRTXint are trapped to EL2, reported using EC syndrome value 0x06.

<table>
<thead>
<tr>
<th>TDA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 or EL1 System register accesses to the debug registers are trapped from both Execution states to EL2 when EL2 is enabled in the current Security state, unless the access generates a higher priority exception.</td>
</tr>
</tbody>
</table>

Traps of AArch32 accesses to DBGDTRRXint and DBGDTRTXint are ignored in Debug state.

Traps of AArch64 accesses to DBGDTR_EL0, DBGDTRRX_EL0, and DBGDTRTX_EL0 are ignored in Debug state.

This field is treated as being 1 for all purposes other than a direct read when one or more of the following are true:

- **MDCR_EL2.TDE == 1**
- **HCR_EL2.TGE == 1**

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TDE, bit [8]**

Trap Debug Exceptions. Controls routing of Debug exceptions, and defines the debug target Exception level, EL_D.

<table>
<thead>
<tr>
<th>TDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The debug target Exception level is EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is enabled for the current Effective value of <strong>SCR_EL3.NS</strong>, the debug target Exception level is EL2, otherwise the debug target Exception level is EL1.</td>
</tr>
</tbody>
</table>

The MDCR_EL2.(TDRA, TDOSA, TDA) fields are treated as being 1 for all purposes other than returning the result of a direct read of the register.

For more information, see 'Routing debug exceptions'.

This field is treated as being 1 for all purposes other than a direct read when **HCR_EL2.TGE == 1**.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**HPME, bit [7]**  
When FEAT_PMUv3 is implemented:

[MDCR_EL2.HPMN..(N-1)] event counters enable.

<table>
<thead>
<tr>
<th>HPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counters in the range [MDCR_EL2.HPMN..(PMCR_EL0.N-1)] are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters in the range [MDCR_EL2.HPMN..(PMCR_EL0.N-1)] are enabled by PMCNTENSET_EL0.</td>
</tr>
</tbody>
</table>

If MDCR_EL2.HPMN is less than PMCR_EL0.N or PMCR.N, the event counters in the range [MDCR_EL2.HPMN..(PMCR_EL0.N-1)] or [HDCR.HPMN..(PMCR.N-1)], are enabled and disabled by this bit. Otherwise this bit has no effect on the operation of the event counters.

**Note**

The effect of MDCR_EL2.HPMN on the operation of this bit applies regardless of whether EL2 is enabled in the current Security state.

For more information see the description of the HPMN field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**TPM, bit [6]**  
When FEAT_PMUv3 is implemented:

Trap Performance Monitors accesses. Traps EL0 and EL1 accesses to all Performance Monitor registers to EL2 when EL2 is enabled in the current Security state, from both Execution states, as follows:

- In AArch64 state, accesses to the following registers are trapped to EL2, reported using EC syndrome value 0x18:
  - PMCR_EL0, PMCNTENSET_EL0, PMCNTENCLR_EL0, PMOVSCLR_EL0, PMSWINC_EL0, PMSEL0_EL0, PMCEID0_EL0, PMCEID1_EL0, PMCCNTR_EL0, PMXEVTYPER_EL0, PMXEVNCTR_EL0, PMUSERENR_EL0, PMINTENSET_EL1, PMINTENCLR_EL1, PMOVSET_EL0, PMEVCNTR<->_EL0, PMEVTYPER<n>_EL0, PMCCFILTR_EL0.
  - If FEAT_PMUv3p4 is implemented, PMMIR_EL1

- In AArch32 state, MRCC or MCR accesses to the following registers are trapped to EL2 and reported using EC syndrome value 0x03, MRRC or MCRR accesses are trapped to EL2 and reported using EC syndrome value 0x04:
  - PMCR, PMCNTENSET, PMCNTENCLR, PMOVS, PMSWINC, PMSEL, PMCEID0, PMCEID1, PMCCNTR, PMXEVTYPER, PMXEVCNTR, PMUSERENR, PMINTENSET, PMINTENCLR, PMOVSET, PMEVCNTR<n>, PMEVTYPER<n>, PMCCFILTR.
  - If FEAT_PMUv3p4 is implemented, PMMIR.
  - If FEAT_PMUv3p1 is implemented, PMCEID2, and PMCEID3.

<table>
<thead>
<tr>
<th>TPM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 and EL1 accesses to all Performance Monitor registers are trapped to EL2 when EL2 is enabled in the current Security state.</td>
</tr>
</tbody>
</table>
Note

EL2 does not provide traps on Performance Monitor register accesses through the optional memory-mapped external debug interface.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TPMCR, bit [5]

When FEAT_PMUv3 is implemented:

Trap PMCR_EL0 or PMCR accesses. Traps EL0 and EL1 accesses to EL2, when EL2 is enabled in the current Security state, as follows:

- In AArch64 state, accesses to PMCR_EL0 are trapped to EL2, reported using EC syndrome value 0x18.
- In AArch32 state, accesses to PMCR are trapped to EL2, reported using EC syndrome value 0x03.

<table>
<thead>
<tr>
<th>TPMCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 and EL1 accesses to the PMCR_EL0 or PMCR are trapped to EL2 when EL2 is enabled in the current Security state, unless it is trapped by PMUSERENR.EN or PMUSERENR_EL0.EN.</td>
</tr>
</tbody>
</table>

Note

EL2 does not provide traps on Performance Monitor register accesses through the optional memory-mapped external debug interface.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HPMN, bits [4:0]

When FEAT_PMUv3 is implemented:

Defines the number of event counters that are accessible from EL3, EL2, EL1, and from EL0 if permitted.

If HPMN is less than PMCR_EL0.N, HPMN divides the Performance Monitors into two ranges: [0..(HPMN-1)] and [HPMN..(PMCR_EL0.N-1)].

For an event counter in the range [0..(HPMN-1)]:

- The counter is accessible from EL3, EL2, and EL1, and from EL0 if permitted by PMUSERENR_EL0 or PMUSERENR.
- If FEAT_PMUv3p5 is implemented, PMCR_EL0.LP or PMCR LP determines whether the counter overflow flag is set on unsigned overflow of PMEVCNTR<n>_EL0[31:0] or PMEVCNTR<n>_EL0[63:0].
- The counter is enabled by PMCR_EL0.E or PMCR.E and bit <n> of PMCNTENSET_EL0.

Note

If HPMN is equal to PMCR_EL0.N, this applies to all event counters.

If HPMN is less than PMCR_EL0.N, for an event counter in the range [HPMN..(PMCR_EL0.N-1)]:

The counter is accessible from EL2 and EL3.
If FEAT_SEL2 is disabled or is not implemented, the counter is also accessible from Secure EL1, and from Secure EL0 if permitted by PMUSERENR_EL0.
If FEAT_PMUv3p5 is implemented, MDCR_EL2.HLP or HDCR.HLP determines whether the counter overflow flag is set on unsigned overflow of PMEVCNTR<n>_EL0[31:0] or PMEVCNTR<n>_EL0[63:0].
The counter is enabled by MDCR_EL2.HPME or HDCR.HPME and bit <n> of PMCNTENSEL_EL0.

If this field is set to 0, or to a value larger than PMCR_EL0.N, then the following CONSTRAINED UNPREDICTABLE behaviors apply:

- The value returned by a direct read of MDCR_EL2.HPMN is UNKNOWN.
- Either:
  - An UNKNOWN number of counters are reserved for EL2 and EL3 use. That is, the PE behaves as if MDCR_EL2.HPMN is set to an UNKNOWN non-zero value less than or equal to PMCR_EL0.N.
  - All counters are reserved for EL2 and EL3 use, meaning no counters are accessible from EL1 and EL0.

On a Warm reset, this field resets to the value in PMCR_EL0.N.

Otherwise:

Reserved, RES0.

**Accessing the MDCR_EL2**

Accesses to this register use the following encodings:

**MRS <Xt>, MDCR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            return MDCR_EL2;
    else
        return MDCR_EL2;
elsif PSTATE.EL == EL3 then
    return MDCR_EL2;

**MSR MDCR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        MDCR_EL2 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    MDCR_EL2 = X[t];
MDCR_EL3, Monitor Debug Configuration Register (EL3)

The MDCR_EL3 characteristics are:

**Purpose**

Provides EL3 configuration options for self-hosted debug and the Performance Monitors Extension.

**Configuration**

AArch64 System register MDCR_EL3 bits [31:0] can be mapped to AArch32 System register $SDCR[31:0]$, but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to MDCR_EL3 are UNDEFINED.

**Attributes**

MDCR_EL3 is a 64-bit register.

**Field descriptions**

The MDCR_EL3 bit assignments are:

| Bits   | 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  |
|--------|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| REG    | RES0| RES0| RES0| RES0| ENPMSN| MTPM| TDC| RES0| SCD| RES0| RES0| RES0| EDM| EPM| TTT| RES0| RES0| SPM| SDD| SPD32| NSP| RES0| RES0| RES0| RES0| RES0| RES0| TPM|
| Values | 313029 | 28 | 27 | 262524 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  |

**Bits [63:37]**

Reserved, RES0.

**EnPMSN, bit [36]**

When FEAT_SPEv1p2 is implemented:

Trap accesses to $PMSNEVFR_EL1$. Controls access to Statistical Profiling $PMSNEVFR_EL1$ System register from EL2 and EL1.

<table>
<thead>
<tr>
<th>EnPMSN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to $PMSNEVFR_EL1$ at EL2 and EL1 generate a Trap exception to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not trap $PMSNEVFR_EL1$ to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
MPMX, bit [35]

When FEAT_PMUv3p7 is implemented:

Monitor Performance Monitors Extended control. In conjunction with MDCR_EL3.SPME, controls when event counters are disabled at EL3 and in other Secure Exception levels.

<table>
<thead>
<tr>
<th>MPMX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting by some or all event counters is prohibited at EL3.</td>
</tr>
</tbody>
</table>

If EL2 is implemented, MDCR_EL3.SPME == 0b1, and MDCR_EL2.HPMN is less than PMCR_EL0.N then all the following are true:

- This bit affects the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)].
- This bit does not affect the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].
- This applies even when EL2 is disabled in Secure state.

If EL2 is not implemented, MDCR_EL3.SPME == 0b0, or MDCR_EL2.HPMN is equal to PMCR_EL0.N then this bit affects the operation of all event counters.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

MCCD, bit [34]

When FEAT_PMUv3p7 is implemented:

Monitor Cycle Counter Disable. Prohibits the Cycle Counter, PMCCNTR_EL0, from counting at EL3.

<table>
<thead>
<tr>
<th>MCCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR_EL0 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counting by PMCCNTR_EL0 is prohibited at EL3.</td>
</tr>
</tbody>
</table>

This bit does not affect the CPU_CYCLES event or any other event that counts cycles.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

Bits [33:29]

Reserved, RES0.

MTPME, bit [28]

When FEAT_MTPMU is implemented:

Multi-threaded PMU Enable. Enables use of the PMEVTYPER<n>_EL0.MT bits.

<table>
<thead>
<tr>
<th>MTPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FEAT_MTPMU is disabled. The Effective value of PMEVTYPER&lt;n&gt;_EL0.MT is zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMEVTYPER&lt;n&gt;_EL0.MT bits not affected by this bit.</td>
</tr>
</tbody>
</table>

If FEAT_MTPMU is disabled for any other PE in the system that has the same level 1 Affinity as the PE, it is IMPLEMENTATION DEFINED whether the PE behaves as if this bit is 0b0.

On a Cold reset, this field resets to 1.
**TDCC, bit [27]**

When FEAT_FGT is implemented:

Trap DCC. Traps use of the Debug Comms Channel at EL2, EL1, and EL0 to EL3.

<table>
<thead>
<tr>
<th>TDCC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any register accesses to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to the DCC registers at EL2, EL1, and EL0 generate a Trap exception to EL3, unless the access also generates a higher priority exception. Traps on the DCC data transfer registers are ignored when the PE is in Debug state.</td>
</tr>
</tbody>
</table>

The DCC registers trapped by this control are:

- **AArch64**: OSDTRRX_EL1, OSDTRTX_EL1, MDCCSR_EL0, MDCCINT_EL1, and, when the PE is in Non-debug state, DBGDTR_EL0, DBGDTRRX_EL0, and DBGDTRTX_EL0.
- **AArch32**: DBGDTRRXext, DBGDTRTXext, DBGDSCRint, DBGDCCINT, and, when the PE is in Non-debug state, DBGDTRRXint and DBGDTRTXint.

The traps are reported with EC syndrome value:

- 0x05 for trapped AArch32 MRC and MCR accesses with coproc == 0b1110.
- 0x06 for trapped AArch32 LDC to DBGDTRRXint and STC from DBGDTRRXint.
- 0x18 for trapped AArch64 MRS and MSR accesses.

When the PE is in Debug state, MDCR_EL3.TDCC does not trap any accesses to:

- **AArch64**: DBGDTR_EL0, DBGDTRRX_EL0, and DBGDTRTX_EL0.
- **AArch32**: DBGDTRRXint and DBGDTRTXint.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SCCD, bit [23]**

When FEAT_PMUv3p5 is implemented:

Secure Cycle Counter Disable. Prohibits PMCCNTR_EL0 from counting in Secure state.

<table>
<thead>
<tr>
<th>SCCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR_EL0 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counting by PMCCNTR_EL0 is prohibited in Secure state.</td>
</tr>
</tbody>
</table>

This bit does not affect the CPU_CYCLES event or any other event that counts cycles.

On a Warm reset, this field resets to 0.
Otherwise:
Reserved, RES0.

Bit [22]
Reserved, RES0.

**EPMAD, bit [21]**

*When FEAT_Debugv8p4 is implemented and FEAT_PMUv3 is implemented:*

External Performance Monitors Non-secure Access Disable. Controls Non-secure access to Performance Monitor registers by an external debugger.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure access to Performance Monitor registers from external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure access to Performance Monitor registers from external debugger is not permitted.</td>
</tr>
</tbody>
</table>

If the Performance Monitors Extension does not support external debug interface accesses this bit is RES0.

Otherwise, if EL3 is not implemented and the Effective value of SCR_EL3.NS is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, this field resets to 0.

*When FEAT_PMUv3 is implemented:*

External Performance Monitors Access Disable. Controls access to Performance Monitor registers by an external debugger.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Performance Monitor registers from external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Performance Monitor registers from external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
</tbody>
</table>

If the Performance Monitors Extension does not support external debug interface accesses this bit is RES0.

Otherwise, if EL3 is not implemented and the Effective value of SCR_EL3.NS is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, this field resets to 0.

*Otherwise:*

Reserved, RES0.

**EDAD, bit [20]**

*When FEAT_Debugv8p4 is implemented:*

External Debug Non-secure Access Disable. Controls Non-secure access to breakpoint, watchpoint, and OSLAR_EL1 registers by an external debugger.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure access to debug registers from external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure access to breakpoint and watchpoint registers, and OSLAR_EL1 from external debugger is not permitted.</td>
</tr>
</tbody>
</table>
If EL3 is not implemented and the Effective value of `SCR_EL3.NS` is \(0b0\), then the Effective value of this field is \(0b1\).

On a Warm reset, this field resets to \(0\).

### When FEAT_Debugv8p2 is implemented:

External Debug Access Disable. Controls access to breakpoint, watchpoint, and `OSLAR_EL1` registers by an external debugger.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>Access to debug registers, and to <code>OSLAR_EL1</code> from external debugger is permitted.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>Access to breakpoint and watchpoint registers, and to <code>OSLAR_EL1</code> from external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of `SCR_EL3.NS` is \(0b0\), then the Effective value of this field is \(0b1\).

On a Warm reset, this field resets to \(0\).

Otherwise:

External Debug Access disable. Controls access to breakpoint, watchpoint, and optionally `OSLAR_EL1` registers by an external debugger.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>Access to debug registers from external debugger is permitted.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>Access to breakpoint and watchpoint registers from an external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface. It is IMPLEMENTATION DEFINED whether access to the <code>OSLAR_EL1</code> register from an external debugger is permitted or not permitted.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of `SCR_EL3.NS` is \(0b0\), then the Effective value of this field is \(0b1\).

On a Warm reset, this field resets to \(0\).

### TTRF, bit [19]

#### When FEAT_TRF is implemented:

Trap Trace Filter controls. Traps use of the Trace Filter control registers at EL2 and EL1 to EL3.

The Trace Filter registers trapped by this control are:

- `TRFCR_EL2`, `TRFCR_EL12`, `TRFCR_EL1`, reported using EC syndrome value \(0x18\).
- `HTRFCR` and `TRFCR`, reported using EC syndrome value \(0x03\).

<table>
<thead>
<tr>
<th>TTRF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>Accesses to Trace Filter registers at EL2 and EL1 are not affected by this bit.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>Accesses to Trace Filter registers at EL2 and EL1 generate a Trap exception to EL3, unless the access generates a higher priority exception.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, \(RES0\).

### STE, bit [18]
When FEAT_TRF is implemented:

Secure Trace enable. Enables tracing in Secure state.

<table>
<thead>
<tr>
<th>STE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace prohibited in Secure state unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace in Secure state is not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit also controls the level of authentication required by an external debugger to enable external tracing. See 'Register controls to enable self-hosted trace'.

If EL3 is not implemented and the Effective value of SCR_EL3_NS is 0b0, the Effective value of this bit is 0b1.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

SPME, bit [17]

When FEAT_PMUv3 is implemented and FEAT_PMUv3p7 is implemented:

Secure Performance Monitors Enable.

Controls event counting in Secure state and EL3.

When MDCR_EL3.MPMX == 0b1, this bit affects the operation of event counters at EL3 only. See MDCR_EL3.MPMX for more information.

<table>
<thead>
<tr>
<th>SPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When MDCR_EL3.MPMX == 0b0: Event counting prohibited in Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>When MDCR_EL3.MPMX == 0b0: Event counting in Secure state not affected by this bit.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of SCR_EL3_NS is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, this field resets to 0.

When FEAT_PMUv3 is implemented and FEAT_Debugv8p2 is implemented:

Secure Performance Monitors Enable. Controls event counting in Secure state.

<table>
<thead>
<tr>
<th>SPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting prohibited in Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting in Secure state not affected by this bit.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of SCR_EL3_NS is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, this field resets to 0.

When FEAT_PMUv3 is implemented:

Secure Performance Monitors Enable. Controls event counting in Secure state.

<table>
<thead>
<tr>
<th>SPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting prohibited in Secure state, unless ExternalSecureNoninvasiveDebugEnabled() is TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting in Secure state not affected by this bit.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of SCR_EL3_NS is 0b0, then the Effective value of this bit is 0b1.
On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**SDD, bit [16]**

AArch64 Secure Self-hosted invasive debug disable. Disables Software debug exceptions in Secure state, other than Breakpoint Instruction exceptions.

<table>
<thead>
<tr>
<th>SDD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Debug exceptions in Secure state are not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Debug exceptions, other than Breakpoint Instruction exceptions, are disabled from all Exception levels in Secure state.</td>
</tr>
</tbody>
</table>

The SDD bit is ignored unless both of the following are true:

- The PE is in Secure state.
- The Effective value of **SCR_EL3**.RW is 0b1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**SPD32, bits [15:14]**

When EL1 is capable of using AArch32:

AArch32 Secure self-hosted privileged debug. Enables or disables debug exceptions from Secure EL1 using AArch32, other than Breakpoint Instruction exceptions.

<table>
<thead>
<tr>
<th>SPD32</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Legacy mode. Debug exceptions from Secure EL1 are enabled by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
<tr>
<td>0b10</td>
<td>Secure privileged debug disabled. Debug exceptions from Secure EL1 are disabled.</td>
</tr>
<tr>
<td>0b11</td>
<td>Secure privileged debug enabled. Debug exceptions from Secure EL1 are enabled.</td>
</tr>
</tbody>
</table>

Other values are reserved, and have the CONstrained UNPredictable behavior that they must have the same behavior as 0b00. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

This field has no effect on Breakpoint Instruction exceptions. These are always enabled.

This field is ignored if the PE is either:

- In Non-secure state.
- In Secure state and Secure EL1 is using AArch64.

If Secure EL1 is using AArch32 then:

- If debug exceptions from Secure EL1 are enabled, then debug exceptions from Secure EL0 are also enabled.
- Otherwise, debug exceptions from Secure EL0 are enabled only if the value of **SDER32_EL3**.SUIDEN is 0b1.

If EL3 is not implemented and the Effective value of **SCR_EL3**.NS is 0b0, then the Effective value of this field is 0b11.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.
When FEAT_SPE is implemented:

Non-secure Profiling Buffer. Controls the owning translation regime and accesses to Statistical Profiling and Profiling Buffer control registers.

<table>
<thead>
<tr>
<th>NSPB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Profiling Buffer uses Secure Virtual Addresses. Statistical Profiling enabled in Secure state and disabled in Non-secure state. Accesses to Statistical Profiling and Profiling Buffer control registers at EL2 and EL1 in both Security states generate Trap exceptions to EL3.</td>
</tr>
<tr>
<td>0b01</td>
<td>Profiling Buffer uses Secure Virtual Addresses. Statistical Profiling enabled in Secure state and disabled in Non-secure state. Accesses to Statistical Profiling and Profiling Buffer control registers at EL2 and EL1 in Non-secure state generate Trap exceptions to EL3.</td>
</tr>
<tr>
<td>0b10</td>
<td>Profiling Buffer uses Non-secure Virtual Addresses. Statistical Profiling enabled in Non-secure state and disabled in Secure state. Accesses to Statistical Profiling and Profiling Buffer control registers at EL2 and EL1 in both Security states generate Trap exceptions to EL3.</td>
</tr>
<tr>
<td>0b11</td>
<td>Profiling Buffer uses Non-secure Virtual Addresses. Statistical Profiling enabled in Non-secure state and disabled in Secure state. Accesses to Statistical Profiling and Profiling Buffer control registers at EL2 and EL1 in Secure state generate Trap exceptions to EL3.</td>
</tr>
</tbody>
</table>

The Statistical Profiling and Profiling Buffer control registers trapped by this control are:

- PMBLIMITR_EL1, PMBPTR_EL1, PMBSR_EL1, PMSCR_EL1, PMSCR_EL2, PMSEVFR_EL1, PMSFCSR_EL1, PMSICR_EL1, PMSIDR_EL1, PMBSR_EL1, and PMSLATFR_EL1.
- If FEAT_SPEv1p2 is implemented, PMSNEVFR_EL1.

If EL3 is not implemented and the Effective value of SCR_EL3.NS is 0b1, the Effective value of this field is 0b11.

If EL3 is not implemented and the Effective value of SCR_EL3.NS is 0b0, the Effective value of this field is 0b01.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [11]

Reserved, RES0.

TDOSA, bit [10]

When FEAT_DoubleLock is implemented:

Trap debug OS-related register access. Traps EL2 and EL1 System register accesses to the powerdown debug registers to EL3.

Accesses to the registers are trapped as follows:

- Accesses from AArch64 state, OSLAR_EL1, OSLSR_EL1, OSDLR_EL1, DBGOSLAR, DBGOSLHR, DBGOSDLR, and DBGOSLHR, are trapped to EL3 and reported using EC syndrome value 0x18.
- Accesses using MCR or MRC to DBGOSLAR, DBGOSLHR, DBGOSDLR, and DBGOSLHR, are trapped to EL3 and reported using EC syndrome value 0x05.
- Accesses to any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.
## TDOSA

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 and EL1 System register accesses to the powerdown debug registers are trapped to EL3, unless it is trapped by \texttt{HDCR.TDOSA} or \texttt{MDCR.EL2.TDOSA}.</td>
</tr>
</tbody>
</table>

### Note

The powerdown debug registers are not accessible at EL0.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

### Otherwise:

Trap debug OS-related register access. Traps EL2 and EL1 System register accesses to the powerdown debug registers to EL3.

The following registers are affected by this trap:

- AArch64: \texttt{Oslar_EL1}, \texttt{Oslsr_EL1}, and \texttt{Dbgpocr_EL1}.
- AArch32: \texttt{Dbgoslar}, \texttt{Dbgoslslr}, and \texttt{Dbgpocr}.
- AArch64 and AArch32: Any \texttt{IMPLEMENTATION DEFINED} register with similar functionality that the implementation specifies as trapped by this bit.
- It is \texttt{IMPLEMENTATION DEFINED} whether accesses to \texttt{Osdler_EL1} and \texttt{Dbgosdlr} are trapped.

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 and EL1 System register accesses to the powerdown debug registers are trapped to EL3, unless it is trapped by \texttt{HDCR.TDOSA} or \texttt{MDCR.EL2.TDOSA}.</td>
</tr>
</tbody>
</table>

### Note

The powerdown debug registers are not accessible at EL0.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

### TDA, bit [9]

Trap Debug Access. Traps EL2, EL1, and EL0 System register accesses to those debug System registers that cannot be trapped using the MDCR.EL3.TDOSA field.

Accesses to the debug registers are trapped as follows:

- In AArch64 state, the following registers are trapped to EL3 and reported using EC syndrome value \texttt{0x18}:
  - \texttt{DBGVR<n> EL1}, \texttt{DBGBCR<n> EL1}, \texttt{DBGWVR<n> EL1}, \texttt{DBGWCR<n> EL1}, \texttt{DBGCLAIMSET_EL1}, \texttt{DBGCLAIMCLR_EL1}, \texttt{DBGAUTHSTATUS_EL1}, \texttt{DBGVCR<n> EL2}.
  - AArch64: \texttt{MDCR_EL2}, \texttt{MDRAR_EL1}, \texttt{MDCCSR_EL0}, \texttt{MDCCINT_EL1}, \texttt{MDSRCR_EL1}, \texttt{OSDTRRX_EL1}, \texttt{OSDTRTX_EL1}, \texttt{OSECRR_EL1}.
- In AArch32 state, \texttt{SDER} is trapped to EL3 and reported using EC syndrome value \texttt{0x03}.
- In AArch32 state, accesses using MCR or MRC to the following registers are reported using EC syndrome value \texttt{0x05}, accesses using MCRR or MRRC are reported using EC syndrome value \texttt{0x0C}:
  - \texttt{HDCR}, \texttt{DBGDRAR}, \texttt{DBGDSAR}, \texttt{DBGDIDR}, \texttt{DBGDCCINT}, \texttt{DBGWFR}, \texttt{DBGVCR}, \texttt{DBGVCR<n>}, \texttt{DBGBCR<n>}, \texttt{DBGWVR<n>}, \texttt{DBGWVR<n>}, \texttt{DBGVCR<n>}, \texttt{DBGCINT}, \texttt{DBGAUTHSTATUS}, \texttt{DBGDEVID}, \texttt{DBGDEVID1}, \texttt{DBGDEVID2}, \texttt{DBGOSECCR}.
- In AArch32 state, STC accesses to \texttt{DBGDTRRXint} and LDC accesses to \texttt{DBGDTRTXint} are reported using EC syndrome value \texttt{0x06}.
- When not in Debug state, the following registers are also trapped to EL3:
  - AArch64 accesses to \texttt{DBGDTR_E0}, \texttt{DBGDTRRX_E0}, and \texttt{DBGDTRTX_E0}, reported using EC syndrome value \texttt{0x18}.
  - AArch32 accesses using MCR or MRC to \texttt{DBGDTRRXint} and \texttt{DBGDTRTXint}, reported using EC syndrome value \texttt{0x05}. 

---

**Page 1129**
TDA | Meaning
--- | ---
0b0 | This control does not cause any instructions to be trapped.
0b1 | EL0, EL1, and EL2 accesses to the debug registers, other than the registers that can be trapped by MDCR_EL3.TDOSA, are trapped to EL3, from both Security states and both Execution states, unless it is trapped by DBGDSCR EXT, UDCCdis, MDSCR_EL1.TDCC, HDCR.TDA or MDCR_EL2.TDA.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [8:7]**

Reserved, RES0.

TPM, bit [6]

**When FEAT_PMUv3 is implemented:**

Trap Performance Monitor register accesses. Accesses to all Performance Monitor registers from EL0, EL1 and EL2 to EL3, from both Security states and both Execution states are trapped as follows:

- In AArch64 state, accesses to the following registers are trapped to EL3 and are reported using EC syndrome value 0x18:
  - PMCR_EL0, PMCNTENSET_EL0, PMCNTENCLR_EL0, PMOVSCLR_EL0, PMSWINC_EL0, PMSELR_EL0, PMCEID0_EL0, PMCEID1_EL0, PMCCNTR_EL0, PMXEVTYPE0_EL0, PMXEVCTR_EL0, PMUSERENR_EL0, PMINTENSET_EL1, PMINTENCLR_EL1, PMOVSSET_EL0, PMEVCTR<n>_EL0, PMEVTYPE<n>_EL0, EL0, PMCCFILTR_EL0.
  - If FEAT_PMUv3p4 is implemented, PMMIR_EL1.
- In AArch32 state, accesses using MCR or MRC to the following registers are reported using EC syndrome value 0x03, accesses using MCRR or MRRC are reported using EC syndrome value 0x04:
  - PMCR, PMCNTENSET, PMCNTENCLR, PMOVS, PMSWINC, PMSELR, PMCEID0, PMCEID1, PMCCNTR, PMXEVTYPE, PMXEVCTR, PMUSERENR, PMINTENSET, PMINTENCLR, PMOVSSET, PMFVCNTR<n>, PMFVTYPE<n>, PMCCFILTR.
  - If FEAT_PMUv3p1 is implemented, PMCEID2, and PMCEID3.
  - If FEAT_PMUv3p4 is implemented, PMMIR.

TPM | Meaning
--- | ---
0b0 | This control does not cause any instructions to be trapped.
0b1 | EL2, EL1, and EL0 System register accesses to all Performance Monitor registers are trapped to EL3, unless it is trapped by HDCR.TPM or MDCR_EL2.TPM.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bits [5:0]**

Reserved, RES0.

**Accessing the MDCR_EL3**

Accesses to this register use the following encodings:

MRS <Xt>, MDCR_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 1130
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return MDCR_EL3;

MSR MDCR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  MDCR_EL3 = X[t];
The MDRAR_EL1 characteristics are:

Purpose

Defines the base physical address of a 4KB-aligned memory-mapped debug component, usually a ROM table that locates and describes the memory-mapped debug components in the system. Armv8 deprecates any use of this register.

Configuration

AArch64 System register MDRAR_EL1 bits [63:0] are architecturally mapped to AArch32 System register DBGDRAR[63:0].

Attributes

MDRAR_EL1 is a 64-bit register.

Field descriptions

The MDRAR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ROMADDR |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:52]

Reserved, RES0.

ROMADDR, bits [51:12]

**ROMADDR encoding when FEAT_LPA is implemented**

| 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ROMADDR |

ROMADDR, bits [39:0]

The ROM table physical address.

Bits [11:0] of the ROM table physical address are defined to be zero.

In an implementation that includes EL3, ROMADDR is an address in Non-secure memory. It is IMPLEMENTATION DEFINED whether the ROM table is also accessible in Secure memory.

Arm strongly recommends that bits ROMADDR[(PAsize-1):32] are zero in any system that supports AArch32 at the highest implemented Exception level.

If MDRAR_EL1.Valid == 0b00, then this field is UNKNOWN.

The upper part of the address value.

If the physical address size in bits (PAsize) is less than 52, then the register bits corresponding to ROMADDR [39:PAsize] are RES0.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ROMADDR encoding when FEAT_LPA is not implemented or AArch32 is supported at any Exception level**

| 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | **ROMADDR** |

**Bits [39:36]**

Reserved, RES0.

**ROMADDR, bits [35:0]**

The ROM table physical address.

Bits [11:0] of the ROM table physical address are defined to be zero.

In an implementation that includes EL3, ROMADDR is an address in Non-secure memory. It is **IMPLEMENTATION DEFINED** whether the ROM table is also accessible in Secure memory.

Arm strongly recommends that bits ROMADDR[(PSize-1):32] are zero in any system that supports AArch32 at the highest implemented Exception level.

If MDRAR_EL1.Valid == 0b00, then this field is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [11:2]**

Reserved, RES0.

**Valid, bits [1:0]**

This field indicates whether the ROM Table address is valid.

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>ROM Table address is not valid. Software must ignore ROMADDR.</td>
</tr>
<tr>
<td>0b11</td>
<td>ROM Table address is valid.</td>
</tr>
</tbody>
</table>

Other values are reserved.

**Accessing the MDRAR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, MDRAR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDRA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      return MDRAR_EL1;
    end
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return MDRAR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return MDRAR_EL1;
else
  return MDRAR_EL1;
elsif PSTATE.EL == EL3 then
  return MDRAR_EL1;
return MDRAR_EL1;

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MDSCR_EL1, Monitor Debug System Control Register

The MDSCR_EL1 characteristics are:

**Purpose**

Main control register for the debug implementation.

**Configuration**

AArch64 System register MDSCR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGDSCRext[31:0].

**Attributes**

MDSCR_EL1 is a 64-bit register.

**Field descriptions**

The MDSCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>TFO</td>
</tr>
<tr>
<td>61</td>
<td>RXfull</td>
</tr>
<tr>
<td>60</td>
<td>TXfull</td>
</tr>
<tr>
<td>59</td>
<td>RES0</td>
</tr>
<tr>
<td>58</td>
<td>RXO</td>
</tr>
<tr>
<td>57</td>
<td>TXU</td>
</tr>
<tr>
<td>56</td>
<td>RXfull</td>
</tr>
<tr>
<td>55</td>
<td>TXU</td>
</tr>
<tr>
<td>54</td>
<td>RES0</td>
</tr>
<tr>
<td>53</td>
<td>RXfull</td>
</tr>
<tr>
<td>52</td>
<td>TXU</td>
</tr>
<tr>
<td>51</td>
<td>RES0</td>
</tr>
<tr>
<td>50</td>
<td>RXfull</td>
</tr>
<tr>
<td>49</td>
<td>TXU</td>
</tr>
<tr>
<td>48</td>
<td>RES0</td>
</tr>
<tr>
<td>47</td>
<td>RXfull</td>
</tr>
<tr>
<td>46</td>
<td>TXU</td>
</tr>
<tr>
<td>45</td>
<td>RES0</td>
</tr>
<tr>
<td>44</td>
<td>RXfull</td>
</tr>
<tr>
<td>43</td>
<td>TXU</td>
</tr>
<tr>
<td>42</td>
<td>RES0</td>
</tr>
<tr>
<td>41</td>
<td>RXfull</td>
</tr>
<tr>
<td>40</td>
<td>TXU</td>
</tr>
<tr>
<td>39</td>
<td>RES0</td>
</tr>
<tr>
<td>38</td>
<td>RXfull</td>
</tr>
<tr>
<td>37</td>
<td>TXU</td>
</tr>
<tr>
<td>36</td>
<td>RES0</td>
</tr>
<tr>
<td>35</td>
<td>RXfull</td>
</tr>
<tr>
<td>34</td>
<td>TXU</td>
</tr>
<tr>
<td>33</td>
<td>RES0</td>
</tr>
<tr>
<td>32</td>
<td>RXfull</td>
</tr>
<tr>
<td>31</td>
<td>RXfull</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

- Reserved, RES0.

**TFO, bit [31]**

When FEAT_TRF is implemented:

- Trace Filter override. Used for save/restore of EDSCR.TFO.
- When OSLSR_EL1.OSLK == 0, software must treat this bit as UNK/SBZP.
- When OSLSR_EL1.OSLK == 1, this bit holds the value of EDSCR.TFO. Reads and writes of this bit are indirect accesses to EDSCR.TFO.

Accessing this field has the following behavior:

- When OSLSR_EL1.OSLK == 1, access to this field is RW.
- When OSLSR_EL1.OSLK == 0, access to this field is RO.

**Otherwise:**

- Reserved, RES0.

**RXfull, bit [30]**

Used for save/restore of EDSCR.RXfull.

When OSLSR_EL1.OSLK == 0, software must treat this bit as UNK/SBZP.
When `OSLSR_EL1.OSLK == 1`, this bit holds the value of `EDSCR.RXfull`. Reads and writes of this bit are indirect accesses to `EDSCR.RXfull`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `OSLSR_EL1.OSLK == 1`, access to this field is **RW**.
- When `OSLSR_EL1.OSLK == 0`, access to this field is **RO**.

**TXfull, bit [29]**

Used for save/restore of `EDSCR.TXfull`.

When `OSLSR_EL1.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `OSLSR_EL1.OSLK == 1`, this bit holds the value of `EDSCR.TXfull`. Reads and writes of this bit are indirect accesses to `EDSCR.TXfull`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `OSLSR_EL1.OSLK == 1`, access to this field is **RW**.
- When `OSLSR_EL1.OSLK == 0`, access to this field is **RO**.

**Bit [28]**

Reserved, RES0.

**RXO, bit [27]**

Used for save/restore of `EDSCR.RXO`.

When `OSLSR_EL1.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `OSLSR_EL1.OSLK == 1`, this bit holds the value of `EDSCR.RXO`. Reads and writes of this bit are indirect accesses to `EDSCR.RXO`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `OSLSR_EL1.OSLK == 1`, access to this field is **RW**.
- When `OSLSR_EL1.OSLK == 0`, access to this field is **RO**.

**TXU, bit [26]**

Used for save/restore of `EDSCR.TXU`.

When `OSLSR_EL1.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `OSLSR_EL1.OSLK == 1`, this bit holds the value of `EDSCR.TXU`. Reads and writes of this bit are indirect accesses to `EDSCR.TXU`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `OSLSR_EL1.OSLK == 1`, access to this field is **RW**.
- When `OSLSR_EL1.OSLK == 0`, access to this field is **RO**.

**Bits [25:24]**

Reserved, RES0.
INTdis, bits [23:22]

Used for save/restore of \texttt{EDSCR}.INTdis.

When \texttt{OSLSR_EL1.OSLK} == 0, and software must treat this bit as UNK/SBZP.

When \texttt{OSLSR_EL1.OSLK} == 1, this field holds the value of \texttt{EDSCR}.INTdis. Reads and writes of this field are indirect accesses to \texttt{EDSCR}.INTdis.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When \texttt{OSLSR_EL1.OSLK} == 1, access to this field is \texttt{RW}.
- When \texttt{OSLSR_EL1.OSLK} == 0, access to this field is \texttt{RO}.

TDA, bit [21]

Used for save/restore of \texttt{EDSCR}.TDA.

When \texttt{OSLSR_EL1.OSLK} == 0, software must treat this bit as UNK/SBZP.

When \texttt{OSLSR_EL1.OSLK} == 1, this bit holds the value of \texttt{EDSCR}.TDA. Reads and writes of this bit are indirect accesses to \texttt{EDSCR}.TDA.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When \texttt{OSLSR_EL1.OSLK} == 1, access to this field is \texttt{RW}.
- When \texttt{OSLSR_EL1.OSLK} == 0, access to this field is \texttt{RO}.

Bit [20]

Reserved, \texttt{RES0}.

SC2, bit [19]

When \texttt{FEAT_PCSRv8} is implemented, \texttt{FEAT_VHE} is implemented and \texttt{FEAT_PCSRv8p2} is not implemented:

Used for save/restore of \texttt{EDSCR}.SC2.

When \texttt{OSLSR_EL1.OSLK} == 0, software must treat this bit as UNK/SBZP.

When \texttt{OSLSR_EL1.OSLK} == 1, this bit holds the value of \texttt{EDSCR}.SC2. Reads and writes of this bit are indirect accesses to \texttt{EDSCR}.SC2.

Accessing this field has the following behavior:

- When \texttt{OSLSR_EL1.OSLK} == 1, access to this field is \texttt{RW}.
- When \texttt{OSLSR_EL1.OSLK} == 0, access to this field is \texttt{RO}.

Otherwise:

Reserved, \texttt{RES0}.

Bits [18:16]

Reserved, \texttt{RAZ/WI}.

Hardware must implement this field as \texttt{RAZ/WI}. Software must not rely on the register reading as zero, and must use a read-modify-write sequence to write to the register.
MDE, bit [15]

Monitor debug events. Enable Breakpoint, Watchpoint, and Vector Catch exceptions.

<table>
<thead>
<tr>
<th>MDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Breakpoint, Watchpoint, and Vector Catch exceptions disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Breakpoint, Watchpoint, and Vector Catch exceptions enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

HDE, bit [14]

Used for save/restore of **EDSCR.HDE**.

When **OSLSR_EL1.OSLK == 0**, software must treat this bit as UNK/ SBZP.

When **OSLSR_EL1.OSLK == 1**, this bit holds the value of **EDSCR.HDE**. Reads and writes of this bit are indirect accesses to **EDSCR.HDE**.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When **OSLSR_EL1.OSLK == 1**, access to this field is **RW**.
- When **OSLSR_EL1.OSLK == 0**, access to this field is **RO**.

KDE, bit [13]

Local (kernel) debug enable. If **ELD** is using AArch64, enable debug exceptions within **ELD**. Permitted values are:

<table>
<thead>
<tr>
<th>KDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Debug exceptions, other than Breakpoint Instruction exceptions, enabled within <strong>ELD</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>All debug exceptions enabled within <strong>ELD</strong>.</td>
</tr>
</tbody>
</table>

RES0 if **ELD** is using AArch32.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

TDCC, bit [12]

Traps EL0 accesses to the Debug Communication Channel (DCC) registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and **HCR_EL2.TGE** is 1, from both Execution states, as follows:

- In AArch64 state, MRS or MSR accesses to the following DCC registers are trapped, reported using EC syndrome value 0x18:
  - MDCCSR_EL0.
  - If not in Debug state, DBGDTR_EL0, DBGDTRTX_EL0, and DBGDTRRX_EL0.
- In AArch32 state, MRC or MCR accesses to the following registers are trapped, reported using EC syndrome value 0x05:
  - DBGDSCRint, DBGDIDR, DBGDSAR, DBGDRAR.
  - If not in Debug state, DBGDTRRXint, and DBGDTRTXint.
- In AArch32 state, LDC access to DBGDTRRXint and STC access to DBGDTRTXint are trapped, reported using EC syndrome value 0x06.
- In AArch32 state, MRRC accesses to DBGDSAR and DBGDRAR are trapped, reported using EC syndrome value 0x0C.

<table>
<thead>
<tr>
<th>TDCC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 using AArch64: EL0 accesses to the AArch64 DCC registers are trapped.</td>
</tr>
<tr>
<td></td>
<td>EL0 using AArch32: EL0 accesses to the AArch32 DCC registers are trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [11:7]

Reserved, RES0.

ERR, bit [6]

Used for save/restore of EDSCR.ERR.

When OSLSR_EL1.OSLK == 0, software must treat this bit as UNK/SBZP.

When OSLSR_EL1.OSLK == 1, this bit holds the value of EDSCR.ERR. Reads and writes of this bit are indirect accesses to EDSCR.ERR.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When OSLSR_EL1.OSLK == 1, access to this field is RW.
- When OSLSR_EL1.OSLK == 0, access to this field is RO.

Bits [5:1]

Reserved, RES0.

SS, bit [0]

Software step control bit. If EL1 is using AArch64, enable Software step. Permitted values are:

<table>
<thead>
<tr>
<th>SS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Software step disabled</td>
</tr>
<tr>
<td>0b1</td>
<td>Software step enabled.</td>
</tr>
</tbody>
</table>

RES0 if EL1 is using AArch32.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the MDSCR_EL1**

Individual fields within this register might have restricted accessibility when OSLSR_EL1.OSLK == 0 (the OS lock is unlocked). See the field descriptions for more detail.

Accesses to this register use the following encodings:

\[
MRS \langle Xt\rangle, \text{MDSCR_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.MDSCR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && HDFGRTR_EL2.MDSCR_EL1 == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  return MDSCR_EL1;
endif
elsif PSTATE.EL == EL3 then
  return MDSCR_EL1;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.MDSCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        NVMem[0x158] = X[t];
    else
        MDSCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MDSCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    MDSCR_EL1 = X[t];
The MIDR_EL1 characteristics are:

**Purpose**

Provides identification information for the PE, including an implementer code for the device and a device ID number.

**Configuration**

AArch64 System register MIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register `.MIDR[31:0]`. AArch64 System register MIDR_EL1 bits [31:0] are architecturally mapped to External register `.MIDR_EL1[31:0]`.

**Attributes**

MIDR_EL1 is a 64-bit register.

**Field descriptions**

The MIDR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Implementer | Variant | Architecture | PartNum | Revision |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, `RES0`.

**Implementer, bits [31:24]**

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Implementer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Reserved for software use</td>
</tr>
<tr>
<td>0xC0</td>
<td>Ampere Computing</td>
</tr>
<tr>
<td>0x41</td>
<td>Arm Limited</td>
</tr>
<tr>
<td>0x42</td>
<td>Broadcom Corporation</td>
</tr>
<tr>
<td>0x43</td>
<td>Cavium Inc.</td>
</tr>
<tr>
<td>0x44</td>
<td>Digital Equipment Corporation</td>
</tr>
<tr>
<td>0x46</td>
<td>Fujitsu Ltd.</td>
</tr>
<tr>
<td>0x49</td>
<td>Infineon Technologies AG</td>
</tr>
<tr>
<td>0x4D</td>
<td>Motorola or Freescale Semiconductor Inc.</td>
</tr>
<tr>
<td>0x4E</td>
<td>NVIDIA Corporation</td>
</tr>
<tr>
<td>0x50</td>
<td>Applied Micro Circuits Corporation</td>
</tr>
<tr>
<td>0x51</td>
<td>Qualcomm Inc.</td>
</tr>
<tr>
<td>0x56</td>
<td>Marvell International Ltd.</td>
</tr>
<tr>
<td>0x69</td>
<td>Intel Corporation</td>
</tr>
</tbody>
</table>

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.
**Variant, bits [23:20]**

An implementation defined variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product.

**Architecture, bits [19:16]**

Architecture version. For A-profile, the defined values are:

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv4.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv4T.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv5 (obsolete).</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv5T.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv5TE.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv5TEJ.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv6.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Architectural features are individually identified in the ID * registers, see 'ID registers'.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**PartNum, bits [15:4]**

An implementation defined primary part number for the device.

On processors implemented by Arm, if the top four bits of the primary part number are 0x0 or 0x7, the variant and architecture are encoded differently.

**Revision, bits [3:0]**

An implementation defined revision number for the device.

**Accessing the MIDR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, MIDR_EL1**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

```c
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
    else
        UNDEFINED;
else if PSTATE.EL == EL1 then
    if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.MIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return VPIDR_EL2;
    else
        return MIDR_EL1;
else if PSTATE.EL == EL2 then
    return MIDR_EL1;
else if PSTATE.EL == EL3 then
    return MIDR_EL1;
else
    return MIDR_EL1;
```
MPAM0_EL1, MPAM0 Register (EL1)

The MPAM0_EL1 characteristics are:

**Purpose**

Holds information to generate MPAM labels for memory requests when executing at EL0. When EL2 is present and enabled, the MPAM virtualization option is present, MPAMHCR_EL2.GSTAPP_PLK == 1 and HCR_EL2.TGE == 0, MPAM1_EL1 is used instead of MPAM0_EL1 to generate MPAM information to label memory requests.

If EL2 is present and enabled, and HCR_EL2.E2H == 0 or HCR_EL2.TGE == 0, the MPAM virtualization option is present and MPAMHCR_EL2.EL0_VPMEN == 1, then MPAM PARTIDs in MPAM0_EL1 are virtual and mapped into physical PARTIDs for the current Security state.

**Configuration**

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAM0_EL1 are UNDEFINED.

**Attributes**

MPAM0_EL1 is a 64-bit register.

**Field descriptions**

The MPAM0_EL1 bit assignments are:

| Bits [63:48] | Reserved, RES0. |
| PMG_D, bits [47:40] | Performance monitoring group property for PARTID_D. On a Warm reset, this field resets to an architecturally UNKNOWN value. |
| PMG_I, bits [39:32] | Performance monitoring group property for PARTID_I. On a Warm reset, this field resets to an architecturally UNKNOWN value. |
| PARTID_D, bits [31:16] | Partition ID for data accesses, including load and store accesses, made from EL0. On a Warm reset, this field resets to an architecturally UNKNOWN value. |
| PARTID_I, bits [15:0] | Partition ID for instruction accesses made from EL0. |
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the MPAM0_EL1

None of the fields in this register are permitted to be cached in a TLB.

Accesses to this register use the following encodings:

**MRS <Xt>, MPAM0_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif EL2Enabled() && MPAM2_EL2.TRAPMPAM0EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return MPAM0_EL1;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  else
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return MPAM0_EL1;
elsif PSTATE.EL == EL3 then
  return MPAM0_EL1;
```

**MSR MPAM0_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif EL2Enabled() && MPAM2_EL2.TRAPMPAM0EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    MPAM0_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  else
    MPAM0_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  MPAM0_EL1 = X[t];
```
MPAM1_EL1, MPAM1 Register (EL1)

The MPAM1_EL1 characteristics are:

**Purpose**

Holds information to generate MPAM labels for memory requests when executing at EL1.

When EL2 is present and enabled, the MPAM virtualization option is present, MPAMHCR_EL2.GSTAPP_PLK == 1 and HCR_EL2.TGE == 0, MPAM1_EL1 is used instead of MPAM0_EL1 to generate MPAM labels for memory requests when executing at EL0.

MPAM1_EL1 is an alias for MPAM2_EL2 when executing at EL2 with HCR_EL2.E2H == 1.

MPAM1_EL12 is an alias for MPAM1_EL1 when executing at EL2 or EL3 with HCR_EL2.E2H == 1.

If EL2 is present and enabled, the MPAM virtualization option is present and MPAMHCR_EL2.EL1_VPMEN == 1, MPAM PARTIDs in MPAM1_EL1 are virtual and mapped into physical PARTIDs for the current Security state. This mapping of MPAM1_EL1 virtual PARTIDs to physical PARTIDs when EL1_VPMEN is 1 also applies when MPAM1_EL1 is used at EL0 due to MPAMHCR_EL2.GSTAPP_PLK.

**Configuration**

AArch64 System register MPAM1_EL1 bit [63] is architecturally mapped to AArch64 System register MPAM3_EL3[63] when EL3 is implemented.

AArch64 System register MPAM1_EL1 bit [63] is architecturally mapped to AArch64 System register MPAM2_EL2[63] when EL3 is not implemented and EL2 is implemented.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAM1_EL1 are UNDEFINED.

**Attributes**

MPAM1_EL1 is a 64-bit register.

**Field descriptions**

The MPAM1_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
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<th>45</th>
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<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAMEN</td>
<td>RES0</td>
<td>FORCED_NS</td>
<td>RES0</td>
<td>PMG_D</td>
<td>PMG_I</td>
<td></td>
<td></td>
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<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**MPAMEN, bit [63]**

MPAM Enable. MPAM is enabled when MPAMEN == 1. When disabled, all PARTIDs and PMGs are output as their default value in the corresponding ID space.

<table>
<thead>
<tr>
<th>MPAMEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The default PARTID and default PMG are output in MPAM information.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM information is output based on the MPAMn_ELx register for ELn according the MPAM configuration.</td>
</tr>
</tbody>
</table>

If neither EL3 nor EL2 is implemented, this field is read/write.

If EL3 is implemented, this field is read-only and reads the current value of the read/write bit MPAM3_EL3.MPAMEN.
If EL3 is not implemented and EL2 is implemented, this field is read-only and reads the current value of the read/write bit MPAM2_EL2.MPAMEN.

On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- When EL3 is not implemented and EL2 is not implemented, access to this field is RW.
- Otherwise, access to this field is RO.

### Bits [62:61]

Reserved, RES0.

### FORCED_NS, bit [60]

When FEAT_MPAMv0p1 is implemented:

In the Secure state, FORCED_NS indicates the state of MPAM3_EL3.FORCE_NS.

<table>
<thead>
<tr>
<th>FORCED_NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>In the Non-secure state, always reads as 0. In the Secure state, indicates that MPAM3_EL3.FORCE_NS == 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>In the Secure state, indicates that MPAM3_EL3.FORCE_NS == 1.</td>
</tr>
</tbody>
</table>

Always reads as 0 in the Non-secure state.

Writes are ignored.

Access to this field is RO.

### Otherwise:

Reserved, RES0.

### Bits [59:48]

Reserved, RES0.

### PMG_D, bits [47:40]

Performance monitoring group property for PARTID_D.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### PMG_I, bits [39:32]

Performance monitoring group property for PARTID_I.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### PARTID_D, bits [31:16]

Partition ID for data accesses, including load and store accesses, made from EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### PARTID_I, bits [15:0]

Partition ID for instruction accesses made from EL1.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the MPAM1_EL1

When `HCR_EL2.E2H` is 1, without explicit synchronization, accesses from EL3 using the mnemonic MPAM1_EL1 or MPAM1_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

None of the fields in this register are permitted to be cached in a TLB.

Accesses to this register use the following encodings:

**MRS `<Xt>`, MPAM1_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif EL2Enabled() && MPAM2_EL2.TRAPMPAM1EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x900];
  else
    return MPAM1_EL1;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  elsif HCR_EL2.E2H == '1' then
    return MPAM2_EL2;
  else
    return MPAM1_EL1;
elsif PSTATE.EL == EL3 then
  return MPAM1_EL1;
```

**MSR MPAM1_EL1, `<Xt>`**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) & MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif EL2Enabled() & MPAM2_EL2.TRAPMPAM1EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x900] = X[t];
    else
    MPAM1_EL1 = X[t];
endif;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) & MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HCR_EL2.E2H == '1' then
    MPAM2_EL2 = X[t];
    else
    MPAM1_EL1 = X[t];
endif;
elsif PSTATE.EL == EL3 then
    MPAM1_EL1 = X[t];
endif;

MRS <Xt>, MPAM1_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x900];
    elsif EL2Enabled() & HCR_EL2.NV == '1' then
    if HaveEL(EL3) & MPAM3_EL3.TRAPLOWER == '1' then
    AArch64.SystemAccessTrap(EL3, 0x18);
    else
    AArch64.SystemAccessTrap(EL2, 0x18);
    else
    UNDEFINED;
endif;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
    if HaveEL(EL3) & MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
    return MPAM1_EL1;
    else
    return MPAM1_EL1;
endif;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.E2H == '1' then
    return MPAM1_EL1;
    else
    UNDEFINED;
endif;
else
    UNDEFINED;
endif;

MSR MPAM1_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x900] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
    else
      MPAM1_EL1 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    MPAM1_EL1 = X[t];
  else
    UNDEFINED;
MPAM2_EL2, MPAM2 Register (EL2)

The MPAM2_EL2 characteristics are:

**Purpose**

Holds information to generate MPAM labels for memory requests when executing at EL2.

**Configuration**

AArch64 System register MPAM2_EL2 bit [63] is architecturally mapped to AArch64 System register MPAM3_EL3[63] when EL3 is implemented.

AArch64 System register MPAM2_EL2 bit [63] is architecturally mapped to AArch64 System register MPAM1_EL1[63].

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAM2_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAM2_EL2 is a 64-bit register.

**Field descriptions**

The MPAM2_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
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<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAMEN</td>
<td>RES0</td>
<td>TIDR</td>
<td>RES0</td>
<td>TRAPMPAM0EL1</td>
<td>TRAPMPAM1EL1</td>
<td>PMG_D</td>
<td>PMG_I</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30292827</td>
<td>26</td>
<td>2524232221201918</td>
<td>17</td>
<td>16</td>
<td>151413121110</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**MPAMEN, bit [63]**

MPAM Enable. MPAM is enabled when MPAMEN == 1. When disabled, all PARTIDs and PMGs are output as their default value in the corresponding ID space.

<table>
<thead>
<tr>
<th>MPAMEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The default PARTID and default PMG are output in MPAM information from all Exception levels.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM information is output based on the MPAMn_ELx register for ELn according the MPAM configuration.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented, this field is read/write.

If EL3 is implemented, this field is read-only and reads the current value of the read/write MPAM3_EL3.MPAMEN bit.

On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- When EL3 is not implemented, access to this field is RW.
- Otherwise, access to this field is RO.

**Bits [62:59]**

Reserved, RES0.
**TIDR, bit [58]**

When (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented) and MPAMIDR_EL1.HAS_TIDR == 1:

TIDR traps accesses to MPAMIDR_EL1 from EL1 to EL2.

<table>
<thead>
<tr>
<th>TIDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trap accesses to MPAMIDR_EL1 from EL1 to EL2.</td>
</tr>
</tbody>
</table>

MPAMHCR_EL2.TRAP_MPAMIDR_EL1 == 1 also traps MPAMIDR_EL1 accesses from EL1 to EL2. If either TIDR or TRAP_MPAMIDR_EL1 are 1, accesses are trapped.

Otherwise:

Reserved, RES0.

**Bits [57:50]**

Reserved, RES0.

**TRAPMPAM0EL1, bit [49]**

TRAPMPAM0EL1: Trap accesses from EL1 to the MPAM0_EL1 register trap to EL2.

<table>
<thead>
<tr>
<th>TRAPMPAM0EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to MPAM0_EL1 from EL1 are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to MPAM0_EL1 from EL1 are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, when EL3 is not implemented, this field resets to 1.

On a Warm reset, when EL3 is implemented, this field resets to an architecturally UNKNOWN value.

**TRAPMPAM1EL1, bit [48]**

TRAPMPAM1EL1: Trap accesses from EL1 to the MPAM1_EL1 register trap to EL2.

<table>
<thead>
<tr>
<th>TRAPMPAM1EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to MPAM1_EL1 from EL1 are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to MPAM1_EL1 from EL1 are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, when EL3 is not implemented, this field resets to 1.

On a Warm reset, when EL3 is implemented, this field resets to an architecturally UNKNOWN value.

**PMG_D, bits [47:40]**

Performance monitoring group for data accesses.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PMG_I, bits [39:32]**

Performance monitoring group for instruction accesses.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PARTID_D, bits [31:16]**

Partition ID for data accesses, including load and store accesses, made from EL2.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PARTID_I, bits [15:0]**

Partition ID for instruction accesses made from EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the MPAM2_EL2

None of the fields in this register are permitted to be cached in a TLB.

Accesses to this register use the following encodings:

**MRS <Xt>, MPAM2_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAM2_EL2;
    end
elsif PSTATE.EL == EL3 then
    return MPAM2_EL2;
end
```

**MSR MPAM2_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if;
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end if;
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HCR_EL2.E2H == '1' then
        return MPAM2_EL2;
    else
        return MPAM1_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return MPAM1_EL1;
MSR <Xt>, MPAM1_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end if;
    elsif EL2Enabled() && MPAM2_EL2.TRAPMPAM1EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x900];
    else
        return MPAM1_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HCR_EL2.E2H == '1' then
        return MPAM2_EL2;
    else
        return MPAM1_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return MPAM1_EL1;
MSR MPAM1_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  elsif EL2Enabled() && MPAM2_EL2.TRAPMPAM1EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x900] = X[t];
  else
    MPAM1_EL1 = X[t];
  end;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  elsif HCR_EL2.E2H == '1' then
    MPAM2_EL2 = X[t];
  else
    MPAM1_EL1 = X[t];
  end;
elsif PSTATE.EL == EL3 then
  MPAM1_EL1 = X[t];

MPAM3_EL3, MPAM3 Register (EL3)

The MPAM3_EL3 characteristics are:

**Purpose**

Holds information to generate MPAM labels for memory requests when executing at EL3.

**Configuration**

AArch64 System register MPAM3_EL3 bit [63] is architecturally mapped to AArch64 System register MPAM2_EL2[63] when EL2 is implemented.

AArch64 System register MPAM3_EL3 bit [63] is architecturally mapped to AArch64 System register MPAM1_EL1[63].

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAM3_EL3 are UNDEFINED.

**Attributes**

MPAM3_EL3 is a 64-bit register.

**Field descriptions**

The MPAM3_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MPAMEN | TRAPLOWER | SDEFLT | FORCE_NS | RES0 | PMG_D | PMG_I | PARTID_D | PARTID_I |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**MPAMEN, bit [63]**

MPAM Enable. MPAM is enabled when MPAMEN == 1. When disabled, all PARTIDs and PMGs are output as their default value in the corresponding ID space.

Values of this field are:

<table>
<thead>
<tr>
<th>MPAMEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The default PARTID and default PMG are output in MPAM information when executing at any ELn.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM information is output based on the MPAMn_ELx register for ELn according the MPAM configuration.</td>
</tr>
</tbody>
</table>

This field is always read/write in MPAM3_EL3.

On a Warm reset, this field resets to 0.

**TRAPLOWER, bit [62]**

Trap direct accesses to any MPAM system registers that are not UNDEFINED from all ELn lower than EL3.

<table>
<thead>
<tr>
<th>TRAPLOWER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not force trapping of direct accesses of MPAM system registers to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>Force all direct accesses of MPAM system registers to trap to EL3.</td>
</tr>
</tbody>
</table>
On a Cold reset, this field resets to 1.

**SDEFLT, bit [61]**

When (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented) and MPAMIDR_EL1.HAS_SDEFLT == 1:

SDEFLT overrides the PARTID with the default PARTID when executing in the Secure state.

<table>
<thead>
<tr>
<th>SDEFLT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>The PARTID is determined normally in the Secure state.</td>
</tr>
<tr>
<td>01</td>
<td>The PARTID is always PARTID 0 when executing in the Secure state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**FORCE_NS, bit [60]**

When FEAT_MPAMv0p1 is implemented and MPAMIDR_EL1.HAS_FORCE_NS == 1:

FORCE_NS forces MPAM_NS to always be 1 in the Secure state.

<table>
<thead>
<tr>
<th>FORCE_NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>MPAM_NS is 0 when executing in the Secure state.</td>
</tr>
<tr>
<td>01</td>
<td>MPAM_NS is 1 when executing in the Secure state.</td>
</tr>
</tbody>
</table>

An implementation is permitted to have this field as RAO if the implementation does not support generating MPAM_NS as 0.

On a Warm reset, this field resets to an **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bits [59:48]**

Reserved, RES0.

**PMG_D, bits [47:40]**

Performance monitoring group for data accesses.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PMG_I, bits [39:32]**

Performance monitoring group for instruction accesses.

**PARTID_D, bits [31:16]**

Partition ID for data accesses, including load and store accesses, made from EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PARTID_I, bits [15:0]**

Partition ID for instruction accesses made from EL3.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAM3_EL3**

None of the fields in this register are permitted to be cached in a TLB.

Accesses to this register use the following encodings:

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return MPAM3_EL3;
```
The MPAMHCR_EL2 characteristics are:

**Purpose**

Controls the PARTID virtualization features of MPAM. It controls the mapping of virtual PARTIDs into physical PARTIDs in MPAM0_EL1 when EL0_VPMEN == 1 and in MPAM1_EL1 when EL1_VPMEN == 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented and MPAMIDR_EL1.HAS_HCR == 1. Otherwise, direct accesses to MPAMHCR_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMHCR_EL2 is a 64-bit register.

**Field descriptions**

The MPAMHCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>TRAP_MPAMIDR_EL1, bit [31]</td>
</tr>
<tr>
<td>30-9</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>GSTAPP_PLK, bit [8]</td>
</tr>
<tr>
<td>7</td>
<td>EL1_VPMEN, bit [7]</td>
</tr>
<tr>
<td>6</td>
<td>EL0_VPMEN, bit [6]</td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**TRAP_MPAMIDR_EL1, bit [31]**

Trap accesses from EL1 to MPAMIDR_EL1 to EL2.

<table>
<thead>
<tr>
<th>TRAP_MPAMIDR_EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Direct accesses to MPAMIDR_EL1 from EL1 are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, when EL3 is not implemented, this field resets to 1.

On a Warm reset, when EL3 is implemented, this field resets to an architecturally UNKNOWN value.

**Bits [30:9]**

Reserved, RES0.

**GSTAPP_PLK, bit [8]**

Make the PARTIDs at EL0 the same as the PARTIDs at EL1. When executing at EL0, EL2 is enabled, HCR_EL2.TGE == 0 and GSTAPP_PLK = 1, MPAM1_EL1 is used instead of MPAM0_EL1 to generate MPAM labels for memory requests.
Meaning

<table>
<thead>
<tr>
<th>GSTAPP_PLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAM0_EL1</strong> is used to generate MPAM labels when executing at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAM0_EL1</strong> is used to generate MPAM labels when executing at EL0 with EL2 enabled and HCR_EL2.TGE == 0. Otherwise <strong>MPAM0_EL1</strong> is used.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [7:2]**

Reserved, RES0.

**EL1_VPMEN, bit [1]**

Enable the virtual PARTID mapping of the PARTID fields in MPAM1_EL1 when executing at EL1. This bit also enables virtual PARTID mapping when **MPAM1_EL1** is used to generate MPAM labels for memory requests at EL0 due to GSTAPP_PLK == 1.

<table>
<thead>
<tr>
<th>EL1_VPMEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAM1_EL1</strong>.PARTID_I and <strong>MPAM1_EL1</strong>.PARTID_D are physical PARTIDs that are used to label memory system requests.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAM1_EL1</strong>.PARTID_I and <strong>MPAM1_EL1</strong>.PARTID_D are virtual PARTIDs that are used to index the PhyPARTID fields of <strong>MPAMVPM0_EL2</strong> to <strong>MPAMVPM7_EL2</strong> registers to map the virtual PARTID into a physical PARTID to label memory system requests.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EL0_VPMEN, bit [0]**

Enable the virtual PARTID mapping of the PARTID fields of **MPAM0_EL1** unless HCR_EL2.E2H == 1 and HCR_EL2.TGE == 1.

When HCR_EL2.E2H == 1 and HCR_EL2.TGE == 1, EL0_VPMEN is ignored and MPAM0_EL1 PARTID fields are not mapped.

When **MPAMHCR_EL2**.GSTAPP_PLK == 1 and HCR_EL2.TGE == 0, **MPAM1_EL1** is used as the source of PARTIDs and the virtual PARTID mapping of **MPAM1_EL1** PARTIDs is controlled by **MPAMHCR_EL2**.EL1_VPMEN.

<table>
<thead>
<tr>
<th>EL0_VPMEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAM0_EL1</strong>.PARTID_I and <strong>MPAM0_EL1</strong>.PARTID_D are physical PARTIDs that are used to label memory system requests.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAM0_EL1</strong>.PARTID_I and <strong>MPAM0_EL1</strong>.PARTID_D are virtual PARTIDs that are used to index the PhyPARTID fields of <strong>MPAMVPM0_EL2</strong> to <strong>MPAMVPM7_EL2</strong> registers to map the virtual PARTID into a physical PARTID to label memory system requests.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMHCR_EL2**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>MRS &lt;Xt&gt;, MPAMHCR_EL2</th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
</tr>
<tr>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x930];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
      else
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        return MPAMHCR_EL2;
  elsif PSTATE.EL == EL3 then
    return MPAMHCR_EL2;

MSR MPAMHCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x930] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        MPAMHCR_EL2 = X[t];
  elsif PSTATE.EL == EL3 then
    MPAMHCR_EL2 = X[t];
MPAMIDR_EL1, MPAM ID Register (EL1)

The MPAMIDR_EL1 characteristics are:

**Purpose**

Indicates the presence and maximum PARTID and PMG values supported in the implementation. It also indicates whether the implementation supports MPAM virtualization.

**Configuration**

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMIDR_EL1 are UNDEFINED.

**Attributes**

MPAMIDR_EL1 is a 64-bit register.

**Field descriptions**

The MPAMIDR_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| HAS_SDEFLT| HAS_FORCE_NS| RES0| HAS_TIDR| RES0| VPMR_MAX| RES0| HAS_HCR| RES0| PMG_MAX| RES0| PARTID_MAX|
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   |

MPAMIDR_EL1 indicates the MPAM implementation parameters of the PE.

**Bits [63:62]**

Reserved, RES0.

**HAS_SDEFLT, bit [61]**

HAS_SDEFLT indicates support for MPAM3_EL3.SDEFLT bit. Defined values are:

<table>
<thead>
<tr>
<th>HAS_SDEFLT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The SDEFLT bit is not implemented in MPAM3_EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>The SDEFLT bit is implemented in MPAM3_EL3.</td>
</tr>
</tbody>
</table>

When MPAM3_EL3.SDEFLT == 1, accesses from the Secure execution state use the default PARTID, PARTID == 0.

**HAS_FORCE_NS, bit [60]**

HAS_FORCE_NS indicates support for MPAM3_EL3.FORCE_NS bit. Defined values are:

<table>
<thead>
<tr>
<th>HAS_FORCE_NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The FORCE_NS bit is not implemented in MPAM3_EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>The FORCE_NS bit is implemented in MPAM3_EL3.</td>
</tr>
</tbody>
</table>

When MPAM3_EL3.FORCE_NS == 1, accesses from the Secure execution state have MPAM_NS == 1.

**Bit [59]**

Reserved, RES0.
HAS_TIDR, bit [58]

HAS_TIDR indicates support for MPAM2_EL2.TIDR bit. Defined values are:

<table>
<thead>
<tr>
<th>HAS_TIDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The TIDR bit is not implemented in MPAM2_EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>The TIDR bit is implemented in MPAM2_EL2.</td>
</tr>
</tbody>
</table>

Bits [57:40]

Reserved, RES0.

PMG_MAX, bits [39:32]

The largest value of PMG that the implementation can generate. The PMG_I and PMG_D fields of every MPAMn_ELx must implement at least enough bits to represent PMG_MAX.

Bits [31:21]

Reserved, RES0.

VPMR_MAX, bits [20:18]

When MPAMIDR_EL1.HAS_HCR == 1:

Indicates the maximum register index n for the MPAMVPM<n>_EL2 registers.

Otherwise:

Reserved, RAZ.

HAS_HCR, bit [17]

HAS_HCR indicates that the PE implementation supports MPAM virtualization, including MPAMHCR_EL2, MPAMVPMV_EL2 and MPAMVPM<n>_EL2 with n in the range 0 to VPMR_MAX. Must be 0 if EL2 is not implemented in either security state.

<table>
<thead>
<tr>
<th>HAS_HCR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAM virtualization is not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM virtualization is supported.</td>
</tr>
</tbody>
</table>

Bit [16]

Reserved, RES0.

PARTID_MAX, bits [15:0]

The largest value of PARTID that the implementation can generate. The PARTID_I and PARTID_D fields of every MPAMn_ELx must implement at least enough bits to represent PARTID_MAX.

Accessing the MPAMIDR_EL1

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    elseif EL2Enabled() && MPAMIDR_EL1.HAS_HCR == '1' && MPAMHCR_EL2.TRAP_MPAMIDR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && MPAMIDR_EL1.HAS_TIDR == '1' && MPAM2_EL2.TIDR == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return MPAMIDR_EL1;
    endif
elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return MPAMIDR_EL1;
    endif
elsif PSTATE_EL == EL3 then
    return MPAMIDR_EL1;
end if
MPAMVPM0_EL2, MPAM Virtual PARTID Mapping Register 0

The MPAMVPM0_EL2 characteristics are:

**Purpose**

MPAMVPM0_EL2 provides mappings from virtual PARTIDs 0 - 3 to physical PARTIDs.

- **MPAMIDR_EL1.VPMR_MAX** field gives the index of the highest implemented MPAMVPM<n>_EL2 register. VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If **MPAMIDR_EL1.VPMR_MAX** == 0, there is only a single MPAMVPM<n>_EL2 register, **MPAMVPM0_EL2**.

- Virtual PARTID mapping is enabled by **MPAMHCR_EL2.EL1_VPMEN** for PARTIDs in **MPAM1_EL1** and by **MPAMHCR_EL2.EL0_VPMEN** for PARTIDs in **MPAM0_EL1**.

- A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the **MPAMVPMV_EL2.VPM_V** bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented and MPAMIDR_EL1.HAS_HCR == 1. Otherwise, direct accesses to MPAMVPM0_EL2 are **UNDEFINED**.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM0_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM0_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 - 48</td>
<td>PhyPARTID3</td>
<td>Virtual PARTID Mapping Entry for virtual PARTID 3. PhyPARTID3 gives the mapping of virtual PARTID 3 to a physical PARTID. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>47 - 32</td>
<td>PhyPARTID2</td>
<td>Virtual PARTID Mapping Entry for virtual PARTID 2. PhyPARTID2 gives the mapping of virtual PARTID 2 to a physical PARTID. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>31 - 16</td>
<td>PhyPARTID1</td>
<td>Virtual PARTID Mapping Entry for virtual PARTID 1. PhyPARTID1 gives the mapping of virtual PARTID 1 to a physical PARTID.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID0, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 0. PhyPARTID0 gives the mapping of virtual PARTID 0 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the MPAMVPM0_EL2

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, MPAMVPM0_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x940];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    end
  else
    AArch64.SystemAccessTrap(EL2, 0x18);
  end
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  end
else
  return MPAMVPM0_EL2;
elsif PSTATE.EL == EL3 then
  return MPAMVPM0_EL2;
```

```plaintext
MSR MPAMVPM0_EL2, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x940] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      AArch64.SystemAccessTrap(EL2, 0x18);
    end if
  else
    UNDEFINED;
  end if
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    MPAMVPM0_EL2 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  MPAMVPM0_EL2 = X[t];
The MPAMVPM1_EL2 characteristics are:

### Purpose

MPAMVPM1_EL2 provides mappings from virtual PARTIDs 4 - 7 to physical PARTIDs.

**MPAMIDR_EL1**.VPMR_MAX field gives the index of the highest implemented MPAMVPM0_EL2 to MPAMVPM7_EL2 registers. VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If **MPAMIDR_EL1**.VPMR_MAX == 0, there is only a single MPAMVPM<n>_EL2 register, MPAMVPM0_EL2.

Virtual PARTID mapping is enabled by **MPAMHCR_EL2.EL1_VPMEN** for PARTIDs in MPAM1_EL1 and by **MPAMHCR_EL2.EL0_VPMEN** for PARTIDs in MPAM0_EL1.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the MPAMVPMV_EL2.VPM_V bit in bit position n is set to 1.

### Configuration

This register is present only when FEAT_MPAM is implemented, **MPAMIDR_EL1**.HAS_HCR == 1 and **MPAMIDR_EL1**.VPMR_MAX > 0. Otherwise, direct accesses to MPAMVPM1_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

### Attributes

MPAMVPM1_EL2 is a 64-bit register.

### Field descriptions

The MPAMVPM1_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| PhyPARTID7 | PhyPARTID5 | PhyPARTID6 | PhyPARTID4 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**PhyPARTID7**, bits [63:48]

Virtual PARTID Mapping Entry for virtual PARTID 7. PhyPARTID7 gives the mapping of virtual PARTID 7 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PhyPARTID6**, bits [47:32]

Virtual PARTID Mapping Entry for virtual PARTID 6. PhyPARTID6 gives the mapping of virtual PARTID 6 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PhyPARTID5**, bits [31:16]

Virtual PARTID Mapping Entry for virtual PARTID 5. PhyPARTID5 gives the mapping of virtual PARTID 5 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID4, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 4. PhyPARTID4 gives the mapping of virtual PARTID 4 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM1_EL2**

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, MPAMVPM1_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x948];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if;
        else
            return MPAMVPM1_EL2;  
        end if;
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end if;
else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return MPAMVPM1_EL2;
    end if;
elsif PSTATE.EL == EL3 then
    return MPAMVPM1_EL2;
```

**MSR MPAMVPM1_EL2, <Xt>**

```plaintext
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsf PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x948] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        elsif EL2Enabled() && HCR_EL2.NV == '1' then
            if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.SystemAccessTrap(EL3, 0x18);
                end
            else
                UNDEFINED;
            end
        else
            if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.SystemAccessTrap(EL3, 0x18);
                end
            else
                MPAMVPM1_EL2 = X[t];
            end
        end
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            MPAMVPM1_EL2 = X[t];
        end
    elsif PSTATE.EL == EL3 then
        MPAMVPM1_EL2 = X[t];
MPAMVPM2_EL2, MPAM Virtual PARTID Mapping Register 2

The MPAMVPM2_EL2 characteristics are:

**Purpose**

MPAMVPM2_EL2 provides mappings from virtual PARTIDs 8 - 11 to physical PARTIDs.

**MPAMIDR_EL1**.VPMR_MAX field gives the index of the highest implemented MPAMVPM0_EL2 to MPAMVPM7_EL2 registers. VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If MPAMIDR_EL1.VPMR_MAX == 0, there is only a single MPAMVPM<n>_EL2 register, MPAMVPM0_EL2.

Virtual PARTID mapping is enabled by MPAMHCR_EL2.EL1.VPMEN for PARTIDs in MPAM1_EL1 and by MPAMHCR_EL2.EL0.VPMEN for PARTIDs in MPAM0_EL1.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the MPAMVPMV_EL2.VPM_V bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented, MPAMIDR_EL1.HAS_HCR == 1 and MPAMIDR_EL1.VPMR_MAX > 1. Otherwise, direct accesses to MPAMVPM2_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM2_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM2_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>53</th>
<th>52</th>
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<th>48</th>
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<th>43</th>
<th>42</th>
<th>41</th>
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<th>39</th>
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<tbody>
<tr>
<td>PhyPARTID11</td>
<td>PhyPARTID10</td>
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<tr>
<td>PhyPARTID9</td>
<td>PhyPARTID8</td>
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</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**PhyPARTID11, bits [63:48]**

Virtual PARTID Mapping Entry for virtual PARTID 11. PhyPARTID11 gives the mapping of virtual PARTID 11 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PhyPARTID10, bits [47:32]**

Virtual PARTID Mapping Entry for virtual PARTID 10. PhyPARTID10 gives the mapping of virtual PARTID 10 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PhyPARTID9, bits [31:16]**

Virtual PARTID Mapping Entry for virtual PARTID 9. PhyPARTID9 gives the mapping of virtual PARTID 9 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID8, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 8. PhyPARTID8 gives the mapping of virtual PARTID 8 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM2_EL2**

Accesses to this register use the following encodings:

```c
MRS <Xt>, MPAMVPM2_EL2
```

<table>
<thead>
<tr>
<th>$op0$</th>
<th>$op1$</th>
<th>$CRn$</th>
<th>$CRm$</th>
<th>$op2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```c
if PSTATE_EL == EL0 then
    UNDEFINED;
elif PSTATE_EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x950];
elif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elif HaveEL(EL3) then
            if MPAM3_EL3.TRAPLOWER == '1' then
                UNDEFINED;
elif PSTATE_EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elif HaveEL(EL3) then
            if MPAM3_EL3.TRAPLOWER == '1' then
                UNDEFINED;
elif PSTATE_EL == EL3 then
    return MPAMVPM2_EL2;
elifesim PSTATE_EL == EL3 then
    return MPAMVPM2_EL2;
```

```c
MSR MPAMVPM2_EL2, <Xt>
```

<table>
<thead>
<tr>
<th>$op0$</th>
<th>$op1$</th>
<th>$CRn$</th>
<th>$CRm$</th>
<th>$op2$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x950] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MPAMVPM2_EL2 = X[t];
    end
elsif PSTATE.EL == EL3 then
    MPAMVPM2_EL2 = X[t];
The MPAMVPM3_EL2 characteristics are:

**Purpose**

MPAMVPM3_EL2 provides mappings from virtual PARTIDs 12 - 15 to physical PARTIDs.

**MPAMIDR_EL1**.VPMR_MAX field gives the index of the highest implemented MPAMVPM<n>_EL2 registers. VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If **MPAMIDR_EL1**.VPMR_MAX == 0, there is only a single MPAMVPM<n>_EL2 register, **MPAMVPM0_EL2**.

Virtual PARTID mapping is enabled by **MPAMHCR_EL2**.EL1_VPMEN for PARTIDs in **MPAM1_EL1** and by **MPAMHCR_EL2**.EL0_VPMEN for PARTIDs in **MPAM0_EL1**.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the **MPAMVPMV_EL2**.VPM_V bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented, **MPAMIDR_EL1**.HAS_HCR == 1 and **MPAMIDR_EL1**.VPMR_MAX > 2. Otherwise, direct accesses to MPAMVPM3_EL2 are **UNDEFINED**.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM3_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM3_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
<th>PhyPARTID15</th>
<th>PhyPARTID14</th>
<th>PhyPARTID13</th>
<th>PhyPARTID12</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**PhyPARTID15, bits [63:48]**

Virtual PARTID Mapping Entry for virtual PARTID 15. PhyPARTID15 gives the mapping of virtual PARTID 15 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID14, bits [47:32]**

Virtual PARTID Mapping Entry for virtual PARTID 14. PhyPARTID14 gives the mapping of virtual PARTID 14 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID13, bits [31:16]**

Virtual PARTID Mapping Entry for virtual PARTID 13. PhyPARTID13 gives the mapping of virtual PARTID 13 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID12, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 12. PhyPARTID12 gives the mapping of virtual PARTID 12 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM3_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, MPAMVPM3_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x958];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAMVPM3_EL2;
    end
elsif PSTATE.EL == EL3 then
    return MPAMVPM3_EL2;
```

MSR MPAMVPM3_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x958] = X[t];
elif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
elif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        MPAMPVM3_EL2 = X[t];
elif PSTATE.EL == EL3 then
    MPAMPVM3_EL2 = X[t];
The MPAMVPM4_EL2 characteristics are:

**Purpose**

MPAMVPM4_EL2 provides mappings from virtual PARTIDs 16 - 19 to physical PARTIDs.

**MPAMIDR_EL1**.VPMR_MAX field gives the index of the highest implemented MPAMVPM<n>_EL2 registers. VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If **MPAMIDR_EL1**.VPMR_MAX == 0, there is only a single MPAMVPM<n>_EL2 register, **MPAMVPM0_EL2**.

Virtual PARTID mapping is enabled by **MPAMHCR_EL2**.EL1_VPMEN for PARTIDs in **MPAM1_EL1** and by **MPAMHCR_EL2**.EL0_VPMEN for PARTIDs in **MPAM0_EL1**.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the **MPAMVPMV_EL2**.VPM_V bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented, MPAMIDR_EL1.HAS_HCR == 1 and MPAMIDR_EL1.VPMR_MAX > 3. Otherwise, direct accesses to MPAMVPM4_EL2 are **UNDEFINED**.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM4_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM4_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| PhyPARTID19 | PhyPARTID18 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**PhyPARTID19**, bits [63:48]

Virtual PARTID Mapping Entry for virtual PARTID 19. PhyPARTID19 gives the mapping of virtual PARTID 19 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID18**, bits [47:32]

Virtual PARTID Mapping Entry for virtual PARTID 18. PhyPARTID18 gives the mapping of virtual PARTID 18 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID17**, bits [31:16]

Virtual PARTID Mapping Entry for virtual PARTID 17. PhyPARTID17 gives the mapping of virtual PARTID 17 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID16, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 16. PhyPARTID16 gives the mapping of virtual PARTID 16 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM4_EL2**

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, MPAMVPM4_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b100</td>
</tr>
</tbody>
</table>
```

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x960];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAMVPM4_EL2;
elsif PSTATE.EL == EL3 then
    return MPAMVPM4_EL2;

MSR MPAMVPM4_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b100</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x960] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      AArch64.SystemAccessTrap(EL2, 0x18);
    end
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    MPAMVM4_EL2 = X[t];
  end
elsif PSTATE.EL == EL3 then
  MPAMVM4_EL2 = X[t];

The MPAMVPM5_EL2 characteristics are:

**Purpose**

MPAMVPM5_EL2 provides mappings from virtual PARTIDs 20 - 23 to physical PARTIDs.

The **MPAMIDR_EL1.VPRMR_MAX** field gives the index of the highest implemented MPAMVPM<n>_EL2 registers. **VPRMR_MAX** can be as large as 7 (8 registers) or 32 virtual PARTIDs. If **MPAMIDR_EL1.VPRMR_MAX == 0**, there is only a single MPAMVPM<n>_EL2 register, **MPAMVPM0_EL2**.

Virtual PARTID mapping is enabled by **MPAMHCR_EL2.EL1_VPMEN** for PARTIDs in **MPAM1_EL1** and by **MPAMHCR_EL2.EL0_VPMEN** for PARTIDs in **MPAM0_EL1**.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the **MPAMVPMV_EL2.VPM_V** bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented, MPAMIDR_EL1.HAS_HCR == 1 and MPAMIDR_EL1.VPRMR_MAX > 4. Otherwise, direct accesses to MPAMVPM5_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM5_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM5_EL2 bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>PhyPARTID23</th>
<th>PhyPARTID22</th>
<th>PhyPARTID21</th>
<th>PhyPARTID20</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
</tr>
</tbody>
</table>

**PhyPARTID23, bits [63:48]**

Virtual PARTID Mapping Entry for virtual PARTID 23. PhyPARTID23 gives the mapping of virtual PARTID 23 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID22, bits [47:32]**

Virtual PARTID Mapping Entry for virtual PARTID 22. PhyPARTID22 gives the mapping of virtual PARTID 22 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID21, bits [31:16]**

Virtual PARTID Mapping Entry for virtual PARTID 21. PhyPARTID21 gives the mapping of virtual PARTID 21 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID20, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 20. PhyPARTID20 gives the mapping of virtual PARTID 20 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM5_EL2**

Accesses to this register use the following encodings:

MRS `<Xt>`, MPAMVPM5_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x968];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        return MPAMVPM5_EL2;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAMVPM5_EL2;
    end
elsif PSTATE.EL == EL3 then
    return MPAMVPM5_EL2;
end
```

MSR MPAMVPM5_EL2, `<Xt>`

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x968] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MPAMVPM5_EL2 = X[t];
    end
elsif PSTATE.EL == EL3 then
    MPAMVPM5_EL2 = X[t];
The MPAMVPM6_EL2 characteristics are:

**Purpose**

MPAMVPM6_EL2 provides mappings from virtual PARTIDs 24 - 27 to physical PARTIDs.

- **MPAMIDR_EL1.VPMR_MAX** field gives the index of the highest implemented MPAMVPM<n>_EL2 registers.
- VPMR_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If MPAMIDR_EL1.VPMR_MAX == 0, there is only one single MPAMVPM<n>_EL2 register, MPAMVPM0_EL2.

Virtual PARTID mapping is enabled by **MPAMHCR_EL2.EL1_VPMEN** for PARTIDs in MPAM1_EL1 and by **MPAMHCR_EL2.EL0_VPMEN** for PARTIDs in MPAM0_EL1.

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the MPAMVPMV_EL2.VPM_V bit in bit position n is set to 1.

**Configuration**

This register is present only when FEAT_MPAM is implemented, MPAMIDR_EL1.HAS_HCR == 1 and MPAMIDR_EL1.VPMR_MAX > 5. Otherwise, direct accesses to MPAMVPM6_EL2 are **UNDEFINED**.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVPM6_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVPM6_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>PhyPARTID27</td>
</tr>
<tr>
<td>62</td>
<td>PhyPARTID25</td>
</tr>
<tr>
<td>61</td>
<td>PhyPARTID26</td>
</tr>
<tr>
<td>60</td>
<td>PhyPARTID24</td>
</tr>
</tbody>
</table>

**PhyPARTID27, bits [63:48]**

Virtual PARTID Mapping Entry for virtual PARTID 27. PhyPARTID27 gives the mapping of virtual PARTID 27 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID26, bits [47:32]**

Virtual PARTID Mapping Entry for virtual PARTID 26. PhyPARTID26 gives the mapping of virtual PARTID 26 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID25, bits [31:16]**

virtual PARTID Mapping Entry for virtual PARTID 25. PhyPARTID25 gives the mapping of virtual PARTID 25 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID24, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 24. PhyPARTID24 gives the mapping of virtual PARTID 24 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM6_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, MPAMVPM6_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b110</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x970];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        elsif PSTATE.EL == EL3 then
            return MPAMVPM6_EL2;
        end
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end
else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAMVPM6_EL2;
    end
elsif PSTATE.EL == EL3 then
    return MPAMVPM6_EL2;
end
```

MSR MPAMVPM6_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x970] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      AArch64.SystemAccessTrap(EL2, 0x18);
    end
  else
    UNDEFINED;
  end
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    MPAMVP6_EL2 = X[t];
  end
elsif PSTATE.EL == EL3 then
  MPAMVP6_EL2 = X[t];
MPAMVPM7_EL2, MPAM Virtual PARTID Mapping Register 7

The MPAMVPM7_EL2 characteristics are:

Purpose

MPAMVPM7_EL2 provides mappings from virtual PARTIDs 28 - 31 to physical PARTIDs.

\[ \text{MPAMIDR_EL1}.\text{VPMR\_MAX} \text{ field gives the index of the highest implemented MPAMVPM<n>_EL2 registers.} \]

VPMR\_MAX can be as large as 7 (8 registers) or 32 virtual PARTIDs. If \[ \text{MPAMIDR_EL1}.\text{VPMR\_MAX} == 0 \], there is only a single MPAMVPM<n>_EL2 register, \[ \text{MPAMVPM0\_EL2} \].

Virtual PARTID mapping is enabled by \[ \text{MPAMHCR_EL2}.\text{EL1\_VPMEN} \] for PARTIDs in \[ \text{MPAM1\_EL1} \] and by \[ \text{MPAMHCR_EL2}.\text{EL0\_VPMEN} \] for \[ \text{MPAM0\_EL1} \].

A virtual-to-physical PARTID mapping entry, PhyPARTID<n>, is only valid when the \[ \text{MPAMVPMV_EL2}.\text{VPM\_V} \] bit in bit position n is set to 1.

Configuration

This register is present only when FEAT\_MPAM is implemented, MPAMIDR_EL1.HAS\_HCR == 1 and MPAMIDR_EL1.VPMR\_MAX == 7. Otherwise, direct accesses to MPAMVPM7_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

Attributes

MPAMVPM7_EL2 is a 64-bit register.

Field descriptions

The MPAMVPM7_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PhyPARTID31</td>
<td></td>
<td>PhyPARTID30</td>
<td></td>
<td>PhyPARTID29</td>
<td></td>
<td>PhyPARTID28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

PhyPARTID31, bits [63:48]

Virtual PARTID Mapping Entry for virtual PARTID 31. PhyPARTID31 gives the mapping of virtual PARTID 31 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

PhyPARTID30, bits [47:32]

Virtual PARTID Mapping Entry for virtual PARTID 30. PhyPARTID30 gives the mapping of virtual PARTID 30 to a physical PARTID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

PhyPARTID29, bits [31:16]

Virtual PARTID Mapping Entry for virtual PARTID 29. PhyPARTID29 gives the mapping of virtual PARTID 29 to a physical PARTID.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PhyPARTID28, bits [15:0]**

Virtual PARTID Mapping Entry for virtual PARTID 28. PhyPARTID28 gives the mapping of virtual PARTID 28 to a physical PARTID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the MPAMVPM7_EL2**

Accesses to this register use the following encodings:

```plaintext
MRS <Xt>, MPAMVPM7_EL2
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x978];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    end
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return MPAMVPM7_EL2;
    end
elsif PSTATE.EL == EL3 then
    return MPAMVPM7_EL2;
end
```

```plaintext
MSR MPAMVPM7_EL2, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0110</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
else if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x978] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      AArch64.SystemAccessTrap(EL2, 0x18);
    end if
  else
    UNDEFINED;
  end if
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    MPAMVPM7_EL2 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  MPAMVPM7_EL2 = X[t];
MPAMVMV_EL2, MPAM Virtual Partition Mapping Valid Register

The MPAMVMV_EL2 characteristics are:

**Purpose**

Valid bits for virtual PARTID mapping entries. Each bit \( m \) corresponds to virtual PARTID mapping entry \( m \) in the MPAMVMV\(<n>\)_EL2 registers where \( n = m \gg 2 \).

**Configuration**

This register is present only when FEAT_MPAM is implemented and MPAMIDR_EL1.HAS_HCR == 1. Otherwise, direct accesses to MPAMVMV_EL2 are undefined.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

MPAMVMV_EL2 is a 64-bit register.

**Field descriptions**

The MPAMVMV_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
</tr>
</thead>
</table>

**Bits [63:32]**

Reserved, RES0.

**VPM_V<m>, bit [m], for m = 31 to 0**

Contains valid bit for virtual PARTID mapping entry corresponding to virtual PARTID\(<m>\).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the MPAMVMV_EL2**

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x938] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && MPAM3_EL3.TRAPLOWER == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        MPAMVPMV_EL2 = X[t];
    end
elsif PSTATE.EL == EL3 then
    MPAMVPMV_EL2 = X[t];

MSR MPAMVPMV_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
**MPIDR_EL1, Multiprocessor Affinity Register**

The MPIDR_EL1 characteristics are:

**Purpose**

In a multiprocessor system, provides an additional PE identification mechanism for scheduling purposes.

**Configuration**

AArch64 System register MPIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register `MPIDR[31:0]`.

In a uniprocessor system Arm recommends that each Aff<n> field of this register returns a value of 0.

**Attributes**

MPIDR_EL1 is a 64-bit register.

**Field descriptions**

The MPIDR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | U | RES0 | MT | Aff2 | Aff1 | Aff0 | Aff3 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:40]**

Reserved, RES0.

**Aff3, bits [39:32]**

Affinity level 3. See the description of Aff0 for more information.

Aff3 is not supported in AArch32 state.

**Bit [31]**

Reserved, RES1.

**U, bit [30]**

Indicates a Uniprocessor system, as distinct from PE 0 in a multiprocessor system. The possible values of this bit are:

<table>
<thead>
<tr>
<th><code>U</code></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Processor is part of a multiprocessor system.</td>
</tr>
<tr>
<td>0b1</td>
<td>Processor is part of a uniprocessor system.</td>
</tr>
</tbody>
</table>

**Bits [29:25]**

Reserved, RES0.
Indicates whether the lowest level of affinity consists of logical PEs that are implemented using a multithreading type approach. See the description of Aff0 for more information about affinity levels. The possible values of this bit are:

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Performance of PEs at the lowest affinity level, or PEs with MPIDR_EL1.MT set to 1, different affinity level 0 values, and the same values for affinity level 1 and higher, is largely independent.</td>
</tr>
<tr>
<td>0b1</td>
<td>Performance of PEs at the lowest affinity level, or PEs with MPIDR_EL1.MT set to 1, different affinity level 0 values, and the same values for affinity level 1 and higher, is very interdependent.</td>
</tr>
</tbody>
</table>

Aff2, bits [23:16]
Affinity level 2. See the description of Aff0 for more information.

Aff1, bits [15:8]
Affinity level 1. See the description of Aff0 for more information.

Aff0, bits [7:0]
Affinity level 0. This is the affinity level that is most significant for determining PE behavior. Higher affinity levels are increasingly less significant in determining PE behavior. The assigned value of the MPIDR.{Aff2, Aff1, Aff0} or MPIDR_EL1.{Aff3, Aff2, Aff1, Aff0} set of fields of each PE must be unique within the system as a whole.

Accessing the MPIDR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, MPIDR_EL1

```c
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    else
        UNDEFINED;
    else
        if EL2Enabled() then
            if EL2Enabled() && !HaveEL(EL3) || SCR_EL3.FGTEn == '1' && HFGRT_EL2.MPIDR_EL1 == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() then
                return VMPIDR_EL2;
            else
                return MPIDR_EL1;
            end
        elsif PSTATE.EL == EL2 then
            return MPIDR_EL1;
        elsif PSTATE.EL == EL3 then
            return MPIDR_EL1;
        else
            return MPIDR_EL1;
        end

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e9e71047211
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MVFR0_EL1, AArch32 Media and VFP Feature Register 0

The MVFR0_EL1 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation.

Must be interpreted with MVFR1_EL1 and MVFR2_EL1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register MVFR0_EL1 bits [31:0] are architecturally mapped to AArch32 System register MVFR0[31:0].

In an implementation where at least one Exception level supports execution in AArch32 state, but there is no support for Advanced SIMD and floating-point operation, this register is RAZ.

**Attributes**

MVFR0_EL1 is a 64-bit register.

**Field descriptions**

The MVFR0_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | FPRound | FPShVec | FPSqrt | FPDivide | FPtrap | FPDP | FPS | SIMDReg |

**Bits [63:32]**

Reserved, RES0.

**FPRound, bits [31:28]**

Floating-Point Rounding modes. Indicates whether the floating-point implementation provides support for rounding modes. Defined values are:

<table>
<thead>
<tr>
<th>FPRound</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or only Round to Nearest mode supported, except that Round towards Zero mode is supported for VCVT instructions that always use that rounding mode regardless of the FPSCR setting.</td>
</tr>
<tr>
<td>0b0001</td>
<td>All rounding modes supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the permitted values are 0b0000 and 0b0001.
FPShVec, bits [27:24]

Short Vectors. Indicates whether the floating-point implementation provides support for the use of short vectors. Defined values are:

<table>
<thead>
<tr>
<th>FPShVec</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Short vectors not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Short vector operation supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the only permitted value is 0b0000.

FPSqrt, bits [23:20]

Square Root. Indicates whether the floating-point implementation provides support for the ARMv6 VFP square root operations. Defined values are:

<table>
<thead>
<tr>
<th>FPSqrt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the permitted values are 0b0000 and 0b0001.

The VSQRT.F32 instruction also requires the single-precision floating-point attribute, bits [7:4], and the VSQRT.F64 instruction also requires the double-precision floating-point attribute, bits [11:8].

FPDivide, bits [19:16]

Indicates whether the floating-point implementation provides support for VFP divide operations. Defined values are:

<table>
<thead>
<tr>
<th>FPDivide</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the permitted values are 0b0000 and 0b0001.

The VDIV.F32 instruction also requires the single-precision floating-point attribute, bits [7:4], and the VDIV.F64 instruction also requires the double-precision floating-point attribute, bits [11:8].

FPTrap, bits [15:12]

Floating Point Exception Trapping. Indicates whether the floating-point implementation provides support for exception trapping. Defined values are:

<table>
<thead>
<tr>
<th>FPTrap</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

A value of 0b0001 indicates that, when the corresponding trap is enabled, a floating-point exception generates an exception.

FPDP, bits [11:8]

Double Precision. Indicates whether the floating-point implementation provides support for double-precision operations. Defined values are:
FPDP, bits [7:4]

Single Precision. Indicates whether the floating-point implementation provides support for single-precision operations. Defined values are:

<table>
<thead>
<tr>
<th>FPDP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported, VFPv2.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Supported, VFPv3, VFPv4, or Armv8. VFPv3 and Armv8 add an instruction to load a double-precision floating-point constant, and conversions between double-precision and fixed-point values.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the permitted values are 0b0000 and 0b0010.

A value of 0b0001 or 0b0010 indicates support for all VFP double-precision instructions in the supported version of VFP, except that, in addition to this field being nonzero:

- VSQRT.F64 is only available if the Square root field is 0b0001.
- VDIV.F64 is only available if the Divide field is 0b0001.
- Conversion between double-precision and single-precision is only available if the single-precision field is nonzero.

SIMDReg, bits [3:0]

Advanced SIMD registers. Indicates whether the Advanced SIMD and floating-point implementation provides support for the Advanced SIMD and floating-point register bank. Defined values are:

<table>
<thead>
<tr>
<th>SIMDReg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The implementation has no Advanced SIMD and floating-point support.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The implementation includes floating-point support with 16 x 64-bit registers.</td>
</tr>
<tr>
<td>0b0010</td>
<td>The implementation includes Advanced SIMD and floating-point support with 32 x 64-bit registers.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A the permitted values are 0b0000 and 0b0010.

Otherwise:
Bits [63:0]

Reserved, UNKNOWN.

Accessing the MVFR0_EL1

Accesses to this register use the following encodings:

\[
\text{MRS} \langle Xt \rangle, \text{MVFR0_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return MVFR0_EL1;
elsif PSTATE.EL == EL2 then
  return MVFR0_EL1;
elsif PSTATE.EL == EL3 then
  return MVFR0_EL1;
The MVFR1_EL1 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation.

Must be interpreted with **MVFR0_EL1** and **MVFR2_EL1**.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register MVFR1_EL1 bits [31:0] are architecturally mapped to AArch32 System register **MVFR1[31:0]**

In an implementation where at least one Exception level supports execution in AArch32 state, but there is no support for Advanced SIMD and floating-point operation, this register is RAZ.

**Attributes**

MVFR1_EL1 is a 64-bit register.

**Field descriptions**

The MVFR1_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bit assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>SIMDFMAC, FPHP, SIMDHP, SIMDSP, SIMDInt, SIMDLS, FPNaN, FPFtZ</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**SIMDFMAC, bits [31:28]**

Advanced SIMD Fused Multiply-Accumulate. Indicates whether the Advanced SIMD implementation provides fused multiply accumulate instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDFMAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

The Advanced SIMD and floating-point implementations must provide the same level of support for these instructions.
**FPHP, bits [27:24]**

Floating Point Half Precision. Indicates the level of half-precision floating-point support. Defined values are:

<table>
<thead>
<tr>
<th>FPHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Floating-point half-precision conversion instructions are supported for conversion between single-precision and half-precision.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds instructions for conversion between double-precision and half-precision.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds support for half-precision floating-point arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 in an implementation without floating-point support.
- 0b0010 in an implementation with floating-point support that does not include the FEAT_FP16 extension.
- 0b0011 in an implementation with floating-point support that includes the FEAT_FP16 extension.

The level of support indicated by this field must be equivalent to the level of support indicated by the SIMDHP field, meaning the permitted values are:

<table>
<thead>
<tr>
<th>Half Precision instructions supported</th>
<th>FPHP</th>
<th>SIMDHP</th>
</tr>
</thead>
<tbody>
<tr>
<td>No support</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
<tr>
<td>Conversions only</td>
<td>0b0010</td>
<td>0b0001</td>
</tr>
<tr>
<td>Conversions and arithmetic</td>
<td>0b0011</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

**SIMDHP, bits [23:20]**

Advanced SIMD Half Precision. Indicates the level of half-precision floating-point support. Defined values are:

<table>
<thead>
<tr>
<th>SIMDHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SIMD half-precision conversion instructions are supported for conversion between single-precision and half-precision.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds support for half-precision floating-point arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 in an implementation without SIMD floating-point support.
- 0b0010 in an implementation with SIMD floating-point support that does not include the FEAT_FP16 extension.
- 0b0011 in an implementation with SIMD floating-point support that includes the FEAT_FP16 extension.

The level of support indicated by this field must be equivalent to the level of support indicated by the FPHP field, meaning the permitted values are:

<table>
<thead>
<tr>
<th>Half Precision instructions supported</th>
<th>FPHP</th>
<th>SIMDHP</th>
</tr>
</thead>
<tbody>
<tr>
<td>No support</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
<tr>
<td>Conversions only</td>
<td>0b0010</td>
<td>0b0001</td>
</tr>
<tr>
<td>Conversions and arithmetic</td>
<td>0b0011</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

**SIMDSP, bits [19:16]**

Advanced SIMD Single Precision. Indicates whether the Advanced SIMD and floating-point implementation provides single-precision floating-point instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDSP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented. This value is permitted only if the SIMDInt field is 0b0001.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the permitted values are 0b0000 and 0b0001.

**SIMDInt, bits [15:12]**

Advanced SIMD Integer. Indicates whether the Advanced SIMD and floating-point implementation provides integer instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDInt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**SIMDLS, bits [11:8]**

Advanced SIMD Load/Store. Indicates whether the Advanced SIMD and floating-point implementation provides load/store instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDLS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**FPDNaN, bits [7:4]**

Default NaN mode. Indicates whether the floating-point implementation provides support only for the Default NaN mode. Defined values are:

<table>
<thead>
<tr>
<th>FPDNaN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or hardware supports only the Default NaN mode.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Hardware supports propagation of NaN values.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**FPFtZ, bits [3:0]**

Flush to Zero mode. Indicates whether the floating-point implementation provides support only for the Flush-to-Zero mode of operation. Defined values are:

<table>
<thead>
<tr>
<th>FPFtZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or hardware supports only the Flush-to-Zero mode of operation.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Hardware supports full denormalized number arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**Otherwise:**

```
63  62  61  60  59  58  57  56  55  54  53  52  51  50  49  48  47  46  45  44  43  42  41  40  39  38  37  36  35  34  33  32
   UNKNOWN

31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9   8   7   6   5   4   3   2   1    0
   UNKNOWN
```
Bits [63:0]

Reserved, UNKNOWN.

Accessing the MVFR1_EL1

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ MVFR1_EL1}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TID3 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return MVFR1_EL1;
elsif PSTATE.EL == EL2 then
  return MVFR1_EL1;
elsif PSTATE.EL == EL3 then
  return MVFR1_EL1;
The MVFR2_EL1 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation. Must be interpreted with MVFR0_EL1 and MVFR1_EL1.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch64 System register MVFR2_EL1 bits [31:0] are architecturally mapped to AArch32 System register MVFR2[31:0].

In an implementation where at least one Exception level supports execution in AArch32 state, but there is no support for Advanced SIMD and floating-point operation, this register is RAZ.

**Attributes**

MVFR2_EL1 is a 64-bit register.

**Field descriptions**

The MVFR2_EL1 bit assignments are:

**When AArch32 is supported at any Exception level:**

<table>
<thead>
<tr>
<th>Bits [63:8]</th>
<th>RES0</th>
<th>FPMisc</th>
<th>SIMDMisc</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Bits [31:0]</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:8]**

Reserved, RES0.

**FPMisc, bits [7:4]**

Indicates whether the floating-point implementation provides support for miscellaneous VFP features.

<table>
<thead>
<tr>
<th>FPMisc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or no support for miscellaneous features.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Floating-point selection.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and Floating-point Conversion to Integer with Directed Rounding modes.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, and Floating-point Round to Integer Floating-point.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As 0b0011, and Floating-point MaxNum and MinNum.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0100.
**SIMDMisc, bits [3:0]**

Indicates whether the Advanced SIMD implementation provides support for miscellaneous Advanced SIMD features.

<table>
<thead>
<tr>
<th>SIMDMisc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or no support for miscellaneous features.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Floating-point Conversion to Integer with Directed Rounding modes.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and Floating-point Round to Integer Floating-point.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, and Floating-point MaxNum and MinNum.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0011.

**Otherwise:**

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>UNKNOWN</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>UNKNOWN</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Reserved, UNKNOWN.

**Accessing the MVFR2_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, MVFR2_EL1

```plaintext
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b010</td>
<td></td>
</tr>
</tbody>
</table>
```

```plaintext
if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID3 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      return MVFR2_EL1;
  elsif PSTATE.EL == EL2 then
    return MVFR2_EL1;
  elsif PSTATE.EL == EL3 then
    return MVFR2_EL1;
```

30/09/2020 15:07; cceed08b089f9ceac50268e82a9e9e719047211

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The NZCV characteristics are:

**Purpose**

Allows access to the condition flags.

**Configuration**

There are no configuration notes.

**Attributes**

NZCV is a 64-bit register.

**Field descriptions**

The NZCV bit assignments are:

```
<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>N</td>
<td>Z</td>
<td>C</td>
<td>V</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

Bits [63:32]

Reserved, RES0.

**N, bit [31]**

Negative condition flag. Set to 1 if the result of the last flag-setting instruction was negative.

**Z, bit [30]**

Zero condition flag. Set to 1 if the result of the last flag-setting instruction was zero, and to 0 otherwise. A result of zero often indicates an equal result from a comparison.

**C, bit [29]**

Carry condition flag. Set to 1 if the last flag-setting instruction resulted in a carry condition, for example an unsigned overflow on an addition.

**V, bit [28]**

Overflow condition flag. Set to 1 if the last flag-setting instruction resulted in an overflow condition, for example a signed overflow on an addition.

**Bits [27:0]**

Reserved, RES0.
Accessing the NZCV

Accesses to this register use the following encodings:

**MRS <Xt>, NZCV**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    return Zeros(32):PSTATE.<N,Z,C,V>:Zeros(28);
elsif PSTATE.EL == EL1 then
    return Zeros(32):PSTATE.<N,Z,C,V>:Zeros(28);
elsif PSTATE.EL == EL2 then
    return Zeros(32):PSTATE.<N,Z,C,V>:Zeros(28);
elsif PSTATE.EL == EL3 then
    return Zeros(32):PSTATE.<N,Z,C,V>:Zeros(28);

**MSR NZCV, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
elsif PSTATE.EL == EL1 then
 elsif PSTATE.EL == EL2 then
elsif PSTATE.EL == EL3 then
OSDLR_EL1, OS Double Lock Register

The OSDLR_EL1 characteristics are:

**Purpose**

Used to control the OS Double Lock.

**Configuration**

AArch64 System register OSDLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGOSDLR[31:0].

**Attributes**

OSDLR_EL1 is a 64-bit register.

**Field descriptions**

The OSDLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit (from 63 to 0)</th>
<th>Bit Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
</tr>
<tr>
<td>61</td>
<td>DLK</td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td></td>
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<tr>
<td>54</td>
<td></td>
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<tr>
<td>53</td>
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<tr>
<td>52</td>
<td></td>
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<tr>
<td>51</td>
<td></td>
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<tr>
<td>50</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td></td>
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<td>33</td>
<td></td>
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<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:1]**

Reserved, RES0.

**DLK, bit [0]**

When FEAT_DoubleLock is implemented:

OS Double Lock control bit.

<table>
<thead>
<tr>
<th>DLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Double Lock unlocked.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Double Lock locked, if DBGPRCR_EL1.CORENPDRQ (Core no powerdown request) bit is set to 0 and the PE is in Non-debug state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Otherwise:**

Reserved, RAZ/WI.

**Accessing the OSDLR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, OSDLR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && IsFeatureImplemented(FEAT_DoubleLock) && HDFGRTR_EL2.OSDLR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDOSA> != '00' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL2.TDOSA") then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return OSDLR_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return OSDLR_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return OSDLR_EL1;

MSR OSDLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && IsFeatureImplemented(FEAT_DoubleLock) && HDFGWTR_EL2.OSDLR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDOSA> != '00' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL2.TDOSA") then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
    else
        OSDLR_EL1 = X[t];
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' && (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
        else
            OSDLR_EL1 = X[t];
        elsif PSTATE.EL == EL3 then
            OSDLR_EL1 = X[t];
    else
        OSDLR_EL1 = X[t];
OSDTRRX_EL1, OS Lock Data Transfer Register, Receive

The OSDTRRX_EL1 characteristics are:

**Purpose**

Used for save/restore of DBGDTRRX_EL0. It is a component of the Debug Communications Channel.

**Configuration**

AArch64 System register OSDTRRX_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRRXext[31:0].

**Attributes**

OSDTRRX_EL1 is a 64-bit register.

**Field descriptions**

The OSDTRRX_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 |

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

Update DTRRX without side-effect.

Writes to this register update the value in DTRRX and do not change RXfull.

Reads of this register return the last value written to DTRRX and do not change RXfull.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

**Accessing the OSDTRRX_EL1**

Arm deprecates reads and writes of OSDTRRX_EL1 when the OS Lock is unlocked.

Accesses to this register use the following encodings:

MRS <Xt>, OSDTRRX_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return OSDTRRX_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return OSDTRRX_EL1;
    end
elsif PSTATE.EL == EL3 then
    return OSDTRRX_EL1;
end

MSR OSDTRRX_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
else PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
eOSDTRRX_EL1 = X[t];
OSDTRTX_EL1, OS Lock Data Transfer Register, Transmit

The OSDTRTX_EL1 characteristics are:

**Purpose**

Used for save/restore of DBGDTRTX_EL0. It is a component of the Debug Communications Channel.

**Configuration**

AArch64 System register OSDTRTX_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRTXEXT[31:0].

**Attributes**

OSDTRTX_EL1 is a 64-bit register.

**Field descriptions**

The OSDTRTX_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td></td>
<td>Return DTRTX without side-effect</td>
</tr>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

Return DTRTX without side-effect.

Reads of this register return the value in DTRTX and do not change TXfull.

Writes of this register update the value in DTRTX and do not change TXfull.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

**Accessing the OSDTRTX_EL1**

Arm deprecates reads and writes of OSDTRTX_EL1 when the OS Lock is unlocked.

Accesses to this register use the following encodings:

```
MRS <Xt>, OSDTRTX_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return OSDTRTX_EL1;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return OSDTRTX_EL1;
  end if;
elsif PSTATE.EL == EL3 then
  return OSDTRTX_EL1;
end if;

MSR OSXTRTX_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && MDCR_EL2.TDCC == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        OSDTRTX_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        OSDTRTX_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    OSDTRTX_EL1 = X[t];
OSECCR_EL1, OS Lock Exception Catch Control Register

The OSECCR_EL1 characteristics are:

**Purpose**

Provides a mechanism for an operating system to access the contents of EDECCR that are otherwise invisible to software, so it can save/restore the contents of EDECCR over powerdown on behalf of the external debugger.

**Configuration**

AArch64 System register OSECCR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGOSECCR[31:0].

AArch64 System register OSECCR_EL1 bits [31:0] are architecturally mapped to External register EDECCR[31:0].

If OSLSR_EL1.OSLK == 0, then OSECCR_EL1 returns an UNKNOWN value on reads and ignores writes.

**Attributes**

OSECCR_EL1 is a 64-bit register.

**Field descriptions**

The OSECCR_EL1 bit assignments are:

**When OSLSR_EL1.OSLK == 1:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | EDECCR |

**Bits [63:32]**

Reserved, RES0.

**EDECCR, bits [31:0]**

Used for save/restore to EDECCR over powerdown.

Reads or writes to this field are indirect accesses to EDECCR.

**Accessing the OSECCR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, OSECCR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.OSECCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return OSECCR_EL1;
    endif
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return OSECCR_EL1;
    endif
elseif PSTATE.EL == EL3 then
    return OSECCR_EL1;
else
    MSR OSECCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.OSECCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        OSECCR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        OSECCR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    OSECCR_EL1 = X[t];
OSLAR_EL1, OS Lock Access Register

The OSLAR_EL1 characteristics are:

**Purpose**

Used to lock or unlock the OS Lock.

**Configuration**

AArch64 System register OSLAR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGOSLAR[31:0].

AArch64 System register OSLAR_EL1 bits [31:0] are architecturally mapped to External register OSLAR_EL1[31:0].

**Attributes**

OSLAR_EL1 is a 64-bit register.

**Field descriptions**

The OSLAR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
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<th>47</th>
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<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
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<th>38</th>
<th>37</th>
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</tr>
<tr>
<td>RES0</td>
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<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
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<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:1]**

Reserved, RES0.

**OSLK, bit [0]**

On writes to OSLAR_EL1, bit[0] is copied to the OS Lock.

Use OSLSR_EL1, OSLK to check the current status of the lock.

**Accessing the OSLAR_EL1**

Accesses to this register use the following encodings:

```
MSR OSLAR_EL1, <Xt>
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.OSLAR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.<TDE,TDOSA> != '00' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    OSLAR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    OSLAR_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  OSLAR_EL1 = X[t];
OSLR_EL1, OS Lock Status Register

The OSLR_EL1 characteristics are:

**Purpose**

Provides the status of the OS Lock.

**Configuration**

AArch64 System register OSLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGOSLR[31:0].

**Attributes**

OSLR_EL1 is a 64-bit register.

**Field descriptions**

The OSLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>OSLM[1]</td>
</tr>
<tr>
<td>60</td>
<td>nTT</td>
</tr>
<tr>
<td>59</td>
<td>OSLK</td>
</tr>
<tr>
<td>58</td>
<td>OSLM[0]</td>
</tr>
<tr>
<td>57</td>
<td>Bits [63:4]</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>45</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>43</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [63:4]**

Reserved, RES0.

**OSLM, bits [3, 0]**

OS lock model implemented. Identifies the form of OS save and restore mechanism implemented.

<table>
<thead>
<tr>
<th>OSLM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Lock not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Lock implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved. In an Armv8 implementation the value 0b0 is not permitted.

The OSLM field is split as follows:

- OSLM[1] is OSLR_EL1[3].
- OSLM[0] is OSLR_EL1[0].

**nTT, bit [2]**

Not 32-bit access. This bit is always RAZ. It indicates that a 32-bit access is needed to write the key to the OS Lock Access Register.

**OSLK, bit [1]**

OS Lock Status.

<table>
<thead>
<tr>
<th>OSLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Lock unlocked.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Lock locked.</td>
</tr>
</tbody>
</table>
The OS Lock is locked and unlocked by writing to the OS Lock Access Register.

On a Cold reset, this field resets to 1.

**Accessing the OSLR_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, OSLR_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.OSLR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL2, 0x18);
  end
elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return OSLSR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDOSA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return OSLSR_EL1;
elsif PSTATE.EL == EL3 then
  return OSLSR_EL1;
```
PAN, Privileged Access Never

The PAN characteristics are:

**Purpose**

Allows access to the Privileged Access Never bit.

**Configuration**

This register is present only when FEAT_PAN is implemented. Otherwise, direct accesses to PAN are UNDEFINED.

**Attributes**

PAN is a 64-bit register.

**Field descriptions**

The PAN bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
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<tr>
<td>59</td>
<td>Reserved, RES0</td>
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<td>58</td>
<td>Reserved, RES0</td>
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<td>Reserved, RES0</td>
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<td>42</td>
<td>Reserved, RES0</td>
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<tr>
<td>41</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:23]**

Reserved, RES0.

**PAN, bit [22]**

Privileged Access Never.

<table>
<thead>
<tr>
<th>PAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 b0</td>
<td>Privileged reads and write are not disabled by this mechanism.</td>
</tr>
<tr>
<td>0 b1</td>
<td>Disables privileged read and write accesses to addresses accessible at EL0 for an enabled stage 1 translation regime that defines the EL0 permissions.</td>
</tr>
</tbody>
</table>

The value of this bit is usually preserved on taking an exception, except in the following situations:

- When the target of the exception is EL1, and the value of the SCTLRL_EL1.SPAN bit is 0, this bit is set to 1.
- When the target of the exception is EL2, HCR_EL2.{E2H, TGE} is \{1, 1\}, and the value of the SCTLRL_EL2.SPAN bit is 0, this bit is set to 1.

**Bits [21:0]**

Reserved, RES0.

**Accessing the PAN**

Accesses to this register use the following encodings:
MRS <Xt>, PAN

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
return Zeros(41):PSTATE.PAN:Zeros(22);
elsif PSTATE.EL == EL2 then
return Zeros(41):PSTATE.PAN:Zeros(22);
elsif PSTATE.EL == EL3 then
return Zeros(41):PSTATE.PAN:Zeros(22);

MSR PAN, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
PSTATE.PAN = X[t]<22>;
elsif PSTATE.EL == EL2 then
PSTATE.PAN = X[t]<22>;
elsif PSTATE.EL == EL3 then
PSTATE.PAN = X[t]<22>;

MSR PAN, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
PAR_EL1, Physical Address Register

The PAR_EL1 characteristics are:

**Purpose**

Returns the output address (OA) from an Address translation instruction that executed successfully, or fault information if the instruction did not execute successfully.

**Configuration**

AArch64 System register PAR_EL1 bits [63:0] are architecturally mapped to AArch32 System register PAR[63:0].

**Attributes**

PAR_EL1 is a 64-bit register.

**Field descriptions**

The PAR_EL1 bit assignments are:

**When PAR_EL1.F == 0:**

<table>
<thead>
<tr>
<th>ATTR</th>
<th>RES0</th>
<th>PA[51:48]</th>
<th>PA[47:12]</th>
<th>RES1</th>
<th>IMPLEMENTATION DEFINED</th>
<th>NS</th>
<th>SH</th>
<th>RES0</th>
<th>F</th>
</tr>
</thead>
</table>

This section describes the register value returned by the successful execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

On a successful conversion, the PAR_EL1 can return a value that indicates the resulting attributes, rather than the values that appear in the translation table descriptors. More precisely:

- The PAR_EL1.{ATTR, SH} fields are permitted to report the resulting attributes, as determined by any permitted implementation choices and any applicable configuration bits, instead of reporting the values that appear in the translation table descriptors.
- See the PAR_EL1.NS bit description for constraints on the value it returns.

**ATTR, bits [63:56]**

Memory attributes for the returned output address. This field uses the same encoding as the Attr<n> fields in MAIR_EL1, MAIR_EL2, and MAIR_EL3.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [55:52]**

Reserved, RES0.
**PA[51:48], bits [51:48]**

*When FEAT_LPA is implemented:*

Extension to PA[47:12]. See PA[47:12] for more details.

On a Warm reset, this field resets to an architecturally *UNKNOWN* value.

*Otherwise:*

Reserved, RES0.

**PA[47:12], bits [47:12]**

Output address. The output address (OA) corresponding to the supplied input address. This field returns address bits[47:12].

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, the PA[51:48] bits form the upper part of the address value. Otherwise the PA[51:48] bits are RES0.

For implementations with fewer than 48 physical address bits, the corresponding upper bits in this field are RES0.

On a Warm reset, this field resets to an architecturally *UNKNOWN* value.

**Bit [11]**

Reserved, RES1.

**IMPLEMENTATION DEFINED, bit [10]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally *UNKNOWN* value.

**NS, bit [9]**

Non-secure. The NS attribute for a translation table entry from a Secure translation regime.

For a result from a Secure translation regime, when SCR_EL3.EEL2 is 1, this bit reflects the Security state of the intermediate physical address space of the translation for the instructions:

- In AArch64 state: AT S1E1R, AT S1E1W, AT S1E1RP, AT S1E1WP, AT S1E0R, and AT S1E0W.
- In AArch32 state: ATS1CPR, ATS1CPW, ATS1CPRP, ATS1CPWP, ATS1CUR, and ATS1CUW.

Otherwise, this bit reflects the Security state of the physical address space of the translation. This means it reflects the effect of the NSTable bits of earlier levels of the translation table walk if those NSTable bits have an effect on the translation.

For a result from a Non-secure translation regime, this bit is *UNKNOWN*.

On a Warm reset, this field resets to an architecturally *UNKNOWN* value.

**SH, bits [8:7]**

Shareability attribute, for the returned output address. Permitted values are:

<table>
<thead>
<tr>
<th>SH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

The value 0b01 is reserved.

**Note**
This field returns the value 0b10 for:

- Any type of Device memory.
- Normal memory with both Inner Non-cacheable and Outer Non-cacheable attributes.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [6:1]**

Reserved, RES0.

**F, bit [0]**

Indicates whether the instruction performed a successful address translation.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Address translation completed successfully.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**When PAR_EL1.F == 1:**

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40</th>
<th>39 38 37 36 35 34 33 32</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMPLEMENTATION DEFINED</td>
<td>IMPLEMENTATION DEFINED</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>RES0</td>
<td>RES1</td>
<td>RES0</td>
</tr>
</tbody>
</table>

This section describes the register value returned by a fault on the execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

**IMPLEMENTATION DEFINED, bits [63:56]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IMPLEMENTATION DEFINED, bits [55:52]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IMPLEMENTATION DEFINED, bits [51:48]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [47:12]**

Reserved, RES0.

**Bit [11]**

Reserved, RES1.
**Bit [10]**

Reserved, RES0.

**S, bit [9]**

Indicates the translation stage at which the translation aborted:

<table>
<thead>
<tr>
<th>S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Translation aborted because of a fault in the stage 1 translation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Translation aborted because of a fault in the stage 2 translation.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PTW, bit [8]**

If this bit is set to 1, it indicates the translation aborted because of a stage 2 fault during a stage 1 translation table walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [7]**

Reserved, RES0.

**FST, bits [6:1]**

Fault status code, as shown in the Data Abort ESR encoding.
<table>
<thead>
<tr>
<th>FST</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of translation or translation table base</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>register</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001100</td>
<td>Permission fault, level 0.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>of translation table, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td></td>
<td>of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011011</td>
<td>Synchronous parity or ECC error on memory access on translation table</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td></td>
<td>walk or hardware update of translation table, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b011100</td>
<td>Synchronous parity or ECC error on memory access on translation table</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td></td>
<td>walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td></td>
<td>walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td></td>
<td>walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td></td>
<td>walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b101001</td>
<td>Address size fault, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b101011</td>
<td>Translation fault, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b110001</td>
<td>Unsupported atomic hardware update fault.</td>
<td>When FEAT_HAFDBS is implemented</td>
</tr>
<tr>
<td>0b111101</td>
<td>Section Domain fault, from an AArch32 stage 1 EL1&amp;0 translation regime</td>
<td>When EL1 is capable of using AArch32</td>
</tr>
<tr>
<td></td>
<td>using Short-descriptor translation table format.</td>
<td></td>
</tr>
</tbody>
</table>
PAR_EL1, Physical Address Register

0b111110 Page Domain fault, from an AArch32 stage 1 EL1&0 translation regime using Short-descriptor translation table format.

When EL1 is capable of using AArch32

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [0]

Indicates whether the instruction performed a successful address translation.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Address translation aborted.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the PAR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PAR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGTR_EL2.PAR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return PAR_EL1;
elsif PSTATE.EL == EL2 then
  return PAR_EL1;
elsif PSTATE.EL == EL3 then
  return PAR_EL1;

MSR PAR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.PAR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    PAR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  PAR_EL1 = X[t];
eisf PSTATE.EL == EL3 then
  PAR_EL1 = X[t];
PMBIDR_EL1, Profiling Buffer ID Register

The PMBIDR_EL1 characteristics are:

**Purpose**

Provides information to software as to whether the buffer can be programmed at the current Exception level.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMBIDR_EL1 are UNDEFINED.

**Attributes**

PMBIDR_EL1 is a 64-bit register.

**Field descriptions**

The PMBIDR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
| Bits [63:6] |

Reserved, RES0.

**F, bit [5]**

Flag updates. Defines whether the address translation performed by the Profiling Buffer manages the Access Flag and dirty state.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hardware management of the Access Flag and dirty state for accesses made by the Statistical Profiling Extension is always disabled for all translation stages.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hardware management for the Access Flag and dirty state for accesses made by the Statistical Profiling Extension is controlled in the same way as explicit memory accesses in the owning translation regime.</td>
</tr>
</tbody>
</table>

If hardware management of the Access Flag is disabled for a stage of translation, an access to Page or Block with the Access flag bit not set in the descriptor will generate an Access Flag fault.

If hardware management of the dirty state is disabled for a stage of translation, an access to a Page or Block will ignore the Dirty Bit Modifier in the descriptor might generate a Permission fault, depending on the values of the access permission bits in the descriptor.

**P, bit [4]**

Programming not allowed. The Profiling Buffer is owned by a higher Exception level or the other Security state.
Meaning

0b0  Profiling Buffer is owned by the current or a lower Exception level in the current Security state.
0b1  Profiling Buffer is owned by a higher Exception level or the other Security state.

The value read from this field depends on the current Exception level and the Effective values of MDCR_EL3.NSPB and MDCR_EL2.E2PB:

- If EL3 is implemented, and either MDCR_EL3.NSPB == 0b00 or MDCR_EL3.NSPB == 0b01, this bit reads as one from:
  - Non-secure EL1.
  - Non-secure EL2.
  - If Secure EL2 is implemented and enabled, and MDCR_EL2.E2PB == 0b00, Secure EL1.
- If EL3 is implemented, and either MDCR_EL3.NSPB == 0b10 or MDCR_EL3.NSPB == 0b11, this bit reads as one from:
  - Secure EL1.
  - If Secure EL2 is implemented, Secure EL2.
  - If EL2 is implemented and MDCR_EL2.E2PB == 0b00, Non-secure EL1.
- If EL3 is not implemented, EL2 is implemented, and MDCR_EL2.E2PB == 0b00, this bit reads as one from EL1.
- Otherwise, this bit reads as zero.

Align, bits [3:0]

Defines the minimum alignment constraint for PMBPTR_EL1. If this field is non-zero, then the PE must pad every record up to a multiple of this size.

<table>
<thead>
<tr>
<th>Align</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Byte</td>
</tr>
<tr>
<td>0b0001</td>
<td>Halfword.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Word</td>
</tr>
<tr>
<td>0b0011</td>
<td>Doubleword.</td>
</tr>
<tr>
<td>0b0100</td>
<td>16 Bytes.</td>
</tr>
<tr>
<td>0b0101</td>
<td>32 Bytes.</td>
</tr>
<tr>
<td>0b0110</td>
<td>64 Bytes.</td>
</tr>
<tr>
<td>0b0111</td>
<td>128 Bytes.</td>
</tr>
<tr>
<td>0b1000</td>
<td>256 Bytes.</td>
</tr>
<tr>
<td>0b1001</td>
<td>512 Bytes.</td>
</tr>
<tr>
<td>0b1010</td>
<td>1KB.</td>
</tr>
<tr>
<td>0b1011</td>
<td>2KB.</td>
</tr>
</tbody>
</table>

For more information, see 'Restrictions on the current write pointer'.

Accessing the PMBIDR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PMBIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  return PMBIDR_EL1;
elsif PSTATE.EL == EL2 then
  return PMBIDR_EL1;
elsif PSTATE.EL == EL3 then
  return PMBIDR_EL1;
PMBLIMITR_EL1, Profiling Buffer Limit Address Register

PMBLIMITR_EL1 characteristics are:

**Purpose**

Defines the upper limit for the profiling buffer, and enables the profiling buffer

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMBLIMITR_EL1 are UNDEFINED.

**Attributes**

PMBLIMITR_EL1 is a 64-bit register.

**Field descriptions**

The PMBLIMITR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | LIMIT |

**LIMIT**, bits [63:12]

Limit address. PMBLIMITR_EL1.LIMIT:Zeros(12) is the address of the first byte in memory after the last byte in the profiling buffer. If the smallest implemented translation granule is not 4KB, then bits[N-1:12] are RES0, where N is the IMPLEMENTATION DEFINED value, \( \text{Log}_2 \text{smallest implemented translation granule})

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [11:6]**

Reserved, RES0.

**PMFZ, bit [5]**

When FEAT_SPEv1p2 is implemented:

Freeze PMU on SPE event. Stop PMU event counters when PMBSR_EL1.S == 0b1.

<table>
<thead>
<tr>
<th>PMFZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze PMU event counters on Statistical Profiling Buffer Management event.</td>
</tr>
<tr>
<td>0b1</td>
<td>Freeze PMU event counters on Statistical Profiling Buffer Management event.</td>
</tr>
</tbody>
</table>

The PMU event counters affected by this control is controlled by PMCR_EL0.FZS and, if EL2 is implemented, MDCR_EL2.HPMFZS. See the descriptions of these control bits for more information.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**Bits [4:3]**

Reserved, RES0.

**FM, bits [2:1]**

Fill mode.

<table>
<thead>
<tr>
<th>FM</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Fill mode. Stop collection and raise maintenance interrupt on buffer fill.</td>
<td>When FEAT_SPEv1p2 is implemented</td>
</tr>
<tr>
<td>0b10</td>
<td>Discard mode. All output is discarded.</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**E, bit [0]**

Profiling Buffer enable

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All output is discarded.</td>
</tr>
<tr>
<td>0b1</td>
<td>Profiling buffer enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the PMBLIMITR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, PMBLIMITR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMBLIMITR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.E2PB == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        AAarch64.SystemAccessTrap(EL3, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        return NVMem[0x800];
    else
        return PMBLIMITR_EL1;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return PMBLIMITR_EL1;
    endif
elsif PSTATE.EL == EL3 then
    return PMBLIMITR_EL1;
else
    return PMBLIMITR_EL1;
endif

MSR PMBLIMITR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMBLIMITR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.E2PB == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        NVMem[0x800] = X[t];
    else
        PMBLIMITER_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        PMBLIMITER_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    PMBLIMITER_EL1 = X[t];
PMBPTR_EL1, Profiling Buffer Write Pointer Register

The PMBPTR_EL1 characteristics are:

**Purpose**

Defines the current write pointer for the profiling buffer.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMBPTR_EL1 are UNDEFINED.

**Attributes**

PMBPTR_EL1 is a 64-bit register.

**Field descriptions**

The PMBPTR_EL1 bit assignments are:

```
63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
| PTR | PTR |
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
```

**PTR, bits [63:0]**

Current write address. Defines the virtual address of the next entry to be written to the buffer.

The architecture places restrictions on the values software can write to the pointer. For more information see 'Restrictions on the current write pointer'.

**Note**

As a result, an implementation might treat some of bits[M:0], where M is defined by PMBIDR_EL1.Align, as RES0.

On a management interrupt, PMBPTR_EL1 is frozen.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMBPTR_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, PMBPTR_EL1
```

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMBPTR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.E2PB == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    return NVMem[0x810];
  else
    return PMBPTR_EL1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return PMBPTR_EL1;
  endif
elsif PSTATE.EL == EL3 then
  return PMBPTR_EL1;
endif

MSR PMBPTR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMBPTR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.E2PB == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && EDSCR.SDD == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elseif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        NVMem[0x810] = X[t];
    else
        PMBPTR_EL1 = X[t];
    endif
else
    PMBPTR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elseif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elseif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        PMBPTR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    PMBPTR_EL1 = X[t];
else
    PMBPTR_EL1 = X[t];
end
**PMBSR_EL1, Profiling Buffer Status/syndrome Register**

The PMBSR_EL1 characteristics are:

**Purpose**

Provides syndrome information to software when the buffer is disabled because the management interrupt has been raised.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMBSR_EL1 are UNDEFINED.

**Attributes**

PMBSR_EL1 is a 64-bit register.

**Field descriptions**

The PMBSR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>EC bits [31:26]</td>
<td>Exception class</td>
</tr>
<tr>
<td>Top-level description of the cause of the buffer management event</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>EC</th>
<th>Meaning</th>
<th>MSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Other buffer management event. All buffer management events other than those described by other defined Exception class codes.</td>
<td><strong>MSS encoding for other buffer management events</strong></td>
</tr>
<tr>
<td>0b011111</td>
<td>Buffer management event for an IMPLEMENTATION DEFINED reason.</td>
<td><strong>MSS encoding for a buffer management event for an IMPLEMENTATION DEFINED reason</strong></td>
</tr>
<tr>
<td>0b100100</td>
<td>Stage 1 Data Abort on write to Profiling Buffer.</td>
<td><strong>MSS encoding for stage 1 or stage 2 Data Aborts on write to buffer</strong></td>
</tr>
<tr>
<td>0b100101</td>
<td>Stage 2 Data Abort on write to Profiling Buffer.</td>
<td><strong>MSS encoding for stage 1 or stage 2 Data Aborts on write to buffer</strong></td>
</tr>
</tbody>
</table>

All other values are reserved. Reserved values might be defined in a future version of the architecture.
Writing a reserved value to this field will make the value of this field **UNKNOWN**. Values that are not supported act as reserved values when writing to this register.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [25:20]**

Reserved, **RES0**.

**DL, bit [19]**

Partial record lost.

Following a buffer management event other than an asynchronous External abort, indicates whether the last record written to the Profiling Buffer is complete.

<table>
<thead>
<tr>
<th>DL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PMBPTR_EL1 points to the first byte after the last complete record written to the Profiling Buffer.</td>
</tr>
<tr>
<td>0b1</td>
<td>Part of a record was lost because of a buffer management event or synchronous External abort. PMBPTR_EL1 might not point to the first byte after the last complete record written to the buffer, and so restarting collection might result in a data record stream that software cannot parse. All records prior to the last record have been written to the buffer.</td>
</tr>
</tbody>
</table>

When the buffer management event was because of an asynchronous external abort, this bit is set to 1 and software must not assume that any valid data has been written to the Profiling Buffer.

This bit is **RES0** if the PE never sets this bit as a result of a buffer management event caused by an asynchronous External abort.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EA, bit [18]**

External abort.

<table>
<thead>
<tr>
<th>EA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An external abort has not been asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>An external abort has been asserted and detected by the Statistical Profiling Extension.</td>
</tr>
</tbody>
</table>

This bit is **RES0** if the PE never sets this bit as the result of an External abort.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**S, bit [17]**

Service

<table>
<thead>
<tr>
<th>S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PMBIRO is not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMBIRO is asserted. All profiling data has either been written to the buffer or discarded.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**COLL, bit [16]**

Collision detected.

<table>
<thead>
<tr>
<th>COLL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No collision events detected.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one collision event was recorded.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**MSS, bits [15:0]**

Management Event Specific Syndrome.
Contains syndrome specific to the management event.
The syndrome contents for each management event are described in the following sections.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**MSS encoding for stage 1 or stage 2 Data Aborts on write to buffer**

| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RES0 | FSC |

**Bits [15:6]**

Reserved, RES0.

**FSC, bits [5:0]**

Fault status code
<table>
<thead>
<tr>
<th>FSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault, level 0 of</td>
<td></td>
</tr>
<tr>
<td></td>
<td>translation or translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001000</td>
<td>Access flag fault, level 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When FEAT_LPA2 is implemented</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Permission fault, level 0.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>When FEAT_LPA2 is implemented</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk or hardware update of translation table.</td>
<td></td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous External abort.</td>
<td></td>
</tr>
<tr>
<td>0b010011</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented</td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 0.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk or hardware update of translation table, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011001</td>
<td>Synchronous parity or ECC error on memory access on translation table walk or hardware update of translation table, level -1.</td>
<td>When FEAT_LPA2 is implemented and FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b100000</td>
<td>Alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b100100</td>
<td>Address size fault, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b101001</td>
<td>Translation fault, level -1.</td>
<td></td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b110001</td>
<td>Unsupported atomic hardware update fault.</td>
<td>When FEAT_HAFDBS is implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

It is IMPLEMENTATION DEFINED whether each of the Access Flag fault, asynchronous External abort and synchronous External abort, Alignment fault, and TLB Conflict abort values can be generated by the PE. For more information see 'Faults and Watchpoints'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
MSS encoding for other buffer management events

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>BSC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [15:6]

Reserved, RES0.

BSC, bits [5:0]

Buffer status code

<table>
<thead>
<tr>
<th>BSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Buffer not filled</td>
</tr>
<tr>
<td>0b000001</td>
<td>Buffer filled</td>
</tr>
</tbody>
</table>

All other values are reserved. Reserved values might be defined in a future version of the architecture.

Writing a reserved value to this field will make the value of this field UNKNOWN. Values that are not supported act as reserved values when writing to this register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

MSS encoding for a buffer management event for an IMPLEMENTATION DEFINED reason

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

IMPLEMENTATION DEFINED, bits [15:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the PMBSR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PMBSR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMBSR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.E2PB == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        return NVMem[0x820];
    else
        return PMBSR_EL1;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return PMBSR_EL1;
    endif
elsif PSTATE.EL == EL3 then
    return PMBSR_EL1;
else
    return PMBSR_EL1;
endif

MSR PMBSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '0' & MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HDFGWTR_EL2.PMBSR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & MDCR_EL2.E2PB == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) & SCR_EL3.NS == '0' & MDCR_EL3.NSPB == '01' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  elsif HaveEL(EL3) & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end;
  elsif EL2Enabled() & HCR_EL2.<NV2,NV1,NV> == '1x1' then
    NVMem[0x820] = X[t];
  else
    PMBSR_EL1 = X[t];
  elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '0' & MDCR_EL3.NSPB != '01' then
      UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
      UNDEFINED;
    elsif HaveEL(EL3) & SCR_EL3.NS == '0' & MDCR_EL3.NSPB != '01' then
      if Halted() & EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end;
    elsif HaveEL(EL3) & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
      if Halted() & EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end;
    else
      PMBSR_EL1 = X[t];
  elsif PSTATE.EL == EL3 then
    PMBSR_EL1 = X[t];
**PMCCFILTR_EL0, Performance Monitors Cycle Count Filter Register**

The PMCCFILTR_EL0 characteristics are:

**Purpose**

Determines the modes in which the Cycle Counter, PMCCNTR_EL0, increments.

**Configuration**

AArch64 System register PMCCFILTR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCCFILTR[31:0].

AArch64 System register PMCCFILTR_EL0 bits [31:0] are architecturally mapped to External register PMCCFILTR_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCCFILTR_EL0 are UNDEFINED.

**Attributes**

PMCCFILTR_EL0 is a 64-bit register.

**Field descriptions**

The PMCCFILTR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| P  | U  | NSK| NSU| M  | RES0|     | RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**Bits [63:32]**

Reserved, RES0.

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMCCFILTR_EL0.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMCCFILTR_EL0.NSU bit.
Meaning

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NSK, bit [29]**

*When EL3 is implemented:*

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of the **PMCCFILTR_EL0.P** bit, cycles in Non-secure EL1 are counted.

Otherwise, cycles in Non-secure EL1 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**NSU, bit [28]**

*When EL3 is implemented:*

Non-secure EL0 (Unprivileged) filtering bit. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of the **PMCCFILTR_EL0.U** bit, cycles in Non-secure EL0 are counted.

Otherwise, cycles in Non-secure EL0 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**NSH, bit [27]**

*When EL2 is implemented:*

EL2 (Hypervisor) filtering bit. Controls counting in EL2.

If Secure EL2 is implemented, and EL3 is implemented, counting in Secure EL2 is further controlled by the **PMCCFILTR_EL0.SH** bit.

<table>
<thead>
<tr>
<th>NSH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not count cycles in EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count cycles in EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**M, bit [26]**

*When EL3 is implemented:*

Secure EL3 filtering bit.
If the value of this bit is equal to the value of the PMCCFILTR_EL0.P bit, cycles in Secure EL3 are counted.

Otherwise, cycles in Secure EL3 are not counted.

Most applications can ignore this field and set its value to 0.

**Note**

This field is not visible in the AArch32 PMCCFILTR System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bit [25]**

Reserved, RES0.

**SH, bit [24]**

When FEAT_SEL2 is implemented and EL3 is implemented:

Secure EL2 filtering.

If the value of this bit is not equal to the value of the PMCCFILTR_EL0.NSH bit, cycles in Secure EL2 are counted.

Otherwise, cycles in Secure EL2 are not counted.

If Secure EL2 is disabled, this field is RES0.

**Note**

This field is not visible in the AArch32 PMCCFILTR System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [23:0]**

Reserved, RES0.

**Accessing the PMCCFILTR_EL0**

PMCCFILTR_EL0 can also be accessed by using PMXEVTYP Hiệp with PMSER SEL set to 0b1111.

Accesses to this register use the following encodings:

**MRS <Xt>, PMCCFILTR_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b1111</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  end
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '1' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMCCFILTR_EL0 == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return PMCCFILTR_EL0;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HDFGRTR_EL2.PMCCFILTR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return PMCCFILTR_EL0;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
else
  return PMCCFILTR_EL0;
elsif PSTATE.EL == EL3 then
  return PMCCFILTR_EL0;
end

MSR PMCCFILTR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b1111</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    else
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMCCFILTR_EL0 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
        else
            PMCCFILTR_EL0 = X[t];
        end if
    end if
else
    PMCCFILTR_EL0 = X[t];
end if

if PSTATE_EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        PMCCFILTR_EL0 = X[t];
    end if
else
    PMCCFILTR_EL0 = X[t];
end if

if PSTATE_EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        PMCCFILTR_EL0 = X[t];
    end if
else
    PMCCFILTR_EL0 = X[t];
end if
PMCCNTR_EL0, Performance Monitors Cycle Count Register

The PMCCNTR_EL0 characteristics are:

**Purpose**

Holds the value of the processor Cycle Counter, CCNT, that counts processor clock cycles. See 'Time as measured by the Performance Monitors cycle counter' for more information.

PMCCFILTR_EL0 determines the modes and states in which the PMCCNTR_EL0 can increment.

**Configuration**

AArch64 System register PMCCNTR_EL0 bits [63:0] are architecturally mapped to AArch32 System register PMCCNTR[63:0].

AArch64 System register PMCCNTR_EL0 bits [63:0] are architecturally mapped to External register PMCCNTR_EL0[63:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCCNTR_EL0 are UNDEFINED.

All counters are subject to any changes in clock frequency, including clock stopping caused by the WFI and WFE instructions. This means that it is **CONSTRAINED UNPREDICTABLE** whether or not PMCCNTR_EL0 continues to increment when clocks are stopped by WFI and WFE instructions.

**Attributes**

PMCCNTR_EL0 is a 64-bit register.

**Field descriptions**

The PMCCNTR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CCNT</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
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<td>2</td>
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<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**CCNT, bits [63:0]**

Cycle count. Depending on the values of PMCR_EL0.{LC,D}, this field increments in one of the following ways:

- Every processor clock cycle.
- Every 64th processor clock cycle.

Writing 1 to PMCR_EL0.C sets this field to 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMCCNTR_EL0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.<CR,EN> == '00' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      return PMCCNTR_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMCCNTR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCCNTR_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCCNTR_EL0;
  end
elsif PSTATE.EL == EL3 then
  return PMCCNTR_EL0;
else
  MSR PMCCNTR_EL0, <Xt>
end

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMCCNTR_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif PMCCNTR_EL0 = X[t];
else if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() || HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elseif PMCCNTR_EL0 = X[t];
else if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elseif PMCCNTR_EL0 = X[t];
else if PSTATE.EL == EL3 then
    PMCCNTR_EL0 = X[t];
The PMCEID0_EL0 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the ranges 0x0000 to 0x001F and 0x4000 to 0x401F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

---

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

---

For more information about the common events and the use of the PMCID<n>_EL0 registers see 'The PMU event number space and common events'.

**Configuration**

AArch64 System register PMCEID0_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCEID0[31:0].

AArch64 System register PMCEID0_EL0 bits [63:32] are architecturally mapped to AArch32 System register PMCEID2[31:0].

AArch64 System register PMCEID0_EL0 bits [31:0] are architecturally mapped to External register PMCEID0[31:0].

AArch64 System register PMCEID0_EL0 bits [63:32] are architecturally mapped to External register PMCEID2[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCEID0_EL0 are UNDEFINED.

**Attributes**

PMCEID0_EL0 is a 64-bit register.

**Field descriptions**

The PMCEID0_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>IDhi&lt;n&gt;, bit [n+32], for n = 31 to 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ID31</td>
</tr>
<tr>
<td>31</td>
</tr>
</tbody>
</table>

When FEAT_PMUv3p1 is implemented:

IDhi[n] corresponds to common event (0x4000 + n).

For each bit:
A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n>_EL0 registers of that earlier version of the PMU architecture.

### Otherwise:

Reserved, RES0.

**ID<n>, bit [n], for n = 31 to 0**

ID[n] corresponds to common event n.

For each bit:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n>_EL0 registers of that earlier version of the PMU architecture.

### Accessing the PMCEID0_EL0

Accesses to this register use the following encodings:

**MRS <Xt>, PMCEID0_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  else
    if EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      return PMCEID0_EL0;
    end if
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return PMCEID0_EL0;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return PMCEID0_EL0;
  end if
elsif PSTATE.EL == EL3 then
  return PMCEID0_EL0;
end if
PMCEID1_EL0, Performance Monitors Common Event Identification register 1

The PMCEID1_EL0 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the ranges 0x0020 to 0x003F and 0x4020 to 0x403F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

For more information about the common events and the use of the PMCEID<n>_EL0 registers see 'The PMU event number space and common events'.

**Configuration**

AArch64 System register PMCEID1_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCEID1[31:0].

AArch64 System register PMCEID1_EL0 bits [63:32] are architecturally mapped to AArch32 System register PMCEID3[31:0].

AArch64 System register PMCEID1_EL0 bits [31:0] are architecturally mapped to External register PMCEID1[31:0].

AArch64 System register PMCEID1_EL0 bits [63:32] are architecturally mapped to External register PMCEID3[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCEID1_EL0 are UNDEFINED.

**Attributes**

PMCEID1_EL0 is a 64-bit register.

**Field descriptions**

The PMCEID1_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
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</thead>
<tbody>
<tr>
<td>Dhi31</td>
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</tr>
</tbody>
</table>

IDhi<n>, bit [n+32], for n = 31 to 0

When FEAT_PMUv3p1 is implemented:

IDhi[n] corresponds to common event (0x4020 + n).

For each bit:
IDhi<n> | Meaning
---|---
0b0 | The common event is not implemented, or not counted.
0b1 | The common event is implemented.

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n>_EL0 registers of that earlier version of the PMU architecture.

Otherwise:

Reserved, RES0.

ID<n>, bit [n], for n = 31 to 0

ID[n] corresponds to common event (0x0020 + n).

For each bit:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n>_EL0 registers of that earlier version of the PMU architecture.

**Accessing the PMCEID1_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, PMCEID1_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCEID1_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCEID1_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCEID1_EL0;
  end
elsif PSTATE.EL == EL3 then
  return PMCEID1_EL0;
The PMCNTENCLR_EL0 characteristics are:

**Purpose**

Disables the Cycle Count Register, PMCCNTR_EL0, and any implemented event counters PMEVCNTR<n>. Reading this register shows which counters are enabled.

**Configuration**

AArch64 System register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCNTENCLR[31:0].

AArch64 System register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to External register PMCNTENCLR_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCNTENCLR_EL0 are UNDEFINED.

**Attributes**

PMCNTENCLR_EL0 is a 64-bit register.

**Field descriptions**

The PMCNTENCLR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:32]**

Reserved, RES0.

**C, bit [31]**

**PMCCNTR_EL0** disable bit. Disables the cycle counter register. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, disables the cycle counter.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter disable bit for PMEVCNTR<n>_EL0.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.
Meaning

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 is enabled. When written, disables PMEVCNTR&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the PMCNTENCLR_EL0

Accesses to this register use the following encodings:

\[
MRS <Xt>, PMCNTENCLR_EL0
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b11</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elseif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMCNTEN == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCNTENCLR_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCNTENCLR_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCNTENCLR_EL0;
  end
elsif PSTATE.EL == EL3 then
  return PMCNTENCLR_EL0;
elsif PSTATE.EL == EL3 then
  return PMCNTENCLR_EL0;
```

Page 1263
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    end
    else
      PMCNTENCLR_EL0 = X[t];
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMCNTENCLR_EL0 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMCNTENCLR_EL0 = X[t];
  end
elsif PSTATE.EL == EL3 then
  PMCNTENCLR_EL0 = X[t];
The PMCNTENSET_EL0 characteristics are:

**Purpose**

Enables the Cycle Count Register, **PMCCNTR_EL0**, and any implemented event counters **PMEVCNTR<n>**. Reading this register shows which counters are enabled.

**Configuration**

AArch64 System register PMCNTENSET_EL0 bits [31:0] are architecturally mapped to AArch32 System register **PMCNTENSET[31:0]**.

AArch64 System register PMCNTENSET_EL0 bits [31:0] are architecturally mapped to External register **PMCNTENSET_EL0[31:0]**.

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCNTENSET_EL0 are **UNDEFINED**.

**Attributes**

PMCNTENSET_EL0 is a 64-bit register.

**Field descriptions**

The PMCNTENSET_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**Bits [63:32]**

Reserved, **RES0**.

**C, bit [31]**

**PMCCNTR_EL0** enable bit. Enables the cycle counter register. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, enables the cycle counter.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**P<n>, bit [n], for n = 30 to 0**

Event counter enable bit for **PMEVCNTR<n>_EL0**.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in **MDCR_EL2.HPMN**. Otherwise, N is the value in **PMCR_EL0.N**.
Meaning

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 event counter is enabled. When written, enables PMEVCNTR&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMCNTENSET_EL0**

Accesses to this register use the following encodings:

**MRS <Xt>, PMCNTENSET_EL0**

```plaintext
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if;
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      return PMCNTENSET_EL0;
    end if;
  elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      return PMCNTENSET_EL0;
    end if;
  elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      return PMCNTENSET_EL0;
    end if;
  elseif PSTATE.EL == EL3 then
    return PMCNTENSET_EL0;
  else
    return PMCNTENSET_EL0;
  end if;
end if;
```
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMCNTEN == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    PMCNTENSET_EL0 = X[t];
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    PMCNTENSET_EL0 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    PMCNTENSET_EL0 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  PMCNTENSET_EL0 = X[t];
end if
PMCR_EL0, Performance Monitors Control Register

The PMCR_EL0 characteristics are:

**Purpose**

Provides details of the Performance Monitors implementation, including the number of counters implemented, and configures and controls the counters.

**Configuration**

AArch64 System register PMCR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCR[31:0].

AArch64 System register PMCR_EL0 bits [7:0] are architecturally mapped to External register PMCR_EL0[7:0].

This register is present only when FEAT_PMUV3 is implemented. Otherwise, direct accesses to PMCR_EL0 are UNDEFINED.

**Attributes**

PMCR_EL0 is a 64-bit register.

**Field descriptions**

The PMCR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>IMP</th>
<th>IDCODE</th>
<th>N</th>
<th>RES0</th>
<th>FZS</th>
<th>RES0</th>
<th>FZS</th>
<th>RES0</th>
<th>LP</th>
<th>LC</th>
<th>DP</th>
<th>X</th>
<th>D</th>
<th>C</th>
<th>P</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
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<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
<td>RES0</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td></td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>FZS</td>
</tr>
</tbody>
</table>

**Bits [63:33]**

Reserved, RES0.

**FZS, bit [32]**

**When FEAT_SPEv1p2 is implemented:**

Freeze-on-SPE event. Stop counters when PMBLIMITR_EL1.(PMFZ,E) == (1,1) and PMBSR_EL1.S == 0b1.

<table>
<thead>
<tr>
<th>FZS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on Statistical Profiling Buffer Management event.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters do not count following a Statistical Profiling Buffer Management event.</td>
</tr>
</tbody>
</table>

If EL2 is implemented, then:

- This bit affects the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)].
- If MDCR_EL2.HPMN is less than PMCR_EL0.N:
  - This bit does not affect the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].
- This applies even when EL2 is disabled in the current Security state.

This bit does not affect the operation of PMCCNTR_EL0.

On a Warm reset, when AArch32 is supported at any Exception level, this field resets to 0.

On a Warm reset, when the implementation only supports execution in AArch64 state, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**IMP, bits [31:24]**

When FEAT_PMUv3p7 is not implemented:

Implementer code.

If this field is zero, then PMCR_EL0.IDCODE is RES0 and software must use MIDR_EL1 to identify the PE.

Otherwise, this field and PMCR_EL0.IDCODE identify the PMU implementation to software. The implementer codes are allocated by Arm. A non-zero value has the same interpretation as MIDR_EL1.Implementer.

Use of this field is deprecated.

This field reads as an IMPLEMENTATION DEFINED value.

Access to this field is RO.

Otherwise:

Reserved, RAZ.

**IDCODE, bits [23:16]**

When PMCR_EL0.IMP != 0x00:

Identification code. Use of this field is deprecated. This field has an IMPLEMENTATION DEFINED value.

Each implementer must maintain a list of identification codes that are specific to the implementer. A specific implementation is identified by the combination of the implementer code and the identification code.

Access to this field is RO.

Otherwise:

Reserved, RES0.

**N, bits [15:11]**

Indicates the number of event counters implemented. This value is in the range of 0b00000-0b11111. If the value is 0b00000 then only PMCCNTR_EL0 is implemented. If the value is 0b11111 PMCCNTR_EL0 and 31 event counters are implemented.

When EL2 is implemented and enabled for the current Security state, reads of this field from EL1 and EL0 return the value of MDCR_EL2.HPMN.

Access to this field is RO.

**Bit [10]**

Reserved, RES0.

**FZO, bit [9]**

When FEAT_PMUv3p7 is implemented:

Freeze-on-overflow. Stop event counters on overflow.
Meaning

0b0    Do not freeze on overflow.
0b1    Event counters do not count when PMOVsCLR_EL0[(N-1):0] is nonzero, where N is the value of MDCR_EL2.HPMN if EL2 is implemented, and PMCR_EL0.N otherwise.

If EL2 is implemented, then:

- This bit affects the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)].
- If MDCR_EL2.HPMN is less than PMCR_EL0.N:
  - This bit does not affect the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].
  - The operation of this bit ignores the values of PMOVsCLR_EL0[(PMCR_EL0.N-1):MDCR_EL2.HPMN].
- This applies even when EL2 is disabled in the current Security state.

This bit does not affect the operation of PMCCNTR_EL0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [8]

Reserved, RES0.

LP, bit [7]

When FEAT_PMUv3p5 is implemented:

Long event counter enable. Determines when unsigned overflow is recorded by a counter overflow bit.

LP

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0     Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;n&gt;_EL0[31:0].</td>
</tr>
<tr>
<td>0b1     Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;n&gt;_EL0[63:0].</td>
</tr>
</tbody>
</table>

If EL2 is implemented and MDCR_EL2.HPMN or HDCR.HPMN is less than PMCR_EL0.N, this bit does not affect the operation of event counters in the range [HDCR.HPMN ..(PMCR_EL0.N-1)] or [MDCR_EL2.HPMN ..(PMCR_EL0.N-1)].

Note

The effect of MDCR_EL2.HPMN or HDCR.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state. For more information, see the description of MDCR_EL2.HPMN or HDCR.HPMN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

LC, bit [6]

When AArch32 is supported at any Exception level:

Long cycle counter enable. Determines when unsigned overflow is recorded by the cycle counter overflow bit.
<table>
<thead>
<tr>
<th>LC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR_EL0[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR_EL0[63:0].</td>
</tr>
</tbody>
</table>

Arm deprecates use of PMCR_EL0, LC = 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.

**DP, bit [5]**

*When EL3 is implemented or (FEAT_PMUv3p1 is implemented and EL2 is implemented):*

Disable cycle counter when event counting is prohibited.

<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR_EL0 is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>When event counting for counters in the range [0,(MDCR_EL2,HPMN-1)] is prohibited, cycle counting by PMCCNTR_EL0 is disabled.</td>
</tr>
</tbody>
</table>

For more information see 'Prohibiting event counting'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**X, bit [4]**

*When the implementation includes a PMU event export bus:*

Enable export of events in an IMPLEMENTATION DEFINED PMU event export bus.

<table>
<thead>
<tr>
<th>X</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not export events.</td>
</tr>
<tr>
<td>0b1</td>
<td>Export events where not prohibited.</td>
</tr>
</tbody>
</table>

This field enables the exporting of events over an IMPLEMENTATION DEFINED PMU event export bus to another device, for example to an OPTIONAL PE trace unit.

No events are exported when counting is prohibited.

This field does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface (CTI) that can be implemented as signals exported from the PE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RAZ/WI.

**D, bit [3]**

*When AArch32 is supported at any Exception level:*

Clock divider.
Meaning

<table>
<thead>
<tr>
<th>D</th>
<th>When enabled, PMCCNTR_EL0 counts every clock cycle.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>When enabled, PMCCNTR_EL0 counts once every 64 clock cycles.</td>
</tr>
</tbody>
</table>

If PMCR_EL0.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.

Arm deprecates use of PMCR_EL0.D = 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**C, bit [2]**

Cycle counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset PMCCNTR_EL0 to zero.</td>
</tr>
</tbody>
</table>

**Note**

Resetting PMCCNTR_EL0 does not change the cycle counter overflow bit.

The value of PMCR_EL0.LC is ignored, and bits [63:0] of all affected event counters are reset.

Access to this field is WO/RAZ.

**P, bit [1]**

Event counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset all event counters accessible in the current Exception level, not including PMCCNTR_EL0, to zero.</td>
</tr>
</tbody>
</table>

In EL0 and EL1:

- If EL2 is implemented and enabled in the current Security state, and MDCR_EL2,HPMN is less than PMCR_EL0.N, a write of 1 to this bit does not reset event counters in the range [MDCR_EL2,HPMN..(PMCR_EL0.N-1)].
- If EL2 is not implemented, EL2 is disabled in the current Security state, or MDCR_EL2,HPMN equals PMCR_EL0.N, a write of 1 to this bit resets all the event counters.

In EL2 and EL3, a write of 1 to this bit resets all the event counters.

**Note**

Resetting the event counters does not change the event counter overflow bits.

If FEAT_PMUv3p5 is implemented, the values of MDCR_EL2,HLP and PMCR_EL0.LP are ignored, and bits [63:0] of all affected event counters are reset.

Access to this field is WO/RAZ.

**E, bit [0]**

Enable.
### PMCR_EL0, Performance Monitors Control Register

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All event counters in the range ([0..(PMN-1)]) and PMCCNTR_EL0 are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>All event counters in the range ([0..(PMN-1)]) and PMCCNTR_EL0 are enabled by PMCNTENSET_EL0.</td>
</tr>
</tbody>
</table>

If EL2 is implemented, then:

- If EL2 is using AArch32, PMN is `HDCR.HPMN`.
- If EL2 is using AArch64, PMN is `MDCR_EL2.HPMN`.
- If PMN is less than PMCR_EL0.N, this bit does not affect the operation of event counters in the range \([PMN..(PMCR_EL0.N-1)]\).

If EL2 is not implemented, PMN is PMCR_EL0.N.

**Note**

The effect of `MDCR_EL2.HPMN` or `HDCR.HPMN` on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state. For more information, see the description of `MDCR_EL2.HPMN` or `HDCR.HPMN`.

On a Warm reset, this field resets to 0.

### Accessing the PMCR_EL0

Accesses to this register use the following encodings:

\[
\text{MRS } \langle Xt \rangle, \text{ PMCR_EL0}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMCR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCR_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMCR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCR_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMCR_EL0;
  end
elsif PSTATE.EL == EL3 then
  return PMCR_EL0;
else
  MSR PMCR_EL0, <Xt>
if PSTATE.EL == EL0 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() & HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    endif
    EL2Enabled() & HCR_EL2.<E2H,TGE> != '11' & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HDFGWTR_EL2.PMCR_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & MDCR_EL2.TPMCR == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) & MDCR_EL3.TPM == '1' then
      if Halted() & EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      endif
    else
      PMCR_EL0 = X[t];
  endif
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & MDCR_EL2.TPMCR == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) & MDCR_EL3.TPM == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    PMCR_EL0 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) & MDCR_EL3.TPM == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    PMCR_EL0 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  PMCR_EL0 = X[t];
PMEVCNTR<n>_EL0, Performance Monitors Event Count Registers, n = 0 - 30

The PMEVCNTR<n>_EL0 characteristics are:

Purpose

Holds event counter n, which counts events, where n is 0 to 30.

Configuration

AArch64 System register PMEVCNTR<n>_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMEVCNTR<n>[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMEVCNTR<n>_EL0 are UNDEFINED.

Attributes

PMEVCNTR<n>_EL0 is a 64-bit register.

Field descriptions

The PMEVCNTR<n>_EL0 bit assignments are:

When FEAT_PMUv3p5 is implemented:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
<th>Event counter n</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>Event counter n</td>
</tr>
</tbody>
</table>

Bits [63:0]

Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>Event counter n</td>
</tr>
</tbody>
</table>

Bits [63:32]

Reserved, RES0.

Bits [31:0]

Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMEVCNTR<n>_EL0**

PMEVCNTR<n>_EL0 can also be accessed by using PMXEVCNTR_EL0 with PMSELR_EL0.SEL set to the value of <n>.

If FEAT_FGT is implemented and <n> is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMEVCNTR<n>_EL0 is as follows:

- If <n> is an unimplemented event counter, the access is **UNDEFINED**.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and <n> is greater than or equal to the number of accessible counters, then reads and writes of PMEVCNTR<n>_EL0 are **CONSTRAINED UNPREDICTABLE**, and the following behaviors are permitted:

- Accesses to the register are **UNDEFINED**.
- Accesses to the register behave as RAZ/WI.
- Accesses to the register execute as a **NOP**.
- If EL2 is implemented and enabled in the current Security state, and <n> is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

**Note**

In EL0, an access is permitted if it is enabled by PMUSERENR_EL0.{ER,EN}.

If EL2 is implemented and enabled in the current Security state, in EL1 and EL0, MDCR_EL2.HPMN identifies the number of accessible event counters. Otherwise, the number of accessible event counters is the number of implemented event counters. See MDCR_EL2.HPMN for more details.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b10:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.<ER,EN> == '00' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '01' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMEVCNTRn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)];
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsifHaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)];
  end if;
elsif PSTATE.EL == EL3 then
  return PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)];
end if;

MSR PMEVCNTR<n>_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b10:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR_SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    endMessage;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMEVCNTRn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endMessage;
  else
    PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)] = X[t];
  endMessage;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR_SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMEVCNTRn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endMessage;
  else
    PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)] = X[t];
  endMessage;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR_SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endMessage;
  else
    PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)] = X[t];
  endMessage;
elsif PSTATE.EL == EL3 then
  PMEVCNTR_EL0[UInt(CRm<1:0>:op2<2:0>)] = X[t];
PMEVTYPER<n>_EL0, Performance Monitors Event Type Registers, n = 0 - 30

The PMEVTYPER<n>_EL0 characteristics are:

**Purpose**

Configures event counter n, where n is 0 to 30.

**Configuration**

AArch64 System register PMEVTYPER<n>_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMEVTYPER<n>[31:0].

AArch64 System register PMEVTYPER<n>_EL0 bits [31:0] are architecturally mapped to External register PMEVTYPER<n>_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMEVTYPER<n>_EL0 are UNDEFINED.

**Attributes**

PMEVTYPER<n>_EL0 is a 64-bit register.

**Field descriptions**

The PMEVTYPER<n>_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| P   | U   | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSK | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH | NSH |
| RES0| evtCount[15:10] | evtCount[9:0] |

**Bits [63:32]**

Reserved, RES0.

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMEVTYPER<n>_EL0.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Count events in EL1.</td>
</tr>
<tr>
<td>1</td>
<td>Do not count events in EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMEVTYPER<n>_EL0.NSU bit.
**NSK, bit [29]**

When EL3 is implemented:

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of the PMEVTYPER<\(n\)>_EL0.P bit, events in Non-secure EL1 are counted. Otherwise, events in Non-secure EL1 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**NSU, bit [28]**

When EL3 is implemented:

Non-secure EL0 (Unprivileged) filtering bit. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of the PMEVTYPER<\(n\)>_EL0.U bit, events in Non-secure EL0 are counted. Otherwise, events in Non-secure EL0 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**NSH, bit [27]**

When EL2 is implemented:

EL2 (Hypervisor) filtering bit. Controls counting in EL2.

If Secure EL2 is implemented, and EL3 is implemented, counting in Secure EL2 is further controlled by the PMEVTYPER<\(n\)>_EL0.SH bit.

**NSH**

<table>
<thead>
<tr>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**M, bit [26]**

When EL3 is implemented:

Secure EL3 filtering bit.
If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.P bit, events in Secure EL3 are counted. Otherwise, events in Secure EL3 are not counted.

Most applications can ignore this field and set its value to 0b0.

**Note**

This field is not visible in the AArch32 PMEVTYPER<n> System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**MT, bit [25]**

When FEAT_MTPMU is implemented or an IMPLEMENTATION DEFINED multi-threaded PMU extension is implemented:

Multithreading.

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events only on controlling PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count events from any PE with the same affinity at level 1 and above as this PE.</td>
</tr>
</tbody>
</table>

From Armv8.6, the IMPLEMENTATION DEFINED multi-threaded PMU extension is not permitted, meaning if FEAT_MTPMU is not implemented, this bit is RES0. See ID_AA64DFR0_EL1.MTPMU.

This bit is ignored by the PE and treated as zero when FEAT_MTPMU is implemented and Disabled.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**SH, bit [24]**

When FEAT_SEL2 is implemented and EL3 is implemented:

Secure EL2 filtering.

If the value of this bit is not equal to the value of the PMEVTYPER<n>_EL0.NSH bit, events in Secure EL2 are counted.

Otherwise, events in Secure EL2 are not counted.

**Note**

This field is not visible in the AArch32 PMEVTYPER<n> System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
Bits [23:16]

Reserved, RES0.

evtCount[15:10], bits [15:10]

When FEAT_PMUv3p1 is implemented:

Extension to evtCount[9:0]. See evtCount[9:0] for more details.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

evtCount[9:0], bits [9:0]

Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.

Software must program this field with an event that is supported by the PE being programmed.

The ranges of event numbers allocated to each type of event are shown in ‘Allocation of the PMU event number space’.

If evtCount is programmed to an event that is reserved or not supported by the PE, the behavior depends on the value written:

- For the range 0x0000 to 0x003F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- If 16-bit evtCount is implemented, for the range 0x4000 to 0x403F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- For IMPLEMENTATION DEFINED events, it is UNPREDICTABLE what event, if any, is counted, and the value returned by a direct or external read of the evtCount field is UNKNOWN.

Note

UNPREDICTABLE means the event must not expose privileged information.

Arm recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the PMEVTYPER<n>_EL0

PMEVTYPER<n>_EL0 can also be accessed by using PMXVTYPER_EL0 with PMSELR_EL0 SEL set to n.

If FEAT_FGT is implemented and <n> is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMEVTYPER<n>_EL0 is as follows:

- If <n> is an unimplemented event counter, the access is UNDEFINED.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and <n> is greater than or equal to the number of accessible counters, then reads and writes of PMEVTYPER<n>_EL0 are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

- Accesses to the register are UNDEFINED.
- Accesses to the register behave as RAZ/WI.
- Accesses to the register execute as a NOP.
- If EL2 is implemented and enabled in the current Security state, and <n> is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

Note
In EL0, an access is permitted if it is enabled by `PMUSERENR_EL0.EN`.

If EL2 is implemented and enabled in the current Security state, in EL1 and EL0, `MDCR_EL2.HPMN` identifies the number of accessible event counters. Otherwise, the number of accessible event counters is the number of implemented event counters. See `MDCR_EL2.HPMN` for more details.

Accesses to this register use the following encodings:

MRS <Xt>, PMEVTYPER<n>_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1110</td>
<td>0b11:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
UNDEFINED;
else if PMUSERENR_EL0.EN == '0' then
if EL2Enabled() && HCR_EL2.TGE == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
else
AArch64.SystemAccessTrap(EL1, 0x18);
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
else
return PMEVTYPER_EL0[UInt(CRm<1:0>:op2<2:0>)];
elsif PSTATE.EL == EL1 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
UNDEFINED;
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMEVTYPERn_EL0 == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
else
return PMEVTYPER_EL0[UInt(CRm<1:0>:op2<2:0>)];
elsif PSTATE.EL == EL2 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
UNDEFINED;
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
else
return PMEVTYPER_EL0[UInt(CRm<1:0>:op2<2:0>)];
elsif PSTATE.EL == EL3 then
return PMEVTYPER_EL0[UInt(CRm<1:0>:op2<2:0>)];
if PSTATE.EL == EL0 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() & MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
        elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            if Halted() & SCR_EL3.FGTEn == '1' & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
            elsif PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    elsif PSTATE.EL == EL1 then
        if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            if Halted() & SCR_EL3.FGTEn == '1' & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
            elsif PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    elsif PSTATE.EL == EL2 then
        if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            if Halted() & SCR_EL3.FGTEn == '1' then
                UNDEFINED;
            end if
            elsif PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    elsif PSTATE.EL == EL3 then
        PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    elsif PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    elsif PSTATE.EL == EL3 then
        PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
    else
        PMEVTPYER_EL0[UInt(CRm<1:0>:op2<2:0>)] == X[t];
PMINTENCLR_EL1, Performance Monitors Interrupt Enable Clear register

The PMINTENCLR_EL1 characteristics are:

**Purpose**

Disables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR_EL0, and the event counters PMEVCNTR<n>_EL0. Reading the register shows which overflow interrupt requests are enabled.

**Configuration**

AArch64 System register PMINTENCLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register PMINTENCLR[31:0].

AArch64 System register PMINTENCLR_EL1 bits [31:0] are architecturally mapped to External register PMINTENCLR_EL1[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMINTENCLR_EL1 are UNDEFINED.

**Attributes**

PMINTENCLR_EL1 is a 64-bit register.

**Field descriptions**

The PMINTENCLR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits 63:32</th>
<th>Meaning</th>
</tr>
</thead>
</table>

**Bits [63:32]**

Reserved, RES0.

**C, bit [31]**

PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.</td>
</tr>
</tbody>
</table>

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow interrupt request disable bit for PMEVCNTR<n>_EL0.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.
Meaning

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the <code>PMEVCNTR&lt;n&gt;_EL0</code> event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the <code>PMEVCNTR&lt;n&gt;_EL0</code> event counter interrupt request is enabled. When written, disables the <code>PMEVCNTR&lt;n&gt;_EL0</code> interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the PMINTENCLR_EL1

Accesses to this register use the following encodings:

**MRS <Xt>, PMINTENCLR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMINTEN == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return PMINTENCLR_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return PMINTENCLR_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return PMINTENCLR_EL1;
else
    return PMINTENCLR_EL1;
end if;
```

**MSR PMINTENCLR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMINTEN == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        PMINTENCLR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        PMINTENCLR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    PMINTENCLR_EL1 = X[t];
PMINTENSET_EL1, Performance Monitors Interrupt Enable Set register

The PMINTENSET_EL1 characteristics are:

**Purpose**

Enables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR_EL0, and the event counters PMEVCNTR<_n>_EL0. Reading the register shows which overflow interrupt requests are enabled.

**Configuration**

AArch64 System register PMINTENSET_EL1 bits [31:0] are architecturally mapped to AArch32 System register PMINTENSET[31:0].

AArch64 System register PMINTENSET_EL1 bits [31:0] are architecturally mapped to External register PMINTENSET_EL1[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMINTENSET_EL1 are UNDEFINED.

**Attributes**

PMINTENSET_EL1 is a 64-bit register.

**Field descriptions**

The PMINTENSET_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>C</td>
</tr>
<tr>
<td>61</td>
<td>P_30</td>
</tr>
<tr>
<td>60</td>
<td>P_29</td>
</tr>
<tr>
<td>59</td>
<td>P_28</td>
</tr>
<tr>
<td>58</td>
<td>P_27</td>
</tr>
<tr>
<td>57</td>
<td>P_26</td>
</tr>
<tr>
<td>56</td>
<td>P_25</td>
</tr>
<tr>
<td>55</td>
<td>P_24</td>
</tr>
<tr>
<td>54</td>
<td>P_23</td>
</tr>
<tr>
<td>53</td>
<td>P_22</td>
</tr>
<tr>
<td>52</td>
<td>P_21</td>
</tr>
<tr>
<td>51</td>
<td>P_20</td>
</tr>
<tr>
<td>50</td>
<td>P_19</td>
</tr>
<tr>
<td>49</td>
<td>P_18</td>
</tr>
<tr>
<td>48</td>
<td>P_17</td>
</tr>
<tr>
<td>47</td>
<td>P_16</td>
</tr>
<tr>
<td>46</td>
<td>P_15</td>
</tr>
<tr>
<td>45</td>
<td>P_14</td>
</tr>
<tr>
<td>44</td>
<td>P_13</td>
</tr>
<tr>
<td>43</td>
<td>P_12</td>
</tr>
<tr>
<td>42</td>
<td>P_11</td>
</tr>
<tr>
<td>41</td>
<td>P_10</td>
</tr>
<tr>
<td>40</td>
<td>P_9</td>
</tr>
<tr>
<td>39</td>
<td>P_8</td>
</tr>
<tr>
<td>38</td>
<td>P_7</td>
</tr>
<tr>
<td>37</td>
<td>P_6</td>
</tr>
<tr>
<td>36</td>
<td>P_5</td>
</tr>
<tr>
<td>35</td>
<td>P_4</td>
</tr>
<tr>
<td>34</td>
<td>P_3</td>
</tr>
<tr>
<td>33</td>
<td>P_2</td>
</tr>
<tr>
<td>32</td>
<td>P_1</td>
</tr>
<tr>
<td>31</td>
<td>P_0</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>29</td>
<td>C</td>
</tr>
<tr>
<td>28</td>
<td>P_30</td>
</tr>
<tr>
<td>27</td>
<td>P_29</td>
</tr>
<tr>
<td>26</td>
<td>P_28</td>
</tr>
<tr>
<td>25</td>
<td>P_27</td>
</tr>
<tr>
<td>24</td>
<td>P_26</td>
</tr>
<tr>
<td>23</td>
<td>P_25</td>
</tr>
<tr>
<td>22</td>
<td>P_24</td>
</tr>
<tr>
<td>21</td>
<td>P_23</td>
</tr>
<tr>
<td>20</td>
<td>P_22</td>
</tr>
<tr>
<td>19</td>
<td>P_21</td>
</tr>
<tr>
<td>18</td>
<td>P_20</td>
</tr>
<tr>
<td>17</td>
<td>P_19</td>
</tr>
<tr>
<td>16</td>
<td>P_18</td>
</tr>
<tr>
<td>15</td>
<td>P_17</td>
</tr>
<tr>
<td>14</td>
<td>P_16</td>
</tr>
<tr>
<td>13</td>
<td>P_15</td>
</tr>
<tr>
<td>12</td>
<td>P_14</td>
</tr>
<tr>
<td>11</td>
<td>P_13</td>
</tr>
<tr>
<td>10</td>
<td>P_12</td>
</tr>
<tr>
<td>9</td>
<td>P_11</td>
</tr>
<tr>
<td>8</td>
<td>P_10</td>
</tr>
<tr>
<td>7</td>
<td>P_9</td>
</tr>
<tr>
<td>6</td>
<td>P_8</td>
</tr>
<tr>
<td>5</td>
<td>P_7</td>
</tr>
<tr>
<td>4</td>
<td>P_6</td>
</tr>
<tr>
<td>3</td>
<td>P_5</td>
</tr>
<tr>
<td>2</td>
<td>P_4</td>
</tr>
<tr>
<td>1</td>
<td>P_3</td>
</tr>
<tr>
<td>0</td>
<td>P_0</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<_n>**, bit [n], for n = 30 to 0

Event count overflow interrupt request enable bit for PMEVCNTR<_n>_EL0.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.
PMINTENSET_EL1, Performance Monitors Interrupt Enable Set register

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR&lt;n&gt;_EL0 interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the PMINTENSET_EL1

Accesses to this register use the following encodings:

**MRS <Xt>, PMINTENSET_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMINTEN == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return PMINTENSET_EL1;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return PMINTENSET_EL1;
    end if;
elsif PSTATE.EL == EL3 then
    return PMINTENSET_EL1;
else
    return PMINTENSET_EL1;
end if;
```

**MSR PMINTENSET_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMINTEN == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMINTENSET_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMINTENSET_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  PMINTENSET_EL1 = X[t];
else
  PMINTENSET_EL1 = X[t];
The PMMIR_EL1 characteristics are:

**Purpose**

Describes Performance Monitors parameters specific to the implementation to software.

**Configuration**

This register is present only when FEAT_PMUv3p4 is implemented. Otherwise, direct accesses to PMMIR_EL1 are UNDEFINED.

**Attributes**

PMMIR_EL1 is a 64-bit register.

**Field descriptions**

The PMMIR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:20</td>
<td>Reserved, res0.</td>
</tr>
<tr>
<td>19:16</td>
<td>BUS_WIDTH, bits</td>
</tr>
<tr>
<td>15:12</td>
<td>BUS_SLOTS</td>
</tr>
<tr>
<td>11:0</td>
<td>SLOTS</td>
</tr>
</tbody>
</table>

**Bits [63:20]**

Reserved, res0.

**BUS_WIDTH, bits [19:16]**

*From Armv8.7*

Bus width. Indicates the number of bytes each BUS_ACCESS event relates to. Encoded as \( \log_2(\text{number of bytes}) \) plus one. Defined values are:

<table>
<thead>
<tr>
<th>BUS_WIDTH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The information is not available.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Four bytes.</td>
</tr>
<tr>
<td>0b0100</td>
<td>8 bytes.</td>
</tr>
<tr>
<td>0b0101</td>
<td>16 bytes.</td>
</tr>
<tr>
<td>0b0110</td>
<td>32 bytes.</td>
</tr>
<tr>
<td>0b0111</td>
<td>64 bytes.</td>
</tr>
<tr>
<td>0b1000</td>
<td>128 bytes.</td>
</tr>
<tr>
<td>0b1001</td>
<td>256 bytes.</td>
</tr>
<tr>
<td>0b1010</td>
<td>512 bytes.</td>
</tr>
<tr>
<td>0b1011</td>
<td>1024 bytes.</td>
</tr>
<tr>
<td>0b1100</td>
<td>2048 bytes.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Each transfer is up to this number of bytes. An access might be smaller than the bus width.

When this field is nonzero, each access counted by BUS_ACCESS is at most BUS_WIDTH bytes. An implementation might treat a wide bus as multiple narrower buses, such that a wide access on the bus increments the BUS_ACCESS counter by more than one.
Otherwise:
Reserved, RAZ.

**BUS_SLOTS, bits [15:8]**

From Armv8.7:
Bus count. The largest value by which the BUS_ACCESS event might increment by in a single BUS_CYCLES cycle.
If the information is not available, this field will read as zero.

Otherwise:
Reserved, RAZ.

**SLOTS, bits [7:0]**
Operation width. The largest value by which the STALL_SLOT event might increment by in a single cycle. If the STALL_SLOT event is not implemented, this field might read as zero.

**Accessing the PMMIR_EL1**

Accesses to this register use the following encodings:

```
MRS <Xt>, PMMIR_EL1
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
else if PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
else if EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HDFGRTR_EL2.PMMIR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else if HaveEL(EL3) & MDCR_EL3.TPM == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
else
      AArch64.SystemAccessTrap(EL3, 0x18);
else
    return PMMIR_EL1;
else if PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
else if HaveEL(EL3) & MDCR_EL3.TPM == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
else
      AArch64.SystemAccessTrap(EL3, 0x18);
else
    return PMMIR_EL1;
else if PSTATE.EL == EL3 then
  return PMMIR_EL1;
```
The PMOVSLR_EL0 characteristics are:

**Purpose**

Contains the state of the overflow bit for the Cycle Count Register, PMCCNTR_EL0, and each of the implemented event counters PMEVCNTR<n>. Writing to this register clears these bits.

**Configuration**

AArch64 System register PMOVSLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMOVSR[31:0].

AArch64 System register PMOVSLR_EL0 bits [31:0] are architecturally mapped to External register PMOVSCLR_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMOVSCLR_EL0 are UNDEFINED.

**Attributes**

PMOVSCLR_EL0 is a 64-bit register.

**Field descriptions**

The PMOVSCLR_EL0 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|

**Bits [63:32]**

Reserved, RES0.

**C, bit [31]**

Cycle counter overflow clear bit.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter has overflowed since this bit was last cleared. When written, clears the cycle counter overflow bit to 0.</td>
</tr>
</tbody>
</table>

PMCR_EL0.LC controls whether an overflow is detected from unsigned overflow of PMCCNTR_EL0[31:0] or unsigned overflow of PMCCNTR_EL0[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow clear bit for PMEVCNTR<n>_EL0.
If \( N \) is less than 31, then bits [30:\( N \)] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, \( N \) is the value in \texttt{MDCR\_EL2.\_HPMN}. Otherwise, \( N \) is the value in \texttt{PMCR\_EL0.N}.

<table>
<thead>
<tr>
<th>( P&lt;n&gt; )</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that \texttt{PMEVCNTR_n_EL0} has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that \texttt{PMEVCNTR_n_EL0} has overflowed since this bit was last cleared. When written, clears the \texttt{PMEVCNTR_n_EL0} overflow bit to 0.</td>
</tr>
</tbody>
</table>

If \texttt{FEAT\_PMUv3p5} is implemented, \texttt{MDCR\_EL2.HLP} and \texttt{PMCR\_EL0.LP} control whether an overflow is detected from unsigned overflow of \texttt{PMEVCNTR\_n\_EL0[31:0]} or unsigned overflow of \texttt{PMEVCNTR\_n\_EL0[63:0]}.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMOVSCLR\_EL0**

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{PMOVSCLR\_EL0}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMOVS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMOVSCLR_EL0;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMOVSCLR_EL0;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return PMOVSCLR_EL0;
  end
elsif PSTATE.EL == EL3 then
  return PMOVSCLR_EL0;
else
  return PMOVSCLR_EL0;
end

MSR PMOVSCLR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
   elsif PMUSERENR_EL0.EN == '0' then
      if EL2Enabled() && HCR_EL2.TGE == '1' then
         AArch64.SystemAccessTrap(EL2, 0x18);
      else
         if EL2Enabled() && HDFGWTR_EL2.PMOVS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
         else
            AArch64.SystemAccessTrap(EL1, 0x18);
         if EL2Enabled() && MDCR_EL2.TPM == '1' then
               AArch64.SystemAccessTrap(EL2, 0x18);
         else
            if EL2Enabled() && HDFGWTR_EL2.PMOVS == '1' then
               AArch64.SystemAccessTrap(EL2, 0x18);
            else
               AArch64.SystemAccessTrap(EL3, 0x18);
            if Halted() && MDCR_EL3.TPM == '1' then
               if Halted() && EDSCR.SDD == '1' then
                  UNDEFINED;
               else
                  AArch64.SystemAccessTrap(EL3, 0x18);
               else
                  PMOVSCLR_EL0 = X[t];
            elsif PSTATE.EL == EL1 then
               if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
                  UNDEFINED;
               elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
                  AArch64.SystemAccessTrap(EL2, 0x18);
               else
                  AArch64.SystemAccessTrap(EL2, 0x18);
               if Halted() && MDCR_EL3.TPM == '1' then
                  if Halted() && EDSCR.SDD == '1' then
                     UNDEFINED;
                  else
                     AArch64.SystemAccessTrap(EL3, 0x18);
                  else
                     PMOVSCLR_EL0 = X[t];
               elsif PSTATE.EL == EL2 then
                  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
                     UNDEFINED;
                  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
                     if Halted() && EDSCR.SDD == '1' then
                        UNDEFINED;
                     else
                        AArch64.SystemAccessTrap(EL3, 0x18);
                     else
                        PMOVSCLR_EL0 = X[t];
               elsif PSTATE.EL == EL3 then
                  PMOVSCLR_EL0 = X[t];
PMOVSSET_EL0, Performance Monitors Overflow Flag Status Set register

The PMOVSSET_EL0 characteristics are:

**Purpose**

Sets the state of the overflow bit for the Cycle Count Register, PMCCNTR_EL0, and each of the implemented event counters PMEVCNTR<n>.

**Configuration**

AArch64 System register PMOVSSET_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMOVSSET[31:0].

AArch64 System register PMOVSSET_EL0 bits [31:0] are architecturally mapped to External register PMOVSSET_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMOVSSET_EL0 are UNDEFINED.

**Attributes**

PMOVSSET_EL0 is a 64-bit register.

**Field descriptions**

The PMOVSSET_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:32]**

Reserved, RES0.

**C, bit [31]**

Cycle counter overflow set bit.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter has overflowed since this bit was last cleared. When written, sets the cycle counter overflow bit to 1.</td>
</tr>
</tbody>
</table>

PMCR_EL0.LC controls whether an overflow is detected from unsigned overflow of PMCCNTR_EL0[31:0] or unsigned overflow of PMCCNTR_EL0[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow set bit for PMEVCNTR<n>_EL0.
If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.

<table>
<thead>
<tr>
<th>( P^{&lt;n&gt;} )</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that \texttt{PMEVCNTR&lt;0&gt;_EL0} has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that \texttt{PMEVCNTR&lt;0&gt;_EL0} has overflowed since this bit was last cleared. When written, sets the \texttt{PMEVCNTR&lt;0&gt;_EL0} overflow bit to 1.</td>
</tr>
</tbody>
</table>

If \texttt{FEAT_PMUv3p5} is implemented, MDCR_EL2.HLP and PMCR_EL0.LP control whether an overflow is detected from unsigned overflow of \texttt{PMEVCNTR<0>_EL0}[31:0] or unsigned overflow of \texttt{PMEVCNTR<0>_EL0}[63:0].

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Accessing the PMOVSET_EL0**

Accesses to this register use the following encodings:

\[
\text{MRS <Xt>, PMOVSET_EL0}
\]

<table>
<thead>
<tr>
<th>( \text{op0} )</th>
<th>( \text{op1} )</th>
<th>( \text{CRn} )</th>
<th>( \text{CRm} )</th>
<th>( \text{op2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() \&\& HaveEL(EL3) \&\& EDSCR.SDD == '1' \&\& boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" \&\& MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() \&\& HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end
    elsif EL2Enabled() \&\& HCR_EL2.<E2H,TGE> != '11' \&\& (!HaveEL(EL3) \|\| SCR_EL3.FGTEn == '1') \&\& HDFGRTR_EL2.PMOVS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() \&\& MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) \&\& MDCR_EL3.TPM == '1' then
        if Halted() \&\& EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return PMOVSSET_EL0;
    end
elsif PSTATE.EL == EL1 then
    if Halted() \&\& HaveEL(EL3) \&\& EDSCR.SDD == '1' \&\& boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" \&\& MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() \&\& (!HaveEL(EL3) \|\| SCR_EL3.FGTEn == '1') \&\& HDFGRTR_EL2.PMOVS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() \&\& MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) \&\& MDCR_EL3.TPM == '1' then
        if Halted() \&\& EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return PMOVSSET_EL0;
    end
elsif PSTATE.EL == EL2 then
    if Halted() \&\& HaveEL(EL3) \&\& EDSCR.SDD == '1' \&\& boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" \&\& MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) \&\& MDCR_EL3.TPM == '1' then
        if Halted() \&\& EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return PMOVSSET_EL0;
    end
elsif PSTATE.EL == EL3 then
    return PMOVSSET_EL0;
end

MSR PMOVSSET_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if;
  else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMOVS == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL1, 0x18);
      end if;
    end if;
  end if;
else
  PMOVSSET_EL0 = X[t];
endif
else
  if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMOVS == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elseif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      PMOVSSET_EL0 = X[t];
    endif
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elseif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      PMOVSSET_EL0 = X[t];
    endif
  else
    if PSTATE.EL == EL3 then
      PMOVSSET_EL0 = X[t];
    endif
  endif
endif
PMSCR_EL1, Statistical Profiling Control Register (EL1)

The PMSCR_EL1 characteristics are:

**Purpose**

Provides EL1 controls for Statistical Profiling.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSCR_EL1 are **UNDEFINED**.

**Attributes**

PMSCR_EL1 is a 64-bit register.

**Field descriptions**

The PMSCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62-61</td>
<td>PCT, bits [7:6]</td>
</tr>
<tr>
<td>59-58</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>56-54</td>
<td>Bits [63:8]</td>
</tr>
</tbody>
</table>

**Bits [63:8]**

Reserved, RES0.

**PCT, bits [7:6]**

When **EL2** is implemented:

Physical Timestamp. If timestamp sampling is enabled and the Profiling Buffer is owned by EL1, requests which timestamp counter value is collected.

If FEAT_ECV is implemented, this is a two-bit field as shown. Otherwise, bit[7] is RES0.

<table>
<thead>
<tr>
<th>PCT</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Virtual timestamp. The collected timestamp is the physical counter minus the value of <strong>CNTPOFF_EL2</strong>.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Physical timestamp. The collected timestamp is the physical counter.</td>
<td></td>
</tr>
</tbody>
</table>
| 0b11 | Guest physical timestamp. The collected timestamp is the physical counter minus a physical offset. If any of the following are true, the physical offset is zero, otherwise the physical offset is the value of **CNTPOFF_EL2**:  
• SCR_EL3.ECVEn == 0b0.  
• CNTHCTL_EL2.ECV == 0b0. |

If EL2 is enabled in the current Security state, then the value of **PMSCR_EL2**.PCT might override or modify the meaning of this field.

This field is ignored by the PE when the Profiling Buffer owning Exception level is EL2.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Physical Timestamp. Reserved. This field reads as 0b01 and ignores writes. Software should treat this field as UNK/ SBZP.

When EL2 is not implemented, the Effective values of CNTVOFF_EL2 and CNTPOFF_EL2 are zero, meaning the virtual counter and physical counter have the same value.

**TS, bit [5]**

Timestamp enable.

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timestamp sampling disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timestamp sampling enabled.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE if EL2 is implemented and the Profiling Buffer is owned by EL2. For more information, see 'Controlling the data that is collected'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PA, bit [4]**

Physical Address sample enable.

<table>
<thead>
<tr>
<th>PA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Physical addresses are not collected.</td>
</tr>
<tr>
<td>0b1</td>
<td>Physical addresses are collected.</td>
</tr>
</tbody>
</table>

If EL2 is implemented:

- If the Profiling Buffer is owned by EL1, this bit is combined with PMSCR_EL2.PA to determine which address is collected. For more information, see 'Controlling the data that is collected'.
- If the Profiling Buffer is owned by EL2, this bit is ignored by the PE.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CX, bit [3]**

CONTEXTIDR_EL1 sample enable.

<table>
<thead>
<tr>
<th>CX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CONTEXTIDR_EL1 is not collected.</td>
</tr>
<tr>
<td>0b1</td>
<td>CONTEXTIDR_EL1 is collected.</td>
</tr>
</tbody>
</table>

If EL2 is implemented and enabled in the current Security state when an operation is sampled:

- If the PE is at EL2, this bit is ignored by the PE.
- If HCR_EL2.TGE == 1, this bit is ignored by the PE.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [2]**

Reserved, RES0.

**E1SPE, bit [1]**

EL1 Statistical Profiling Enable.
If EL2 is implemented and enabled in the current Security state, this bit is ignored by the PE when $HCR_{EL2}.TGE == 1$.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E0SPE, bit [0]**

EL0 Statistical Profiling Enable. Controls sampling at EL0 when $HCR_{EL2}.TGE == 0$ or if EL2 is disabled or not implemented.

<table>
<thead>
<tr>
<th>E0SPE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sampling disabled at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sampling enabled at EL0.</td>
</tr>
</tbody>
</table>

If EL2 is implemented and enabled in the current Security state, this bit is ignored by the PE when $HCR_{EL2}.TGE == 1$.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMSCR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, PMSCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x828];
    else
        return PMSCR_EL1;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HCR_EL2.E2H == '1' then
        return PMSCR_EL2;
    else
        return PMSCR_EL1;
    endif
elsif PSTATE.EL == EL3 then
    return PMSCR_EL1;
endif

MSR PMSCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x828] = X[t];
    else
        PMSCR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HCR_EL2.E2H == '1' then
        PMSCR_EL2 = X[t];
    else
        PMSCR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    PMSCR_EL1 = X[t];
else
    PMSCR_EL1, Statistical Profiling Control Register (EL1)

MRS <Xt>, PMSCR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x828];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
                UNDEFINED;
            elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
                UNDEFINED;
            elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.SystemAccessTrap(EL3, 0x18);
            elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.SystemAccessTrap(EL3, 0x18);
            else
                return PMSCR_EL1;
            end
        else
            UNDEFINED;
    elsif PSTATE.EL == EL3 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
            return PMSCR_EL1;
        else
            UNDEFINED;
    end
else
    return PMSCR_EL1;
end

MSR PMSCR_EL12, <Xt>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x828] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end;
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end;
    else
      PMSCR_EL1 = X[t];
  end;
else
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    PMSCR_EL1 = X[t];
  else
    UNDEFINED;
end;
PMSCR_EL2, Statistical Profiling Control Register (EL2)

The PMSCR_EL2 characteristics are:

**Purpose**

Provides EL2 controls for Statistical Profiling.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSCR_EL2 are UNDEFINED.

**Attributes**

PMSCR_EL2 is a 64-bit register.

**Field descriptions**

The PMSCR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
| RES0 | RES0 | PCT | TS | PA | CX | RES0 | E2SPE | E0HSPE |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:8]**

Reserved, RES0.

**PCT, bits [7:6]**

Physical Timestamp. If timestamp sampling is enabled, determines which counter is collected. The behavior depends on the Profiling Buffer owning Exception level.

If FEAT_ECV is implemented, this is a two-bit field as shown. Otherwise, bit[7] is RES0.
PCT

<table>
<thead>
<tr>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>Virtual timestamp. The collected timestamp is the physical counter minus a virtual offset. If any of the following are true, the virtual offset is zero, otherwise the virtual offset is the value of CNTVOFF_EL2:</td>
<td></td>
</tr>
<tr>
<td>The sampled operation executed at EL2 and ( HCR_{EL2}.E2H == 0b1 ).</td>
<td></td>
</tr>
<tr>
<td>The sampled operation executed at EL0 and ( HCR_{EL2}.{E2H,TGE} == {1,1} ).</td>
<td></td>
</tr>
</tbody>
</table>

Note

If the Profiling Buffer owning Exception level is EL1, the virtual offset is always CNTVOFF_EL2.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>If the Profiling Buffer owning Exception level is EL1, then the timestamp value is selected by PMSCR_EL1.PCT. Otherwise, physical timestamp. The collected timestamp is the physical counter.</td>
<td></td>
</tr>
</tbody>
</table>

0b01

If the Profiling Buffer owning Exception level is EL1, then the timestamp value is selected by PMSCR_EL1.PCT. Otherwise, physical timestamp. The collected timestamp is the physical counter.

0b11

If the Profiling Buffer owning Exception level is EL1 and PMSCR_EL1.PCT == 0b00, then guest virtual timestamp. The collected timestamp is the physical counter minus the value of CNTVOFF_EL2. Otherwise, guest physical timestamp. The collected timestamp is the physical counter minus a physical offset. If any of the following are true, the physical offset is zero, otherwise the physical offset is the value of CNTPOFF_EL2:

- \( SCR_{EL3}.ECVEn == 0b0 \).
- \( CNTHCTL_{EL2}.ECV == 0b0 \).

When FEAT_ECV is implemented

All other values are reserved.

If EL2 is not implemented or EL2 is disabled in the current Security state, then the Effective value of this field is 0b01, other than for a direct read of the register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TS, bit [5]

Timestamp Enable.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timestamp sampling disabled.</td>
<td></td>
</tr>
<tr>
<td>Timestamp sampling enabled.</td>
<td></td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when any of the following are true:

- The Profiling Buffer owning Exception level is EL1.
- In Secure state, and either FEAT_SEL2 is not implemented or Secure EL2 is disabled.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

PA, bit [4]

Physical Address Sample Enable.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>Physical addresses are not collected.</td>
<td></td>
</tr>
<tr>
<td>Physical addresses are collected.</td>
<td></td>
</tr>
</tbody>
</table>

If the Profiling Buffer owning Exception level is EL1, and EL2 is enabled in the current Security state, this bit is combined with PMSCR_EL1.PA to determine which address is collected.
If EL2 is not implemented or EL2 is disabled in the current Security state, the PE ignores the value of this bit and behaves as if this bit is set to 1, other than for a direct read of the register.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CX, bit [3]**

<table>
<thead>
<tr>
<th>CX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>CONTEXTIDR_EL2</strong> is not collected.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>CONTEXTIDR_EL2</strong> is collected.</td>
</tr>
</tbody>
</table>

If EL2 is not implemented or EL2 is disabled in the current Security state, the PE ignores the value of this bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [2]**

Reserved, **RES0**.

**E2SPE, bit [1]**

EL2 Statistical Profiling Enable.

<table>
<thead>
<tr>
<th>E2SPE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sampling disabled at EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sampling enabled at EL2.</td>
</tr>
</tbody>
</table>

This bit is **RES0** if **MDCR_EL2.E2PB != 0b00**.

If EL2 is disabled in the current Security state, this bit is ignored by the PE.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E0HSPE, bit [0]**

EL0 Statistical Profiling Enable.

<table>
<thead>
<tr>
<th>E0HSPE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sampling disabled at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sampling enabled at EL0.</td>
</tr>
</tbody>
</table>

If **MDCR_EL2.E2PB != 0b00**, this bit is **RES0**.

If EL2 is implemented and enabled in the current Security state, this bit is ignored by the PE when **HCR_EL2.TGE == 0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMSCR_EL2**

Accesses to this register use the following encodings:

```
MRS <Xt>, PMSCR_EL2
```

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
priority when SDD == '1' && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
priority when SDD == '1' && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    return PMSCR_EL2;
  endif
elsif PSTATE.EL == EL3 then
  PMSCR_EL2 = X[t];
endif
MRS <Xt>, PMSCR_EL1

\[
\begin{array}{|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} \\
\hline
0b11 & 0b000 & 0b1001 & 0b1001 \\
\hline
\end{array}
\]

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '0' & MDCR_EL3.NSPB != '01' then
UNDEFINED;
elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
UNDEFINED;
elif EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HDFGRTR_EL2.PMSCR_EL1 == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() & MDCR_EL2.TPMS == '1' then
AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) & & SCR_EL3.NS == '0' & & MDCR_EL3.NSPB != '01' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
elsif HaveEL(EL3) & & SCR_EL3.NS == '1' & & MDCR_EL3.NSPB != '11' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
elsif EL2Enabled() & & HCR_EL2.<NV2,NV1,NV> == '111' then
return NVMem[0x828];
else
return PMSCR_EL1;
elsif PSTATE.EL == EL2 then
if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '0' & MDCR_EL3.NSPB != '01' then
UNDEFINED;
elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & SCR_EL3.NS == '1' & MDCR_EL3.NSPB != '11' then
UNDEFINED;
elsif HaveEL(EL3) & & SCR_EL3.NS == '0' & & MDCR_EL3.NSPB != '01' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
elsif HaveEL(EL3) & & SCR_EL3.NS == '1' & & MDCR_EL3.NSPB != '11' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.SystemAccessTrap(EL3, 0x18);
elsif HCR_EL2.E2H == '1' then
return PMSCR_EL2;
else
return PMSCR_EL1;
elsif PSTATE.EL == EL3 then
return PMSCR_EL1;

MSR PMSCR_EL1, <Xt>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSCR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
 elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif HCR_EL2.E2H == '1' then
    PMSCR_EL2 = X[t];
  else
    PMSCR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif HCR_EL2.E2H == '1' then
    PMSCR_EL2 = X[t];
  else
    PMSCR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  PMSCR_EL1 = X[t];
else
  PMSCR_EL1 = X[t];
end if
PMSELR_EL0, Performance Monitors Event Counter Selection Register

The PMSELR_EL0 characteristics are:

**Purpose**

Selects the current event counter \texttt{PMEVCNTR<n>_EL0} or the cycle counter, CCNT.

PMSELR_EL0 is used in conjunction with \texttt{PMXEVTYPER_EL0} to determine the event that increments a selected event counter, and the modes and states in which the selected counter increments.

It is also used in conjunction with \texttt{PMXEVCNTR_EL0}, to determine the value of a selected event counter.

**Configuration**

AArch64 System register PMSELR_EL0 bits [31:0] are architecturally mapped to AArch32 System register \texttt{PMSELR[31:0]}.

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMSELR_EL0 are UNDEFINED.

**Attributes**

PMSELR_EL0 is a 64-bit register.

**Field descriptions**

The PMSELR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:5]**

Reserved, RES0.

**SEL, bits [4:0]**

Selects event counter, \texttt{PMEVCNTR<n>_EL0}, where \text{n\text{}} is the value held in this field. This value identifies which event counter is accessed when a subsequent access to \texttt{PMXEVTYPER_EL0} or \texttt{PMXEVCNTR_EL0} occurs.

This field can take any value from 0 (0b00000) to (PMCR.N)-1, or 31 (0b11111).

When PMSELR_EL0.SEL is 0b11111, it selects the cycle counter and:

- A read of the \texttt{PMXEVTYPER_EL0} returns the value of \texttt{PMCCFILTR_EL0}.
- A write of the \texttt{PMXEVTYPER_EL0} writes to \texttt{PMCCFILTR_EL0}.
- A read or write of \texttt{PMXEVCNTR_EL0} has CONSTRAINED UNPREDICTABLE effects. See \texttt{PMXEVCNTR_EL0} for more details.

For details of the results of accesses to the event counters, see \texttt{PMXEVTYPER_EL0} and \texttt{PMXEVCNTR_EL0}.

For information about the number of counters accessible at each Exception level, see \texttt{MDCR_EL2.HPMN}.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMSELR_EL0

Accesses to this register use the following encodings:

MRS <Xt>, PMSELR_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.<ER,EN> == '00' then
    if EL2Enabled() & HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end if
elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
else
  return PMSELR_EL0;
end if

elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() & MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return PMSELR_EL0;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) & MDCR_EL3.TPM == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end if
else
  return PMSELR_EL0;
end if

elif PSTATE.EL == EL3 then
  return PMSELR_EL0;
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.<ER,EN> == '00' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '1' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSELR_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        PMSELR_EL0 = X[t];
    end
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSELR_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        PMSELR_EL0 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        PMSELR_EL0 = X[t];
    end
elsif PSTATE.EL == EL3 then
    PMSELR_EL0 = X[t];
PMSEVFR_EL1, Sampling Event Filter Register

The PMSEVFR_EL1 characteristics are:

**Purpose**

Controls sample filtering by events. The overall filter is the logical AND of these filters. For example, if E[3] and E[5] are both set to 1, only samples that have both event 3 (Level 1 unified or data cache refill) and event 5 set (TLB walk) are recorded.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSEVFR_EL1 are UNDEFINED.

**Attributes**

PMSEVFR_EL1 is a 64-bit register.

**Field descriptions**

The PMSEVFR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
</tr>
</tbody>
</table>

E[<x>], bit [x], for x = 63 to 48, 31 to 24, 15 to 12

E[<x>] is the event filter for event <x>. If event <x> is not implemented, or filtering on event <x> is not supported, the corresponding bit is RAZ/WI.

<table>
<thead>
<tr>
<th>E[&lt;x&gt;]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event &lt;x&gt; is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have event &lt;x&gt; == 0.</td>
</tr>
</tbody>
</table>

An IMPLEMENTATION DEFINED event might be recorded as a multi-bit field. In this case, if the corresponding bits of PMSEVFR_EL1 define an IMPLEMENTATION DEFINED filter for the event.

This field is ignored by the PE when PMSCFR_EL1.FE == 0

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [47:32]**

Reserved, RAZ/WI.

**Bits [23:19]**

Reserved, RAZ/WI.
**E[18], bit [18]**

When **FEAT_SPEv1p1** is implemented and **FEAT_SVE** is implemented:

Empty predicate.

<table>
<thead>
<tr>
<th>E[18]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Empty predicate event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Empty predicate event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when **PMSFCR_EL1.FE == 0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RAZ/WI.

**E[17], bit [17]**

When **FEAT_SPEv1p1** is implemented and **FEAT_SVE** is implemented:

Partial predicate.

<table>
<thead>
<tr>
<th>E[17]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Partial predicate event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Partial predicate event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when **PMSFCR_EL1.FE == 0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RAZ/WI.

**Bit [16]**

Reserved, RAZ/WI.

**E[11], bit [11]**

When **FEAT_SPEv1p1** is implemented:

Alignment.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Alignment event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Alignment event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when **PMSFCR_EL1.FE == 0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RAZ/WI.
Bits [10:8]

Reserved, RAZ/WI.

E[7], bit [7]

Mispredicted.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Mispredicted event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Mispredicted event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FE == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E[6], bit [6]

When FEAT_SPEv1p2 is implemented:

Not taken.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Not taken event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Not taken event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAZ/WI.

E[5], bit [5]

TLB walk.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TLB walk event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the TLB walk event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FE == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [4]

Reserved, RAZ/WI.

E[3], bit [3]

Level 1 data or unified cache refill.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Level 1 data or unified cache refill event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Level 1 data or unified cache refill event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FE == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [2]
Reserved, RAZ/WI.

E[1], bit [1]
When the PE supports sampling of speculative instructions:
Architecturally retired.

When the PE supports sampling of speculative instructions:

<table>
<thead>
<tr>
<th>E[1]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Architecturally retired event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Architecturally retired event == 0.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FE == 0.

If the PE does not support the sampling of speculative instructions, or always discards the sample record for speculative instructions, this bit reads as an UNKNOWN value and the PE ignores its value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, UNKNOWN.

Bit [0]
Reserved, RAZ/WI.

Accessing the PMSEVFR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PMSEVFR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSEVFR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    return NVMem[0x830];
  else
    return PMSEVFR_EL1;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  else
    return PMSEVFR_EL1;
  end if;
elsif PSTATE.EL == EL3 then
  return PMSEVFR_EL1;
else
  return PMSEVFR_EL1;
end if;

MSR PMSEVFR_EL1, <Xt>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSEVFR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        NVMem[0x830] = X[t];
    else
        PMSEVFR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        PMSEVFR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    PMSEVFR_EL1 = X[t];
PMSFCR_EL1, Sampling Filter Control Register

The PMSFCR_EL1 characteristics are:

Purpose

Controls sample filtering. The filter is the logical AND of the FL, FT and FE bits. For example, if FE == 1 and FT == 1 only samples including the selected operation types and the selected events will be recorded.

Configuration

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSFCR_EL1 are UNDEFINED.

Attributes

PMSFCR_EL1 is a 64-bit register.

Field descriptions

The PMSFCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-19</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td>ST (Store filter enable)</td>
</tr>
<tr>
<td>17</td>
<td>LD (Load filter enable)</td>
</tr>
</tbody>
</table>

ST, bit [18]

Store filter enable

<table>
<thead>
<tr>
<th>ST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not record store operations</td>
</tr>
<tr>
<td>0b1</td>
<td>Record all store operations, including vector stores and all atomic operations</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FT == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

LD, bit [17]

Load filter enable

<table>
<thead>
<tr>
<th>LD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not record load operations</td>
</tr>
<tr>
<td>0b1</td>
<td>Record all load operations, including vector loads and atomic operations that return data</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FT == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
B, bit [16]

Branch filter enable

<table>
<thead>
<tr>
<th>B</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not record branch and exception return operations</td>
</tr>
<tr>
<td>0b1</td>
<td>Record all branch and exception return operations</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FT == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [15:4]

Reserved, RES0.

FnE, bit [3]

When FEAT_SPEv1p2 is implemented:

Filter by event, inverted.

<table>
<thead>
<tr>
<th>FnE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inverted event filtering disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inverted event filtering enabled. Samples including the events selected by PMSNEVFR_EL1 will not be recorded.</td>
</tr>
</tbody>
</table>

If any of the following are true, it is CONSTRAINED UNPREDICTABLE whether no samples are recorded or the PE behaves as if PMSFCR_EL1.FnE == 0b0:

- PMSFCR_EL1.FnE == 0b1 and PMSNEVFR_EL1 is zero.
- PMSFCR_EL1.FnE == 0b1, PMSFCR_EL1.FE == 0b1, and there exists a value x such that PMSEVFR_EL1.E[x] == 0b1 and PMSNEVFR_EL1.E[x] == 0b1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

FL, bit [2]

Filter by latency

<table>
<thead>
<tr>
<th>FL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Latency filtering disabled</td>
</tr>
<tr>
<td>0b1</td>
<td>Latency filtering enabled. Samples with a total latency less than PMSLATFR_EL1.MINLAT will not be recorded</td>
</tr>
</tbody>
</table>

If this field is set to 1 and PMSLATFR_EL1.MINLAT is set to zero, it is CONSTRAINED UNPREDICTABLE whether no samples are recorded or the PE behaves as if PMSFCR_EL1.FL is set to 0

On a Warm reset, this field resets to an architecturally UNKNOWN value.

FT, bit [1]

Filter by operation type. The filter is the logical OR of the ST, LD and B bits. For example, if LD and ST are both set, both load and store operations are recorded

<table>
<thead>
<tr>
<th>FT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Type filtering disabled</td>
</tr>
<tr>
<td>0b1</td>
<td>Type filtering enabled. Samples not one of the selected operation types will not be recorded</td>
</tr>
</tbody>
</table>
If this field is set to 1 and the PMSFCR_EL1.{ST, LD, B} bits are all set to zero, it is **CONSTRAINED UNPREDICTABLE** whether no samples are recorded or the PE behaves as if PMSFCR_EL1.FT is set to 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### FE, bit [0]

Filter by event.

<table>
<thead>
<tr>
<th>FE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event filtering disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event filtering enabled. Samples not including the events selected by PMSEVFR_EL1 will not be recorded.</td>
</tr>
</tbody>
</table>

If any of the following are true, it is **CONSTRAINED UNPREDICTABLE** whether no samples are recorded or the PE behaves as if PMSFCR_EL1.FE == 0b0:

- PMSFCR_EL1.FE == 0b1 and PMSEVFR_EL1 is zero.
- FEAT_SPEv1p2 is implemented, PMSFCR_EL1.FnE == 0b1, PMSFCR_EL1.FE == 0b1, and there exists a value \(x\) such that PMSEVFR_EL1.E[\(x\)] == 0b1 and PMSNEVFR_EL1.E[\(x\)] == 0b1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the PMSFCR_EL1

Accesses to this register use the following encodings:

**MRS <Xt>, PMSFCR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSFCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elselse
            AArch64.SystemAccessTrap(EL3, 0x18);
else
            return PMSFCR_EL1;
eelsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
elselse
            AArch64.SystemAccessTrap(EL3, 0x18);
else
            return PMSFCR_EL1;
eelsif PSTATE.EL == EL3 then
    return PMSFCR_EL1;
else
    return PMSFCR_EL1;

MSR PMSFCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    else
        EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSFCR_EL1 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    endif
else
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
    if Halted() && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        PMSFCR_EL1 = X[t];
    endif
else
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        if HAVE_EL_EL3 && SCR_EL3.FGTEn == '1' then
            AArch64.SystemAccessTrap(EL3, 0x18);
        else
            PMSFCR_EL1 = X[t];
        endif
    endif
else
    PMSFCR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    PMSFCR_EL1 = X[t];
PMSICR_EL1, Sampling Interval Counter Register

The PMSICR_EL1 characteristics are:

**Purpose**

Software must write zero to PMSICR_EL1 before enabling sample profiling for a sampling session. Software must then treat PMSICR_EL1 as an opaque, 64-bit, read/write register used for context switches only.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSICR_EL1 are UNDEFINED.

The value of PMSICR_EL1 does not change whilst profiling is disabled.

**Attributes**

PMSICR_EL1 is a 64-bit register.

**Field descriptions**

The PMSICR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**ECOUNT, bits [63:56]**

When PMSIDR_EL1.ERnd == 1:

Secondary sample interval counter.

This field provides the secondary counter used after the primary counter reaches zero. Whilst the secondary counter is nonzero and profiling is enabled, the secondary counter decrements by 1 for each member of the sample population. The primary counter also continues to decrement since it is also nonzero. When the secondary counter reaches zero, a member of the sampling population is selected for sampling.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [55:32]**

Reserved, RES0.

**COUNT, bits [31:0]**

Primary sample interval counter

Provides the primary counter used for sampling.
The primary counter is reloaded when the value of this register is zero and the PE moves from a state or Exception level where profiling is disabled to a state or Exception level where profiling is enabled.

Whilst the primary counter is nonzero and sampling is enabled, the primary counter decrements by 1 for each member of the sample population.

When the counter reaches zero, the behavior depends on the values of PMSIDR_EL1.ERnd and PMSIRR_EL1.RND:

- If PMSIRR_EL1.RND == 0 or PMSIDR_EL1.ERnd == 0:
  - A member of the sampling population is selected for sampling
  - The primary counter is reloaded

- If PMSIRR_EL1.RND == 1 and PMSIDR_EL1.ERnd == 1:
  - The secondary counter is set to a random or pseudorandom value in the range 0x00 to 0xFF
  - The primary counter is reloaded

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMSICR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, PMSICR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSICR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        return NVMem[0x838];
    else
        return PMSICR_EL1;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    return PMSICR_EL1;
endif
elsif PSTATE.EL == EL3 then
    return PMSICR_EL1;
endif

MSR PMSICR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSICR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        PMSICR_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        PMSICR_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    PMSICR_EL1 = X[t];
The PMSIDR_EL1 characteristics are:

**Purpose**

Describes the Statistical Profiling implementation to software

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSIDR_EL1 are UNDEFINED.

**Attributes**

PMSIDR_EL1 is a 64-bit register.

**Field descriptions**

The PMSIDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-24</td>
<td>Reserved</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23-20</td>
<td>Format</td>
<td>Format of sample records</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Defined values:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Format 0</td>
</tr>
<tr>
<td></td>
<td>CountSize</td>
<td>Size of counters</td>
</tr>
<tr>
<td></td>
<td>MaxSize</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Interval</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>19-16</td>
<td>Reserved</td>
<td>RAZ</td>
</tr>
<tr>
<td>15-12</td>
<td>Interval</td>
<td></td>
</tr>
<tr>
<td>11-8</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>7-4</td>
<td>Format</td>
<td></td>
</tr>
<tr>
<td>3-0</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**Format, bits [23:20]**

From Armv8.7:

Defines the format of the sample records. Defined values are:

<table>
<thead>
<tr>
<th>Format</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Format 0</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Otherwise:**

Reserved, RAZ.

**CountSize, bits [19:16]**

Defines the size of the counters. Defined values are:

<table>
<thead>
<tr>
<th>CountSize</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0010</td>
<td>12-bit saturating counters</td>
</tr>
</tbody>
</table>

All other values are reserved.

Reserved values might be defined in a future version of the architecture.
MaxSize, bits [15:12]

Defines the largest size for a single record, rounded up to a power-of-two. If this is the same as the minimum alignment (PMBIDR_EL1.Align), then each record is exactly this size. Defined values are:

<table>
<thead>
<tr>
<th>MaxSize</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0100</td>
<td>16 bytes</td>
</tr>
<tr>
<td>0b0101</td>
<td>32 bytes</td>
</tr>
<tr>
<td>0b0110</td>
<td>64 bytes</td>
</tr>
<tr>
<td>0b0111</td>
<td>128 bytes</td>
</tr>
<tr>
<td>0b1000</td>
<td>256 bytes</td>
</tr>
<tr>
<td>0b1001</td>
<td>512 bytes</td>
</tr>
<tr>
<td>0b1010</td>
<td>1024 bytes</td>
</tr>
<tr>
<td>0b1011</td>
<td>2KB</td>
</tr>
</tbody>
</table>

All other values are reserved.

Reserved values might be defined in a future version of the architecture.

Interval, bits [11:8]

Recommended minimum sampling interval. This provides guidance from the implementer to the smallest minimum sampling interval, N. Defined values are:

<table>
<thead>
<tr>
<th>Interval</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>256</td>
</tr>
<tr>
<td>0b0010</td>
<td>512</td>
</tr>
<tr>
<td>0b0011</td>
<td>768</td>
</tr>
<tr>
<td>0b0100</td>
<td>1,024</td>
</tr>
<tr>
<td>0b0101</td>
<td>1,536</td>
</tr>
<tr>
<td>0b0110</td>
<td>2,048</td>
</tr>
<tr>
<td>0b0111</td>
<td>3,072</td>
</tr>
<tr>
<td>0b1000</td>
<td>4,096</td>
</tr>
</tbody>
</table>

All other values are reserved.

Reserved values might be defined in a future version of the architecture.

Bit [7]

Reserved, RES0.

FnE, bit [6]

Filtering by events, inverted. Defined values are:

<table>
<thead>
<tr>
<th>FnE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PMSNEVFR_EL1 is not implemented and PMSFCR_EL1.FnE is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMSNEVFR_EL1 and PMSFCR_EL1.FnE are implemented.</td>
</tr>
</tbody>
</table>

The value 0b1 indicates support for the FEAT_SPEv1p2 feature.

ERnd, bit [5]

Defines how the random number generator is used in determining the interval between samples, when enabled by PMSIRR_EL1.RND. Defined values are:

<table>
<thead>
<tr>
<th>ERnd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The random number is added at the start of the interval, and the sample is taken and a new interval started when the combined interval expires.</td>
</tr>
<tr>
<td>0b1</td>
<td>The random number is added and the new interval started after the interval programmed in PMSIRR_EL1.INTERVAL expires, and the sample is taken when the random interval expires.</td>
</tr>
</tbody>
</table>
LDS, bit [4]

Data source indicator for sampled load instructions. Defined values are:

<table>
<thead>
<tr>
<th>LDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Loaded data source not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Loaded data source implemented.</td>
</tr>
</tbody>
</table>

ArchInst, bit [3]

Architectural instruction profiling. Defined values are:

<table>
<thead>
<tr>
<th>ArchInst</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Micro-op sampling implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Architecture instruction sampling implemented.</td>
</tr>
</tbody>
</table>

FL, bit [2]

Filtering by latency. This bit is RAO.

FT, bit [1]

Filtering by operation type. This bit is RAO.

FE, bit [0]

Filtering by events. This bit is RAO.

Accessing the PMSIDR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PMSIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elside PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
elside Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
elside EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elside EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elside HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elside Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elside haveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elside Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
eelse
    return PMSIDR_EL1;
elside PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
elside Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
elside HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elside Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elside HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elside Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
eelse
    AArch64.SystemAccessTrap(EL3, 0x18);
elside HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elside HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      UNDEFINED;
eelse
    AArch64.SystemAccessTrap(EL3, 0x18);
eelse
    return PMSIDR_EL1;
elside PSTATE.EL == EL3 then
  return PMSIDR_EL1;
The PMSIRR_EL1 characteristics are:

**Purpose**

Defines the interval between samples.

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSIRR_EL1 are **UNDEFINED**.

**Attributes**

PMSIRR_EL1 is a 64-bit register.

**Field descriptions**

The PMSIRR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTERVAL | RES0 | RND |

**Bits [63:32]**

Reserved, RES0.

**INTERVAL, bits [31:8]**

Bits [31:8] of the PMSICR_EL1 interval counter reload value. Software must set this to a non-zero value. If software sets this to zero, an **UNKNOWN** sampling interval is used. Software should set this to a value greater than the minimum indicated by PMSIDR_EL1.Interval.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [7:1]**

Reserved, RES0.

**RND, bit [0]**

Controls randomization of the sampling interval.

<table>
<thead>
<tr>
<th>RND</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disable randomization of sampling interval.</td>
</tr>
<tr>
<td>0b1</td>
<td>Add (pseudo-)random jitter to sampling interval.</td>
</tr>
</tbody>
</table>

The random number generator is not architected.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Accessing the PMSIRR_EL1

Accesses to this register use the following encodings:

MRS <Xt>, PMSIRR_EL1

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSIRR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
        return NVMem[0x840];
    else
        return PMSIRR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    else
        return PMSIRR_EL1;
    end
elsif PSTATE.EL == EL3 then
    return PMSIRR_EL1;
end
```

MSR PMSIRR_EL1, <Xt>
if \( \text{PSTATE.EL} = \text{EL0} \) then

UNDEFINED;
elseif \( \text{PSTATE.EL} = \text{EL1} \) then

if Halted() \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"} \&\& \text{SCR_EL3.NS} == '0' \&\& \text{MDCR_EL3.NSPB} != '01' \) then

UNDEFINED;
elseif Halted() \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"} \&\& \text{SCR_EL3.NS} == '1' \&\& \text{MDCR_EL3.NSPB} != '11' \) then

UNDEFINED;
elseif \text{EL2Enabled()} \&\& (!\text{HaveEL(EL3)} \mid | \text{SCR_EL3.FGTEn} == '1') \&\& \text{HDFGWTR_EL2.PMSIRR_EL1} == '1' \) then

AArch64.SystemAccessTrap(EL2, 0x18);
elseif \text{EL2Enabled()} \&\& \text{MDCR_EL2.TPMS} == '1' \) then

AArch64.SystemAccessTrap(EL2, 0x18);
elseif \text{HaveEL(EL3)} \&\& \text{EDSCR.NS} == '0' \&\& \text{MDCR_EL3.NSPB} != '01' \) then

if Halted() \&\& \text{EDSCR.SDD} == '1' \) then

UNDEFINED;
else

AArch64.SystemAccessTrap(EL3, 0x18);
elseif \text{HaveEL(EL3)} \&\& \text{SCR_EL3.NS} == '1' \&\& \text{MDCR_EL3.NSPB} != '11' \) then

if Halted() \&\& \text{EDSCR.SDD} == '1' \) then

UNDEFINED;
else

AArch64.SystemAccessTrap(EL3, 0x18);
elseif \text{HaveEL(EL3)} \&\& \text{HCR_EL2.<NV2,NV1,NV>} == '1x1' \) then

\text{NVMem[0x840]} = X[t];
else

\text{PMISR EL1} = X[t];
elseif \text{PSTATE.EL} == \text{EL2} then

if Halted() \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"} \&\& \text{SCR_EL3.NS} == '0' \&\& \text{MDCR_EL3.NSPB} != '01' \) then

UNDEFINED;
elseif Halted() \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} == '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"} \&\& \text{SCR_EL3.NS} == '1' \&\& \text{MDCR_EL3.NSPB} != '11' \) then

UNDEFINED;
elseif \text{HaveEL(EL3)} \&\& \text{SCR_EL3.NS} == '0' \&\& \text{MDCR_EL3.NSPB} != '01' \) then

if Halted() \&\& \text{EDSCR.SDD} == '1' \) then

UNDEFINED;
else

AArch64.SystemAccessTrap(EL3, 0x18);
elseif \text{HaveEL(EL3)} \&\& \text{SCR_EL3.NS} == '1' \&\& \text{MDCR_EL3.NSPB} != '11' \) then

if Halted() \&\& \text{EDSCR.SDD} == '1' \) then

UNDEFINED;
else

AArch64.SystemAccessTrap(EL3, 0x18);
else

\text{PMISR EL1} = X[t];
elseif \text{PSTATE.EL} == \text{EL3} then

\text{PMISR EL1} = X[t];
PMSLATFR_EL1, Sampling Latency Filter Register

The PMSLATFR_EL1 characteristics are:

**Purpose**

Controls sample filtering by latency

**Configuration**

This register is present only when FEAT_SPE is implemented. Otherwise, direct accesses to PMSLATFR_EL1 are UNDEFINED.

**Attributes**

PMSLATFR_EL1 is a 64-bit register.

**Field descriptions**

The PMSLATFR_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

RES0

MINLAT

Bits [63:12]

Reserved, RES0.

**MINLAT, bits [11:0]**

Minimum latency. When PMSFCR_EL1.FL == 1, defines the minimum total latency for filtered operations. Samples with a total latency less than MINLAT will not be recorded.

This field is ignored by the PE when PMSFCR_EL1.FL == 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMSLATFR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, PMSLATFR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMSLATFR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  AArch64.SystemAccessTrap(EL3, 0x18);
  return NVMem[0x848];
else
  return PMSLATFR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    return PMSLATFR_EL1;
elsif PSTATE.EL == EL3 then
  return PMSLATFR_EL1;
else
  return PMSLATFR_EL1;
endif

MSR PMSLATFR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMSLATFR_EL1 == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
  AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
  if Halted() && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    NVMem[0x848] = X[t];
  else
    PMSLATFR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
elsif EL2Enabled() && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
elsif EL2Enabled() && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else
  PMSLATFR_EL1 = X[t];
else
  PSTATE.EL = EL3 then
  PMSLATFR_EL1 = X[t];
PMSNEVFR_EL1, Sampling Inverted Event Filter Register

The PMSNEVFR_EL1 characteristics are:

**Purpose**

Controls sample filtering by events. The overall filter is the logical AND of these filters. For example, if E[3] and E[5] are both set to 0b1, only samples that have both event 3 (Level 1 unified or data cache refill) and event 5 (TLB walk) clear are recorded.

**Configuration**

This register is present only when FEAT_SPEv1p2 is implemented. Otherwise, direct accesses to PMSNEVFR_EL1 are UNDEFINED.

**Attributes**

PMSNEVFR_EL1 is a 64-bit register.

**Field descriptions**

The PMSNEVFR_EL1 bit assignments are:

|   | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| E | [63] | [62] | [61] | [60] | [59] | [58] | [57] | [56] | [55] | [54] | [53] | [52] | [51] | [50] | [49] | [48] | [47] | [46] | [45] | [44] | [43] |
| E | [31] | [30] | [29] | [28] | [27] | [26] | [25] | [24] | [23] | [22] | [21] | [20] | [19] | [18] | [17] | [16] | [15] | [14] | [13] | [12] | [11] |

<table>
<thead>
<tr>
<th>E[&lt;x&gt;]</th>
<th>bit [x], for x = 63 to 48, 31 to 24, 15 to 12</th>
</tr>
</thead>
<tbody>
<tr>
<td>E[&lt;x&gt;]</td>
<td>is the event filter for IMPLEMENTATION DEFINED event &lt;x&gt;.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>E[&lt;x&gt;]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event &lt;x&gt; is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have event &lt;x&gt; == 1.</td>
</tr>
</tbody>
</table>

An IMPLEMENTATION DEFINED event might be recorded as a multi-bit field. In this case, the corresponding bits of PMSNEVFR_EL1 define an IMPLEMENTATION DEFINED filter for the event.

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When event <x> is not implemented, or filtering on event <x> is not supported, access to this field is RAZ/WI.

**Bits [47:32]**

Reserved, RAZ/WI.

**Bits [23:19]**

Reserved, RAZ/WI.

**E[18], bit [18]**
When FEAT_SVE is implemented and FEAT_SPEv1p1 is implemented:

Not empty predicate.

<table>
<thead>
<tr>
<th>E[18]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Empty predicate event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Empty predicate event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAZ/WI.

E[17], bit [17]

When FEAT_SVE is implemented and FEAT_SPEv1p1 is implemented:

Not partial predicate.

<table>
<thead>
<tr>
<th>E[17]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Partial predicate event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Partial predicate event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAZ/WI.

Bit [16]

Reserved, RAZ/WI.


When FEAT_SPEv1p1 is implemented:

Aligned.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Misalignment event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Misalignment event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAZ/WI.

Bits [10:8]

Reserved, RAZ/WI.
E[7], bit [7]
Correctly predicted.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Mispredicted event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Mispredicted event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E[6], bit [6]
Taken.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Not taken event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Not taken event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E[5], bit [5]
TLB hit.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TLB walk event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the TLB walk event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [4]
Reserved, RAZ/WI.

E[3], bit [3]
Level 1 data or unified cache hit.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Level 1 data or unified cache refill event is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not record samples that have the Level 1 data or unified cache refill event == 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [2]
Reserved, RAZ/WI.

E[1], bit [1]
Speculative.
### E[1]

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0 Architecturally retired event is ignored.</td>
</tr>
<tr>
<td>0b1 Do not record samples that have the Architecturally retired event</td>
</tr>
<tr>
<td>== 1.</td>
</tr>
</tbody>
</table>

This bit is ignored by the PE when PMSFCR_EL1.FnE == 0b0. This bit is RES0 if the PE does not support sampling of speculative instructions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [0]**

Reserved, RAZ/WI.

**Accessing the PMSNEVFR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, PMSNEVFR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && ((HaveEL(EL3) && SCR_EL3.FGTEn == '0') || HDFGRTR_EL2.nPMSNEVFR_EL1 == '0') then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && MDCR_EL3.EnPMSN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    return NVMem[0x850];
else
  return PMSNEVFR_EL1;
endif;
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && MDCR_EL3.EnPMSN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
else
  return PMSNEVFR_EL1;
endif;
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
  elsif HaveEL(EL3) && MDCR_EL3.EnPMSN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if;
else
  return PMSNEVFR_EL1;
endif;
else
  if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
      UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
      UNDEFINED;
    elseif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    elseif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    elseif HaveEL(EL3) && MDCR_EL3.EnPMSN == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if;
    else
      return PMSNEVFR_EL1;
    endif;
  elseif PSTATE.EL == EL3 then
    return PMSNEVFR_EL1;
  else
    return PMSNEVFR_EL1;
  endif;
MSR PMSNEVFR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then

  UNDEFINED;

elsif PSTATE.EL == EL1 then

  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && ((HaveEL(EL3) && SCR_EL3.FGTEn == '0') || HDFGWTR_EL2.nPMSNEVFR_EL1 == '0') then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPMS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && MDCR_EL3.EnPMSN == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  endif
else

  PMSNEVFR_EL1 = X[t];
endif
else

  if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.EnPMSN == '0' then
      UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
      NVMem[0x850] = X[t];
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '0' && MDCR_EL3.NSPB != '01' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif HaveEL(EL3) && SCR_EL3.NS == '1' && MDCR_EL3.NSPB != '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    endif
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '1x1' then
    NVMem[0x850] = X[t];
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  endif
else

  if PSTATE.EL == EL3 then
    AArch64.SystemAccessTrap(EL3, 0x18);
  else
    if PSTATE.EL == EL3 then
      PMSNEVFR_EL1 = X[t];
    else
      PMSNEVFR_EL1 = X[t];
    endif
  endif
endif

PMSNEVFR_EL1, Sampling Inverted Event Filter Register
The PMSWINC_EL0 characteristics are:

**Purpose**

Increments a counter that is configured to count the Software increment event, event 0x00. For more information, see ‘SW_INCR’.

**Configuration**

AArch64 System register PMSWINC_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMSWINC[31:0].

AArch64 System register PMSWINC_EL0 bits [31:0] are architecturally mapped to External register PMSWINC_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMSWINC_EL0 are UNDEFINED.

**Attributes**

PMSWINC_EL0 is a 64-bit register.

**Field descriptions**

The PMSWINC_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>P30, bit [30], for n = 30 to 0</td>
</tr>
<tr>
<td>60</td>
<td>Event counter software increment bit for PMEVCNTR&lt;n&gt;_EL0.</td>
</tr>
<tr>
<td>59</td>
<td>If N is less than 31, then bits [30:N] are WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.</td>
</tr>
<tr>
<td>58</td>
<td>If N is less than 31, then bits [30:N] are WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN. Otherwise, N is the value in PMCR_EL0.N.</td>
</tr>
</tbody>
</table>

**Accessing the PMSWINC_EL0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.<SW,EN> == '00' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if
    end if
    elsif EL2Enabled() && HDFGWTR_EL2.PMSWINC_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    end if
else
    PMSWINC_EL0 = X[t];
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif Halted() && HDFGWTR_EL2.PMSWINC_EL0 == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
        end if
    else
        PMSWINC_EL0 = X[t];
    endif
else
    if PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            end if
        end if
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    PMSWINC_EL0 = X[t];
else
    if PSTATE.EL == EL3 then
        PMSWINC_EL0 = X[t];
end if
PMUSERENR_EL0, Performance Monitors User Enable Register

The PMUSERENR_EL0 characteristics are:

**Purpose**

Enables or disables EL0 access to the Performance Monitors.

**Configuration**

AArch64 System register PMUSERENR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMUSERENR[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMUSERENR_EL0 are UNDEFINED.

**Attributes**

PMUSERENR_EL0 is a 64-bit register.

**Field descriptions**

The PMUSERENR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | ER | CR | SW | EN |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:4]**

Reserved, RES0.

**ER, bit [3]**

Event counter Read. Traps EL0 access to event counters to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1.

In AArch64 state, trapped accesses are reported using EC syndrome value 0x18.

In AArch32 state, trapped accesses are reported using EC syndrome value 0x03.

<table>
<thead>
<tr>
<th>ER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 using AArch64: EL0 reads of the PMXEVCNTR_EL0 and PMEVCNTR&lt;n&gt;_EL0 and EL0 read/write accesses to the PMSELR_EL0, are trapped if PMUSERENR_EL0.EN is also 0. EL0 using AArch32: EL0 reads of the PMXEVCNTR and PMEVCNTR&lt;n&gt;, and EL0 read/write accesses to the PMSELR, are trapped if PMUSERENR_EL0.EN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overrides PMUSERENR_EL0.EN and enables: • RO access to PMXEVCNTR_EL0 and PMEVCNTR&lt;n&gt;_EL0 at EL0. • RW access to PMSELR_EL0 at EL0. • RW access to PMSELR at EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
CR, bit [2]

Cycle counter Read. Traps EL0 access to cycle counter reads to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1.

In AArch64 state, trapped accesses are reported using EC syndrome value 0x18.

In AArch32 state, trapped MRC accesses are reported using EC syndrome value 0x03, trapped MRRC accesses are reported using EC syndrome value 0x04.

<table>
<thead>
<tr>
<th>CR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 using AArch64: EL0 read accesses to the PMCCNTR_EL0 are trapped if PMUSERENR_EL0.EN is also 0. EL0 using AArch32: EL0 read accesses to the PMCCNTR are trapped if PMUSERENR_EL0.EN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overrides PMUSERENR_EL0.EN and enables access to:</td>
</tr>
<tr>
<td></td>
<td>• PMCCNTR_EL0 at EL0.</td>
</tr>
<tr>
<td></td>
<td>• PMCCNTR at EL0.</td>
</tr>
</tbody>
</table>

SW, bit [1]

Traps Software Increment writes to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1.

In AArch64 state, trapped accesses are reported using EC syndrome value 0x18.

In AArch32 state, trapped accesses are reported using EC syndrome value 0x03.

<table>
<thead>
<tr>
<th>SW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 using AArch64: EL0 writes to the PMSWINC_EL0 are trapped if PMUSERENR_EL0.EN is also 0. EL0 using AArch32: EL0 writes to the PMSWINC are trapped if PMUSERENR_EL0.EN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overrides PMUSERENR_EL0.EN and enables access to:</td>
</tr>
<tr>
<td></td>
<td>• PMSWINC_EL0 at EL0.</td>
</tr>
<tr>
<td></td>
<td>• PMSWINC at EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EN, bit [0]

Traps EL0 accesses to the Performance Monitor registers to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, from both Execution states as follows:

- In AArch64 state, MRS or MSR accesses to the following registers are reported using EC syndrome value 0x18:
  - PMCR_EL0, PMOVSCLR_EL0, PMSELR_EL0, PMCEID0_EL0, PMCEID1_EL0, PMCCNTR_EL0, PMXEVTYPEP_EL0, PMXEVCNTR_EL0, PMCNTENSET_EL0, PMCNTENCLR_EL0, PMOVSSSET_EL0, PEMVCNTR<n>_EL0, PMEVTYPER<n>_EL0, PMEVTYPER<n>_EL0, PMCCFILTR_EL0, PMSWINC_EL0.
  - If FEAT_PMUv3p4 is implemented, PMMIR_EL1.

- In AArch32 state, MRC or MCR accesses to the following registers are reported using EC syndrome value 0x03:
  - PMCR, PMOVSR, PMSELR, PMCEID0, PMCEID1, PMCCNTR, PMXEVTYPEP, PMXEVCNTR, PMCNTENSET, PMCNTENCLR, PMOVSSSET, PEMVCNTR<n>, PMEVTYPER<n>, PMCCFILTR, PMSWINC.
  - If FEAT_PMUv3p4 is implemented, PMMIR.
  - If FEAT_PMUv3p4 is implemented, in AArch32 state, PMCEID2, and PMCEID3.

- In AArch32 state, MRRC or MCRR accesses to PMCCNTR are reported using EC syndrome value 0x04.
While at EL0, accesses to the specified registers at EL0 are trapped, unless overridden by one of PMUSERENR_EL0.{ER, CR, SW}.

While at EL0, software can access all of the specified registers.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the PMUSERENR_EL0

Accesses to this register use the following encodings:

**MRS <Xt>, PMUSERENR_EL0**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b11</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```markdown
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return PMUSERENR_EL0;
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && EDSCR.SDD == '1' && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      return PMUSERENR_EL0;
    end if
  else
    return PMUSERENR_EL0;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      return PMUSERENR_EL0;
    end if
  else
    return PMUSERENR_EL0;
elsif PSTATE.EL == EL3 then
  return PMUSERENR_EL0;
else
  return PMUSERENR_EL0;
end if
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && Boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMUSERENR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  end
else
  PMUSERENR_EL0 = X[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && Boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMUSERENR_EL0 = X[t];
elsif PSTATE.EL == EL3 then
  PMUSERENR_EL0 = X[t];
PMXEVCNTR_EL0, Performance Monitors Selected Event Count Register

The PMXEVCNTR_EL0 characteristics are:

**Purpose**

Reads or writes the value of the selected event counter, \texttt{PMEVCNTR<n>\_EL0}. \texttt{PMSELR\_EL0}.SEL determines which event counter is selected.

**Configuration**

AArch64 System register PMXEVCNTR_EL0 bits [31:0] are architecturally mapped to AArch32 System register \texttt{PMEVCNTR[31:0]}.

This register is present only when FEAT\_PMUv3 is implemented. Otherwise, direct accesses to PMXEVCNTR_EL0 are UNDEFINED.

**Attributes**

PMXEVCNTR_EL0 is a 64-bit register.

**Field descriptions**

The PMXEVCNTR_EL0 bit assignments are:

When FEAT\_PMUv3p5 is implemented:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

\texttt{PMEVCNTR<n>}

\texttt{PMEVCNTR<n>}

PMXEVCNTR\(<n>\), bits [63:0]

Value of the selected event counter, \texttt{PMEVCNTR\(<n>\)\_EL0}, where \(n\) is the value stored in \texttt{PMSELR\_EL0}.SEL.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

\texttt{RES0}

\texttt{PMEVCNTR\(<n>\)\_EL0}

Bits [63:32]

Reserved, RES0.

PMXEVCNTR\(<n>\), bits [31:0]

Value of the selected event counter, \texttt{PMEVCNTR\(<n>\)\_EL0}, where \(n\) is the value stored in \texttt{PMSELR\_EL0}.SEL.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMXEVCNTR_EL0

If FEAT_FGT is implemented and PMSELR_EL0.SEL is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMXEVCNTR_EL0 is as follows:

- If PMSELR_EL0.SEL selects an unimplemented event counter, the access is UNDEFINED.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and PMSELR_EL0.SEL is greater than or equal to the number of accessible counters, then reads and writes of PMXEVCNTR_EL0 are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

- Accesses to the register are UNDEFINED.
- Accesses to the register behave as RAZ/WI.
- Accesses to the register execute as a NOP.
- Accesses to the register behave as if PMSELR_EL0.SEL has an UNKNOWN value less than the number of counters accessible at the current Exception level and Security state.
- If EL2 is implemented and enabled in the current Security state, and PMSELR_EL0.SEL is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

Note

In EL0, an access is permitted if it is enabled by PMUSERENR_EL0.{ER,EN}.

If EL2 is implemented and enabled in the current Security state, in EL1 and EL0, MDCR_EL2.HPMN identifies the number of accessible event counters. Otherwise, the number of accessible event counters is the number of implemented event counters. See MDCR_EL2.HPMN for more details.

Accesses to this register use the following encodings:

MRS <Xt>, PMXEVCNTR_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.<ER,EN> == '00' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        endif
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
    return PMXEVCNTR_EL0;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return PMXEVCNTR_EL0;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return PMXEVCNTR_EL0;
    endif
elsif PSTATE.EL == EL3 then
    return PMXEVCNTR_EL0;
endif

MSR PMXEVCNTR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end if;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMEVCNTRn_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        PMXEVCNTR_EL0 = X[t];
    end if;
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if;
        else
            PMXEVCNTR_EL0 = X[t];
        end if;
    elseif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if;
        else
            PMXEVCNTR_EL0 = X[t];
        end if;
    elseif PSTATE.EL == EL3 then
        PMXEVCNTR_EL0 = X[t];
    else
        PMXEVCNTR_EL0 = X[t];
    end if;
PMXEVTYPE_EL0, Performance Monitors Selected Event Type Register

The PMXEVTYPE_EL0 characteristics are:

**Purpose**

When PMSELR_EL0 SEL selects an event counter, this accesses a PMEVTYPE<n>_EL0 register. When PMSELR_EL0 SEL selects the cycle counter, this accesses PMCCFILTR_EL0.

**Configuration**

AArch64 System register PMXEVTYPE_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMXEVTYPE_EL0[31:0].

This register is present only when FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMXEVTYPE_EL0 are UNDEFINED.

**Attributes**

PMXEVTYPE_EL0 is a 64-bit register.

**Field descriptions**

The PMXEVTYPE_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
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<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Event type register or PMCCFILTR_EL0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**Bits [31:0]**

When PMSELR_EL0 SEL == 31, this register accesses PMCCFILTR_EL0.

Otherwise, this register accesses PMEVTYPE<n>_EL0 where n is the value in PMSELR_EL0 SEL.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMXEVTYPE_EL0**

If FEAT_FGT is implemented, and PMSELR_EL0 SEL is not 31 and is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMXEVTYPE_EL0 is as follows:

- If PMSELR_EL0 SEL selects an unimplemented event counter, the access is UNDEFINED.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented, and PMSELR_EL0 SEL is not 31 and is greater than or equal to the number of accessible counters, then reads and writes of PMXEVTYPE_EL0 are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

- Accesses to the register are UNDEFINED.
- Accesses to the register behave as RAZ/WI.
• Accesses to the register execute as a NOP.
• Accesses to the register behave as if PMSELR_EL0.SEL has an UNKNOWN value less than the number of event counters accessible at the current Exception level and Security state.
• Accesses to the register behave as if PMSELR_EL0.SEL is 31.
• If EL2 is implemented and enabled in the current Security state, PMSELR_EL0 is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

**Note**

In EL0, an access is permitted if it is enabled by PMUSERENR_EL0.EN.

If EL2 is implemented and enabled in the current Security state, in EL1 and EL0, MDCR_EL2.HPMN identifies the number of accessible event counters. Otherwise, the number of accessible event counters is the number of implemented event counters. See MDCR_EL2.HPMN for more details.

Accesses to this register use the following encodings:

MRS <Xt>, PMXEVTPER_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMEVTYPERn_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      return PMXEVTYPER_EL0;
    end if
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMEVTYPERn_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      return PMXEVTYPER_EL0;
    end if
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      return PMXEVTYPER_EL0;
    end if
  elsif PSTATE.EL == EL3 then
    return PMXEVTYPER_EL0;
else
  return PMXEVTYPER_EL0;
end if

MSR PMXEVTYPER_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end
  elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMXEVTYPER_EL0 = X[t];
  end
elsif PSTATE_EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMXEVTYPER_EL0 = X[t];
  end
elsif PSTATE_EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    PMXEVTYPER_EL0 = X[t];
  end
elsif PSTATE_EL == EL3 then
  PMXEVTYPER_EL0 = X[t];
else
  PMXEVTYPER_EL0 = X[t];
end
The REVIDR_EL1 characteristics are:

**Purpose**

Provides implementation-specific minor revision information.

**Configuration**

AArch64 System register REVIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register REVIDR[31:0].

If REVIDR_EL1 has the same value as MIDR_EL1, then its contents have no significance.

**Attributes**

REVIDR_EL1 is a 64-bit register.

**Field descriptions**

The REVIDR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED |

**IMPLEMENTATION DEFINED, bits [63:0]**

IMPLEMENTATION DEFINED.

**Accessing the REVIDR_EL1**

Accesses to this register use the following encodings:

**MRS <Xt>, REVIDR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if IsFeatureImplemented(FEAT_IDST) then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL1, 0x18);
        end
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TID1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.REVIDR_EL1 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return REVIDR_EL1;
    end
elsif PSTATE.EL == EL2 then
    return REVIDR_EL1;
eslif PSTATE.EL == EL3 then
    return REVIDR_EL1;
RGSR_EL1, Random Allocation Tag Seed Register.

The RGSR_EL1 characteristics are:

**Purpose**

Random Allocation Tag Seed Register.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to RGSR_EL1 are **UNDEFINED**.

When GCR_EL1.RRND==0b1, updates to RGSR_EL1 are implementation-specific.

**Attributes**

RGSR_EL1 is a 64-bit register.

**Field descriptions**

The RGSR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SEED | RES0 | TAG |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:24]**

Reserved, RES0.

**SEED, bits [23:8]**

Seed register used for generating values returned by RandomAllocationTag().

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [7:4]**

Reserved, RES0.

**TAG, bits [3:0]**

Tag generated by the most recent IRG instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the RGSR_EL1**

Accesses to this register use the following encodings:
MRS <Xt>, RGSR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.ATA == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    else
      return RGSR_EL1;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        return RGSR_EL1;
    elsif PSTATE.EL == EL3 then
      return RGSR_EL1;

MSR RGSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        RGSR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        RGSR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    RGSR_EL1 = X[t];
else
    RGSR_EL1 = X[t];
end if
The RMR_EL1 characteristics are:

**Purpose**

When this register is implemented:

- A write to the register at EL1 can request a Warm reset.
- If EL1 can use all Execution states, this register specifies the Execution state that the PE boots into on a Warm reset.

**Configuration**

AArch64 System register RMR_EL1 bits [31:0] are architecturally mapped to AArch32 System register RMR[31:0] when the highest implemented Exception level is EL1.

This register is present only when the highest implemented Exception level is EL1. Otherwise, direct accesses to RMR_EL1 are **UNDEFINED**.

When EL1 is the highest implemented Exception level:

- If EL1 can use all Execution states then this register must be implemented.
- If EL1 cannot use AArch32 then it is **IMPLEMENTATION DEFINED** whether the register is implemented.

**Attributes**

RMR_EL1 is a 64-bit register.

**Field descriptions**

The RMR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | RR AA64 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:2]**

Reserved, RES0.

**RR, bit [1]**

Reset Request. Setting this bit to 1 requests a Warm reset.

On a Warm reset, this field resets to 0.

**AA64, bit [0]**

When EL1 is capable of using AArch32:

When EL1 can use AArch32, determines which Execution state the PE boots into after a Warm reset:

<table>
<thead>
<tr>
<th>AA64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>AArch64.</td>
</tr>
</tbody>
</table>
On coming out of the Warm reset, execution starts at the implementation defined reset vector address of the specified Execution state.

If EL1 can only use AArch64 state, this bit is RAO/WI.

When implemented as a RW field, this field resets to 1 on a Cold reset.

**Otherwise:**

Reserved, RAO/WI.

### Accessing the RMR_EL1

Accesses to this register use the following encodings:

**MRS <Xt>, RMR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL1 && IsHighestEL(EL1) then
    return RMR_EL1;
else
    UNDEFINED;
```

**MSR RMR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL1 && IsHighestEL(EL1) then
    RMR_EL1 = X[t];
else
    UNDEFINED;
```
RMR_EL2, Reset Management Register (EL2)

The RMR_EL2 characteristics are:

**Purpose**

When this register is implemented:

- A write to the register at EL2 can request a Warm reset.
- If EL2 can use all Execution states, this register specifies the Execution state that the PE boots into on a Warm reset.

**Configuration**

AArch64 System register RMR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HRMR[31:0] when the highest implemented Exception level is EL2.

This register is present only when the highest implemented Exception level is EL2. Otherwise, direct accesses to RMR_EL2 are **UNDEFINED**.

When EL2 is the highest implemented Exception level:

- If EL2 can use all Execution states then this register must be implemented.
- If EL2 cannot use AArch32 then it is **IMPLEMENTATION DEFINED** whether the register is implemented.

**Attributes**

RMR_EL2 is a 64-bit register.

**Field descriptions**

The RMR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RR AA64 |

**Bits [63:2]**

Reserved, RES0.

**RR, bit [1]**

Reset Request. Setting this bit to 1 requests a Warm reset.

On a Warm reset, this field resets to 0.

**AA64, bit [0]**

When EL2 is capable of using AArch32:

When EL2 can use AArch32, determines which Execution state the PE boots into after a Warm reset:

<table>
<thead>
<tr>
<th>AA64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>AArch64.</td>
</tr>
</tbody>
</table>
On coming out of the Warm reset, execution starts at the implementation defined reset vector address of the specified Execution state.

If EL2 can only use AArch64 state, this bit is RAO/WI.

When implemented as a RW field, this field resets to 1 on a Cold reset.

Otherwise:

Reserved, RAO/WI.

Accessing the RMR_EL2

Accesses to this register use the following encodings:

**MRS <Xt>, RMR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif PSTATE.EL == EL2 && IsHighestEL(EL2) then
    return RMR_EL2;
else
    UNDEFINED;

**MSR RMR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif PSTATE.EL == EL2 && IsHighestEL(EL2) then
    RMR_EL2 = X[t];
else
    UNDEFINED;
RMR_EL3, Reset Management Register (EL3)

The RMR_EL3 characteristics are:

**Purpose**

If EL3 is the implemented and this register is implemented:

- A write to the register at EL3 can request a Warm reset.
- If EL3 can use all Execution states, this register specifies the Execution state that the PE boots into on a Warm reset.

**Configuration**

AArch64 System register RMR_EL3 bits [31:0] are architecturally mapped to AArch32 System register RMR[31:0] when EL3 is implemented.

This register is present only when EL3 is implemented. Otherwise, direct accesses to RMR_EL3 are undefined.

When EL3 is implemented:

- If EL3 can use all Execution states then this register must be implemented.
- If EL3 cannot use AArch32, then it is implementation defined whether the register is implemented.

Otherwise, direct accesses to RMR_EL3 are undefined.

**Attributes**

RMR_EL3 is a 64-bit register.

**Field descriptions**

The RMR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>RR, Reset Request. Setting this bit to 1 requests a Warm reset. On a Warm reset, this field resets to 0.</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>58</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>57</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>47</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>45</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>43</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>AArch32.</td>
</tr>
<tr>
<td>30</td>
<td>AArch64.</td>
</tr>
<tr>
<td>29</td>
<td>AArch32.</td>
</tr>
<tr>
<td>28</td>
<td>AArch64.</td>
</tr>
<tr>
<td>27</td>
<td>AArch32.</td>
</tr>
<tr>
<td>26</td>
<td>AArch64.</td>
</tr>
<tr>
<td>25</td>
<td>AArch32.</td>
</tr>
<tr>
<td>24</td>
<td>AArch64.</td>
</tr>
<tr>
<td>23</td>
<td>AArch32.</td>
</tr>
<tr>
<td>22</td>
<td>AArch64.</td>
</tr>
<tr>
<td>21</td>
<td>AArch32.</td>
</tr>
<tr>
<td>20</td>
<td>AArch64.</td>
</tr>
<tr>
<td>19</td>
<td>AArch32.</td>
</tr>
<tr>
<td>18</td>
<td>AArch64.</td>
</tr>
<tr>
<td>17</td>
<td>AArch32.</td>
</tr>
<tr>
<td>16</td>
<td>AArch64.</td>
</tr>
<tr>
<td>15</td>
<td>AArch32.</td>
</tr>
<tr>
<td>14</td>
<td>AArch64.</td>
</tr>
<tr>
<td>13</td>
<td>AArch32.</td>
</tr>
<tr>
<td>12</td>
<td>AArch64.</td>
</tr>
<tr>
<td>11</td>
<td>AArch32.</td>
</tr>
<tr>
<td>10</td>
<td>AArch64.</td>
</tr>
<tr>
<td>9</td>
<td>AArch32.</td>
</tr>
<tr>
<td>8</td>
<td>AArch64.</td>
</tr>
<tr>
<td>7</td>
<td>AArch32.</td>
</tr>
<tr>
<td>6</td>
<td>AArch64.</td>
</tr>
<tr>
<td>5</td>
<td>AArch32.</td>
</tr>
<tr>
<td>4</td>
<td>AArch64.</td>
</tr>
<tr>
<td>3</td>
<td>AArch32.</td>
</tr>
<tr>
<td>2</td>
<td>AArch64.</td>
</tr>
<tr>
<td>1</td>
<td>AArch32.</td>
</tr>
<tr>
<td>0</td>
<td>AArch64.</td>
</tr>
</tbody>
</table>

**AA64, bit [0]**

When EL3 is capable of using AArch32:

When EL3 can use AArch32, determines which Execution state the PE boots into after a Warm reset:
On coming out of the Warm reset, execution starts at the implementation-defined reset vector address of the specified execution state.

If EL3 can only use AArch64 state, this bit is RAO/WI.

When implemented as a RW field, this field resets to 1 on a Cold reset.

Otherwise:

Reserved, RAO/WI.

**Accessing the RMR_EL3**

Accesses to this register use the following encodings:

MRS <Xt>, RMR_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL3 && IsHighestEl(EL3) then
return RMR_EL3;
else
UNDEFINED;

MSR RMR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL3 && IsHighestEl(EL3) then
RMR_EL3 = X[t];
else
UNDEFINED;
The RNDR characteristics are:

**Purpose**

Random Number. Returns a 64-bit random number which is reseeded from the True Random Number source at an IMPLEMENTATION DEFINED rate.

If the hardware returns a genuine random number, PSTATE.NZCV is set to 0b0000.

If the instruction cannot return a genuine random number in a reasonable period of time, PSTATE.NZCV is set to 0b0100 and the data value returned is 0.

RNDR is a read-only register.

**Configuration**

This register is present only when FEAT_RNG is implemented. Otherwise, direct accesses to RNDR are UNDEFINED.

**Attributes**

RNDR is a 64-bit register.

**Field descriptions**

The RNDR bit assignments are:

```
   63  62  61  60  59  58  57  56  55  54  53  52  51  50  49  48  47  46  45  44  43  42  41  40  39  38  37  36  35  34  33  32  
     RNDR  
   31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9   8   7   6   5   4   3   2   1   0  
     RNDR  
```

**RNDR, bits [63:0]**

Random Number. Returns a 64-bit Random Number which is reseeded from the True Random Number source at an IMPLEMENTATION DEFINED rate.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the RNDR**

Accesses to this register use the following encodings:

```
MRS <Xt>, RNDR

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0010</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
    return RNDR;
elif PSTATE.EL == EL1 then
    return RNDR;
elif PSTATE.EL == EL2 then
    return RNDR;
elif PSTATE.EL == EL3 then
    return RNDR;

The RNDRRS characteristics are:

**Purpose**

Reseeded Random Number. Returns a 64-bit random number which is reseeded from the True Random Number source immediately before the read of the random number.

If the hardware returns a genuine random number, PSTATE.NZCV is set to \(0b0000\).

If the instruction cannot return a genuine random number in a reasonable period of time, PSTATE.NZCV is set to \(0b0100\) and the data value returned is 0.

RNDRRS is a read-only register.

**Configuration**

This register is present only when FEAT_RNG is implemented. Otherwise, direct accesses to RNDRRS are **UNDEFINED**.

**Attributes**

RNDRRS is a 64-bit register.

**Field descriptions**

The RNDRRS bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RNDRRS</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
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<td>58</td>
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<td>57</td>
<td></td>
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<td>56</td>
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<td>54</td>
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<td>53</td>
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<td>52</td>
<td></td>
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<td>51</td>
<td></td>
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<tr>
<td>50</td>
<td></td>
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<tr>
<td>49</td>
<td></td>
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<tr>
<td>48</td>
<td></td>
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<tr>
<td>47</td>
<td></td>
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<td>46</td>
<td></td>
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<tr>
<td>45</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td></td>
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<tr>
<td>40</td>
<td></td>
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<td>39</td>
<td></td>
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<tr>
<td>38</td>
<td></td>
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<tr>
<td>37</td>
<td></td>
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<tr>
<td>36</td>
<td></td>
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<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**RNDRRS, bits [63:0]**

Reseeded Random Number. Returns a 64-bit Random Number which is reseeded from the True Random Number source immediately before this read.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the RNDRRS**

Accesses to this register use the following encodings:

\[ MRS \ <Xt>, \ RNDRRS \]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0010</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  return RNDRRS;
elsif PSTATE.EL == EL1 then
  return RNDRRS;
elsif PSTATE.EL == EL2 then
  return RNDRRS;
elsif PSTATE.EL == EL3 then
  return RNDRRS;
RVBAR_EL1, Reset Vector Base Address Register (if EL2 and EL3 not implemented)

The RVBAR_EL1 characteristics are:

**Purpose**

If EL1 is the highest Exception level implemented, contains the IMPLEMENTATION DEFINED address that execution starts from after reset when executing in AArch64 state.

**Configuration**

This register is present only when the highest implemented Exception level is EL1. Otherwise, direct accesses to RVBAR_EL1 are UNDEFINED.

**Attributes**

RVBAR_EL1 is a 64-bit register.

**Field descriptions**

The RVBAR_EL1 bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reset Address | Reset Address |
| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |

**Bits [63:0]**

Reset Address. The IMPLEMENTATION DEFINED address that execution starts from after reset when executing in 64-bit state. Bits[1:0] of this register are 00, as this address must be aligned, and the address must be within the physical address size supported by the PE.

**Accessing the RVBAR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, RVBAR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && IsHighestEL(EL1) then
return RVBAR_EL1;
else
UNDEFINED;
RVBAR_EL2, Reset Vector Base Address Register (if EL3 not implemented)

The RVBAR_EL2 characteristics are:

**Purpose**

If EL2 is the highest Exception level implemented, contains the IMPLEMENTATION_DEFINED address that execution starts from after reset when executing in AArch64 state.

**Configuration**

This register is present only when the highest implemented Exception level is EL2. Otherwise, direct accesses to RVBAR_EL2 are UNDEFINED.

**Attributes**

RVBAR_EL2 is a 64-bit register.

**Field descriptions**

The RVBAR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**Bits [63:0]**

Reset Address. The IMPLEMENTATION_DEFINED address that execution starts from after reset when executing in 64-bit state. Bits[1:0] of this register are 00, as this address must be aligned, and the address must be within the physical address size supported by the PE.

**Accessing the RVBAR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, RVBAR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b0000</td>
<td>0b1100</td>
<td>0b100</td>
<td>0b11</td>
</tr>
</tbody>
</table>

```c
if PSTATE_EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif PSTATE_EL == EL2 && IsHighestEL(EL2) then
    return RVBAR_EL2;
else
    UNDEFINED;
```
RVBAR_EL3, Reset Vector Base Address Register (if EL3 implemented)

The RVBAR_EL3 characteristics are:

**Purpose**

If EL3 is the highest Exception level implemented, contains the IMPLEMENTATION DEFINED address that execution starts from after reset when executing in AArch64 state.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to RVBAR_EL3 are UNDEFINED.

Only implemented if the highest Exception level implemented is EL3.

**Attributes**

RVBAR_EL3 is a 64-bit register.

**Field descriptions**

The RVBAR_EL3 bit assignments are:

```
<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Reset Address</th>
<th>Reset Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60</td>
<td></td>
<td></td>
</tr>
<tr>
<td>59 58 57 56</td>
<td></td>
<td></td>
</tr>
<tr>
<td>55 54 53 52</td>
<td></td>
<td></td>
</tr>
<tr>
<td>51 50 49 48</td>
<td></td>
<td></td>
</tr>
<tr>
<td>47 46 45 44</td>
<td></td>
<td></td>
</tr>
<tr>
<td>43 42 41 40</td>
<td></td>
<td></td>
</tr>
<tr>
<td>39 38 37 36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>35 34 33 32</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 30 29 28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27 26 25 24</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23 22 21 20</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19 18 17 16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 14 13 12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11 10 9  8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7  6  5  4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3  2  1  0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**Bits [63:0]**

Reset Address. The IMPLEMENTATION DEFINED address that execution starts from after reset when executing in 64-bit state. Bits[1:0] of this register are 00, as this address must be aligned, and the address must be within the physical address size supported by the PE.

**Accessing the RVBAR_EL3**

Accesses to this register use the following encodings:

```
MRS <Xt>, RVBAR_EL3
```

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b11</td>
<td>0b110</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

```
if PSTATE.EL == EL3 && IsHighestEL(EL3) then
  return RVBAR_EL3;
else
  UNDEFINED;
```
The SYS S1_<op1>_<Cn>_<Cm>_<op2>, SYSL S1_<op1>_<Cn>_<Cm>_<op2>, IMPLEMENTATION DEFINED maintenance instructions

Purpose

This area of the System instruction encoding space is reserved for IMPLEMENTATION DEFINED System instructions.

Configuration

There are no configuration notes.

Attributes

SYS S1_<op1>_<Cn>_<Cm>_<op2>, SYSL S1_<op1>_<Cn>_<Cm>_<op2> is a 64-bit System instruction.

Field descriptions

The SYS S1_<op1>_<Cn>_<Cm>_<op2>, SYSL S1_<op1>_<Cn>_<Cm>_<op2> input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

Executing the SYS S1_<op1>_<Cn>_<Cm>_<op2>, SYSL S1_<op1>_<Cn>_<Cm>_<op2> instruction

Accesses to this instruction use the following encodings:

SYS #<op1>, <Cn>, <Cm>, #<op2>{, <Xt>}
<table>
<thead>
<tr>
<th>0b01</th>
<th>op1[2:0]</th>
<th>0b1x11</th>
<th>Cm[3:0]</th>
<th>op2[2:0]</th>
</tr>
</thead>
</table>

```c
if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TIDCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    IMPLEMENTATION_DEFINED "SYS";
else
  IMPLEMENTATION_DEFINED "SYS";
```
S3_<op1>_<_Cn>_<_Cm>_<_op2>, IMPLEMENTATION DEFINED registers

The S3_<op1>_<_Cn>_<_Cm>_<_op2> characteristics are:

**Purpose**

This area of the instruction set space is reserved for IMPLEMENTATION DEFINED registers.

**Configuration**

There are no configuration notes.

**Attributes**

S3_<op1>_<_Cn>_<_Cm>_<_op2> is a 64-bit register.

**Field descriptions**

The S3_<op1>_<_Cn>_<_Cm>_<_op2> bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>61</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>60</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>59</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>58</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>57</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>56</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>55</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>54</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>53</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>52</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>51</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>50</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>49</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>48</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>47</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>46</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>45</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>44</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>43</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>42</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>41</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>40</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>39</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>38</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>37</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>36</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>35</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>34</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>33</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>32</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**Accessing the S3_<op1>_<_Cn>_<_Cm>_<_op2>**

Accesses to this register use the following encodings:

MRS <Xt>, S3_<op1>_C<Cn>_C<Cm>_<_op2>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>op1[2:0]</td>
<td>0b1x11</td>
<td>Cm[3:0]</td>
<td>op2[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 then
if EL2Enabled() && HCR_EL2.TIDCP == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    IMPLEMENTATION_DEFINED "S3";
else
    IMPLEMENTATION_DEFINED "S3";

MSR S3_<op1>_C<Cn>_C<Cm>_<_op2>, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>op1[2:0]</td>
<td>0b1x11</td>
<td>Cm[3:0]</td>
<td>op2[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL1 then
    if EL2Enabled() && HCR_EL2.TIDCP == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        IMPLEMENTATION_DEFINED "S3";
else
    IMPLEMENTATION_DEFINED "S3";
The SCR_EL3 characteristics are:

**Purpose**

Defines the configuration of the current Security state. It specifies:

- The Security state of EL0, EL1, and EL2. The Security state is either Secure or Non-secure.
- The Execution state at lower Exception levels.
- Whether IRQ, FIQ, SError interrupts, and External abort exceptions are taken to EL3.
- Whether various operations are trapped to EL3.

**Configuration**

AArch64 System register SCR_EL3 bits [31:0] can be mapped to AArch32 System register SCR[31:0], but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to SCR_EL3 are UNDEFINED.

**Attributes**

SCR_EL3 is a 64-bit register.

**Field descriptions**

The SCR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>HXEn</td>
<td>Enables access to the HCRX_EL2 register at EL2 from EL3.</td>
</tr>
<tr>
<td>62</td>
<td>FIEN</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>NMEA</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>60</td>
<td>EASE</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>59</td>
<td>EEL2</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>58</td>
<td>API</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>57</td>
<td>APK</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>56</td>
<td>TERR</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55</td>
<td>TLOR</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>54</td>
<td>TWE</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>53</td>
<td>TWI</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>52</td>
<td>ST</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>51</td>
<td>RW</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>50</td>
<td>SIF</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>49</td>
<td>HCE</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>48</td>
<td>SMD</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>47</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>46</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>45</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>44</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>43</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>42</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>41</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>40</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>39</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>38</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>37</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>36</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>34</td>
<td></td>
<td>Reserved, RES0.</td>
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<tr>
<td>33</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>32</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>26</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>24</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>23</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>22</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>21</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>20</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>16</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>14</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>12</td>
<td></td>
<td>Reserved, RES0.</td>
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<tr>
<td>11</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [63:39]**

Reserved, RES0.

**HXEn, bit [38]**

When FEAT_HCX is implemented:

<table>
<thead>
<tr>
<th>HXEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 accesses to HCRX_EL2 are trapped to EL3. Indirect reads of HCRX_EL2 return 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
**ADEn, bit [37]**

When FEAT_LS64 is implemented:

Enables access to the ACCDATA_EL1 register at EL1 and EL2.

<table>
<thead>
<tr>
<th>ADEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to ACCDATA_EL1 at EL1 and EL2 are trapped to EL3, unless the accesses are trapped to EL2 by the EL2 fine-grained trap.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause accesses to ACCDATA_EL1 to be trapped.</td>
</tr>
</tbody>
</table>

If the HFGWTR_EL2.nACCDATA_EL1 or HFGRTR_EL2.nACCDATA_EL1 traps are enabled, they take priority over this trap.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**EnAS0, bit [36]**

When FEAT_LS64 is implemented:

Traps execution of an ST64BV0 instruction at EL0, EL1, or EL2 to EL3.

<table>
<thead>
<tr>
<th>EnAS0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 execution of an ST64BV0 instruction is trapped to EL3, unless it is trapped to EL1 by SCTLR_EL1.EnAS0, or to EL2 by either HCRX_EL2.EnAS0 or SCTLR_EL2.EnAS0. EL1 execution of an ST64BV0 instruction is trapped to EL3, unless it is trapped to EL2 by HCRX_EL2.EnAS0. EL2 execution of an ST64BV0 instruction is trapped to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV0 instruction is reported using an ESR_ELx.EC value of 0x0A, with an ISS code of 0x0000001.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**AMVOFFEN, bit [35]**

When FEAT_AMUv1p1 is implemented:

Activity Monitors Virtual Offsets Enable.

<table>
<thead>
<tr>
<th>AMVOFFEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to AMEVCNTVOFF0&lt;n&gt;_EL2 and AMEVCNTVOFF1&lt;n&gt;_EL2 at EL2 are trapped to EL3. Indirect reads of the virtual offset registers are zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to AMEVCNTVOFF0&lt;n&gt;_EL2 and AMEVCNTVOFF1&lt;n&gt;_EL2 are not affected by this field.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
Bit [34]

Reserved, RES0.

TWDEL, bits [33:30]

When FEAT_TWED is implemented:

TWE Delay. A 4-bit unsigned number that, when SCR_EL3.TWEDEn is 1, encodes the minimum delay in taking a trap of WFE* caused by SCR_EL3.TWE as \(2^{(TWDEL + 8)}\) cycles.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TWDEn, bit [29]

When FEAT_TWED is implemented:

TWE Delay Enable. Enables a configurable delayed trap of the WFE* instruction caused by SCR_EL3.TWE.

<table>
<thead>
<tr>
<th>TWDEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The delay for taking the trap is IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The delay for taking the trap is at least the number of cycles defined in SCR_EL3.TWDEL.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

ECVEn, bit [28]

When FEAT_ECV is implemented:

ECV Enable. Enables access to the CNTPOFF_EL2 register.

<table>
<thead>
<tr>
<th>ECVEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 accesses to CNTPOFF_EL2 are trapped to EL3, and the value of CNTPOFF_EL2 is treated as 0 for all purposes other than direct reads or writes to the register from EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 accesses to CNTPOFF_EL2 are not trapped to EL3 by this mechanism.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

FGTEn, bit [27]

When FEAT_FGT is implemented:

Fine-Grained Traps Enable. When EL2 is implemented, enables access to HAFGRTR_EL2, HDFGRTR_EL2, HDFGWTR_EL2, HFGTR_EL2, HFGITR_EL2 and HFGWTR_EL2.

Note
If EL2 is not implemented but EL3 is implemented, FEAT_FGT implements the MDCR_EL3 TDCC traps.

<table>
<thead>
<tr>
<th>FGTEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 accesses to HAFGRTR_EL2, HDFGRTR_EL2, HDFGWTR_EL2, HFGRTR_EL2, HFGITR_EL2, and HFGWTR_EL2 registers are trapped to EL3, and those registers behave as if all bits are set to 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 accesses to HAFGRTR_EL2, HDFGRTR_EL2, HDFGWTR_EL2, HFGRTR_EL2, HFGITR_EL2, and HFGWTR_EL2 registers are not trapped to EL3 by this mechanism.</td>
</tr>
</tbody>
</table>

Traps caused by accesses to the fine-grained trap registers are reported using an ESR_ELx.EC value of 0x18 and its associated ISS.

Otherwise:

Reserved, RES0.

ATA, bit [26]

When FEAT_MTE2 is implemented:

Allocation Tag Access. Controls access at EL2, EL1 and EL0 to Allocation Tags.

When access is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.
- MRS and MSR instructions at EL1 and EL2 using GCR_EL1, RGSR_EL1, TFSR_EL1, TFSR_EL2 or TFSRE0_EL1 that are not UNDEFINED or trapped to a lower Exception level are trapped to EL3.
- MRS and MSR instructions at EL2 using TFSR_EL12 that are not UNDEFINED are trapped to EL3.

<table>
<thead>
<tr>
<th>ATA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access is not prevented.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EnSCXT, bit [25]

When FEAT_CSV2 is implemented:

Enable access to the SCXTNUM_EL2, SCXTNUM_EL1, and SCXTNUM_EL0 registers. The defined values are:
EnSCXT

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [24:22]**

Reserved, RES0.

**FIEN, bit [21]**

*When FEAT_RASv1p1 is implemented:*

Fault Injection enable. Trap accesses to the registers ERXPFGCDN_EL1, ERXPFGCTL_EL1, and ERXPFGF_EL1 from EL1 and EL2 to EL3, reported using an ESR_ELx.EC value of 0x18.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

If EL3 is not implemented, the Effective value of SCR_EL3.FIEN is 0b1.

If ERRIDR_EL1.NUM is zero, meaning no error records are implemented, or no error record accessible using System registers is owned by a node that implements the RAS Common Fault Injection Model Extension, then this bit might be RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**NMEA, bit [20]**

*When FEAT_DoubleFault is implemented:*

Non-maskable External Aborts. When SCR_EL3.EA == 1, controls whether PSTATE.A masks SError interrupts at EL3.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

When SCR_EL3.EA == 0:

- Asserted SError interrupts are not taken at EL3 regardless of the value of PSTATE.A and this field.
- This field is ignored and its Effective value is 0.

On a Warm reset, this field resets to 0.
Reserved, RES0.

**EASE, bit [19]**

*When FEAT_DoubleFault is implemented:*

External aborts to SError interrupt vector.

<table>
<thead>
<tr>
<th>EASE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Synchronous External abort exceptions taken to EL3 are taken to the appropriate synchronous exception vector offset from VBAR_EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>Synchronous External abort exceptions taken to EL3 are taken to the appropriate SError interrupt vector offset from VBAR_EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**EEL2, bit [18]**

*When FEAT_SEL2 is implemented:*

Secure EL2 Enable.

<table>
<thead>
<tr>
<th>EEL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All behaviors associated with Secure EL2 are disabled. All registers, including timer registers, defined by FEAT_SEL2 are UNDEFINED, and those timers are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>All behaviors associated with Secure EL2 are enabled.</td>
</tr>
</tbody>
</table>

When the value of this bit is 1, then:

- When SCR_EL3.NS == 0, the SCR_EL3.RW bit is treated as 1 for all purposes other than reading or writing the register.

- If Secure EL1 is using AArch32, then any of the following operations, executed in Secure EL1, is trapped to Secure EL2, using the EC value of ESR_EL2.EC == 0x3:
  - A read or write of the SCR.
  - A read or write of the NSACR.
  - A read or write of the MVBAR.
  - A read or write of the SDCR.
  - Execution of an ATS12NSO** instruction.

- If Secure EL1 is using AArch32, then any of the following operations, executed in Secure EL1, is trapped to Secure EL2 using the EC value of ESR_EL2.EC == 0x0:
  - Execution of an SRS instruction that uses R13_mon.
  - Execution of an MRS (Banked register) or MSR (Banked register) instruction that would access SPSR_mon, R13_mon, or R14_mon.

**Note**

If the Effective value of SCR_EL3.EEL2 is 0, then these operations executed in Secure EL1 using AArch32 are trapped to EL3.

A Secure only implementation that does not implement EL3 but implements EL2, behaves as if SCR_EL3.EEL2 == 1. This bit is permitted to be cached in a TLB.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**API, bit [17]**

**When FEAT_SEL2 is implemented and FEAT_PAuth is implemented:**

Controls the use of the following instructions related to Pointer Authentication. Traps are reported using an ESR_ELx.EC value of 0x09:

- PACGA, which is always enabled.
- AUTDA, AUTDB, AUTDZA, AUTDZB, AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZA, AUTIZB, PACDA, PACDB, PACDZA, PACDZB, PACIA, PACIA1716, PACIASP, PACIAZ, PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZA, PACIZB, RETAA, RETAB, BRAA, BRAB, BLRAA, BLRAB, BRAAZ, BRABZ, BLRAAZ, BLRBZ, ERATAA, ERETAB, LDRAA and LDRAB when:
  - In EL0, when **HCR_EL2.TGE == 0 or HCR_EL2.E2H == 0**, and the associated **SCTLR_EL1.En<N><M> == 1**.
  - In EL0, when **HCR_EL2.TGE == 1 and HCR_EL2.E2H == 1**, and the associated **SCTLR_EL2.En<N><M> == 1**.
  - In EL1, when the associated **SCTLR_EL1.En<N><M> == 1**.
  - In EL2, when the associated **SCTLR_EL2.En<N><M> == 1**.

<table>
<thead>
<tr>
<th>API</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The use of any instruction related to pointer authentication in any Exception level except EL3 when the instructions are enabled are trapped to EL3 unless they are trapped to EL2 as a result of the <strong>HCR_EL2.API</strong> bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

An instruction is trapped only if Pointer Authentication is enabled for that instruction, for more information, see 'System register control of pointer authentication'.

**Note**

If FEAT_PAuth is implemented but EL3 is not implemented, the system behaves as if this bit is 1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When FEAT_SEL2 is not implemented and FEAT_PAuth is implemented:**

Controls the use of instructions related to Pointer Authentication:

- PACGA.
- AUTDA, AUTDB, AUTDZA, AUTDZB, AUTIA, AUTIA1716, AUTIASP, AUTIAZ, AUTIB, AUTIB1716, AUTIBSP, AUTIBZ, AUTIZA, AUTIZB, PACDA, PACDB, PACDZA, PACDZB, PACIA, PACIA1716, PACIASP, PACIAZ, PACIB, PACIB1716, PACIBSP, PACIBZ, PACIZA, PACIZB, RETAA, RETAB, BRAA, BRAB, BLRAA, BLRAB, BRAAZ, BRABZ, BLRAAZ, BLRBZ, ERATAA, ERETAB, LDRAA and LDRAB when:
  - In Non-secure EL0, when **HCR_EL2.TGE == 0 or HCR_EL2.E2H == 0**, and the associated **SCTLR_EL1.En<N><M> == 1**.
  - In Non-secure EL0, when **HCR_EL2.TGE == 1 and HCR_EL2.E2H == 1**, and the associated **SCTLR_EL2.En<N><M> == 1**.
  - In Secure EL0, when the associated **SCTLR_EL2.En<N><M> == 1**.
  - In Secure or Non-secure EL1, when the associated **SCTLR_EL1.En<N><M> == 1**.
  - In EL2, when the associated **SCTLR_EL2.En<N><M> == 1**.

<table>
<thead>
<tr>
<th>API</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The use of any instruction related to pointer authentication in any Exception level except EL3 when the instructions are enabled are trapped to EL3 unless they are trapped to EL2 as a result of the <strong>HCR_EL2.API</strong> bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
Note

If FEAT_PAuth is implemented but EL3 is not implemented, the system behaves as if this bit is 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

APK, bit [16]

When FEAT_PAuth is implemented:

Trap registers holding "key" values for Pointer Authentication. Traps accesses to the following registers, using an ESR_ELx.EC value of 0x18, from EL1 or EL2 to EL3 unless they are trapped to EL2 as a result of the HCR_EL2.APK bit or other traps:

- APIAKeyLo_EL1, APIAKeyHi_EL1, APIBKeyLo_EL1, APIBKeyHi_EL1.
- APDAKeyLo_EL1, APDAKeyHi_EL1, APDBKeyLo_EL1, APDBKeyHi_EL1.
- APGAKeyLo_EL1, and APGAKeyHi_EL1.

<table>
<thead>
<tr>
<th>APK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to the registers holding &quot;key&quot; values for pointer authentication from EL1 or EL2 are trapped to EL3 unless they are trapped to EL2 as a result of the HCR_EL2.APK bit or other traps.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

For more information, see 'System register control of pointer authentication'.

Note

If FEAT_PAuth is implemented but EL3 is not implemented, the system behaves as if this bit is 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TERR, bit [15]

When FEAT_RAS is implemented:

Trap Error record accesses. Accesses to the RAS ERR* and RAS ERX* registers from EL1 and EL2 to EL3 are trapped as follows:

- Accesses from EL1 and EL2 using AArch64 to the following registers are trapped and reported using an ESR_ELx.EC value of 0x18:
  - ERRDR_EL1, ERRSELRL_EL1, ERXADDR_EL1, ERXCTRL_EL1, ERXFR_EL1, ERXMISC0_EL1, ERXMISC1_EL1, and ERXSTATUS_EL1.
- If FEAT_RASv1p1 is implemented, accesses from EL1 and EL2 using AArch64 to ERXMISC2_EL1, and ERXMISC3_EL1, are trapped and reported using an ESR_ELx.EC value of 0x18.
- Accesses from EL1 and EL2 using AArch32, to the following registers are trapped and reported using an ESR_ELx.EC value of 0x03:
ERRIDR, ERRSELR, ERXADDR, ERXADDR2, ERXCTLRL, ERXCTLRL2, ERXFR, ERXFR2, ERXMISC0, ERXMISC1, ERXMISC2, ERXMISC3, and ERXSTATUS.

- If FEAT_RASv1p1 is implemented, accesses from EL1 and EL2 using AArch32 to the following registers are trapped and reported using an ESR_ELx.EC value of 0x03:
  - ERXMISC4, ERXMISC5, ERXMISC6, and ERXMISC7.

<table>
<thead>
<tr>
<th>TERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to the specified registers from EL1 and EL2 generate a Trap exception to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TLOR, bit [14]

When FEAT_LOR is implemented:

Trap LOR registers. Traps accesses to the LORSA_EL1, LOREA_EL1, LORN_EL1, LORC_EL1, and LORID_EL1 registers from EL1 and EL2 to EL3, unless the access has been trapped to EL2.

<table>
<thead>
<tr>
<th>TLOR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 and EL2 accesses to the LOR registers that are not UNDEFINED are trapped to EL3, unless it is trapped HCR_EL2.TLOR.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TWE, bit [13]

Traps EL2, EL1, and EL0 execution of WFE instructions to EL3, from both Security states and both Execution states, reported using an ESR_ELx.EC value of 0x01.

When FEAT_WFxT is implemented, this trap also applies to the WFET instruction.

<table>
<thead>
<tr>
<th>TWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFE instruction at any Exception level lower than EL3 is trapped to EL3, if the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by SCTLR.nTWE, HCR.TWE, SCTLR_EL1.nTWE, SCTLR_EL2.nTWE, or HCR_EL2.TWE.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

Note

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.
For more information about when WFE instructions can cause the PE to enter a low-power state, see 'Wait for Event mechanism and Send event'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TWI, bit [12]**

Traps EL2, EL1, and EL0 execution of WFI instructions to EL3, from both Security states and both Execution states, reported using an ESR_ELx.EC value of 0x01.

When **FEAT_WFxT** is implemented, this trap also applies to the WFIT instruction.

<table>
<thead>
<tr>
<th>TWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFI instruction at any Exception level lower than EL3 is trapped to EL3, if the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by <strong>SCTLR.nTWI</strong>, <strong>HCR.TWI</strong>, <strong>SCTLR_EL1.nTWI</strong>, <strong>SCTLR_EL2.nTWI</strong>, or <strong>HCR_EL2.TWI</strong>.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

For more information about when WFI instructions can cause the PE to enter a low-power state, see ‘Wait for Interrupt’.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ST, bit [11]**

Traps Secure EL1 accesses to the Counter-timer Physical Secure timer registers to EL3, from AArch64 state only, reported using an ESR_ELx.EC value of 0x18.

<table>
<thead>
<tr>
<th>ST</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure EL1 using AArch64 accesses to the <strong>CNTPS.TVAL_EL1</strong>, <strong>CNTPS.CTL_EL1</strong>, and <strong>CNTPS.CVAL_EL1</strong> are trapped to EL3 when Secure EL2 is disabled. If Secure EL2 is enabled, the behavior is as if the value of this field was 0b1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

**Note**

Accesses to the Counter-timer Physical Secure timer registers are always enabled at EL3. These registers are not accessible at EL0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**RW, bit [10]**

When AArch32 is supported at any Exception level:

Execution state control for lower Exception levels.
SCR_EL3, Secure Configuration Register

<table>
<thead>
<tr>
<th>RW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Lower levels are all AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>The next lower level is AArch64.</td>
</tr>
<tr>
<td></td>
<td>If EL2 is present:</td>
</tr>
<tr>
<td></td>
<td>• EL2 is AArch64.</td>
</tr>
<tr>
<td></td>
<td>• EL2 controls EL1 and EL0 behaviors.</td>
</tr>
<tr>
<td></td>
<td>If EL2 is not present:</td>
</tr>
<tr>
<td></td>
<td>• EL1 is AArch64.</td>
</tr>
<tr>
<td></td>
<td>• EL0 is determined by the Execution state described in the</td>
</tr>
<tr>
<td></td>
<td>current process state when executing at EL0.</td>
</tr>
</tbody>
</table>

If AArch32 state is not supported by the implementation at EL2 and AArch32 state is not supported by the implementation at EL1, then this bit is RAO/WI.

If AArch32 state is supported by the implementation at EL1, SCR_EL3.NS == 1 and AArch32 state is not supported by the implementation at EL2, the Effective value of this bit is 1.

If AArch32 state is supported by the implementation at EL1, FEAT_SEL2 is implemented and SCR_EL3.{EEL2, NS} == {1, 0}, the Effective value of this bit is 1.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RAO/WI.

**SIF, bit [9]**

**When FEAT_SEL2 is implemented:**

Secure instruction fetch. When the PE is in Secure state, this bit disables instruction fetch from memory marked in the first stage of translation as being Non-secure. The possible values for this bit are:

<table>
<thead>
<tr>
<th>SIF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state instruction fetches from memory marked in the first stage</td>
</tr>
<tr>
<td></td>
<td>of translation as being Non-secure are permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure state instruction fetches from memory marked in the first stage</td>
</tr>
<tr>
<td></td>
<td>of translation as being Non-secure are not permitted.</td>
</tr>
</tbody>
</table>

When FEAT_PAN3 is implemented, it is IMPLEMENTATION DEFINED whether SCR_EL3.SIF is also used to determine instruction access permission for the purpose of PAN.

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Secure instruction fetch. When the PE is in Secure state, this bit disables instruction fetch from Non-secure memory.

<table>
<thead>
<tr>
<th>SIF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state instruction fetches from Non-secure memory are permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure state instruction fetches from Non-secure memory are not</td>
</tr>
<tr>
<td></td>
<td>permitted.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
HCE, bit [8]

Hypervisor Call instruction enable. Enables HVC instructions at EL3 and, if EL2 is enabled in the current Security state, at EL2 and EL1, in both Execution states, reported using an ESR_ELx.EC value of 0x00.

<table>
<thead>
<tr>
<th>HCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>HVC instructions are UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>HVC instructions are enabled at EL3, EL2, and EL1.</td>
</tr>
</tbody>
</table>

**Note**

HVC instructions are always UNDEFINED at EL0 and, if Secure EL2 is disabled, at Secure EL1. Any resulting exception is taken from the current Exception level to the current Exception level.

If EL2 is not implemented, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

SMD, bit [7]

Secure Monitor Call disable. Disables SMC instructions at EL1 and above, from both Security states and both Execution states, reported using an ESR_ELx.EC value of 0x00.

<table>
<thead>
<tr>
<th>SMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SMC instructions are enabled at EL3, EL2 and EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>SMC instructions are UNDEFINED.</td>
</tr>
</tbody>
</table>

**Note**

SMC instructions are always UNDEFINED at EL0. Any resulting exception is taken from the current Exception level to the current Exception level.

If HCR_EL2.TSC or HCR.TSC traps attempted EL1 execution of SMC instructions to EL2, that trap has priority over this disable.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [6]

Reserved, RES0.

Bits [5:4]

Reserved, RES1.

EA, bit [3]

External Abort and SError interrupt routing.

<table>
<thead>
<tr>
<th>EA</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0 | When executing at Exception levels below EL3, External aborts and SError interrupts are not taken to EL3. In addition, when executing at EL3:  
• SError interrupts are not taken.  
• External aborts are taken to EL3. |
| 0b1 | When executing at any Exception level, External aborts and SError interrupts are taken to EL3. |

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
FIQ, bit [2]

Physical FIQ Routing.

<table>
<thead>
<tr>
<th>FIQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When executing at Exception levels below EL3, physical FIQ interrupts are not taken to EL3. When executing at EL3, physical FIQ interrupts are not taken.</td>
</tr>
<tr>
<td>0b1</td>
<td>When executing at any Exception level, physical FIQ interrupts are taken to EL3.</td>
</tr>
</tbody>
</table>

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IRQ, bit [1]

Physical IRQ Routing.

<table>
<thead>
<tr>
<th>IRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When executing at Exception levels below EL3, physical IRQ interrupts are not taken to EL3. When executing at EL3, physical IRQ interrupts are not taken.</td>
</tr>
<tr>
<td>0b1</td>
<td>When executing at any Exception level, physical IRQ interrupts are taken to EL3.</td>
</tr>
</tbody>
</table>

For more information, see 'Asynchronous exception routing'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

NS, bit [0]

Non-secure bit.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Indicates that EL0 and EL1 are in Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Indicates that Exception levels lower than EL3 are in Non-secure state, so memory accesses from those Exception levels cannot access Secure memory.</td>
</tr>
</tbody>
</table>

When SCR_EL3.{EEL2, NS} == {1, 0}, then EL2 is using AArch64 and in Secure state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SCR_EL3

Accesses to this register use the following encodings:

\[
\text{MRS} \, <\text{Xt}>, \, \text{SCR}_{-}\text{EL3}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then UNDEFINED;
elsiif PSTATE.EL == EL1 then UNDEFINED;
elsiif PSTATE.EL == EL2 then UNDEFINED;
elsiif PSTATE.EL == EL3 then return SCR_EL3;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elseif PSTATE.EL == EL3 then
    SCR_EL3 = X[t];
The SCTLR_EL1 characteristics are:

**Purpose**

Provides top level control of the system, including its memory system, at EL1 and EL0.

**Configuration**

AArch64 System register SCTLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register SCTLR[31:0].

**Attributes**

SCTLR_EL1 is a 64-bit register.

**Field descriptions**

The SCTLR_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| EPAN| EnALS| EnAS0| EnASR| RES0| TWEDEL| TWEDEN| DS5E| EnIA| EnIBLSMAOE| nTLSMD| EnDAUCI| EE| E0E| SPAN| EIS| IESB| TSCXT| WXN| nTWE| RES0| nTWI| UCT| DZE| EnDB| I |

**Bits [63:58]**

Reserved, RES0.

**EPAN, bit [57]**

When FEAT_PAN3 is implemented:

Enhanced Privileged Access Never. When PSTATE.PAN is 1, determines whether an EL1 data access to a page with stage 1 EL0 instruction access permission generates a Permission fault as a result of the Privileged Access Never mechanism.

<table>
<thead>
<tr>
<th>EPAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No additional Permission faults are generated by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>An EL1 data access to a page with stage 1 EL0 data access permission or stage 1 EL0 instruction access permission generates a Permission fault. Any speculative data accesses that would generate a Permission fault if the accesses were not speculative will not cause an allocation into a cache.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**EnALS, bit [56]**
When FEAT_LS64 is implemented:

When \texttt{HCR\_EL2.\{E2H, TGE\} \neq \{1, 1\}}, traps execution of an LD64B or ST64B instruction at EL0 to EL1.

<table>
<thead>
<tr>
<th>EnALS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an LD64B or ST64B instruction at EL0 is trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an LD64B or ST64B instruction is reported using an ESR\_ELx.EC value of 0x0A, with an ISS code of 0x0000002.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \texttt{UNKNOWN} value.

Otherwise:

Reserved, RES0.

\textbf{EnAS0, bit [55]}

When FEAT_LS64 is implemented:

When \texttt{HCR\_EL2.\{E2H, TGE\} \neq \{1, 1\}}, traps execution of an ST64BV0 instruction at EL0 to EL1.

<table>
<thead>
<tr>
<th>EnAS0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV0 instruction at EL0 is trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV0 instruction is reported using an ESR\_ELx.EC value of 0x0A, with an ISS code of 0x0000001.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \texttt{UNKNOWN} value.

Otherwise:

Reserved, RES0.

\textbf{EnASR, bit [54]}

When FEAT_LS64 is implemented:

When \texttt{HCR\_EL2.\{E2H, TGE\} \neq \{1, 1\}}, traps execution of an ST64BV instruction at EL0 to EL1.

<table>
<thead>
<tr>
<th>EnASR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV instruction at EL0 is trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV instruction is reported using an ESR\_ELx.EC value of 0x0A, with an ISS code of 0x0000000.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \texttt{UNKNOWN} value.

Otherwise:

Reserved, RES0.

\textbf{Bits [53:50]}

Reserved, RES0.
**TWEDEL, bits [49:46]**

When `FEAT_TWED` is implemented:

TWE Delay. A 4-bit unsigned number that, when `SCTLR_EL1.TWEDEn` is 1, encodes the minimum delay in taking a trap of WFE* caused by `SCTLR_EL1.nTWE` as $2^{(TWEDEL + 8)}$ cycles.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TWEDEn, bit [45]**

When `FEAT_TWED` is implemented:

TWE Delay Enable. Enables a configurable delayed trap of the WFE* instruction caused by `SCTLR_EL1.nTWE`.

<table>
<thead>
<tr>
<th>TWEDEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The delay for taking the trap is IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The delay for taking the trap is at least the number of cycles defined in <code>SCTLR_EL1.TWEDEL</code>.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**DSSBS, bit [44]**

When `FEAT_SSBS` is implemented:

Default PSTATE.SSBS value on Exception Entry. The defined values are:

<table>
<thead>
<tr>
<th>DSSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.SSBS is set to 0 on an exception to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>PSTATE.SSBS is set to 1 on an exception to EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an IMPLEMENTATION DEFINED value.

Otherwise:

Reserved, RES0.

**ATA, bit [43]**

When `FEAT_MTE2` is implemented:

Allocation Tag Access in EL1. When `SCR_EL3.ATA=1` and `HCR_EL2.ATA=1`, controls EL1 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.
<table>
<thead>
<tr>
<th>ATA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**ATA0, bit [42]**

**When FEAT_MTE2 is implemented:**

Allocation Tag Access in EL0. When $\text{SCR\_EL3}.\text{ATA}=1$, $\text{HCR\_EL2}.\text{ATA}=1$, and $\text{HCR\_EL2}.\{\text{E2H, TGE}\} \neq \{1, 1\}$, controls EL0 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.

<table>
<thead>
<tr>
<th>ATA0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

**Note**

Software may change this control bit on a context switch.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**TCF, bits [41:40]**

**When FEAT_MTE2 is implemented:**

Tag Check Fault in EL1. Controls the effect of Tag Check Faults due to Loads and Stores in EL1.

If FEAT_MTE3 is not implemented, the value 0b11 is reserved.
### Reference Pages: 1407

<table>
<thead>
<tr>
<th>TCF</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Tag Check Faults have no effect on the PE.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Tag Check Faults cause a synchronous exception.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are asynchronously accumulated on writes.</td>
<td>When FEAT_MTE3 is implemented</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally `UNKNOWN` value.

**Otherwise:**

Reserved, RES0.

**TCF0, bits [39:38]**

**When FEAT_MTE2 is implemented:**

Tag Check Fault in EL0. When `HCR_EL2.{E2H,TGE} != {1,1}`, controls the effect of Tag Check Faults due to Loads and Stores in EL0.

If FEAT_MTE3 is not implemented, the value `0b11` is reserved.

**Note**

Software may change this control bit on a context switch.

<table>
<thead>
<tr>
<th>TCF0</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Tag Check Faults have no effect on the PE.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Tag Check Faults cause a synchronous exception.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are asynchronously accumulated on writes.</td>
<td>When FEAT_MTE3 is implemented</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally `UNKNOWN` value.

**Otherwise:**

Reserved, RES0.

**ITFSB, bit [37]**

**When FEAT_MTE2 is implemented:**

When synchronous exceptions are not being generated by Tag Check Faults, this field controls whether on exception entry into EL1, all Tag Check Faults due to instructions executed before exception entry, that are reported asynchronously, are synchronized into `TFSRE0_EL1` and `TFSR_EL1` registers.

<table>
<thead>
<tr>
<th>ITFSB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tag Check Faults are not synchronized on entry to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tag Check Faults are synchronized on entry to EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally `UNKNOWN` value.
Otherwise:

Reserved, RES0.

**BT1, bit [36]**

*When FEAT_BT1 is implemented:*

PAC Branch Type compatibility at EL1.

<table>
<thead>
<tr>
<th>BT1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL1, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL1, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**BT0, bit [35]**

*When FEAT_BT1 is implemented:*

PAC Branch Type compatibility at EL0.

<table>
<thead>
<tr>
<th>BT0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL0, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL0, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

When \texttt{HCR_EL2.E2H} == 1 && \texttt{HCR_EL2.TGE} == 1, the value of the SCTLR_EL1.BT0 has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**Bits [34:32]**

Reserved, RES0.

**EnIA, bit [31]**

*When FEAT_PAuth is implemented:*

Controls enabling of pointer authentication (using the APIAKey_EL1 key) of instruction addresses in the EL1&0 translation regime.

For more information, see ‘System register control of pointer authentication’.

<table>
<thead>
<tr>
<th>EnIA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

**Note**
This field controls the behavior of the AddPACIA and AuthIA pseudocode functions. Specifically, when the field is 1, AddPACIA returns a copy of a pointer to which a pointer authentication code has been added, and AuthIA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**EnIB, bit [30]**

When **FEAT_PAuth** is implemented:

Controls enabling of pointer authentication (using the APIBKey_EL1 key) of instruction addresses in the EL1&0 translation regime.

For more information, see ‘System register control of pointer authentication’.

<table>
<thead>
<tr>
<th><strong>EnIB</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

**Note**

This field controls the behavior of the AddPACIB and AuthIB pseudocode functions. Specifically, when the field is 1, AddPACIB returns a copy of a pointer to which a pointer authentication code has been added, and AuthIB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**LSMAOE, bit [29]**

When **FEAT_LSMAOC** is implemented:

Load Multiple and Store Multiple Atomicity and Ordering Enable.

<table>
<thead>
<tr>
<th><strong>LSMAOE</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For all memory accesses at EL0, A32 and T32 Load Multiple and Store Multiple can have an interrupt taken during the sequence memory accesses, and the memory accesses are not required to be ordered.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ordering and interrupt behavior of A32 and T32 Load Multiple and Store Multiple at EL0 is as defined for Armv8.0.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

When **FEAT_VHE** is implemented, and the value of **HCR_EL2.(E2H, TGE)** is {1,1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES1.

nTLSMD, bit [28]

When FEAT_LSMAOC is implemented:

No Trap Load Multiple and Store Multiple to Device-nGRE/Device-nGnRE/Device-nGnRnE memory.

<table>
<thead>
<tr>
<th>nTLSMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL0 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are trapped and generate a stage 1 Alignment fault.</td>
</tr>
<tr>
<td>0b1</td>
<td>All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL0 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are not trapped.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of HCR_EL2.\{E2H, TGE\} is \{1,1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

EnDA, bit [27]

When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APDAKey_EL1 key) of instruction addresses in the EL1&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnDA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

Note

This field controls the behavior of the AddPACDA and AuthDA pseudocode functions. Specifically, when the field is 1, AddPACDA returns a copy of a pointer to which a pointer authentication code has been added, and AuthDA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
UCI, bit [26]

Traps EL0 execution of cache maintenance instructions, to EL1, or to EL2 when it is implemented and enabled for the current Security state and \( HCR\_EL2 \). TGE is 1, from AArch64 state only, reported using an ESR_ELx.EC value of 0x18.

This applies to\( DC\_CVAU\), \( DC\_CIVAC\), \( DC\_CVAC\), \( DC\_CVAP\), and \( IC\_IVAU\).

If FEAT_DPB2 is implemented, this trap also applies to \( DC\_CVADP\).

If FEAT_MTE2 is implemented, this trap also applies to \( DC\_CIGVAC\), \( DC\_CIGDVAC\), \( DC\_CGVAC\), \( DC\_CGDVAC\), \( DC\_CGVAP\), and \( DC\_CGDVAP\).

If FEAT_DPB2 and FEAT_MTE2 are implemented, this trap also applies to \( DC\_CVADP\) and \( DC\_CGDVADP\).

<table>
<thead>
<tr>
<th>UCI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of the specified instructions at EL0 using AArch64 is trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of \( HCR\_EL2\).\( \{E2H, TGE\} \) is \( \{1, 1\} \), this bit has no effect on execution at EL0.

If the Point of Coherency is before any level of data cache, it is \( \text{IMPLEMENTATION DEFINED} \) whether the execution of any data or unified cache clean, or clean and invalidate instruction that operates by VA to the point of coherency can be trapped when the value of this control is 1.

If the Point of Unification is before any level of data cache, it is \( \text{IMPLEMENTATION DEFINED} \) whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is \( \text{IMPLEMENTATION DEFINED} \) whether the execution of any instruction cache invalidate by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \( \text{UNKNOWN} \) value.

EE, bit [25]

Endianness of data accesses at EL1, and stage 1 translation table walks in the EL1&0 translation regime.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL1, and stage 1 translation table walks in the EL1&amp;0 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL1, and stage 1 translation table walks in the EL1&amp;0 translation regime are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation does not provide Big-endian support at Exception Levels higher than EL0, this bit is \( \text{RES0} \).

If an implementation does not provide Little-endian support at Exception Levels higher than EL0, this bit is \( \text{RES1} \).

The EE bit is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of \( HCR\_EL2\).\( \{E2H, TGE\} \) is \( \{1, 1\} \), this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an \( \text{IMPLEMENTATION DEFINED} \) value.

E0E, bit [24]

Endianness of data accesses at EL0.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>E0E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL0 are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL0 are big-endian.</td>
</tr>
</tbody>
</table>
If an implementation only supports Little-endian accesses at EL0 then this bit is RES0. This option is not permitted when SCTLR_EL1.EE is RES1.

If an implementation only supports Big-endian accesses at EL0 then this bit is RES1. This option is not permitted when SCTLR_EL1.EE is RES0.

This bit has no effect on the endianness of LDTR, LDTRH, LDTRSH, LDTRSW, STTR, and STTRH instructions executed at EL1.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

**SPAN, bit [23]**

When FEAT_PAN is implemented:

Set Privileged Access Never, on taking an exception to EL1.

<table>
<thead>
<tr>
<th>SPAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.PAN is set to 1 on taking an exception to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The value of PSTATE.PAN is left unchanged on taking an exception to EL1.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

**EIS, bit [22]**

When FEAT_ExS is implemented:

Exception Entry is Context Synchronizing. The defined values are:

<table>
<thead>
<tr>
<th>EIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The taking of an exception to EL1 is not a context synchronizing event.</td>
</tr>
<tr>
<td>0b1</td>
<td>The taking of an exception to EL1 is a context synchronizing event.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1,1}, this bit has no effect on execution at EL0.

If SCTLR_EL1.EIS is set to 0b0:

- Indirect writes to ESR_EL1, FAR_EL1, SPSR_EL1, ELR_EL1 are synchronized on exception entry to EL1, so that a direct read of the register after exception entry sees the indirectly written value caused by the exception entry.
- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL1.EIS:

- Changes to the PSTATE information on entry to EL1.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.
**Otherwise:**

Reserved, RES1.

### IESB, bit [21]

**When FEAT_IESB is implemented:**

Implicit Error Synchronization event enable. Possible values are:

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
</tbody>
</table>
| 0b1  | An implicit error synchronization event is added:  
|      | • At each exception taken to EL1.  
|      | • Before the operational pseudocode of each ERET instruction  
|      |   executed at EL1. |

When the PE is in Debug state, the effect of this field is **CONSTRAINED UNPREDICTABLE**, and its Effective value might be 0 or 1 regardless of the value of the field. If the Effective value of the field is 1, then an implicit error synchronization event is added after each DCPSX instruction taken to EL1 and before each DRPS instruction executed at EL1, in addition to the other cases where it is added.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

### TSCXT, bit [20]

**When FEAT_CSV2 is implemented:**

Trap EL0 Access to the $\text{SCXTNUM_{EL0}}$ register, when EL0 is using AArch64. The defined values are:

<table>
<thead>
<tr>
<th>TSCXT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 access to $\text{SCXTNUM_{EL0}}$ is not disabled by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 access to $\text{SCXTNUM_{EL0}}$ is disabled, causing an exception to EL1, or to EL2 when it is implemented and enabled for the current Security state and $\text{HCR_{EL2}.TGE}$ is 1. The value of $\text{SCXTNUM_{EL0}}$ is treated as 0.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of $\text{HCR_{EL2}.{E2H, TGE}}$ is \{1,1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES1.

### WXN, bit [19]

Write permission implies XN (Execute-never). For the EL1&0 translation regime, this bit can force all memory regions that are writable to be treated as XN. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable in the EL1&amp;0 translation regime is forced to XN for accesses from software executing at EL1 or EL0.</td>
</tr>
</tbody>
</table>

This bit applies only when SCTLR_EL1.M bit is set.
The WXN bit is permitted to be cached in a TLB.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

### nTWE, bit [18]

Traps EL0 execution of WFE instructions to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, from both Execution states, reported using an ESR_ELx.EC value of 0x01.

When FEAT_WFxT is implemented, this trap also applies to the WFET instruction.

<table>
<thead>
<tr>
<th>nTWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute a WFE instruction at EL0 is trapped, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

**Bit [17]**

Reserved, RES0.

### nTWI, bit [16]

Traps EL0 execution of WFI instructions to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, from both Execution states, reported using an ESR_ELx.EC value of 0x01.

When FEAT_WFxT is implemented, this trap also applies to the WFIT instruction.

<table>
<thead>
<tr>
<th>nTWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute a WFI instruction at EL0 is trapped, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on execution at EL0.
On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

**UCT, bit [15]**

Traps EL0 accesses to the \texttt{CTR\_EL0} to EL1, or to EL2 when it is implemented and enabled for the current Security state and \texttt{HCR\_EL2}.TGE is 1, from AArch64 state only, reported using an ESR\_ELx.EC value of 0x18.

<table>
<thead>
<tr>
<th>UCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to the \texttt{CTR_EL0} from EL0 using AArch64 are trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT\_VHE is implemented, and the value of \texttt{HCR\_EL2}.E2H, TGE is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

**DZE, bit [14]**

Traps EL0 execution of \texttt{DC ZVA} instructions to EL1, or to EL2 when it is implemented and enabled for the current Security state and \texttt{HCR\_EL2}.TGE is 1, from AArch64 state only, reported using an ESR\_ELx.EC value of 0x18.

If FEAT\_MTE2 is implemented, this trap also applies to \texttt{DC GVA} and \texttt{DC GZVA}.

<table>
<thead>
<tr>
<th>DZE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute an instruction that this trap applies to at EL0 using AArch64 is trapped. Reading \texttt{DCZID_EL0}.DZP from EL0 returns 1, indicating that the instructions this trap applies to are not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT\_VHE is implemented, and the value of \texttt{HCR\_EL2}.E2H, TGE is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

**EnDB, bit [13]**

When FEAT\_PAuth is implemented:

Controls enabling of pointer authentication (using the APDBKey\_EL1 key) of instruction addresses in the EL1&0 translation regime.

For more information, see ‘System register control of pointer authentication’.

<table>
<thead>
<tr>
<th>EnDB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

**Note**

This field controls the behavior of the AddPACDB and AuthDB pseudocode functions. Specifically, when the field is 1, AddPACDB returns a copy of a pointer to which a pointer authentication code has been added, and AuthDB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

**Otherwise:**

Reserved, RES0.
I, bit [12]

Stage 1 instruction access Cacheability control, for accesses at EL0 and EL1:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction access to Stage 1 Normal memory from EL0 and EL1 are Stage 1 Non-cacheable. If the value of SCTLR_EL1.M is 0, instruction accesses from stage 1 of the EL1&amp;0 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Stage 1 Cacheability of instruction access to Stage 1 Normal memory from EL0 and EL1. If the value of SCTLR_EL1.M is 0, instruction accesses from stage 1 of the EL1&amp;0 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

When the value of the HCR_EL2 DC bit is 1, then instruction access to Normal memory from EL0 and EL1 are Cacheable regardless of the value of the SCTLR_EL1.1 bit.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to 0.

EOS, bit [11]

When FEAT_ExS is implemented:

Exception Exit is Context Synchronizing. The defined values are:

<table>
<thead>
<tr>
<th>EOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An exception return from EL1 is not a context synchronizing event</td>
</tr>
<tr>
<td>0b1</td>
<td>An exception return from EL1 is a context synchronizing event</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1,1\}, this bit has no effect on execution at EL0.

If SCTLR_EL1.EOS is set to 0b0:

- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL1.EOS:

- The indirect write of the PSTATE and PC values from SPSR_EL1 and ELR_EL1 on exception return is synchronized.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

EnRCTX, bit [10]

When FEAT_SPECRES is implemented:

Enable EL0 Access to the following instructions:

- AArch32 CFPRCTX, DVPRCTX and CPPRCTX instructions.
- AArch64 CFP RCTX, DVP RCT and CPP RCTX instructions.
The defined values are:

<table>
<thead>
<tr>
<th>EnRCTX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 access to these instructions is disabled, and these instructions are trapped to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 access to these instructions is enabled.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is \{1,1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

UMA, bit [9]

User Mask Access. Traps EL0 execution of MSR and MRS instructions that access the PSTATE.(D, A, I, F) masks to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, from AArch64 state only, reported using an ESR_ELx.EC value of 0x18.

<table>
<thead>
<tr>
<th>UMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt at EL0 using AArch64 to execute an MRS, MSR(REGISTER), or MSR(IMMEDIATE) instruction that accesses the DAIF is trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

SED, bit [8]

When EL0 is capable of using AArch32:

SETEND instruction disable. Disables SETEND instructions at EL0 using AArch32.

<table>
<thead>
<tr>
<th>SED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SETEND instruction execution is enabled at EL0 using AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>SETEND instructions are UNDEFINED at EL0 using AArch32 and any attempt at EL0 to access a SETEND instruction generates an exception to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1, reported using an ESR_ELx.EC value of 0x00.</td>
</tr>
</tbody>
</table>

If the implementation does not support mixed-endian operation at any Exception level, this bit is RES1.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

ITD, bit [7]

When EL0 is capable of using AArch32:

IT Disable. Disables some uses of IT instructions at EL0 using AArch32.
<table>
<thead>
<tr>
<th>ITD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All IT instruction functionality is enabled at EL0 using AArch32.</td>
</tr>
</tbody>
</table>
| 0b1   | Any attempt at EL0 using AArch32 to execute any of the following is UNDEFINED and generates an exception, reported using an ESR_ELx.EC value of 0x00, to EL1 or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1:  
  - All encodings of the IT instruction with hw1[3:0]!=1000.  
  - All encodings of the subsequent instruction with the following values for hw1:  
    - 0b11xxxxxxxxxxxx: All 32-bit instructions, and the 16-bit instructions B, UDF, SVC, LDM, and STM.  
    - 0b1011xxxxxxxxxxxx: All instructions in 'Miscellaneous 16-bit instructions' in the Arm® Architecture Reference Manual, Armv8, for Armv8-A architecture profile, section F3.2.5.  
    - 0b10100xxxxxxxxxxx: ADD Rd, PC, #imm  
    - 0b01001xxxxxxxxxxx: LDR Rd, [PC, #imm]  
    - 0b10101xxxxx1111xxx: ADD Rdn, PC; CMP Rn, PC; MOV Rd, PC; BX PC; BLX PC.  
    - 0b010001xx1xxxx1111: ADD PC, Rm; CMP PC, Rm; MOV PC, Rm. This pattern also covers unpredictable cases with BLX Rn.  
These instructions are always UNDEFINED, regardless of whether they would pass or fail the condition code check that applies to them as a result of being in an IT block.  
It is IMPLEMENTATION DEFINED whether the IT instruction is treated as:  
  - A 16-bit instruction, that can only be followed by another 16-bit instruction.  
  - The first half of a 32-bit instruction.  
This means that, for the situations that are UNDEFINED, either the second 16-bit instruction or the 32-bit instruction is UNDEFINED.  
An implementation might vary dynamically as to whether IT is treated as a 16-bit instruction or the first half of a 32-bit instruction.  

If an instruction in an active IT block that would be disabled by this field sets this field to 1 then behavior is CONSTRAINED UNPREDICTABLE. For more information see 'Changes to an ITD control by an instruction in an IT block'.  
ITD is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAZ/WI.  

When FEAT_VHE is implemented, and the value of HCR_EL2. {E2H, TGE} is \{1, 1\}, this bit has no effect on execution at EL0.  
On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.  

Otherwise:  

Reserved, RES1.  

nAA, bit [6]  

When FEAT_LSE2 is implemented:  
Non-aligned access. This bit controls generation of Alignment faults at EL1 and EL0 under certain conditions.
nAA | Meaning
---|---
0b0 | LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSH, LDAPURSW, LDAR, LDARH, LDLAR, LDLARH, STLLR, STLLRH, STLR, STLRH, STLUR, and STLURH generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes for accesses.
0b1 | This control bit does not cause LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSH, LDAPURSW, LDAR, LDARH, LDLAR, LDLARH, STLLR, STLLRH, STLR, STLRH, STLUR, or STLURH to generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**CP15BEN, bit [5]**

**When EL0 is capable of using AArch32:**

System instruction memory barrier enable. Enables accesses to the DMB, DSB, and ISB System instructions in the (coproc==0b1111) encoding space from EL0:

<table>
<thead>
<tr>
<th>CP15BEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 using AArch32: EL0 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is UNDEFINED and generates an exception to EL1, or to EL2 when it is implemented and enabled for the current Security state and HCR_EL2.TGE is 1. The exception is reported using an ESR_ELx.EC value of 0x80.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 using AArch32: EL0 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is enabled.</td>
</tr>
</tbody>
</table>

CP15BEN is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAO/WI.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**SA0, bit [4]**

SP Alignment check enable for EL0. When set to 1, if a load or store instruction executed at EL0 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally UNKNOWN value.
SA, bit [3]

SP Alignment check enable. When set to 1, if a load or store instruction executed at EL1 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

C, bit [2]

Stage 1 Cacheability control, for data accesses.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All data access to Stage 1 Normal memory from EL0 and EL1, and all Normal memory accesses from unified cache to the EL1&amp;0 Stage 1 translation tables, are treated as Stage 1 Non-cacheable.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Stage 1 Cacheability of:</td>
</tr>
<tr>
<td></td>
<td>• Data access to Normal memory from EL0 and EL1.</td>
</tr>
<tr>
<td></td>
<td>• Normal memory accesses to the EL1&amp;0 Stage 1 translation tables.</td>
</tr>
</tbody>
</table>

When the value of the HCR_EL2.DC bit is 1, the PE ignores SCTLR.C. This means that Non-secure EL0 and Non-secure EL1 data accesses to Normal memory are Cacheable.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to 0.

A, bit [1]

Alignment check enable. This is the enable bit for Alignment fault checking at EL1 and EL0.

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Alignment fault checking disabled when executing at EL1 or EL0.</td>
</tr>
<tr>
<td></td>
<td>Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element(s) being accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alignment fault checking enabled when executing at EL1 or EL0.</td>
</tr>
<tr>
<td></td>
<td>All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception.</td>
</tr>
</tbody>
</table>

Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.

When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \{1, 1\}, this bit has no effect on execution at EL0.

On a Warm reset, in a system where the PE resets into EL1, this field resets to an architecturally \textit{UNKNOWN} value.

M, bit [0]

MMU enable for EL1&0 stage 1 address translation.

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1&amp;0 stage 1 address translation disabled.</td>
</tr>
<tr>
<td></td>
<td>See the SCTLR_EL1.I field for the behavior of instruction accesses to Normal memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1&amp;0 stage 1 address translation enabled.</td>
</tr>
</tbody>
</table>

If the value of HCR_EL2.(DC, TGE) is not \{0, 0\} then in Non-secure state the PE behaves as if the value of the SCTLR_EL1.M field is 0 for all purposes other than returning the value of a direct read of the field.
When FEAT_VHE is implemented, and the value of HCR_EL2.(E2H, TGE) is \(1, 1\), this bit has no effect on the PE.

On a Warm reset, in a system where the PE resets into EL1, this field resets to 0.

**Accessing the SCTLR_EL1**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic SCTLR_EL1 or SCTLR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
\hline
0b11 & 0b000 & 0b0001 & 0b0000 & 0b000 \\
\hline
\end{array}
\]

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCTLR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return SCTLR_EL1;
  end if
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return SCTLR_EL2;
  else
    return SCTLR_EL1;
  end if
elsif PSTATE.EL == EL3 then
  return SCTLR_EL1;
end if
```

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCTLR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return SCTLR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    SCTLR_EL2 = X[t];
  else
    SCTLR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  SCTLR_EL1 = X[t];
```

SCTLR_EL1, System Control Register (EL1)
MRS <Xt>, SCTLR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x110];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return SCTLR_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return SCTLR_EL1;
  else
    UNDEFINED;

MSR SCTLR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x110] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    SCTLR_EL1 = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    SCTLR_EL1 = X[t];
  else
    UNDEFINED;
SCTLR_EL2, System Control Register (EL2)

The SCTLR_EL2 characteristics are:

**Purpose**

Provides top level control of the system, including its memory system, at EL2.

When FEAT_VHE is implemented, and the value of HCR_EL2.{E2H, TGE} is \{1, 1\}, these controls apply also to execution at EL0.

**Configuration**

AArch64 System register SCTLR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HSCTLR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

SCTLR_EL2 is a 64-bit register.

**Field descriptions**

The SCTLR_EL2 bit assignments are:

**When HCR_EL2.E2H != 1 or HCR_EL2.TGE != 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>62</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>61</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>58</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>57</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>55</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>54</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>53</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>51</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>50</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>49</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>47</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>46</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>45</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>43</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>42</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>41</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>39</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>38</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>37</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>35</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>34</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>33</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31</td>
<td>Bits [63:45]</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>29</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>28</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>27</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>24</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>23</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>21</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>20</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>19</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>17</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>16</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>15</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>13</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>12</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>11</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>9</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>8</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>7</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>5</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>4</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td>3</td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>0</td>
<td>When FEAT_SSBS is implemented:</td>
</tr>
<tr>
<td></td>
<td>Default PSTATE.SSBS value on Exception Entry.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an IMPLEMENTATIONDEFINED value.

**Otherwise:**

Reserved, RES0.
ATA, bit [43]

When FEAT_MTE2 is implemented:

Allocation Tag Access in EL2. When SCR_EL3.ATA is 1, controls EL2 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.

<table>
<thead>
<tr>
<th>ATA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [42]

Reserved, RES0.

TCF, bits [41:40]

When FEAT_MTE2 is implemented:

Tag Check Fault. Controls the effect of Tag Check Faults due to Loads and Stores in EL2.

If FEAT_MTE3 is not implemented, the value 0b11 is reserved.

<table>
<thead>
<tr>
<th>TCF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tag Check Faults have no effect on the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tag Check Faults cause a synchronous exception.</td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are</td>
</tr>
<tr>
<td></td>
<td>asynchronously accumulated on writes.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [39:38]

Reserved, RES0.
ITFSB, bit [37]

When FEAT_MTE2 is implemented:

When synchronous exceptions are not being generated by Tag Check Faults, this field controls whether on exception entry into EL2, all Tag Check Faults due to instructions executed before exception entry, that are reported asynchronously, are synchronized into TFSRE0_EL1, TFSR_EL1 and TFSB_EL2 registers.

<table>
<thead>
<tr>
<th>ITFSB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tag Check Faults are not synchronized on entry to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tag Check Faults are synchronized on entry to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

BT, bit [36]

When FEAT_BT1 is implemented:

PAC Branch Type compatibility at EL2.

<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL2, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL2, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [35:32]

Reserved, RES0.

EnIA, bit [31]

When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APIAKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see ‘System register control of pointer authentication’.

<table>
<thead>
<tr>
<th>EnIA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

Note

This field controls the behavior of the AddPACIA and AuthIA pseudocode functions. Specifically, when the field is 1, AddPACIA returns a copy of a pointer to which a pointer authentication code has been added, and AuthIA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.
On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**EnIB, bit [30]**

**When FEAT_PAuth is implemented:**

Controls enabling of pointer authentication (using the APIBKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

**Note**

This field controls the behavior of the AddPACIB and AuthIB pseudocode functions. Specifically, when the field is 1, AddPACIB returns a copy of a pointer to which a pointer authentication code has been added, and AuthIB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bits [29:28]**

Reserved, RES1.

**EnDA, bit [27]**

**When FEAT_PAuth is implemented:**

Controls enabling of pointer authentication (using the APDAKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnDA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

**Note**

This field controls the behavior of the AddPACDA and AuthDA pseudocode functions. Specifically, when the field is 1, AddPACDA returns a copy of a pointer to which a pointer authentication code has been added, and AuthDA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

Bit [26]

Reserved, RES0.

EE, bit [25]

Endianness of data accesses at EL2, stage 1 translation table walks in the EL2 or EL2&0 translation regime, and stage 2 translation table walks in the EL1&0 translation regime.

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL2, stage 1 translation table walks in the</td>
</tr>
<tr>
<td></td>
<td>EL2 or EL2&amp;0 translation regime, and stage 2 translation table walks</td>
</tr>
<tr>
<td></td>
<td>in the EL1&amp;0 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL2, stage 1 translation table walks in the</td>
</tr>
<tr>
<td></td>
<td>EL2 or EL2&amp;0 translation regime, and stage 2 translation table walks</td>
</tr>
<tr>
<td></td>
<td>in the EL1&amp;0 translation regime are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation does not provide Big-endian support at Exception Levels higher than EL0, this bit is RES0.

If an implementation does not provide Little-endian support at Exception Levels higher than EL0, this bit is RES1.

The EE bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an IMPLEMENTATION DEFINED value.

Bit [24]

Reserved, RES0.

Bit [23]

Reserved, RES1.

EIS, bit [22]

When FEAT_ExS is implemented:

Exception entry is a context synchronization event.

<table>
<thead>
<tr>
<th>EIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The taking of an exception to EL2 is not a context synchronization</td>
</tr>
<tr>
<td></td>
<td>event.</td>
</tr>
<tr>
<td>0b1</td>
<td>The taking of an exception to EL2 is a context synchronization event.</td>
</tr>
</tbody>
</table>

If SCTLR_EL2.EIS is set to 0b0:

- Indirect writes to ESR_EL2, FAR_EL2, SPSR_EL2, ELR_EL2, and HPFAR_EL2 are synchronized on exception entry to EL2, so that a direct read of the register after exception entry sees the indirectly written value caused by the exception entry.
- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL2.EIS:

- Changes to the PSTATE information on entry to EL2.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores, and data processing instructions.
- Exit from Debug state.
On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally *UNKNOWN* value.

**Otherwise:**

Reserved, RES1.

### IESB, bit [21]

**When FEAT_IESB is implemented:**

Implicit Error Synchronization event enable.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
</tbody>
</table>
| 0b1  | An implicit error synchronization event is added:  
|      | • At each exception taken to EL2.  
|      | • Before the operational pseudocode of each ERET instruction executed at EL2. |

When the PE is in Debug state, the effect of this field is *CONSTRAINED UNPREDICTABLE*, and its Effective value might be 0 or 1 regardless of the value of the field. If the Effective value of the field is 1, then an implicit error synchronization event is added after each DCPSX instruction taken to EL2 and before each DRPS instruction executed at EL2, in addition to the other cases where it is added.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally *UNKNOWN* value.

**Otherwise:**

Reserved, RES0.

### Bit [20]

Reserved, RES0.

### WXN, bit [19]

Write permission implies XN (Execute-never). For the EL2 or EL2&0 translation regime, this bit can force all memory regions that are writable to be treated as XN.

<table>
<thead>
<tr>
<th>WXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable in the EL2 or EL2&amp;0 translation regime is forced to XN for accesses from software executing at EL2.</td>
</tr>
</tbody>
</table>

This bit applies only when SCTLR_EL2.M bit is set.

The WXN bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally *UNKNOWN* value.

### Bit [18]

Reserved, RES1.

### Bit [17]

Reserved, RES0.
Bit [16]
Reserved, RES1.

Bits [15:14]
Reserved, RES0.

EnDB, bit [13]
When FEAT_PAuth is implemented:
Controls enabling of pointer authentication (using the APDBKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnDB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

Note
This field controls the behavior of the AddPACDB and AuthDB pseudocode functions. Specifically, when the field is 1, AddPACDB returns a copy of a pointer to which a pointer authentication code has been added, and AuthDB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

I, bit [12]
Instruction access Cacheability control, for accesses at EL2:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction accesses to Normal memory from EL2 are Non-cacheable for all levels of instruction and unified cache. If the value of SCTLR_EL2.M is 0, instruction accesses from stage 1 of the EL2 or EL2&amp;0 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Cacheability of instruction access to Normal memory from EL2. If the value of SCTLR_EL2.M is 0, instruction accesses from stage 1 of the EL2 or EL2&amp;0 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL1&0 or EL3 translation regimes.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

EOS, bit [11]
When FEAT_ExS is implemented:
Exception exit is a context synchronization event.
Meaning

0b0  An exception return from EL2 is not a context synchronization event.

0b1  An exception return from EL2 is a context synchronization event.

If SCTLR_EL2.EOS is set to 0b0:

- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL2.EOS:

- The indirect write of the PSTATE and PC values from SPSR_EL2 and ELR_EL2 on exception return is synchronized.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores, and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

Bits [10:7]

Reserved, RES0.

nAA, bit [6]

When FEAT_LSE2 is implemented:

Non-aligned access. This bit controls generation of Alignment faults at EL2 under certain conditions.

<table>
<thead>
<tr>
<th>nAA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSW, LDAR, LDARH, LDLAR, LDLARH, STLLL, STLURH, STLUR, and STLURH generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes for accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control bit does not cause LDAPR, LDAPRH, LDAPUR, LDAPURSW, LDLAR, LDLARH, STLLL, STLURH, STLUR, STLUR, or STLURH to generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [5:4]

Reserved, RES1.

SA, bit [3]

SP Alignment check enable. When set to 1, if a load or store instruction executed at EL2 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.
On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

### C, bit [2]
Cacheability control, for data accesses.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All data accesses to Normal memory from EL2, and all Normal memory accesses to the EL2 translation tables, are Non-cacheable for all levels of data and unified cache.</td>
</tr>
</tbody>
</table>
| 0b1 | This control has no effect on the Cacheability of:  
  - Data access to Normal memory from EL2.  
  - Normal memory accesses to the EL2 translation tables. This bit has no effect on the EL1&0 or EL3 translation regimes. |

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

### A, bit [1]
Alignment check enable. This is the enable bit for Alignment fault checking at EL2:

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Alignment fault checking disabled when executing at EL2. Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element(s) being accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alignment fault checking enabled when executing at EL2. All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception. Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

### M, bit [0]
MMU enable for EL2 stage 1 address translation.

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 stage 1 address translation disabled. See the SCTLR_EL2.I field for the behavior of instruction accesses to Normal memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 stage 1 address translation enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

#### When HCR_EL2.E2H == 1 and HCR_EL2.TGE == 1:

This format applies only from Armv8.1 when EL2 is enabled in the current Security state and **HCR_EL2. {E2H, TGE}** == {1, 1}.

### Bits [63:58]
Reserved, RES0.
EPAN, bit [57]

When FEAT_PAN3 is implemented:

Enhanced Privileged Access Never. When PSTATE.PAN is 1, determines whether an EL2 data access to a page with EL0 instruction access permission generates a Permission fault as a result of the Privileged Access Never mechanism.

<table>
<thead>
<tr>
<th>EPAN</th>
<th>Meaning</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No additional Permission faults are generated by this mechanism.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>An EL1 data access to a page with stage 1 EL0 data access permission or stage 1 EL0 instruction access permission generates a Permission fault. Any speculative data accesses that would generate a Permission fault if the accesses were not speculative will not cause an allocation into a cache.</td>
<td></td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EnALS, bit [56]

When FEAT_LS64 is implemented:

Traps execution of an LD64B or ST64B instruction at EL0 to EL2.

<table>
<thead>
<tr>
<th>EnALS</th>
<th>Meaning</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an LD64B or ST64B instruction at EL0 is trapped to EL2.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
<td></td>
</tr>
</tbody>
</table>

A trap of an LD64B or ST64B instruction is reported using an ESR_ELx.EC value of 0x0A, with an ISS code of 0x00000002.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EnAS0, bit [55]

When FEAT_LS64 is implemented:

Traps execution of an ST64BV0 instruction at EL0 to EL2.

<table>
<thead>
<tr>
<th>EnAS0</th>
<th>Meaning</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV0 instruction at EL0 is trapped to EL2.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
<td></td>
</tr>
</tbody>
</table>

A trap of an ST64BV0 instruction is reported using an ESR_ELx.EC value of 0x0A, with an ISS code of 0x00000001.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
EnASR, bit [54]

When FEAT_LS64 is implemented:

Traps execution of an ST64BV instruction at EL0 to EL2.

<table>
<thead>
<tr>
<th>EnASR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Execution of an ST64BV instruction at EL0 is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

A trap of an ST64BV instruction is reported using an ESR_ELx.EC value of 0x0A, with an ISS code of 0x0000000.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [53:50]

Reserved, RES0.

TWEDEL, bits [49:46]

When FEAT_TWED is implemented:

TWE Delay. A 4-bit unsigned number that, when SCTLR_EL2.TWEDEn is 1, encodes the minimum delay in taking a trap of WFE caused by SCTLR_EL2.nTWE as $2^{(TWEDEL + 8)}$ cycles.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TWEDEn, bit [45]

When FEAT_TWED is implemented:

TWE Delay Enable. Enables a configurable delayed trap of the WFE instruction caused by SCTLR_EL2.nTWE.

<table>
<thead>
<tr>
<th>TWEDEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The delay for taking a WFE trap is IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The delay for taking a WFE trap is at least the number of cycles defined in SCTLR_EL2.TWEDEL.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

DSSBS, bit [44]

When FEAT_SSSBS is implemented:

Default PSTATE.SSBS value on Exception Entry.

<table>
<thead>
<tr>
<th>DSSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.SSBS is set to 0 on an exception to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>PSTATE.SSBS is set to 1 on an exception to EL2.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL2, this field resets to an IMPLEMENTATION DEFINED value.

Otherwise:

Reserved, RES0.

ATA, bit [43]

When FEAT_MTE2 is implemented:

Allocation Tag Access in EL2. When SCR_EL3.ATA is 1, controls EL2 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.

<table>
<thead>
<tr>
<th>ATA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

ATA0, bit [42]

When FEAT_MTE2 is implemented:

Allocation Tag Access in EL0. When SCR_EL3.ATA is 1, controls EL0 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
- Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.
- Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.

<table>
<thead>
<tr>
<th>ATA0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

Note

Software may change this control bit on a context switch.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**TCF, bits [41:40]**

*When FEAT_MTE2 is implemented:*

Tag Check Fault in EL2. Controls the effect of Tag Check Faults due to Loads and Stores in EL2.

If FEAT_MTE3 is not implemented, the value 0b11 is reserved.

<table>
<thead>
<tr>
<th>TCF</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Tag Check Faults have no effect on the PE.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Tag Check Faults cause a synchronous exception.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are asynchronously accumulated on writes.</td>
<td>When FEAT_MTE3 is implemented</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TCF0, bits [39:38]**

*When FEAT_MTE2 is implemented:*

Tag Check Fault in EL0. Controls the effect of Tag Check Faults due to Loads and Stores in EL0.

If FEAT_MTE3 is not implemented, the value 0b11 is reserved.

<table>
<thead>
<tr>
<th>TCF0</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Tag Check Faults have no effect on the PE.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Tag Check Faults cause a synchronous exception.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are asynchronously accumulated on writes.</td>
<td>When FEAT_MTE3 is implemented</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Note

Software may change this control bit on a context switch.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.
ITFSB, bit [37]

When FEAT_MTE2 is implemented:

When synchronous exceptions are not being generated by Tag Check Faults, this field controls whether on exception entry into EL2, all Tag Check Faults due to instructions executed before exception entry, that are reported asynchronously, are synchronized into TFSRE0_EL1, TFSR_EL1 and TFSB_EL2 registers.

<table>
<thead>
<tr>
<th>ITFSB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tag Check Faults are not synchronized on entry to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tag Check Faults are synchronized on entry to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

BT1, bit [36]

When FEAT_BTI is implemented:

PAC Branch Type compatibility at EL2.

<table>
<thead>
<tr>
<th>BT1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL2, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL2, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

BT0, bit [35]

When FEAT_BTI is implemented:

PAC Branch Type compatibility at EL0.

<table>
<thead>
<tr>
<th>BT0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL0, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL0, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bits [34:32]

Reserved, RES0.
EnIA, bit [31]
When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APIAKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnIA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

Note

This field controls the behavior of the AddPACIA and AuthIA pseudocode functions. Specifically, when the field is 1, AddPACIA returns a copy of a pointer to which a pointer authentication code has been added, and AuthIA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

EnIB, bit [30]
When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APIBKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

<table>
<thead>
<tr>
<th>EnIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

Note

This field controls the behavior of the AddPACIB and AuthIB pseudocode functions. Specifically, when the field is 1, AddPACIB returns a copy of a pointer to which a pointer authentication code has been added, and AuthIB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

LSMAOE, bit [29]
When FEAT_LSMAOC is implemented:

Load Multiple and Store Multiple Atomicity and Ordering Enable.
The ordering and interrupt behavior of A32 and T32 Load Multiple and Store Multiple at EL0 is as defined for Armv8.0.

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**nTLSMD, bit [28]**

*When FEAT_LSMAOC is implemented:*

All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL0 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are trapped and generate a stage 1 Alignment fault.

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**EnDA, bit [27]**

*When FEAT_PAuth is implemented:*

Controls enabling of pointer authentication (using the APDAKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see 'System register control of pointer authentication'.

This field controls the behavior of the AddPACDA and AuthDA pseudocode functions. Specifically, when the field is 1, AddPACDA returns a copy of a pointer to which a pointer authentication code has been added, and AuthDA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**UCI, bit [26]**

Traps execution of cache maintenance instructions at EL0 to EL2, from AArch64 state only. This applies to DC_CVAU, DC_CIVAC, DC_CVAC, DC_CVAP, and IC_IVAU.

If FEAT_DPB2 is implemented, this trap also applies to DC_CVADP.

If FEAT_MTE2 is implemented, this trap also applies to DC_CIGVAC, DC_CIGDVAC, DC_CGVAC, DC_CGDVAC, DC_CGVP, and DC_CGDVAP.

If FEAT_DPB2 and FEAT_MTE2 are implemented, this trap also applies to DC_CGVADP and DC_CGDVADP.

<table>
<thead>
<tr>
<th>UCI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute an instruction that this trap applies to at EL0 using AArch64 is trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If the Point of Coherency is before any level of data cache, it is IMPLEMENTATION DEFINED whether the execution of any data or unified cache clean, or clean and invalidate instruction that operates by VA to the point of coherency can be trapped when the value of this control is 1.

If the Point of Unification is before any level of data cache, it is IMPLEMENTATION DEFINED whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is IMPLEMENTATION DEFINED whether the execution of any instruction cache invalidate by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**EE, bit [25]**

Endianness of data accesses at EL2, stage 1 translation table walks in the EL2 or EL2&0 translation regime, and stage 2 translation table walks in the EL2&0 translation regime.

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL2, stage 1 translation table walks in the EL2 or EL2&amp;0 translation regime, and stage 2 translation table walks in the EL2&amp;0 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL2, stage 1 translation table walks in the EL2 or EL2&amp;0 translation regime, and stage 2 translation table walks in the EL2&amp;0 translation regime are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation does not provide Big-endian support at Exception Levels higher than EL0, this bit is RES0.

If an implementation does not provide Little-endian support at Exception Levels higher than EL0, this bit is RES1.

The EE bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an IMPLEMENTATION DEFINED value.

**E0E, bit [24]**

Endianness of data accesses at EL0.

<table>
<thead>
<tr>
<th>E0E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL0 are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL0 are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation only supports Little-endian accesses at EL0 then this bit is RES0. This option is not permitted when SCTLR_EL1.EE is RES1.
If an implementation only supports Big-endian accesses at EL0 then this bit is RES1. This option is not permitted when SCTLR_EL1.EE is RES0.

This bit has no effect on the endianness of LDTR, LDTRH, LDTRSH, LDTRSW, STTR, and STTRH instructions executed at EL1.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**SPAN, bit [23]**

Set Privileged Access Never, on taking an exception to EL2.

<table>
<thead>
<tr>
<th>SPAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.PAN is set to 1 on taking an exception to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>The value of PSTATE.PAN is left unchanged on taking an exception to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**EIS, bit [22]**

When FEAT_ExS is implemented:

Exception entry is a context synchronization event.

<table>
<thead>
<tr>
<th>EIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The taking of an exception to EL2 is not a context synchronization event.</td>
</tr>
<tr>
<td>0b1</td>
<td>The taking of an exception to EL2 is a context synchronization event.</td>
</tr>
</tbody>
</table>

If SCTLR_EL2.EIS is set to 0b0:

- Indirect writes to ESR_EL2, FAR_EL2, SPSR_EL2, ELR_EL2, and HPFAR_EL2 are synchronized on exception entry to EL2, so that a direct read of the register after exception entry sees the indirectly written value caused by the exception entry.
- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL2.EIS:

- Changes to the PSTATE information on entry to EL2.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores, and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.

**IESB, bit [21]**

When FEAT_IESB is implemented:

Implicit Error Synchronization event enable.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>An implicit error synchronization event is added:</td>
</tr>
<tr>
<td></td>
<td>• At each exception taken to EL2.</td>
</tr>
<tr>
<td></td>
<td>• Before the operational pseudocode of each ERET instruction executed at EL2.</td>
</tr>
</tbody>
</table>
When the PE is in Debug state, the effect of this field is **CONSTRAINED UNPREDICTABLE**, and its Effective value might be 0 or 1 regardless of the value of the field. If the Effective value of the field is 1, then an implicit error synchronization event is added after each DCPSX instruction taken to EL2 and before each DRPS instruction executed at EL2, in addition to the other cases where it is added.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**TSCXT, bit [20]**

When FEAT_CSV2 is implemented:

Trap EL0 access to the SCXTNUM_EL0 register, when EL0 is using AArch64.

<table>
<thead>
<tr>
<th>TSCXT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 access to SCXTNUM_EL0 is not disabled by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 access to SCXTNUM_EL0 is disabled, causing an exception to EL2, and the SCXTNUM_EL0 value is treated at 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES1.

**WXN, bit [19]**

Write permission implies XN (Execute-never). For the EL2 or EL2&0 translation regime, this bit can force all memory regions that are writable to be treated as XN.

<table>
<thead>
<tr>
<th>WXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable in the EL2 or EL2&amp;0 translation regime is forced to XN for accesses from software executing at EL2.</td>
</tr>
</tbody>
</table>

This bit applies only when SCTLR_EL2.M bit is set.

The WXN bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally **UNKNOWN** value.

**nTWE, bit [18]**

Traps execution of WFE instructions at EL0 to EL2, from both Execution states.

<table>
<thead>
<tr>
<th>nTWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute a WFE instruction at EL0 is trapped to EL2, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or
WFI is executed when there is no Wakeup event. The only guarantee is that if
the instruction does not complete in finite time in the absence of a Wakeup
event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**Bit [17]**

Reserved, RES0.

**nTWI, bit [16]**

Traps execution of WFI instructions at EL0 to EL2, from both Execution states.

<table>
<thead>
<tr>
<th>nTWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute a WFI instruction at EL0 is trapped EL2, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

In AArch32 state, the attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**UCT, bit [15]**

Traps EL0 accesses to the CTR_EL0 to EL2, from AArch64 state only.

<table>
<thead>
<tr>
<th>UCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to the CTR_EL0 from EL0 using AArch64 are trapped to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**DZE, bit [14]**

Traps execution of DC ZVA instructions at EL0 to EL2, from AArch64 state only.

If FEAT_MTE2 is implemented, this trap also applies to DC GVA and DC GZVA.

<table>
<thead>
<tr>
<th>DZE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Any attempt to execute an instruction that this trap applies to at EL0 using AArch64 is trapped to EL2. Reading DCZID_EL0.DZP from EL0 returns 1, indicating that the instructions that this trap applies to are not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.
When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APDBKey_EL1 key) of instruction addresses in the EL2&0 translation regime.

For more information, see ‘System register control of pointer authentication’.

<table>
<thead>
<tr>
<th>EnDB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

Note

This field controls the behavior of the AddPACDB and AuthDB pseudocode functions. Specifically, when the field is 1, AddPACDB returns a copy of a pointer to which a pointer authentication code has been added, and AuthDB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally \textit{UNKNOWN} value.

Otherwise:

Reserved, RES0.

I, bit [12]

Instruction access Cacheability control, for accesses at EL2 and EL0:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction access to Normal memory from EL2 and EL0 are Non-cacheable for all levels of instruction and unified cache. If the value of \textit{SCTLR EL2.M} is 0, instruction accesses from stage 1 of the EL2&amp;0 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Cacheability of instruction access to Normal memory from EL2 and EL0. If the value of \textit{SCTLR EL2.M} is 0, instruction accesses from stage 1 of the EL2&amp;0 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL3 translation regimes.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

EOS, bit [11]

When FEAT_ExS is implemented:

Exception exit is a context synchronization event.

<table>
<thead>
<tr>
<th>EOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An exception return from EL2 is not a context synchronization event.</td>
</tr>
<tr>
<td>0b1</td>
<td>An exception return from EL2 is a context synchronization event.</td>
</tr>
</tbody>
</table>

If \textit{SCTLR_EL2.EOS} is set to 0b0:

- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
- DCPS* and DRPS instructions are context synchronization events.
The following are not affected by the value of SCTLR_EL2.EOS:

- The indirect write of the PSTATE and PC values from SPSR_EL2 and ELR_EL2 on exception return is synchronized.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores, and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.

**EnRCTX, bit [10]**

*When FEAT_SPECRES is implemented:*

Enable EL0 Access to the following instructions:

- AArch32 CFPRCTX, DVPRCTX and CPPRCTX instructions.
- AArch64 CFP RCTX, DVP RCT and CPP RCTX instructions.

The defined values are:

<table>
<thead>
<tr>
<th>EnRCTX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 access to these instructions is disabled, and these instructions are trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 access to these instructions is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bit [9]**

Reserved, RES0.

**SED, bit [8]**

*When EL0 is capable of using AArch32:*

SETEND instruction disable. Disables SETEND instructions at EL0 using AArch32.

<table>
<thead>
<tr>
<th>SED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SETEND instruction execution is enabled at EL0 using AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>SETEND instructions are UNDEFINED at EL0 using AArch32.</td>
</tr>
</tbody>
</table>

If the implementation does not support mixed-endian operation at any Exception level, this bit is RES1.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.
ITD, bit [7]

When EL0 is capable of using AArch32:

IT Disable. Disables some uses of IT instructions at EL0 using AArch32.

<table>
<thead>
<tr>
<th>ITD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All IT instruction functionality is enabled at EL0 using AArch32. Any attempt at EL0 using AArch32 to execute any of the following is UNDEFINED:</td>
</tr>
<tr>
<td></td>
<td>• All encodings of the IT instruction with hw1[3:0]! = 1000.</td>
</tr>
<tr>
<td></td>
<td>• All encodings of the subsequent instruction with the following values for hw1:</td>
</tr>
<tr>
<td></td>
<td>◦ 0b11xxxxxxxxxxxxxx: All 32-bit instructions, and the 16-bit instructions B, UDF, SVC, LDM, and STM.</td>
</tr>
<tr>
<td></td>
<td>◦ 0b1011xxxxxxxxxxx: All instructions in 'Miscellaneous 16-bit instructions' in the Arm® Architecture Reference Manual, Armv8, for Armv8-A architecture profile, section F3.2.5.</td>
</tr>
<tr>
<td></td>
<td>◦ 0b10000xxxxxxx: ADD Rd, PC, #imm</td>
</tr>
<tr>
<td></td>
<td>◦ 0b10001xxxxxxx: LDR Rd, [PC, #imm]</td>
</tr>
<tr>
<td></td>
<td>◦ 0b10001xxxx1xxx11: ADD Rdn, PC; CMP Rn, PC; MOV Rd, PC; BX PC; BLX PC.</td>
</tr>
<tr>
<td></td>
<td>◦ 0b10001xx1xxxx111: ADD PC, Rm; CMP PC, Rm; MOV PC, Rm. This pattern also covers UNPREDICTABLE cases with BLX Rn.</td>
</tr>
<tr>
<td>0b1</td>
<td>These instructions are always UNDEFINED, regardless of whether they would pass or fail the condition code check that applies to them as a result of being in an IT block. It is IMPLEMENTATION DEFINED whether the IT instruction is treated as:</td>
</tr>
<tr>
<td></td>
<td>• A 16-bit instruction, that can only be followed by another 16-bit instruction.</td>
</tr>
<tr>
<td></td>
<td>• The first half of a 32-bit instruction.</td>
</tr>
<tr>
<td></td>
<td>This means that, for the situations that are UNDEFINED, either the second 16-bit instruction or the 32-bit instruction is UNDEFINED. An implementation might vary dynamically as to whether IT is treated as a 16-bit instruction or the first half of a 32-bit instruction.</td>
</tr>
</tbody>
</table>

If an instruction in an active IT block that would be disabled by this field sets this field to 1 then behavior is CONSTRAINED UNPREDICTABLE. For more information see 'Changes to an ITD control by an instruction in an IT block'.

ITD is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAZ/WI.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

nAA, bit [6]

When FEAT_LSE2 is implemented:

Non-aligned access. This bit controls generation of Alignment faults at EL2 and EL0 under certain conditions.
Meaning

0b0 LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSW, LDAR, LDARH, LDLAR, LDLARH, STLLR, STLLRH, STLAR, STLARH, STLUR, and STLURH generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes for accesses.

0b1 This control bit does not cause LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSW, LDAR, LDARH, LDLAR, LDLARH, STLLR, STLLRH, STLAR, STLARH, STLUR, or STLURH to generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**CP15BEN, bit [5]**

*When EL0 is capable of using AArch32:*

System instruction memory barrier enable. Enables accesses to the DMB, DSB, and ISB System instructions in the (coproc==0b1111) encoding space from EL0:

<table>
<thead>
<tr>
<th>CP15BEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 using AArch32: EL0 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 using AArch32: EL0 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is enabled.</td>
</tr>
</tbody>
</table>

CP15BEN is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAO/WI.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SA0, bit [4]**

SP Alignment check enable for EL0. When set to 1, if a load or store instruction executed at EL0 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**SA, bit [3]**

SP Alignment check enable. When set to 1, if a load or store instruction executed at EL2 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**C, bit [2]**

Cacheability control, for data accesses.
Meaning

0b0 All data access to Normal memory from EL2 and EL0, and all Normal memory accesses to the EL2&0 translation tables, are Non-cacheable for all levels of data and unified cache.

0b1 This control has no effect on the Cacheability of:
- Data access to Normal memory from EL2 and EL0.
- Normal memory accesses to the EL2&0 translation tables.

This bit has no effect on the EL3 translation regimes.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

A, bit [1]

Alignment check enable. This is the enable bit for Alignment fault checking at EL2 and EL0.

Meaning

0b0 Alignment fault checking disabled when executing at EL2 and EL0. Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element(s) being accessed.

0b1 Alignment fault checking enabled when executing at EL2 and EL0. All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception.

Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

M, bit [0]

MMU enable for EL2&0 stage 1 address translation.

Meaning

0b0 EL2&0 stage 1 address translation disabled.
See the SCTLR_EL2.I field for the behavior of instruction accesses to Normal memory.

0b1 EL2&0 stage 1 address translation enabled.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Accessing the SCTLR_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic SCTLR_EL2 or SCTLR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{SCTLR}\_\text{EL2}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b00</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return SCTLR_EL2;
elsif PSTATE.EL == EL3 then
    return SCTLR_EL2;

MSR SCTLR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    SCTLR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    SCTLR_EL2 = X[t];

MRS <Xt>, SCTLR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TRVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.SCTLR_EL1 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
            return NVMem[0x110];
        else
            return SCTLR_EL1;
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            return SCTLR_EL2;
        else
            return SCTLR_EL1;
    elsif PSTATE.EL == EL3 then
        return SCTLR_EL1;

MSR SCTLR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCTRL_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x110] = X[t];
  else
    SCTLR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    SCTLR_EL2 = X[t];
  else
    SCTLR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  SCTLR_EL1 = X[t];
SCTLR_EL3, System Control Register (EL3)

The SCTLR_EL3 characteristics are:

**Purpose**

Provides top level control of the system, including its memory system, at EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to SCTLR_EL3 are **UNDEFINED**.

**Attributes**

SCTLR_EL3 is a 64-bit register.

**Field descriptions**

The SCTLR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>DSSBS, bit [44]</td>
</tr>
<tr>
<td>61</td>
<td>ATA, bit [43]</td>
</tr>
<tr>
<td>60</td>
<td>WXN</td>
</tr>
<tr>
<td>59</td>
<td>Reserved</td>
</tr>
<tr>
<td>58</td>
<td>Reserved</td>
</tr>
<tr>
<td>57</td>
<td>Reserved</td>
</tr>
<tr>
<td>56</td>
<td>Reserved</td>
</tr>
<tr>
<td>55</td>
<td>Reserved</td>
</tr>
<tr>
<td>54</td>
<td>Reserved</td>
</tr>
<tr>
<td>53</td>
<td>Reserved</td>
</tr>
<tr>
<td>52</td>
<td>Reserved</td>
</tr>
<tr>
<td>51</td>
<td>Reserved</td>
</tr>
<tr>
<td>50</td>
<td>Reserved</td>
</tr>
<tr>
<td>49</td>
<td>Reserved</td>
</tr>
<tr>
<td>48</td>
<td>Reserved</td>
</tr>
<tr>
<td>47</td>
<td>Reserved</td>
</tr>
<tr>
<td>46</td>
<td>Reserved</td>
</tr>
<tr>
<td>45</td>
<td>Reserved</td>
</tr>
<tr>
<td>44</td>
<td>Reserved</td>
</tr>
<tr>
<td>43</td>
<td>Reserved</td>
</tr>
<tr>
<td>42</td>
<td>Reserved</td>
</tr>
<tr>
<td>41</td>
<td>Reserved</td>
</tr>
<tr>
<td>40</td>
<td>Reserved</td>
</tr>
<tr>
<td>39</td>
<td>Reserved</td>
</tr>
<tr>
<td>38</td>
<td>Reserved</td>
</tr>
<tr>
<td>37</td>
<td>Reserved</td>
</tr>
<tr>
<td>36</td>
<td>Reserved</td>
</tr>
<tr>
<td>35</td>
<td>Reserved</td>
</tr>
<tr>
<td>34</td>
<td>Reserved</td>
</tr>
<tr>
<td>33</td>
<td>Reserved</td>
</tr>
<tr>
<td>32</td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**DSSBS, bit [44]**

When **FEAT_SBS** is implemented:

Default PSTATE.SBS value on Exception Entry.

<table>
<thead>
<tr>
<th>DSSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.SBS is set to 0 on an exception to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>PSTATE.SBS is set to 1 on an exception to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to an **IMPLEMENTATION DEFINED** value.

**ATA, bit [43]**

When **FEAT_MTE2** is implemented:

Allocation Tag Access in EL3. Controls EL3 access to Allocation Tags.

When access to Allocation Tags is prevented:

- Instructions which Load or Store data are Unchecked.
- Instructions which Load or Store Allocation Tags treat the Allocation Tag as RAZ/WI.
• Instructions which insert Logical Address Tags into addresses treat the Allocation Tag used to generate the Logical Address Tag as 0.

• Cache maintenance instructions which invalidate Allocation Tags from caches behave as the equivalent Clean and Invalidate operation on Allocation Tags.

<table>
<thead>
<tr>
<th>ATA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Allocation Tags is prevented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Allocation Tags is not prevented.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Bit [42]**

Reserved, RES0.

**TCF, bits [41:40]**

When FEAT_MTE2 is implemented:

Tag Check Fault in EL3. Controls the effect of Tag Check Faults due to Loads and Stores in EL3.

If FEAT_MTE3 is not implemented, the value 0b11 is reserved.

<table>
<thead>
<tr>
<th>TCF</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Tag Check Faults have no effect on the PE.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Tag Check Faults cause a synchronous exception.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>Tag Check Faults are asynchronously accumulated.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>Tag Check Faults cause a synchronous exception on reads, and are asynchronously accumulated on writes.</td>
<td>When FEAT_MTE3 is implemented</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Bits [39:38]**

Reserved, RES0.

**ITFSB, bit [37]**

When FEAT_MTE2 is implemented:

When synchronous exceptions are not being generated by Tag Check Faults, this field controls whether on exception entry into EL3, all Tag Check Faults due to instructions executed before exception entry, that are reported asynchronously, are synchronized into TFSREQ_EL1 and TFSR_ELx registers.

<table>
<thead>
<tr>
<th>ITFSB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tag Check Faults are not synchronized on entry to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tag Check Faults are synchronized on entry to EL3.</td>
</tr>
</tbody>
</table>
On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

**BT, bit [36]**

When FEAT_BTI is implemented:

PAC Branch Type compatibility at EL3.

<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When the PE is executing at EL3, PACIASP and PACIBSP are compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
<tr>
<td>0b1</td>
<td>When the PE is executing at EL3, PACIASP and PACIBSP are not compatible with PSTATE.BTYPE == 0b11.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

**Bits [35:32]**

Reserved, RES0.

**EnIA, bit [31]**

When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APIAKey_EL1 key) of instruction addresses in the EL3 translation regime.

Possible values of this bit are:

<table>
<thead>
<tr>
<th>EnIA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIAKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

For more information, see ‘System register control of pointer authentication’.

**Note**

This field controls the behavior of the AddPACIA and AuthIA pseudocode functions. Specifically, when the field is 1, AddPACIA returns a copy of a pointer to which a pointer authentication code has been added, and AuthIA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

**EnIB, bit [30]**
When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APIBKey_EL1 key) of instruction addresses in the EL3 translation regime.

Possible values of this bit are:

<table>
<thead>
<tr>
<th>EnIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APIBKey_EL1 key) of instruction addresses is enabled.</td>
</tr>
</tbody>
</table>

For more information, see 'System register control of pointer authentication'.

**Note**

This field controls the behavior of the AddPACIB and AuthIB pseudocode functions. Specifically, when the field is 1, AddPACIB returns a copy of a pointer to which a pointer authentication code has been added, and AuthIB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Bits [29:28]**

Reserved, RES1.

**EnDA, bit [27]**

When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APDAKey_EL1 key) of instruction addresses in the EL3 translation regime.

<table>
<thead>
<tr>
<th>EnDA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDAKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

For more information, see 'System register control of pointer authentication'.

**Note**

This field controls the behavior of the AddPACDA and AuthDA pseudocode functions. Specifically, when the field is 1, AddPACDA returns a copy of a pointer to which a pointer authentication code has been added, and AuthDA returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
SCTLR_EL3, System Control Register (EL3)

Bit [26]
Reserved, RES0.

EE, bit [25]
Endianness of data accesses at EL3, and stage 1 translation table walks in the EL3 translation regime.

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Explicit data accesses at EL3, and stage 1 translation table walks</td>
</tr>
<tr>
<td></td>
<td>in the EL3 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Explicit data accesses at EL3, and stage 1 translation table walks</td>
</tr>
<tr>
<td></td>
<td>in the EL3 translation regime are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation does not provide Big-endian support at Exception Levels higher than EL0, this bit is RES0.
If an implementation does not provide Little-endian support at Exception Levels higher than EL0, this bit is RES1.
The EE bit is permitted to be cached in a TLB.
On a Warm reset, in a system where the PE resets into EL3, this field resets to an IMPLEMENTATION DEFINED value.

Bit [24]
Reserved, RES0.

Bit [23]
Reserved, RES1.

EIS, bit [22]
When FEAT_ExS is implemented:

Exception Entry is Context Synchronizing.

<table>
<thead>
<tr>
<th>EIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The taking of an exception to EL3 is not a context synchronizing</td>
</tr>
<tr>
<td></td>
<td>event.</td>
</tr>
<tr>
<td>0b1</td>
<td>The taking of an exception to EL3 is a context synchronizing event.</td>
</tr>
</tbody>
</table>

If SCTLR_EL3.EIS is set to 0b0:
• Indirect writes to ESR_EL3, FAR_EL3, SPSR_EL3, ELR_EL3 are synchronized on exception entry to EL3, so that a direct read of the register after exception entry sees the indirectly written value caused by the exception entry.
• Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
• Exception Catch debug events are synchronous debug events.
• DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL3.EIS:
• Changes to the PSTATE information on entry to EL3.
• Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores and data processing instructions.
• Debug state exit.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES1.
IESB, bit [21]

When FEAT_IESB is implemented:

Implicit Error Synchronization event enable.

<table>
<thead>
<tr>
<th>IESB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>An implicit error synchronization event is added:</td>
</tr>
<tr>
<td></td>
<td>• At each exception taken to EL3.</td>
</tr>
<tr>
<td></td>
<td>• Before the operational pseudocode of each ERET instruction executed at EL3.</td>
</tr>
</tbody>
</table>

When the PE is in Debug state, the effect of this field is CONSTRAINED UNPREDICTABLE, and its Effective value might be 0 or 1 regardless of the value of the field. If the Effective value of the field is 1, then an implicit error synchronization event is added after each `DCPSX` instruction taken to EL3 and before each `DRPS` instruction executed at EL3, in addition to the other cases where it is added.

When FEAT_DoubleFault is implemented, and the Effective value of SCR_EL3.NMEA is 1, this field is ignored and its Effective value is 1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [20]

Reserved, RES0.

WXN, bit [19]

Write permission implies XN (Execute-never). For the EL3 translation regime, this bit can force all memory regions that are writable to be treated as XN. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable in the EL3 translation regime is forced to XN for accesses from software executing at EL3.</td>
</tr>
</tbody>
</table>

This bit applies only when SCTLR_EL3.M bit is set.

The WXN bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Bit [18]

Reserved, RES1.

Bit [17]

Reserved, RES0.

Bit [16]

Reserved, RES1.

Bits [15:14]

Reserved, RES0.
EnDB, bit [13]

When FEAT_PAuth is implemented:

Controls enabling of pointer authentication (using the APDBKey_EL1 key) of instruction addresses in the EL3 translation regime.

<table>
<thead>
<tr>
<th>EnDB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is not enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Pointer authentication (using the APDBKey_EL1 key) of data addresses is enabled.</td>
</tr>
</tbody>
</table>

For more information, see ‘System register control of pointer authentication’.

**Note**

This field controls the behavior of the AddPACDB and AuthDB pseudocode functions. Specifically, when the field is 1, AddPACDB returns a copy of a pointer to which a pointer authentication code has been added, and AuthDB returns an authenticated copy of a pointer. When the field is 0, both of these functions are NOP.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

**Otherwise:**

Reserved, RES0.

I, bit [12]

Instruction access Cacheability control, for accesses at EL3:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction access to Normal memory from EL3 are non-cacheable for all levels of instruction and unified cache. If the value of SCTLR_EL3.M is 0, instruction accesses from stage 1 of the EL3 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Cacheability of instruction access to Normal memory from EL3. If the value of SCTLR_EL3.M is 0, instruction accesses from stage 1 of the EL3 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL1&0, EL2, or EL2&0 translation regimes.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

EOS, bit [11]

When FEAT_ExS is implemented:

Exception Exit is Context Synchronizing.

<table>
<thead>
<tr>
<th>EOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An exception return from EL3 is not a context synchronizing event</td>
</tr>
<tr>
<td>0b1</td>
<td>An exception return from EL3 is a context synchronizing event</td>
</tr>
</tbody>
</table>

If SCTLR_EL3.EOS is set to 0b0:

- Memory transactions, including instruction fetches, from an Exception level always use the translation resources associated with that translation regime.
- Exception Catch debug events are synchronous debug events.
DCPS* and DRPS instructions are context synchronization events.

The following are not affected by the value of SCTLR_EL3.EOS:

- The indirect write of the PSTATE and PC values from SPSR_EL3 and ELR_EL3 on exception return is synchronized.
- If the PE enters Debug state before the first instruction after an Exception return from EL3 to Non-secure state, any pending Halting debug event completes execution.
- The GIC behavior that allocates interrupts to FIQ or IRQ changes simultaneously with leaving the EL3 Exception level.
- Behavior of accessing the banked copies of the stack pointer using the SP register name for loads, stores and data processing instructions.
- Exit from Debug state.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES1.

**Bits [10:7]**

Reserved, RES0.

**nAA, bit [6]**

When FEAT_LSE2 is implemented:

Non-aligned access. This bit controls generation of Alignment faults at EL3 under certain conditions.

<table>
<thead>
<tr>
<th>nAA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSW, LDAPURSH, LDAPURSW, LDLAR, LDARH, LDLARH, STLR, STLURH, STLRH, STLRH, STLURH, and STLURH generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes for accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control bit does not cause LDAPR, LDAPRH, LDAPUR, LDAPURH, LDAPURSW, LDLARH, LDARH, LDLARH, LDLARH, STLRLR, STLRLR, STLRLR, STLRLR, STLRLR, STLRLR, STLRLR, or STLRLR to generate an Alignment fault if all bytes being accessed are not within a single 16-byte quantity, aligned to 16 bytes.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

**Bits [5:4]**

Reserved, RES1.

**SA, bit [3]**

SP Alignment check enable. When set to 1, if a load or store instruction executed at EL3 uses the SP as the base address and the SP is not aligned to a 16-byte boundary, then a SP alignment fault exception is generated. For more information, see ‘SP alignment checking’.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally unknown value.
C, bit [2]

Cacheability control, for data accesses.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All data access to Normal memory from EL3, and all Normal memory accesses to the EL3 translation tables, are Non-cacheable for all levels of data and unified cache.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control has no effect on the Cacheability of:</td>
</tr>
<tr>
<td></td>
<td>- Data access to Normal memory from EL3.</td>
</tr>
<tr>
<td></td>
<td>- Normal memory accesses to the EL3 translation tables.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL1&0, EL2, or EL2&0 translation regimes.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

A, bit [1]

Alignment check enable. This is the enable bit for Alignment fault checking at EL3.

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Alignment fault checking disabled when executing at EL3.</td>
</tr>
<tr>
<td></td>
<td>Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element(s) being accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alignment fault checking enabled when executing at EL3.</td>
</tr>
<tr>
<td></td>
<td>All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception.</td>
</tr>
</tbody>
</table>

Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

M, bit [0]

MMU enable for EL3 stage 1 address translation. Possible values of this bit are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL3 stage 1 address translation disabled.</td>
</tr>
<tr>
<td></td>
<td>See the SCTLR_EL3.I field for the behavior of instruction accesses to Normal memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL3 stage 1 address translation enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

Accessing the SCTLR_EL3

Accesses to this register use the following encodings:

\[
\text{MRS } <Xt>, \text{ SCTLR_EL3}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return SCTLR_EL3;

MSR SCTLR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    SCTLR_EL3 = X[t];
SCXTNUM_EL0, EL0 Read/Write Software Context Number

The SCXTNUM_EL0 characteristics are:

Purpose

Provides a number that can be used to separate out different context numbers with the EL0 exception level, for the purpose of protecting against side-channels using branch prediction and similar resources.

Configuration

This register is present only when FEAT_CSV2 is implemented. Otherwise, direct accesses to SCXTNUM_EL0 are UNDEFINED.

Attributes

SCXTNUM_EL0 is a 64-bit register.

Field descriptions

The SCXTNUM_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

Software Context Number. A number to identify the context within the EL0 exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SCXTNUM_EL0

Accesses to this register use the following encodings:

MRS <Xt>, SCXTNUM_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.TSCXT == '1' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    end if
  else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.EnSCXT == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
      HFGRTR_EL2.SCXTNUM_EL0 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.TSCXT == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end if
    else
      return SCXTNUM_EL0;
    end if
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.EnSCXT == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
    HFGRTR_EL2.SCXTNUM_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return SCXTNUM_EL0;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return SCXTNUM_EL0;
  end if
elsif PSTATE.EL == EL3 then
  return SCXTNUM_EL0;
end if

MSR SCXTNUM_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL0, 0x18);
    end
elsif !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.TSCXT == '1' then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL1, 0x18);
    end
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.EnSCXT == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCXTNUM_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.TSCXT == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    end
else
    SCXTNUM_EL0 = X[t];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.EnSCXT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCXTNUM_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    end
else
    SCXTNUM_EL0 = X[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
else
    SCXTNUM_EL0 = X[t];
elsif PSTATE.EL == EL3 then
    SCXTNUM_EL0 = X[t];
else
    SCXTNUM_EL0 = X[t];
The SCXTNUM_EL1 characteristics are:

**Purpose**

Provides a number that can be used to separate out different context numbers with the EL1 exception level, for the purpose of protecting against side-channels using branch prediction and similar resources.

**Configuration**

This register is present only when FEAT_CSV2 is implemented. Otherwise, direct accesses to SCXTNUM_EL1 are UNDEFINED.

**Attributes**

SCXTNUM_EL1 is a 64-bit register.

**Field descriptions**

The SCXTNUM_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Software Context Number | Software Context Number |

**Bits [63:0]**

Software Context Number. A number to identify the context within the EL1 exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the SCXTNUM_EL1**

Accesses to this register use the following encodings:

- MRS <Xt>, SCXTNUM_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.EnSCXT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.SCXTNUM_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif HCR_EL2.E2H == '1' then
        return SCXTNUM_EL2;
    else
        return SCXTNUM_EL1;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elseif HCR_EL2.E2H == '1' then
        return SCXTNUM_EL2;
    else
        return SCXTNUM_EL1;
    end if
elsif PSTATE.EL == EL3 then
    return SCXTNUM_EL1;
end if

MSR SCXTNUM_EL1, <Xt>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif EL2Enabled() && SCR_EL3.EnSCXT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && SCR_EL3.EnSCXT == '1' then
        UNDEFINED;
    elsif HCR_EL2.EnSCXT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif EL2Enabled() && HCR_EL2.EnSCXT == '1' then
        NVMem[0x188] = X[t];
    else
        SCXTNUM_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    elsif HCR_EL2.E2H == '1' then
        SCXTNUM_EL2 = X[t];
    else
        SCXTNUM_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    SCXTNUM_EL1 = X[t];
end if

MRS <Xt>, SCXTNUM_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x188];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            return SCXTNUM_EL1;
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return SCXTNUM_EL1;
    else
        UNDEFINED;
end

MSR SCXTNUM_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x188] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            SCXTNUM_EL1 = X[t];
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        SCXTNUM_EL1 = X[t];
    else
        UNDEFINED;
SCXTNUM_EL2, EL2 Read/Write Software Context Number

The SCXTNUM_EL2 characteristics are:

**Purpose**

Provides a number that can be used to separate out different context numbers with the EL2 exception level, for the purpose of protecting against side-channels using branch prediction and similar resources.

**Configuration**

This register is present only when FEAT_CSV2 is implemented. Otherwise, direct accesses to SCXTNUM_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

SCXTNUM_EL2 is a 64-bit register.

**Field descriptions**

The SCXTNUM_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>bits [63:0]</th>
<th>Software Context Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td></td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Software Context Number. A number to identify the context within the EL2 exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the SCXTNUM_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic SCXTNUM_EL2 or SCXTNUM_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    return SCXTNUM_EL2;
  end if
elsif PSTATE.EL == EL3 then
  return SCXTNUM_EL2;
end if

MSR SCXTNUM_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
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<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  else
    SCXTNUM EL2 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  SCXTNUM_EL2 = X[t];
end if

MRS <Xt>, SCXTNUM_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.EnSCXT == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.SCXTNUM_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.SystemAccessTrap(EL3, 0x18);
  end
elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
  return NVMem[0x188];
else
  return SCXTNUM_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  else
    return SCXTNUM_EL1;
  end
elsif PSTATE.EL == EL3 then
  return SCXTNUM_EL1;
endif

MSR SCXTNUM_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.EnSCXT == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.SCXTNUM_EL1 == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x188] = X[t];
    else
        SCXTNUM_EL1 = X[t];
    else
        SCXTNUM_EL2 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.EnSCXT == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.EnSCXT == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end
    elif HCR_EL2.E2H == '1' then
        SCXTNUM_EL2 = X[t];
    else
        SCXTNUM_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    SCXTNUM_EL2 = X[t];
else
    SCXTNUM_EL1 = X[t];
SCXTNUM_EL3, EL3 Read/Write Software Context Number

The SCXTNUM_EL3 characteristics are:

**Purpose**

Provides a number that can be used to separate out different context numbers with the EL3 exception level, for the purpose of protecting against side-channels using branch prediction and similar resources.

**Configuration**

This register is present only when EL3 is implemented and FEAT_CSV2 is implemented. Otherwise, direct accesses to SCXTNUM_EL3 are **undefined**.

**Attributes**

SCXTNUM_EL3 is a 64-bit register.

**Field descriptions**

The SCXTNUM_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Software Context Number</td>
</tr>
<tr>
<td>62</td>
<td>Software Context Number</td>
</tr>
<tr>
<td>61</td>
<td>Software Context Number</td>
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<tr>
<td>60</td>
<td>Software Context Number</td>
</tr>
<tr>
<td>59</td>
<td>Software Context Number</td>
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<td>58</td>
<td>Software Context Number</td>
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<td>Software Context Number</td>
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<td>39</td>
<td>Software Context Number</td>
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<td>38</td>
<td>Software Context Number</td>
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<tr>
<td>37</td>
<td>Software Context Number</td>
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<tr>
<td>36</td>
<td>Software Context Number</td>
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<td>35</td>
<td>Software Context Number</td>
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<tr>
<td>34</td>
<td>Software Context Number</td>
</tr>
<tr>
<td>33</td>
<td>Software Context Number</td>
</tr>
<tr>
<td>32</td>
<td>Software Context Number</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Software Context Number. A number to identify the context within the EL3 exception level.

On a Warm reset, this field resets to an architecturally **unknown** value.

**Accessing the SCXTNUM_EL3**

Accesses to this register use the following encodings:

```assembly
MRS <Xt>, SCXTNUM_EL3
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsiPSTATE.EL == EL1 then
  UNDEFINED;
elsiPSTATE.EL == EL2 then
  UNDEFINED;
elsiPSTATE.EL == EL3 then
  return SCXTNUM_EL3;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    SCXTNUM_EL3 = X[t];
SDER32_EL2, AArch32 Secure Debug Enable Register

The SDER32_EL2 characteristics are:

**Purpose**

Allows access to the AArch32 register SDER from Secure EL2 and EL3 only.

**Configuration**

This register is present only when EL2 is implemented, AArch32 is supported at any Exception level, FEAT_SEL2 is implemented and EL1 supports AArch32. Otherwise, direct accesses to SDER32_EL2 are UNDEFINED.

This register is ignored by the PE when one or more of the following are true:

- The PE is in Non-secure state.
- EL1 is using AArch64.

**Attributes**

SDER32_EL2 is a 64-bit register.

**Field descriptions**

The SDER32_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>SUNIDEN</td>
<td>Secure User Non-Invasive Debug Enable.</td>
</tr>
<tr>
<td>60</td>
<td>SUIDEN</td>
<td>Secure User Invasive Debug Enable.</td>
</tr>
<tr>
<td>59</td>
<td></td>
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<tr>
<td>1</td>
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<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SUNIDEN, bit [1]**

Secure User Non-Invasive Debug Enable.

<table>
<thead>
<tr>
<th>SUNIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect Performance Monitors event counting at Secure EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL1 is using AArch32, Performance Monitors event counting is allowed in Secure EL0.</td>
</tr>
</tbody>
</table>

**SUIDEN, bit [0]**

Secure User Invasive Debug Enable.

<table>
<thead>
<tr>
<th>SUIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect the generation of debug exceptions at Secure EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL1 is using AArch32, debug exceptions from Secure EL0 are enabled.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the SDER32_EL2

Accesses to this register use the following encodings:

**MRS <Xt>, SDER32_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        return SDER32_EL2;
    end if;
else
    SDER32_EL2 = X[t];
eendif;
```

**MSR SDER32_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        SDER32_EL2 = X[t];
    end if;
else
    SDER32_EL2 = X[t];
eendif;
```
SDER32_EL3, AArch32 Secure Debug Enable Register

The SDER32_EL3 characteristics are:

**Purpose**

Allows access to the AArch32 register SDER from AArch64 state only. Its value has no effect on execution in AArch64 state.

**Configuration**

AArch64 System register SDER32_EL3 bits [31:0] are architecturally mapped to AArch32 System register SDER[31:0].

This register is present only when EL3 is implemented, AArch32 is supported at any Exception level and EL1 supports AArch32. Otherwise, direct accesses to SDER32_EL3 are **UNDEFINED**.

This register is ignored by the PE when one or more of the following are true:

- The PE is in Non-secure state.
- EL1 is using AArch64.

**Attributes**

SDER32_EL3 is a 64-bit register.

**Field descriptions**

The SDER32_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td></td>
<td>RES0</td>
</tr>
<tr>
<td>31</td>
<td>SUNIDEN</td>
</tr>
</tbody>
</table>

**Bits [63:2]**

Reserved, RES0.

**SUNIDEN, bit [1]**

Secure User Non-Invasive Debug Enable.

<table>
<thead>
<tr>
<th>SUNIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect Performance Monitors event counting at Secure EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL1 is using AArch32, Performance Monitors event counting is allowed in Secure EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**SUIDEN, bit [0]**

Secure User Invasive Debug Enable.
### SDER32_EL3, AArch32 Secure Debug Enable Register

<table>
<thead>
<tr>
<th>SUIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect the generation of debug exceptions at Secure EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL1 is using AArch32, debug exceptions from Secure EL0 are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the SDER32_EL3

Accesses to this register use the following encodings:

**MRS <Xt>, SDER32_EL3**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return SDER32_EL3;
```

**MSR SDER32_EL3, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    SDER32_EL3 = X[t];
```
SP_EL0, Stack Pointer (EL0)

The SP_EL0 characteristics are:

Purpose

Holds the stack pointer associated with EL0. At higher Exception levels, this is used as the current stack pointer when the value of SPsel.SP is 0.

Configuration

There are no configuration notes.

Attributes

SP_EL0 is a 64-bit register.

Field descriptions

The SP_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Stack pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61</td>
<td></td>
</tr>
<tr>
<td>60 59 58</td>
<td></td>
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<tr>
<td>57 56 55</td>
<td></td>
</tr>
<tr>
<td>54 53 52</td>
<td></td>
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<tr>
<td>51 50 49</td>
<td></td>
</tr>
<tr>
<td>48 47 46</td>
<td></td>
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<tr>
<td>45 44 43</td>
<td></td>
</tr>
<tr>
<td>42 41 40</td>
<td></td>
</tr>
<tr>
<td>39 38 37</td>
<td></td>
</tr>
<tr>
<td>36 35 34</td>
<td></td>
</tr>
<tr>
<td>33 32 31</td>
<td>Stack pointer</td>
</tr>
<tr>
<td>30 29 28</td>
<td>Stack pointer</td>
</tr>
<tr>
<td>27 26 25</td>
<td></td>
</tr>
<tr>
<td>24 23 22</td>
<td></td>
</tr>
<tr>
<td>21 20 19</td>
<td></td>
</tr>
<tr>
<td>18 17 16</td>
<td></td>
</tr>
<tr>
<td>15 14 13</td>
<td></td>
</tr>
<tr>
<td>12 11 10</td>
<td></td>
</tr>
<tr>
<td>9 8 7</td>
<td></td>
</tr>
<tr>
<td>6 5 4</td>
<td></td>
</tr>
<tr>
<td>3 2 1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:0]

Stack pointer:

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SP_EL0

When the value of PSTATE.SP is 0, this register is accessible at all Exception levels as the current stack pointer.

Accesses to this register use the following encodings:

MRS <Xt>, SP_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    return SP_EL0;
elsif PSTATE.EL == EL2 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    return SP_EL0;
elsif PSTATE.EL == EL3 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    return SP_EL0;

MSR SP_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    SP_EL0 = X[t];
elsif PSTATE.EL == EL2 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    SP_EL0 = X[t];
elsif PSTATE.EL == EL3 then
  if PSTATE.SP == '0' then
    UNDEFINED;
  else
    SP_EL0 = X[t];
SP_EL1, Stack Pointer (EL1)

The SP_EL1 characteristics are:

**Purpose**

Holds the stack pointer associated with EL1. When executing at EL1, the value of `SPSel.SP` determines the current stack pointer:

<table>
<thead>
<tr>
<th>SP_SEL</th>
<th>Current stack pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SP_EL0</td>
</tr>
<tr>
<td>0b1</td>
<td>SP_EL1</td>
</tr>
</tbody>
</table>

**Configuration**

There are no configuration notes.

**Attributes**

SP_EL1 is a 64-bit register.

**Field descriptions**

The SP_EL1 bit assignments are:

```
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
```

**Bits [63:0]**

Stack pointer.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SP_EL1**

This accessibility information only applies to accesses using the MRS or MSR instructions.

When the value of `SPSel.SP` is 1, this register is also accessible at EL1 as the current stack pointer.

---

**Note**

When the value of `SPSel.SP` is 0, **SP_EL0** is used as the current stack pointer at all Exception levels.

Accesses to this register use the following encodings:

**MRS <Xt>, SP_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x240];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  return SP_EL1;
elsif PSTATE.EL == EL3 then
  return SP_EL1;
endif

MSR SP_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x240] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  SP_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  SP_EL1 = X[t];
endif

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SP_EL2, Stack Pointer (EL2)

The SP_EL2 characteristics are:

**Purpose**

Holds the stack pointer associated with EL2. When executing at EL2, the value of **SPSel**.SP determines the current stack pointer:

<table>
<thead>
<tr>
<th>SPSel.SP</th>
<th>Current stack pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SP_EL0</td>
</tr>
<tr>
<td>0b1</td>
<td>SP_EL2</td>
</tr>
</tbody>
</table>

**Configuration**

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

SP_EL2 is a 64-bit register.

**Field descriptions**

The SP_EL2 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

Stack pointer.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SP_EL2**

This accessibility information only applies to accesses using the MRS or MSR instructions.

When the value of **SPSel**.SP is 1, this register is also accessible at EL2 as the current stack pointer.

**Note**

When the value of **SPSel**.SP is 0, **SP_EL0** is used as the current stack pointer at all Exception levels.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return SP_EL2;

MSR SP_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    SP_EL2 = X[t];
The SP_El3 characteristics are:

**Purpose**

Holds the stack pointer associated with EL3. When executing at EL3, the value of SPSel.SP determines the current stack pointer:

<table>
<thead>
<tr>
<th>SPSel.SP</th>
<th>Current stack pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SP_EL0</td>
</tr>
<tr>
<td>0b1</td>
<td>SP_EL3</td>
</tr>
</tbody>
</table>

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to SP_EL3 are undefined.

**Attributes**

SP_EL3 is a 64-bit register.

**Field descriptions**

The SP_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:0]</th>
<th>Stack pointer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stack pointer</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Stack pointer.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the SP_EL3**

This register is not accessible using MRS and MSR instructions.

When the value of SPSel.SP is 1, this register is accessible at EL3 as the current stack pointer.

**Note**

When the value of SPSel.SP is 0, SP_EL0 is used as the current stack pointer at all Exception levels.
SPSel, Stack Pointer Select

The SPSel characteristics are:

**Purpose**

Allows the Stack Pointer to be selected between SP_EL0 and SP_ELx.

**Configuration**

There are no configuration notes.

**Attributes**

SPSel is a 64-bit register.

**Field descriptions**

The SPSel bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | SP |

**Bits [63:1]**

Reserved, RES0.

**SP, bit [0]**

Stack pointer to use. Possible values of this bit are:

<table>
<thead>
<tr>
<th>SP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Use SP_EL0 at all Exception levels.</td>
</tr>
<tr>
<td>0b1</td>
<td>Use SP_ELx for Exception level ELx.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 1.

**Accessing the SPSel**

Accesses to this register use the following encodings:

```
MRS <Xt>, SPSel
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    return Zeros(63):PSTATE.SP;
elsif PSTATE.EL == EL2 then
    return Zeros(63):PSTATE.SP;
elsif PSTATE.EL == EL3 then
    return Zeros(63):PSTATE.SP;

MSR SPSel, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    PSTATE.SP = X[t]<0>;
elsif PSTATE.EL == EL2 then
    PSTATE.SP = X[t]<0>;
elsif PSTATE.EL == EL3 then
    PSTATE.SP = X[t]<0>;

MSR SPSel, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211

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SPSR_abt, Saved Program Status Register (Abort mode)

The SPSR_abt characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Abort mode.

**Configuration**

AArch64 System register SPSR_abt bits [31:0] are architecturally mapped to AArch32 System register SPSR_abt[31:0].

If EL1 only supports execution in AArch64 state, this register is RES0 from EL2 and EL3.

**Attributes**

SPSR_abt is a 64-bit register.

**Field descriptions**

The SPSR_abt bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| N  | Z  | C  | V  | Q  | IT[1:0] | SSB | SPAN | DIT | IL | GE | IT[7:2] | E  | A  | I  | F  | T  | M[4:0] | RES0 |

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Abort mode, and copied to PSTATE.N on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Abort mode, and copied to PSTATE.Z on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Abort mode, and copied to PSTATE.C on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
V, bit [28]

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Abort mode, and copied to PSTATE.V on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Abort mode, and copied to PSTATE.Q on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Abort mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Abort mode.

On executing an exception return operation in Abort mode SPSR_abt.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

J, bit [24]

RES0.

In previous versions of the architecture, the {J, T} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Abort mode, and copied to PSTATE.SSBS on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Abort mode, and copied to PSTATE.PAN on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
**DIT, bit [21]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Abort mode, and copied to PSTATE.DIT on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Abort mode, and copied to PSTATE.IL on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Abort mode, and copied to PSTATE.GE on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Abort mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Abort mode.

SPSR_abt.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to Abort mode, and copied to PSTATE.E on executing an exception return operation in Abort mode.

If the implementation does not support big-endian operation, SPSR_abt.E is RES0. If the implementation does not support little-endian operation, SPSR_abt.E is RES1. On executing an exception return operation in Abort mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_abt.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_abt.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Abort mode, and copied to PSTATE.A on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Abort mode, and copied to PSTATE.I on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Abort mode, and copied to PSTATE.F on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Abort mode, and copied to PSTATE.T on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Abort mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Abort mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_abt.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Abort mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the SPSR_abt

Accesses to this register use the following encodings:

**MRS <Xt>, SPSR_abt**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return SPSR_abt;
elsif PSTATE.EL == EL3 then
  return SPSR_abt;

**MSR SPSR_abt, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  SPSR_abt = X[t];
elsif PSTATE.EL == EL3 then
  SPSR_abt = X[t];
SPSR_EL1, Saved Program Status Register (EL1)

The SPSR_EL1 characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to EL1.

**Configuration**

AArch64 System register SPSR_EL1 bits [31:0] are architecturally mapped to AArch32 System register SPSR_svc[31:0].

**Attributes**

SPSR_EL1 is a 64-bit register.

**Field descriptions**

The SPSR_EL1 bit assignments are:

**When AArch32 is supported at any Exception level and exception taken from AArch32 state:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

An exception return from EL1 using AArch64 makes SPSR_EL1 become UNKNOWN.

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL1, and copied to PSTATE.N on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL1, and copied to PSTATE.Z on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL1, and copied to PSTATE.C on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
V, bit [28]

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL1, and copied to PSTATE.V on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to EL1, and copied to PSTATE.Q on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to EL1, and copied to PSTATE.IT[1:0] on executing an exception return operation in EL1.

On executing an exception return operation in EL1 SPSR_EL1.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DIT, bit [24]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL1, and copied to PSTATE.DIT on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

SSBS, bit [23]

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL1, and copied to PSTATE.SSBS on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL1, and copied to PSTATE.PAN on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

SS, bit [21]

Software Step. Set to the value of PSTATE_SS on taking an exception to EL1, and conditionally copied to PSTATE_SS on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE_IL on taking an exception to EL1, and copied to PSTATE_IL on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE_GE on taking an exception to EL1, and copied to PSTATE_GE on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to EL1, and copied to PSTATE.IT[7:2] on executing an exception return operation in EL1.

SPSR_EL1.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE_E on taking an exception to EL1, and copied to PSTATE_E on executing an exception return operation in EL1.

If the implementation does not support big-endian operation, SPSR_EL1.E is RES0. If the implementation does not support little-endian operation, SPSR_EL1.E is RES1. On executing an exception return operation in EL1, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_EL1.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_EL1.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE_A on taking an exception to EL1, and copied to PSTATE_A on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE_I on taking an exception to EL1, and copied to PSTATE_I on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL1, and copied to PSTATE.F on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to EL1, and copied to PSTATE.T on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4], bit [4]

Execution state. Set to \(0b1\), the value of PSTATE.nRW, on taking an exception to EL1 from AArch32 state, and copied to PSTATE.nRW on executing an exception return operation in EL1.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b1)</td>
<td>AArch32 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]

AArch32 Mode. Set to the value of PSTATE.M[3:0] on taking an exception to EL1, and copied to PSTATE.M[3:0] on executing an exception return operation in EL1.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0000)</td>
<td>User.</td>
</tr>
<tr>
<td>(0b0001)</td>
<td>FIQ.</td>
</tr>
<tr>
<td>(0b0010)</td>
<td>IRQ.</td>
</tr>
<tr>
<td>(0b0011)</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>(0b0111)</td>
<td>Abort.</td>
</tr>
<tr>
<td>(0b1011)</td>
<td>Undefined.</td>
</tr>
<tr>
<td>(0b1111)</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL1.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL1 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When exception taken from AArch64 state:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

An exception return from EL1 using AArch64 makes SPSR_EL1 become UNKNOWN.

Bits [63:32]

Reserved, RES0.

N, bit [31]

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL1, and copied to PSTATE.N on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Z, bit [30]
Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL1, and copied to PSTATE.Z on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

C, bit [29]
Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL1, and copied to PSTATE.C on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

V, bit [28]
Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL1, and copied to PSTATE.V on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [27:26]
Reserved, RES0.

TCO, bit [25]
When FEAT_MTE is implemented:
Tag Check Override. Set to the value of PSTATE.TCO on taking an exception to EL1, and copied to PSTATE.TCO on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

DIT, bit [24]
When FEAT_DIT is implemented:
Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL1, and copied to PSTATE.DIT on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

UAO, bit [23]
When FEAT_UAO is implemented:
User Access Override. Set to the value of PSTATE.UAO on taking an exception to EL1, and copied to PSTATE.UAO on executing an exception return operation in EL1.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

  Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL1, and copied to PSTATE.PAN on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

  Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on taking an exception to EL1, and conditionally copied to PSTATE.SS on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to EL1, and copied to PSTATE.IL on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [19:13]**

Reserved, RES0.

**SSBS, bit [12]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL1, and copied to PSTATE.SSBS on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

  Reserved, RES0.

**BTYPE, bits [11:10]**

*When FEAT_BTI is implemented:*

Branch Type Indicator. Set to the value of PSTATE.BTYPE on taking an exception to EL1, and copied to PSTATE.BTYPE on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

  Reserved, RES0.
D, bit [9]

Debug exception mask. Set to the value of PSTATE.D on taking an exception to EL1, and copied to PSTATE.D on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to EL1, and copied to PSTATE.A on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to EL1, and copied to PSTATE.I on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL1, and copied to PSTATE.F on executing an exception return operation in EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.

M[4], bit [4]

Execution state. Set to 0b0, the value of PSTATE.nRW, on taking an exception to EL1 from AArch64 state, and copied to PSTATE.nRW on executing an exception return operation in EL1.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch64 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]

AArch64 Exception level and selected Stack Pointer.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL0t.</td>
</tr>
<tr>
<td>0b0100</td>
<td>EL1t.</td>
</tr>
<tr>
<td>0b0101</td>
<td>EL1h.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL1.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL1 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

The bits in this field are interpreted as follows:

- M[3:2] is set to the value of PSTATE.EL on taking an exception to EL1 and copied to PSTATE.EL on executing an exception return operation in EL1.
- M[1] is unused and is 0 for all non-reserved values.
- M[0] is set to the value of PSTATE.SP on taking an exception to EL1 and copied to PSTATE.SP on executing an exception return operation in EL1

On a Warm reset, this field resets to an architecturally UNKNOWN value.
SPSR_EL1, Saved Program Status Register (EL1)

Accessing the SPSR_EL1

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic SPSR_EL1 or SPSR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, SPSR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x160];
  else
    return SPSR_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return SPSR_EL2;
  else
    return SPSR_EL1;
elsif PSTATE.EL == EL3 then
  return SPSR_EL1;

MSR SPSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x160] = X[t];
  else
    SPSR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    SPSR_EL2 = X[t];
  else
    SPSR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
  SPSR_EL1 = X[t];

MRS <Xt>, SPSR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x160];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return SPSR_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return SPSR_EL1;
    else
        UNDEFINED;
MSR SPSR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x160] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        SPSR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        SPSR_EL1 = X[t];
    else
        UNDEFINED;
MRS <Xt>, SPSR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return SPSR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return SPSR_EL2;
elsif PSTATE.EL == EL3 then
    return SPSR_EL2;
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    SPSR_EL1 = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  SPSR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  SPSR_EL3 = X[t];

SPSR_EL2, Saved Program Status Register (EL2)

The SPSR_EL2 characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to EL2.

**Configuration**

AArch64 System register SPSR_EL2 bits [31:0] are architecturally mapped to AArch32 System register SPSR_hyp[31:0].

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

SPSR_EL2 is a 64-bit register.

**Field descriptions**

The SPSR_EL2 bit assignments are:

**When AArch32 is supported at any Exception level and exception taken from AArch32 state:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| **N** | **Z** | **C** | **V** | **Q** | **I[1:0]** | **DIT** | **SSBS** | **PAN** | **SS** | **IL** | **GE** | **IT[7:2]** | **E** | **A** | **I** | **F** | **T** | **M[4]** | **M[3:0]** |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

An exception return from EL2 using AArch64 makes SPSR_EL2 become **UNKNOWN**.

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL2, and copied to PSTATE.N on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL2, and copied to PSTATE.Z on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL2, and copied to PSTATE.C on executing an exception return operation in EL2.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL2, and copied to PSTATE.V on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to EL2, and copied to PSTATE.Q on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to EL2, and copied to PSTATE.IT[1:0] on executing an exception return operation in EL2.

On executing an exception return operation in EL2 SPSR_EL2.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DIT, bit [24]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL2, and copied to PSTATE.DIT on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL2, and copied to PSTATE.SSBS on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL2, and copied to PSTATE.PAN on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on taking an exception to EL2, and conditionally copied to PSTATE.SS on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to EL2, and copied to PSTATE.IL on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to EL2, and copied to PSTATE.GE on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to EL2, and copied to PSTATE.IT[7:2] on executing an exception return operation in EL2.

SPSR_EL2.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to EL2, and copied to PSTATE.E on executing an exception return operation in EL2.

If the implementation does not support big-endian operation, SPSR_EL2.E is RES0. If the implementation does not support little-endian operation, SPSR_EL2.E is RES1. On executing an exception return operation in EL2, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_EL2.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_EL2.E is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to EL2, and copied to PSTATE.A on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to EL2, and copied to PSTATE.I on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL2, and copied to PSTATE.F on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to EL2, and copied to PSTATE.T on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4], bit [4]

Execution state. Set to 0b1, the value of PSTATE.nRW, on taking an exception to EL2 from AArch32 state, and copied to PSTATE.nRW on executing an exception return operation in EL2.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>AArch32 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]

AArch32 Mode. Set to the value of PSTATE.M[3:0] on taking an exception to EL2, and copied to PSTATE.M[3:0] on executing an exception return operation in EL2.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>User.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b0010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b1111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL2.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL2 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When exception taken from AArch64 state:

When a Soft Fault exception occurs, the exception return from EL2 using AArch64 makes SPSR_EL2 become UNKNOWN.

Bits [63:32]

Reserved, RES0.

N, bit [31]

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL2, and copied to PSTATE.N on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Z, bit [30]

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL2, and copied to PSTATE.Z on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

C, bit [29]

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL2, and copied to PSTATE.C on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

V, bit [28]

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL2, and copied to PSTATE.V on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [27:26]

Reserved, RES0.

TCO, bit [25]

When FEAT_MTE is implemented:

Tag Check Override. Set to the value of PSTATE.TCO on taking an exception to EL2, and copied to PSTATE.TCO on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

DIT, bit [24]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL2, and copied to PSTATE.DIT on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

UAO, bit [23]

When FEAT_UAO is implemented:

User Access Override. Set to the value of PSTATE.UAO on taking an exception to EL2, and copied to PSTATE.UAO on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**PAN, bit [22]**

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL2, and copied to PSTATE.PAN on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on taking an exception to EL2, and conditionally copied to PSTATE.SS on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to EL2, and copied to PSTATE.IL on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:13]**

Reserved, RES0.

**SSBS, bit [12]**

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL2, and copied to PSTATE.SSBS on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**BTYPE, bits [11:10]**

When FEAT_BT is implemented:

Branch Type Indicator. Set to the value of PSTATE.BTYPE on taking an exception to EL2, and copied to PSTATE.BTYPE on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
D, bit [9]

Debug exception mask. Set to the value of PSTATE.D on taking an exception to EL2, and copied to PSTATE.D on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to EL2, and copied to PSTATE.A on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to EL2, and copied to PSTATE.I on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL2, and copied to PSTATE.F on executing an exception return operation in EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.

M[4], bit [4]

Execution state. Set to \(0b0\), the value of PSTATE.nRW, on taking an exception to EL2 from AArch64 state, and copied to PSTATE.nRW on executing an exception return operation in EL2.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch64 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]

AArch64 Exception level and selected Stack Pointer.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL0t.</td>
</tr>
<tr>
<td>0b0100</td>
<td>EL1t.</td>
</tr>
<tr>
<td>0b0101</td>
<td>EL1h.</td>
</tr>
<tr>
<td>0b1000</td>
<td>EL2t.</td>
</tr>
<tr>
<td>0b1001</td>
<td>EL2h.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL2.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL2 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

The bits in this field are interpreted as follows:

- \(M[3:2]\) is set to the value of PSTATE.EL on taking an exception to EL2 and copied to PSTATE.EL on executing an exception return operation in EL2.
- \(M[1]\) is unused and is 0 for all non-reserved values.
- \(M[0]\) is set to the value of PSTATE.SP on taking an exception to EL2 and copied to PSTATE.SP on executing an exception return operation in EL2.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the SPSR_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic SPSR_EL2 or SPSR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, SPSR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return SPSR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return SPSR_EL2;
elsif PSTATE.EL == EL3 then
    return SPSR_EL2;
```  

**MSR SPSR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        SPSR_EL1 = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    SPSR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    SPSR_EL2 = X[t];
```  

**MRS <Xt>, SPSR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x160];
    else
        return SPSR_EL1;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return SPSR_EL2;
    else
        return SPSR_EL1;
elsif PSTATE.EL == EL3 then
    return SPSR_EL1;

MSR SPSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x160] = X[t];
    else
        SPSR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        SPSR_EL2 = X[t];
    else
        SPSR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    SPSR_EL1 = X[t];
SPSR_EL3, Saved Program Status Register (EL3)

The SPSR_EL3 characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to EL3.

**Configuration**

AArch64 System register SPSR_EL3 bits [31:0] can be mapped to AArch32 System register SPSR_mon[31:0], but this is not architecturally mandated.

This register is present only when EL3 is implemented. Otherwise, direct accesses to SPSR_EL3 are UNDEFINED.

**Attributes**

SPSR_EL3 is a 64-bit register.

**Field descriptions**

The SPSR_EL3 bit assignments are:

**When AArch32 is supported at any Exception level and exception taken from AArch32 state:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

An exception return from EL3 using AArch64 makes SPSR_EL1 become UNKNOWN.

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL3, and copied to PSTATE.N on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL3, and copied to PSTATE.Z on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL3, and copied to PSTATE.C on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL3, and copied to PSTATE.V on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to EL3, and copied to PSTATE.Q on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to EL3, and copied to PSTATE.IT[1:0] on executing an exception return operation in EL3.

On executing an exception return operation in EL3 SPSR_EL1.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DIT, bit [24]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL3, and copied to PSTATE.DIT on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL3, and copied to PSTATE.SSBS on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL3, and copied to PSTATE.PAN on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
SPSR_EL3, Saved Program Status Register (EL3)

Otherwise:

Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on taking an exception to EL3, and conditionally copied to PSTATE.SS on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to EL3, and copied to PSTATE.IL on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to EL3, and copied to PSTATE.GE on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to EL3, and copied to PSTATE.IT[7:2] on executing an exception return operation in EL3.

SPSR_EL1.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to EL3, and copied to PSTATE.E on executing an exception return operation in EL3.

If the implementation does not support big-endian operation, SPSR_EL1.E is RES0. If the implementation does not support little-endian operation, SPSR_EL1.E is RES1. On executing an exception return operation in EL3, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_EL1.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_EL1.E is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to EL3, and copied to PSTATE.A on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to EL3, and copied to PSTATE.I on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
**F, bit [6]**

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL3, and copied to PSTATE.F on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**T, bit [5]**

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to EL3, and copied to PSTATE.T on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**M[4], bit [4]**

Execution state. Set to 0b1, the value of PSTATE.nRW, on taking an exception to EL3 from AArch32 state, and copied to PSTATE.nRW on executing an exception return operation in EL3.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>AArch32 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**M[3:0], bits [3:0]**

AArch32 Mode. Set to the value of PSTATE.M[3:0] on taking an exception to EL3, and copied to PSTATE.M[3:0] on executing an exception return operation in EL3.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>User</td>
</tr>
<tr>
<td>0b0001</td>
<td>FIQ</td>
</tr>
<tr>
<td>0b0010</td>
<td>IRQ</td>
</tr>
<tr>
<td>0b0011</td>
<td>Supervisor</td>
</tr>
<tr>
<td>0b0110</td>
<td>Monitor</td>
</tr>
<tr>
<td>0b0111</td>
<td>Abort</td>
</tr>
<tr>
<td>0b1010</td>
<td>Hyp</td>
</tr>
<tr>
<td>0b1011</td>
<td>Undefined</td>
</tr>
<tr>
<td>0b1111</td>
<td>System</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL1.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL3 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When exception taken from AArch64 state:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| N  | Z  | C  | V  | RES0 | TCO | DI | TI | UA | AO | PA | N  | SS | IL | RES0 | SSBS | BTYPE | D | A | I | F | RES0 | M[4] | M[3:0] |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

An exception return from EL3 using AArch64 makes SPSR_EL1 become **UNKNOWN**.

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to EL3, and copied to PSTATE.N on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Z, bit [30]

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to EL3, and copied to PSTATE.Z on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### C, bit [29]

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to EL3, and copied to PSTATE.C on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### V, bit [28]

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to EL3, and copied to PSTATE.V on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [27:26]

Reserved, RES0.

### TCO, bit [25]

**When FEAT_MTE is implemented:**

Tag Check Override. Set to the value of PSTATE.TCO on taking an exception to EL3, and copied to PSTATE.TCO on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

### DIT, bit [24]

**When FEAT_DIT is implemented:**

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to EL3, and copied to PSTATE.DIT on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

### UAO, bit [23]

**When FEAT_UAO is implemented:**

User Access Override. Set to the value of PSTATE.UAO on taking an exception to EL3, and copied to PSTATE.UAO on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**PAN, bit [22]**

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to EL3, and copied to PSTATE.PAN on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on taking an exception to EL3, and conditionally copied to PSTATE.SS on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to EL3, and copied to PSTATE.IL on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:13]**

Reserved, RES0.

**SSBS, bit [12]**

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to EL3, and copied to PSTATE.SSBS on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**BTYPE, bits [11:10]**

When FEAT_BTI is implemented:

Branch Type Indicator. Set to the value of PSTATE.BTYPE on taking an exception to EL3, and copied to PSTATE.BTYPE on executing an exception return operation in EL3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
D, bit [9]
Debug exception mask. Set to the value of PSTATE.D on taking an exception to EL3, and copied to PSTATE.D on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]
SError interrupt mask. Set to the value of PSTATE.A on taking an exception to EL3, and copied to PSTATE.A on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]
IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to EL3, and copied to PSTATE.I on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]
FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to EL3, and copied to PSTATE.F on executing an exception return operation in EL3.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]
Reserved, RES0.

M[4], bit [4]
Execution state. Set to 0b0, the value of PSTATE.nRW, on taking an exception to EL3 from AArch64 state, and copied to PSTATE.nRW on executing an exception return operation in EL3.

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch64 execution state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[3:0], bits [3:0]
AArch64 Exception level and selected Stack Pointer.

<table>
<thead>
<tr>
<th>M[3:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL0t.</td>
</tr>
<tr>
<td>0b0100</td>
<td>EL1t.</td>
</tr>
<tr>
<td>0b0101</td>
<td>EL1h.</td>
</tr>
<tr>
<td>0b1000</td>
<td>EL2t.</td>
</tr>
<tr>
<td>0b1001</td>
<td>EL2h.</td>
</tr>
<tr>
<td>0b1100</td>
<td>EL3t.</td>
</tr>
<tr>
<td>0b1101</td>
<td>EL3h.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_EL1.M[3:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in EL3 is an illegal return event, as described in ‘Illegal return events from AArch64 state’.

The bits in this field are interpreted as follows:

- M[3:2] is set to the value of PSTATE.EL on taking an exception to EL3 and copied to PSTATE.EL on executing an exception return operation in EL3.
- M[1] is unused and is 0 for all non-reserved values.
M[0] is set to the value of PSTATE.SP on taking an exception to EL3 and copied to PSTATE.SP on executing an exception return operation in EL3

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the SPSR_EL3

Accesses to this register use the following encodings:

**MRS <Xt>, SPSR_EL3**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return SPSR_EL3;

**MSR SPSR_EL3, <Xt>**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  SPSR_EL3 = X[t];
SPSR_fiq, Saved Program Status Register (FIQ mode)

The SPSR_fiq characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to FIQ mode.

**Configuration**

AArch64 System register SPSR_fiq bits [31:0] are architecturally mapped to AArch32 System register SPSR_fiq[31:0].

If EL1 only supports execution in AArch64 state, this register is RES0 from EL2 and EL3.

**Attributes**

SPSR_fiq is a 64-bit register.

**Field descriptions**

The SPSR_fiq bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to FIQ mode, and copied to PSTATE.N on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to FIQ mode, and copied to PSTATE.Z on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to FIQ mode, and copied to PSTATE.C on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to FIQ mode, and copied to PSTATE.V on executing an exception return operation in FIQ mode.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to FIQ mode, and copied to PSTATE.Q on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to FIQ mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in FIQ mode.

On executing an exception return operation in FIQ mode SPSR_fiq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**J, bit [24]**

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to FIQ mode, and copied to PSTATE.SSBS on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to FIQ mode, and copied to PSTATE.PAN on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**DIT, bit [21]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to FIQ mode, and copied to PSTATE.DIT on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to FIQ mode, and copied to PSTATE.IL on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to FIQ mode, and copied to PSTATE.GE on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to FIQ mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in FIQ mode.

SPSR_fiq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to FIQ mode, and copied to PSTATE.E on executing an exception return operation in FIQ mode.

If the implementation does not support big-endian operation, SPSR_fiq.E is RES0. If the implementation does not support little-endian operation, SPSR_fiq.E is RES1. On executing an exception return operation in FIQ mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_fiq.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_fiq.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to FIQ mode, and copied to PSTATE.A on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to FIQ mode, and copied to PSTATE.I on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to FIQ mode, and copied to PSTATE.F on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
T[5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to FIQ mode, and copied to PSTATE.T on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to FIQ mode, and copied to PSTATE.M[4:0] on executing an exception return operation in FIQ mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_fiq.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in FIQ mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_fiq

Accesses to this register use the following encodings:

MRS <Xt>, SPSR_fiq

```assembly
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return SPSR_fiq;
elsif PSTATE.EL == EL3 then
  return SPSR_fiq;
end if;
```

MSR SPSR_fiq, <Xt>

```assembly
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return SPSR_fiq;
elsif PSTATE.EL == EL3 then
  return SPSR_fiq;
end if;
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    SPSR_fiq = X[t];
elsif PSTATE.EL == EL3 then
    SPSR_fiq = X[t];
**SPSR_irq**, Saved Program Status Register (IRQ mode)

The SPSR_irq characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to IRQ mode.

**Configuration**

AArch64 System register SPSR_irq bits [31:0] are architecturally mapped to AArch32 System register SPSR_irq[31:0]. If EL1 only supports execution in AArch64 state, this register is RES0 from EL2 and EL3.

**Attributes**

SPSR_irq is a 64-bit register.

**Field descriptions**

The SPSR_irq bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td><strong>N</strong>, bit [31] Negative Condition flag. Set to the value of PSTATE.N on taking an exception to IRQ mode, and copied to PSTATE.N on executing an exception return operation in IRQ mode.</td>
</tr>
<tr>
<td>61</td>
<td><strong>Z</strong>, bit [30] Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to IRQ mode, and copied to PSTATE.Z on executing an exception return operation in IRQ mode.</td>
</tr>
<tr>
<td>60</td>
<td><strong>C</strong>, bit [29] Carry Condition flag. Set to the value of PSTATE.C on taking an exception to IRQ mode, and copied to PSTATE.C on executing an exception return operation in IRQ mode.</td>
</tr>
<tr>
<td>59</td>
<td><strong>V</strong>, bit [28] Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to IRQ mode, and copied to PSTATE.V on executing an exception return operation in IRQ mode.</td>
</tr>
</tbody>
</table>

Bits [63:32]

Reserved, RES0.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to IRQ mode, and copied to PSTATE.Q on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to IRQ mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in IRQ mode.

On executing an exception return operation in IRQ mode SPSR_irq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**J, bit [24]**

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

**SSBS, bit [23]**

**When FEAT_SSBS is implemented:**

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to IRQ mode, and copied to PSTATE.SSBS on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**PAN, bit [22]**

**When FEAT_PAN is implemented:**

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to IRQ mode, and copied to PSTATE.PAN on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**DIT, bit [21]**

**When FEAT_DIT is implemented:**

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to IRQ mode, and copied to PSTATE.DIT on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to IRQ mode, and copied to PSTATE.IL on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to IRQ mode, and copied to PSTATE.GE on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to IRQ mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in IRQ mode.

SPSR_irq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to IRQ mode, and copied to PSTATE.E on executing an exception return operation in IRQ mode.

If the implementation does not support big-endian operation, SPSR_irq.E is RES0. If the implementation does not support little-endian operation, SPSR_irq.E is RES1. On executing an exception return operation in IRQ mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_irq.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_irq.E is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to IRQ mode, and copied to PSTATE.A on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to IRQ mode, and copied to PSTATE.I on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**F, bit [6]**

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to IRQ mode, and copied to PSTATE.F on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to IRQ mode, and copied to PSTATE.T on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to IRQ mode, and copied to PSTATE.M[4:0] on executing an exception return operation in IRQ mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_irq.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in IRQ mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_irq

Accesses to this register use the following encodings:

\[
\text{MRS <Xt>, SPSR_irq}
\]

\[
\begin{array}{c c c c c}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b11 & 0b100 & 0b0100 & 0b0011 & 0b000 \\
\end{array}
\]

\[
\begin{array}{c c c c c}
\text{op0} & \text{op1} & \text{CRn} & \text{CRm} & \text{op2} \\
0b11 & 0b100 & 0b0100 & 0b0011 & 0b000 \\
\end{array}
\]

\[
\text{MSR SPSR_irq, <Xt>}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    SPSR_irq = X[t];
elsif PSTATE.EL == EL3 then
    SPSR_irq = X[t];
SPSR_und, Saved Program Status Register (Undefined mode)

The SPSR_und characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Undefined mode.

**Configuration**

AArch64 System register SPSR_und bits [31:0] are architecturally mapped to AArch32 System register SPSR_und[31:0].

If EL1 only supports execution in AArch64 state, this register is RES0 from EL2 and EL3.

**Attributes**

SPSR_und is a 64-bit register.

**Field descriptions**

The SPSR_und bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | RES0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:32]**

Reserved, RES0.

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Undefined mode, and copied to PSTATE.N on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Undefined mode, and copied to PSTATE.Z on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Undefined mode, and copied to PSTATE.C on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
V, bit [28]

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Undefined mode, and copied to PSTATE.V on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Undefined mode, and copied to PSTATE.Q on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

IT[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Undefined mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Undefined mode.

On executing an exception return operation in Undefined mode SPSR_und.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

J, bit [24]

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]

**When FEAT_SBS is implemented:**

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Undefined mode, and copied to PSTATE.SSBS on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

PAN, bit [22]

**When FEAT_PAN is implemented:**

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Undefined mode, and copied to PSTATE.PAN on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.
DIT, bit [21]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Undefined mode, and copied to PSTATE.DIT on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Undefined mode, and copied to PSTATE.IL on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Undefined mode, and copied to PSTATE.GE on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Undefined mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Undefined mode.

SPSR_und.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to Undefined mode, and copied to PSTATE.E on executing an exception return operation in Undefined mode.

If the implementation does not support big-endian operation, SPSR_und.E is RES0. If the implementation does not support little-endian operation, SPSR_und.E is RES1. On executing an exception return operation in Undefined mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_und.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_und.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Undefined mode, and copied to PSTATE.A on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Undefined mode, and copied to PSTATE.I on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Undefined mode, and copied to PSTATE.F on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Undefined mode, and copied to PSTATE.T on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Undefined mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Undefined mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined</td>
</tr>
<tr>
<td>0b11111</td>
<td>System</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_und.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Undefined mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_und

Accesses to this register use the following encodings:

MRS <Xt>, SPSR_und

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return SPSR_und;
elsif PSTATE.EL == EL3 then
    return SPSR_und;

MSR SPSR_und, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0100</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    SPSR_und = X[t];
elsif PSTATE.EL == EL3 then
    SPSR_und = X[t];
SSBS, Speculative Store Bypass Safe

The SSBS characteristics are:

**Purpose**

Allows access to the Speculative Store Bypass Safe bit.

**Configuration**

This register is present only when FEAT_SSBS is implemented. Otherwise, direct accesses to SSBS are **UNDEFINED**.

**Attributes**

SSBS is a 64-bit register.

**Field descriptions**

The SSBS bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     | RES0 |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | RES0 |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**Bits [63:13]**

Reserved, RES0.

**SSBS, bit [12]**

Speculative Store Bypass Safe.

Prohibits speculative loads or stores which might practically allow a cache timing side channel.

A cache timing side channel might be exploited where a load or store uses an address that is derived from a register that is being loaded from memory using a load instruction speculatively read from a memory location. If PSTATE.SSBS is enabled, the address derived from the load instruction might be from earlier in the coherence order than the latest store to that memory location with the same virtual address.

<table>
<thead>
<tr>
<th>SSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hardware is not permitted to load or store speculatively, in a manner that could practically give rise to a cache timing side channel, using an address derived from a register value that has been loaded from memory using a load instruction (L) that speculatively reads an entry from earlier in the coherence order from that location being loaded from than the entry generated by the latest store (S) to that location using the same virtual address as L.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hardware is permitted to load or store speculatively, in a manner that could practically give rise to a cache timing side channel, using an address derived from a register value that has been loaded from memory using a load instruction (L) that speculatively reads an entry from earlier in the coherence order from that location being loaded from than the entry generated by the latest store (S) to that location using the same virtual address as L.</td>
</tr>
</tbody>
</table>

The value of this bit is set to the value in the SCTLR_ELx.DSSBS field on taking an exception to ELx.
On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

**Bits [11:0]**

Reserved, RES0.

**Accessing the SSBS**

Accesses to this register use the following encodings:

**MRS <Xt>, SSBS**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    return Zeros(51):PSTATE.SSBS:Zeros(12);
elsif PSTATE.EL == EL1 then
    return Zeros(51):PSTATE.SSBS:Zeros(12);
elsif PSTATE.EL == EL2 then
    return Zeros(51):PSTATE.SSBS:Zeros(12);
elsif PSTATE.EL == EL3 then
    return Zeros(51):PSTATE.SSBS:Zeros(12);

**MSR SSBS, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    PSTATE.SSBS = X[t]<12>;
elsif PSTATE.EL == EL1 then
    PSTATE.SSBS = X[t]<12>;
elsif PSTATE.EL == EL2 then
    PSTATE.SSBS = X[t]<12>;
elsif PSTATE.EL == EL3 then
    PSTATE.SSBS = X[t]<12>;

**MSR SSBS, #<imm>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

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TCO, Tag Check Override

The TCO characteristics are:

**Purpose**

When FEAT_MTE is implemented, this register allows tag checks to be disabled globally.

**Configuration**

This register is present only when FEAT_MTE is implemented. Otherwise, direct accesses to TCO are UNDEFINED.

**Attributes**

TCO is a 64-bit register.

**Field descriptions**

The TCO bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>TCO</td>
</tr>
<tr>
<td>24-0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:26]**

Reserved, RES0.

**TCO, bit [25]**

Allows memory tag checks to be globally disabled.

<table>
<thead>
<tr>
<th>TCO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Loads and Stores are not affected by this control.</td>
</tr>
<tr>
<td>0b1</td>
<td>Loads and Stores are unchecked.</td>
</tr>
</tbody>
</table>

**Bits [24:0]**

Reserved, RES0.

**Accessing the TCO**

For details on the operation of the MSR (immediate) accessor, see MSR (immediate).

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    return Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL1 then
    return Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL2 then
    return Zeros(38):PSTATE.TCO:Zeros(25);
elsif PSTATE.EL == EL3 then
    return Zeros(38):PSTATE.TCO:Zeros(25);

MSR TCO, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b11</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    PSTATE.TCO = X[t]<25>;
elsif PSTATE.EL == EL1 then
    PSTATE.TCO = X[t]<25>;
elsif PSTATE.EL == EL2 then
    PSTATE.TCO = X[t]<25>;
elsif PSTATE.EL == EL3 then
    PSTATE.TCO = X[t]<25>;

MSR TCO, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

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TCR_EL1, Translation Control Register (EL1)

The TCR_EL1 characteristics are:

**Purpose**

The control register for stage 1 of the EL1&0 translation regime.

**Configuration**

AArch64 System register TCR_EL1 bits [31:0] are architecturally mapped to AArch32 System register TTBCR[31:0].

AArch64 System register TCR_EL1 bits [63:32] are architecturally mapped to AArch32 System register TTBCR2[31:0].

**Attributes**

TCR_EL1 is a 64-bit register.

**Field descriptions**

The TCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>DS</td>
<td>TCMA1</td>
<td>TCMA0</td>
<td>E0PD1</td>
<td>E0PD0</td>
<td>NFDO</td>
<td>TFID1</td>
<td>TBID0</td>
<td>HWU162</td>
<td>HWU161</td>
<td>HWU160</td>
<td>HWU159</td>
<td>HWU062</td>
<td>HWU061</td>
<td>HWU060</td>
<td>HWU059</td>
<td>HPD1</td>
<td>HPD0</td>
</tr>
<tr>
<td>TG1</td>
<td>SH1</td>
<td>ORGN1</td>
<td>IRGN1</td>
<td>EPD1</td>
<td>A1</td>
<td>T1SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
<td>T0SZ</td>
</tr>
<tr>
<td>31302928</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
</tr>
</tbody>
</table>

Any of the bits in TCR_EL1, other than the A1 bit and the EPDx bits when they have the value 1, are permitted to be cached in a TLB.

**Bits [63:60]**

Reserved, RES0.

**DS, bit [59]**

When FEAT_LPA2 is implemented:

This field affects 52-bit output addressing when using 4KB and 16KB translation granules in stage 1 of the EL1&0 translation regime.
### DS

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits[49:48] of translation descriptors are RES0. Bits[9:8] in block and page descriptors encode shareability information in the SH[1:0] field. Bits[9:8] in table descriptors are ignored by hardware. The minimum value of the TCR_EL1.{T0SZ, T1SZ} fields is 16. Any memory access using a smaller value generates a stage 1 level 0 translation table fault. Output address[51:48] is 0b0000.</td>
</tr>
</tbody>
</table>
| 0b1  | Bits[49:48] of translation descriptors hold output address[49:48]. Bits[9:8] of translation table descriptors hold output address[51:50]. The shareability information of block and page descriptors for cacheable locations is determined by:

- TCR_EL1.SH0 if the VA is translated using tables pointed to by TTBR0_EL1.
- TCR_EL1.SH1 if the VA is translated using tables pointed to by TTBR1_EL1.

The minimum value of the TCR_EL1.{T0SZ, T1SZ} fields is 12. Any memory access using a smaller value generates a stage 1 level 0 translation table fault. All calculations of the stage 1 base address are modified for tables of fewer than 8 entries so that the table is aligned to 64 bytes. Bits[5:2] of TTBR0_EL1 or TTBR1_EL1 are used to hold bits[51:48] of the output address in all cases. |

**Note**
As FEAT_LVA must be implemented if TCR_EL1.DS == 1, the minimum value of the TCR_EL1.{T0SZ, T1SZ} fields is 12, as determined by that extension.

For the TLBI Range instructions affecting VA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as 0b0000. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as 0b00.

**Note**
This forces alignment of the ranges used by the TLBI range instructions.

This field is RES0 for a 64KB translation granule.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

### TCMA1, bit [58]

**When FEAT_MTE is implemented:**

Controls the generation of Unchecked accesses at EL1, and at EL0 if HCR_EL2.{E2H, TGE}!={1,1}, when address[59:55] = 0b111111.

<table>
<thead>
<tr>
<th>TCMA1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses at EL1 or EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses at EL1 and EL0 are Unchecked.</td>
</tr>
</tbody>
</table>

**Note**
Software may change this control bit on a context switch.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**TCMA0, bit [57]**

*When FEAT_MTE is implemented:*

Controls the generation of Unchecked accesses at EL1, and at EL0 if HCR_EL2.E2H,TGE!=\{1,1\}, when address[59:55] = 0b00000.

<table>
<thead>
<tr>
<th>TCMA0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses at EL1 or EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses at EL1 and EL0 are Unchecked.</td>
</tr>
</tbody>
</table>

**Note**

Software may change this control bit on a context switch.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**E0PD1, bit [56]**

*When FEAT_E0PD is implemented:*

Faulting control for Unprivileged access to any address translated by TTBR1_EL1.

<table>
<thead>
<tr>
<th>E0PD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unprivileged access to any address translated by TTBR1_EL1 will not generate a fault by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>Unprivileged access to any address translated by TTBR1_EL1 will generate a level 0 translation fault.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**E0PD0, bit [55]**

*When FEAT_E0PD is implemented:*

Faulting control for Unprivileged access to any address translated by TTBR0_EL1.

<table>
<thead>
<tr>
<th>E0PD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unprivileged access to any address translated by TTBR0_EL1 will not generate a fault by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>Unprivileged access to any address translated by TTBR0_EL1 will generate a level 0 translation fault.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
NFD1, bit [54]

When FEAT_SVE is implemented:

Non-fault translation table walk disable for stage 1 translations using TTBR1_EL1.

This bit controls whether to perform a stage 1 translation table walk in response to a non-fault unprivileged access for a virtual address that is translated using TTBR1_EL1.

If SVE is implemented, the affected access types include:

- All accesses due to an SVE non-fault contiguous load instruction.
- Accesses due to an SVE first-fault gather load instruction that are not for the First active element. Accesses due to an SVE first-fault contiguous load instruction are not affected.
- Accesses due to prefetch instructions might be affected, but the effect is not architecturally visible.

For more information, see 'The Scalable Vector Extension (SVE)'.

<table>
<thead>
<tr>
<th>NFD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not disable stage 1 translation table walks using TTBR1_EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on a virtual address that is translated using TTBR1_EL1 due to the specified access types causes the access to fail without taking an exception. No stage 1 translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

NFD0, bit [53]

When FEAT_SVE is implemented:

Non-fault translation table walk disable for stage 1 translations using TTBR0_EL1.

This bit controls whether to perform a stage 1 translation table walk in response to a non-fault unprivileged access for a virtual address that is translated using TTBR0_EL1.

If SVE is implemented, the affected access types include:

- All accesses due to an SVE non-fault contiguous load instruction.
- Accesses due to an SVE first-fault gather load instruction that are not for the First active element. Accesses due to an SVE first-fault contiguous load instruction are not affected.
- Accesses due to prefetch instructions might be affected, but the effect is not architecturally visible.

For more information, see 'The Scalable Vector Extension (SVE)'.

<table>
<thead>
<tr>
<th>NFD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not disable stage 1 translation table walks using TTBR0_EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on a virtual address that is translated using TTBR0_EL1 due to the specified access types causes the access to fail without taking an exception. No stage 1 translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TBID1, bit [52]
When FEAT_PAuth is implemented:

Controls the use of the top byte of instruction addresses for address matching.

For the purpose of this field, all cache maintenance and address translation instructions that perform address translation are treated as data accesses.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBID1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL1.TBI1 applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL1.TBI1 applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR1_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TBID0, bit [51]

When FEAT_PAuth is implemented:

Controls the use of the top byte of instruction addresses for address matching.

For the purpose of this field, all cache maintenance and address translation instructions that perform address translation are treated as data accesses.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBID0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL1.TBI0 applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL1.TBI0 applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR0_EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU162, bit [50]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using TTBR1_EL1.

<table>
<thead>
<tr>
<th>HWU162</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1_EL1, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1_EL1, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**HWU161, bit [49]**

**When FEAT_HPDS2 is implemented:**

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using **TTBR1_EL1**.

<table>
<thead>
<tr>
<th>HWU161</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using <strong>TTBR1_EL1</strong>, bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using <strong>TTBR1_EL1</strong>, bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU160, bit [48]**

**When FEAT_HPDS2 is implemented:**

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using **TTBR1_EL1**.

<table>
<thead>
<tr>
<th>HWU160</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using <strong>TTBR1_EL1</strong>, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using <strong>TTBR1_EL1</strong>, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU159, bit [47]**

**When FEAT_HPDS2 is implemented:**

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using **TTBR1_EL1**.
HWU159, Meaning

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1_EL1, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1_EL1, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU062, bit [46]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU062</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU061, bit [45]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU061</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL1.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
HWU060, bit [44]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates implementation defined hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU060</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an implementation defined purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an implementation defined purpose if the value of TCR_EL1.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD0 is 0.

On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

HWU059, bit [43]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates implementation defined hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU059</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an implementation defined purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an implementation defined purpose if the value of TCR_EL1.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL1.HPD0 is 0.

On a Warm reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

HPD1, bit [42]

When FEAT_HPDS is implemented:

Hierarchical Permission Disable. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBR1_EL1.

<table>
<thead>
<tr>
<th>HPD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally unknown value.
Otherwise:

Reserved, RES0.

**HPD0, bit [41]**

When FEAT_HPDS is implemented:

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBR0_EL1.

<table>
<thead>
<tr>
<th>HPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**HD, bit [40]**

When FEAT_HAFDBS is implemented:

Hardware management of dirty state in stage 1 translations from EL0 and EL1.

<table>
<thead>
<tr>
<th>HD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 hardware management of dirty state disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 hardware management of dirty state enabled, only if the HA bit is also set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**HA, bit [39]**

When FEAT_HAFDBS is implemented:

Hardware Access flag update in stage 1 translations from EL0 and EL1.

<table>
<thead>
<tr>
<th>HA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 Access flag update disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 Access flag update enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**TBI1, bit [38]**

Top Byte ignored. Indicates whether the top byte of an address is used for address match for the TTBR1_EL1 region, or ignored and used for tagged addresses.
TBI1, Top Byte Used in the Address Calculation

<table>
<thead>
<tr>
<th>TBI1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL0 and EL1 using AArch64 where the address would be translated by tables pointed to by TTBR1_EL1. It has an effect whether the EL1&0 translation regime is enabled or not.

If FEAT_PAuth is implemented and TCR_EL1.TBID1 is 1, then this field only applies to Data accesses.

Otherwise, if the value of TBI1 is 1 and bit [55] of the target address to be stored to the PC is 1, then bits[63:56] of that target address are also set to 1 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL0 or EL1.
- An exception taken to EL1.
- An exception return to EL0 or EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TBI0, Top Byte Ignored

<table>
<thead>
<tr>
<th>TBI0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL0 and EL1 using AArch64 where the address would be translated by tables pointed to by TTBR0_EL1. It has an effect whether the EL1&0 translation regime is enabled or not.

If FEAT_PAuth is implemented and TCR_EL1.TBID0 is 1, then this field only applies to Data accesses.

Otherwise, if the value of TBI0 is 1 and bit [55] of the target address to be stored to the PC is 0, then bits[63:56] of that target address are also set to 0 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL0 or EL1.
- An exception taken to EL1.
- An exception return to EL0 or EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

AS, ASID Size

<table>
<thead>
<tr>
<th>AS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>8 bit - the upper 8 bits of TTBR0_EL1 and TTBR1_EL1 are ignored by hardware for every purpose except reading back the register, and are treated as if they are all zeros for when used for allocation and matching entries in the TLB.</td>
</tr>
<tr>
<td>0b1</td>
<td>16 bit - the upper 16 bits of TTBR0_EL1 and TTBR1_EL1 are used for allocation and matching in the TLB.</td>
</tr>
</tbody>
</table>

If the implementation has only 8 bits of ASID, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [35]

Reserved, RES0.

IPS, Intermediate Physical Address Size
<table>
<thead>
<tr>
<th>IPS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>32 bits, 4GB.</td>
</tr>
<tr>
<td>0b001</td>
<td>36 bits, 64GB.</td>
</tr>
<tr>
<td>0b010</td>
<td>40 bits, 1TB.</td>
</tr>
<tr>
<td>0b011</td>
<td>42 bits, 4TB.</td>
</tr>
<tr>
<td>0b100</td>
<td>44 bits, 16TB.</td>
</tr>
<tr>
<td>0b101</td>
<td>48 bits, 256TB.</td>
</tr>
<tr>
<td>0b110</td>
<td>52 bits, 4PB.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The reserved values behave in the same way as the 0b101 or 0b110 encoding, but software must not rely on this property as the behavior of the reserved values might change in a future revision of the architecture.

If the translation granule is not 64KB and FEAT_LPA2 is not implemented, the value 0b110 is treated as reserved.

It is **IMPLEMENTATION DEFINED** whether an implementation that does not implement FEAT_LPA supports setting the value of 0b110 for the 64KB translation granule size or whether setting this value behaves as the 0b101 encoding.

In an implementation that supports 52-bit PAs, if the value of this field is not 0b110 or a value treated as 0b110, then bits[51:48] of every translation table base address for the stage of translation controlled by TCR_EL1 are 0b0000.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### TG1, bits [31:30]

Granule size for the **TTBR1_EL1**.

<table>
<thead>
<tr>
<th>TG1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>16KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b11</td>
<td>64KB.</td>
</tr>
</tbody>
</table>

Other values are reserved.

If the value is programmed to either a reserved value or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an **IMPLEMENTATION DEFINED** choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is **IMPLEMENTATION DEFINED** whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### SH1, bits [29:28]

Shareability attribute for memory associated with translation table walks using **TTBR1_EL1**.

<table>
<thead>
<tr>
<th>SH1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is **CONSTRAINED UNPREDICTABLE**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### ORGN1, bits [27:26]

Outer cacheability attribute for memory associated with translation table walks using **TTBR1_EL1**.
### ORGN1

<table>
<thead>
<tr>
<th>Meaning</th>
<th>ORGN1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### IRGN1, bits [25:24]

Inner cacheability attribute for memory associated with translation table walks using **TTBR1_EL1**.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>IRGN1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EPD1, bit [23]

Translation table walk disable for translations using **TTBR1_EL1**. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using **TTBR1_EL1**. The encoding of this bit is:

<table>
<thead>
<tr>
<th>Meaning</th>
<th>EPD1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using <strong>TTBR1_EL1</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using <strong>TTBR1_EL1</strong> generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### A1, bit [22]

Selects whether **TTBR0_EL1** or **TTBR1_EL1** defines the ASID. The encoding of this bit is:

<table>
<thead>
<tr>
<th>Meaning</th>
<th>A1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>TTBR0_EL1</strong> ASID defines the ASID.</td>
<td>0b0</td>
</tr>
<tr>
<td><strong>TTBR1_EL1</strong> ASID defines the ASID.</td>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### T1SZ, bits [21:16]

The size offset of the memory region addressed by **TTBR1_EL1**. The region size is $2^{(64-T1SZ)}$ bytes.

The maximum and minimum possible values for T1SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TG0, bits [15:14]**

Granule size for the TTBR0_EL1.

<table>
<thead>
<tr>
<th>TG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB</td>
</tr>
<tr>
<td>0b01</td>
<td>64KB</td>
</tr>
<tr>
<td>0b10</td>
<td>16KB</td>
</tr>
</tbody>
</table>

Other values are reserved.

If the value is programmed to either a reserved value or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an IMPLEMENTATION DEFINED choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is IMPLEMENTATION DEFINED whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SH0, bits [13:12]**

Shareability attribute for memory associated with translation table walks using TTBR0_EL1.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ORGN0, bits [11:10]**

Outer cacheability attribute for memory associated with translation table walks using TTBR0_EL1.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IRGN0, bits [9:8]**

Inner cacheability attribute for memory associated with translation table walks using TTBR0_EL1.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.


**EPD0, bit [7]**

Translation table walk disable for translations using TTBRO_EL1. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBRO_EL1. The encoding of this bit is:

<table>
<thead>
<tr>
<th>EPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBRO_EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBRO_EL1 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [6]**

Reserved, RES0.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by TTBRO_EL1. The region size is $2^{(64-T0SZ)}$ bytes.

The maximum and minimum possible values for T0SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

*Note*

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TCR_EL1**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic TCR_EL1 or TCR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, TCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x120] = X[t];
    else
        return TCR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TCR_EL2 = X[t];
    else
        TCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    TCR_EL1 = X[t];
endif

MSR TCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x120] = X[t];
    else
        TCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TCR_EL2 = X[t];
    else
        TCR_EL1 = X[t];
    end
elsif PSTATE.EL == EL3 then
    TCR_EL1 = X[t];
endif

MRS <Xt>, TCR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x120];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return TCR_EL1;
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return TCR_EL1;
    else
        UNDEFINED;
    end if;
end if;

MSR TCR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x120] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TCR_EL1 = X[t];
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        TCR_EL1 = X[t];
    else
        UNDEFINED;
    end if;
TCR_EL2, Translation Control Register (EL2)

The TCR_EL2 characteristics are:

**Purpose**

The control register for stage 1 of the EL2, or EL2&0, translation regime:

- When the Effective value of HCR_EL2.E2H is 0, this register controls stage 1 of the EL2 translation regime, that supports a single VA range, translated using TTBR0_EL2.
- When the value of HCR_EL2.E2H is 1, this register controls stage 1 of the EL2&0 translation regime, that supports both:
  - A lower VA range, translated using TTBR0_EL2.
  - A higher VA range, translated using TTBR1_EL2.

**Configuration**

AArch64 System register TCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HTC[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

TCR_EL2 is a 64-bit register.

**Field descriptions**

The TCR_EL2 bit assignments are:

**When HCR_EL2.E2H == 0:**

Any of the bits in TCR_EL2, other than the A1 bit and the EPDx bits when they have the value 1, are permitted to be cached in a TLB.

**Bits [63:33]**

Reserved, RES0.

**DS, bit [32]**

**When FEAT_LPA2 is implemented:**

This field affects 52-bit output addressing when using 4KB and 16KB translation granules in stage 1 of the EL2 translation regime.
Bits[49:48] of translation descriptors are res0. Bits[9:8] in block and page descriptors encode shareability information in the SH[1:0] field. Bits[9:8] in table descriptors are ignored by hardware. The minimum value of TCR_EL2.T0SZ is 16. Any memory access using a smaller value generates a stage 1 level 0 translation table fault. Output address[51:48] is 0b0000. Bits[49:48] of translation descriptors hold output address[49:48]. Bits[9:8] of translation table descriptors hold output address[51:50]. The shareability information of block and page descriptors for cacheable locations is determined by TCR_EL2.SH0. The minimum value of TCR_EL2.T0SZ is 12. Any memory access using a smaller value generates a stage 1 level 0 translation table fault. All calculations of the stage 1 base address are modified for tables of fewer than 8 entries so that the table is aligned to 64 bytes. Bits[5:2] of TTBRO_EL2 are used to hold bits[51:48] of the output address in all cases.

**Note**
As FEAT_LVA must be implemented if TCR_EL2.DS == 1, the minimum value of the TCR_EL2.T0SZ field is 12, as determined by that extension.

For the TLBI Range instructions affecting VA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as 0b0000. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as 0b00.

**Note**
This forces alignment of the ranges used by the TLBI range instructions.

This field is res0 for a 64KB translation granule.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, res0.

**Bit [31]**

Reserved, res1.

**TCMA, bit [30]**

When FEAT_MTE is implemented:

Controls the generation of Unchecked accesses at EL2 when address [59:56] = 0b0000.

<table>
<thead>
<tr>
<th>TCMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses are Unchecked.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**TBID, bit [29]**

*When FEAT_PAuth is implemented:*

Controls the use of the top byte of instruction addresses for address matching.

For the purpose of this field, all cache maintenance and address translation instructions that perform address translation are treated as data accesses.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL2.TBI applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL2.TBI applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR0_EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU62, bit [28]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU62</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU61, bit [27]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU61</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD is 1.</td>
</tr>
</tbody>
</table>
The Effective value of this field is 0 if the value of TCR_EL2.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU60, bit [26]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU60</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU59, bit [25]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU59</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HPD, bit [24]**

When FEAT_HPDS is implemented:

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBR0_EL2.
<table>
<thead>
<tr>
<th>HPD</th>
<th>Meaning</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
<td>In this case, bit[61] (APTable[0]) and bit[59] (PXNTable) of the next level descriptor attributes are required to be ignored by the PE and are no longer reserved, allowing them to be used by software.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
<td></td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bit [23]**

Reserved, RES1.

**HD, bit [22]**

*When FEAT_HAFDBS is implemented:*

Hardware management of dirty state in stage 1 translations from EL2.

<table>
<thead>
<tr>
<th>HD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 hardware management of dirty state disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 hardware management of dirty state enabled, only if the HA bit is also set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**HA, bit [21]**

*When FEAT_HAFDBS is implemented:*

Hardware Access flag update in stage 1 translations from EL2.

<table>
<thead>
<tr>
<th>HA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 Access flag update disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 Access flag update enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**TBI, bit [20]**

Top Byte Ignored. Indicates whether the top byte of an address is used for address match for the **TTBR0_EL2** region, or ignored and used for tagged addresses.
For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL2 using AArch64 where the address would be translated by tables pointed to by TTBR0_EL2. It has an effect whether the EL2, or EL2&0, translation regime is enabled or not.

If FEAT_PAAuth is implemented and TCR_EL2.TBID is 1, then this field only applies to Data accesses.

If the value of TBI is 1, then bits[63:56] of that target address are also set to 0 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL2.
- An exception taken to EL2.
- An exception return to EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [19]**

Reserved, RES0.

**PS, bits [18:16]**

Physical Address Size.

<table>
<thead>
<tr>
<th>PS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>32 bits, 4GB.</td>
</tr>
<tr>
<td>0b01</td>
<td>36 bits, 64GB.</td>
</tr>
<tr>
<td>0b10</td>
<td>40 bits, 1TB.</td>
</tr>
<tr>
<td>0b11</td>
<td>42 bits, 4TB.</td>
</tr>
<tr>
<td>0b100</td>
<td>44 bits, 16TB.</td>
</tr>
<tr>
<td>0b101</td>
<td>48 bits, 256TB.</td>
</tr>
<tr>
<td>0b110</td>
<td>52 bits, 4PB.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The reserved values behave in the same way as the 0b101 or 0b110 encoding, but software must not rely on this property as the behavior of the reserved values might change in a future revision of the architecture.

If the translation granule is not 64KB and FEAT_LPA2 is not implemented, the value 0b110 is treated as reserved.

It is IMPLEMENTATION DEFINED whether an implementation that does not implement FEAT_LPA supports setting the value of 0b110 for the 64KB translation granule size or whether setting this value behaves as the 0b101 encoding.

In an implementation that supports 52-bit PAs, if the value of this field is not 0b110 or a value treated as 0b110, then bits[51:48] of every translation table base address for the stage of translation controlled by TCR_EL2 are 0b0000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TG0, bits [15:14]**

Granule size for the TTBR0_EL2.

<table>
<thead>
<tr>
<th>TG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>16KB.</td>
</tr>
</tbody>
</table>

Other values are reserved.

If the value is programmed to either a reserved value or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an IMPLEMENTATION DEFINED choice of the sizes that has been implemented for all purposes other than the value read back from this register.
It is **IMPLEMENTATION DEFINED** whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**SH0, bits [13:12]**

Shareability attribute for memory associated with translation table walks using TTBR0_EL2.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is **CONSTRAINED UNPREDICTABLE**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ORGN0, bits [11:10]**

Outer cacheability attribute for memory associated with translation table walks using TTBR0_EL2.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IRGN0, bits [9:8]**

Inner cacheability attribute for memory associated with translation table walks using TTBR0_EL2.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [7:6]**

Reserved, RES0.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by TTBR0_EL2. The region size is \(2^{(64-T0SZ)}\) bytes.

The maximum and minimum possible values for T0SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.
For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**When FEAT_VHE is implemented and HCR_EL2.E2H == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>DS</td>
<td>Reserved</td>
</tr>
<tr>
<td>59</td>
<td>TCMA1</td>
<td>Translation Control Register (EL2)</td>
</tr>
<tr>
<td>58</td>
<td>TCMA0</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>E0PD1</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>E0PD0</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>NF0</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td>NF1</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>TBID1</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>TBID0</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td>HWU161</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td>HWU160</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td>HWU159</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td>HWU158</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td>HWU157</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>HWU156</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>AS</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td>IPS</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td>TG1</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td>SH1</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td>ORGN1</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td>IRGN1</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>EPD1</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>A1</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>T1SZ</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>TG0</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>T0SZ</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>21</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>19</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>17</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>13</td>
<td></td>
</tr>
</tbody>
</table>

This view of the register is only valid from Armv8.1 when HCR_EL2.E2H is 1.

Any of the bits in TCR_EL2 are permitted to be cached in a TLB.

### Bits [63:60]

Reserved, RES0.

### DS, bit [59]

**When FEAT_LPA2 is implemented:**

This field affects 52-bit output addressing when using 4KB and 16KB translation granules in stage 1 of the EL2&0 translation regime.
Bits[49:48] of translation descriptors are \texttt{RES0}.


The minimum value of the TCR\_EL2.\{T0SZ, T1SZ\} fields is 16. Any memory access using a smaller value generates a stage 1 level 0 translation table fault.

Output address[51:48] is \texttt{0b0000}.


The shareability information of block and page descriptors for cacheable locations is determined by:

- TCR\_EL2.SH0 if the VA is an address that is translated using tables pointed to by TTBR\_EL2.
- TCR\_EL2.SH1 if the VA is an address that is translated using tables pointed to by TTBR\_EL2.

The minimum value of the TCR\_EL2.\{T0SZ, T1SZ\} fields is 12. Any memory access using a smaller value generates a stage 1 level 0 translation table fault.

All calculations of the stage 1 base address are modified for tables of fewer than 16 entries so that the table is aligned to 64 bytes. Bits[5:2] of TTBR\_EL2 or TTBR\_EL2 are used to hold bits[51:48] of the output address in all cases.

\textbf{Note}
As FEAT\_LVA must be implemented if TCR\_EL2.DS == 1, the minimum value of the TCR\_EL2.\{T0SZ, T1SZ\} fields is 12, as determined by that extension.

For the TLBI Range instructions affecting VA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as \texttt{0b0000}. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as \texttt{0b00}.

\textbf{Note}
This forces alignment of the ranges used by the TLBI range instructions.

This field is \texttt{RES0} for a 64KB translation granule.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{Otherwise:}

Reserved, \texttt{RES0}.

\textbf{TCMA1, bit [58]}

\textbf{When FEAT\_MTE is implemented:}

Controls the generation of Unchecked accesses at EL2, and at EL0 if HCR\_EL2.TGE=1, when address[59:55] = \texttt{0b11111}.

<table>
<thead>
<tr>
<th>TCMA1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses at EL2 or EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses are Unchecked.</td>
</tr>
</tbody>
</table>

\textbf{Note}
Software may change this control bit on a context switch.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.
Otherwise:
Reserved, RES0.

**TCMA0, bit [57]**

*When FEAT_MTE is implemented:*

Controls the generation of Unchecked accesses at EL2, and at EL0 if \( \text{HCR}_{EL2}.\text{TGE}=1 \), when \( \text{address}[59:55] = 0b00000 \).

<table>
<thead>
<tr>
<th>TCMA0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses at EL2 or EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses are Unchecked.</td>
</tr>
</tbody>
</table>

**Note**

Software may change this control bit on a context switch.

On a Warm reset, this field resets to an architecturally \text{UNKNOWN} value.

Otherwise:
Reserved, RES0.

**E0PD1, bit [56]**

*When FEAT_E0PD is implemented:*

Faulting control for Unprivileged access to any address translated by \( \text{TTBR}_{1\_EL2} \).

<table>
<thead>
<tr>
<th>E0PD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unprivileged access to any address translated by ( \text{TTBR}_{1_EL2} ) will not generate a fault by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>Unprivileged access to any address translated by ( \text{TTBR}_{1_EL2} ) will generate a level 0 translation fault.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally \text{UNKNOWN} value.

Otherwise:
Reserved, RES0.

**E0PD0, bit [55]**

*When FEAT_E0PD is implemented:*

Faulting control for Unprivileged access to any address translated by \( \text{TTBR}_{0\_EL2} \).

<table>
<thead>
<tr>
<th>E0PD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unprivileged access to any address translated by ( \text{TTBR}_{0_EL2} ) will not generate a fault by this mechanism.</td>
</tr>
<tr>
<td>0b1</td>
<td>Unprivileged access to any address translated by ( \text{TTBR}_{0_EL2} ) will generate a level 0 translation fault.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally \text{UNKNOWN} value.

Otherwise:
Reserved, RES0.
NFD1, bit [54]

When FEAT_SVE is implemented:

Non-fault translation table walk disable for stage 1 translations using TTBR1_EL2.

This bit controls whether to perform a stage 1 translation table walk in response to a non-fault unprivileged access for a virtual address that is translated using TTBR1_EL2.

If SVE is implemented, the affected access types include:

- All accesses due to an SVE non-fault contiguous load instruction.
- Accesses due to an SVE first-fault gather load instruction that are not for the First active element. Accesses due to an SVE first-fault contiguous load instruction are not affected.
- Accesses due to prefetch instructions might be affected, but the effect is not architecturally visible.

For more information, see 'The Scalable Vector Extension (SVE)'.

<table>
<thead>
<tr>
<th>NFD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not disable stage 1 translation table walks using TTBR1_EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on a virtual address that is translated using TTBR1_EL2 due to the specified access types causes the access to fail without taking an exception. No stage 1 translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

NFD0, bit [53]

When FEAT_SVE is implemented:

Non-fault translation table walk disable for stage 1 translations using TTBR0_EL2.

This bit controls whether to perform a stage 1 translation table walk in response to a non-fault unprivileged access for a virtual address that is translated using TTBR0_EL2.

If SVE is implemented, the affected access types include:

- All accesses due to an SVE non-fault contiguous load instruction.
- Accesses due to an SVE first-fault gather load instruction that are not for the First active element. Accesses due to an SVE first-fault contiguous load instruction are not affected.
- Accesses due to prefetch instructions might be affected, but the effect is not architecturally visible.

For more information, see 'The Scalable Vector Extension (SVE)'.

<table>
<thead>
<tr>
<th>NFD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not disable stage 1 translation table walks using TTBR0_EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on a virtual address that is translated using TTBR0_EL2 due to the specified access types causes the access to fail without taking an exception. No stage 1 translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

TBID1, bit [52]
When FEAT_PAuth is implemented:

Controls the use of the top byte of instruction addresses for address matching.

For the purpose of this field, all cache maintenance and address translation instructions that perform address translation are treated as data accesses.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBID1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL2.TBI1 applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL2.TBI1 applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR1_EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TBID0, bit [51]**

When FEAT_PAuth is implemented:

Controls the use of the top byte of instruction addresses for address matching.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBID0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL2.TBI0 applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL2.TBI0 applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR0_EL2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU162, bit [50]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using TTBR1_EL2.

<table>
<thead>
<tr>
<th>HWU162</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1_EL2, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1_EL2, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**HWU161, bit [49]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using TTBRI_EL2.

<table>
<thead>
<tr>
<th>HWU161</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBRI_EL2, bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBRI_EL2, bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU160, bit [48]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using TTBRI_EL2.

<table>
<thead>
<tr>
<th>HWU160</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBRI_EL2, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBRI_EL2, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU159, bit [47]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using TTBRI_EL2.
Meaning

| 0b0 | For translations using `TTBR1_EL2`, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose. |
| 0b1 | For translations using `TTBR1_EL2`, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD1 is 1. |

The Effective value of this field is 0 if the value of TCR_EL2.HPD1 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU062, bit [46]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using `TTBR0_EL1`.

Meaning

| 0b0 | For translations using `TTBR0_EL1`, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose. |
| 0b1 | For translations using `TTBR0_EL1`, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD0 is 1. |

The Effective value of this field is 0 if the value of TCR_EL2.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU061, bit [45]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using `TTBR0_EL1`.

Meaning

| 0b0 | For translations using `TTBR0_EL1`, bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose. |
| 0b1 | For translations using `TTBR0_EL1`, bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD0 is 1. |

The Effective value of this field is 0 if the value of TCR_EL2.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
HWU060, bit [44]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU060</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU059, bit [43]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using TTBR0_EL1.

<table>
<thead>
<tr>
<th>HWU059</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0_EL1, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0_EL1, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL2.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL2.HPD0 is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HPD1, bit [42]

When FEAT_HPDS is implemented:

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBR1_EL2.

<table>
<thead>
<tr>
<th>HPD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**HPD0, bit [41]**

*When FEAT_HPDS is implemented:*

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBRO_EL2.

<table>
<thead>
<tr>
<th>HPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HD, bit [40]**

*When FEAT_HAFDBS is implemented:*

Hardware management of dirty state in stage 1 translations from EL2.

<table>
<thead>
<tr>
<th>HD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 hardware management of dirty state disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 hardware management of dirty state enabled, only if the HA bit is also set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HA, bit [39]**

*When FEAT_HAFDBS is implemented:*

Hardware Access flag update in stage 1 translations from EL2.

<table>
<thead>
<tr>
<th>HA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 1 Access flag update disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 1 Access flag update enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**TBI1, bit [38]**

Top Byte Ignored. Indicates whether the top byte of an address is used for address match for the TTBRI_EL2 region, or ignored and used for tagged addresses.
For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBI1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL0 and EL2 using AArch64 where the address would be translated by tables pointed to by TTBR1_EL2. It has an effect whether the EL2, or EL2&0, translation regime is enabled or not.

If FEAT_PAuth is implemented and TCR_EL2.TBID1 is 1, then this field only applies to Data accesses.

If the value of TBI1 is 1 and bit [55] of the target address to be stored to the PC is 1, then bits[63:56] of that target address are also set to 1 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL0 or EL1.
- An exception taken to EL1.
- An exception return to EL0 or EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

TBI0, bit [37]

Top Byte Ignored. Indicates whether the top byte of an address is used for address match for the TTBR0_EL2 region, or ignored and used for tagged addresses.

For more information, see 'Address tagging in AArch64 state'.

<table>
<thead>
<tr>
<th>TBI0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL0 and EL2 using AArch64 where the address would be translated by tables pointed to by TTBR0_EL2. It has an effect whether the EL2, or EL2&0, translation regime is enabled or not.

If FEAT_PAuth is implemented and TCR_EL2.TBID0 is 1, then this field only applies to Data accesses.

If the value of TBI0 is 1 and bit [55] of the target address to be stored to the PC is 0, then bits[63:56] of that target address are also set to 0 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL0 or EL1.
- An exception taken to EL1.
- An exception return to EL0 or EL1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

AS, bit [36]

ASID Size.

<table>
<thead>
<tr>
<th>AS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>8 bit - the upper 8 bits of TTBR0_EL2 and TTBR1_EL2 are ignored by hardware for every purpose except reading back the register, and are treated as if they are all zeros for when used for allocation and matching entries in the TLB.</td>
</tr>
<tr>
<td>0b1</td>
<td>16 bit - the upper 16 bits of TTBR0_EL2 and TTBR1_EL2 are used for allocation and matching in the TLB.</td>
</tr>
</tbody>
</table>

If the implementation has only 8 bits of ASID, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [35]

Reserved, RES0.
**IPS, bits [34:32]**

Intermediate Physical Address Size.

<table>
<thead>
<tr>
<th>IPS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>32 bits, 4GB.</td>
<td></td>
</tr>
<tr>
<td>0b001</td>
<td>36 bits, 64GB.</td>
<td></td>
</tr>
<tr>
<td>0b010</td>
<td>40 bits, 1TB.</td>
<td></td>
</tr>
<tr>
<td>0b011</td>
<td>42 bits, 4TB.</td>
<td></td>
</tr>
<tr>
<td>0b100</td>
<td>44 bits, 16TB.</td>
<td></td>
</tr>
<tr>
<td>0b101</td>
<td>48 bits, 256TB.</td>
<td></td>
</tr>
<tr>
<td>0b110</td>
<td>52 bits, 4PB.</td>
<td>When FEAT_LPA is implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

The reserved values behave in the same way as the 0b101 or 0b110 encoding, but software must not rely on this property as the behavior of the reserved values might change in a future revision of the architecture.

If the translation granule is not 64KB, the value 0b110 is treated as reserved.

It is implementation defined whether an implementation that does not implement FEAT_LPA supports setting the value of 0b110 for the 64KB translation granule size or whether setting this value behaves as the 0b101 encoding.

In an implementation that supports 52-bit PAs, if the value of this field is not 0b110 or a value treated as 0b110, then bits[51:48] of every translation table base address for the stage of translation controlled by TCR_EL2 are 0b0000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TG1, bits [31:30]**

Granule size for the **TTBR1_EL2**.

<table>
<thead>
<tr>
<th>TG1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>16KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b11</td>
<td>64KB.</td>
</tr>
</tbody>
</table>

Other values are reserved.

If the value is programmed to either a reserved value, or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an implementation defined choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is implementation defined whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SH1, bits [29:28]**

Shareability attribute for memory associated with translation table walks using **TTBR1_EL2**.

<table>
<thead>
<tr>
<th>SH1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is constrained unpredictable.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ORGN1, bits [27:26]**

Outer cacheability attribute for memory associated with translation table walks using **TTBR1_EL2**.
### ORGN1, Meaning

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### IRGN1, bits [25:24]

Inner cacheability attribute for memory associated with translation table walks using **TTBR1_EL2**.

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### EPD1, bit [23]

Translation table walk disable for translations using **TTBR1_EL2**. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using **TTBR1_EL2**. The encoding of this bit is:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using <strong>TTBR1_EL2</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using <strong>TTBR1_EL2</strong> generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### A1, bit [22]

Selects whether **TTBR0_EL2** or **TTBR1_EL2** defines the ASID. The encoding of this bit is:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>TTBR0_EL2</strong> ASID defines the ASID.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>TTBR1_EL2</strong> ASID defines the ASID.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### T1SZ, bits [21:16]

The size offset of the memory region addressed by **TTBR1_EL2**. The region size is $2^{(64-\text{T1SZ})}$ bytes.

The maximum and minimum possible values for T1SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.
On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.

\textbf{TG0, bits [15:14]}

Granule size for the \texttt{TTBR0_EL2}.

\begin{center}
\begin{tabular}{|c|c|}
\hline
\textbf{TG0} & \textbf{Meaning} \\
\hline
0b00 & 4KB. \\
0b01 & 64KB. \\
0b10 & 16KB. \\
\hline
\end{tabular}
\end{center}

Other values are reserved.

If the value is programmed to either a reserved value, or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an \texttt{IMPLEMENTATION DEFINED} choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is \texttt{IMPLEMENTATION DEFINED} whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.

\textbf{SH0, bits [13:12]}

Shareability attribute for memory associated with translation table walks using \texttt{TTBR0_EL2}.

\begin{center}
\begin{tabular}{|c|c|}
\hline
\textbf{SH0} & \textbf{Meaning} \\
\hline
0b00 & Non-shareable. \\
0b10 & Outer Shareable. \\
0b11 & Inner Shareable. \\
\hline
\end{tabular}
\end{center}

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is \texttt{CONSTRAINED UNPREDICTABLE}.

On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.

\textbf{ORGN0, bits [11:10]}

Outer cacheability attribute for memory associated with translation table walks using \texttt{TTBR0_EL2}.

\begin{center}
\begin{tabular}{|c|c|}
\hline
\textbf{ORGN0} & \textbf{Meaning} \\
\hline
0b00 & Normal memory, Outer Non-cacheable. \\
0b01 & Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable. \\
0b10 & Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable. \\
0b11 & Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable. \\
\hline
\end{tabular}
\end{center}

On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.

\textbf{IRGN0, bits [9:8]}

Inner cacheability attribute for memory associated with translation table walks using \texttt{TTBR0_EL2}.

\begin{center}
\begin{tabular}{|c|c|}
\hline
\textbf{IRGN0} & \textbf{Meaning} \\
\hline
0b00 & Normal memory, Inner Non-cacheable. \\
0b01 & Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable. \\
0b10 & Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable. \\
0b11 & Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable. \\
\hline
\end{tabular}
\end{center}

On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.
**EPD0, bit [7]**

Translation table walk disable for translations using TTBR0_EL2. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR0_EL2. The encoding of this bit is:

<table>
<thead>
<tr>
<th>EPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBR0_EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBR0_EL2 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [6]**

Reserved, RES0.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by TTBR0_EL2. The region size is $2^{(64-T0SZ)}$ bytes.

The maximum and minimum possible values for T0SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the TCR_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic TCR_EL2 or TCR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, TCR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return TCR_EL2;
elsif PSTATE.EL == EL3 then
    return TCR_EL2;
TCR_EL2, Translation Control Register (EL2)

**MSR TCR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TCR_EL2 = X[t];
else
  TCR_EL2 = X[t];

**MRS <Xt>, TCR_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TCR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x120];
  else
    return TCR_EL1;
else
  TCR_EL2 = X[t];
else
  TCR_EL2 = X[t];
else
  TCR_EL2 = X[t];
else
  TCR_EL1 = X[t];

**MSR TCR_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TCR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x120] = X[t];
  else
    TCR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TCR_EL2 = X[t];
  else
    TCR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL3 then
  TCR_EL1 = X[t];
endif
TCR_EL3, Translation Control Register (EL3)

The TCR_EL3 characteristics are:

**Purpose**

The control register for stage 1 of the EL3 translation regime.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to TCR_EL3 are undefined.

**Attributes**

TCR_EL3 is a 64-bit register.

**Field descriptions**

The TCR_EL3 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
| RES0 | DS | RES1 | TCMA | TBID | HWU62 | HWU61 | HWU60 | HWU59 | HDHA | TBI | RES0 | PS | TG0 | SH0 | ORGN0 | IRGN0 | RES0 | T0SZ |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |

Any of the bits in TCR_EL3 are permitted to be cached in a TLB.

**Bits [63:33]**

Reserved, RES0.

**DS, bit [32]**

When FEAT_LPA2 is implemented:

This field affects 52-bit output addressing when using 4KB and 16KB translation granules in stage 1 of the EL3 translation regime.
Meaning

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits[49:48] of translation descriptors hold output address[49:48]. Bits[9:8] of table translation descriptors hold output address[51:50]. The shareability information of block and page descriptors for cacheable locations is determined by TCR_EL3.SH0. The minimum value of TCR_EL3.T0SZ is 12. Any memory access using a smaller value generates a stage 1 level 0 translation table fault. All calculations of the stage 1 base address are modified for tables of fewer than 8 entries so that the table is aligned to 64 bytes. Bits[5:2] of TTB0_EL3 are used to hold bits[51:48] of the output address in all cases.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>Note: As FEAT_LVA must be implemented if TCR_EL3.DS == 1, the minimum value of the TCR_EL3.T0SZ field is 12, as determined by that extension. For the TLBI Range instructions affecting VA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as 0b0000. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as 0b00.</td>
<td></td>
</tr>
</tbody>
</table>

Note

As FEAT_LVA must be implemented if TCR_EL3.DS == 1, the minimum value of the TCR_EL3.T0SZ field is 12, as determined by that extension.

For the TLBI Range instructions affecting VA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as 0b0000. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as 0b00.

This field is RES0 for a 64KB translation granule.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [31]

Reserved, RES1.

TCMA, bit [30]

When FEAT_MTE is implemented:

Controls the generation of Unchecked accesses at EL3 when address [59:56] = 0b0000.

<table>
<thead>
<tr>
<th>TCMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the generation of Unchecked accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>All accesses are Unchecked.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**TBID, bit [29]**

When FEAT_PAuth is implemented:

Controls the use of the top byte of instruction addresses for address matching.

<table>
<thead>
<tr>
<th>TBID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TCR_EL3.TBI applies to Instruction and Data accesses.</td>
</tr>
<tr>
<td>0b1</td>
<td>TCR_EL3.TBI applies to Data accesses only.</td>
</tr>
</tbody>
</table>

This affects addresses where the address would be translated by tables pointed to by TTBR0_EL3.

For the purpose of this field, all cache maintenance and address translation instructions that perform address translation are treated as data accesses.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**HWU62, bit [28]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU62</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL3.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL3.HPD is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**HWU61, bit [27]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU61</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TCR_EL3.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL3.HPD is 0.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**HWU60, bit [26]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates **IMPLEMENTATION DEFINED** hardware use of bit[60] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU60</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an <strong>IMPLEMENTATION DEFINED</strong> purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an <strong>IMPLEMENTATION DEFINED</strong> purpose if the value of TCR_EL3.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL3.HPD is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**HWU59, bit [25]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates **IMPLEMENTATION DEFINED** hardware use of bit[59] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU59</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an <strong>IMPLEMENTATION DEFINED</strong> purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an <strong>IMPLEMENTATION DEFINED</strong> purpose if the value of TCR_EL3.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TCR_EL3.HPD is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**HPD, bit [24]**

*When FEAT_HPDS is implemented:*

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, PXNTable, and UXNTable, except NSTable, in the translation tables pointed to by TTBR0_EL3.
**HPD**

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>Hierarchical permissions are enabled.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

**Note**
In this case, bit[61] \( \text{APTTable}[0] \) and bit[59] \( \text{PXNTable} \) of the next level descriptor attributes are required to be ignored by the PE, and are no longer reserved, allowing them to be used by software.

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**Bit [23]**

Reserved, **RES1**.

**HD, bit [22]**

When **FEAT_HAFDBS** is implemented:

Hardware management of dirty state in stage 1 translations from EL3.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>Stage 1 hardware management of dirty state disabled.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b1</td>
<td>Stage 1 hardware management of dirty state enabled, only if the HA bit is also set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**HA, bit [21]**

When **FEAT_HAFDBS** is implemented:

Hardware Access flag update in stage 1 translations from EL3.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>Stage 1 Access flag update disabled.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b1</td>
<td>Stage 1 Access flag update enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**TBI, bit [20]**

Top Byte Ignored. Indicates whether the top byte of an address is used for address match for the **TTBR0_EL3** region, or ignored and used for tagged addresses.
<table>
<thead>
<tr>
<th>TBI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Top Byte used in the address calculation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Top Byte ignored in the address calculation.</td>
</tr>
</tbody>
</table>

This affects addresses generated in EL3 using AArch64 where the address would be translated by tables pointed to by TTBR0_EL3. It has an effect whether the EL3 translation regime is enabled or not.

If FEAT_PAuth is implemented and TCR_EL3.TBID is 1, then this field only applies to Data accesses.

Otherwise, if the value of TBI is 1, then bits[63:56] of that target address are also set to 0 before the address is stored in the PC, in the following cases:

- A branch or procedure return within EL3.
- A exception taken to EL3.
- An exception return to EL3.

For more information, see 'Address tagging in AArch64 state'.

**Note**

This control determines the scope of address tagging. It never causes an exception to be generated.

On a Warm reset, this field resets to an architecturally unknown value.

**Bit [19]**

Reserved, RES0.

**PS, bits [18:16]**

Physical Address Size.

<table>
<thead>
<tr>
<th>PS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>32 bits, 4GB.</td>
</tr>
<tr>
<td>0b001</td>
<td>36 bits, 64GB.</td>
</tr>
<tr>
<td>0b010</td>
<td>40 bits, 1TB.</td>
</tr>
<tr>
<td>0b011</td>
<td>42 bits, 4TB.</td>
</tr>
<tr>
<td>0b100</td>
<td>44 bits, 16TB.</td>
</tr>
<tr>
<td>0b101</td>
<td>48 bits, 256TB.</td>
</tr>
<tr>
<td>0b110</td>
<td>52 bits, 4PB.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The reserved values behave in the same way as the 0b101 or 0b110 encoding, but software must not rely on this property as the behavior of the reserved values might change in a future revision of the architecture.

If the translation granule is not 64KB and FEAT_LPA2 is not implemented, the value 0b110 is treated as reserved.

It is implementation defined whether an implementation that does not implement FEAT_LPA supports setting the value of 0b110 for the 64KB translation granule size or whether setting this value behaves as the 0b101 encoding.

In an implementation that supports 52-bit PAs, if the value of this field is not 0b110 or a value treated as 0b110, then bits[51:48] of every translation table base address for the stage of translation controlled by TCR_EL3 are 0b0000.

On a Warm reset, this field resets to an architecturally unknown value.

**TG0, bits [15:14]**

Granule size for the TTBR0_EL3.

<table>
<thead>
<tr>
<th>TG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>16KB.</td>
</tr>
</tbody>
</table>
Other values are reserved.

If the value is programmed to either a reserved value or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an IMPLEMENTATION DEFINED choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is IMPLEMENTATION DEFINED whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SH0, bits [13:12]**

Shareability attribute for memory associated with translation table walks using TTBR0_EL3.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ORGN0, bits [11:10]**

Outer cacheability attribute for memory associated with translation table walks using TTBR0_EL3.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IRGN0, bits [9:8]**

Inner cacheability attribute for memory associated with translation table walks using TTBR0_EL3.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [7:6]**

Reserved, RES0.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by TTBR0_EL3. The region size is $2^{(64-T0SZ)}$ bytes.

The maximum and minimum possible values for T0SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.
Note

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the TCR_EL3

Accesses to this register use the following encodings:

MRS <Xt>, TCR_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return TCR_EL3;

MSR TCR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TCR_EL3 = X[t];
The TFSR_EL1 characteristics are:

**Purpose**

Holds accumulated Tag Check Faults occurring in EL1 that are not taken precisely.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to TFSR_EL1 are UNDEFINED.

**Attributes**

TFSR_EL1 is a 64-bit register.

**Field descriptions**

The TFSR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignments</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>61</td>
<td>TF1</td>
</tr>
<tr>
<td>60</td>
<td>TF0</td>
</tr>
<tr>
<td>59</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
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<tr>
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<td>36</td>
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<td>35</td>
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<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:2]**

Reserved, RES0.

**TF1, bit [1]**

Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b1 occurs.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TF0, bit [0]**

Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b0 occurs.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TFSR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, TFSR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return NVMem[0x190];
    endif
    return TFSR_EL1;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        endif
    else
        return TFSR_EL2;
    endif
    return TFSR_EL1;
elsif PSTATE.EL == EL3 then
    return TFSR_EL1;

MSR TFSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TFSR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TFSR_EL2 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    TFSR_EL1 = X[t];
else
    MRS <Xt>, TFSR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x190];
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      TFSR_EL1 = X[t];
    end
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    TFSR_EL1 = X[t];
  else
    UNDEFINED;
end

MSR TFSR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x190] = X[t];
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    else
      TFSR_EL1 = X[t];
    end
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    TFSR_EL1 = X[t];
  else
    UNDEFINED;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
            UNDEFINED;
        elsif EL2Enabled() && HCR_EL2.ATA == '0' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
        else
            UNDEFINED;
        end if
    else
        return TFSR_EL1;
    end if
elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return TFSR_EL2;
    end if
elsif PSTATE.EL == EL3 then
    return TFSR_EL2;

MSR TFSR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
      & SCR_EL3.ATA == '0' then
        UNDEFINED;
      elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
      elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.SystemAccessTrap(EL3, 0x18);
      else
        TFSR_EL1 = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'
    & SCR_EL3.ATA == '0' then
      UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
  else
    TFSR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TFSR_EL2 = X[t];
**TFSR_EL2, Tag Fault Status Register (EL2)**

The TFSR_EL2 characteristics are:

**Purpose**

Holds accumulated Tag Check Faults occurring in EL2 that are not taken precisely.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to TFSR_EL2 are UNDEFINED.

**Attributes**

TFSR_EL2 is a 64-bit register.

**Field descriptions**

The TFSR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
</tr>
<tr>
<td>-----</td>
<td>-----------------------------</td>
</tr>
<tr>
<td>RES0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**Bits [63:2]**

Reserved, RES0.

**TF1, bit [1]**

Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b1 occurs.

When **HCR_EL2.E2H==0b0**, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TF0, bit [0]**

Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b0 occurs.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TFSR_EL2**

When **HCR_EL2.E2H==1**, without explicit synchronization, access from EL2 using the mnemonic TFSR_EL2 or TFSR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      else
        return TFSR_EL1;
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        return TFSR_EL2;
    elsif PSTATE.EL == EL3 then
      return TFSR_EL2;

MSR TFSR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
      UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.SystemAccessTrap(EL3, 0x18);
      end
    end
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  end
elsif PSTATE.EL == EL3 then
  TFSR_EL2 = X[t];
end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  end
else
  TFSR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TFSR_EL2 = X[t];
end

MRS <Xt>, TFSR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.ATA == '0' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif HCR_EL2.E2H == '1' then
    return TFSR_EL2;
  else
    return TFSR_EL1;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR_EL3.ATA == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end if
  elsif HCR_EL2.E2H == '1' then
    return TFSR_EL2;
  else
    return TFSR_EL1;
  end if
elsif PSTATE.EL == EL3 then
  return TFSR_EL1;

MSR TFSR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    else
        if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
            NVMem[0x190] = X[t];
        else
            TFSR_EL1 = X[t];
        end if;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1" && SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && SCR_EL3.ATA == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if;
    elsif HCR_EL2.E2H == '1' then
        TFSR_EL2 = X[t];
    else
        TFSR_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    TFSR_EL1 = X[t];
else
    TFSR_EL1 = X[t];
end if;
TFSR_EL3, Tag Fault Status Register (EL3)

The TFSR_EL3 characteristics are:

**Purpose**

Holds accumulated Tag Check Faults occurring in EL3 that are not taken precisely.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to TFSR_EL3 are **UNDEFINED**.

**Attributes**

TFSR_EL3 is a 64-bit register.

**Field descriptions**

The TFSR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>-----</td>
<td>----------------</td>
<td>-------------</td>
</tr>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
</tbody>
</table>

**Bits [63:1]**

Reserved, RES0.

**TF0, bit [0]**

Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b0 occurs.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the TFSR_EL3**

Accesses to this register use the following encodings:

```assembly
MRS <Xt>, TFSR_EL3
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```assembly
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return TFSR_EL3;
```
MSR TFSR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TFSR_EL3 = X[t];
The TFSRE0_EL1 characteristics are:

**Purpose**

Holds accumulated Tag Check Faults occurring in EL0 that are not taken precisely.

**Configuration**

This register is present only when FEAT_MTE2 is implemented. Otherwise, direct accesses to TFSRE0_EL1 are UNDEFINED.

**Attributes**

TFSRE0_EL1 is a 64-bit register.

**Field descriptions**

The TFSRE0_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>TF1, bit [1]</td>
</tr>
<tr>
<td>61</td>
<td>Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b1 occurs.</td>
</tr>
<tr>
<td>60</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>61</td>
<td>TF0, bit [0]</td>
</tr>
<tr>
<td>60</td>
<td>Tag Check Fault. Asynchronously set to 1 when a Tag Check Fault using a virtual address with bit[55] == 0b0 occurs.</td>
</tr>
<tr>
<td>59</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>

**Accessing the TFSRE0_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, TFSRE0_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" & SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() & HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) & SCR_EL3.ATA == '0' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        return TFSRE0_EL1;
    end if
else
    if PSTATE.EL == EL2 then
        if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" & SCR_EL3.ATA == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) & SCR_EL3.ATA == '0' then
            if Halted() & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end if
        else
            return TFSRE0_EL1;
        end if
    elsif PSTATE.EL == EL3 then
        return TFSRE0_EL1;
    else
        MSR TFSRE0_EL1, <Xt>;
    end if
end if

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" & SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif EL2Enabled() & HCR_EL2.ATA == '0' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) & SCR_EL3.ATA == '0' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TFSRE0_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
priority when SDD == '1'" & SCR_EL3.ATA == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & SCR_EL3.ATA == '0' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TFSRE0_EL1 = X[t];
    end if
elsif PSTATE.EL == EL3 then
    TFSRE0_EL1 = X[t];
end if
TFSRE0_EL1, Tag Fault Status Register (EL0).
**TLBI ALLE1, TLBI ALLE1NXS, TLB Invalidate All, EL1**

The TLBI ALLE1, TLBI ALLE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If $\text{SCR\_EL3}_\text{NS}$ is 0 and the entry would be required to translate an address using the Secure EL1&0 translation regime.
- If $\text{SCR\_EL3}_\text{NS}$ is 1 and the entry would be required to translate an address using the Non-secure EL1&0 translation regime.

The invalidation applies to entries with any VMID.

The invalidation only applies to the PE that executes this System instruction.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE1, TLBI ALLE1NXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by $<Xt>$ is ignored.

**Executing the TLBI ALLE1, TLBI ALLE1NXS instruction**

When executing this instruction $Xt$ should be encoded as $0b11111$. If the $Xt$ field is not set to $0b11111$, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the $Xt$ field is set to $0b11111$.

Accesses to this instruction use the following encodings:
TLBI ALLE1, TLBI ALLE1NXS, TLB Invalidate All, EL1

TLBI ALLE1{}, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsf PSTATE.EL == EL2 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_None, TLBI_AllAttr);
elsf PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_None, TLBI_AllAttr);

tlbi allex1, tlbi allex1nxs, tlb invalidate all, el1

TLBI ALLE1NXS{}, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsf PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsf PSTATE.EL == EL2 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_None, TLBI_ExcludeXS);
elsf PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_None, TLBI_ExcludeXS);
The TLBI ALLE1IS, TLBI ALLE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If `SCR_EL3.NS` is 0 and the entry would be required to translate an address using the Secure EL1&0 translation regime.
- If `SCR_EL3.NS` is 1 and the entry would be required to translate an address using the Non-secure EL1&0 translation regime.

The invalidation applies to entries with any VMID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE1IS, TLBI ALLE1ISNXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by `<Xt>` is ignored.

**Executing the TLBI ALLE1IS, TLBI ALLE1ISNXS instruction**

When executing this instruction Xt should be encoded as `0b11111`. If the Xt field is not set to `0b11111`, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to `0b11111`. 

TLBI ALLE1IS, TLBI ALLE1ISNXS, TLB Invalidate All, EL1, Inner Shareable
Accesses to this instruction use the following encodings:

**TLBI ALLE1IS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
elsif PSTATE.EL == EL2 then
   TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Inner, TLBI_AllAttr);
eelsif PSTATE.EL == EL3 then
   TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Inner, TLBI_AllAttr);

**TLBI ALLE1ISNXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
   UNDEFINED;
elsif PSTATE.EL == EL0 then
   UNDEFINED;
eelsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
eelsif PSTATE.EL == EL2 then
   TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Inner, TLBI_ExcludeXS);
eelsif PSTATE.EL == EL3 then
   TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Inner, TLBI_ExcludeXS);
The TLBI ALLE1OS, TLBI ALLE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If SCR_EL3.NS is 0 and the entry would be required to translate an address using the Secure EL1&0 translation regime.
- If SCR_EL3.NS is 1 and the entry would be required to translate an address using the Non-secure EL1&0 translation regime.

The invalidation applies to entries with any VMID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI ALLE1OS, TLBI ALLE1OSNXS are **UNDEFINED**.

**Attributes**

TLBI ALLE1OS, TLBI ALLE1OSNXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the TLBI ALLE1OS, TLBI ALLE1OSNXS instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is **CONSTRAINED UNPREDICTABLE** whether:

- The instruction is **UNDEFINED**.
- The instruction behaves as if the Xt field is set to 0b11111.
Accesses to this instruction use the following encodings:

**TLBI ALLE1OS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Outer, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Outer, TLBI_AllAttr);

**TLBI ALLE1OSNXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
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<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Outer, TLBI_ExcludeXS);
elsif PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL1), Regime_EL10, Shareability_Outer, TLBI_ExcludeXS);
TLBI ALLE2, TLBI ALLE2NXS, TLB Invalidate All, EL2

The TLBI ALLE2, TLBI ALLE2NXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- If `SCR_EL3.NS` is 0 and the entry would be required to translate an address using the Secure EL2 or Secure EL2&0 translation regime.
- If `SCR_EL3.NS` is 1 and the entry would be required to translate an address using the Non-secure EL2 or Non-secure EL2&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE2, TLBI ALLE2NXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by `<Xt>` is ignored.

**Executing the TLBI ALLE2, TLBI ALLE2NXS instruction**

When executing this instruction `<Xt>` should be encoded as `0b11111`. If the `<Xt>` field is not set to `0b11111`, it is **CONSTRAINED UNPREDICTABLE** whether:

- The instruction is **UNDEFINED**.
- The instruction behaves as if the `<Xt>` field is set to `0b11111`.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_None, TLBI_AllAttr);
    else
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_None, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_None, TLBI_AllAttr);
    else
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_None, TLBI_AllAttr);

TLBI ALLE2NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_None, TLBI_ExcludeXS);
    else
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_None, TLBI_ExcludeXS);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_None, TLBI_ExcludeXS);
    else
        TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_None, TLBI_ExcludeXS);
The TLBI ALLE2IS, TLBI ALLE2ISNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- If \( \text{SCR}_{\text{EL3}} \).NS is 0 and the entry would be required to translate an address using the Secure EL2 or Secure EL2&0 translation regime.
- If \( \text{SCR}_{\text{EL3}} \).NS is 1 and the entry would be required to translate an address using the Non-secure EL2 or Non-secure EL2&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If \( \text{FEAT}_{\text{XS}} \) is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE2IS, TLBI ALLE2ISNXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by \(<\text{Xt}>\) is ignored.

**Executing the TLBI ALLE2IS, TLBI ALLE2ISNXS instruction**

When executing this instruction \(\text{Xt}\) should be encoded as 0b11111. If the \(\text{Xt}\) field is not set to 0b11111, it is constrained unpredictable whether:

- The instruction is undefined.
- The instruction behaves as if the \(\text{Xt}\) field is set to 0b11111.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>(\text{op0})</th>
<th>(\text{op1})</th>
<th>(\text{CRn})</th>
<th>(\text{CRm})</th>
<th>(\text{op2})</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
elsif PSTATE.EL == EL2 then
   if HCR_EL2.E2H == '1' then
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Inner, TLBI_AllAttr);
   else
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Inner, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
   if !EL2Enabled() then
      UNDEFINED;
   elsif HCR_EL2.E2H == '1' then
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Inner, TLBI_AllAttr);
   else
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Inner, TLBI_AllAttr);

TLB invalidate all, EL2, Inner Shareable

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
   UNDEFINED;
elsif PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
elsif PSTATE.EL == EL2 then
   if HCR_EL2.E2H == '1' then
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Inner, TLBI_ExcludeXS); 
   else
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Inner, TLBI_ExcludeXS);
elsif PSTATE.EL == EL3 then
   if !EL2Enabled() then
      UNDEFINED;
   elsif HCR_EL2.E2H == '1' then
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Inner, TLBI_ExcludeXS);
   else
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Inner, TLBI_ExcludeXS);
The TLBI ALLE2OS, TLBI ALLE2OSNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- If SCR_EL3.NS is 0 and the entry would be required to translate an address using the Secure EL2 or Secure EL2&0 translation regime.
- If SCR_EL3.NS is 1 and the entry would be required to translate an address using the Non-secure EL2 or Non-secure EL2&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI ALLE2OS, TLBI ALLE2OSNXS are UNDEFINED.

**Attributes**

TLBI ALLE2OS, TLBI ALLE2OSNXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the TLBI ALLE2OS, TLBI ALLE2OSNXS instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

```
TLBI ALLE2OS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
  if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
  elsif PSTATE.EL == EL0 then
    UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Outer, TLBI_AllAttr);
    else
      TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL20, Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_ALL(SecurityStateAtEL(EL2), Regime_EL2, Shareability_Outer, TLBI_AllAttr);
The TLBI ALLE3, TLBI ALLE3NXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be required to translate an address using the EL3 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE3, TLBI ALLE3NXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the TLBI ALLE3, TLBI ALLE3NXS instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL3), Regime_EL3, Shareability_None, TLBI_AllAttr);

TLBI ALLE3NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL3), Regime_EL3, Shareability_None, TLBI_ExcludeXS);
TLBI ALLE3IS, TLBI ALLE3ISNXS, TLB Invalidate All, EL3, Inner Shareable

The TLBI ALLE3IS, TLBI ALLE3ISNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be required to translate an address using the EL3 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ALLE3IS, TLBI ALLE3ISNXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by \(<Xt>\) is ignored.

**Executing the TLBI ALLE3IS, TLBI ALLE3ISNXS instruction**

When executing this instruction \(Xt\) should be encoded as \(0b11111\). If the \(Xt\) field is not set to \(0b11111\), it is \textit{CONSTRAINED UNPREDICTABLE} whether:

- The instruction is \textit{UNDEFINED}.
- The instruction behaves as if the \(Xt\) field is set to \(0b11111\).

Accesses to this instruction use the following encodings:

\[
\text{TLBI ALLE3IS\{, <Xt>\}}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_ALL(SecurityStateAtEL(EL3), Regime_EL3, Shareability_Inner, TLBI_AllAttr);

TLBI Alle3ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_ALL(SecurityStateAtEL(EL3), Regime_EL3, Shareability_Inner, TLBI_ExcludeXS);
TLBI ALLE3OS, TLBI ALLE3OSNXS, TLB Invalidate All, EL3, Outer Shareable

The TLBI ALLE3OS, TLBI ALLE3OSNXS characteristics are:

Purpose

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be required to translate an address using the EL3 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

Configuration

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI ALLE3OS, TLBI ALLE3OSNXS are UNDEFINED.

Attributes

TLBI ALLE3OS, TLBI ALLE3OSNXS is a 64-bit System instruction.

Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

Executing the TLBI ALLE3OS, TLBI ALLE3OSNXS instruction

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

TLBI ALLE3OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_ALL(SecurityStateAtEL(EL3), Regime_EL3, Shareability_Outer, TLBI_AllAttr);

TLBIALLE3OSNXS{
\,<Xt>\}
TLBI ASIDE1, TLBI ASIDE1NXS, TLB Invalidate by ASID, EL1

The TLBI ASIDE1, TLBI ASIDE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate an address using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate an address using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate an address using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ASIDE1, TLBI ASIDE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI ASIDE1, TLBI ASIDE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASID</td>
</tr>
<tr>
<td>RES0</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any appropriate TLB entries that match the ASID values will be affected by this System instruction.
If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**Bits [47:0]**

Reserved, RES0.

**Executing the TLBI ASIDE1, TLBI ASIDE1NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI ASIDE1{
\begin{tabular}{|c|c|c|c|c|}
\hline
  op0 & op1 & CRn & CRm & op2 \\
\hline
  0b01 & 0b000 & 0b1000 & 0b0111 & 0b010 \\
\hline
\end{tabular}

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIASIDE1 == '1' then
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBI_AllAttr, X[t]);
  endif
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
    TLBI_AllAttr, X[t]);
  endif
endif
if PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  endif
endif
if PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  endif
endif
**TLBI ASIDE1NXS{
\begin{tabular}{|c|c|c|c|c|}
\hline
  op0 & op1 & CRn & CRm & op2 \\
\hline
  0b01 & 0b000 & 0b1001 & 0b0111 & 0b010 \\
\hline
\end{tabular}

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIASIDE1 == '1' then
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBI_AllAttr, X[t]);
  endif
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
    TLBI_AllAttr, X[t]);
  endif
endif
if PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  endif
endif
if PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr,
    X[t]);
  endif
endif
**
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
        HFGITR_EL2.TLBIASIDE1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS, X[t]);
    else
        TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS, X[t]);
    end if PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_ExcludeXS, X[t]);
    else
        TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS, X[t]);
    end if PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_ExcludeXS, X[t]);
    else
        TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS, X[t]);
    end if
TLBI ASIDE1IS, TLBI ASIDE1ISNXS, TLB Invalidate by ASID, EL1, Inner Shareable

The TLBI ASIDE1IS, TLBI ASIDE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3.NS`:
  - If `HCR_EL2.{E2H, TGE}` is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate an address using the EL1&0 translation regime.
  - If `HCR_EL2.{E2H, TGE}` is \{1, 1\}, the entry would be required to translate an address using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate an address using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI ASIDE1IS, TLBI ASIDE1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI ASIDE1IS, TLBI ASIDE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>ASID</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
</tr>
<tr>
<td>61</td>
<td>60</td>
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<tr>
<td>59</td>
<td>58</td>
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<td>57</td>
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<td>14</td>
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<td>12</td>
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<td>11</td>
<td>10</td>
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<td>8</td>
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<td>7</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any appropriate TLB entries that match the ASID values will be affected by this System instruction.
If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Bits [47:0]
Reserved, RES0.

**Executing the TLBI ASIDE1IS, TLBI ASIDE1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI ASIDE1IS\{, <Xt>\}

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() &\& HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() &\& HCR_EL2.TTLB2 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() &\& (!HaveEL(EL3) || SCR_EL3.FGE == '1') &\& HCR_EL2.TLBIASIDE1IS == '1'
  then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) &\& HCRX_EL2.FnXS == '1' then
      TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
      TLBI_AllAttr, X[t]);
    else
      TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
      TLBI_AllAttr, X[t]);
    endif
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBI_AllAttr, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBI_AllAttr, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBI_AllAttr, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBI_AllAttr, X[t]);
  endif
```

TLBI ASIDE1ISNXS\{, <Xt>\}

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
```
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE_EL == EL0 then
  UNDEFINED;
elsif PSTATE_EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCR_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIASIDEI1S == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS, X[t]);
  end
elsif PSTATE_EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS, X[t]);
  end
elsif PSTATE_EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS, X[t]);
end
TLBI ASIDE1OS, TLBI ASIDE1OSNXS, TLB Invalidate by ASID, EL1, Outer Shareable

The TLBI ASIDE1OS, TLBI ASIDE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the entry would be used with the current VMID, and would be required to translate an address using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the entry would be required to translate an address using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate an address using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI ASIDE1OS, TLBI ASIDE1OSNXS are UNDEFINED.

**Attributes**

TLBI ASIDE1OS, TLBI ASIDE1OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI ASIDE1OS, TLBI ASIDE1OSNXS input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| ASID |     |
| RES0 |     |

Page 1626
ASID, bits [63:48]

ASID value to match. Any appropriate TLB entries that match the ASID values will be affected by this System instruction.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Bits [47:0]

Reserved, RES0.

Executing the TLBI ASIDE1OS, TLBI ASIDE1OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI ASIDE1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIASIDE1OS == '1'
    then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, 
    TLBI ExcludeXS, X[t]);
  else
    TLBI ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, 
    TLBI AllAttr, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, 
    TLBI AllAttr, X[t]);
  else
    TLBI ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, 
    TLBI AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, 
    TLBI AllAttr, X[t]);
  else
    TLBI ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, 
    TLBI AllAttr, X[t]);

TLBI ASIDE1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(Feat_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBISIDE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_ASID(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_ExcludeXS, X[t]);
  else
    TLBI_ASID(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS, X[t]);
  endif
The TLBI IPAS2E1, TLBI IPAS2E1NXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI IPAS2E1, TLBI IPAS2E1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI IPAS2E1, TLBI IPAS2E1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>NS</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
</tr>
<tr>
<td>61</td>
<td>TTL</td>
</tr>
<tr>
<td>60</td>
<td>RES0</td>
</tr>
<tr>
<td>59</td>
<td>IPA[51:48]</td>
</tr>
<tr>
<td>58</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>57</td>
<td></td>
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<tr>
<td>56</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**NS, bit [63]**

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.
### NS

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is **RES0**, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is **RES0**.

**Otherwise:**

Reserved, **RES0**.

**Bits [62:48]**

Reserved, **RES0**.

**TTL, bits [47:44]**

**When FEAT_TTL is implemented:**

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is <strong>RES0</strong>.</td>
</tr>
</tbody>
</table>
| 0b01xx | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:

  - 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00.
  - 0b01 : Level 1.
  - 0b10 : Level 2.
  - 0b11 : Level 3. |
| 0b10xx | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:

  - 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
  - 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00.
  - 0b10 : Level 2.
  - 0b11 : Level 3. |
| 0b11xx | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:

  - 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
  - 0b01 : Level 1.
  - 0b10 : Level 2.
  - 0b11 : Level 3. |

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, **RES0**.

**Bits [43:40]**

Reserved, **RES0**.
IPA[51:48], bits [39:36]

When FEAT_LPA is implemented:

Extension to IPA[47:12]. See IPA[47:12] for more details.

Otherwise:

Reserved, RES0.

IPA[47:12], bits [35:0]

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.

**Executing the TLBI IPAS2E1, TLBI IPAS2E1NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI IPAS2E1{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);

**TLBI IPAS2E1NXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
    elsif PSTATE_EL == EL2 then
        TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Any, TLBI_ExcludeXS, X[t]);
    elsif PSTATE_EL == EL3 then
        if !EL2Enabled() then
            //no operation
        else
            TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Any, TLBI_ExcludeXS, X[t]);
    end
else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Any, TLBI_ExcludeXS, X[t]);
The TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see ‘Invalidation of TLB entries from stage 2 translations’.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS input value bit assignments are:
NS, bit [63]

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

Otherwise:

Reserved, RES0.

Bits [62:48]

Reserved, RES0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00x</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01x</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10x</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11x</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.
**Bits [43:40]**

Reserved, RES0.

**IPA[51:48], bits [39:36]**

*When FEAT_LPA is implemented:*

Extension to IPA[47:12]. See IPA[47:12] for more details.

*Otherwise:*

Reserved, RES0.

**IPA[47:12], bits [35:0]**

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

*When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.*

**Executing the TLBI IPAS2E1IS, TLBI IPAS2E1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI IPAS2E1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if !EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
TLBI_IPAS2E1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
            TLBIExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    // no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
              TLBIExcludeXS, X[t]);
The TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see ‘Invalidation of TLB entries from stage 2 translations’.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS are UNDEFINED.

**Attributes**

TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>NS</td>
</tr>
<tr>
<td>62-60</td>
<td>RES0</td>
</tr>
<tr>
<td>59-57</td>
<td>TTL</td>
</tr>
<tr>
<td>56-54</td>
<td>RES0</td>
</tr>
<tr>
<td>53-50</td>
<td>IPA[51:48]</td>
</tr>
<tr>
<td>49-47</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>39-34</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>33-32</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>31-29</td>
<td>RES0</td>
</tr>
<tr>
<td>28-26</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>25-23</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>22-20</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>19-17</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>16-15</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>14-12</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>11-10</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>9-8</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>7-6</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>5-4</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>3-2</td>
<td>IPA[47:12]</td>
</tr>
<tr>
<td>1-0</td>
<td>IPA[47:12]</td>
</tr>
</tbody>
</table>

**NS, bit [63]**
When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is res0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is res0.

Otherwise:

Reserved, res0.

Bits [62:48]

Reserved, res0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, res0.

Bits [43:40]

Reserved, res0.
IPA[51:48], bits [39:36]

Extension to IPA[47:12]. See IPA[47:12] for more details.

IPA[47:12], bits [35:0]

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.

Executing the TLBI IPAS2E1OS, TLBI IPAS2E1OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI IPAS2E1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elseif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
elseif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);

TLBI IPAS2E1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elseif PSTATE.EL == EL0 then
  UNDEFINED;
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elseif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_ExcludeXS, X[t]);
elseif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_ExcludeXS, X[t]);
The TLBI IPAS2LE1, TLBI IPAS2LE1NXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI IPAS2LE1, TLBI IPAS2LE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI IPAS2LE1, TLBI IPAS2LE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>NS</th>
<th>RES0</th>
<th>TTL</th>
<th>RES0</th>
<th>IPA[51:48]</th>
<th>IPA[47:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
</tr>
</tbody>
</table>
**NS, bit [63]**

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

Otherwise:

Reserved, RES0.

**Bits [62:48]**

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.
**Bits [43:40]**

Reserved, RES0.

**IPA[51:48], bits [39:36]**

When FEAT_LPA is implemented:

Extension to IPA[47:12]. See IPA[47:12] for more details.

Otherwise:

Reserved, RES0.

**IPA[47:12], bits [35:0]**

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.

**Executing the TLBI IPAS2LE1, TLBI IPAS2LE1NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI IPAS2LE1{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elseif PSTATE.EL == EL2 then
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);

**TLBI IPAS2LE1NXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Last, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Last, TLBI_ExcludeXS, X[t]);
TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS, TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Inner Shareable

The TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see ‘Invalidation of TLB entries from stage 2 translations’.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NS | RES0 | TTL | RES0 | IPA[51:48] | IPA[47:12] |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
**NS, bit [63]**

When `FEAT_SEL2` is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is `RES0`, and the instruction applies only to the Non-secure IPA space.

When `FEAT_SEL2` is not implemented or is disabled in the current Security state, this field is `RES0`.

**Otherwise:**

Reserved, `RES0`.

**Bits [62:48]**

Reserved, `RES0`.

**TTL, bits [47:44]**

When `FEAT_TTL` is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is <code>RES0</code>.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If <code>FEAT_LPA2</code> is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If <code>FEAT_LPA2</code> is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, `RES0`. 
Bits [43:40]

Reserved, RES0.

IPA[51:48], bits [39:36]
When FEAT_LPA is implemented:

Extension to IPA[47:12]. See IPA[47:12] for more details.

Otherwise:

Reserved, RES0.

IPA[47:12], bits [35:0]

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.

**Executing the TLBI IPAS2LE1IS, TLBI IPAS2LE1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI IPAS2LE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if !EL2Enabled() && HCR_EL2.NV == ‘1’ then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        // no operation
    else
        TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI IPAS2LE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);

The TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS characteristics are:

### Purpose

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS are **Undefined**.

### Attributes

TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS is a 64-bit System instruction.

### Field descriptions

The TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS input value bit assignments are:

<p>| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|</p>
<table>
<thead>
<tr>
<th>NS</th>
<th>RES0</th>
<th>TTL</th>
<th>RES0</th>
<th>IPA[51:48]</th>
<th>IPA[47:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
</tr>
</tbody>
</table>

**NS, bit [63]**

Page 1649
When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

Otherwise:

Reserved, RES0.

Bits [62:48]

Reserved, RES0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

Bits [43:40]

Reserved, RES0.
IPA[51:48], bits [39:36]

Extension to IPA[47:12]. See IPA[47:12] for more details.

IPA[47:12], bits [35:0]

Bits[47:12] of the intermediate physical address to match. For implementations with fewer than 48 bits, the upper bits of this field are RES0.

When FEAT_LPA is implemented, and 52-bit addresses and a 64KB translation granule are in use, IPA[51:48] form the upper part of the address value. Otherwise, IPA[51:48] are RES0.

Executing the TLBI IPAS2LE1OS, TLBI IPAS2LE1OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI IPAS2LE10S{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI IPAS2LE10SNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then UNDEFINED;
elseif PSTATE.EL == EL0 then UNDEFINED;
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elseif PSTATE.EL == EL2 then
  TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
elseif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_IPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
The TLBI RIPAS2E1, TLBI RIPAS2E1NXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation_Granule_Size})]\).

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

For more information about the architectural requirements for this System instruction, see ‘Invalidation of TLB entries from stage 2 translations’.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RIPAS2E1, TLBI RIPAS2E1NXS are undefined.

Attributes

TLBI RIPAS2E1, TLBI RIPAS2E1NXS is a 64-bit System instruction.

Field descriptions

The TLBI RIPAS2E1, TLBI RIPAS2E1NXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NS | RES0 | TG | SCALE | NUM | TTL | BaseADDR |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

NS, bit [63]

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

Otherwise:

Reserved, RES0.

Bits [62:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.
NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this</td>
</tr>
<tr>
<td></td>
<td>field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RIPAS2E1, TLBI RIPAS2E1NXS instruction

Accesses to this instruction use the following encodings:

```
TLBI RIPAS2E1{, <Xt>}
```

<p>| | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>op0</td>
<td>op1</td>
<td>CRn</td>
<td>CRm</td>
<td>op2</td>
</tr>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b0100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_ANY, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    // no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_ANY, TLBI_AllAttr, X[t]);

TLBI_RIPAS2E1NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_ANY, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    // no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_ANY, TLBI_ExcludeXS, X[t]);
The TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \( \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation_Granule_Size}) \).

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS are UNDEFINED.

Attributes

TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS is a 64-bit System instruction.

Field descriptions

The TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved.</td>
</tr>
<tr>
<td>62</td>
<td>Reserved.</td>
</tr>
<tr>
<td>61</td>
<td>Reserved.</td>
</tr>
<tr>
<td>60</td>
<td>Reserved.</td>
</tr>
<tr>
<td>59</td>
<td>Reserved.</td>
</tr>
<tr>
<td>58</td>
<td>Reserved.</td>
</tr>
<tr>
<td>57</td>
<td>Reserved.</td>
</tr>
<tr>
<td>56</td>
<td>Reserved.</td>
</tr>
<tr>
<td>55</td>
<td>Reserved.</td>
</tr>
<tr>
<td>54</td>
<td>Reserved.</td>
</tr>
<tr>
<td>53</td>
<td>Reserved.</td>
</tr>
<tr>
<td>52</td>
<td>Reserved.</td>
</tr>
<tr>
<td>51</td>
<td>Reserved.</td>
</tr>
<tr>
<td>50</td>
<td>Reserved.</td>
</tr>
<tr>
<td>49</td>
<td>Reserved.</td>
</tr>
<tr>
<td>48</td>
<td>Reserved.</td>
</tr>
<tr>
<td>47</td>
<td>Reserved.</td>
</tr>
<tr>
<td>46</td>
<td>Reserved.</td>
</tr>
<tr>
<td>45</td>
<td>Reserved.</td>
</tr>
<tr>
<td>44</td>
<td>Reserved.</td>
</tr>
<tr>
<td>43</td>
<td>Reserved.</td>
</tr>
<tr>
<td>42</td>
<td>Reserved.</td>
</tr>
<tr>
<td>41</td>
<td>Reserved.</td>
</tr>
<tr>
<td>40</td>
<td>Reserved.</td>
</tr>
<tr>
<td>39</td>
<td>Reserved.</td>
</tr>
<tr>
<td>38</td>
<td>Reserved.</td>
</tr>
<tr>
<td>37</td>
<td>Reserved.</td>
</tr>
<tr>
<td>36</td>
<td>Reserved.</td>
</tr>
<tr>
<td>35</td>
<td>Reserved.</td>
</tr>
<tr>
<td>34</td>
<td>Reserved.</td>
</tr>
<tr>
<td>33</td>
<td>Reserved.</td>
</tr>
<tr>
<td>32</td>
<td>Reserved.</td>
</tr>
<tr>
<td>31</td>
<td>Reserved.</td>
</tr>
<tr>
<td>30</td>
<td>Reserved.</td>
</tr>
<tr>
<td>29</td>
<td>Reserved.</td>
</tr>
<tr>
<td>28</td>
<td>Reserved.</td>
</tr>
<tr>
<td>27</td>
<td>Reserved.</td>
</tr>
<tr>
<td>26</td>
<td>Reserved.</td>
</tr>
<tr>
<td>25</td>
<td>Reserved.</td>
</tr>
<tr>
<td>24</td>
<td>Reserved.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved.</td>
</tr>
<tr>
<td>21</td>
<td>Reserved.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved.</td>
</tr>
<tr>
<td>17</td>
<td>Reserved.</td>
</tr>
<tr>
<td>16</td>
<td>Reserved.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved.</td>
</tr>
<tr>
<td>14</td>
<td>Reserved.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved.</td>
</tr>
<tr>
<td>12</td>
<td>Reserved.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved.</td>
</tr>
<tr>
<td>9</td>
<td>Reserved.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved.</td>
</tr>
<tr>
<td>4</td>
<td>Reserved.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

NS, bit [63]

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

Otherwise:

Reserved, RES0.

Bits [62:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.
NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this</td>
</tr>
<tr>
<td></td>
<td>field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RIPAS2E1IS, TLBI RIPAS2E1ISNXS instruction**

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>TLBI RIPAS2E1IS{, &lt;Xt&gt;}</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);

TLBI RIPAS2E1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
The TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)\times2^{(5\times\text{SCALE} + 1)} \times \text{Translation_Granule_Size})]\).

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS are **UNDEFINED**.

Attributes

TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>NS</td>
<td>Not Secure. Specifies the IPA space.</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>61</td>
<td>TG</td>
<td>Translation granule size.</td>
</tr>
<tr>
<td>60</td>
<td>SCALE</td>
<td>The exponent element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>59</td>
<td>NUM</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>58</td>
<td>TTL</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>57</td>
<td>BaseADDR</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**NS, bit [63]**

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is **RES0**, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is **RES0**.

Otherwise:

Reserved, **RES0**.

**Bits [62:48]**

Reserved, **RES0**.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.
NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field</td>
</tr>
<tr>
<td></td>
<td>as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RIPAS2E1OS, TLBI RIPAS2E1OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI RIPAS2E1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllocAttr, X[t]);
else if PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllocAttr, X[t]);
endif

TLBI RIPAS2E1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_EXCLUDEXS, X[t]);
else if PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_EXCLUDEXS, X[t]);
endif
The TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - SCR_EL3.NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3.NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \[ \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation_Granule_Size}) \].

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation only applies to the PE that executes this System instruction.

The range of addresses invalidated is \text{UNPREDICTABLE} when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS are undefined.

**Attributes**

TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>NS</th>
<th>RES0</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
</tr>
<tr>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
</tr>
<tr>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td>45</td>
<td>44</td>
<td>43</td>
</tr>
<tr>
<td>42</td>
<td>41</td>
<td>40</td>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
</tr>
<tr>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
<tr>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BaseADDR</td>
</tr>
</tbody>
</table>

**NS, bit [63]**

*When FEAT_SEL2 is implemented:*

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is RES0, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is RES0.

*Otherwise:*

Reserved, RES0.

**Bits [62:48]**

Reserved, RES0.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.
NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field as</td>
</tr>
<tr>
<td></td>
<td>0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RIPAS2LE1, TLBI RIPAS2LE1NXS instruction

Accesses to this instruction use the following encodings:

TLBI RIPAS2LE1{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
                    TLBILevel_Last, TLBI_AllAttr, X[t]);
endif;

TLBI_RIPAS2LE1NXS{,< Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
                    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
endif;
The TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - \( \text{SCR}_{\text{EL3}} \).NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - \( \text{SCR}_{\text{EL3}} \).NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \star 2^{(5 \star \text{SCALE} + 1)} \star \text{Translation_Granule_Size})]\).

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 00000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT-xs is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS are **UNDEFINED**.

Attributes

TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS is a 64-bit System instruction.

Field descriptions

The TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>NS</th>
<th>RES0</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
</tr>
<tr>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
</tr>
<tr>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td>45</td>
<td>44</td>
<td>43</td>
</tr>
<tr>
<td>42</td>
<td>41</td>
<td>40</td>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
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<tr>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
<td>31</td>
<td>30</td>
<td>29</td>
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<tr>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
</tr>
<tr>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NS, bit [63]**

When FEAT_SEL2 is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is **RES0**, and the instruction applies only to the Non-secure IPA space.

When FEAT_SEL2 is not implemented or is disabled in the current Security state, this field is **RES0**.

Otherwise:

Reserved, RES0.

**Bits [62:48]**

Reserved, RES0.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.
NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RIPAS2LE1IS, TLBI RIPAS2LE1ISNXS instruction

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b10</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
  TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI_RIPAS2LE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
  TLBIExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    //no operation
  else
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
    TLBILevel_Last, TLBIExcludeXS, X[t]);
The TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS, TLB Range Invalidate by Intermediate Physical Address, Stage 2, Last level, EL1, Outer Shareable characteristics are:

**Purpose**

If EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- One of the following applies:
  - SCR_EL3_NS is 0 and the entry would be required to translate the specified IPA using the Secure EL1&0 translation regime.
  - SCR_EL3_NS is 1 and the entry would be required to translate the specified IPA using the Non-secure EL1&0 translation regime.
- The entry would be used with the current VMID.
- The entry is within the address range determined by the formula \[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{5 \times \text{SCALE} + 1}) \times \text{Translation_Granule_Size}\].

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is UNPREDICTABLE when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000000000.
If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS are **undefined**.

**Attributes**

TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>NS</th>
<th>RES0</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
</tr>
<tr>
<td></td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td>51</td>
</tr>
<tr>
<td></td>
<td>50</td>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>44</td>
<td>43</td>
<td>42</td>
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<td>40</td>
<td>39</td>
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<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
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<td>33</td>
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<td></td>
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<td>25</td>
<td>24</td>
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<td>22</td>
<td>21</td>
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<td></td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
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<td></td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
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<td>9</td>
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<tr>
<td></td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NS, bit [63]**

When **FEAT_SEL2** is implemented:

Not Secure. Specifies the IPA space.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IPA is in the Secure IPA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>IPA is in the Non-secure IPA space.</td>
</tr>
</tbody>
</table>

When the instruction is executed in Non-secure state, this field is **RES0**, and the instruction applies only to the Non-secure IPA space.

When **FEAT_SEL2** is not implemented or is disabled in the current Security state, this field is **RES0**.

Otherwise:

Reserved, **RES0**.

**Bits [62:48]**

Reserved, **RES0**.

**TG, bits [47:46]**

Translation granule size.
The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.

**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

*When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:*

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

*Otherwise:*

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RIPAS2LE1OS, TLBI RIPAS2LE1OSNXS instruction**

Accesses to this instruction use the following encodings:

\[
\text{TLBI RIPAS2LE1OS\{, <Xt>\}}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b10</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
                    TLBILevel_Last, TLBI_AllAttr, X[t]);
TLBI RIPAS2LE1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        //no operation
    else
        TLBI_RIPAS2(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
                    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
TLBI RVAAE1, TLBI RVAAE1NXS, TLB Range Invalidate by VA, All ASID, EL1

The TLBI RVAAE1, TLBI RVAAE1NXS characteristics are:

Purpose

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3:NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{5\times\text{SCALE} + 1}) \times \text{Translation_Granule Size})\).

The invalidation applies to the PE that executes this System instruction.

Note

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is UNPREDICTABLE when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAAE1, TLBI RVAAE1NXS are UNDEFINED.
Attributes

TLBI RVAAE1, TLBI RVAAE1NXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAAE1, TLBI RVAAE1NXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TG | SCALE | NUM | TTL | BaseADDR |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAAE1, TLBI RVAAE1NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI RVAAE1{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!(HaveEL(EL3) || SCR_EL3.FGTEn == '1')) && HFGITR_EL2.TLBIRVAAE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBLLevel_Lower, TLBLExcludeXS, X[t]);
  elsif EL2Enabled() && HCR_EL2.EF == '1' then
    if IsFeatureImplemented(FEAT_XS) && HCR_EL2.FnXS == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBLLevel_Lower, TLBLExcludeXS, X[t]);
    elsif EL2Enabled() && !HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBLLevel_Lower, TLBLExcludeXS, X[t]);
    end
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    if IsFeatureImplemented(FEAT_XS) && HCR_EL2.FnXS == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBLLevel_Lower, TLBLExcludeXS, X[t]);
    elsif EL2Enabled() && HCR_EL2.FnXS == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBLLevel_Lower, TLBLExcludeXS, X[t]);
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBLLevel_Lower, TLBLAllAttr, X[t]);
    elsif PSTATE.EL == EL3 then
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBLLevel_Lower, TLBLAllAttr, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBLLevel_Lower, TLBLAllAttr, X[t]);
  else
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif PSTATE.EL == EL3 then
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBLLevel_Lower, TLBLAllAttr, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBLLevel_Lower, TLBLAllAttr, X[t]);
```

**TLBI RVAAE1NXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIRVAEE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    TLBI_RVAAE1(SecurityStateAtEL(EL2), Regime_EL10, VMID[], Shareability_Inner, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAAE1(SecurityStateAtEL(EL2), Regime_EL10, VMID[], Shareability_None, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAAE1XN(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAAE1XN(SecurityStateAtEL(EL2), Regime_EL10, VMID[], Shareability_None, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL10, VMID[], Shareability_None, TLBILevel.Any, TLBI_ExcludeXS, X[t]);
end if

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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The TLBI RVAAE1IS, TLBI RVAAE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of $\text{SCR_EL3}$.NS:
  - If $\text{HCR_EL2}$.{E2H, TGE} is not $\{1, 1\}$, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If $\text{HCR_EL2}$.{E2H, TGE} is $\{1, 1\}$, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula $[(\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)\times 2^{(5\times \text{SCALE} + 1)} \times \text{Translation_Granule_Size})]$.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if $\text{SCR_EL3}.EEL2==1$, then:

- A PE with $\text{SCR_EL3}.EEL2==1$ is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with $\text{SCR_EL3}.EEL2==0$.
- A PE with $\text{SCR_EL3}.EEL2==0$ is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with $\text{SCR_EL3}.EEL2==1$.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is *UNPREDICTABLE* when:

- For the 4K translation granule:
  - If $\text{TTL}==01$ and $\text{BaseADDR}[29:12]$ is not equal to $000000000000000000$.  
  - If $\text{TTL}==10$ and $\text{BaseADDR}[20:12]$ is not equal to $000000000$.  
- For the 16K translation granule:
  - If $\text{TTL}==10$ and $\text{BaseADDR}[24:14]$ is not equal to $00000000000$.  
- For the 64K translation granule:
  - If $\text{TTL}==01$ and $\text{BaseADDR}[41:16]$ is not equal to $00000000000000000000$.  

Page 1681
If `TTL==10` and `BaseADDR[28:16]` is not equal to `0000000000000000`.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when `FEAT_TLBIRANGE` is implemented. Otherwise, direct accesses to TLBI RVAAE11IS, TLBI RVAAE11ISNXS are **UNDEFINED**.

### Attributes

TLBI RVAAE11IS, TLBI RVAAE11ISNXS is a 64-bit System instruction.

### Field descriptions

The TLBI RVAAE11IS, TLBI RVAAE11ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62-61</td>
<td>TG</td>
</tr>
<tr>
<td>59-58</td>
<td>Translation granule size.</td>
</tr>
<tr>
<td>54</td>
<td>SCALE</td>
</tr>
<tr>
<td>50</td>
<td>NUM</td>
</tr>
<tr>
<td>49</td>
<td>TTL</td>
</tr>
<tr>
<td>0</td>
<td>BaseADDR</td>
</tr>
</tbody>
</table>

#### Bits [63:48]

Reserved, RES0.

#### TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

#### SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

#### NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

#### TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
### TTL

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

#### BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

- When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
- When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

- When using a 4KB translation granule, this field is BaseADDR[48:12].
- When using a 16KB translation granule, this field is BaseADDR[50:14].
- When using a 64KB translation granule, this field is BaseADDR[52:16].

### Executing the TLBI RVAAE1IS, TLBI RVAAE1ISNXS instruction

Accesses to this instruction use the following encodings:

TLBI RVAAE1IS\{, <Xt>\}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTL == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
end

TLBI RVAAE1ISNXS({, <Xt>})

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTL == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
end
The TLBI RVAAE1OS, TLBI RVAAE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)\times 2^5\times \text{SCALE} + 1) \times \text{Translation_Granule_Size}]\).

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIO is implemented. Otherwise, direct accesses to TLBI RVAAE1OS, TLBI RVAAE1OSNXS are UNDEFINED.

Attributes

TLBI RVAAE1OS, TLBI RVAAE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAAE1OS, TLBI RVAAE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-58</td>
<td>Reserved</td>
</tr>
<tr>
<td>57-51</td>
<td>Translation granule size</td>
</tr>
<tr>
<td>50-44</td>
<td>The exponent element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>43-39</td>
<td>The base element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>38-37</td>
<td>TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.</td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
### TTL

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

### BaseADDR, bits [36:0]

**When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:**

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

**Otherwise:**

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

### Executing the TLBI RVAAE1OS, TLBI RVAAE1OSNXS instruction

Accesses to this instruction use the following encodings:

**TLBI RVAAE1OS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1OS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
        endif
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    endif
else
    if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
    else
        if PSTATE.EL == EL0 then
            UNDEFINED;
        elsif PSTATE.EL == EL1 then
            if EL2Enabled() && HCR_EL2.TTLB == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1OS == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS, X[t]);
            endif
        elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
                TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            endif
        elsif PSTATE.EL == EL3 then
            if HCR_EL2.<E2H,TGE> == '11' then
                TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            endif
        endif
    endif
endif

TLBI RVAAE1OSN{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1OS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
        endif
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
    endif
else
    if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
    else
        if PSTATE.EL == EL0 then
            UNDEFINED;
        elsif PSTATE.EL == EL1 then
            if EL2Enabled() && HCR_EL2.TTLB == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAAE1OS == '1' then
                AArch64.SystemAccessTrap(EL2, 0x18);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS, X[t]);
            endif
        elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
                TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            endif
        elsif PSTATE.EL == EL3 then
            if HCR_EL2.<E2H,TGE> == '11' then
                TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            else
                TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
            endif
        endif
    endif
endif
The TLBI RVAALE1, TLBI RVAALE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula [BaseADDR <= VA < BaseADDR + ((NUM +1)*2^[5*SCALE +1] * Translation_Granule_Size)].

The invalidation applies to the PE that executes this System instruction.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAALE1, TLBI RVAALE1NXS are **UNDEFINED**.
Attributes

TLBI RVAALE1, TLBI RVAALE1NXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAALE1, TLBI RVAALE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>TG, Translation granule size.</td>
</tr>
<tr>
<td>61</td>
<td>SCALE, The exponent element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>60</td>
<td>NUM, The base element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>59</td>
<td>TTL, TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.</td>
</tr>
<tr>
<td>58</td>
<td>BaseADDR, The starting address for the range of the maintenance instructions.</td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAALE1, TLBI RVAALE1NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI RVAALE1{}, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (HaveEL(EL3) && SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAALE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
   TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
  elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '1' then
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
      TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);

**TLBI RVAALE1NXS{}, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0110</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
        HFGITR_EL2.TLBIRVAALE1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
        TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
            TLBI_ExcludeXS, X[t]);
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
            TLBILevel_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBILevel_Last,
            TLBI_ExcludeXS, X[t]);
    elsif PSTATE.EL == EL3 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
            TLBILevel_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBILevel_Last,
            TLBI_ExcludeXS, X[t]);
The TLBI RVAELE1IS, TLBI RVAELE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} +1)\times2^{(5\times\text{SCALE}+1)} \times \text{Translation_Granule_Size})]\).

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.

If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAALE1IS, TLBI RVAALE1ISNXS are UNDEFINED.

**Attributes**

TLBI RVAALE1IS, TLBI RVAALE1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVAALE1IS, TLBI RVAALE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>RES0, TG, SCALE, NUM, TTL, BaseADDR</td>
</tr>
<tr>
<td>31-0</td>
<td>BaseADDR</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.

**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAALE1IS, TLBI RVAALE1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI RVAALE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
  if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
  elsif PSTATE.EL == EL0 then
    UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() & HCR_EL2.TTLB == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
      elsif PSTATE.EL == EL0 then
        UNDEFINED;
      elsif PSTATE.EL == EL1 then
        if EL2Enabled() & HCR_EL2.TTLB == '1' then
          AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
          AArch64.SystemAccessTrap(EL2, 0x18);
        else
          if !IsFeatureImplemented(FEAT_XS) then
            UNDEFINED;
          elsif PSTATE.EL == EL0 then
            UNDEFINED;
          elsif PSTATE.EL == EL1 then
            if EL2Enabled() & HCR_EL2.TTLB == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            else
              UNDEFINED;
            end
          elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
            end
          elsif PSTATE.EL == EL3 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
            end
          end
        else
          if !IsFeatureImplemented(FEAT_XS) then
            UNDEFINED;
          elsif PSTATE.EL == EL0 then
            UNDEFINED;
          elsif PSTATE.EL == EL1 then
            if EL2Enabled() & HCR_EL2.TTLB == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            else
              UNDEFINED;
            end
          elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
            end
          elsif PSTATE.EL == EL3 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
          end
        else
          if !IsFeatureImplemented(FEAT_XS) then
            UNDEFINED;
          elsif PSTATE.EL == EL0 then
            UNDEFINED;
          elsif PSTATE.EL == EL1 then
            if EL2Enabled() & HCR_EL2.TTLB == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            else
              UNDEFINED;
            end
          elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
          end
        else
          if !IsFeatureImplemented(FEAT_XS) then
            UNDEFINED;
          elsif PSTATE.EL == EL0 then
            UNDEFINED;
          elsif PSTATE.EL == EL1 then
            if EL2Enabled() & HCR_EL2.TTLB == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            elsif EL2Enabled() & HCR_EL2.TTLBIS == '1' then
              AArch64.SystemAccessTrap(EL2, 0x18);
            else
              UNDEFINED;
            end
          elsif PSTATE.EL == EL2 then
            if HCR_EL2.<E2H,TGE> == '11' then
              TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
            else
              TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
          end
        end
      end
    end
  end
end

TLBI_RVAALE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>
The TLBI RVALE1OS, TLBI RVALE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.

- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.

- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5\times\text{SCALE} + 1)} \times \text{Translation_Granule_Size})]\). The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 0000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.

- For the 64K translation granule:
If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.

If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVAALE1OS, TLBI RVAALE1OSNXS are UNDEFINED.

### Attributes

TLBI RVAALE1OS, TLBI RVAALE1OSNXS is a 64-bit System instruction.

### Field descriptions

The TLBI RVAALE1OS, TLBI RVAALE1OSNXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TG | SCALE | NUM | TTL | BaseADDR |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:48]**

Reserved, RES0.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.

**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
### TLB TTL

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

### BaseADDR, bits [36:0]

**When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:**

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

- When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
- When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

**Otherwise:**

The starting address for the range of the maintenance instruction.

- When using a 4KB translation granule, this field is BaseADDR[48:12].
- When using a 16KB translation granule, this field is BaseADDR[50:14].
- When using a 64KB translation granule, this field is BaseADDR[52:16].

### Executing the TLBI RVAALE1OS, TLBI RVAALE1OSNXS instruction

Accesses to this instruction use the following encodings:

\[
\text{TLBI RVAALE1OS}\{, <Xt>\}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b10</td>
<td>0b0101</td>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end if;
else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
                   TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
                   TLBILevel_Last, TLBI_AllAttr, X[t]);
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
                   TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
                   TLBILevel_Last, TLBI_AllAttr, X[t]);
    end if;
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
                   TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                   TLBI_AllAttr, X[t]);
    end if;
else
    if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
    elif PSTATE.EL == EL0 then
        UNDEFINED;
    elseif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TTLB == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            AArch64.SystemAccessTrap(EL2, 0x18);
        end if;
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                       TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                       TLBI_AllAttr, X[t]);
        end if;
    elseif PSTATE.EL == EL3 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                       TLBI_AllAttr, X[t]);
        else
            TLBI_RVAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
                       TLBI_AllAttr, X[t]);
        end if;
    end if;
end if;

TLBI_RVAALE1OSXN{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b101</td>
<td>0b0101</td>
<td>0b111</td>
</tr>
</tbody>
</table>
TLBI RVAE1, TLBI RVAE1NXS, TLB Range Invalidate by VA, EL1

The TLBI RVAE1, TLBI RVAE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3.NS`:
  - If `HCR_EL2.{E2H, TGE}` is not `{1, 1}`, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If `HCR_EL2.{E2H, TGE}` is `{1, 1}`, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation_Granule_Size})]\).

The invalidation applies to the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

**Configuration**

This instruction is present only when `FEAT_TLBIRANGE` is implemented. Otherwise, direct accesses to TLBI RVAE1, TLBI RVAE1NXS are **UNDEFINED**.

**Attributes**

TLBI RVAE1, TLBI RVAE1NXS is a 64-bit System instruction.
Field descriptions

The TLBI RVAE1, TLBI RVAE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>ASID</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-48</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31-0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.
When using a 4KB translation granule, BaseADDR[15:12] is treated as \texttt{0b0000}.

When using a 16KB translation granule, BaseADDR[15:14] is treated as \texttt{0b00}.

\textbf{Otherwise:}

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

\textbf{Executing the TLBI RVAE1, TLBI RVAE1NXS instruction}

Accesses to this instruction use the following encodings:

\[
\text{TLBI RVAE1\{}{, <Xt>}\}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b01}</td>
<td>\texttt{0b000}</td>
<td>\texttt{0b1000}</td>
<td>\texttt{0b0110}</td>
<td>\texttt{0b001}</td>
</tr>
</tbody>
</table>

if \texttt{PSTATE.EL} == \texttt{EL0} then
    UNDEFINED;
elseif \texttt{PSTATE.EL} == \texttt{EL1} then
    if \texttt{EL2Enabled()} &\& \texttt{HCR_EL2.TTLB} == '1' then
        \texttt{AArch64.SystemAccessTrap(EL2, 0x18)};
    elseif \texttt{EL2Enabled()} &\& (!HaveEL(EL3) || \texttt{SCR_EL3.FGEn} == '1') &\& \texttt{HFGITR_EL2.TLBIRVAE1} == '1' then
        \texttt{AArch64.SystemAccessTrap(EL2, 0x18)};
    elseif \texttt{HCR_EL2.FB} == '1' then
        if \texttt{IsFeatureImplemented(\texttt{FEAT_XS})} &\& \texttt{HCRX_EL2.FnXS} == '1' then
            \texttt{TLBI RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel Any, TLBIExcludeXS, X[t]);}
        else
            \texttt{TLBI RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel Any, TLBIExcludeXS, X[t]);}
        endif
    elseif \texttt{PSTATE.EL} == \texttt{EL2} then
        if \texttt{HCR_EL2.<E2H,TGE>} == '11' then
            \texttt{TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any, TLBIAllAttr, X[t]);}
        else
            \texttt{TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any, TLBIAllAttr, X[t]);}
        endif
    elseif \texttt{PSTATE.EL} == \texttt{EL3} then
        if \texttt{HCR_EL2.<E2H,TGE>} == '11' then
            \texttt{TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any, TLBIAllAttr, X[t]);}
        else
            \texttt{TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any, TLBIAllAttr, X[t]);}
        endif
    endif
else
    if \texttt{IsFeatureImplemented(\texttt{FEAT_XS})} &\& \texttt{HCRX_EL2.FnXS} == '1' then
        \texttt{TLBI RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel Any, TLBIExcludeXS, X[t]);}
    else
        \texttt{TLBI RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel Any, TLBIExcludeXS, X[t]);}
    endif
endif

\textbf{TLBI RVAE1NXS\{}{, <Xt>}\}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

TLBI RVAE1NXS
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (SCR_EL2.FGTEn == '1') && HCR_EL2.FGTxnXS == '0' &&
    HFGITR_EL2.TLBIRVAE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTxnXS == '0' &&
    HFGITR_EL2.TLBIRVAE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' then
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
  elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
endif

TLBI RVAE1IS, TLBI RVAE1ISNXS, TLB Range Invalidate by VA, EL1, Inner Shareable

The TLBI RVAE1IS, TLBI RVAE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3 NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula\[BaseADDR <= VA < BaseADDR + ((NUM +1)*2^{5 SCALE} +1) * Translation_Granule_Size).\]

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
TLBI RVAE1IS, TLBI RVAE1ISNXS, TLB Range Invalidate by VA, EL1, Inner Shareable

- If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000.
- If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAE1IS, TLBI RVAE1ISNXS are UNDEFINED.

**Attributes**

TLBI RVAE1IS, TLBI RVAE1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVAE1IS, TLBI RVAE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>ASID</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td>32</td>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.

**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this</td>
</tr>
<tr>
<td></td>
<td>field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAE1IS, TLBI RVAE1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI RVAE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTL == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1IS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
        else
            TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
        endif
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLB_RA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
        TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLB_RA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
        TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    endif
else
    if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
    elsif PSTATE.EL == EL0 then
        UNDEFINED;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TTL == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.TTLIS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1IS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
                TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
            else
                TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
            endif
        endif
    endif
endif
TLB RVAE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTL == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1IS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
        else
            TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
        endif
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLB_RA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
        TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLB_RA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
        TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
    endif
else
    if !IsFeatureImplemented(FEAT_XS) then
        UNDEFINED;
    elsif PSTATE.EL == EL0 then
        UNDEFINED;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.TTL == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && HCR_EL2.TTLIS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1IS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
                TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
            else
                TLB_RA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBIExcludeXS, X[t]);
            endif
        endif
    endif
endif
TLB RVAE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
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<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
The TLBI RVAE1OS, TLBI RVAE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.E2H, TGE is not {1, 1}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.E2H, TGE is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)2^{(5 \times \text{SCALE} + 1)} \times \text{Translation	extunderscore Granule	extunderscore Size})\].

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 0000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 000000000000.
- For the 64K translation granule:
If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000000.

Configuration

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVAE1OS, TLBI RVAE1OSNXS are **UNDEFINED**.

Attributes

TLBI RVAE1OS, TLBI RVAE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAE1OS, TLBI RVAE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td>TG</td>
</tr>
<tr>
<td>61</td>
<td>SCALE</td>
</tr>
<tr>
<td>60</td>
<td>NUM</td>
</tr>
<tr>
<td>59</td>
<td>TTL</td>
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<td>58</td>
<td>BaseADDR</td>
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<td></td>
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<tr>
<td>32</td>
<td>BaseADDR</td>
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<td>31</td>
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<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation granule,</td>
</tr>
<tr>
<td></td>
<td>this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

- When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
- When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

- When using a 4KB translation granule, this field is BaseADDR[48:12].
- When using a 16KB translation granule, this field is BaseADDR[50:14].
- When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAE1OS, TLBI RVAE1OSNXS instruction**

Accesses to this instruction use the following encodings:

```
TLBI RVAE1OS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any, TLBIExcludeXS, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  end
end

TLBI RVAE1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b0001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVAE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any, TLBIExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any, TLBIExcludeXS, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBIAllAttr, X[t]);
  end
end
The TLBI RVAE2, TLBI RVAE2NXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula
  \[ \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5\times\text{SCALE} + 1)} \times \text{Translation Granule Size}) \], using the EL2 or EL2&0 translation regime.
- If \( \text{HCR\_EL2}.E2H = 0 \), the entry is from any level of the translation table walk.
- If \( \text{HCR\_EL2}.E2H = 1 \), one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAE2, TLBI RVAE2NXS are **UNDEFINED**.
Attributes

TLBI RVAE2, TLBI RVAE2NXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAE2, TLBI RVAE2NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td></td>
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<tr>
<td>61</td>
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<tr>
<td>52</td>
<td></td>
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<tr>
<td>51</td>
<td></td>
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<tr>
<td>50</td>
<td></td>
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<tr>
<td>49</td>
<td></td>
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<tr>
<td>48</td>
<td></td>
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<tr>
<td>47</td>
<td></td>
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<tr>
<td>46</td>
<td></td>
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<td>45</td>
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<td>37</td>
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<tr>
<td>36</td>
<td></td>
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<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
### TTL

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field as</td>
</tr>
<tr>
<td></td>
<td>0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

### BaseADDR, bits [36:0]

**When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:**

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

**Otherwise:**

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

### Executing the TLBI RVAE2, TLBI RVAE2NXS instruction

Accesses to this instruction use the following encodings:

**TLBI RVAE2{, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b10</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
    TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any,
    TLBI_AllAttr, X[t]);
selsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
elsif HCR_EL2.E2H == '1' then
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBILevel_Any,
  TLBI_AllAttr, X[t]);
else
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any,
  TLBI_AllAttr, X[t]);
```
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[][], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
The TLBI RVAE2IS, TLBI RVAE2ISNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula $[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation\_Granule\_Size})]$, using the EL2 or EL2&0 translation regime.
- If $HCR\_EL2.E2H == 0$, the entry is from any level of the translation table walk.
- If $HCR\_EL2.E2H == 1$, one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAE2IS, TLBI RVAE2ISNXS are **UNDEFINED**.
Attributes

TLBI RVAE2IS, TLBI RVAE2ISNXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAE2IS, TLBI RVAE2ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td>TG</td>
</tr>
<tr>
<td>61</td>
<td>SCALE</td>
</tr>
<tr>
<td>60</td>
<td>NUM</td>
</tr>
<tr>
<td>59</td>
<td>TTL</td>
</tr>
<tr>
<td>58</td>
<td>BaseADDR</td>
</tr>
<tr>
<td>57</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
</tr>
<tr>
<td>55</td>
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<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
### TTL

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field</td>
</tr>
<tr>
<td></td>
<td>as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

### BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

### Executing the TLBI RVAE2IS, TLBI RVAE2ISNXS instruction

Accesses to this instruction use the following encodings:

```plaintext
TLBI RVAE2IS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
             TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any,
             TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elseif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_Inner, TLBILevel_Any,
             TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any,
             TLBI_AllAttr, X[t]);
```
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Inner,
    TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
elsif HCR_EL2.E2H == '1' then
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any,
  TLBI_ExcludeXS, X[t]);
else
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any,
  TLBI_ExcludeXS, X[t]);
The TLBI RVAE2OS, TLBI RVAE2OSNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula \[ BaseADDR \leq VA < BaseADDR + ((NUM +1)*2^{(5\times SCALE +1)} \times Translation\_Granule\_Size) \], using the EL2 or EL2&0 translation regime.
- If \texttt{HCR\_EL2} \_E2H == 0, the entry is from any level of the translation table walk.
- If \texttt{HCR\_EL2} \_E2H == 1, one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is UNPREDICTABLE when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT\_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT\_TLBIRANGE is implemented and FEAT\_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVAE2OS, TLBI RVAE2OSNXS are UNDEFINED.
Attributes

TLBI RVAE2OS, TLBI RVAE2OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI RVAE2OS, TLBI RVAE2OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASID</td>
<td>[63:48]</td>
<td>Translation Granule Size</td>
</tr>
<tr>
<td>TG</td>
<td>[47:46]</td>
<td>Translation Granule Size</td>
</tr>
<tr>
<td>SCALE</td>
<td>[45:44]</td>
<td>Translation Granule Size</td>
</tr>
<tr>
<td>NUM</td>
<td>[43:39]</td>
<td>Translation Granule Size</td>
</tr>
<tr>
<td>TTL</td>
<td>[38:37]</td>
<td>Translation Granule Size</td>
</tr>
<tr>
<td>BaseADDR</td>
<td></td>
<td>Translation Granule Size</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.

**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAE2OS, TLBI RVAE2OSNXS instruction**

Accesses to this instruction use the following encodings:

TLBI RVAE2OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE_EL == EL0 then
  UNDEFINED;
elsif PSTATE_EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE_EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Outer, TLBI_Level_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBI_Level_Any, TLBI_AllAttr, X[t]);
elsif PSTATE_EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBI_Level_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBI_Level_Any, TLBI_AllAttr, X[t]);
TLBI RVAE20SNXS\{, \langle Xt \rangle \}\}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    if PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
            TLBILevel_Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Any,
            TLBI_ExcludeXS, X[t]);
    elsif PSTATE.EL == EL3 then
        if !EL2Enabled() then
            UNDEFINED;
        elsif HCR_EL2.E2H == '1' then
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer,
            TLBILevel_Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Any,
            TLBI_ExcludeXS, X[t]);
```
The TLBI RVAE3, TLBI RVAE3NXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula $\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + (((\text{NUM} + 1) \times 2^{\text{5*SCALE} + 1}) \times \text{Translation\_Granule\_Size})$.

The invalidation applies to the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAE3, TLBI RVAE3NXS are **UNDEFINED**.

**Attributes**

TLBI RVAE3, TLBI RVAE3NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVAE3, TLBI RVAE3NXS input value bit assignments are:
Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field as</td>
</tr>
<tr>
<td></td>
<td>0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAE3, TLBI RVAE3NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI RVAE3{, <Xt>}**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);

**TLBI RVAE3NXS{, <Xt>}**

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
```

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
TLBI RVAE3IS, TLBI RVAE3ISNXS, TLB Range Invalidate by VA, EL3, Inner Shareable

The TLBI RVAE3IS, TLBI RVAE3ISNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula [BaseADDR <= VA < BaseADDR + ((NUM +1)*2[(5*SCALE +1) * Translation_Granule_Size])].

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **unpredictable** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVAE3IS, TLBI RVAE3ISNXS are **undefined**.

**Attributes**

TLBI RVAE3IS, TLBI RVAE3ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVAE3IS, TLBI RVAE3ISNXS input value bit assignments are:
Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

- When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
- When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

- When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is `BaseADDR[50:14]`.
When using a 64KB translation granule, this field is `BaseADDR[52:16]`.

**Executing the TLBI RVAE3IS, TLBI RVAE3ISNXS instruction**

Accesses to this instruction use the following encodings:

```plaintext
TLBI RVAE3IS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if `PSTATE.EL == EL0` then
  UNDEFINED;
elsif `PSTATE.EL == EL1` then
  UNDEFINED;
elsif `PSTATE.EL == EL2` then
  UNDEFINED;
elsif `PSTATE.EL == EL3` then
  TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);

```plaintext
TLBI RVAE3ISNXS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if `!IsFeatureImplemented(FEAT_XS)` then
  UNDEFINED;
elsif `PSTATE.EL == EL0` then
  UNDEFINED;
elsif `PSTATE.EL == EL1` then
  UNDEFINED;
elsif `PSTATE.EL == EL2` then
  UNDEFINED;
elsif `PSTATE.EL == EL3` then
  TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
The TLBI RVAE3OS, TLBI RVAE3OSNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula \(\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation Granule Size})\).

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVAE3OS, TLBI RVAE3OSNXS are **UNDEFINED**.

**Attributes**

TLBI RVAE3OS, TLBI RVAE3OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVAE3OS, TLBI RVAE3OSNXS input value bit assignments are:
Bits [63:48]

Reserved. RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16K translation granule,</td>
</tr>
<tr>
<td></td>
<td>this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVAE3OS, TLBI RVAE3OSNXS instruction**

Accesses to this instruction use the following encodings:

TLBI RVAE3OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);

TLBI RVAE3OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
The TLBI RVALE1, TLBI RVALE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.E2H, TGE is not \{1, 1\}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.E2H, TGE is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1) \times \text{TranslationGranuleSize}})\].

The invalidation applies to the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL=01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL=10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL=10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL=01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL=10 and BaseADDR[28:16] is not equal to 0000000000000.

For more information about the architectural requirements for this System instruction, see 'Invalidation of TLB entries from stage 2 translations'.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.
**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVALE1, TLBI RVALE1NXS are **UNDEFINED**.

**Attributes**

TLBI RVALE1, TLBI RVALE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE1, TLBI RVALE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-48</td>
<td>ASID</td>
<td>Value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction. Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field. If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.</td>
</tr>
<tr>
<td>47-46</td>
<td>TG</td>
<td>Translation granule size.</td>
</tr>
<tr>
<td>45-44</td>
<td>SCALE</td>
<td>The exponent element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>43-39</td>
<td>NUM</td>
<td>The base element of the calculation that is used to produce the upper range.</td>
</tr>
<tr>
<td>38-37</td>
<td>TTL</td>
<td>TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>BaseADDR</td>
<td></td>
</tr>
<tr>
<td>TTL</td>
<td>Meaning</td>
<td></td>
</tr>
<tr>
<td>------</td>
<td>-------------------------------------------------------------------------</td>
<td></td>
</tr>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
<td></td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation granule,</td>
<td></td>
</tr>
<tr>
<td></td>
<td>this value is reserved and hardware should treat this field as 0b00.</td>
<td></td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
<td></td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
<td></td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVALE1, TLBI RVALE1NXS instruction**

Accesses to this instruction use the following encodings:

TLBI _RVALE1{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVALE1 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
                TLBI_Level_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
                TLBI_Level_Last, TLBI_AllAttr, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None,
                TLBI_Level_Last, TLBI_AllAttr, X[t]);
        endif
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
                TLBI_Level_Last, TLBI_AllAttr, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Last,
                TLBI_AllAttr, X[t]);
        endif
    elsif PSTATE.EL == EL3 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
                TLBI_Level_Last, TLBI_AllAttr, X[t]);
        else
            TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_Level_Last,
                TLBI_AllAttr, X[t]);
        endif
    endif
endif

TLBI RVALE1NXS{, <Xt>}
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBRVALE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.FB == '1' then
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
The TLBI RVALE1IS, TLBI RVALE1ISNXS, TLB Range Invalidate by VA, Last level, EL1, Inner Shareable characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \( \{1, 1\} \), the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \( \{1, 1\} \), the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)^2(5\times\text{SCALE} + 1) \times \text{Translation_Granule_Size})]\).

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 0000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000000000000000.
If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBRANGE is implemented. Otherwise, direct accesses to TLBI RVALE1IS, TLBI RVALE1ISNXS are **UNDEFINED**.

**Attributes**

TLBI RVALE1IS, TLBI RVALE1ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE1IS, TLBI RVALE1ISNXS input value bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| ASID   | TG     | SCALE  | NUM    | TTL    | BaseADDR |
| 31     | 30     | 29     | 28     | 27     | 26     | 25     | 24     | 23     | 22     | 21     | 20     | 19     | 18     | 17     | 16     | 15     | 14     | 13     | 12     | 11     | 10     | 9      | 8      | 7      | 6      | 5      | 4      | 3      | 2      | 1      | 0      |

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.
TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RVALE1IS, TLBI RVALE1ISNXS instruction

Accesses to this instruction use the following encodings:

TLBI RVALE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVALE1IS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end if;
else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_AllAttr, X[t]);
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_level_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_AllAttr, X[t]);
    end if;
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_level_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_AllAttr, X[t]);
    end if;
end if;

TLBI RVALE1ISNXS(, <Xt>)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVALE1IS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        AArch64.SystemAccessTrap(EL2, 0x18);
    end if;
else
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    end if;
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_level_Last, TLBI_ExcludeXS, X[t]);
    end if;
end if;
The TLBI RVALE1OS, TLBI RVALE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3.NS`:
  - If `HCR_EL2.{E2H, TGE}` is not `{1, 1}`, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If `HCR_EL2.{E2H, TGE}` is `{1, 1}`, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.
- The entry is within the address range determined by the formula \[ \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1)2^{(5\times\text{SCALE} + 1)} \times \text{Translation\_Granule\_Size}) \].

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if `SCR_EL3.EEL2==1`, then:

- A PE with `SCR_EL3.EEL2==1` is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with `SCR_EL3.EEL2==0`.
- A PE with `SCR_EL3.EEL2==0` is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with `SCR_EL3.EEL2==1`.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000.
If TTL==10 and BaseADDR[28:16] is not equal to 0000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVALE1OS, TLBI RVALE1OSNXS are **UNDEFINED**.

**Attributes**

TLBI RVALE1OS, TLBI RVALE1OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE1OS, TLBI RVALE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td>TG</td>
</tr>
<tr>
<td>61</td>
<td>SCALE</td>
</tr>
<tr>
<td>60</td>
<td>NUM</td>
</tr>
<tr>
<td>59</td>
<td>TTL</td>
</tr>
<tr>
<td>58</td>
<td>BaseADDR</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TG, bits [47:46]**

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

**SCALE, bits [45:44]**

The exponent element of the calculation that is used to produce the upper range.

**NUM, bits [43:39]**

The base element of the calculation that is used to produce the upper range.
**TTL, bits [38:37]**

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

**BaseADDR, bits [36:0]**

When FEAT_LPA2 is implemented and TCR_EL1.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].

When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVALE1OS, TLBI RVALE1OSNXS instruction**

Accesses to this instruction use the following encodings:

TLBI RVALE1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b00</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVALE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
    endif
  endif
else
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIRVALE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
      TLBI_RVA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
    endif
  endif
endif

TLBI RVALE1OSNXS{}, <Xt>
The TLBI RVALE2, TLBI RVALE2NXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula 
  \[ \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM}+1) \times 2^{(\text{SCALE}+1)} \times \text{Translation_Granule_Size}) \] using the EL2 or EL2&0 translation regime.
- If \text{HCR_EL2}.E2H == 0, the entry is from the final level of the translation table walk.
- If \text{HCR_EL2}.E2H == 1, one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to the PE that executes this System instruction. The range of addresses invalidated is UNPREDICTABLE when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 00000000000000000000000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined. Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete. The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVALE2, TLBI RVALE2NXS are UNDEFINED.

**Attributes**

TLBI RVALE2, TLBI RVALE2NXS is a 64-bit System instruction.
Field descriptions

The TLBI RVALE2, TLBI RVALE2NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>ASID</th>
<th>TG</th>
<th>SCALE</th>
<th>NUM</th>
<th>TTL</th>
<th>BaseADDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
</tr>
<tr>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
</tr>
<tr>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
</tr>
<tr>
<td>45</td>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
</tr>
<tr>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
</tr>
<tr>
<td>33</td>
<td>32</td>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not</td>
</tr>
<tr>
<td></td>
<td>implemented, when using a 16KB translation granule, this value is reserved and hardware</td>
</tr>
<tr>
<td></td>
<td>should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>
BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RVALE2, TLBI RVALE2NXS instruction

Accesses to this instruction use the following encodings:

TLBI RVALE2{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
elsif HCR_EL2.E2H == '1' then
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
  TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI RVALE2NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
    TLBLevel_Last, TLBI ExcludeXS, X[t]);
  else
    TLBI RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBLevel_Last,
    TLBI ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBLevel_Last,
    TLBI ExcludeXS, X[t]);
  else
    TLBI RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBLevel_Last,
    TLBI ExcludeXS, X[t]);

TLBI RVALE2IS, TLBI RVALE2ISNXS, TLB Range Invalidate by VA, Last level, EL2, Inner Shareable

The TLBI RVALE2IS, TLBI RVALE2ISNXS characteristics are:

### Purpose

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula \[ \text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times (5^{\text{SCALE}} + 1) \times \text{Translation_Granule_Size}) \] using the EL2 or EL2&0 translation regime.
- If \( \text{HCR}_{\text{EL2}}.E2H == 0 \), the entry is from the final level of the translation table walk.
- If \( \text{HCR}_{\text{EL2}}.E2H == 1 \), one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If \( \text{FEAT}_{\text{XS}} \) is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when \( \text{FEAT}_{\text{TBLIRANGE}} \) is implemented. Otherwise, direct accesses to TLBI RVALE2IS, TLBI RVALE2ISNXS are **UNDEFINED**.

### Attributes

TLBI RVALE2IS, TLBI RVALE2ISNXS is a 64-bit System instruction.
Field descriptions

The TLBI RVALE2IS, TLBI RVALE2ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-62</td>
<td>ASID</td>
</tr>
<tr>
<td>61-60</td>
<td>TG</td>
</tr>
<tr>
<td>59-58</td>
<td>SCALE</td>
</tr>
<tr>
<td>57-48</td>
<td>NUM</td>
</tr>
<tr>
<td>47-37</td>
<td>TTL</td>
</tr>
<tr>
<td>36-32</td>
<td>BaseADDR</td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>
BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b0.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RVALE2IS, TLBI RVALE2ISNXS instruction

Accesses to this instruction use the following encodings:

TLBI RVALE2IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
elsif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI RVALE2ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability.Inner,
                  TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability.Inner, TLBILevel.Last,
                  TLBI_ExcludeXS, X[t]);
    end if
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elseif HCR_EL2.E2H == '1' then
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability.Inner,
                  TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
        TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability.Inner, TLBILevel.Last,
                  TLBI_ExcludeXS, X[t]);
    end if
end if
The TLBI RVALE2OS, TLBI RVALE2OSNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA in the specified range determined by the formula
  \[ \text{Base ADDR} \leq \text{VA} < \text{Base ADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation Granule Size}) \] using the EL2 or EL2&0 translation regime.
- If `HCR_EL2.E2H == 0`, the entry is from the final level of the translation table walk.
- If `HCR_EL2.E2H == 1`, one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 00000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVALE2OS, TLBI RVALE2OSNXS are **UNDEFINED**.

**Attributes**

TLBI RVALE2OS, TLBI RVALE2OSNXS is a 64-bit System instruction.
Field descriptions

The TLBI RVALE2OS, TLBI RVALE2OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit Number</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td>TG</td>
</tr>
<tr>
<td>61</td>
<td>SCALE</td>
</tr>
<tr>
<td>60</td>
<td>NUM</td>
</tr>
<tr>
<td>59</td>
<td>TTL</td>
</tr>
<tr>
<td>58</td>
<td>BaseADDR</td>
</tr>
<tr>
<td>57</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td></td>
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<td>54</td>
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<td>52</td>
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<td>51</td>
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<td>50</td>
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<td>48</td>
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<td>44</td>
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<td>41</td>
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<td>32</td>
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<td>31</td>
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<td>25</td>
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<td>24</td>
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<tr>
<td>14</td>
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<tr>
<td>13</td>
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<tr>
<td>12</td>
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</tr>
<tr>
<td>11</td>
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</tr>
<tr>
<td>10</td>
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<td>9</td>
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<td>8</td>
<td></td>
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<tr>
<td>7</td>
<td></td>
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<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

When HCR_EL2.E2H == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>
BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL2.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RVALE2OS, TLBI RVALE2OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI RVALE2OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI RVALE2OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_RVA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
The TLBI RVALE3, TLBI RVALE3NXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula \([\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation_Granule_Size})]\).

The invalidation applies to the PE that executes this System instruction. The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 00000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVALE3, TLBI RVALE3NXS are **UNDEFINED**.

**Attributes**

TLBI RVALE3, TLBI RVALE3NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE3, TLBI RVALE3NXS input value bit assignments are:
Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this</td>
</tr>
<tr>
<td></td>
<td>field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.
When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].

When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVALE3, TLBI RVALE3NXS instruction**

Accesses to this instruction use the following encodings:

**TLBI RVALE3{}, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   UNDEFINED;
elsif PSTATE.EL == EL2 then
   UNDEFINED;
elsif PSTATE.EL == EL3 then
   TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Last, TLBI_AllAttr, X[t]);

**TLBI RVALE3NXS{}, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0110</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
   UNDEFINED;
elsif PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   UNDEFINED;
elsif PSTATE.EL == EL2 then
   UNDEFINED;
elsif PSTATE.EL == EL3 then
   TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
The TLBI RVALE3IS, TLBI RVALE3ISNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula \[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation Granule Size})\].

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is UNPREDICTABLE when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 00000000.
- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.
- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented. Otherwise, direct accesses to TLBI RVALE3IS, TLBI RVALE3ISNXS are UNDEFINED.

**Attributes**

TLBI RVALE3IS, TLBI RVALE3ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE3IS, TLBI RVALE3ISNXS input value bit assignments are:
Bits [63:48]

Reserved, RES0.

TG, bits [47:46]

Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]

The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]

The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]

TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries. If FEAT_LPA2 is not implemented, when using a 16KB translation granule, this value is reserved and hardware should treat this field as 0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]

When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:

The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:

The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

Executing the TLBI RVALE3IS, TLBI RVALE3ISNXS instruction

Accesses to this instruction use the following encodings:

**TLBI RVALE3IS{, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);

**TLBI RVALE3ISNXS{, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
The TLBI RVALE3OS, TLBI RVALE3OSNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.
- The entry is within the address range determined by the formula \[\text{BaseADDR} \leq \text{VA} < \text{BaseADDR} + ((\text{NUM} + 1) \times 2^{(5 \times \text{SCALE} + 1)} \times \text{Translation Granule Size})\].

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

The range of addresses invalidated is **UNPREDICTABLE** when:

- For the 4K translation granule:
  - If TTL==01 and BaseADDR[29:12] is not equal to 000000000000000000.
  - If TTL==10 and BaseADDR[20:12] is not equal to 000000000.

- For the 16K translation granule:
  - If TTL==10 and BaseADDR[24:14] is not equal to 0000000000.

- For the 64K translation granule:
  - If TTL==01 and BaseADDR[41:16] is not equal to 00000000000000000000000000.
  - If TTL==10 and BaseADDR[28:16] is not equal to 00000000000000.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIRANGE is implemented and FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI RVALE3OS, TLBI RVALE3OSNXS are **UNDEFINED**.

**Attributes**

TLBI RVALE3OS, TLBI RVALE3OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI RVALE3OS, TLBI RVALE3OSNXS input value bit assignments are:
Bits [63:48]  
Reserved, RES0.

TG, bits [47:46]  
Translation granule size.

<table>
<thead>
<tr>
<th>TG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b01</td>
<td>4K translation granule.</td>
</tr>
<tr>
<td>0b10</td>
<td>16K translation granule.</td>
</tr>
<tr>
<td>0b11</td>
<td>64K translation granule.</td>
</tr>
</tbody>
</table>

The instruction takes a translation granule size for the translations that are being invalidated. If the translations used a different translation granule size than the one being specified, then the architecture does not require that the instruction invalidates any entries.

SCALE, bits [45:44]  
The exponent element of the calculation that is used to produce the upper range.

NUM, bits [43:39]  
The base element of the calculation that is used to produce the upper range.

TTL, bits [38:37]  
TTL Level hint. The TTL hint is only guaranteed to invalidate entries in the range that match the level described by the TTL hint.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The entries in the range can be using any level for the translation</td>
</tr>
<tr>
<td></td>
<td>table entries.</td>
</tr>
<tr>
<td>0b01</td>
<td>All entries to invalidate are Level 1 translation table entries.</td>
</tr>
<tr>
<td></td>
<td>If FEAT_LPA2 is not implemented, when using a 16KB translation</td>
</tr>
<tr>
<td></td>
<td>granule, this value is reserved and hardware should treat this field as</td>
</tr>
<tr>
<td></td>
<td>0b00.</td>
</tr>
<tr>
<td>0b10</td>
<td>All entries to invalidate are Level 2 translation table entries.</td>
</tr>
<tr>
<td>0b11</td>
<td>All entries to invalidate are Level 3 translation table entries.</td>
</tr>
</tbody>
</table>

BaseADDR, bits [36:0]  
When FEAT_LPA2 is implemented and TCR_EL3.DS == 1:  
The starting address for the range of the maintenance instructions. This field is BaseADDR[52:16] for all translation granules.

When using a 4KB translation granule, BaseADDR[15:12] is treated as 0b0000.

When using a 16KB translation granule, BaseADDR[15:14] is treated as 0b00.

Otherwise:  
The starting address for the range of the maintenance instruction.

When using a 4KB translation granule, this field is BaseADDR[48:12].
When using a 16KB translation granule, this field is BaseADDR[50:14].
When using a 64KB translation granule, this field is BaseADDR[52:16].

**Executing the TLBI RVALE3OS, TLBI RVALE3OSNXS instruction**

Accesses to this instruction use the following encodings:

**TLBI RVALE3OS{}, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
   TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);

**TLBI RVALE3OSNXS{}, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
UNDEFINED;
elsif PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
UNDEFINED;
elsif PSTATE.EL == EL2 then
UNDEFINED;
elsif PSTATE.EL == EL3 then
   TLBI_RVA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
TLBI VAAE1, TLBI VAAE1NXS, TLB Invalidate by VA, All ASID, EL1

The TLBI VAAE1, TLBI VAAE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3`.NS:
  - If `HCR_EL2.{E2H, TGE}` is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If `HCR_EL2.{E2H, TGE}` is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAAE1, TLBI VAAE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAAE1, TLBI VAAE1NXS input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | TTL | VA[55:12] |

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|

Bits [63:48]

Reserved, RES0.
**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAAE1, TLBI VAAE1NXS instruction**

Accesses to this instruction use the following encodings:

TLBI VAAE1{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
</table>

Page 1777
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVAE1 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
                TLBILevel Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_VAA(Regime_EL10, VMID[], Shareability_Inner,
                TLBILevel Any, TLBI_AllAttr, X[t]);
        end if;
    else
        if IsFeatureImplemented(FEAT_XS) && HCR_EL2.FnXS == '1' then
            TLBI_VAA(Regime_EL10, VMID[], Shareability_Inner,
                TLBILevel Any, TLBI_ExcludeXS, X[t]);
        else
            TLBI_VAA(Regime_EL10, VMID[], Shareability_Inner,
                TLBILevel Any, TLBI_AllAttr, X[t]);
        end if;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAA(Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any,
            TLBI_AllAttr, X[t]);
    else
        TLBI_VAA(Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any,
            TLBI_AllAttr, X[t]);
    end if;
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAA(Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any,
            TLBI_AllAttr, X[t]);
    else
        TLBI_VAA(Regime_EL20, VMID_NONE, Shareability_None, TLBILevel Any,
            TLBI_AllAttr, X[t]);
    end if;
else
    TLBI_VAAE1NXS{, <Xt>}
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
      HFGITR_EL2.TLIBVAAE1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
  elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
  elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
TLBI VAAE1IS, TLBI VAAE1ISNXS, TLB Invalidate by VA, All ASID, EL1, Inner Shareable

The TLBI VAAE1IS, TLBI VAAE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAAE1IS, TLBI VAAE1ISNXS is a 64-bit System instruction.
Field descriptions

The TLBI VAAE1IS, TLBI VAAE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-48</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>47-44</td>
<td>When FEAT_TTL is implemented:</td>
</tr>
<tr>
<td>43-40</td>
<td>Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.</td>
</tr>
<tr>
<td>47-44</td>
<td>TTL, bits [47:44]</td>
</tr>
<tr>
<td>47-44</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>47-44</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td>47-44</td>
<td>0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>47-44</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td>47-44</td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>47-44</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td>47-44</td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td>47-44</td>
<td>0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
• Where a 16KB translation granule is being used, bits \([1:0]\) of this field are RES0 and ignored when the instruction is executed, because VA\([13:12]\) have no effect on the operation of the instruction.

• Where a 64KB translation granule is being used, bits \([3:0]\) of this field are RES0 and ignored when the instruction is executed, because VA\([15:12]\) have no effect on the operation of the instruction.

## Executing the TLBI VAAE1IS, TLBI VAAE1ISNXS instruction

Accesses to this instruction use the following encodings:

### TLBI VAAE1IS\(\{, <Xt>\}\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVAAE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
else
  TLBI VAAE1ISNXS\(\{, <Xt>\}\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVAE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '1' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBILevel_Any, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '1' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
    TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
    TLBI_ExcludeXS, X[t]);
TLBI VAAE1OS, TLBI VAAE1OSNXS, TLB Invalidate by VA, All ASID, EL1, Outer Shareable

The TLBI VAAE1OS, TLBI VAAE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3_NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VAAE1OS, TLBI VAAE1OSNXS are **UNDEFINED**.
Attributes

TLBI VAAE1OS, TLBI VAAE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI VAAE1OS, TLBI VAAE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
</tr>
<tr>
<td>61</td>
<td>TTL</td>
</tr>
<tr>
<td>60</td>
<td>VA[55:12]</td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.
The treatment of the low-order bits of this field depends on the translation granularity size, as follows:

- Where a 4KB translation granularity is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granularity is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granularity is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAAE1OS, TLBI VAAE10SNXS instruction**

Accesses to this instruction use the following encodings:

**TLBI VAAE1OS{}, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVAAE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_ExcludeXS, X[t]);
  elsif TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
else
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
  elsif TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);
  elsif TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Any, TLBI_AllAttr, X[t]);

**TLBI VAAE10SNXS{}, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLB0S == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!(HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
      HFGITR_EL2.TLBVAE1OS == '1') then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
      TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
      TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any,
      TLBI_ExcludeXS, X[t]);
  endif
endif
TLBI VAALE1, TLBI VAALE1NXS, TLB Invalidate by VA, All ASID, Last level, EL1

The TLBI VAALE1, TLBI VAALE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3.NS`:
  - If `HCR_EL2.{E2H, TGE}` is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If `HCR_EL2.{E2H, TGE}` is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAALE1, TLBI VAALE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAALE1, TLBI VAALE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:62</td>
<td>RES0</td>
</tr>
<tr>
<td>61:51</td>
<td>TTL</td>
</tr>
<tr>
<td>50:42</td>
<td>VA[55:12]</td>
</tr>
<tr>
<td>31:0</td>
<td>VA[55:12]</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.
TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

Executing the TLBI VAALE1, TLBI VAALE1NXS instruction

Accesses to this instruction use the following encodings:

\[
\text{TLBI VAALE1}, \quad \langle \text{Xt} \rangle
\]

| op0 | op1 | CRn | CRm | op2 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCR_GT_EL2.TLBIVAAE1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_VAALE1(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBILevel_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBILevel_Last, TLBI_AllAttr, X[t]);
        end if
    else
        if IsFeatureImplemented(FEAT_XS) && HCR_EL2.FnXS == '1' then
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBILevel_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBILevel_Last, TLBI_AllAttr, X[t]);
        end if
    end if
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAALE1(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
        TLBILevel_Last, TLBI_VAALE1NXS, X[t]);
    else
        TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_None,
        TLBILevel_Last, TLBI_VAALE1NXS, X[t]);
    end if
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
        TLBILevel_Last, TLBI_VAALE1NXS, X[t]);
    else
        TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_None,
        TLBILevel_Last, TLBI_VAALE1NXS, X[t]);
    end if
end if

TLBI VAALE1NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(_FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCR_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVALE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    TLBI_VAA(EL2, SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(EL1, SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(EL2, SecurityStateAtEL(EL1), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(EL1, SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(EL2, SecurityStateAtEL(EL1), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VAA(EL1, SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif
The TLBI VAALE1IS, TLBI VAALE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3_NS:
  - If \( \text{HCR}_\text{EL2}.\{\text{E2H}, \text{TGE}\} \) is not \( \{1, 1\} \), the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If \( \text{HCR}_\text{EL2}.\{\text{E2H}, \text{TGE}\} \) is \( \{1, 1\} \), the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with \( \text{SCR}_\text{EL3}.\text{EEL2}==1 \) is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with \( \text{SCR}_\text{EL3}.\text{EEL2}==0 \).
- A PE with \( \text{SCR}_\text{EL3}.\text{EEL2}==0 \) is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with \( \text{SCR}_\text{EL3}.\text{EEL2}==1 \).
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAALE1IS, TLBI VAALE1ISNXS is a 64-bit System instruction.
Field descriptions

The TLBI VAALE1IS, TLBI VAALE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.

Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

### Executing the TLBI VAALE1IS, TLBI VAALE1ISNXS instruction

Accesses to this instruction use the following encodings:

**TLBI VAALE1IS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVAALE1IS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
        else
            TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
        endif
    endif
elseif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
    endif
elseif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
        TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);
    endif
endif
```

**TLBI VAALE1ISNXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLIBVAEALE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
      TLBIExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
      TLBILevel_Last, TLBIExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
      TLBIExcludeXS, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
      TLBILevel_Last, TLBIExcludeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
      TLBIExcludeXS, X[t]);
  endif
The TLBI VAALE1OS, TLBI VAALE1OSNXS characteristics are:

### Purpose

Invalidate cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

### Note

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

### Note

For the EL1&0 and EL2&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VAALE1OS, TLBI VAALE1OSNXS are UNDEFINED.
Attributes

TLBI VAALE1OS, TLBI VAALE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI VAALE1OS, TLBI VAALE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved</td>
</tr>
<tr>
<td>62</td>
<td>Reserved</td>
</tr>
<tr>
<td>61</td>
<td>Reserved</td>
</tr>
<tr>
<td>60</td>
<td>Reserved</td>
</tr>
<tr>
<td>59</td>
<td>Reserved</td>
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<tr>
<td>58</td>
<td>Reserved</td>
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<tr>
<td>57</td>
<td>Reserved</td>
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<td>Reserved</td>
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<tr>
<td>52</td>
<td>Reserved</td>
</tr>
<tr>
<td>51</td>
<td>TTL</td>
</tr>
<tr>
<td>50</td>
<td>Reserved</td>
</tr>
<tr>
<td>49</td>
<td>Reserved</td>
</tr>
<tr>
<td>48</td>
<td>Reserved</td>
</tr>
<tr>
<td>47</td>
<td>Reserved</td>
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<td>46</td>
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<td>44</td>
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<td>42</td>
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<td>40</td>
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<td>39</td>
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<td>36</td>
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<td>35</td>
<td>Reserved</td>
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<tr>
<td>34</td>
<td>Reserved</td>
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<tr>
<td>33</td>
<td>Reserved</td>
</tr>
<tr>
<td>32</td>
<td>Reserved</td>
</tr>
<tr>
<td>31</td>
<td>Bits[55:12]</td>
</tr>
<tr>
<td>30</td>
<td>Reserved</td>
</tr>
<tr>
<td>29</td>
<td>Reserved</td>
</tr>
<tr>
<td>28</td>
<td>Reserved</td>
</tr>
<tr>
<td>27</td>
<td>Reserved</td>
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<tr>
<td>26</td>
<td>Reserved</td>
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<td>22</td>
<td>Reserved</td>
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<td>21</td>
<td>Reserved</td>
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<td>20</td>
<td>Reserved</td>
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<td>19</td>
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<td>18</td>
<td>Reserved</td>
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<td>Reserved</td>
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<td>9</td>
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<td>7</td>
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<td>6</td>
<td>Reserved</td>
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<td>5</td>
<td>Reserved</td>
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<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
</tbody>
</table>
| 0b01xx  | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
| 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00.
| 0b01 : Level 1.
| 0b10 : Level 2.
| 0b11 : Level 3. |
| 0b10xx  | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
| 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
| 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00.
| 0b10 : Level 2.
| 0b11 : Level 3. |
| 0b11xx  | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
| 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
| 0b01 : Level 1.
| 0b10 : Level 2.
| 0b11 : Level 3. |

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.
The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

### Executing the TLBI VAALE1OS, TLBI VAALE1OSNXS instruction

Accesses to this instruction use the following encodings:

**TLBI VAALE1OS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```java
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLB0S == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVAALE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnxS == '1' then
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    elsif EL2Enabled() && HCR_EL2.TTLB == '1' then
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    elsif EL2Enabled() && HCR_EL2.FnxS == '1' then
      TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_IncludeXS, X[t]);
else
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
  elsif EL2Enabled() && HCR_EL2.TTLB0S == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
  if EL2Enabled() && HCR_EL2.FnxS == '1' then
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
  if PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
      TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
else
  if EL3Enabled() then
    if EL3Enabled() then
      if HCR_EL3.FGTEn == '1' then
        TLBI_VAA(SecurityStateAtEL(EL3), Regime_EL30, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
      else
        TLBI_VAA(SecurityStateAtEL(EL3), Regime_EL30, VMID[], Shareability_Outer, TLBILevel_Last, TLBI_AllAttr, X[t]);
    else
      TLBI VAALE1OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVALE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
      TLBI_ExcudeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
      TLBILevel_Last, TLBI_ExcudeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
      TLBI_ExcudeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VAA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
      TLBILevel_Last, TLBI_ExcudeXS, X[t]);
  else
    TLBI_VAA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Last,
      TLBI_ExcudeXS, X[t]);
The TLBI VAE1, TLBI VAE1NXS, TLB Invalidate by VA, EL1

The TLBI VAE1, TLBI VAE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not {1, 1}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAE1, TLBI VAE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE1, TLBI VAE1NXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ASID | TTL | VA[55:12] |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE1, TLBI VAE1NXS instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  end
else
  if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
else
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
end
else
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);

declare TLBI VAE1NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>

declare TLBI VAE1{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCR_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVAE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel:Any,
    TLBI_ExcludeXS, X[t]);
TLBI VAE1IS, TLBI VAE1ISNXS, TLB Invalidate by VA, EL1, Inner Shareable

The TLBI VAE1IS, TLBI VAE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.
Attributes

TLBI VAE1IS, TLBI VAE1ISNXS is a 64-bit System instruction.

Field descriptions

The TLBI VAE1IS, TLBI VAE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
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<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASID</td>
<td>TTL</td>
<td>VA[55:12]</td>
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<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, res0.
VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE1IS, TLBI VAE1ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI VAE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then UNDEFINED;
else if PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI ExcludeXS, X[t]);
    else
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI AllAttr, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI AllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI AllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI AllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any, TLBI AllAttr, X[t]);
end

TLBI VAE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elif PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
elif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
elif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
        HFGITR_EL2.TLBIVAE1IS == '1' then
            AArch64.SystemAccessTrap(EL2, 0x10);
else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
elif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any,
            TLBI_ExcludeXS, X[t]);
else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
elif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Any,
            TLBI_ExcludeXS, X[t]);
else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Any,
        TLBI_ExcludeXS, X[t]);
TLBI VAE1OS, TLBI VAE1OSNXS, TLB Invalidate by VA, EL1, Outer Shareable

The TLBI VAE1OS, TLBI VAE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VAE1OS, TLBI VAE1OSNXS are UNDEFINED.
Attributes

TLBI VAE1OS, TLBI VAE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI VAE1OS, TLBI VAE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>ASID</th>
<th>TTL</th>
<th>VA[55:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>59</td>
<td>58</td>
<td>57</td>
</tr>
<tr>
<td>55</td>
<td>54</td>
<td>53</td>
</tr>
<tr>
<td>51</td>
<td>50</td>
<td>49</td>
</tr>
<tr>
<td>47</td>
<td>46</td>
<td>45</td>
</tr>
<tr>
<td>43</td>
<td>42</td>
<td>41</td>
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<tr>
<td>39</td>
<td>38</td>
<td>37</td>
</tr>
<tr>
<td>35</td>
<td>34</td>
<td>33</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
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<tr>
<td>27</td>
<td>26</td>
<td>25</td>
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<tr>
<td>23</td>
<td>22</td>
<td>21</td>
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<tr>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>9</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, res0.
VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

Executing the TLBI VAE1OS, TLBI VAE1OSNXS instruction

Accesses to this instruction use the following encodings:

TLBI VAE105{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & HCR_EL2.TTLB0S == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HFGITR_EL2.TLBIVAE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) & HCRX_EL2.FnXS == '1' then
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBIExcludeXS, X[t]);
    else
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel_Any, TLBIAllAttr, X[t]);
    endif
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBIAllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBIAllAttr, X[t]);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBIAllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBIAllAttr, X[t]);
  endif
endif

TLBI VAE10SNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCR_EL2.FGTnXS == '0' &&
        HFGITR_EL2.TLBIVAE1OS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any,
        TLBI ExcludeXS, X[t]);
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID.NONE, Shareability_Outer, TLBILevel.Any,
        TLBI ExcludeXS, X[t]);
    else
        TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any,
        TLBI ExcludeXS, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any,
        TLBI ExcludeXS, X[t]);
    else
        TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBILevel.Any,
        TLBI ExcludeXS, X[t]);
    endif
TLBI VAE2, TLBI VAE2NXS, TLB Invalidate by VA, EL2

The TLBI VAE2, TLBI VAE2NXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be required to translate the specified VA using the EL2 or the EL2&0 translation regime.
- If $HCR_{EL2}.E2H == 0$, the entry is from any level of the translation table walk.
- If $HCR_{EL2}.E2H == 1$, one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to the PE that executes this System instruction.

If $FEAT_{XS}$ is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAE2, TLBI VAE2NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE2, TLBI VAE2NXS input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| ASID |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| TTL  |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VA[55:12] |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE2, TLBI VAE2NXS instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_AllAttr, X[t]);

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
TLBI VAE2IS, TLBI VAE2ISNXS, TLB Invalidate by VA, EL2, Inner Shareable

The TLBI VAE2IS, TLBI VAE2ISNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be required to translate the specified VA using the EL2 or the EL2&0 translation regime.
- If `HCR_EL2.E2H == 0`, the entry is from any level of the translation table walk.
- If `HCR_EL2.E2H == 1`, one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAE2IS, TLBI VAE2ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE2IS, TLBI VAE2ISNXS input value bit assignments are:

<p>| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|</p>
<table>
<thead>
<tr>
<th>ASID</th>
<th>TTL</th>
<th>VA[55:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TTL, bits [47:44]**

*When FEAT_TTL is implemented:*

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

*Otherwise:*

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE2IS, TLBI VAE2ISNXS instruction**

Accesses to this instruction use the following encodings:
TLBI VAE2IS{, \langle X \rangle}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \( PSTATE.EL == EL0 \) then
  UNDEFINED;
elsif \( PSTATE.EL == EL1 \) then
  if \( EL2Enabled() \) && \( HCR.EL2.NV == '1' \) then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif \( PSTATE.EL == EL2 \) then
  if \( HCR.EL2.E2H == '1' \) then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif \( PSTATE.EL == EL3 \) then
  if \( !EL2Enabled() \) then
    UNDEFINED;
  elsif \( HCR.EL2.E2H == '1' \) then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_AllAttr, X[t]);

TLBI VAE2ISNXS{, \langle X \rangle}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \( !IsFeatureImplemented(FEAT_XS) \) then
  UNDEFINED;
elsif \( PSTATE.EL == EL0 \) then
  UNDEFINED;
elsif \( PSTATE.EL == EL1 \) then
  if \( EL2Enabled() \) && \( HCR.EL2.NV == '1' \) then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif \( PSTATE.EL == EL2 \) then
  if \( HCR.EL2.E2H == '1' \) then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID_NONE, Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
elsif \( PSTATE.EL == EL3 \) then
  if \( !EL2Enabled() \) then
    UNDEFINED;
  elsif \( HCR.EL2.E2H == '1' \) then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Any, TLBI_ExcludeXS, X[t]);
TLBI VAE2OS, TLBI VAE2OSNXS, TLB Invalidate by VA, EL2, Outer Shareable

The TLBI VAE2OS, TLBI VAE2OSNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be required to translate the specified VA using the EL2 or the EL2&0 translation regime.
- If `HCR_EL2.E2H == 0`, the entry is from any level of the translation table walk.
- If `HCR_EL2.E2H == 1`, one of the following applies:
  - The entry is from a level of the translation table walk above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk and matches the specified ASID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If `FEAT_XS` is implemented, the nXS variant of this System instruction is defined. Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when `FEAT_TLBIOS` is implemented. Otherwise, direct accesses to TLBI VAE2OS, TLBI VAE2OSNXS are **UNDEFINED**.

**Attributes**

TLBI VAE2OS, TLBI VAE2OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE2OS, TLBI VAE2OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
<td></td>
</tr>
<tr>
<td>62</td>
<td>TTL</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>VA[55:12]</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>VA[55:12]</td>
<td></td>
</tr>
</tbody>
</table>

Page 1820
### ASID, bits [63:48]

When `HCR_EL2.E2H == 1`:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**Otherwise:**

Reserved, `RES0`.

### TTL, bits [47:44]

When `FEAT_TTL` is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is <code>RES0</code>.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: If <code>FEAT_LPA2</code> is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: If <code>FEAT_LPA2</code> is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, `RES0`.

### VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as `RES0`.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:
Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.

Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.

Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE2OS, TLBI VAE2OSNXS instruction**

Accesses to this instruction use the following encodings:

TLBI VAE2OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b01</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[1], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
elsif HCR_EL2.E2H == '1' then
  TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);
else
  TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[1], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);

TLBI VAE2OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b01</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBI.ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel.Any, TLBI.ExcludeXS, X[t]);
    endif
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elseif HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBILevel.Any, TLBI.ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel.Any, TLBI.ExcludeXS, X[t]);
    endif
endif

The TLBI VAE3, TLBI VAE3NXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VAE3, TLBI VAE3NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE3, TLBI VAE3NXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TTL | VA[55:12] |

**Bits [63:48]**

Reserved, RES0.

**TTL, bits [47:44]**

*When FEAT_TTL is implemented:*

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
### TTL | Meaning
---|---
0b00xx | No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL<1:0> is RES0.
0b01xx | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00.
0b01 : Level 1.
0b10 : Level 2.
0b11 : Level 3.
0b10xx | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00.
0b10 : Level 2.
0b11 : Level 3.
0b11xx | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
0b01 : Level 1.
0b10 : Level 2.
0b11 : Level 3.

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

### VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

### Executing the TLBI VAE3, TLBI VAE3NXS instruction

Accesses to this instruction use the following encodings:

TLBI VAE3{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Any,
    TLBI_AllAttr, X[t]);

TLBI VAE3NXS{}, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Any,
    TLBI_ExcludeXS, X[t]);
**TLBI VAE3IS, TLBI VAE3ISNXS, TLB Invalidate by VA, EL3, Inner Shareable**

The TLBI VAE3IS, TLBI VAE3ISNXS characteristics are:

### Purpose

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

There are no configuration notes.

### Attributes

TLBI VAE3IS, TLBI VAE3ISNXS is a 64-bit System instruction.

### Field descriptions

The TLBI VAE3IS, TLBI VAE3ISNXS input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     | TTL |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     |     | VA[55:12]|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [63:48]**

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
### TTL | Meaning
--- | ---
0b00xx | No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL<1:0> is RES0.
0b01xx | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00.
0b01 : Level 1.
0b10 : Level 2.
0b11 : Level 3.
0b10xx | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00.
0b10 : Level 2.
0b11 : Level 3.
0b11xx | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.
0b01 : Level 1.
0b10 : Level 2.
0b11 : Level 3.

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

### VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

### Executing the TLBI VAE3IS, TLBI VAE3ISNXS instruction

Accesses to this instruction use the following encodings:

```
TLBI VAE3IS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Any,
             TLBI_AllAttr, X[t]);

TLBI VAE3ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI_VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Any,
             TLBI_ExcludeXS, X[t]);
The TLBI VAE3OS, TLBI VAE3OSNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VAE3OS, TLBI VAE3OSNXS are UNDEFINED.

**Attributes**

TLBI VAE3OS, TLBI VAE3OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VAE3OS, TLBI VAE3OSNXS input value bit assignments are:

<p>| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|     |</p>
<table>
<thead>
<tr>
<th>RES0</th>
<th>TTL</th>
<th>VA[55:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VAE3OS, TLBI VAE3OSNXS instruction**

Accesses to this instruction use the following encodings:

```
TLBI VAE3OS{, <Xt>}  
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_AllAttr, X[t]);

TLBI VAE3OSNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elif PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  UNDEFINED;
elif PSTATE.EL == EL2 then
  UNDEFINED;
elif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Any, TLBI_ExcludeXS, X[t]);

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211

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The TLBI VALE1, TLBI VALE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \(\{1, 1\}\), the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \(\{1, 1\}\), the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE1, TLBI VALE1NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE1, TLBI VALE1NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>ASID</td>
</tr>
<tr>
<td>31-0</td>
<td>VA[55:12]</td>
</tr>
<tr>
<td></td>
<td>TTL</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TTL, bits [47:44]**

When **FEAT_TTL** is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If <strong>FEAT_LPA2</strong> is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If <strong>FEAT_LPA2</strong> is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE1, TLBI VALE1NXS instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVALE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBILevel_Last, TLBI_AllAttr, X[t]);
    end if;
  else
    if IsFeatureImplemented(FEAT_XS) && HCR_EL2.FnXS == '1' then
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBILevel_Last, TLBI_ExcludeXS, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBILevel_Last, TLBI_AllAttr, X[t]);
    end if;
  end if;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
      TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
      TLBI_AllAttr, X[t]);
  end if;
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
      TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
      TLBI_AllAttr, X[t]);
  end if;
end if;

---

TLBI VALE1NXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVALE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
endif
The TLBI VALE1IS, TLBI VALE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of `SCR_EL3 NS`:
  - If `HCR_EL2.E2H, TGE` is not (1, 1), the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If `HCR_EL2.E2H, TGE` is (1, 1), the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Note**

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if `SCR_EL3.EEL2==1`, then:

- A PE with `SCR_EL3.EEL2==1` is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with `SCR_EL3.EEL2==0`.
- A PE with `SCR_EL3.EEL2==0` is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with `SCR_EL3.EEL2==1`.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE1IS, TLBI VALE1ISNXS is a 64-bit System instruction.
Field descriptions

The TLBI VALE1IS, TLBI VALE1ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>ASID</th>
<th>TTL</th>
<th>VA[55:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>60</td>
<td>59</td>
<td>58</td>
</tr>
<tr>
<td>57</td>
<td>56</td>
<td>55</td>
</tr>
<tr>
<td>54</td>
<td>53</td>
<td>52</td>
</tr>
<tr>
<td>51</td>
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<td>49</td>
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<tr>
<td>48</td>
<td>47</td>
<td>46</td>
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<td>45</td>
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<td>42</td>
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<td>36</td>
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<td>33</td>
<td>32</td>
<td>31</td>
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<td>27</td>
<td>26</td>
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<td>21</td>
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<td>19</td>
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<td>18</td>
<td>17</td>
<td>16</td>
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<td>15</td>
<td>14</td>
<td>13</td>
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<td>12</td>
<td>11</td>
<td>10</td>
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<td>9</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.
If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

### Executing the TLBI VALE1IS, TLBI VALE1ISNXS instruction

Accesses to this instruction use the following encodings:

**TLBI VALE1IS{,<Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVALE1IS == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBI-Level_Last, TLBI-ExcludeXS, X[t];
        else
            TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
            TLBI-Level_Last, TLBI-AllAttr, X[t]);
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
            TLBI-Level_Last, TLBI-AllAttr, X[t]);
        else
            TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
            TLBI-Level_Last, TLBI-AllAttr, X[t]);
    elsif PSTATE.EL == EL3 then
        if HCR_EL2.<E2H,TGE> == '11' then
            TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
            TLBI-Level_Last, TLBI-AllAttr, X[t]);
        else
            TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
            TLBI-Level_Last, TLBI-AllAttr, X[t]);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI-Level_Last,
            TLBI-AllAttr, X[t]);
        else
            TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI-Level_Last,
            TLBI-AllAttr, X[t]);

**TLBI VALE1ISNXS{,<Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(_FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' && HFGITR_EL2.TLBIVAEII IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif;
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  endif;
The TLBI VALE1OS, TLBI VALE1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.E2H, TGE is not {1, 1}, the entry would be used with the current VMID and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.E2H, TGE is {1, 1}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBiOS is implemented. Otherwise, direct accesses to TLBI VALE1OS, TLBI VALE1OSNXS are UNDEFINED.
Attributes

TLBI VALE1OS, TLBI VALE1OSNXS is a 64-bit System instruction.

Field descriptions

The TLBI VALE1OS, TLBI VALE1OSNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
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<td>59</td>
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<td>56</td>
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<td>54</td>
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<td>52</td>
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<td>51</td>
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<td>50</td>
<td></td>
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<td>49</td>
<td></td>
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<td>48</td>
<td></td>
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<tr>
<td>47</td>
<td></td>
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<tr>
<td>46</td>
<td></td>
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<tr>
<td>45</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
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<tr>
<td>43</td>
<td></td>
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<tr>
<td>42</td>
<td></td>
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<tr>
<td>41</td>
<td></td>
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<tr>
<td>40</td>
<td></td>
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<tr>
<td>39</td>
<td></td>
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<tr>
<td>38</td>
<td></td>
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<tr>
<td>37</td>
<td></td>
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<tr>
<td>36</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

ASID, bits [63:48]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, res0.
**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granularity size, as follows:

- Where a 4KB translation granularity is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granularity is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granularity is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE1OS, TLBI VALE10SNXS instruction**

Accesses to this instruction use the following encodings:

TLBI VALE1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & HCR_EL2.TTL == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() & HCR_EL2.TTL0S == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) & HCRX_EL2.FnXS == '1' then
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI Level_Last, TLBI ExcludeXS, X[t]);
    else
      TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI Level_Last, TLBI AllAttr, X[t]);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI Level_Last, TLBI AllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI Level_Last, TLBI AllAttr, X[t]);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI Level_Last, TLBI AllAttr, X[t]);
  else
    TLBI VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI Level_Last, TLBI AllAttr, X[t]);
  end
TLBI VALE10SNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b0000</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVALE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBLevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBLevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBLevel_Last,
    TLBI_ExcludeXS, X[t]);
The TLBI VALE2, TLBI VALE2NXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA using the EL2 or EL2&0 translation regime.
- If HCR_EL2.E2H == 0, the entry is from the final level of the translation table walk.
- If HCR_EL2.E2H == 1, one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE2, TLBI VALE2NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE2, TLBI VALE2NXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>ASID</td>
</tr>
<tr>
<td>62</td>
<td>TTL</td>
</tr>
<tr>
<td>55:12</td>
<td>VA</td>
</tr>
<tr>
<td>31</td>
<td>29</td>
</tr>
<tr>
<td>28</td>
<td>26</td>
</tr>
<tr>
<td>25</td>
<td>23</td>
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<td>24</td>
<td>22</td>
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<td>21</td>
<td>20</td>
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<td>19</td>
<td>18</td>
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<td>17</td>
<td>16</td>
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<td>15</td>
<td>14</td>
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<td>13</td>
<td>12</td>
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<tr>
<td>11</td>
<td>10</td>
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<tr>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

When HCR_EL2.E2H == 1:

- ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
- Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

TTL, bits [47:44]

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level.</td>
</tr>
<tr>
<td></td>
<td>Hardware must assume that the entry can be from any level.</td>
</tr>
<tr>
<td></td>
<td>In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk</td>
</tr>
<tr>
<td></td>
<td>for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat</td>
</tr>
<tr>
<td></td>
<td>as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk</td>
</tr>
<tr>
<td></td>
<td>for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat</td>
</tr>
<tr>
<td></td>
<td>as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk</td>
</tr>
<tr>
<td></td>
<td>for the leaf level 0bxx is encoded as:</td>
</tr>
<tr>
<td></td>
<td>0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00.</td>
</tr>
<tr>
<td></td>
<td>0b01 : Level 1.</td>
</tr>
<tr>
<td></td>
<td>0b10 : Level 2.</td>
</tr>
<tr>
<td></td>
<td>0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.
Executing the TLBI VALE2, TLBI VALE2NXS instruction

Accesses to this instruction use the following encodings:

**TLBI VALE2{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_AllAttr, X[t]);
```

**TLBI VALE2NXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```c
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        UNDEFINED;
    elsif HCR_EL2.E2H == '1' then
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
    else
        TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_None, TLBILevel_Last,
                TLBI_ExcludeXS, X[t]);
```
TLBI VALE2IS, TLBI VALE2ISNXS, TLB Invalidate by VA, Last level, EL2, Inner Shareable

The TLBI VALE2IS, TLBI VALE2ISNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA using the EL2 or EL2&0 translation regime.
- If $HCR_{EL2}.E2H == 0$, the entry is from the final level of the translation table walk.
- If $HCR_{EL2}.E2H == 1$, one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE2IS, TLBI VALE2ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE2IS, TLBI VALE2ISNXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ASID | TTL | VA[55:12] |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**ASID, bits [63:48]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

**TTL, bits [47:44]**

**When FEAT_TTL is implemented:**

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00: Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01: Level 1. 0b10: Level 2. 0b11: Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE2IS, TLBI VALE2ISNXS instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
             TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last,
             TLBI_AllAttr, X[t]);
  end if;
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    if HCR_EL2.E2H == '1' then
      TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_Inner, TLBILevel_Last,
               TLBI_AllAttr, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last,
               TLBI_AllAttr, X[t]);
    end if;
  end if;
endif;

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner,
             TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last,
             TLBI_ExcludeXS, X[t]);
  end if;
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    if HCR_EL2.E2H == '1' then
      TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID[], Shareability_Inner, TLBILevel_Last,
               TLBI_ExcludeXS, X[t]);
    else
      TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Inner, TLBILevel_Last,
               TLBI_ExcludeXS, X[t]);
    end if;
  end if;
endif;
The TLBI VALE2OS, TLBI VALE2OSNXS characteristics are:

**Purpose**

When EL2 is implemented and enabled in the current Security state, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified VA using the EL2 or EL2&0 translation regime.
- If \( \text{HCR\_EL2\_E2H} \) == 0, the entry is from the final level of the translation table walk.
- If \( \text{HCR\_EL2\_E2H} \) == 1, one of the following applies:
  - The entry is a global entry from the final level of the translation table walk.
  - The entry is a non-global entry from the final level of the translation table walk that matches the specified ASID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VALE2OS, TLBI VALE2OSNXS are UNDEFINED.

**Attributes**

TLBI VALE2OS, TLBI VALE2OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE2OS, TLBI VALE2OSNXS input value bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ASID | TTL | VA[55:12] |

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**ASID, bits [63:48]**

When \( \text{HCR\_EL2\_E2H} \) == 1:

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

If the implementation supports 16 bits of ASID, then the upper 8 bits of the ASID must be written to 0 by software when the context being invalidated only uses 8 bits.

Otherwise:

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
</tbody>
</table>
| 0b01xx  | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
|         | 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00. |
|         | 0b01 : Level 1.                                                        |
|         | 0b10 : Level 2.                                                       |
|         | 0b11 : Level 3.                                                       |
| 0b10xx  | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
|         | 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.                         |
|         | 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00. |
|         | 0b10 : Level 2.                                                       |
|         | 0b11 : Level 3.                                                       |
| 0b11xx  | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:
|         | 0b00 : Reserved. Treat as if TTL<3:2> is 0b00.                         |
|         | 0b01 : Level 1.                                                       |
|         | 0b10 : Level 2.                                                       |
|         | 0b11 : Level 3.                                                       |

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.
Executing the TLBI VALE2OS, TLBI VALE2OSNXS instruction

Accesses to this instruction use the following encodings:

**TLBI VALE2OS**, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_AllAttr, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBILevel_Last, TLBI_AllAttr, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_AllAttr, X[t]);

TLBI VALE2OSNXS, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
elsif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  elsif HCR_EL2.E2H == '1' then
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer,
    TLBILevel_Last, TLBI_ExcludeXS, X[t]);
  else
    TLBI_VA(SecurityStateAtEL(EL2), Regime_EL2, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
The TLBI VALE3, TLBI VALE3NXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE3, TLBI VALE3NXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE3, TLBI VALE3NXS input value bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | TTL | VA[55:12] |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

Bits [63:48]

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is RES0.</td>
</tr>
<tr>
<td>0b01xx</td>
<td>The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL&lt;3:2&gt; is 0b00. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
<tr>
<td>0b11xx</td>
<td>The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as: 0b00 : Reserved. Treat as if TTL&lt;3:2&gt; is 0b00. 0b01 : Level 1. 0b10 : Level 2. 0b11 : Level 3.</td>
</tr>
</tbody>
</table>

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, RES0.

**VA[55:12], bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE3, TLBI VALE3NXS instruction**

Accesses to this instruction use the following encodings:

```
TLBI VALE3{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI_VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Last,
          TLBI_AllAttr, X[t]);

TLBI VALE3NXS{}, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_None, TLBILevel_Last,
          TLBI_ExcludeXS, X[t]);
The TLBI VALE3IS, TLBI VALE3ISNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VALE3IS, TLBI VALE3ISNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE3IS, TLBI VALE3ISNXS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>TTL</td>
</tr>
<tr>
<td>55:12</td>
<td>VA[55:12]</td>
</tr>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
TLBI VALE3IS, TLBI VALE3ISNXS, TLB Invalidate by VA, Last level, EL3, Inner Shareable

<table>
<thead>
<tr>
<th>TTL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00xx</td>
<td>No information supplied as to the translation table level. Hardware must assume that the entry can be from any level. In this case, TTL&lt;1:0&gt; is res0.</td>
</tr>
</tbody>
</table>
| 0b01xx | The entry comes from a 4KB translation granule. The level of walk for the leaf level 0bxx is encoded as:  
0b00 : If FEAT_LPA2 is implemented, level 0. Otherwise, treat as if TTL<3:2> is 0b00.  
0b01 : Level 1.  
0b10 : Level 2.  
0b11 : Level 3. |
| 0b10xx | The entry comes from a 16KB translation granule. The level of walk for the leaf level 0bxx is encoded as:  
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.  
0b01 : If FEAT_LPA2 is implemented, level 1. Otherwise, treat as if TTL<3:2> is 0b00.  
0b10 : Level 2.  
0b11 : Level 3. |
| 0b11xx | The entry comes from a 64KB translation granule. The level of walk for the leaf level 0bxx is encoded as:  
0b00 : Reserved. Treat as if TTL<3:2> is 0b00.  
0b01 : Level 1.  
0b10 : Level 2.  
0b11 : Level 3. |

If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

Otherwise:

Reserved, res0.

VA[55:12], bits [43:0]

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as res0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are res0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are res0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE3IS, TLBI VALE3ISNXS instruction**

Accesses to this instruction use the following encodings:

TLBI VALE3IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_AllAttr, X[t]);

TLBI VA(E3ISNXS{, <Xt>})

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Inner, TLBILevel_Last, TLBI_ExcludeXS, X[t]);
TLBI VALE3OS, TLBI VALE3OSNXS, TLB Invalidate by VA, Last level, EL3, Outer Shareable

The TLBI VALE3OS, TLBI VALE3OSNXS characteristics are:

**Purpose**

If EL3 is implemented, invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified VA using the EL3 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VALE3OS, TLBI VALE3OSNXS are UNDEFINED.

**Attributes**

TLBI VALE3OS, TLBI VALE3OSNXS is a 64-bit System instruction.

**Field descriptions**

The TLBI VALE3OS, TLBI VALE3OSNXS input value bit assignments are:

<p>| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|</p>
<table>
<thead>
<tr>
<th>RES0</th>
<th>TTL</th>
<th>VA[55:12]</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**TTL, bits [47:44]**

When FEAT_TTL is implemented:

Translation Table Level. Indicates the level of the page table walk that holds the leaf entry for the address being invalidated.
If an incorrect value of the TTL field is specified for the entry being invalidated by the instruction, then no entries are required by the architecture to be invalidated from the TLB.

**Otherwise:**

Reserved, RES0.

**VA(55:12), bits [43:0]**

Bits[55:12] of the virtual address to match. Any appropriate TLB entries that match the ASID value (if appropriate) and VA will be affected by this System instruction.

If the TLB maintenance instructions are targeting a translation regime that is using AArch32, and so has a VA of only 32 bits, then the software must treat bits[55:32] as RES0.

The treatment of the low-order bits of this field depends on the translation granule size, as follows:

- Where a 4KB translation granule is being used, all bits are valid and used for the invalidation.
- Where a 16KB translation granule is being used, bits [1:0] of this field are RES0 and ignored when the instruction is executed, because VA[13:12] have no effect on the operation of the instruction.
- Where a 64KB translation granule is being used, bits [3:0] of this field are RES0 and ignored when the instruction is executed, because VA[15:12] have no effect on the operation of the instruction.

**Executing the TLBI VALE3OS, TLBI VALE3OSNXS instruction**

Accesses to this instruction use the following encodings:

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b110</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    UNDEFINED;
elif PSTATE.EL == EL2 then
    UNDEFINED;
elif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_AllAttr, X[t]);

TLBI VALE3OSNXS{}, <Xt>}

<table>
<thead>
<tr>
<th></th>
<th>op0</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b01</td>
<td>0b101</td>
<td>0b001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elif PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    UNDEFINED;
elif PSTATE.EL == EL2 then
    UNDEFINED;
elif PSTATE.EL == EL3 then
    TLBI VA(SecurityStateAtEL(EL3), Regime_EL3, VMID[], Shareability_Outer, TLBILevel_Last,
    TLBI_ExcludeXS, X[t]);
TLBI VMALLE1, TLBI VMALLE1NXS, TLB Invalidate by VMID, All at stage 1, EL1

The TLBI VMALLE1, TLBI VMALLE1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3:NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to the PE that executes this System instruction.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VMALLE1, TLBI VMALLE1NXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

**Executing the TLBI VMALLE1, TLBI VMALLE1NXS instruction**

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is constrained unpredictable whether:

- The instruction is Undefined.
The instruction behaves as if the Xt field is set to 0b1111.

Accesses to this instruction use the following encodings:

**TLBIVMALLE1{, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGETn == '1') && HFGITR_EL2.TLBIVMALLE1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.FB == '1' then
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS);
    else
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);
    end
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS);
    else
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_AllAttr);
    end
  end
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr);
  else
    TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr);
  end
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr);
  else
    TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_AllAttr);
  end
TLBI VMALLE1NXS{, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(Feat_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
        HFGITR_EL2.TLBIVMALLE1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.FB == '1' then
        TLBI_VMALLE(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBI_ExcludeXS);
    else
        TLBI_VMALLE(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS);
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VMALLE(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
        TLBI_ExcludeXS);
    else
        TLBI_VMALLE(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_ExcludeXS);
    end
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VMALLE(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None,
        TLBI_ExcludeXS);
    else
        TLBI_VMALLE(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_None, TLBI_ExcludeXS);
    end
end
TLBI VMALLE1IS, TLBI VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable

The TLBI VMALLE1IS, TLBI VMALLE1ISNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \(\{1, 1\}\), the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \(\{1, 1\}\), the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

---

**Note**

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

---

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

---

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VMALLE1IS, TLBI VMALLE1ISNXS is a 64-bit System instruction.
Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

Executing the TLBI VMALLE1IS, TLBI VMALLE1ISNXS instruction

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

TLBI VMALLE1IS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVMALLE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS);
    else
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);
    endif
  endif
else
  if PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
      TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_AllAttr);
    else
      TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_AllAttr);
    endif
  else
    if PSTATE.EL == EL3 then
      if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_AllAttr);
      else
        TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Inner, TLBI_AllAttr);
      endif
    else
      TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);
    endif
  endif
endif

TLBI VMALLE1ISNXS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() \&\& HCR_EL2.TTLB == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() \&\& HCR_EL2.TTLBIS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() \&\& (!HaveEL(EL3) \|\| SCR_EL3.FGTEn == '1') \&\& HCRX_EL2.FGTnXS == '0' \&\& HFGITR_EL2.TLBIVMALLE1IS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
else
  TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  else
    TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
else
  TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  else
    TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
else
  TLBI_VMALLE1IS, TLBI_VMALLE1ISNXS, TLB Invalidate by VMID, All at stage 1, EL1, Inner Shareable
  fi
The TLBI VMALLE1OS, TLBI VMALLE1OSNXS characteristics are:

### Purpose

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- When EL2 is implemented and enabled in the Security state described by the current value of SCR_EL3.NS:
  - If HCR_EL2.{E2H, TGE} is not \{1, 1\}, the entry would be used with the current VMID, and would be required to translate the specified VA using the EL1&0 translation regime.
  - If HCR_EL2.{E2H, TGE} is \{1, 1\}, the entry would be required to translate the specified VA using the EL2&0 translation regime.
- When EL2 is not implemented or is disabled in the current Security state, the entry would be required to translate the specified VA using the EL1&0 translation regime.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

### Note

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

### Note

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

### Configuration

This instruction is present only when FEAT_TLBIO1OS is implemented. Otherwise, direct accesses to TLBI VMALLE1OS, TLBI VMALLE1OSNXS are UNDEFINED.
Attributes

TLBI VMALLE1OS, TLBI VMALLE1OSNXS is a 64-bit System instruction.

Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

Executing the TLBI VMALLE1OS, TLBI VMALLE1OSNXS instruction

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

TLBI VMALLE1OS{, <Xt>}

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
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<th>op2</th>
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<tbody>
<tr>
<td>0b01</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TTLB == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.TTLB0S == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGITR_EL2.TLBIVMALLE1OS == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        if IsFeatureImplemented(FEAT_XS) && HCRX_EL2.FnXS == '1' then
            TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
        else
            TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_AllAttr);
        end
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_AllAttr);
    else
        if PSTATE.EL == EL10 then
            if PSTATE.EL == EL10 then
                TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBI_AllAttr);
            end
        end
    end
elsif PSTATE.EL == EL3 then
    if HCR_EL2.<E2H,TGE> == '11' then
        TLBI_VMALL(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_AllAttr);
    else
        if PSTATE.EL == EL10 then
            if PSTATE.EL == EL10 then
                TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID_NONE, Shareability_Outer, TLBI_AllAttr);
            end
        end
    end
TLBI_VMALLE1OSNXS{, <Xt>}

<table>
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<th>op1</th>
<th>CRn</th>
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<tbody>
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<td>0b01</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TTL == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.TTLBOS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HCRX_EL2.FGTnXS == '0' &&
    HFGITR_EL2.TLBIVMALLE1OS == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TLBI_VMALLE1OS(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
  endif
elsif PSTATE.EL == EL2 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALLE1OS(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_ExcludeXS);
  else
    TLBI_VMALLE1OS(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
  endif
elsif PSTATE.EL == EL3 then
  if HCR_EL2.<E2H,TGE> == '11' then
    TLBI_VMALLE1OS(SecurityStateAtEL(EL2), Regime_EL20, VMID_NONE, Shareability_Outer, TLBI_ExcludeXS);
  else
    TLBI_VMALLE1OS(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
  endif
else
  TLBI_VMALLE1OS(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
end
The TLBI VMALLS12E1, TLBI VMALLS12E1NXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If $\text{SCR\_EL3}.\text{NS}$ is 0, then:
  - The entry would be required to translate an address using the Secure EL1&0 translation regime.
  - If $\text{FEAT\_SEL2}$ is implemented and enabled, the entry would be used with the current VMID.
- If $\text{SCR\_EL3}.\text{NS}$ is 1, then:
  - The entry would be required to translate an address using the Non-secure EL1&0 translation regime.
  - If Non-secure EL2 is implemented, the entry would be used with the current VMID.

The invalidation applies to the PE that executes this System instruction.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If $\text{FEAT\_XS}$ is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

There are no configuration notes.

**Attributes**

TLBI VMALLS12E1, TLBI VMALLS12E1NXS is a 64-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by $<\text{Xt}>$ is ignored.

**Executing the TLBI VMALLS12E1, TLBI VMALLS12E1NXS instruction**

When executing this instruction $\text{Xt} =$ should be encoded as $0b11111$. If the $\text{Xt}$ field is not set to $0b11111$, it is **CONSTRAINED UNPREDICTABLE** whether:
The instruction is **UNDEFINED**.

The instruction behaves as if the Xt field is set to 0b1111.

Accesses to this instruction use the following encodings:

**TLBI VMALLS12E1{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsf PSTATE.EL == EL2 then
  TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_AllAttr);
elsf PSTATE.EL == EL3 then
  if !EL2Enabled() then
    TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_AllAttr);
  else
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_AllAttr);

**TLBI VMALLS12E1NXS{, <Xt>}**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
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<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1001</td>
<td>0b0111</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if !IsFeatureImplemented(FEAT_XS) then
  UNDEFINED;
elsf PSTATE.EL == EL0 then
  UNDEFINED;
elsf PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsf PSTATE.EL == EL2 then
  TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS);
elsf PSTATE.EL == EL3 then
  if !EL2Enabled() then
    TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS);
  else
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_None, TLBI_ExcludeXS);
The TLBI VMALLS12E1IS, TLBI VMALLS12E1ISNXS, TLB Invalidate by VMID, All at Stage 1 and 2, EL1, Inner Shareable characteristics are:

### Purpose

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If SCR_EL3.NS is 0, then:
  - The entry would be required to translate an address using the Secure EL1&0 translation regime.
  - If FEAT_SEL2 is implemented and enabled, the entry would be used with the current VMID.
- If SCR_EL3.NS is 1, then:
  - The entry would be required to translate an address using the Non-secure EL1&0 translation regime.
  - If Non-secure EL2 is implemented, the entry would be used with the current VMID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

### Note

From Armv8.4, when a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

### Note

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

### Configuration

There are no configuration notes.
Attributes

TLBI VMALLS12E1IS, TLBI VMALLS12E1ISNXS is a 64-bit System instruction.

Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

Executing the TLBI VMALLS12E1IS, TLBI VMALLS12E1ISNXS instruction

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is constrained unpredictable whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

```
TLBI VMALLS12E1IS{, <Xt>}
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
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<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);
elseif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);
  else
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_AllAttr);

TLBI VMALLS12E1ISNXS{, <Xt>}

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<td>0b100</td>
<td>0b1001</td>
<td>0b0011</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner, TLBI_ExcludeXS);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBI_ExcludeXS);
    else
        TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Inner,
        TLBI_ExcludeXS);
    endif
The TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS characteristics are:

**Purpose**

Invalidates cached copies of translation table entries from TLBs that meet all the following requirements:

- The entry is a stage 1 or stage 2 translation table entry, from any level of the translation table walk.
- If SCR_EL3 NS is 0, then:
  - The entry would be required to translate an address using the Secure EL1&0 translation regime.
  - If FEAT_SEL2 is implemented and enabled, the entry would be used with the current VMID.
- If SCR_EL3 NS is 1, then:
  - The entry would be required to translate an address using the Non-secure EL1&0 translation regime.
  - If Non-secure EL2 is implemented, the entry would be used with the current VMID.

The invalidation applies to all PEs in the same Outer Shareable shareability domain as the PE that executes this System instruction.

**Note**

When a TLB maintenance instruction is generated to the Secure EL1&0 translation regime and is defined to pass a VMID argument, or would be defined to pass a VMID argument if SCR_EL3.EEL2==1, then:

- A PE with SCR_EL3.EEL2==1 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==0.
- A PE with SCR_EL3.EEL2==0 is not architecturally required to invalidate any entries in the Secure EL1&0 translation of a PE in the same required shareability domain with SCR_EL3.EEL2==1.
- A PE is architecturally required to invalidate all relevant entries in the Secure EL1&0 translation of a System MMU in the same required shareability domain with a VMID of 0.

**Note**

For the EL1&0 translation regimes, the invalidation applies to both global entries and non-global entries with any ASID.

If FEAT_XS is implemented, the nXS variant of this System instruction is defined.

Both variants perform the same invalidation, but the TLBI System instruction without the nXS qualifier waits for all memory accesses using in-scope old translation information to complete before it is considered complete.

The TLBI System instruction with the nXS qualifier is considered complete when the subset of these memory accesses with XS attribute set to 0 are complete.

**Configuration**

This instruction is present only when FEAT_TLBIOS is implemented. Otherwise, direct accesses to TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS are undefined.
Attributes

TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS is a 64-bit System instruction.

Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Xt> is ignored.

Executing the TLBI VMALLS12E1OS, TLBI VMALLS12E1OSNXS instruction

When executing this instruction Xt should be encoded as 0b11111. If the Xt field is not set to 0b11111, it is CONSTRAINED UNPREDICTABLE whether:

- The instruction is UNDEFINED.
- The instruction behaves as if the Xt field is set to 0b11111.

Accesses to this instruction use the following encodings:

TLBI VMALLS12E1OS{, <Xt>}

<table>
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<tr>
<td>0b01</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elifs PSTATE.EL == EL2 then
  TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_AllAttr);
elifs PSTATE.EL == EL3 then
  if !EL2Enabled() then
    TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_AllAttr);
  else
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_AllAttr);

TLBI VMALLS12E1OSNXS{, <Xt>}

<table>
<thead>
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<td>0b1001</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if !IsFeatureImplemented(FEAT_XS) then
    UNDEFINED;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer, TLBI_ExcludeXS);
elsif PSTATE.EL == EL3 then
    if !EL2Enabled() then
        TLBI_VMALL(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
        TLBI_ExcludeXS);
    else
        TLBI_VMALLS12(SecurityStateAtEL(EL1), Regime_EL10, VMID[], Shareability_Outer,
        TLBI_ExcludeXS);
TPIDR_EL0, EL0 Read/Write Software Thread ID Register

The TPIDR_EL0 characteristics are:

**Purpose**

Provides a location where software executing at EL0 can store thread identifying information, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch64 System register TPIDR_EL0 bits [31:0] are architecturally mapped to AArch32 System register TPIDRURW[31:0].

**Attributes**

TPIDR_EL0 is a 64-bit register.

**Field descriptions**

The TPIDR_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TPIDR_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, TPIDR_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
    HFGWTR_EL2.TPIDR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return TPIDR_EL0;
elsif PSTATE.EL == EL1 then
  if EL2_ENABLED() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TPIDR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    return TPIDR_EL0;
elsif PSTATE.EL == EL2 then
  return TPIDR_EL0;
elsif PSTATE.EL == EL3 then
  return TPIDR_EL0;

MSR TPIDR_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b01</td>
<td>0b101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
    HFGWTR_EL2.TPIDR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TPIDR_EL0 = X[t];
elsif PSTATE.EL == EL1 then
  if EL2_ENABLED() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TPIDR_EL0 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TPIDR_EL0 = X[t];
elsif PSTATE.EL == EL2 then
  TPIDR_EL0 = X[t];
elsif PSTATE.EL == EL3 then
  TPIDR_EL0 = X[t];
TPIDR_EL1, EL1 Software Thread ID Register

The TPIDR_EL1 characteristics are:

**Purpose**

Provides a location where software executing at EL1 can store thread identifying information, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch64 System register TPIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register TPIDRPRW[31:0].

**Attributes**

TPIDR_EL1 is a 64-bit register.

**Field descriptions**

The TPIDR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Thread ID</td>
<td>Thread ID. Thread identifying information stored by software running at this Exception level.</td>
</tr>
<tr>
<td>62</td>
<td>Thread ID</td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the TPIDR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, TPIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then

UNDEFINED;

elsif PSTATE.EL == EL1 then

if EL2Enabled() && !HaveEL(EL3) || SCR_EL3.FGTEn == '1' && HFGTR_EL2.TPIDR_EL1 == '1' then

AArch64.SystemAccessTrap(EL2, 0x18);

else

return TPIDR_EL1;

elsif PSTATE.EL == EL2 then

return TPIDR_EL1;

elsif PSTATE.EL == EL3 then

return TPIDR_EL1;
MSR TPIDR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TPIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    TPIDR_EL1 = X[t];
elsif PSTATE.EL == EL2 then
  TPIDR_EL1 = X[t];
else if PSTATE.EL == EL3 then
  TPIDR_EL1 = X[t];
TPIDR_EL2, EL2 Software Thread ID Register

The TPIDR_EL2 characteristics are:

**Purpose**

Provides a location where software executing at EL2 can store thread identifying information, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch64 System register TPIDR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HTPIDR[31:0]

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

TPIDR_EL2 is a 64-bit register.

**Field descriptions**

The TPIDR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Thread ID</td>
</tr>
<tr>
<td>62</td>
<td>Thread ID</td>
</tr>
<tr>
<td>61</td>
<td>Thread ID</td>
</tr>
<tr>
<td>60</td>
<td>Thread ID</td>
</tr>
<tr>
<td>59</td>
<td>Thread ID</td>
</tr>
<tr>
<td>58</td>
<td>Thread ID</td>
</tr>
<tr>
<td>57</td>
<td>Thread ID</td>
</tr>
<tr>
<td>56</td>
<td>Thread ID</td>
</tr>
<tr>
<td>55</td>
<td>Thread ID</td>
</tr>
<tr>
<td>54</td>
<td>Thread ID</td>
</tr>
<tr>
<td>53</td>
<td>Thread ID</td>
</tr>
<tr>
<td>52</td>
<td>Thread ID</td>
</tr>
<tr>
<td>51</td>
<td>Thread ID</td>
</tr>
<tr>
<td>50</td>
<td>Thread ID</td>
</tr>
<tr>
<td>49</td>
<td>Thread ID</td>
</tr>
<tr>
<td>48</td>
<td>Thread ID</td>
</tr>
<tr>
<td>47</td>
<td>Thread ID</td>
</tr>
<tr>
<td>46</td>
<td>Thread ID</td>
</tr>
<tr>
<td>45</td>
<td>Thread ID</td>
</tr>
<tr>
<td>44</td>
<td>Thread ID</td>
</tr>
<tr>
<td>43</td>
<td>Thread ID</td>
</tr>
<tr>
<td>42</td>
<td>Thread ID</td>
</tr>
<tr>
<td>41</td>
<td>Thread ID</td>
</tr>
<tr>
<td>40</td>
<td>Thread ID</td>
</tr>
<tr>
<td>39</td>
<td>Thread ID</td>
</tr>
<tr>
<td>38</td>
<td>Thread ID</td>
</tr>
<tr>
<td>37</td>
<td>Thread ID</td>
</tr>
<tr>
<td>36</td>
<td>Thread ID</td>
</tr>
<tr>
<td>35</td>
<td>Thread ID</td>
</tr>
<tr>
<td>34</td>
<td>Thread ID</td>
</tr>
<tr>
<td>33</td>
<td>Thread ID</td>
</tr>
<tr>
<td>32</td>
<td>Thread ID</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TPIDR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, TPIDR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
      return NVMem[0x090];
   elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
   endif
elsif PSTATE.EL == EL2 then
   return TPIDR_EL2;
elsif PSTATE.EL == EL3 then
   return TPIDR_EL2;
endif

---

**MSR TPIDR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
      NVMem[0x090] = X[t];
   elsif EL2Enabled() && HCR_EL2.NV == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   else
      UNDEFINED;
   endif
elsif PSTATE.EL == EL2 then
   TPIDR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
   TPIDR_EL2 = X[t];
TPIDR_EL3, EL3 Software Thread ID Register

The TPIDR_EL3 characteristics are:

**Purpose**

Provides a location where software executing at EL3 can store thread identifying information, for OS management purposes.

The PE makes no use of this register.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to TPIDR_EL3 are **UNDEFINED**.

**Attributes**

TPIDR_EL3 is a 64-bit register.

**Field descriptions**

The TPIDR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Thread ID</td>
</tr>
<tr>
<td>31-0</td>
<td>Thread ID</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the TPIDR_EL3**

Accesses to this register use the following encodings:

```
MRS <Xt>, TPIDR_EL3
```

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b10</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return TPIDR_EL3;
MSR TPIDR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  TPIDR_EL3 = X[t];
The TPIDRRO_EL0 characteristics are:

**Purpose**

Provides a location where software executing at EL1 or higher can store thread identifying information that is visible to software executing at EL0, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch64 System register TPIDRRO_EL0 bits [31:0] are architecturally mapped to AArch32 System register TPIDRURO[31:0].

**Attributes**

TPIDRRO_EL0 is a 64-bit register.

**Field descriptions**

The TPIDRRO_EL0 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Thread ID | Thread ID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0 |

**Bits [63:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

**Accessing the TPIDRRO_EL0**

Accesses to this register use the following encodings:

MRS <Xt>, TPIDRRO_EL0

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') &&
    HFGTR_EL2.TPIDRRO_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return TPIDRRO_EL0;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TPIDRRO_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        return TPIDRRO_EL0;
elsif PSTATE.EL == EL2 then
    return TPIDRRO_EL0;
elsif PSTATE.EL == EL3 then
    return TPIDRRO_EL0;

MSR TPIDRRO_EL0, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b011</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TPIDRRO_EL0 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        TPIDRRO_EL0 = X[t];
elsif PSTATE.EL == EL2 then
    TPIDRRO_EL0 = X[t];
elsif PSTATE.EL == EL3 then
    TPIDRRO_EL0 = X[t];
The TRFCR_EL1 characteristics are:

**Purpose**

Provides EL1 controls for Trace.

**Configuration**

AArch64 System register TRFCR_EL1 bits [31:0] are architecturally mapped to AArch32 System register TRFCR[31:0].

This register is present only when FEAT_TRF is implemented. Otherwise, direct accesses to TRFCR_EL1 are UNDEFINED.

**Attributes**

TRFCR_EL1 is a 64-bit register.

**Field descriptions**

The TRFCR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:7</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>6:5</td>
<td>Timestamp Control. Controls which timebase is used for trace timestamps.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>Virtual timestamp. The traced timestamp is the physical counter value minus the value of CNTPOFF_EL2.</td>
<td>When FEAT_ECV is implemented</td>
</tr>
</tbody>
</table>
| 0b10 | Guest physical timestamp. The traced timestamp is the physical counter value minus a physical offset. If any of the following are true, the physical offset is zero, otherwise the physical offset is the value of CNTPOFF_EL2:  
  - SCR_EL3.ECVEn == 0b0.  
  - CNTHCTL_EL2.ECV == 0b0. |                                   |
| 0b11 | Physical timestamp. The traced timestamp is the physical counter value. |                                   |

All other values are reserved.

This field is ignored by the PE when any of the following are true:

- EL2 is implemented and TRFCR_EL2.TS != 0b00.
- SelfHostedTraceEnabled() == FALSE.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [4:2]**

Reserved, **RES0**.

**E1TRE, bit [1]**

EL1 Trace Enable.

<table>
<thead>
<tr>
<th>E1TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace is prohibited at EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace is allowed at EL1.</td>
</tr>
</tbody>
</table>

This field is ignored if **SelfHostedTraceEnabled() == FALSE**.

On a Warm reset, this field resets to 0.

**E0TRE, bit [0]**

EL0 Trace Enable.

<table>
<thead>
<tr>
<th>E0TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace is prohibited at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace is allowed at EL0.</td>
</tr>
</tbody>
</table>

This field is ignored if any of the following are true:

- **SelfHostedTraceEnabled() == FALSE**.
- EL2 is implemented and enabled in the current Security state and **HCR_EL2.TGE == 1**.

On a Warm reset, this field resets to 0.

**Accessing the TRFCR_EL1**

Accesses to this register use the following encodings:

MRS <Xt>, TRFCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
      UNDEFINED;
   elsif EL2Enabled() && MDCR_EL2.TTRF == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
   elsif Halted() && MDCR_EL3.TTRF == '1' then
      UNDEFINED;
   else
      AArch64.SystemAccessTrap(EL3, 0x18);
   end
   return NVMem[0x880];
else
   return TRFCR_EL1;
elseif PSTATE.EL == EL2 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
      UNDEFINED;
   elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
      if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
      else
         AArch64.SystemAccessTrap(EL3, 0x18);
      end
      return TRFCR_EL2;
   else
      return TRFCR_EL1;
   end
elsif PSTATE.EL == EL3 then
   return TRFCR_EL1;

MSR TRFCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.TRFCR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && MDCR_EL2.TTRF == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TRFCR_EL1 = X[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x18);
        end if
    else
        TRFCR_EL1 = X[t];
    endif
elsif PSTATE.EL == EL3 then
    TRFCR_EL1 = X[t];
else
    TRFCR_EL1 = X[t];
end if

MRS <Xt>, TRFCR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x880];
    elseif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
            UNDEFINED;
        elseif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            return TRFCR_EL1;
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return TRFCR_EL1;
    else
        UNDEFINED;
end

MSR TRFCR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x880] = X[t];
    elseif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
            UNDEFINED;
        elseif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.SystemAccessTrap(EL3, 0x18);
            end
        else
            TRFCR_EL1 = X[t];
        end
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        TRFCR_EL1 = X[t];
    else
        UNDEFINED;
TRFCR_EL2, Trace Filter Control Register (EL2)

The TRFCR_EL2 characteristics are:

**Purpose**

Provides EL2 controls for Trace.

**Configuration**

AArch64 System register TRFCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HTRFCR[31:0].

This register is present only when FEAT_TRF is implemented. Otherwise, direct accesses to TRFCR_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

TRFCR_EL2 is a 64-bit register.

**Field descriptions**

The TRFCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>RES0</td>
<td>TS</td>
<td>RES0</td>
<td>CX</td>
<td>RES0</td>
<td>E2TRE</td>
<td>E0HTRE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:7]

Reserved, RES0.

TS, bits [6:5]

Timestamp Control. Controls which timebase is used for trace timestamps.

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Timestamp controlled by TRFCR_EL1.TS or TRFCR.TS.</td>
<td></td>
</tr>
<tr>
<td>0b01</td>
<td>Virtual timestamp. The traced timestamp is the physical counter value minus the value of CNTPOFF_EL2.</td>
<td></td>
</tr>
</tbody>
</table>
| 0b10 | Guest physical timestamp. The traced timestamp is the physical counter value minus a physical offset. If any of the following are true, the physical offset is zero, otherwise the physical offset is the value of CNTPOFF_EL2:  
  • SCR_EL3.ECVEn == 0b0.  
  • CNTHCTL_EL2.ECV == 0b0. | When FEAT_ECV is implemented |
| 0b11 | Physical timestamp. The traced timestamp is the physical counter value. | |

This field is ignored by the PE when SelfHostedTraceEnabled() == FALSE.

On a Warm reset, this field resets to 0.
Bit [4]

Reserved, RES0.

CX, bit [3]

CONTEXTIDR_EL2 and VMID trace enable.

<table>
<thead>
<tr>
<th>CX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CONTEXTIDR_EL2 and VMID trace prohibited.</td>
</tr>
<tr>
<td>0b1</td>
<td>CONTEXTIDR_EL2 and VMID trace allowed.</td>
</tr>
</tbody>
</table>

This field is ignored if SelfHostedTraceEnabled() == FALSE.

On a Warm reset, this field resets to 0.

Bit [2]

Reserved, RES0.

E2TRE, bit [1]

EL2 Trace Enable.

<table>
<thead>
<tr>
<th>E2TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace is prohibited at EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace is allowed at EL2.</td>
</tr>
</tbody>
</table>

This field is ignored if SelfHostedTraceEnabled() == FALSE.

On a Warm reset, this field resets to 0.

E0HTRE, bit [0]

EL0 Trace Enable.

<table>
<thead>
<tr>
<th>E0HTRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace is prohibited at EL0 when HCR_EL2.TGE == 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace is allowed at EL0 when HCR_EL2.TGE == 1.</td>
</tr>
</tbody>
</table>

This field is ignored if any of the following are true:

- SelfHostedTraceEnabled() == FALSE.
- EL2 is disabled in the current security state.
- HCR_EL2.TGE == 0.

On a Warm reset, this field resets to 0.

### Accessing the TRFCR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, TRFCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
else
    return TRFCR_EL2;
elsif PSTATE.EL == EL3 then
    return TRFCR_EL2;

MSR TRFCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
elsif EL2Enabled() && MDCR_EL2.TTRF == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    if HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x880];
    else
        return TRFCR_EL1;
    endif
endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.SystemAccessTrap(EL3, 0x18);
    endif
else
    if HCR_EL2.E2H == '1' then
        return TRFCR_EL2;
    else
        return TRFCR_EL1;
    endif
endif
elsif PSTATE.EL == EL3 then
    return TRFCR_EL1;
endif

MSR TRFCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>opr</th>
<th>opr1</th>
<th>CRn</th>
<th>CRm</th>
<th>opr2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
    UNDEFINED;
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGWTR_EL2.TRFCR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && MDCR_EL2.TTRF == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x880] = X[t];
  else
    TRFCR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && MDCR_EL3.TTRF == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x18);
    end
  elsif HCR_EL2.E2H == '1' then
    TRFCR_EL2 = X[t];
  else
    TRFCR_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  TRFCR_EL1 = X[t];
end
TTBR0_EL1, Translation Table Base Register 0 (EL1)

The TTBR0_EL1 characteristics are:

Purpose

Holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the lower VA range in the EL1&0 translation regime, and other information for this translation regime.

Configuration

AArch64 System register TTBR0_EL1 bits [63:0] are architecturally mapped to AArch32 System register TTBR0[63:0].

Attributes

TTBR0_EL1 is a 64-bit register.

Field descriptions

The TTBR0_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

ASID, bits [63:48]

An ASID for the translation table base address. The TCR_EL1.A1 field selects either TTBR0_EL1.ASID or TTBR1_EL1.ASID.

If the implementation has only 8 bits of ASID, then the upper 8 bits of this field are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

BADDR[47:1], bits [47:1]

Translation table base address:

- Bits A[47:x] of the stage 1 translation table base address bits are in register bits[47:x].
- Bits A[(x-1):0] of the stage 1 translation table base address are zero.

Address bit x is the minimum address bit required to align the translation table to the size of the table. The smallest permitted value of x is 6. The AArch64 Virtual Memory System Architecture chapter describes how x is calculated based on the value of TCR_EL1.T0SZ, the translation stage, and the translation granule size.

Note

A translation table is required to be aligned to the size of the table. If a table contains fewer than eight entries, it must be aligned on a 64 byte address boundary.

If the value of TCR_EL1.IPS is not 0b110, then:

- Register bits[(x-1):1] are RES0.
- If the implementation supports 52-bit PAs and IPAs, then bits A[51:48] of the stage 1 translation table base address are 0b0000.
If FEAT_LPA is implemented and the value of TCR_EL1.IPS is \texttt{0b110}, then:

- Bits A[51:48] of the stage 1 translation table base address bits are in register bits[5:2].
- Register bit[1] is \texttt{RES0}.
- When \(x>6\), register bits[(x-1):6] are \texttt{RES0}.

\textbf{Note}

\texttt{TCR_EL1.IPS==0b110} is permitted when:

- FEAT_LPA is implemented and the 64KB translation granule is used.
- FEAT_LPA2 is implemented and the 4KB or 16KB translation granule is used.

When the value of \texttt{ID_AA64MMFR0_EL1.PARange} indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register when \texttt{TCR_EL1.IPS} is \texttt{0b110} and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If any register bit[47:1] that is defined as \texttt{RES0} has the value 1 when a translation table walk is done using TTBR0_EL1, then the translation table base address might be misaligned, with effects that are \texttt{CONSTRAINED UNPREDICTABLE}, and must be one of the following:

- Bits A[(x-1):0] of the stage 1 translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{CnP, bit [0]}

\textbf{When FEAT_TTCNP is implemented:}

Common not Private. This bit indicates whether each entry that is pointed to by TTBR0_EL1 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR0_EL1.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| \texttt{0b0} | The translation table entries pointed to by TTBR0_EL1, for the current translation regime and ASID, are permitted to differ from corresponding entries for TTBR0_EL1 for other PEs in the Inner Shareable domain. This is not affected by:  
  - The value of TTBR0_EL1.CnP on those other PEs.  
  - The value of the current ASID.  
  - If EL2 is implemented and enabled in the current Security state, the value of the current VMID. |
| \texttt{0b1} | The translation table entries pointed to by TTBR0_EL1 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR0_EL1.CnP is 1 and all of the following apply:  
  - The translation table entries are pointed to by TTBR0_EL1.  
  - The translation tables relate to the same translation regime.  
  - The ASID is the same as the current ASID.  
  - If EL2 is implemented and enabled in the current Security state, the value of the current VMID. |

This field is permitted to be cached in a TLB.

When a TLB combines entries from stage 1 translation and stage 2 translation into a single entry, that entry can only be shared between different PEs if the value of the CnP bit is 1 for both stage 1 and stage 2.

\textbf{Note}

If the value of the TTBR0_EL1.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR0_EL1s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are \texttt{CONSTRAINED}
UNPREDICTABLE, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Accessing the TTBR0_EL1**

When HCR\_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic TTBR0\_EL1 or TTBR0\_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, TTBR0\_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if EL2Enabled() \&\& HCR\_EL2.TVWM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elseif EL2Enabled() \&\& (!HaveEL(EL3) \|\| SCR\_EL3.FGTEn == '1') \&\& HFGRT_EL2.TTBR0\_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
elseif EL2Enabled() \&\& HCR\_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x200];
else
    return TTBR0\_EL1;
elseif PSTATE.EL == EL2 then
    if HCR\_EL2.E2H == '1' then
        return TTBR0\_EL2;
else
    return TTBR0\_EL1;
elseif PSTATE.EL == EL3 then
    return TTBR0\_EL1;
else
    return TTBR0\_EL1;
```

**MSR TTBR0\_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x10);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TTBR0_EL2 == '1'
        then
            AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x200] = X[t];
    else
        TTBR0_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TTBR0_EL2 = X[t];
    else
        TTBR0_EL1 = X[t];
    end if;
elsif PSTATE.EL == EL3 then
    TTBR0_EL1 = X[t];
end if;

MRS <Xt>, TTBR0_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x200];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return TTBR0_EL1;
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return TTBR0_EL1;
    else
        UNDEFINED;
    end if;
end if;

MSR TTBR0_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
  UNDEFINED;
elsif PSTATE_EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x200] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elseif PSTATE_EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TTBR0_EL1 = X[t];
  else
    UNDEFINED;
elseif PSTATE_EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    TTBR0_EL1 = X[t];
  else
    UNDEFINED;
TTBR0_EL2, Translation Table Base Register 0 (EL2)

The TTBR0_EL2 characteristics are:

**Purpose**

When **HCR_EL2.E2H** is 0, holds the base address of the translation table for the initial lookup for stage 1 of an address translation in the EL2 translation regime, and other information for this translation regime.

When **HCR_EL2.E2H** is 1, holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the lower VA range in the EL2&0 translation regime, and other information for this translation regime.

**Configuration**

AArch64 System register TTBR0_EL2 bits [47:1] are architecturally mapped to AArch32 System register **HTTBR[47:1]**.

If EL2 is not implemented, this register is **RES0** from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

TTBR0_EL2 is a 64-bit register.

**Field descriptions**

The TTBR0_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>ASID</th>
<th>BADDR[47:1]</th>
<th>CnP</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASID, bits [63:48]</td>
<td>BADDR[47:1]</td>
<td></td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

When **FEAT_VHE** is implemented:

When **HCR_EL2.E2H** is 0, this field is **RES0**.

When **HCR_EL2.E2H** is 1, it holds an ASID for the translation table base address. The **TCR_EL2.A1** field selects either TTBR0_EL2.ASID or TTBR1_EL2.ASID.

If the implementation has only 8 bits of ASID, then the upper 8 bits of this field are **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**BADDR[47:1], bits [47:1]**

Translation table base address:

- Bits A[47:x] of the stage 1 translation table base address bits are in register bits[47:x].
- Bits A[(x-1):0] of the stage 1 translation table base address are zero.
Address bit \( x \) is the minimum address bit required to align the translation table to the size of the table. The smallest permitted value of \( x \) is 6. The AArch64 Virtual Memory System Architecture chapter describes how \( x \) is calculated based on the value of \( \text{TCR_EL2}.T0SZ \), the translation stage, and the translation granule size.

### Note

A translation table is required to be aligned to the size of the table. If a table contains fewer than eight entries, it must be aligned on a 64 byte address boundary.

If the value of \( \text{TCR_EL2}.\{I\}PS \) is not \( 0b110 \), then:

- Register bits\([x-1]:1\] are \( \text{RES0} \).
- If the implementation supports 52-bit PAs and IPAs, then bits \( A[51:48] \) of the stage 1 translation table base address are \( 0b0000 \).

If FEAT_LPA is implemented and the value of \( \text{TCR_EL2}.\{I\}PS \) is \( 0b110 \), then:

- Bits \( A[51:48] \) of the stage 1 translation table base address bits are in register bits\([5:2]\).
- Register bit\([1]\) is \( \text{RES0} \).
- When \( x>6 \), register bits\([x-1]:6\] are \( \text{RES0} \).

### Note

The OA size specified by \( \text{TCR_EL2}.\{I\}PS \) is determined as follows:

- The value of \( \text{TCR_EL2}.PS \) when the value of \( \text{HCR_EL2}.E2H \) is 0.
- The value of \( \text{TCR_EL2}.IPS \) when the value of \( \text{HCR_EL2}.E2H \) is 1.

\( \text{TCR_EL2}.\{I\}PS==0b110 \) is permitted when:

- FEAT_LPA is implemented and the 64KB translation granule is used.
- FEAT_LPA2 is implemented and the 4KB or 16KB translation granule is used.

When the value of \( \text{ID_AA64MMFR0_EL1}.\text{PARange} \) indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register when \( \text{TCR_EL2}.\{I\}PS \) is \( 0b110 \) and the value of register bits\([5:2]\) is nonzero, an Address size fault is generated.

If any register \( [47:1] \) that is defined as \( \text{RES0} \) has the value 1 when a translation table walk is done using TTBR0_EL2, then the translation table base address might be misaligned, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Bits \( A[(x-1):0] \) of the stage 1 translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### CnP, bit [0]

When FEAT_TTCNP is implemented:

Common not Private. This bit indicates whether each entry that is pointed to by TTBR0_EL2 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR0_EL2.CnP is 1.
The translation table entries pointed to by TTBR0_EL2 for the current translation regime, and ASID if applicable, are permitted to differ from corresponding entries for TTBR0_EL2 for other PEs in the Inner Shareable domain. This is not affected by:

- The value of TTBR0_EL2.CnP on those other PEs.
- When the current translation regime is the EL2&0 regime, the value of the current ASID.

The translation table entries pointed to by TTBR0_EL2 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR0_EL2.CnP is 1 and all of the following apply:

- The translation table entries are pointed to by TTBR0_EL2.
- The translation tables relate to the same translation regime.
- If that translation regime is the EL2&0 regime, the ASID is the same as the current ASID.

This field is permitted to be cached in a TLB.

**Note**

If the value of the TTBR0_EL2.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR0_EL2s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are **CONSTRAINED UNPREDICTABLE**, see ‘CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values’.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Accessing the TTBR0_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic TTBR0_EL2 or TTBR0_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, TTBR0_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return TTBR0_EL2;
elsif PSTATE.EL == EL3 then
    return TTBR0_EL2;
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TTBR0_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TTBR0_EL2 = X[t];

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TTBR0_EL1 == '1'
      then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
      return NVMem[0x200];
    else
      return TTBR0_EL1;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      return TTBR0_EL2;
    else
      return TTBR0_EL1;
  elsif PSTATE.EL == EL3 then
    return TTBR0_EL1;

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TTBR0_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TTBR0_EL2 = X[t];

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TTBR0_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TTBR0_EL2 = X[t];
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if EL2Enabled() && HCR_EL2.TVM == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TTBR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x200] = X[t];
    else
        TTBR0_EL1 = X[t];
    end
elsif PSTATE_EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TTBR0_EL2 = X[t];
    else
        TTBR0_EL1 = X[t];
    end
elsif PSTATE_EL == EL3 then
    TTBR0_EL1 = X[t];
TTBR0_EL3, Translation Table Base Register 0 (EL3)

The TTBR0_EL3 characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 1 of an address translation in the EL3 translation regime, and other information for this translation regime.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to TTBR0_EL3 are UNDEFINED.

**Attributes**

TTBR0_EL3 is a 64-bit register.

**Field descriptions**

The TTBR0_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>BADDR[47:1]</td>
</tr>
<tr>
<td>31</td>
<td>CnP</td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**BADDR[47:1], bits [47:1]**

Translation table base address:

- Bits A[47:x] of the stage 1 translation table base address bits are in register bits[47:x].
- Bits A[(x-1):0] of the stage 1 translation table base address are zero.

Address bit x is the minimum address bit required to align the translation table to the size of the table. The smallest permitted value of x is 6. The AArch64 Virtual Memory System Architecture chapter describes how x is calculated based on the value of TCR_EL3.T0SZ, the translation stage, and the translation granule size.

**Note**

A translation table is required to be aligned to the size of the table. If a table contains fewer than eight entries, it must be aligned on a 64 byte address boundary.

If the value of TCR_EL3.PS is not 0b110, then:

- Register bits[(x-1):1] are RES0.
- If the implementation supports 52-bit PAs and IPAs, then bits A[51:48] of the stage 1 translation table base address are 0b0000.

If FEAT_LPA is implemented and the value of TCR_EL3.PS is 0b110, then:

- Bits A[51:48] of the stage 1 translation table base address bits are in register bits[5:2].
- Register bit[1] is RES0.
- When x>6, register bits[(x-1):6] are RES0.
Note

TCR_EL3.PS==0b110 is permitted when:

• FEAT_LPA is implemented and the 64KB translation granule is used.
• FEAT_LPA2 is implemented and the 4KB or 16KB translation granule is used.

When the value of ID_AA64MMFR0_EL1.PARange indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register when TCR_EL3.PS is 0b110 and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If any register bit[47:1] that is defined as RES0 has the value 1 when a translation table walk is done using TTBR0_EL3, then the translation table base address might be misaligned, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

• Bits A[(x-1):0] of the stage 1 translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
• The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CnP, bit [0]

When FEAT_TTCNP is implemented:
Common not Private. This bit indicates whether each entry that is pointed to by TTBR0_EL3 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR0_EL3.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table entries pointed to by TTBR0_EL3, for the current translation regime, are permitted to differ from corresponding entries for TTBR0_EL3 for other PEs in the Inner Shareable domain. This is not affected by the value of TTBR0_EL3.CnP on those other PEs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The translation table entries pointed to by TTBR0_EL3 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR0_EL3.CnP is 1 and the translation table entries are pointed to by TTBR0_EL3.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

Note

If the value of the TTBR0_EL3.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR0_EL3s do not point to the same translation table entries the results of translations using TTBR0_EL3 are CONSTRAINED UNPREDICTABLE, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

Accessing the TTBR0_EL3

Accesses to this register use the following encodings:
MRS \(<Xt>\), TTBR0_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
esif PSTATE.EL == EL1 then
  UNDEFINED;
esif PSTATE.EL == EL2 then
  UNDEFINED;
esif PSTATE.EL == EL3 then
  return TTBR0_EL3;

MSR TTBR0_EL3, \(<Xt>\)

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
esif PSTATE.EL == EL1 then
  UNDEFINED;
esif PSTATE.EL == EL2 then
  UNDEFINED;
esif PSTATE.EL == EL3 then
  TTBR0_EL3 = X[t];
The TTBR1_EL1 characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the higher VA range in the EL1&0 stage 1 translation regime, and other information for this translation regime.

**Configuration**

AArch64 System register TTBR1_EL1 bits [63:0] are architecturally mapped to AArch32 System register TTBR1[63:0].

**Attributes**

TTBR1_EL1 is a 64-bit register.

**Field descriptions**

The TTBR1_EL1 bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**ASID, bits [63:48]**

An ASID for the translation table base address. The TCR_EL1.A1 field selects either TTBR0_EL1.ASID or TTBR1_EL1.ASID.

If the implementation has only 8 bits of ASID, then the upper 8 bits of this field are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**BADDR[47:1], bits [47:1]**

Translation table base address:

- Bits A[47:x] of the stage 1 translation table base address bits are in register bits[47:x].
- Bits A[(x-1):0] of the stage 1 translation table base address are zero.

Address bit x is the minimum address bit required to align the translation table to the size of the table. The smallest permitted value of x is 6. The AArch64 Virtual Memory System Architecture chapter describes how x is calculated based on the value of TCR_EL1.TSZ, the translation stage, and the translation granule size.

**Note**

A translation table is required to be aligned to the size of the table. If a table contains fewer than eight entries, it must be aligned on a 64 byte address boundary.

If the value of TCR_EL1.IPS is not 0b110, then:

- Register bits[(x-1):1] are RES0.
- If the implementation supports 52-bit PAs and IPAs, then bits A[51:48] of the stage 1 translation table base address are 0b0000.
If Feat_Lpa is implemented and the value of TCR_EL1.IPS is 0b110, then:

- Bits A[51:48] of the stage 1 translation table base address bits are in register bits[5:2].
- Register bit[1] is RES0.
- When x>6, register bits[(x-1):6] are RES0.

**Note**

TCR_EL1.IPS==0b110 is permitted when:

- Feat_Lpa is implemented and the 64KB translation granule is used.
- Feat_Lpa2 is implemented and the 4KB or 16KB translation granule is used.

When the value of ID_AA64MMFR0_EL1_PARange indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register when TCR_EL1.IPS is 0b110 and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If any register bit[47:1] that is defined as RES0 has the value 1 when a translation table walk is done using TTBR1_EL1, then the translation table base address might be misaligned, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Bits A[(x-1):0] of the stage 1 translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CnP, bit [0]**

*When Feat_TTCNP is implemented:*

Common not Private. This bit indicates whether each entry that is pointed to by TTBR1_EL1 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR1_EL1.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0   | The translation table entries pointed to by TTBR1_EL1, for the current translation regime and ASID, are permitted to differ from corresponding entries for TTBR1_EL1 for other PEs in the Inner Shareable domain. This is not affected by:  
- The value of TTBR1_EL1.CnP on those other PEs.  
- The value of the current ASID.  
- If EL2 is implemented and enabled in the current Security state, the value of the current VMID. |
| 0b1   | The translation table entries pointed to by TTBR1_EL1 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR1_EL1.CnP is 1 and all of the following apply:  
- The translation table entries are pointed to by TTBR1_EL1.  
- The translation tables relate to the same translation regime.  
- The ASID is the same as the current ASID.  
- If EL2 is implemented and enabled in the current Security state, the value of the current VMID. |

This field is permitted to be cached in a TLB.

When a TLB combines entries from stage 1 translation and stage 2 translation into a single entry, that entry can only be shared between different PEs if the value of the CnP bit is 1 for both stage 1 and stage 2.

**Note**

If the value of the TTBR1_EL1.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR1_EL1s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are CONSTRAINED.
**UNPREDICTABLE**, see ‘CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values’.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Accessing the TTBR1_EL1**

When **HCR_EL2.E2H** is 1, without explicit synchronization, access from EL3 using the mnemonic TTBR1_EL1 or TTBR1_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Access to this register use the following encodings:

**MRS <Xt>, TTBR1_EL1**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TRVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TTBR1_EL1 == '1'
  then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elseif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x210];
  else
    return TTBR1_EL1;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return TTBR1_EL2;
  else
    return TTBR1_EL1;
elsif PSTATE.EL == EL3 then
  return TTBR1_EL1;

**MSR TTBR1_EL1, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TTBR1_EL1 == '1'
    then
      AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x210] = X[t];
  else
    TTBR1_EL1 = X[t];
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      TTBR1_EL2 = X[t];
    else
      TTBR1_EL1 = X[t];
  elsif PSTATE.EL == EL3 then
    TTBR1_EL1 = X[t];
  else
    TTBR1_EL1 = X[t];
else
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x210];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return TTBR1_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return TTBR1_EL1;
  else
    UNDEFINED;
MSR TTBR1_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWTR_EL2.TTBR1_EL1 == '1'
    then
      AArch64.SystemAccessTrap(EL2, 0x10);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
    NVMem[0x210] = X[t];
  else
    TTBR1_EL1 = X[t];
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
      TTBR1_EL2 = X[t];
    else
      TTBR1_EL1 = X[t];
  elsif PSTATE.EL == EL3 then
    TTBR1_EL1 = X[t];
  else
    TTBR1_EL1 = X[t];
else
  UNDEFINED;
elsif PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x210];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x10);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return TTBR1_EL1;
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    return TTBR1_EL1;
  else
    UNDEFINED;
MSR TTBR1_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x210] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elseif PSTATE_EL == EL2 then
    if HCR_EL2.E2H == '1' then
        TTBR1_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE_EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        TTBR1_EL1 = X[t];
    else
        UNDEFINED;
The TTBR1_EL2 characteristics are:

**Purpose**

When HCR_EL2.E2H is 1, holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the higher VA range in the EL2&0 translation regime, and other information for this translation regime.

**Note**

When HCR_EL2.E2H is 0, the contents of this register are ignored by the PE, except for a direct read or write of the register.

**Configuration**

This register is present only when FEAT_VHE is implemented. Otherwise, direct accesses to TTBR1_EL2 are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

TTBR1_EL2 is a 64-bit register.

**Field descriptions**

The TTBR1_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
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<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASID</td>
<td>BADDR[47:1]</td>
<td>CnP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**ASID, bits [63:48]**

An ASID for the translation table base address. The TCR_EL2.A1 field selects either TTBR0_EL2.ASID or TTBR1_EL2.ASID.

If the implementation has only 8 bits of ASID, then the upper 8 bits of this field are **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**BADDR[47:1], bits [47:1]**

Translation table base address:

- Bits A[47:x] of the stage 1 translation table base address bits are in register bits[47:x].
- Bits A[(x-1):0] of the stage 1 translation table base address are zero.

Address bit x is the minimum address bit required to align the translation table to the size of the table. The smallest permitted value of x is 6. The AArch64 Virtual Memory System Architecture chapter describes how x is calculated based on the value of TCR_EL2.T1SZ, the translation stage, and the translation granule size.

**Note**
A translation table is required to be aligned to the size of the table. If a table contains fewer than eight entries, it must be aligned on a 64 byte address boundary.

If the value of \texttt{TCR EL2}.(1)PS is not 0b110, then:

• Register bits[(x-1):1] are res0.
• If the implementation supports 52-bit PAs and IPAs, then bits A[51:48] of the stage 1 translation table base address are 0b0000.

If \texttt{FEAT LPA} is implemented and the value of \texttt{TCR EL2}.(1)PS is 0b110, then:

• Bits A[51:48] of the stage 1 translation table base address bits are in register bits[5:2].
• Register bit[1] is res0.
• When x>6, register bits[(x-1):6] are res0.

\textbf{Note}

The OA size specified by \texttt{TCR EL2}.(1)PS is determined as follows:

• The value of \texttt{TCR EL2}.PS when the value of \texttt{HCR EL2} E2H is 0.
• The value of \texttt{TCR EL2}.IPS when the value of \texttt{HCR EL2} E2H is 1.

\texttt{TCR EL2}.(1)PS==0b110 is permitted when:

• \texttt{FEAT LPA} is implemented and the 64KB translation granule is used.
• \texttt{FEAT LPA2} is implemented and the 4KB or 16KB translation granule is used.

When the value of \texttt{ID AA64MMFRO EL1} PARange indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register when \texttt{TCR EL2}.(1)PS is 0b110 and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If any register bit[47:1] that is defined as res0 has the value 1 when a translation table walk is done using \texttt{TTBR1 EL2}, then the translation table base address might be misaligned, with effects that are \textsc{constrained} \textsc{unpredictable}, and must be one of the following:

• Bits A[(x-1):0] of the stage 1 translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
• The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally \textsc{unknown} value.

\textbf{CnP, bit [0]}

\textit{When FEAT_TTCNP is implemented:}

Common not Private. This bit indicates whether each entry that is pointed to by TBR1_EL2 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBRI_EL2.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0 | The translation table entries pointed to by TTBRI_EL2 for the current ASID are permitted to differ from corresponding entries for TTBRI_EL2 for other PEs in the Inner Shareable domain. This is not affected by:
  • The value of TTBRI_EL2.CnP on those other PEs.
  • The value of the current ASID. |

| 0b1 | The translation table entries pointed to by TTBRI_EL2 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBRI_EL2.CnP is 1 and all of the following apply:
  • The translation table entries are pointed to by TTBRI_EL2.
  • The ASID is the same as the current ASID. |

This field is permitted to be cached in a TLB.
• TTBR1_EL2 is accessible only when the value of HCR_EL2.E2H is 1, meaning the current translation regime is the EL2\&0 regime.
• If the value of the TTBR1_EL2.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR1_EL2s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are CONSTRAINED UNPREDICTABLE, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Accessing the TTBR1_EL2**

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic TTBR1_EL2 or TTBR1_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, TTBR1_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return TTBR1_EL2;
elsif PSTATE.EL == EL3 then
  return TTBR1_EL2;

**MSR TTBR1_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TTBR1_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  TTBR1_EL2 = X[t];
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWR_EL2.TTBR1_EL1 == '1'
    then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111'
    then
      return NVMem[0x210];
  else
    return TTBR1_EL1;
  end if;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    return TTBR1_EL2;
  else
    return TTBR1_EL1;
  end if;
elsif PSTATE.EL == EL3 then
  return TTBR1_EL1;
endif;

MSR TTBR1_EL1, <Xt>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.TVM == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWR_EL2.TTBR1_EL1 == '1'
    then
      AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111'
    then
      NVMem[0x210] = X[t];
  else
    TTBR1_EL1 = X[t];
  end if;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    TTBR1_EL2 = X[t];
  else
    TTBR1_EL1 = X[t];
  end if;
elsif PSTATE.EL == EL3 then
  TTBR1_EL1 = X[t];
endif;
The UAO characteristics are:

**Purpose**

Allows access to the User Access Override bit.

**Configuration**

This register is present only when FEAT_UAO is implemented. Otherwise, direct accesses to UAO are UNDEFINED.

**Attributes**

UAO is a 64-bit register.

**Field descriptions**

The UAO bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>UAO</td>
</tr>
<tr>
<td>62</td>
<td>RES0</td>
</tr>
<tr>
<td>61</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>Reserved, RES0</td>
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<td>58</td>
<td>Reserved, RES0</td>
</tr>
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<td>57</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
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<td>Reserved, RES0</td>
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<td>48</td>
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<td>39</td>
<td>Reserved, RES0</td>
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<td>Reserved, RES0</td>
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<td>36</td>
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<tr>
<td>35</td>
<td>Reserved, RES0</td>
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<tr>
<td>34</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:24]**

Reserved, RES0.

**UAO, bit [23]**

User Access Override.

<table>
<thead>
<tr>
<th>UAO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The behavior of LDTR* and STTR* instructions is as defined in the base Armv8 architecture.</td>
</tr>
<tr>
<td>0b1</td>
<td>When executed at EL1, or at EL2 with HCR_EL2.E2H, TGE ({1, 1}), LDTR* and STTR* instructions behave as the equivalent LDR* and STR* instructions.</td>
</tr>
</tbody>
</table>

When executed at EL3, or at EL2 with HCR_EL2.E2H == 0 or HCR_EL2.TGE == 0, the LDTR* and STTR* instructions behave as the equivalent LDR* and STR* instructions, regardless of the setting of the PSTATE.UAO bit.

**Bits [22:0]**

Reserved, RES0.

**Accessing the UAO**

For details on the operation of the MSR (immediate) accessor, see 'MSR (immediate)'.

Accesses to this register use the following encodings:
### MRS <Xt>, UAO

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    return Zeros(40):PSTATE.UAO:Zeros(23);
elsif PSTATE.EL == EL2 then
    return Zeros(40):PSTATE.UAO:Zeros(23);
elsif PSTATE.EL == EL3 then
    return Zeros(40):PSTATE.UAO:Zeros(23);

MSR UAO, <Xt>
```

### MSR UAO, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    PSTATE.UAO = X[t]<23>;
elsif PSTATE.EL == EL2 then
    PSTATE.UAO = X[t]<23>;
elsif PSTATE.EL == EL3 then
    PSTATE.UAO = X[t]<23>;

MSR UAO, #<imm>
```

### MSR UAO, #<imm>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>

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VBAR_EL1, Vector Base Address Register (EL1)

The VBAR_EL1 characteristics are:

**Purpose**

Holds the vector base address for any exception that is taken to EL1.

**Configuration**

AArch64 System register VBAR_EL1 bits [31:0] are architecturally mapped to AArch32 System register `VBAR[31:0]`.

**Attributes**

VBAR_EL1 is a 64-bit register.

**Field descriptions**

The VBAR_EL1 bit assignments are:

<p>| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|</p>
<table>
<thead>
<tr>
<th>Vector Base Address</th>
<th>Vector Base Address</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
</tr>
</tbody>
</table>

**Bits [63:11]**

Vector Base Address. Base address of the exception vectors for exceptions taken to EL1.

**Note**

If the implementation does not support FEAT_LVA, then:

- If tagged addresses are being used, bits [55:48] of VBAR_EL1 must be the same or else the use of the vector address will result in a recursive exception.
- If tagged addresses are not being used, bits [63:48] of VBAR_EL1 must be the same or else the use of the vector address will result in a recursive exception.

If the implementation supports FEAT_LVA, then:

- If tagged addresses are being used, bits [55:52] of VBAR_EL1 must be the same or else the use of the vector address will result in a recursive exception.
- If tagged addresses are not being used, bits [63:52] of VBAR_EL1 must be the same or else the use of the vector address will result in a recursive exception.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [10:0]**

Reserved, RES0.
Accessing the VBAR_EL1

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic VBAR_EL1 or VBAR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, VBAR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.VBAR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x250];
    else
        return VBAR_EL1;
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '1' then
            return VBAR_EL2;
        elsif PSTATE.EL == EL3 then
            return VBAR_EL1;
    if EL2Enabled() && HCR_EL2.E2H == '1' then
        return VBAR_EL2;
    else
        return VBAR_EL1;
    elsif PSTATE.EL == EL3 then
        VBAR_EL1 = X[t];
else
    VBAR_EL1 = X[t];

MSR VBAR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.VBAR_EL1 == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        NVMem[0x250] = X[t];
    else
        VBAR_EL1 = X[t];
else
    VBAR_EL1 = X[t];
elsif PSTATE.EL == EL3 then
    VBAR_EL1 = X[t];

MRS <Xt>, VBAR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        return NVMem[0x250];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        return VBAR_EL1;
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        return VBAR_EL1;
    else
        UNDEFINED;
else
    UNDEFINED;

MSR VBAR_EL12, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
        NVMem[0x250] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '1' then
        VBAR_EL1 = X[t];
    else
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
        VBAR_EL1 = X[t];
    else
        UNDEFINED;
VBAR_EL2, Vector Base Address Register (EL2)

The VBAR_EL2 characteristics are:

Purpose

Holds the vector base address for any exception that is taken to EL2.

Configuration

AArch64 System register VBAR_EL2 bits [31:0] are architecturally mapped to AArch32 System register HVBAR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

Attributes

VBAR_EL2 is a 64-bit register.

Field descriptions

The VBAR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Vector Base Address</th>
<th>RES0</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>60</td>
<td>59</td>
<td>58</td>
</tr>
<tr>
<td>57</td>
<td>56</td>
<td>55</td>
</tr>
<tr>
<td>54</td>
<td>53</td>
<td>52</td>
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<tr>
<td>51</td>
<td>50</td>
<td>49</td>
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<td>48</td>
<td>47</td>
<td>46</td>
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<tr>
<td>45</td>
<td>44</td>
<td>43</td>
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<tr>
<td>42</td>
<td>41</td>
<td>40</td>
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<tr>
<td>39</td>
<td>38</td>
<td>37</td>
</tr>
<tr>
<td>36</td>
<td>35</td>
<td>34</td>
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<tr>
<td>33</td>
<td>32</td>
<td>31</td>
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<tr>
<td>30</td>
<td>29</td>
<td>28</td>
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<td>27</td>
<td>26</td>
<td>25</td>
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<td>24</td>
<td>23</td>
<td>22</td>
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<td>21</td>
<td>20</td>
<td>19</td>
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<td>18</td>
<td>17</td>
<td>16</td>
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<tr>
<td>15</td>
<td>14</td>
<td>13</td>
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<tr>
<td>12</td>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:11]

Vector Base Address. Base address of the exception vectors for exceptions taken to EL2.

Note

If FEAT_LVA is implemented:

- If HCR_EL2.E2H == 0b1:
  - If tagged addresses are being used, bits [55:52] of VBAR_EL2 must be the same or else the use of the vector address will result in a recursive exception.
  - If tagged addresses are not being used, bits [63:52] of VBAR_EL2 must be the same or else the use of the vector address will result in a recursive exception.
- If HCR_EL2.E2H == 0b0:
  - If tagged addresses are being used, bits [55:52] of VBAR_EL2 must be 0 or else the use of the vector address will result in a recursive exception.
  - If tagged addresses are not being used, bits [63:52] of VBAR_EL2 must be 0 or else the use of the vector address will result in a recursive exception.

If FEAT_LVA is not implemented:

- If HCR_EL2.E2H == 0b1:
  - If tagged addresses are being used, bits [55:48] of VBAR_EL2 must be the same or else the use of the vector address will result in a recursive exception.
If tagged addresses are not being used, bits [63:48] of VBAR_EL2 must be the same or else the use of the vector address will result in a recursive exception.

- If HCR_EL2.E2H == 0b0:
  - If tagged addresses are being used, bits [55:48] of VBAR_EL2 must be 0 or else the use of the vector address will result in a recursive exception.
  - If tagged addresses are not being used, bits [63:48] of VBAR_EL2 must be 0 or else the use of the vector address will result in a recursive exception.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Bits [10:0]

Reserved, RES0.

### Accessing the VBAR_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic VBAR_EL2 or VBAR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

**MRS <Xt>, VBAR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return VBAR_EL2;
elsif PSTATE.EL == EL3 then
  return VBAR_EL2;

**MSR VBAR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  VBAR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  VBAR_EL2 = X[t];
MRS <Xt>, VBAR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then  
  UNDEFINED;
elsif PSTATE.EL == EL1 then  
  if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then  
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWR_EL2.VBAR_EL1 == '1' then  
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then  
    NVMem[0x250] = X[t];
  else  
    return VBAR_EL1;
  endif
elsif PSTATE.EL == EL2 then  
  if HCR_EL2.E2H == '1' then  
    VBAR_EL2 = X[t];
  else  
    VBAR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL3 then  
  VBAR_EL1 = X[t];
endif

MSR VBAR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then  
  UNDEFINED;
elsif PSTATE.EL == EL1 then  
  if EL2Enabled() && HCR_EL2.<NV2,NV1> == '01' then  
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGWR_EL2.VBAR_EL1 == '1' then  
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then  
    NVMem[0x250] = X[t];
  else  
    VBAR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL2 then  
  if HCR_EL2.E2H == '1' then  
    VBAR_EL2 = X[t];
  else  
    VBAR_EL1 = X[t];
  endif
elsif PSTATE.EL == EL3 then  
  VBAR_EL1 = X[t];
endif

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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**Purpose**

Holds the vector base address for any exception that is taken to EL3.

**Configuration**

This register is present only when EL3 is implemented. Otherwise, direct accesses to VBAR_EL3 are **UNDEFINED**.

**Attributes**

VBAR_EL3 is a 64-bit register.

**Field descriptions**

The VBAR_EL3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>62</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>61</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>60</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>59</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>58</td>
<td>Vector Base Address</td>
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<tr>
<td>57</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>56</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>55</td>
<td>Vector Base Address</td>
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<tr>
<td>54</td>
<td>Vector Base Address</td>
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<tr>
<td>53</td>
<td>Vector Base Address</td>
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<tr>
<td>52</td>
<td>Vector Base Address</td>
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<tr>
<td>51</td>
<td>Vector Base Address</td>
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<tr>
<td>50</td>
<td>Vector Base Address</td>
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<tr>
<td>49</td>
<td>Vector Base Address</td>
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<tr>
<td>48</td>
<td>Vector Base Address</td>
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<tr>
<td>47</td>
<td>Vector Base Address</td>
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<td>46</td>
<td>Vector Base Address</td>
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<td>45</td>
<td>Vector Base Address</td>
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<tr>
<td>44</td>
<td>Vector Base Address</td>
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<td>43</td>
<td>Vector Base Address</td>
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<td>42</td>
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<td>41</td>
<td>Vector Base Address</td>
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<td>40</td>
<td>Vector Base Address</td>
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<td>38</td>
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<td>Vector Base Address</td>
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<td>35</td>
<td>Vector Base Address</td>
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<tr>
<td>34</td>
<td>Vector Base Address</td>
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<tr>
<td>33</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>32</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>31</td>
<td>Bits [63:11]</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>22</td>
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<td>21</td>
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<td>Reserved, RES0</td>
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<td>Reserved, RES0</td>
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<td>13</td>
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<td>12</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0</td>
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<td>10</td>
<td>Reserved, RES0</td>
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<td>6</td>
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<tr>
<td>5</td>
<td>Reserved, RES0</td>
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<td>4</td>
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<tr>
<td>3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [63:11]**

Vector Base Address. Base address of the exception vectors for exceptions taken to EL3.

**Note**

If the implementation does not support FEAT_LVA, then:

- If tagged addresses are being used, bits [55:48] of VBAR_EL3 must be 0 or else the use of the vector address will result in a recursive exception.
- If tagged addresses are not being used, bits [63:48] of VBAR_EL3 must be 0 or else the use of the vector address will result in a recursive exception.

If the implementation supports FEAT_LVA, then:

- If tagged addresses are being used, bits [55:52] of VBAR_EL3 must be 0 or else the use of the vector address will result in a recursive exception.
- If tagged addresses are not being used, bits [63:52] of VBAR_EL3 must be 0 or else the use of the vector address will result in a recursive exception.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [10:0]**

Reserved, RES0.

**Accessing the VBAR_EL3**

Accesses to this register use the following encodings:
MRS <Xt>, VBAR_EL3

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    return VBAR_EL3;

MSR VBAR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    VBAR_EL3 = X[t];
The VDISR_EL2 characteristics are:

**Purpose**

Records that a virtual SError interrupt has been consumed by an ESB instruction executed at EL1.

An indirect write to VDISR_EL2 made by an ESB instruction does not require an explicit synchronization operation for the value written to be observed by a direct read of DISR_EL1 or DISR occurring in program order after the ESB instruction.

**Configuration**

AArch64 System register VDISR_EL2 bits [31:0] are architecturally mapped to AArch32 System register VDISR[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to VDISR_EL2 are UNDEFINED.

If EL2 is not implemented, this register is res0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VDISR_EL2 is a 64-bit register.

**Field descriptions**

The VDISR_EL2 bit assignments are:

### When EL1 is using AArch64:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>res0</td>
<td>IDS</td>
<td>ISS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, res0.

**A, bit [31]**

Set to 1 when an ESB instruction defers a virtual SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [30:25]**

Reserved, res0.

**IDS, bit [24]**

The value copied from VESR_EL2.IDS.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
ISS, bits [23:0]

The value copied from VSESR_EL2.ISS.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**When EL1 is using AArch32 and VDISR_EL2.LPAE == 0:**

<table>
<thead>
<tr>
<th>RES0</th>
<th>AET</th>
<th>RES0</th>
<th>ExT</th>
<th>FS(4)</th>
<th>LPAE</th>
<th>RES0</th>
<th>FS[3:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**A, bit [31]**

Set to 1 when an ESB instruction defers a virtual SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [30:16]**

Reserved, RES0.

**AET, bits [15:14]**

The value copied from VSESR_EL2.AET.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [13]**

Reserved, RES0.

**ExT, bit [12]**

The value copied from VSESR_EL2.ExT.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [11]**

Reserved, RES0.

**FS, bits [10, 3:0]**

Fault status code. Set to 0b10110 when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>FS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10110</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The FS field is split as follows:

- FS[4] is VDISR_EL2[10].
- FS[3:0] is VDISR_EL2[3:0].
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**LPAE, bit [9]**

Format.

Set to **TTBCR.EAE** when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [8:4]**

Reserved, **RES0**.

**When EL1 is using AArch32 and VDISR_EL2.LPAE == 1:**

|63|62|61|60|59|58|57|56|55|54|53|52|51|50|49|48|47|46|45|44|43|42|41|40|39|38|37|36|35|34|33|32|
|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| **A** | **RES0** | **AET** | **RES0** | **Ext** | **RES0** | **LPAE** | **RES0** | **STATUS** |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:32]**

Reserved, **RES0**.

**A, bit [31]**

Set to 1 when an ESB instruction defers a virtual SError interrupt.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [30:16]**

Reserved, **RES0**.

**AET, bits [15:14]**

The value copied from **VSESR_EL2.AET**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [13]**

Reserved, **RES0**.

**ExT, bit [12]**

The value copied from **VSESR_EL2.ExT**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [11:10]**

Reserved, **RES0**.
LPAE, bit [9]

Format.

Set to TTBCE.AE when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [8:6]

Reserved, RES0.

STATUS, bits [5:0]

Fault status code. Set to 0b010001 when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the VDISR_EL2

An indirect write to VDISR_EL2 made by an ESB instruction does not require an explicit synchronization operation for the value that is written to be observed by a direct read of DISR_EL1 or DISR occurring in program order after the ESB instruction.

Accesses to this register use the following encodings:

### MRS <Xt>, VDISR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
define_MRS_VDISR_EL2:
    if PSTATE.EL == EL0 then
        UNDEFINED;
    elif PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
            return NVMem[0x500];
        elif EL2Enabled() && HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x18);
        else
            UNDEFINED;
    elif PSTATE.EL == EL2 then
        return VDISR_EL2;
    elsif PSTATE.EL == EL3 then
        return VDISR_EL2;
    endif
enddefine_MRS_VDISR_EL2
```

### MSR VDISR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsf if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x500] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end if;
elsf if PSTATE.EL == EL2 then
    VDISR_EL2 = X[t];
elsf if PSTATE.EL == EL3 then
    VDISR_EL2 = X[t];

MRS <Xt>, DISR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsf if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AMO == '1' then
        return VDISR_EL2;
    else
        return DISR_EL1;
    end if;
elsf if PSTATE.EL == EL2 then
    return DISR_EL1;
elsf if PSTATE.EL == EL3 then
    return DISR_EL1;

MSR DISR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsf if PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.AMO == '1' then
        VDISR_EL2 = X[t];
    else
        DISR_EL1 = X[t];
    end if;
elsf if PSTATE.EL == EL2 then
    DISR_EL1 = X[t];
elsf if PSTATE.EL == EL3 then
    DISR_EL1 = X[t];
VMPIDR_EL2, Virtualization Multiprocessor ID Register

The VMPIDR_EL2 characteristics are:

**Purpose**

Holds the value of the Virtualization Multiprocessor ID. This is the value returned by EL1 reads of MPIDR_EL1.

**Configuration**

AArch64 System register VMPIDR_EL2 bits [31:0] are architecturally mapped to AArch32 System register VMPIDR[31:0].

If EL2 is not implemented, reads of this register return the value of the MPIDR_EL1 and writes to the register are ignored.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VMPIDR_EL2 is a 64-bit register.

**Field descriptions**

The VMPIDR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Affinity level 3</td>
</tr>
<tr>
<td>61</td>
<td>U</td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>59</td>
<td>MT</td>
</tr>
<tr>
<td>58</td>
<td>Affinity level 2</td>
</tr>
<tr>
<td>57</td>
<td>Affinity level 1</td>
</tr>
<tr>
<td>56</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>55</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>54</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>53</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>52</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>51</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>50</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>49</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>48</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>47</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>46</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>45</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>44</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>43</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>42</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>41</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>40</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>39</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>38</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>37</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>36</td>
<td>Reserved, Aff0</td>
</tr>
<tr>
<td>35</td>
<td>Reserved, Aff3</td>
</tr>
<tr>
<td>34</td>
<td>Reserved, Aff2</td>
</tr>
<tr>
<td>33</td>
<td>Reserved, Aff1</td>
</tr>
<tr>
<td>32</td>
<td>Reserved, Aff0</td>
</tr>
</tbody>
</table>

**Bits [63:40]**

Reserved, RES0.

**Aff3, bits [39:32]**

Affinity level 3. See the description of VMPIDR_EL2.Aff0 for more information.

Aff3 is not supported in AArch32 state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [31]**

Reserved, RES1.

**U, bit [30]**

Indicates a Uniprocessor system, as distinct from PE 0 in a multiprocessor system.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Processor is part of a multiprocessor system.</td>
</tr>
<tr>
<td>0b1</td>
<td>Processor is part of a uniprocessor system.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [29:25]
Reserved, RES0.

MT, bit [24]
Indicates whether the lowest level of affinity consists of logical PEs that are implemented using a multithreading type approach. See the description of VMPIDR_EL2.Aff0 for more information about affinity levels.

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Performance of PEs at the lowest affinity level is largely independent.</td>
</tr>
<tr>
<td>0b1</td>
<td>Performance of PEs at the lowest affinity level is very interdependent.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Aff2, bits [23:16]
Affinity level 2. See the description of VMPIDR_EL2.Aff0 for more information.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Aff1, bits [15:8]
Affinity level 1. See the description of VMPIDR_EL2.Aff0 for more information.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Aff0, bits [7:0]
Affinity level 0. This is the affinity level that is most significant for determining PE behavior. Higher affinity levels are increasingly less significant in determining PE behavior. The assigned value of the MPIDR.{Aff2, Aff1, Aff0} or MPIDR_EL1.{Aff3, Aff2, Aff1, Aff0} set of fields of each PE must be unique within the system as a whole.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the VMPIDR_EL2
Accesses to this register use the following encodings:

MRS <Xt>, VMPIDR_EL2

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x050];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        return VMPIDR_EL2;
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        return MPIDR_EL1;
    else
        return VMPIDR_EL2;
```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0x050] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  VMPIDR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    //no operation
  else
    VMPIDR_EL2 = X[t];
end if

MRS <Xt>, MPIDR_EL1

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  else
    return VMPIDR_EL2;
  else
    return MPIDR_EL1;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.MPIDR_EL1 == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  elsif EL2Enabled() then
    return VMPIDR_EL2;
  else
    return MPIDR_EL1;
elsif PSTATE.EL == EL2 then
  return MPIDR_EL1;
elsif PSTATE.EL == EL3 then
  return MPIDR_EL1;
The VNCR_EL2 characteristics are:

**Purpose**

When FEAT_NV2 is implemented, holds the base address that is used to define the memory location that is accessed by transformed reads and writes of System registers.

**Configuration**

This register is present only when FEAT_NV2 is implemented. Otherwise, direct accesses to VNCR_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VNCR_EL2 is a 64-bit register.

**Field descriptions**

The VNCR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RESS | BADDR |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**RESS, bits [63:53]**

Reserved, Sign extended. If the bits marked as RESS do not all have the same value, then there is a CONSTRAINED UNPREDICTABLE choice between:

- Generating an EL2 translation regime Translation abort on use of the VNCR_EL2 register.
- Bits[63:49] of VNCR_EL2 are treated as the same value as bit[48] for all purposes other than reading back the register.
- Bits[63:49] of VNCR_EL2 are treated as the same value as bit[48] for all purposes.
- If the virtual address space for EL2 supports more than 48 bits, bits[63:53] of VNCR_EL2 are treated as the same value as bit[52] for all purposes other than reading back the register.
- If the virtual address space for EL2 supports more than 48 bits, bits[63:53] of VNCR_EL2 are treated as the same value as bit[52].

Where the EL2 translation regime has upper and lower address ranges, bit[52] is used to select between those address ranges to determine if the address space supports more than 48 bits.

**BADDR, bits [52:12]**

Base Address. If the virtual address space for EL2 does not support more than 48 bits, then bits [52:49] are RESS.

When a register read/write is transformed to be a Load or Store, the address of the load/store is to SignOffset(VNCR_EL2.BADDR:Offset<11:0>, 64).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [11:0]**

Reserved, RES0.
Accessing the VNCR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, VNCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x0B00];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end;
elsif PSTATE.EL == EL2 then
    return VNCR_EL2;
elsif PSTATE.EL == EL3 then
    return VNCR_EL2;

MSR VNCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x0B00] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end;
elsif PSTATE.EL == EL2 then
    VNCR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    VNCR_EL2 = X[t];
VPIDR_EL2, Virtualization Processor ID Register

The VPIDR_EL2 characteristics are:

**Purpose**

Holds the value of the Virtualization Processor ID. This is the value returned by EL1 reads of MIDR_EL1.

**Configuration**

AArch64 System register VPIDR_EL2 bits [31:0] are architecturally mapped to AArch32 System register VPIDR[31:0].

If EL2 is not implemented, reads of this register return the value of the MIDR_EL1 and writes to the register are ignored.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VPIDR_EL2 is a 64-bit register.

**Field descriptions**

The VPIDR_EL2 bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| RES0   |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

**Bits [63:32]**

Reserved, RES0.

**Implementer, bits [31:24]**

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>ASCII representation</th>
<th>Implementer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x41</td>
<td>A</td>
<td>Arm Limited</td>
</tr>
<tr>
<td>0x42</td>
<td>B</td>
<td>Broadcom Corporation</td>
</tr>
<tr>
<td>0x43</td>
<td>C</td>
<td>Cavium Inc.</td>
</tr>
<tr>
<td>0x44</td>
<td>D</td>
<td>Digital Equipment Corporation</td>
</tr>
<tr>
<td>0x49</td>
<td>I</td>
<td>Infineon Technologies AG</td>
</tr>
<tr>
<td>0x40</td>
<td>M</td>
<td>Motorola or Freescale</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Semiconductor Inc.</td>
</tr>
<tr>
<td>0x4E</td>
<td>N</td>
<td>NVIDIA Corporation</td>
</tr>
<tr>
<td>0x50</td>
<td>P</td>
<td>Applied Micro Circuits Corporation</td>
</tr>
<tr>
<td>0x51</td>
<td>Q</td>
<td>Qualcomm Inc.</td>
</tr>
<tr>
<td>0x56</td>
<td>V</td>
<td>Marvell International Ltd.</td>
</tr>
<tr>
<td>0x69</td>
<td>i</td>
<td>Intel Corporation</td>
</tr>
</tbody>
</table>

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Variant, bits [23:20]**

An implementation-defined variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Architecture, bits [19:16]**

Architecture version. Defined values are:

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv4.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv4T.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv5 (obsolete).</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv5T.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv5TE.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv5TEJ.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv6.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Architectural features are individually identified in the ID_* registers, see 'ID registers'.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PartNum, bits [15:4]**

An implementation-defined primary part number for the device.

On processors implemented by Arm, if the top four bits of the primary part number are 0x0 or 0x7, the variant and architecture are encoded differently.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Revision, bits [3:0]**

An implementation-defined revision number for the device.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the VPIDR_EL2**

Accesses to this register use the following encodings:

\[
\text{MRS} \ <Xt>, \ \text{VPIDR\_EL2}
\]

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x088];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return VPIDR_EL2;
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    return MIDR_EL1;
  else
    return VPIDR_EL2;
endif

MSR VPIDR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if IsFeatureImplemented(FEAT_IDST) then
    if EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    else
      AArch64.SystemAccessTrap(EL1, 0x18);
    else
      UNDEFINED;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HFGRTR_EL2.MIDR_EL1 == '1' then
      AArch64.SystemAccessTrap(EL2, 0x18);
    elsif EL2Enabled() then
      return VPIDR_EL2;
    else
      return MIDR_EL1;
  elsif PSTATE.EL == EL2 then
    return MIDR_EL1;
  elsif PSTATE.EL == EL3 then
    return MIDR_EL1;
endif

MRS <Xt>, MIDR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
The VESR_EL2 characteristics are:

**Purpose**

Provides the syndrome value reported to software on taking a virtual SError interrupt exception to EL1, or on executing an ESB instruction at EL1.

When the virtual SError interrupt is taken to EL1 using AArch64, then the syndrome value is reported in ESR_EL1.

When the virtual SError interrupt is taken to EL1 using AArch32, then the syndrome value is reported in DFSR.{AET, Ext} and the remainder of DFSR is set as defined by VMSAv8-32. For more information, see The AArch32 Virtual Memory System Architecture.

When the virtual SError interrupt is deferred by an ESB instruction, then the syndrome value is written to VDISR_EL2.

**Configuration**

AArch64 System register VESR_EL2 bits [31:0] are architecturally mapped to AArch32 System register VDFSR[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to VESR_EL2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VESR_EL2 is a 64-bit register.

**Field descriptions**

The VESR_EL2 bit assignments are:

**When EL1 is using AArch32:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:16]**

Reserved, RES0.

**AET, bits [15:14]**

When a virtual SError interrupt is taken to EL1 using AArch32, DFSR[15:4] is set to VESR_EL2.AET.

When a virtual SError interrupt is deferred by an ESB instruction, VDISR_EL2[15:4] is set to VESR_EL2.AET.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [13]
Reserved, RES0.

ExT, bit [12]

When a virtual SError interrupt is taken to EL1 using AArch32, DFSR[12] is set to VSESR_EL2.ExT.
When a virtual SError interrupt is deferred by an ESB instruction, VDISR_EL2[12] is set to VSESR_EL2.ExT.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [11:0]
Reserved, RES0.

When EL1 is using AArch64:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | IDS | RES0 | ISS |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0 |

Bits [63:25]
Reserved, RES0.

IDS, bit [24]

When a virtual SError interrupt is taken to EL1 using AArch64, ESR_EL1[24] is set to VSESR_EL2.IDS.
When a virtual SError interrupt is deferred by an ESB instruction, VDISR_EL2[24] is set to VSESR_EL2.IDS.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

ISS, bits [23:0]

When a virtual SError interrupt is taken to EL1 using AArch64, ESR_EL1[23:0] is set to VSESR_EL2.ISS.
When a virtual SError interrupt is deferred by an ESB instruction, VDISR_EL2[23:0] is set to VSESR_EL2.ISS.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the VSESR_EL2

Accesses to this register use the following encodings:

MRS <Xt>, VSESR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0×508];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return VSESR_EL2;
elsif PSTATE.EL == EL3 then
  return VSESR_EL2;

MSR VSESR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    NVMem[0×508] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  VSESR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  VSESR_EL2 = X[t];
VSTCR_EL2, Virtualization Secure Translation Control Register

The VSTCR_EL2 characteristics are:

**Purpose**

The control register for stage 2 of the Secure EL1&0 translation regime.

**Configuration**

This register is present only when FEAT_SEL2 is implemented. Otherwise, direct accesses to VSTCR_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VSTCR_EL2 is a 64-bit register.

**Field descriptions**

The VSTCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td>SL2</td>
</tr>
<tr>
<td>61</td>
<td>RES0</td>
</tr>
<tr>
<td>60</td>
<td>SA</td>
</tr>
<tr>
<td>59</td>
<td>SW</td>
</tr>
<tr>
<td>58</td>
<td>RES0</td>
</tr>
<tr>
<td>57</td>
<td>TG0</td>
</tr>
<tr>
<td>56</td>
<td>RES0</td>
</tr>
<tr>
<td>55</td>
<td>T0S0</td>
</tr>
<tr>
<td>54</td>
<td>SL0</td>
</tr>
<tr>
<td>53</td>
<td>RES0</td>
</tr>
<tr>
<td>52</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td></td>
</tr>
<tr>
<td>50</td>
<td></td>
</tr>
<tr>
<td>49</td>
<td></td>
</tr>
<tr>
<td>48</td>
<td></td>
</tr>
<tr>
<td>47</td>
<td></td>
</tr>
<tr>
<td>46</td>
<td></td>
</tr>
<tr>
<td>45</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
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<tr>
<td>43</td>
<td></td>
</tr>
<tr>
<td>42</td>
<td></td>
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<tr>
<td>41</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td></td>
</tr>
<tr>
<td>38</td>
<td></td>
</tr>
<tr>
<td>37</td>
<td></td>
</tr>
<tr>
<td>36</td>
<td></td>
</tr>
<tr>
<td>35</td>
<td></td>
</tr>
<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

Any of the bits in VSTCR_EL2 are permitted to be cached in a TLB.

**Bits [63:34]**

Reserved, RES0.

**SL2, bit [33]**

*When FEAT_LPA2 is implemented:*

Starting level of the Secure stage 2 translation lookup controlled by VSTCR_EL2.

If VTCR_EL2.DS == 1, then VSTCR_EL2.SL2, in combination with VSTCR_EL2.SL0, gives encodings for the Secure stage 2 translation table walk initial lookup level.

If VTCR_EL2.DS == 0, then VSTCR_EL2.SL2 is RES0.

If the translation granule size is not 4KB, then this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
**Bit [32]**

Reserved, RES0.

**Bit [31]**

Reserved, RES1.

**SA, bit [30]**

Secure stage 2 translation output address space.

<table>
<thead>
<tr>
<th>SA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All stage 2 translations for the Secure IPA space access the Secure PA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>All stage 2 translations for the Secure IPA space access the Non-secure PA space.</td>
</tr>
</tbody>
</table>

When the value of VSTCR_EL2.SW is 1, this bit behaves as 1 for all purposes other than reading back the value of the bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**SW, bit [29]**

Secure stage 2 translation address space.

<table>
<thead>
<tr>
<th>SW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All stage 2 translation table walks for the Secure IPA space are to the Secure PA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>All stage 2 translation table walks for the Secure IPA space are to the Non-secure PA space.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [28:16]**

Reserved, RES0.

**TG0, bits [15:14]**

Secure stage 2 granule size for **VSTTBR_EL2**.

<table>
<thead>
<tr>
<th>TG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>16KB.</td>
</tr>
</tbody>
</table>

Other values are reserved.

If **FEAT_GTG** is implemented, **ID_AA64MMFR0_EL1** {TGran4_2, TGran16_2, TGran64_2} indicate which granule sizes are supported for Level 2 translation.

If **FEAT_GTG** is not implemented, **ID_AA64MMFR0_EL1** {TGran4, TGran16, TGran64} indicate which granule sizes are supported.

If the value is programmed to either a reserved value, or a size that has not been implemented, then for all purposes other than read back from this register, the hardware will treat the field as if it has been programmed to an **IMPLEMENTATION DEFINED** choice of the sizes that has been implemented.

It is **IMPLEMENTATION DEFINED** whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [13:8]

Reserved, RES0.

SL0, bits [7:6]

When FEAT_TTST is implemented:

Starting level of the Secure stage 2 translation lookup, controlled by VSTCR_EL2. The meaning of this field depends on the value of VSTCR_EL2.TG0.

<table>
<thead>
<tr>
<th>SL0</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b00  | If VSTCR_EL2.TG0 is 0b00 (4KB granule):  
       | - If FEAT_LPA2 is not implemented, start at level 2.  
       | - If FEAT_LPA2 is implemented and VSTCR_EL2.SL2 is 0b0, start at level 2.  
       | - If FEAT_LPA2 is implemented and VSTCR_EL2.SL2 is 0b1, start at level -1. |
|       | If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 3. |
| 0b01  | If VSTCR_EL2.TG0 is 0b00 (4KB granule):  
       | - If FEAT_LPA2 is not implemented, start at level 1.  
       | - If FEAT_LPA2 is implemented and VSTCR_EL2.SL2 is 0b0, start at level 1.  
       | - If FEAT_LPA2 is implemented, the combination of VSTCR_EL2.SL0 == 01 and VSTCR_EL2.SL2 == 1 is reserved. |
|       | If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 2. |
| 0b10  | If VSTCR_EL2.TG0 is 0b00 (4KB granule):  
       | - If FEAT_LPA2 is not implemented, start at level 0.  
       | - If FEAT_LPA2 is implemented and VSTCR_EL2.SL2 is 0b0, start at level 0.  
       | - If FEAT_LPA2 is implemented, the combination of VSTCR_EL2.SL0 == 10 and VSTCR_EL2.SL2 == 1 is reserved. |
|       | If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 1. |
| 0b11  | If VSTCR_EL2.TG0 is 0b00 (4KB granule):  
       | - If FEAT_LPA2 is not implemented, start at level 3.  
       | - If FEAT_LPA2 is implemented and VSTCR_EL2.SL2 is 0b0, start at level 3.  
       | - If FEAT_LPA2 is implemented, the combination of VSTCR_EL2.SL0 == 11 and VSTCR_EL2.SL2 == 1 is reserved. |
|       | If VSTCR_EL2.TG0 is 0b10 (16KB granule) and FEAT_LPA2 is implemented, start at level 0. |

If this field is programmed to a value that is not consistent with the programming of VSTCR_EL2.T0SZ, then a stage 2 level 0 Translation fault is generated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Starting level of the Secure stage 2 translation lookup, controlled by VSTCR_EL2. The meaning of this field depends on the value of VSTCR_EL2.TG0.
SL0 | Meaning
---|---
0b00 | If VSTCR_EL2.TG0 is 0b00 (4KB granule), start at level 2. If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 3.
0b01 | If VSTCR_EL2.TG0 is 0b00 (4KB granule), start at level 1. If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 2.
0b10 | If VSTCR_EL2.TG0 is 0b00 (4KB granule), start at level 0. If VSTCR_EL2.TG0 is 0b10 (16KB granule) or 0b01 (64KB granule), start at level 1.

All other values are reserved. If this field is programmed to a reserved value, or to a value that is not consistent with the programming of VSTCR_EL2.T0SZ, then a stage 2 level 0 Translation fault is generated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by VSTTBR_EL2. The region size is $2^{(64-T0SZ)}$ bytes.

The maximum and minimum possible values for this field depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

If this field is programmed to a value that is not consistent with the programming of SL0, then a stage 2 level 0 Translation fault is generated.

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the VSTCR_EL2**

Accesses to this register use the following encodings:

MRS $<Xt>$, VSTCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x048];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    return VSTCR_EL2;
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    return VSTCR_EL2;

MSR VSTCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
    return NVMem[0x048] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && SCR_EL3.NS == '1' then
    UNDEFINED;
  else
    VSTCR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
  if SCR_EL3.EEL2 == '0' then
    UNDEFINED;
  else
    VSTCR_EL2 = X[t];
VSTTBR_EL2, Virtualization Secure Translation Table Base Register

The VSTTBR_EL2 characteristics are:

**Purpose**

The base register for stage 2 of the Secure EL1&0 translation regime. Holds the base address of the translation table for the initial lookup for stage 2 of an address translation in the Secure EL1&0 translation regime, and other information for this translation stage.

**Configuration**

This register is present only when FEAT_SEL2 is implemented. Otherwise, direct accesses to VSTTBR_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VSTTBR_EL2 is a 64-bit register.

**Field descriptions**

The VSTTBR_EL2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | BADDR |

Any of the bits in VSTTBR_EL2 are permitted to be cached in a TLB.

**Bits [63:48]**

Reserved, RES0.

**BADDR, bits [47:1]**

Translation table base address, A[47:x] or A[51:x].

**Note**

- Translation table base addresses of 52 bits, A[51:x], are supported only in an implementation that includes FEAT_LPA and is using the 64KB translation granule.
- A translation table must be aligned to the size of the table, except that when using a translation table base address larger than 48 bits the minimum alignment of a table containing fewer than eight entries is 64 bytes.

If the value of VTCR_EL2. PS is 0b110, then:

- Register bits[47:z] hold bits[47:z] of the stage 1 translation table base address, where z is determined as follows:
  - If x >= 6 then z=x.
  - Otherwise, z=6.
- When z>x register bits[(z-1):x] are RES0, and bits[(z-1):x] of the translation table base address are zero.
When \( x > 6 \) register bits\([(x-1):6]\) are RES0.
- Register bit[1] is RES0.
- Bits[5:2] of the stage 1 translation table base address are zero.

**Note**

When the value of \( \text{ID}_{\text{AA64MMFR0_EL1}}.\text{PARange} \) indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register with the 64KB translation granule when the Effective value of \( \text{VTCR}_{\text{EL2}}.\text{PS} \) is 0b110 and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If the Effective value of \( \text{VTCR}_{\text{EL2}}.\text{PS} \) is not 0b110 then:

- Register bits[47:x] hold bits[47:x] of the stage 1 translation table base address.
- Register bits[(x-1):1] are RES0.
- If the implementation supports 52-bit PAs and IPAs then bits[51:48] of the translation table base addresses used in this stage of translation are 0b0000.

If any VSTTBR_EL2[47:1] bit that is defined as RES0 has the value 1 when a translation table walk is performed using VSTTBR_EL2, then the translation table base address might be misaligned, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Bits[x-1:0] of the translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is one of the values written to the register or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

The AArch64 Virtual Memory System Architecture chapter describes how \( x \) is calculated based on the value of \( \text{VTCR}_{\text{EL2}}.\text{T0SZ} \), the stage of translation, and the translation granule size.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CnP, bit [0]**

Common not Private, for stage 2 of the Secure EL1&0 translation regime. In an implementation that includes FEAT_TTCNP, indicates whether each entry that is pointed to by VSTTBR_EL2 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of VSTTBR_EL2.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table entries pointed to by VSTTBR_EL2 are permitted to differ from the entries for VSTTBR_EL2 for other PEs in the Inner Shareable domain. This is not affected by the value of the current VMID.</td>
</tr>
<tr>
<td>0b1</td>
<td>The translation table entries pointed to by VSTTBR_EL2 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of VSTTBR_EL2.CnP is 1 and the VMID is the same as the current VMID.</td>
</tr>
</tbody>
</table>

**Note**

If the value of VSTTBR_EL2.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those VSTTBR_EL2s do not point to the same translation table entries when using the current VMID, then the results of translations using VSTTBR_EL2 are CONSTRAINED UNPREDICTABLE, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

When this register has an architecturally-defined reset value, this field resets to a value that is architecturally UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the VSTTBR_EL2**

Accesses to this register use the following encodings:
MRS $<Xt>$, VSTTBR_EL2

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then 
  UNDEFINED;
elsif PSTATE.EL == EL1 then 
  if HaveEL(EL3) && SCR_EL3.NS == '1' then 
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then 
    return NVMem[0x030];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then 
    AArch64.SystemAccessTrap(EL2, 0x18);
  else 
    UNDEFINED;
elsif PSTATE.EL == EL2 then 
  if HaveEL(EL3) && SCR_EL3.NS == '1' then 
    UNDEFINED;
  else 
    VSTTBR_EL2 = $<Xt>$;
elsif PSTATE.EL == EL3 then 
  if SCR_EL3.EEL2 == '0' then 
    UNDEFINED;
  else 
    VSTTBR_EL2 = $<Xt>$;
```

MSR VSTTBR_EL2, $<Xt>$

```
<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
```

if PSTATE.EL == EL0 then 
  UNDEFINED;
elsif PSTATE.EL == EL1 then 
  if HaveEL(EL3) && SCR_EL3.NS == '1' then 
    UNDEFINED;
  elsif EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then 
    NVMem[0x030] = $<t>$;
  elsif EL2Enabled() && HCR_EL2.NV == '1' then 
    AArch64.SystemAccessTrap(EL2, 0x18);
  else 
    UNDEFINED;
elsif PSTATE.EL == EL2 then 
  if HaveEL(EL3) && SCR_EL3.NS == '1' then 
    UNDEFINED;
  else 
    VSTTBR_EL2 = $<Xt>$;
elsif PSTATE.EL == EL3 then 
  if SCR_EL3.EEL2 == '0' then 
    UNDEFINED;
  else 
    VSTTBR_EL2 = $<Xt>$;
```
VTCR_EL2, Virtualization Translation Control Register

The VTCR_EL2 characteristics are:

**Purpose**

The control register for stage 2 of the EL1&0 translation regime.

**Configuration**

AArch64 System register VTCR_EL2 bits [31:0] are architecturally mapped to AArch32 System register VTCR[31:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VTCR_EL2 is a 64-bit register.

**Field descriptions**

The VTCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-34</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>33</td>
<td>SL2, bit [33]</td>
</tr>
<tr>
<td>32-0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

Any of the bits in VTCR_EL2 are permitted to be cached in a TLB.

**Bits [63:34]**

Reserved, RES0.

**SL2, bit [33]**

*When FEAT_LPA2 is implemented:*

Starting level of the stage 2 translation lookup controlled by VTCR_EL2.

If VTCR_EL2.DS == 1, then VTCR_EL2.SL2, in combination with VTCR_EL2.SL0, gives encodings for the stage 2 translation table walk initial lookup level.

If VTCR_EL2.DS == 0, then VTCR_EL2.SL2 is RES0.

If the translation granule size is not 4KB, then this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
**DS, bit [32]**

When **FEAT_LPA2** is implemented:

This field affects 52-bit output addressing when using 4KB and 16KB translation granules in stage 2 of the EL1&0 translation regime.

<table>
<thead>
<tr>
<th>DS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits[49:48] of translation descriptors are RES0. Bits[9:8] in block and page descriptors encode shareability information in the SH[1:0] field. Bits[9:8] in table descriptors are ignored by hardware. The minimum value of VTCR_EL2.T0SZ is 16. Any memory access using a smaller value generates a stage 2 level 0 translation table fault. The minimum value of VSTCR_EL2.T0SZ is 16. Any memory access using a smaller value generates a stage 2 level 0 translation table fault. Output address[51:48] is 0000.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bits[49:48] of translation descriptors hold output address[49:48]. Bits[9:8] in translation descriptors hold output address[51:50]. The shareability information of block and page descriptors for cacheable locations is determined by VTCR_EL2.SH0. The minimum value of VTCR_EL2.T0SZ is 12. Any memory access using a smaller value generates a stage 2 level 0 translation table fault. The minimum value of VSTCR_EL2.T0SZ is 12. Any memory access using a smaller value generates a stage 2 level 0 translation table fault.</td>
</tr>
</tbody>
</table>

**Note**
As FEAT_LPA must be implemented if VTCR_EL2.DS == 1, the minimum values of VTCR_EL2.T0SZ and VSTCR_EL2.T0SZ are 12, as determined by that extension.

For the TLBI range instructions affecting IPA, the format of the argument is changed so that bits[36:0] hold BaseADDR[52:16]. For the 4KB translation granule, bits[15:12] of BaseADDR are treated as 0000. For the 16KB translation granule, bits[15:14] of BaseADDR are treated as 00.

**Note**
This forces alignment of the ranges used by the TLBI range instructions.

This field is RES0 for a 64KB translation granule.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bit [31]**

Reserved, RES1.

**NSA, bit [30]**

When **FEAT_SEL2** is implemented:

Non-secure stage 2 translation output address space.
NSA, bit [29]

When FEAT_SEL2 is implemented:

Non-secure stage 2 translation table address space.

<table>
<thead>
<tr>
<th>NSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All stage 2 translations for the Non-secure IPA space of the Secure EL1&amp;0 translation regime access the Secure PA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>All stage 2 translations for the Non-secure IPA space of the Secure EL1&amp;0 translation regime access the Non-secure PA space.</td>
</tr>
</tbody>
</table>

This bit behaves as 1 for all purposes other than reading back the value of the bit when one of the following is true:

- The PE is executing in Non-secure state.
- The value of VTCR_EL2.NSW is 1.
- The value of VSTCR_EL2.SA is 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

NSW, bit [29]

When FEAT_SEL2 is implemented:

Non-secure stage 2 translation table address space.

<table>
<thead>
<tr>
<th>NSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All stage 2 translation table walks for the Non-secure IPA space of the Secure EL1&amp;0 translation regime are to the Secure PA space.</td>
</tr>
<tr>
<td>0b1</td>
<td>All stage 2 translation table walks for the Non-secure IPA space of the Secure EL1&amp;0 translation regime are to the Non-secure PA space.</td>
</tr>
</tbody>
</table>

When the PE is executing in Non-secure state, this bit behaves as 1 for all purposes other than reading back the value of the bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU62, bit [28]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU62</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[62] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[62] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
HWU61, bit [27]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU61</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[61] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[61] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU60, bit [26]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU60</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[60] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[60] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU59, bit [25]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU59</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[59] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[59] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
**Bits [24:23]**

Reserved, RES0.

**HD, bit [22]**

*When FEAT_HAFDBS is implemented:*

Hardware management of dirty state in stage 2 translations when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>HD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 2 hardware management of dirty state disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 2 hardware management of dirty state enabled, only if the VTCR_EL2.HA bit is also set to 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**HA, bit [21]**

*When FEAT_HAFDBS is implemented:*

Hardware Access flag update in Non-secure and Secure stage 2 translations when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>HA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Stage 2 Access flag update disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Stage 2 Access flag update enabled.</td>
</tr>
</tbody>
</table>

**Otherwise:**

Reserved, RES0.

**Bit [20]**

Reserved, RES0.

**VS, bit [19]**

*When FEAT_VMID16 is implemented:*

VMID Size.

<table>
<thead>
<tr>
<th>VS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>8 bit - the upper 8 bits of VTTBR_EL2 and VSTTBR_EL2 are ignored by the hardware, and treated as if they are all zeros, for every purpose except when reading back the register.</td>
</tr>
<tr>
<td>0b1</td>
<td>16 bit - the upper 8 bits of VTTBR_EL2 and VSTTBR_EL2 are used for allocation and matching in the TLB.</td>
</tr>
</tbody>
</table>

If the implementation only supports an 8-bit VMID, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
**PS, bits [18:16]**

Physical address Size for the Second Stage of translation.

<table>
<thead>
<tr>
<th>PS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>32 bits, 4GB.</td>
</tr>
<tr>
<td>0b001</td>
<td>36 bits, 64GB.</td>
</tr>
<tr>
<td>0b010</td>
<td>40 bits, 1TB.</td>
</tr>
<tr>
<td>0b011</td>
<td>42 bits, 4TB.</td>
</tr>
<tr>
<td>0b100</td>
<td>44 bits, 8GB.</td>
</tr>
<tr>
<td>0b101</td>
<td>48 bits, 256TB.</td>
</tr>
<tr>
<td>0b110</td>
<td>52 bits, 4PB.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The reserved values behave in the same way as the 0b101 or 0b110 encoding, but software must not rely on this property as the behavior of the reserved values might change in a future revision of the architecture.

If the translation granularity is not 64KB and FEAT_LPA2 is not implemented, the value 0b110 is treated as reserved.

It is IMPLEMENTATION DEFINED whether an implementation that does not implement FEAT_LPA supports setting the value of 0b110 for the 64KB translation granularity size or whether setting this value behaves as the 0b101 encoding.

In an implementation that supports 52-bit PAs, if the value of this field is not 0b110 or a value treated as 0b110, then bits[51:48] of every translation table base address for the stage of translation controlled by VTCR_EL2 are 0b0000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**TG0, bits [15:14]**

Granule size for the VTTBR_EL2.

<table>
<thead>
<tr>
<th>TG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>16KB.</td>
</tr>
</tbody>
</table>

Other values are reserved.

If FEAT_GTG is implemented, ID_AA64MMFR0_EL1.{TGran4_2, TGran16_2, TGran64_2} indicate which granule sizes are supported for Level 2 translation.

If FEAT_GTG is not implemented, ID_AA64MMFR0_EL1.{TGran4, TGran16, TGran64} indicate which granule sizes are supported.

If the value is programmed to either a reserved value or a size that has not been implemented, then the hardware will treat the field as if it has been programmed to an IMPLEMENTATION DEFINED choice of the sizes that has been implemented for all purposes other than the value read back from this register.

It is IMPLEMENTATION DEFINED whether the value read back is the value programmed or the value that corresponds to the size chosen.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SH0, bits [13:12]**

Shareability attribute for memory associated with translation table walks using VTTBR_EL2 or VSTTBR_EL2.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
ORGN0, bits [11:10]

Outer cacheability attribute for memory associated with translation table walks using VTTBR_EL2 or VSTTBR_EL2.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IRGN0, bits [9:8]

Inner cacheability attribute for memory associated with translation table walks using VTTBR_EL2 or VSTTBR_EL2.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

SL0, bits [7:6]

When FEAT_TTST is implemented:

Starting level of the stage 2 translation lookup, controlled by VTCR_EL2. The meaning of this field depends on the value of VTCR_EL2.TG0.
If VTCR_EL2.TG0 is \(0b00\) (4KB granularity):
- If FEAT_LPA2 is not implemented, start at level 2.
- If FEAT_LPA2 is implemented and VTCR_EL2.SL2 is \(0b0\), start at level 2.
- If FEAT_LPA2 is implemented and VTCR_EL2.SL2 is \(0b1\), start at level -1.

If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 3.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity):
- If FEAT_LPA2 is not implemented, start at level 1.
- If FEAT_LPA2 is implemented and VTCR_EL2.SL2 is \(0b0\), start at level 1.
- If FEAT_LPA2 is implemented, the combination of VTCR_EL2.SL0 == \(0b1\) and VTCR_EL2.SL2 == \(0b1\) is reserved.

If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 2.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity):
- If FEAT_LPA2 is not implemented, start at level 0.
- If FEAT_LPA2 is implemented and VTCR_EL2.SL2 is \(0b0\), start at level 0.
- If FEAT_LPA2 is implemented, the combination of VTCR_EL2.SL0 == \(0b1\) and VTCR_EL2.SL2 == \(0b1\) is reserved.

If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 1.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity):
- If FEAT_LPA2 is not implemented, start at level 3.
- If FEAT_LPA2 is implemented and VTCR_EL2.SL2 is \(0b0\), start at level 3.
- If FEAT_LPA2 is implemented, the combination of VTCR_EL2.SL0 == \(0b1\) and VTCR_EL2.SL2 == \(0b1\) is reserved.

If this field is programmed to a value that is not consistent with the programming of VTCR_EL2.T0SZ, then a stage 2 level 0 Translation fault is generated.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Starting level of the stage 2 translation lookup, controlled by VTCR_EL2. The meaning of this field depends on the value of VTCR_EL2.TG0.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity), start at level 2. If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 3.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity), start at level 1. If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 2.

If VTCR_EL2.TG0 is \(0b00\) (4KB granularity), start at level 0. If VTCR_EL2.TG0 is \(0b10\) (16KB granularity) or \(0b01\) (64KB granularity), start at level 1.

All other values are reserved. If this field is programmed to a reserved value, or to a value that is not consistent with the programming of VTCR_EL2.T0SZ, then a stage 2 level 0 Translation fault is generated.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**T0SZ, bits [5:0]**

The size offset of the memory region addressed by VTTBR_EL2. The region size is \(2^{(64-T0SZ)}\) bytes.
The maximum and minimum possible values for T0SZ depend on the level of translation table and the memory translation granule size, as described in the AArch64 Virtual Memory System Architecture chapter.

If this field is programmed to a value that is not consistent with the programming of SL0, then a stage 2 level 0 Translation fault is generated.

---

**Note**

For the 4KB translation granule, if FEAT_LPA2 is implemented and this field is less than 16, the translation table walk begins with a level -1 initial lookup.

For the 16KB translation granule, if FEAT_LPA2 is implemented and this field is less than 17, the translation table walk begins with a level 0 initial lookup.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the VTCR_EL2

Any of the bits in VTCR_EL2 are permitted to be cached in a TLB.

Accesses to this register use the following encodings:

**MRS <Xt>, VTCR_EL2**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x040];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    return VTCR_EL2;
elsif PSTATE.EL == EL3 then
    return VTCR_EL2;
endif
```

**MSR VTCR_EL2, <Xt>**

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x040] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    VTCR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    VTCR_EL2 = X[t];
```
VTTBR_EL2, Virtualization Translation Table Base Register

The VTTBR_EL2 characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 2 of an address translation in the EL1&0 translation regime, and other information for this translation regime.

**Configuration**

AArch64 System register VTTBR_EL2 bits [63:0] are architecturally mapped to AArch32 System register VTTBR[63:0].

If EL2 is not implemented, this register is RES0 from EL3.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

VTTBR_EL2 is a 64-bit register.

**Field descriptions**

The VTTBR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>VMID Encoding</th>
<th>BADDR</th>
<th>CnP</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>VMID</td>
<td>BADDR</td>
<td>CnP</td>
</tr>
<tr>
<td>31-0</td>
<td>VMID</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VMID, bits [63:48]**

VMID encoding when FEAT_VMID16 is implemented or (VTCR_EL2.VS == 1 or AArch32 is supported at any Exception level)

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>VMID Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0</td>
<td>VMID</td>
</tr>
</tbody>
</table>

**VMID, bits [15:0]**

The VMID for the translation table.

If EL2 is using AArch32, or if the implementation has an 8-bit VMID, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

VMID encoding when FEAT_VMID16 is not implemented or (VTCR_EL2.VS == 0 or the implementation only supports execution in AArch64 state)

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>VMID Encoding</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

Page 1971
Bits [15:8]

Reserved, RES0.

VMID, bits [7:0]

The VMID for the translation table.

The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- The VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

BADDR, bits [47:1]

Translation table base address, A[47:x] or A[51:x], bits[47:1].

Note

- Translation table base addresses of 52 bits, A[51:x], are supported only in an implementation that includes FEAT_LPA and is using the 64KB translation granule.
- A translation table must be aligned to the size of the table, except that when using a translation table base address larger than 48 bits the minimum alignment of a table containing fewer than eight entries is 64 bytes.

In an implementation that includes FEAT_LPA, if the value of VTCR_EL2.PS is 0b110, then:

- Register bits[47:z] hold bits[47:z] of the stage 1 translation table base address, where z is determined as follows:
  - If x >= 6 then z=x.
  - Otherwise, z=6.
- When z>x register bits[(z-1):x] are RES0, and bits[(z-1):x] of the translation table base address are zero.
- When x>6 register bits[(x-1):6] are RES0.
- Register bit[1] is RES0.
- Bits[5:2] of the stage 1 translation table base address are zero.
- In an implementation that includes FEAT_TTCNP, bit[0] of the stage 1 translation table base address is zero.

Note

- In an implementation that includes FEAT_LPA a VTCR_EL2.PS value of 0b110, that selects a PA size of 52 bits, is permitted only when using the 64KB translation granule.
- When the value of ID_AA64MMFR0_EL1.PARange indicates that the implementation does not support a 52 bit PA size, if a translation table lookup uses this register with the 64KB translation granule when the Effective value of VTCR_EL2.PS is 0b110 and the value of register bits[5:2] is nonzero, an Address size fault is generated.

If the Effective value of VTCR_EL2.PS is not 0b110 then:

- Register bits[47:x] hold bits[47:x] of the stage 1 translation table base address.
- Register bits[(x-1):1] are RES0.
- If the implementation supports 52-bit PAs and IPAs then bits[51:48] of the translation table base addresses used in this stage of translation are 0b0000.

Note

This definition applies:

- To an implementation that includes FEAT_LPA and is using a translation granule smaller than 64KB.
- To any implementation that does not include FEAT_LPA.
If any VTTBR_EL2[47:0] bit that is defined as RES0 has the value 1 when a translation table walk is performed using VTTBR_EL2, then the translation table base address might be misaligned, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Bits[x-1:0] of the translation table base address are treated as if all the bits are zero. The value read back from the corresponding register bits is either the value written to the register or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

The AArch64 Virtual Memory System Architecture chapter describes how x is calculated based on the value of VTCR_EL2.T0SZ, the stage of translation, and the translation granule size.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CnP, bit [0]**

When FEAT_TTCNP is implemented:

Common not Private. This bit indicates whether each entry that is pointed to by VTTBR_EL2 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of VTTBR_EL2.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table entries pointed to by VTTBR_EL2 are permitted to differ from the entries for VTTBR_EL2 for other PEs in the Inner Shareable domain. This is not affected by the value of the current VMID.</td>
</tr>
<tr>
<td>0b1</td>
<td>The translation table entries pointed to by VTTBR_EL2 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of VTTBR_EL2.CnP is 1 and the VMID is the same as the current VMID.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

**Note**

If the value of VTTBR_EL2.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those VTTBR_EL2s do not point to the same translation table entries when using the current VMID then the results of translations using VTTBR_EL2 are CONSTRAINED UNPREDICTABLE, see ‘CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Accessing the VTTBR_EL2**

Accesses to this register use the following encodings:

MRS <Xt>, VTTBR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        return NVMem[0x020];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    return VTTBR_EL2;
elsif PSTATE.EL == EL3 then
    return VTTBR_EL2;

MSR VTTBR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b00</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && HCR_EL2.<NV2,NV> == '11' then
        NVMem[0x020] = X[t];
    elsif EL2Enabled() && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x18);
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    VTTBR_EL2 = X[t];
elsif PSTATE.EL == EL3 then
    VTTBR_EL2 = X[t];
ZCR_EL1, SVE Control Register for EL1

The ZCR_EL1 characteristics are:

**Purpose**

The SVE Control Register for EL1 is used to control aspects of SVE visible at Exception levels EL1 and EL0.

**Configuration**

This register is present only when FEAT_SVE is implemented. Otherwise, direct accesses to ZCR_EL1 are **UNDEFINED**.

When \texttt{HCR_EL2.\{E2H, TGE\} == \{1, 1\}} and EL2 is enabled in the current Security state, the fields in this register have no effect on execution at EL0.

**Attributes**

ZCR_EL1 is a 64-bit register.

**Field descriptions**

The ZCR_EL1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | RAZ/WI | LEN |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:9]**

Reserved, RES0.

**Bits [8:4]**

Reserved, RAZ/WI.

**LEN, bits [3:0]**

Effective Scalable Vector Length.

Constrains the scalable vector register length for EL1 and EL0 to \((\text{LEN}+1)\times 128\) bits.

For all purposes other than returning the result of a direct read of ZCR_EL1, this field behaves as if:

- It is set to the minimum of the stored value and the constrained length inherited from more privileged Exception levels in the current Security state.
- It is rounded down to the nearest implemented vector length.

An indirect read of ZCR_EL1.LEN appears to occur in program order relative to a direct write of the same register, without the need for explicit synchronization.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Accessing the ZCR_EL1

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL3 using the mnemonic ZCR_EL1 or ZCR_EL12 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, ZCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() &amp; HaveEL(EL3) &amp; EDSCR.SDD == '1' &amp; boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" &amp; CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif CPACR_EL1.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL1, 0x19);
  elsif EL2Enabled() &amp; HCR_EL2.E2H != '1' &amp; CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif EL2Enabled() &amp; HCR_EL2.E2H == '1' &amp; CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) &amp; CPTR_EL3.EZ == '0' then
    if Halted() &amp; EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end
  elsif EL2Enabled() &amp; HCR_EL2.<NV2,NV1,NV> == '111' then
    return NVMem[0x1E0];
  else
    return ZCR_EL1;
elsif PSTATE.EL == EL2 then
  if Halted() &amp; HaveEL(EL3) &amp; EDSCR.SDD == '1' &amp; boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" &amp; CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif HCR_EL2.E2H == '0' &amp; CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HCR_EL2.E2H == '1' &amp; CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) &amp; CPTR_EL3.EZ == '0' then
    if Halted() &amp; EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end
  elsif HCR_EL2.E2H == '1' then
    return ZCR_EL2;
  else
    return ZCR_EL1;
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.EZ == '0' then
    AArch64.SystemAccessTrap(EL3, 0x19);
  else
    return ZCR_EL1;

MSR ZCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif CPACR_EL1.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL1, 0x19);
  elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  else
    ZCR_EL1 = X[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  else
    ZCR_EL1 = X[t];
  end
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.EZ == '0' then
    AArch64.SystemAccessTrap(EL3, 0x19);
  else
    ZCR_EL1 = X[t];
end

MRS <Xt>, ZCR_EL12

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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</thead>
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<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b00010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    return NVMem[0x1E0];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && CPTR_EL3.EZ == '0' then
      UNDEFINED;
    elsif CPTR_EL2.ZEN == 'x0' then
      AArch64.SystemAccessTrap(EL2, 0x19);
    else
      AArch64.SystemAccessTrap(EL2, 0x19);
    end if
  else
    return ZCR_EL1;
  end if
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    if CPTR_EL3.EZ == '0' then
      AArch64.SystemAccessTrap(EL3, 0x19);
    else
      return ZCR_EL1;
    end if
  else
    UNDEFINED;
  end if

MSR ZCR_EL1, SVE Control Register for EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b101</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '101' then
    NVMem[0x1E0] = X[t];
  elsif EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if HCR_EL2.E2H == '1' then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
      UNDEFINED;
    elsif CPTR_EL2.ZEN == 'x0' then
      AArch64.SystemAccessTrap(EL2, 0x19);
    elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        ZCR_EL1 = X[t];
      end
    else
      ZCR_EL1 = X[t];
    end
  else
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
    if CPTR_EL3.EZ == '0' then
      AArch64.SystemAccessTrap(EL3, 0x19);
    else
      ZCR_EL1 = X[t];
    end
  else
    UNDEFINED;
ZCR_EL2, SVE Control Register for EL2

The ZCR_EL2 characteristics are:

**Purpose**

The SVE Control Register for EL2 is used to control aspects of SVE visible at Exception levels EL2, EL1, and EL0, when EL2 is enabled in the current Security state.

**Configuration**

This register is present only when FEAT_SVE is implemented. Otherwise, direct accesses to ZCR_EL2 are UNDEFINED.

This register has no effect if EL2 is not enabled in the current Security state.

**Attributes**

ZCR_EL2 is a 64-bit register.

**Field descriptions**

The ZCR_EL2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RAZ/WI</td>
</tr>
<tr>
<td>3:0</td>
<td>Effective Scalable Vector Length</td>
</tr>
</tbody>
</table>

**Bits [63:9]**

Reserved, RES0.

**Bits [8:4]**

Reserved, RAZ/WI.

**LEN, bits [3:0]**

Effective Scalable Vector Length.

Constrains the scalable vector register length for EL2, EL1, and EL0 to (LEN+1)x128 bits, when EL2 is enabled in the current Security state.

For all purposes other than returning the result of a direct read of ZCR_EL2, this field behaves as if:

- It is set to the minimum of the stored value and the constrained length inherited from more privileged Exception levels in the current Security state.
- It is rounded down to the nearest implemented vector length.

An indirect read of ZCR_EL2.LEN appears to occur in program order relative to a direct write of the same register, without the need for explicit synchronization.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the ZCR_EL2

When HCR_EL2.E2H is 1, without explicit synchronization, access from EL2 using the mnemonic ZCR_EL2 or ZCR_EL1 are not guaranteed to be ordered with respect to accesses using the other mnemonic.

Accesses to this register use the following encodings:

MRS <Xt>, ZCR_EL2

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elseif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elseif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elseif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end
  else
    AArch64.SystemAccessTrap(EL3, 0x19);
  end
  return ZCR_EL2;
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.EZ == '0' then
    AArch64.SystemAccessTrap(EL3, 0x19);
  else
    return ZCR_EL2;
end

MSR ZCR_EL2, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HCR_EL2.NV == '1' then
    AArch64.SystemAccessTrap(EL2, 0x18);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end if;
  else
    ZCR_EL2 = X[t];
  end if;
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.EZ == '0' then
    AArch64.SystemAccessTrap(EL3, 0x19);
  else
    ZCR_EL2 = X[t];
  end if;
MRS <Xt>, ZCR_EL1

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && CPTR_EL3.EZ == '0' then
        UNDEFINED;
    elsif CPACR_EL1.ZEN == 'x0' then
        AArch64.SystemAccessTrap(EL1, 0x19);
    elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TZ == '1' then
        AArch64.SystemAccessTrap(EL2, 0x19);
    elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x19);
    elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x19);
        end
    elsif EL2Enabled() && HCR_EL2.<NV2,NV1,NV> == '111' then
        return NVMem[0x1E0];
    else
        return ZCR_EL1;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && CPTR_EL3.EZ == '0' then
        UNDEFINED;
    elsif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
        AArch64.SystemAccessTrap(EL2, 0x19);
    elsif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
        AArch64.SystemAccessTrap(EL2, 0x19);
    elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.SystemAccessTrap(EL3, 0x19);
        end
    elsif HCR_EL2.E2H == '1' then
        return ZCR_EL2;
    else
        return ZCR_EL1;
    end
elsif PSTATE.EL == EL3 then
    if CPTR_EL3.EZ == '0' then
        AArch64.SystemAccessTrap(EL3, 0x19);
    else
        return ZCR_EL1;
    end
else
    return ZCR_EL1;
end

MSR ZCR_EL1, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif CPACR_EL1.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL1, 0x19);
  elsif EL2Enabled() && HCR_EL2.E2H != '1' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif EL2Enabled() && HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end if
  elsif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end if
  elsif HCR_EL2.E2H == '1' then
    ZCR_EL2 = X[t];
  else
    ZCR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && CPTR_EL3.EZ == '0' then
    UNDEFINED;
  elsif HCR_EL2.E2H == '0' && CPTR_EL2.TZ == '1' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HCR_EL2.E2H == '1' && CPTR_EL2.ZEN == 'x0' then
    AArch64.SystemAccessTrap(EL2, 0x19);
  elsif HaveEL(EL3) && CPTR_EL3.EZ == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.SystemAccessTrap(EL3, 0x19);
    end if
  elsif HCR_EL2.E2H == '1' then
    ZCR_EL2 = X[t];
  else
    ZCR_EL1 = X[t];
  end if
elsif PSTATE.EL == EL3 then
  if CPTR_EL3.EZ == '0' then
    AArch64.SystemAccessTrap(EL3, 0x19);
  else
    ZCR_EL1 = X[t];
  end if
The ZCR_EL3 characteristics are:

**Purpose**

The SVE Control Register for EL3 is used to control aspects of SVE visible at all Exception levels.

**Configuration**

This register is present only when FEAT_SVE is implemented. Otherwise, direct accesses to ZCR_EL3 are UNDEFINED.

**Attributes**

ZCR_EL3 is a 64-bit register.

**Field descriptions**

The ZCR_EL3 bit assignments are:

| Bits [63:9] | Reserved, RES0. |
| Bits [8:4]  | Reserved, RAZ/WI. |
| LEN, bits [3:0] | Effective Scalable Vector Length. |

Constrains the scalable vector register length for all Exception levels to (LEN+1)x128 bits.

For all purposes other than returning the result of a direct read of ZCR_EL3, this field behaves as if:

- It is rounded down to the nearest implemented vector length.

An indirect read of ZCR_EL3.LEN appears to occur in program order relative to a direct write of the same register, without the need for explicit synchronization.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ZCR_EL3**

Accesses to this register use the following encodings:

MRS <Xt>, ZCR_EL3

| op0 | op1 | CRn | CRm | op2 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    if CPTR_EL3.EZ == '0' then
        AArch64.SystemAccessTrap(EL3, 0x19);
    else
        return ZCR_EL3;
    end
end

MSR ZCR_EL3, <Xt>

<table>
<thead>
<tr>
<th>op0</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
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</thead>
<tbody>
<tr>
<td>0b11</td>
<td>0b110</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b000</td>
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</tbody>
</table>
AArch32 System Registers

ACTLR: Auxiliary Control Register
ACTLR2: Auxiliary Control Register 2
ADFSR: Auxiliary Data Fault Status Register
AIDR: Auxiliary ID Register
AIFSR: Auxiliary Instruction Fault Status Register
AMAIR0: Auxiliary Memory Attribute Indirection Register 0
AMAIR1: Auxiliary Memory Attribute Indirection Register 1
AMCFGR: Activity Monitors Configuration Register
AMCGCR: Activity Monitors Counter Group Configuration Register
AMCNTENCLR0: Activity Monitors Count Enable Clear Register 0
AMCNTENCLR1: Activity Monitors Count Enable Clear Register 1
AMCNTENSET0: Activity Monitors Count Enable Set Register 0
AMCNTENSET1: Activity Monitors Count Enable Set Register 1
AMCR: Activity Monitors Control Register
AMEVCNTR0<n>: Activity Monitors Event Counter Registers 0
AMEVCNTR1<n>: Activity Monitors Event Counter Registers 1
AMEVTYPER0<n>: Activity Monitors Event Type Registers 0
AMEVTYPER1<n>: Activity Monitors Event Type Registers 1
AMUSERENR: Activity Monitors User Enable Register
APSR: Application Program Status Register
CCSIDR: Current Cache Size ID Register
CCSIDR2: Current Cache Size ID Register 2
CLIDR: Cache Level ID Register
CNTFRQ: Counter-timer Frequency register
CNTHCTL: Counter-timer Hyp Control register
CNTHPS_CTL: Counter-timer Secure Physical Timer Control Register (EL2)
CNTHPS_CVAL: Counter-timer Secure Physical Timer CompareValue Register (EL2)
CNTHPS_TVAL: Counter-timer Secure Physical Timer TimerValue Register (EL2)
CNTHP_CTL: Counter-timer Hyp Physical Timer Control register
CNTHP_CVAL: Counter-timer Hyp Physical CompareValue register
CNTHP_TVAL: Counter-timer Hyp Physical Timer TimerValue register
CNTHVS_CTL: Counter-timer Secure Virtual Timer Control Register (EL2)
CNTHVS_CVAL: Counter-timer Secure Virtual Timer CompareValue Register (EL2)
CNTHVS_TVAL: Counter-timer Secure Virtual Timer TimerValue Register (EL2)
<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTHV_CTL</td>
<td>Counter-timer Virtual Timer Control register (EL2)</td>
</tr>
<tr>
<td>CNTHV_CVAL</td>
<td>Counter-timer Virtual Timer CompareValue register (EL2)</td>
</tr>
<tr>
<td>CNTHV_TVAL</td>
<td>Counter-timer Virtual Timer TimerValue register (EL2)</td>
</tr>
<tr>
<td>CNTKCTL</td>
<td>Counter-timer Kernel Control register</td>
</tr>
<tr>
<td>CNTPCT</td>
<td>Counter-timer Physical Count register</td>
</tr>
<tr>
<td>CNTPCTSS</td>
<td>Counter-timer Self-Synchronized Physical Count register</td>
</tr>
<tr>
<td>CNTP_CTL</td>
<td>Counter-timer Physical Timer Control register</td>
</tr>
<tr>
<td>CNTP_CVAL</td>
<td>Counter-timer Physical Timer CompareValue register</td>
</tr>
<tr>
<td>CNTP_TVAL</td>
<td>Counter-timer Physical Timer TimerValue register</td>
</tr>
<tr>
<td>CNTVCT</td>
<td>Counter-timer Virtual Count register</td>
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<tr>
<td>CNTVCTSS</td>
<td>Counter-timer Self-Synchronized Virtual Count register</td>
</tr>
<tr>
<td>CNTVOFF</td>
<td>Counter-timer Virtual Offset register</td>
</tr>
<tr>
<td>CNTV_CTL</td>
<td>Counter-timer Virtual Timer Control register</td>
</tr>
<tr>
<td>CONTEXTIDR</td>
<td>Context ID Register</td>
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<tr>
<td>CPACR</td>
<td>Architectural Feature Access Control Register</td>
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<tr>
<td>CPSR</td>
<td>Current Program Status Register</td>
</tr>
<tr>
<td>CSSELR</td>
<td>Cache Size Selection Register</td>
</tr>
<tr>
<td>CTR</td>
<td>Cache Type Register</td>
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<tr>
<td>DACR</td>
<td>Domain Access Control Register</td>
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<tr>
<td>DBGAUTHSTATUS</td>
<td>Debug Authentication Status register</td>
</tr>
<tr>
<td>DBGBCR&lt;n&gt;</td>
<td>Debug Breakpoint Control Registers</td>
</tr>
<tr>
<td>DBGBV&lt;R&lt;n&gt;</td>
<td>Debug Breakpoint Value Registers</td>
</tr>
<tr>
<td>DBGBXVR&lt;n&gt;</td>
<td>Debug Breakpoint Extended Value Registers</td>
</tr>
<tr>
<td>DBGCLAIMCLR</td>
<td>Debug CLAIM Tag Clear register</td>
</tr>
<tr>
<td>DBGCLAIMSET</td>
<td>Debug CLAIM Tag Set register</td>
</tr>
<tr>
<td>DBGDCCINT</td>
<td>DCC Interrupt Enable Register</td>
</tr>
<tr>
<td>DBGDEVID</td>
<td>Debug Device ID register 0</td>
</tr>
<tr>
<td>DBGDEVID1</td>
<td>Debug Device ID register 1</td>
</tr>
<tr>
<td>DBGDEVID2</td>
<td>Debug Device ID register 2</td>
</tr>
<tr>
<td>DBGIDR</td>
<td>Debug ID Register</td>
</tr>
<tr>
<td>DBGDRAR</td>
<td>Debug ROM Address Register</td>
</tr>
<tr>
<td>DBGDSAR</td>
<td>Debug Self Address Register</td>
</tr>
<tr>
<td>DBGDSCRext</td>
<td>Debug Status and Control Register, External View</td>
</tr>
<tr>
<td>DBGDSCRint</td>
<td>Debug Status and Control Register, Internal View</td>
</tr>
</tbody>
</table>
**DBGDTRRx** ext: Debug OS Lock Data Transfer Register, Receive, External View

**DBGDTRRx** int: Debug Data Transfer Register, Receive

**DBGDTRTx** ext: Debug OS Lock Data Transfer Register, Transmit

**DBGDTRTx** int: Debug Data Transfer Register, Transmit

**DBGOSDLR**: Debug OS Double Lock Register

**DBGOSECCR**: Debug OS Lock Exception Catch Control Register

**DBGOSLAR**: Debug OS Lock Access Register

**DBGOSLSR**: Debug OS Lock Status Register

**DBGPRCR**: Debug Power Control Register

**DBGVCR**: Debug Vector Catch Register

**DBGWCR<n>**: Debug Watchpoint Control Registers

**DBGWFAR**: Debug Watchpoint Fault Address Register

**DBGWVR<n>**: Debug Watchpoint Value Registers

**DFAR**: Data Fault Address Register

**DFSR**: Data Fault Status Register

**DISR**: Deferred Interrupt Status Register

**DLR**: Debug Link Register

**DSPSR**: Debug Saved Program Status Register

**ELR_hyp**: Exception Link Register (Hyp mode)

**ERRIDR**: Error Record ID Register

**ERRSELR**: Error Record Select Register

**ERXADDR**: Selected Error Record Address Register

**ERXADDR2**: Selected Error Record Address Register 2

**ERXCTRLR**: Selected Error Record Control Register

**ERXCTRLR2**: Selected Error Record Control Register 2

**ERXFR**: Selected Error Record Feature Register

**ERXFR2**: Selected Error Record Feature Register 2

**ERXMISC0**: Selected Error Record Miscellaneous Register 0

**ERXMISC1**: Selected Error Record Miscellaneous Register 1

**ERXMISC2**: Selected Error Record Miscellaneous Register 2

**ERXMISC3**: Selected Error Record Miscellaneous Register 3

**ERXMISC4**: Selected Error Record Miscellaneous Register 4

**ERXMISC5**: Selected Error Record Miscellaneous Register 5

**ERXMISC6**: Selected Error Record Miscellaneous Register 6

**ERXMISC7**: Selected Error Record Miscellaneous Register 7

**ERXSTATUS**: Selected Error Record Primary Status Register
FCSEIDR: FCSE Process ID register
FPEXC: Floating-Point Exception Control register
FPSCR: Floating-Point Status and Control Register
FPSID: Floating-Point System ID register
HACR: Hyp Auxiliary Configuration Register
HACTLR: Hyp Auxiliary Control Register
HACTLR2: Hyp Auxiliary Control Register 2
HADFSR: Hyp Auxiliary Data Fault Status Register
HAIFSR: Hyp Auxiliary Instruction Fault Status Register
HAMAIR0: Hyp Auxiliary Memory Attribute Indirection Register 0
HAMAIR1: Hyp Auxiliary Memory Attribute Indirection Register 1
HCPTR: Hyp Architectural Feature Trap Register
HCR: Hyp Configuration Register
HCR2: Hyp Configuration Register 2
HDCR: Hyp Debug Control Register
HDFAR: Hyp Data Fault Address Register
HIFAR: Hyp Instruction Fault Address Register
HMAIR0: Hyp Memory Attribute Indirection Register 0
HMAIR1: Hyp Memory Attribute Indirection Register 1
HPFAR: Hyp IPA Fault Address Register
HRMR: Hyp Reset Management Register
HSCTLR: Hyp System Control Register
HSR: Hyp Syndrome Register
HSTR: Hyp System Trap Register
HTCR: Hyp Translation Control Register
HTPIDR: Hyp Software Thread ID Register
HTRFCR: Hyp Trace Filter Control Register
HTTBR: Hyp Translation Table Base Register
HVBAR: Hyp Vector Base Address Register
ICC_AP0R<n>: Interrupt Controller Active Priorities Group 0 Registers
ICC_AP1R<n>: Interrupt Controller Active Priorities Group 1 Registers
ICC_ASGI1R: Interrupt Controller Alias Software Generated Interrupt Group 1 Register
ICC_BPR0: Interrupt Controller Binary Point Register 0
ICC_BPR1: Interrupt Controller Binary Point Register 1
ICC_CTLR: Interrupt Controller Control Register
ICC_DIR: Interrupt Controller Deactivate Interrupt Register
ICC_EOIR0: Interrupt Controller End Of Interrupt Register 0
ICC_EOIR1: Interrupt Controller End Of Interrupt Register 1
ICC_HPPIR0: Interrupt Controller Highest Priority Pending Interrupt Register 0
ICC_HPPIR1: Interrupt Controller Highest Priority Pending Interrupt Register 1
ICC_HSRE: Interrupt Controller Hyp System Register Enable register
ICC_IAR0: Interrupt Controller Interrupt Acknowledge Register 0
ICC_IAR1: Interrupt Controller Interrupt Acknowledge Register 1
ICC_IGRPEN0: Interrupt Controller Interrupt Group 0 Enable register
ICC_IGRPEN1: Interrupt Controller Interrupt Group 1 Enable register
ICC_MCTLR: Interrupt Controller Monitor Control Register
ICC_MGRPEN1: Interrupt Controller Monitor Interrupt Group 1 Enable register
ICC_MSRE: Interrupt Controller Monitor System Register Enable register
ICC_PMR: Interrupt Controller Interrupt Priority Mask Register
ICC_RPR: Interrupt Controller Running Priority Register
ICC_SGI0R: Interrupt Controller Software Generated Interrupt Group 0 Register
ICC_SGI1R: Interrupt Controller Software Generated Interrupt Group 1 Register
ICC_SRE: Interrupt Controller System Register Enable register
ICH_AP0R<n>: Interrupt Controller Hyp Active Priorities Group 0 Registers
ICH_AP1R<n>: Interrupt Controller Hyp Active Priorities Group 1 Registers
ICH_EISR: Interrupt Controller End of Interrupt Status Register
ICH_ELBSR: Interrupt Controller Empty List Register Status Register
ICH_HCR: Interrupt Controller Hyp Control Register
ICH_LR<n>: Interrupt Controller List Registers
ICH_LRC<n>: Interrupt Controller List Registers
ICH_MISR: Interrupt Controller Maintenance Interrupt State Register
ICH_VMCR: Interrupt Controller Virtual Machine Control Register
ICH_VTR: Interrupt Controller VGIC Type Register
ICV_AP0R<n>: Interrupt Controller Virtual Active Priorities Group 0 Registers
ICV_AP1R<n>: Interrupt Controller Virtual Active Priorities Group 1 Registers
ICV_BPR0: Interrupt Controller Virtual Binary Point Register 0
ICV_BPR1: Interrupt Controller Virtual Binary Point Register 1
ICV_CTLR: Interrupt Controller Virtual Control Register
ICV_DIR: Interrupt Controller Deactivate Virtual Interrupt Register
ICV_EOIR0: Interrupt Controller Virtual End Of Interrupt Register 0
ICV_EOIR1: Interrupt Controller Virtual End Of Interrupt Register 1
ICV_HPPIR0: Interrupt Controller Virtual Highest Priority Pending Interrupt Register 0
ICV_HPPR1: Interrupt Controller Virtual Highest Priority Pending Interrupt Register 1
ICV_IAR0: Interrupt Controller Virtual Interrupt Acknowledge Register 0
ICV_IAR1: Interrupt Controller Virtual Interrupt Acknowledge Register 1
ICV_IGRPEN0: Interrupt Controller Virtual Interrupt Group 0 Enable register
ICV_IGRPEN1: Interrupt Controller Virtual Interrupt Group 1 Enable register
ICV_PMR: Interrupt Controller Virtual Interrupt Priority Mask Register
ICV_RPR: Interrupt Controller Virtual Running Priority Register
ID_AFR0: Auxiliary Feature Register 0
ID_DFR0: Debug Feature Register 0
ID_DFR1: Debug Feature Register 1
ID_ISAR0: Instruction Set Attribute Register 0
ID_ISAR1: Instruction Set Attribute Register 1
ID_ISAR2: Instruction Set Attribute Register 2
ID_ISAR3: Instruction Set Attribute Register 3
ID_ISAR4: Instruction Set Attribute Register 4
ID_ISAR5: Instruction Set Attribute Register 5
ID_ISAR6: Instruction Set Attribute Register 6
ID_MMFR0: Memory Model Feature Register 0
ID_MMFR1: Memory Model Feature Register 1
ID_MMFR2: Memory Model Feature Register 2
ID_MMFR3: Memory Model Feature Register 3
ID_MMFR4: Memory Model Feature Register 4
ID_MMFR5: Memory Model Feature Register 5
ID_PFR0: Processor Feature Register 0
ID_PFR1: Processor Feature Register 1
ID_PFR2: Processor Feature Register 2
IFAR: Instruction Fault Address Register
IFSR: Instruction Fault Status Register
ISR: Interrupt Status Register
JIDR: Jazelle ID Register
JMCR: Jazelle Main Configuration Register
JOSCR: Jazelle OS Control Register
MAIR0: Memory Attribute Indirection Register 0
MAIR1: Memory Attribute Indirection Register 1
MIDR: Main ID Register
MPIDR: Multiprocessor Affinity Register
MVBAR: Monitor Vector Base Address Register
MVFR0: Media and VFP Feature Register 0
MVFR1: Media and VFP Feature Register 1
MVFR2: Media and VFP Feature Register 2
NMRR: Normal Memory Remap Register
NSACR: Non-Secure Access Control Register
PAR: Physical Address Register
PMCCFILTR: Performance Monitors Cycle Count Filter Register
PMCCNTR: Performance Monitors Cycle Count Register
PMCEID0: Performance Monitors Common Event Identification register 0
PMCEID1: Performance Monitors Common Event Identification register 1
PMCEID2: Performance Monitors Common Event Identification register 2
PMCEID3: Performance Monitors Common Event Identification register 3
PMCNECLR: Performance Monitors Count Enable Clear register
PMCNESET: Performance Monitors Count Enable Set register
PMCR: Performance Monitors Control Register
PMEVCNTR<n>: Performance Monitors Event Count Registers
PMEVTYPER<n>: Performance Monitors Event Type Registers
PMINTECLR: Performance Monitors Interrupt Enable Clear register
PMINTENSET: Performance Monitors Interrupt Enable Set register
PMMIR: Performance Monitors Machine Identification Register
PMOVSR: Performance Monitors Overflow Flag Status Register
PMOVSSET: Performance Monitors Overflow Flag Status Set register
PMSELR: Performance Monitors Event Counter Selection Register
PMSWINC: Performance Monitors Software Increment register
PMUSERENR: Performance Monitors User Enable Register
PMXEVCTR: Performance Monitors Selected Event Count Register
PMXETYPER: Performance Monitors Selected Event Type Register
PRRR: Primary Region Remap Register
REVIDR: Revision ID Register
RMR: Reset Management Register
RVBAR: Reset Vector Base Address Register
SCR: Secure Configuration Register
SCTLR: System Control Register
SDCR: Secure Debug Control Register
SDER: Secure Debug Enable Register
SPSR: Saved Program Status Register

SPSR_abt: Saved Program Status Register (Abort mode)

SPSR_fiq: Saved Program Status Register (FIQ mode)

SPSR_hyp: Saved Program Status Register (Hyp mode)

SPSR_irq: Saved Program Status Register (IRQ mode)

SPSR_mon: Saved Program Status Register (Monitor mode)

SPSR_svc: Saved Program Status Register (Supervisor mode)

SPSR_und: Saved Program Status Register (Undefined mode)

TCMTR: TCM Type Register

TLBTR: TLB Type Register

TPIIDRPRW: PL1 Software Thread ID Register

TPIIDRORO: PL0 Read-Only Software Thread ID Register

TPIIDRURW: PL0 Read/Write Software Thread ID Register

TRFCR: Trace Filter Control Register

TTBCR: Translation Table Base Control Register

TTBCR2: Translation Table Base Control Register 2

TTBR0: Translation Table Base Register 0

TTBR1: Translation Table Base Register 1

VBAR: Vector Base Address Register

VDFSR: Virtual SError Exception Syndrome Register

VDISR: Virtual Deferred Interrupt Status Register

VMPIDR: Virtualization Multiprocessor ID Register

VPIDR: Virtualization Processor ID Register

VTCR: Virtualization Translation Control Register

VTTBR: Virtualization Translation Table Base Register
AArch32 System Instructions

**ATS12NSOPR**: Address Translate Stages 1 and 2 Non-secure Only PL1 Read

**ATS12NSOPW**: Address Translate Stages 1 and 2 Non-secure Only PL1 Write

**ATS12NSOUR**: Address Translate Stages 1 and 2 Non-secure Only Unprivileged Read

**ATS12NSOUW**: Address Translate Stages 1 and 2 Non-secure Only Unprivileged Write

**ATS1CPR**: Address Translate Stage 1 Current state PL1 Read

**ATS1CPRP**: Address Translate Stage 1 Current state PL1 Read PAN

**ATS1CPW**: Address Translate Stage 1 Current state PL1 Write

**ATS1CPWP**: Address Translate Stage 1 Current state PL1 Write PAN

**ATS1CUR**: Address Translate Stage 1 Current state Unprivileged Read

**ATS1CUW**: Address Translate Stage 1 Current state Unprivileged Write

**ATS1HR**: Address Translate Stage 1 Hyp mode Read

**ATS1HW**: Address Translate Stage 1 Hyp mode Write

**BPIALL**: Branch Predictor Invalidate All

**BPIALLIS**: Branch Predictor Invalidate All, Inner Shareable

**BPIMVA**: Branch Predictor Invalidate by VA

**CFPRCTX**: Control Flow Prediction Restriction by Context

**CP15DMB**: Data Memory Barrier System instruction

**CP15DSB**: Data Synchronization Barrier System instruction

**CP15ISB**: Instruction Synchronization Barrier System instruction

**CPPRCTX**: Cache Prefetch Prediction Restriction by Context

**DCCIMVAC**: Data Cache line Clean and Invalidate by VA to PoC

**DCCISW**: Data Cache line Clean and Invalidate by Set/Way

**DCCMVAC**: Data Cache line Clean by VA to PoC

**DCCMVAU**: Data Cache line Clean by VA to PoU

**DCCSW**: Data Cache line Clean by Set/Way

**DCIMVAC**: Data Cache line Invalidate by VA to PoC

**DCISW**: Data Cache line Invalidate by Set/Way

**DTLBIALL**: Data TLB Invalidate All

**DTLBIASID**: Data TLB Invalidate by ASID match

**DTLBMVA**: Data TLB Invalidate by VA

**DVPRCTX**: Data Value Prediction Restriction by Context

**ICIALLU**: Instruction Cache Invalidate All to PoU

**ICIALLUIS**: Instruction Cache Invalidate All to PoU, Inner Shareable

**ICIMVAU**: Instruction Cache line Invalidate by VA to PoU
TLBIALL: Instruction TLB Invalidate All
TLBIASID: Instruction TLB Invalidate by ASID match
TLBIMVA: Instruction TLB Invalidate by VA
TLBIAL: TLB Invalidate All
TLBIALLH: TLB Invalidate All, Hyp mode
TLBIALLHIS: TLB Invalidate All, Hyp mode, Inner Shareable
TLBIALLIS: TLB Invalidate All, Inner Shareable
TLBIALLNSNH: TLB Invalidate All, Non-Secure Non-Hyp
TLBIALLNSNHIS: TLB Invalidate All, Non-Secure Non-Hyp, Inner Shareable
TLBiasid: TLB Invalidate by ASID match
TLBiasidis: TLB Invalidate by ASID match, Inner Shareable
TLBIIIPAS2: TLB Invalidate by Intermediate Physical Address, Stage 2
TLBIIIPAS2IS: TLB Invalidate by Intermediate Physical Address, Stage 2, Inner Shareable
TLBIIIPAS2L: TLB Invalidate by Intermediate Physical Address, Stage 2, Last level
TLBIIIPAS2LIS: TLB Invalidate by Intermediate Physical Address, Stage 2, Last level, Inner Shareable
TLBIMVA: TLB Invalidate by VA
TLBIMVAA: TLB Invalidate by VA, All ASID
TLBIMVAAIS: TLB Invalidate by VA, All ASID, Inner Shareable
TLBIMVAAL: TLB Invalidate by VA, All ASID, Last level
TLBIMVAALIS: TLB Invalidate by VA, All ASID, Last level, Inner Shareable
TLBIMVAH: TLB Invalidate by VA, Hyp mode
TLBIMVAHIS: TLB Invalidate by VA, Hyp mode, Inner Shareable
TLBIMVAIS: TLB Invalidate by VA, Inner Shareable
TLBIMVAL: TLB Invalidate by VA, Last level
TLBIMVALH: TLB Invalidate by VA, Last level, Hyp mode
TLBIMVALHIS: TLB Invalidate by VA, Last level, Hyp mode, Inner Shareable
TLBIMVALIS: TLB Invalidate by VA, Last level, Inner Shareable
ACTLR, Auxiliary Control Register

The ACTLR characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED configuration and control options for execution at EL1 and EL0.

**Configuration**

AArch32 System register ACTLR bits [31:0] are architecturally mapped to AArch64 System register \texttt{ACTLR_EL1[31:0]}.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ACTLR are UNDEFINED.

Some bits might define global configuration settings, and be common to the Secure and Non-secure instances of the register.

**Attributes**

ACTLR is a 32-bit register.

**Field descriptions**

The ACTLR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ACTLR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}, \{#\}<opc1>, <Rt>, <CRn>, <CRm>, \{#\}<opc2>\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 1997
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TACR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TAC == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    ACTLR_NS = R[t];
  else
    ACTLR = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    ACTLR_NS = R[t];
  else
    ACTLR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    ACTLR_S = R[t];
  else
    ACTLR_NS = R[t];
  
MCR{<coproc>}{<opc1>, {#}<opc2>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TACR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TAC == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    ACTLR_NS = R[t];
  else
    ACTLR = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    ACTLR_NS = R[t];
  else
    ACTLR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    ACTLR_S = R[t];
  else
    ACTLR_NS = R[t];
ACTLR2, Auxiliary Control Register 2

The ACTLR2 characteristics are:

**Purpose**

Provides additional space to the ACTLR register to hold IMPLEMENTATION DEFINED trap functionality for execution at EL1 and EL0.

**Configuration**

AArch32 System register ACTLR2 bits [31:0] are architecturally mapped to AArch64 System register ACTLR_EL1[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ACTLR2 are UNDEFINED.

In Armv8.0 and Armv8.1, it is IMPLEMENTATION DEFINED whether this register is implemented, or whether it causes UNDEFINED exceptions when accessed. The implementation of this register can be detected by examining ID_MMFR4.AC2.

From Armv8.2 this register must be implemented.

**Attributes**

ACTLR2 is a 32-bit register.

**Field descriptions**

The ACTLR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ACTLR2**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#<opc1>, <Rt>, <CRn>, <CRm>{, {#<opc2>}}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TACR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TAC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return ACTLR2_NS;
    else
        return ACTLR2;
    endif
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return ACTLR2_NS;
    else
        return ACTLR2;
    endif
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        ACTLR2_S = R[t];
    else
        ACTLR2_NS = R[t];
    endif
endif

MCR{<c>}{<qp>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
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<td>0b0001</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TACR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TAC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        ACTLR2_NS = R[t];
    else
        ACTLR2 = R[t];
    endif
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        ACTLR2_NS = R[t];
    else
        ACTLR2 = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        ACTLR2_S = R[t];
    else
        ACTLR2_NS = R[t];
    endif
ADFSR, Auxiliary Data Fault Status Register

The ADFSR characteristics are:

### Purpose

Provides additional IMPLEMENTATION DEFINED fault status information for Data Abort exceptions taken to EL1 modes, and EL3 modes when EL3 is implemented and is using AArch32.

### Configuration

AArch32 System register ADFSR bits [31:0] are architecturally mapped to AArch64 System register AFSR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ADFSR are UNDEFINED.

### Attributes

ADFSR is a 32-bit register.

### Field descriptions

The ADFSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the ADFSR

Accesses to this register use the following encodings:

MRC{<c>{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return ADFSR_NS;
    else
        return ADFSR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return ADFSR_NS;
    else
        return ADFSR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return ADFSR_S;
    else
        return ADFSR_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        ADFSR_NS = R[t];
    else
        ADFSR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        ADFSR_NS = R[t];
    else
        ADFSR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        ADFSR_S = R[t];
    else
        ADFSR_NS = R[t];
AIDR, Auxiliary ID Register

The AIDR characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED identification information.

The value of this register must be used in conjunction with the value of MIDR.

**Configuration**

AArch32 System register AIDR bits [31:0] are architecturally mapped to AArch64 System register AIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to AIDR are UNDEFINED.

**Attributes**

AIDR is a 32-bit register.

**Field descriptions**

The AIDR bit assignments are:

```
  31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
```

<table>
<thead>
<tr>
<th></th>
<th>IMPLEMENTATION DEFINED</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>IMPLEMENTATION DEFINED, bits [31:0]</strong></td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
</tbody>
</table>

**Accessing the AIDR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
        AArch32.TID1 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return AIDR;
    end
elsif PSTATE.EL == EL2 then
    return AIDR;
elsif PSTATE.EL == EL3 then
    return AIDR;
AIFSR, Auxiliary Instruction Fault Status Register

The AIFSR characteristics are:

Purpose

Provides additional IMPLEMENTATION DEFINED fault status information for Prefetch Abort exceptions taken to EL1 modes, and EL3 modes when EL3 is implemented and is using AArch32.

Configuration

AArch32 System register AIFSR bits [31:0] are architecturally mapped to AArch64 System register $AFSR_{EL1}[31:0]$.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to AIFSR are UNDEFINED.

Attributes

AIFSR is a 32-bit register.

Field descriptions

The AIFSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the AIFSR

Accesses to this register use the following encodings:

$\text{MRC}\{<c>\}\{<q>\} <\text{coproc}, \{#<\text{opc1}\}, <\text{Rt}, <\text{CRn}, <\text{CRm}\}{, \{#<\text{opc2}\}}>$

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemSystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AIFSR_NS;
    else
        return AIFSR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AIFSR_NS;
    else
        return AIFSR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        AIFSR_S = R[t];
    else
        AIFSR_NS = R[t];
else
    AIFSR = R[t];
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
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<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemSystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AIFSR_NS;
    else
        return AIFSR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AIFSR_NS;
    else
        return AIFSR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        AIFSR_S = R[t];
    else
        AIFSR_NS = R[t];
else
    AIFSR = R[t];
endif
AMAIR0, Auxiliary Memory Attribute Indirection Register 0

The AMAIR0 characteristics are:

**Purpose**

When using the Long-descriptor format translation tables for stage 1 translations, provides IMPLEMENTATION DEFINED memory attributes for the memory regions specified by MAIR0.

**Configuration**

AArch32 System register AMAIR0 bits [31:0] are architecturally mapped to AArch64 System register AMAIR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to AMAIR0 are UNDEFINED.

**Attributes**

AMAIR0 is a 32-bit register.

**Field descriptions**

The AMAIR0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
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<th>22</th>
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</tr>
</tbody>
</table>

This register is RES0 in the following cases:

- When an implementation does not provide any IMPLEMENTATION DEFINED memory attributes.
- When the Long-descriptor translation table format is not used.

If EL3 is implemented and is using AArch32:

- AMAIR0(S) gives the value for memory accesses from Secure state.
- AMAIR0(NS) gives the value for memory accesses from Non-secure states other than Hyp mode.

Any IMPLEMENTATION DEFINED memory attributes are additional qualifiers for the memory locations and must not change the architectured behavior specified by MAIR0 and MAIR1.

In a typical implementation, AMAIR0 and AMAIR1 split into eight one-byte fields, corresponding to the MAIRn.Attr<n> fields, but the architecture does not require them to do so.

**IMPLEMENTATION DEFINED, bits [31:0]**

**IMPLEMENTATION DEFINED.**

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AMAIR0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AMAIR0_NS;
    else
        return AMAIR0;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AMAIR0_NS;
    else
        return AMAIR0;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return AMAIR0_S;
    else
        return AMAIR0_NS;

if PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return AMAIR0_NS;
    else
        return AMAIR0;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return AMAIR0_S;
    else
        return AMAIR0_NS;
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
        AMAIR0_NS = R[t];
    else
        AMAIR0 = R[t];
elseif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        AMAIR0_NS = R[t];
    else
        AMAIR0 = R[t];
elseif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15DISABLE == HIGH then
        UNDEFINED;
    elseif SCR.NS == '0' && CP15DISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            AMAIR0_S = R[t];
        else
            AMAIR0_NS = R[t];

The AMAIR1 characteristics are:

**Purpose**

When using the Long-descriptor format translation tables for stage 1 translations, provides IMPLEMENTATION DEFINED memory attributes for the memory regions specified by MAIR1.

**Configuration**

AArch32 System register AMAIR1 bits [31:0] are architecturally mapped to AArch64 System register AMAIR_EL1[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to AMAIR1 are UNDEFINED.

When EL3 is using AArch32, write access to AMAIR1(S) is disabled when the CP15SDISABLE signal is asserted HIGH.

**Attributes**

AMAIR1 is a 32-bit register.

**Field descriptions**

The AMAIR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

This register is RES0 in the following cases:

- When an implementation does not provide any IMPLEMENTATION DEFINED memory attributes.
- When the Long-descriptor translation table format is not used.

If EL3 is implemented and is using AArch32:

- AMAIR1(S) gives the value for memory accesses from Secure state.
- AMAIR1(NS) gives the value for memory accesses from Non-secure states other than Hyp mode.

Any IMPLEMENTATION DEFINED memory attributes are additional qualifiers for the memory locations and must not change the architected behavior specified by MAIR0 and MAIR1.

In a typical implementation, AMAIR0 and AMAIR1 split into eight one-byte fields, corresponding to the MAIRn.Attr<n> fields, but the architecture does not require them to do so.

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the AMAIR1**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return AMAIR1_NS;
  else
    return AMAIR1;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return AMAIR1_NS;
  else
    return AMAIR1;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return AMAIR1_S;
  else
    return AMAIR1_NS;
else
  return AMAIR1_NS;

if PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return AMAIR1_NS;
  else
    return AMAIR1;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return AMAIR1_S;
  else
    return AMAIR1_NS;
else
  return AMAIR1_NS;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        AMAIR1_NS = R[t];
    else
        AMAIR1 = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        AMAIR1_NS = R[t];
    else
        AMAIR1 = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            AMAIR1_S = R[t];
        else
            AMAIR1_NS = R[t];

AMCFGR, Activity Monitors Configuration Register

The AMCFGR characteristics are:

**Purpose**

Global configuration register for the activity monitors.

Provides information on supported features, the number of counter groups implemented, the total number of activity monitor event counters implemented, and the size of the counters. AMCFGR is applicable to both the architected and the auxiliary counter groups.

**Configuration**

AArch32 System register AMCFGR bits [31:0] are architecturally mapped to AArch64 System register AMCFGR_EL0[31:0].

AArch32 System register AMCFGR bits [31:0] are architecturally mapped to External register AMCFGR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCFGR are UNDEFINED.

**Attributes**

AMCFGR is a 32-bit register.

**Field descriptions**

The AMCFGR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NCG | RES0 | HDBG | RAZ | SIZE | N |

**NCG, bits [31:28]**

Defines the number of counter groups.

The number of implemented counter groups is defined as \([\text{AMCFGR.NCG} + 1]\).

If the number of implemented auxiliary activity monitor event counters is zero, this field has a value of \(0b0000\). Otherwise, this field has a value of \(0b0001\).

**Bits [27:25]**

Reserved, RES0.

**HDBG, bit [24]**

Halt-on-debug supported.

From Armv8, this feature must be supported, and so this bit is \(0b1\).

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>AMCR.HDBG is RES0.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>AMCR.HDBG is read/write.</td>
</tr>
</tbody>
</table>
Bits [23:14]

Reserved, RAZ.

SIZE, bits [13:8]

Defines the size of activity monitor event counters.

The size of the activity monitor event counters implemented by the Activity Monitors Extension is defined as \([\text{AMCFGR.SIZE} + 1]\). From Armv8, the counters are 64-bit, and so this field is \(0b111111\).

Note

Software also uses this field to determine the spacing of counters in the memory-map. From Armv8, the counters are at doubleword-aligned addresses.

N, bits [7:0]

Defines the number of activity monitor event counters.

The total number of counters implemented in all groups by the Activity Monitors Extension is defined as \([\text{AMCFGR.N} + 1]\).

Accessing the AMCFGR

Accesses to this register use the following encodings:

\[
\text{MRC\{<c}\{<q>\} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

AMCFGR, Activity Monitors Configuration Register
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
            else
                AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
    else
        UNDEFINED;
    end
else
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
end
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR_EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 != '11' && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end
        else
            return AMCFGR;
        end
    elsif PSTATE.EL == EL3 then
        return AMCFGR;
    end
else
    return AMCFGR;
end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    else
        return AMCFGR;
    end
elsif PSTATE.EL == EL3 then
    return AMCFGR;
The AMCGCR characteristics are:

**Purpose**

Provides information on the number of activity monitor event counters implemented within each counter group.

**Configuration**

AArch32 System register AMCGCR bits [31:0] are architecturally mapped to AArch64 System register AMCGCR_EL0[31:0].

AArch32 System register AMCGCR bits [31:0] are architecturally mapped to External register AMCGCR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCGCR are UNDEFINED.

**Attributes**

AMCGCR is a 32-bit register.

**Field descriptions**

The AMCGCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>CG1NC</td>
</tr>
<tr>
<td>29</td>
<td>CG0NC</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**CG1NC, bits [15:8]**

Counter Group 1 Number of Counters. The number of counters in the auxiliary counter group.

In an implementation that includes FEAT_AMUv1, the permitted range of values is 0 to 16.

**CG0NC, bits [7:0]**

Counter Group 0 Number of Counters. The number of counters in the architected counter group.

In an implementation that includes FEAT_AMUv1, the value of this field is 4.

**Accessing the AMCGCR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    elsif EL2Enabled() && !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch32.TakeHypTrapException(0x00);
        end if;
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if;
        else
            return AMCGCR;
        end if;
    elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 != '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if;
        else
            return AMCGCR;
        end if;
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if;
        end if;
    elsif PSTATE.EL == EL3 then
        return AMCGCR;
    end if;
else
    return AMCGCR;
end if;

AMCGCR, Activity Monitors Counter Group Configuration Register
AMCNTENCLR0, Activity Monitors Count Enable Clear Register 0

The AMCNTENCLR0 characteristics are:

**Purpose**

Disable control bits for the architected activity monitors event counters, AMEVCNTR0<n>.

**Configuration**

AArch32 System register AMCNTENCLR0 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENCLR0_EL0[31:0].

AArch32 System register AMCNTENCLR0 bits [31:0] are architecturally mapped to External register AMCNTENCLR0[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR0 are UNDEFINED.

**Attributes**

AMCNTENCLR0 is a 32-bit register.

**Field descriptions**

The AMCNTENCLR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

Bits [31:16]

Reserved, RES0.

P<n>, bit [n], for n = 15 to 0

Activity monitor event counter disable bit for AMEVCNTR0<n>.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR.CG0NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR0&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR0&lt;n&gt; is enabled. When written, disables AMEVCNTR0&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENCLR0**

Accesses to this register use the following encodings:
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  elsif EL2Enabled() && ELUsingAArch32(EL2) && !EDSCR.SDD == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x00);
  else
    UNDEFINED;
  end if
elsif EL2Enabled() && !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  end if
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HAFGRTR_EL2.AMCNTEN0 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTE == '1') && HAFGRTR_EL2.AMCNTEN0 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if
else
  return AMCNTENCLR0;
end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
else
  return AMCNTENCLR0;
end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
else
  return AMCNTENCLR0;
end if
elsif PSTATE.EL == EL3 then
  return AMCNTENCLR0;
end if
if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) then
  AMCNTENCLR0 = R[t];
else
  UNDEFINED;

Table:

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>

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AMCNTENCLR1, Activity Monitors Count Enable Clear Register 1

The AMCNTENCLR1 characteristics are:

**Purpose**

Disable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>.

**Configuration**

AArch32 System register AMCNTENCLR1 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENCLR1_EL0[31:0].

AArch32 System register AMCNTENCLR1 bits [31:0] are architecturally mapped to External register AMCNTENCLR1[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR1 are UNDEFINED.

**Attributes**

AMCNTENCLR1 is a 32-bit register.

**Field descriptions**

The AMCNTENCLR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | P15 | P14 | P13 | P12 | P11 | P10 | P9 | P8 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 |

**Bits [31:16]**

Reserved, RES0.

**P<n>, bit [n], for n = 15 to 0**

Activity monitor event counter disable bit for AMEVCNTR1<n>.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR_EL0.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>(P&lt;n&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is enabled. When written, disables AMEVCNTR1&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENCLR1**

If the number of auxiliary activity monitor event counters implemented is zero, reads and writes of AMCNTENCLR1 are UNDEFINED.

**Note**


The number of auxiliary activity monitor event counters implemented is zero exactly when `AMCFGR.NCG == 0b0000`.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \coproc, \{#\}<opc1>, \Rt, \CRn, \CRm, \{#\}<opc2>\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) & AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        endif
    else
        UNDEFINED;
    endif
elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.<E2H,TGE> != '1' & HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else
    return AMCNTENCLR1;
else
    return AMCNTENCLR1;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    endif
else
    return AMCNTENCLR1;
else
    return AMCNTENCLR1;
 elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & CPTR_EL3.TAM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return AMCNTENCLR1;
    else
        return AMCNTENCLR1;
 elsif PSTATE.EL == EL3 then
    return AMCNTENCLR1;
MCR{<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) then
    AMCNTENCLR1 = R[t];
else
    UNDEFINED;

30/09/2020 15:07; cceed0cb9f089f9ceec50268e82aec9e71047211
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AMCNTENSET0, Activity Monitors Count Enable Set Register 0

The AMCNTENSET0 characteristics are:

### Purpose

Enable control bits for the architected activity monitors event counters, \texttt{AMEVCNTR0<n>}.

### Configuration

AArch32 System register AMCNTENSET0 bits [31:0] are architecturally mapped to AArch64 System register \texttt{AMCNTENSET0_EL0[31:0]}.

AArch32 System register AMCNTENSET0 bits [31:0] are architecturally mapped to External register \texttt{AMCNTENSET0[31:0]}.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET0 are UNDEFINED.

### Attributes

AMCNTENSET0 is a 32-bit register.

### Field descriptions

The AMCNTENSET0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>P15</td>
<td>P14</td>
<td>P13</td>
<td>P12</td>
<td>P11</td>
<td>P10</td>
<td>P9</td>
<td>P8</td>
<td>P7</td>
<td>P6</td>
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<td>P4</td>
<td>P3</td>
<td>P2</td>
<td>P1</td>
<td>P0</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**\texttt{P<n>}, bit \texttt{[n]}, for \texttt{n = 15 to 0}**

Activity monitor event counter enable bit for \texttt{AMEVCNTR0<n>}.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in \texttt{AMCGCR.CG0NC}.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>\texttt{P&lt;n&gt;}</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that \texttt{AMEVCNTR0&lt;n&gt;} is disabled. When written, has no effect.</td>
</tr>
</tbody>
</table>
| 0b1          | When read, means that \texttt{AMEVCNTR0<n>} is enabled. When written, enables \texttt{AMEVCNTR0<n>}.

On a Cold reset, this field resets to 0.

### Accessing the AMCNTENSET0

Accesses to this register use the following encodings:
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        UNDEFINED;
      endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
      else
        UNDEFINED;
      endif
    elsif EL2Enabled() && AMUSERENR.EN == '0' then
      if EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
      elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
      elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elseif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x00);
      elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elseif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x00);
      elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && (HaveEL(EL3) || SCR_EL3.FGTE == '1') && HAFGTR_EL2.AMCNTEN0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
      elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && AMUSERENR_EL0.T13 == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
          AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
          AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
          else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
          endif
        else
          return AMCNTENSET0;
        endif
      elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
          AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
          AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
          else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
          endif
        else
          return AMCNTENSET0;
        endif
      elsif PSTATE.EL == EL3 then
        return AMCNTENSET0;
      else
        return AMCNTENSET0;
      endif
    else
      return AMCNTENSET0;
    endif
  else
    return AMCNTENSET0;
  endif
else
  return AMCNTENSET0;
endif
else
  return AMCNTENSET0;
else
  return AMCNTENSET0;
endif
else
  return AMCNTENSET0;
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) then
    AMCNTENSE0 = R[t];
else
    UNDEFINED;
The AMCNTENSET1 characteristics are:

**Purpose**

Enable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>.

**Configuration**

AArch32 System register AMCNTENSET1 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENSET1_EL0[31:0].

AArch32 System register AMCNTENSET1 bits [31:0] are architecturally mapped to External register AMCNTENSET1[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET1 are UNDEFINED.

**Attributes**

AMCNTENSET1 is a 32-bit register.

**Field descriptions**

The AMCNTENSET1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>P15</td>
</tr>
<tr>
<td>29</td>
<td>P14</td>
</tr>
<tr>
<td>28</td>
<td>P13</td>
</tr>
<tr>
<td>27</td>
<td>P12</td>
</tr>
<tr>
<td>26</td>
<td>P11</td>
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<td>25</td>
<td>P10</td>
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<td>24</td>
<td>P9</td>
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<td>22</td>
<td>P7</td>
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<td>P3</td>
</tr>
<tr>
<td>17</td>
<td>P2</td>
</tr>
<tr>
<td>16</td>
<td>P1</td>
</tr>
<tr>
<td>15</td>
<td>P0</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0.</td>
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<tr>
<td>7</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**P<n>**, bit [n], for n = 15 to 0

Activity monitor event counter enable bit for AMEVCNTR1<n>.

Bits [31:16] are RES0. Bits [15:N] are RAZ/WI. N is the value in AMCGCR.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is enabled. When written, enables AMEVCNTR1&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENSET1**

If the number of auxiliary activity monitor event counters implemented is zero, reads and writes of AMCNTENSET1 are UNDEFINED.
The number of auxiliary activity monitor counters implemented is zero when \texttt{AMCFGR.NCG == 0b0000}.

Accesses to this register use the following encodings:

\[
\text{MRC\{<c}\}{\{<q>\} \ <\text{coproc}, \ {#}<\text{opc1}, \ <\text{Rt}, \ <\text{CRn}, \ <\text{CRm}\{, \ {#}<\text{opc2}\}}
\]

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<td>0b000</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then UNDEFINED;
else if !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
else if EL2Enabled() && ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
else if EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL1) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL1) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL1) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMCNTE1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else
    if EL2Enabled() && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        return AMCNTENSET1;
else if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then UNDEFINED;
else if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then UNDEFINED;
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
else
    return AMCNTENSET1;
else if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then UNDEFINED;
else if EL2Enabled() && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then UNDEFINED;
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
else
    return AMCNTENSET1;
else if PSTATE.EL == EL3 then
    return AMCNTENSET1;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) then
  AMCNTENSET1 = R[t];
else
  UNDEFINED;
AMCR, Activity Monitors Control Register

The AMCR characteristics are:

**Purpose**

Global control register for the activity monitors implementation. AMCR is applicable to both the architected and the auxiliary counter groups.

**Configuration**

AArch32 System register AMCR bits [31:0] are architecturally mapped to AArch64 System register AMCR_EL0[31:0].

AArch32 System register AMCR bits [31:0] are architecturally mapped to External register AMCR[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCR are UNDEFINED.

**Attributes**

AMCR is a 32-bit register.

**Field descriptions**

The AMCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
|     | CG1RZ | RES0 |   | HDBG | RES0 |

**Bits [31:18]**

Reserved, RES0.

**CG1RZ, bit [17]**

*When FEAT_AMUv1p1 is implemented:*

Counter Group 1 Read Zero.

<table>
<thead>
<tr>
<th>CG1RZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>System register reads of AMEVCNTR1&lt;n&gt; return the event count at all implemented and enabled Exception levels.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the current Exception level is the highest implemented Exception level, system register reads of AMEVCNTR1&lt;n&gt; return the event count. Otherwise, reads of AMEVCNTR1&lt;n&gt; return a zero value.</td>
</tr>
</tbody>
</table>

**Note**

Reads from the memory-mapped view are unaffected by this field.

**Otherwise:**

Reserved, RES0.
Bits [16:11]
Reserved, RES0.

HDBG, bit [10]
This bit controls whether activity monitor counting is halted when the PE is halted in Debug state.

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Activity monitors do not halt counting when the PE is halted in Debug state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Activity monitors halt counting when the PE is halted in Debug state.</td>
</tr>
</tbody>
</table>

Bits [9:0]
Reserved, RES0.

Accessing the AMCR
Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>, \{#\}<opc2>} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        endif
    elsif EL2Enabled() &! ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
        if EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T13 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x03);
        else
            UNDEFINED;
        endif
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return AMCR;
    endif
else
    return AMCR;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL2) && AMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            endif
        else
            return AMCR;
        endif
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            endif
        else
            return AMCR;
        endif
    elsif PSTATE.EL == EL3 then
        return AMCR;
    endif
else
    return AMCR;
end if

MCR\{c\}\{q\} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) then
    AMCR = R[t];
else
    UNDEFINED;

AMEVCNTR0\<n\>, Activity Monitors Event Counter Registers 0, n = 0 - 15

The AMEVCNTR0\<n\> characteristics are:

**Purpose**

Provides access to the architected activity monitor event counters.

**Configuration**

AArch32 System register AMEVCNTR0\<n\> bits [63:0] are architecturally mapped to AArch64 System register AMEVCNTR0\<n\>\_EL0[63:0].

AArch32 System register AMEVCNTR0\<n\> bits [63:0] are architecturally mapped to External register AMEVCNTR0\<n\>[63:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR0\<n\> are UNDEFINED.

**Attributes**

AMEVCNTR0\<n\> is a 64-bit register.

**Field descriptions**

The AMEVCNTR0\<n\> bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | ACNT |

ACNT, bits [63:0]

Architected activity monitor event counter n.

Value of architected activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If FEAT_AMUv1p1 is implemented, HCR\_EL2.AMVOFFEN is 1, SCR\_EL3.AMVOFFEN is 1, HCR\_EL2.\{E2H, TGE\} is not \{1,1\}, and EL2 is using AArch64 and is implemented in the current Security state, access to these registers at EL0 or EL1 return (PCount\<63:0\> - AMEVCNTRV0\<n\>_EL2<63:0>).

PCount is the physical count returned when AMEVCNTR0\<n\> is read from EL2 or EL3.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

**Accessing the AMEVCNTR0\<n\>**

If \<n\> is greater than or equal to the number of architected activity monitor event counters, reads and writes of AMEVCNTR0\<n\> are UNDEFINED.

---

**Note**
AMCGCR.CG0NC identifies the number of architected activity monitor event counters.

Accesses to this register use the following encodings:

\[
\text{MRRC}\{<c>\}{<q>} \quad \text{coproc}, \quad \{#\}<\text{opc1}>, \quad <\text{Rt}>, \quad <\text{Rt2}>, \quad <\text{CRm}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000:n[3]</td>
<td>0b0:n[2:0]</td>
</tr>
</tbody>
</table>
if CRm == '0000' then
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    endif
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HAFGRTR_EL2.AMEVCNTR0<n>_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x04);
  endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    endif
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    endif
  else
    return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
  endif
endif
else
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    endif
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    endif
  else
    return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
  endif
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      endif
    endif
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrapException(0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    endif
  else
    return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
  endif
endif
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x04);
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif
else
  return AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)];
endif

```plaintext
MCRR{<coproc>, {#<opc1>, <Rt>, <Rt2>, <CRm>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000:n[3]</td>
<td>0b0:n[2:0]</td>
</tr>
</tbody>
</table>

if CRm == '0000' then
  if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif IsHighestEL(PSTATE.EL) then
    AMEVCNTR0[UInt(CRm<0>:opc1<2:0>)] = R[t2]:R[t];
  else
    UNDEFINED;
else
  UNDEFINED;
```

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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AMEVCNTR1<n>, Activity Monitors Event Counter Registers 1, n = 0 - 15

The AMEVCNTR1<n> characteristics are:

**Purpose**

Provides access to the auxiliary activity monitor event counters.

**Configuration**

AArch32 System register AMEVCNTR1<n> bits [63:0] are architecturally mapped to AArch64 System register AMEVCNTR1<n>_EL0[63:0].

AArch32 System register AMEVCNTR1<n> bits [63:0] are architecturally mapped to External register AMEVCNTR1<n>[63:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR1<n> are UNDEFINED.

**Attributes**

AMEVCNTR1<n> is a 64-bit register.

**Field descriptions**

The AMEVCNTR1<n> bit assignments are:

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|

**ACNT, bits [63:0]**

Auxiliary activity monitor event counter n.

Value of auxiliary activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If FEAT_AMUv1p1 is implemented, HCR_EL2.AMVOFFEN is 1, SCR_EL3.AMVOFFEN is 1, HCR_EL2.{E2H, TGE} is not {1,1}, EL2 is using AArch64 and is implemented in the current Security state, and AMCR_EL0.CG1RZ is 0, reads to these registers at EL0 or EL1 return (PCount<63:0> - AMEVCNTVOFF1<n>_EL2<63:0>).

PCount is the physical count returned when AMEVCTR1<n> is read from EL2 or EL3.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

**Accessing the AMEVCNTR1<n>**

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads and writes of AMEVCNTR1<n> are UNDEFINED.

---

**Note**
AMCGCR.CG1NC identifies the number of auxiliary activity monitor event counters.

Accesses to this register use the following encodings:

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b010:n[3]</td>
<td>0b0:n[2:0]</td>
</tr>
</tbody>
</table>
if CRm == '0100' then
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      end if;
    elsif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x04);
      else
        UNDEFINED;
      end if;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      elsif !HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
        return Zeros();
      elsif HighestELUsingAArch32() && AMCR.CG1RZ == '1' then
        return Zeros();
      else
        return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
      end if;
    else
      return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
    end if;
  else
    if PSTATE.EL == EL1 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
      elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x04);
      elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        elsif !IsHighestEL(PSTATE.EL) && !HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
          return Zeros();
        elsif !IsHighestEL(PSTATE.EL) && HighestELUsingAArch32() && AMCR.CG1RZ == '1' then
          return Zeros();
        else
          return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
        end if;
      else
        return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
      end if;
    else
      if PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
          if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
          else
            AArch64.AArch32SystemAccessTrap(EL3, 0x04);
          end if;
        elsif !IsHighestEL(PSTATE.EL) && !HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
          return Zeros();
        elsif !IsHighestEL(PSTATE.EL) && HighestELUsingAArch32() && AMCR.CG1RZ == '1' then
          return Zeros();
        else
          return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
        end if;
      else
        return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
      end if;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    end if;
  end if;
else
  if PSTATE.EL == EL2 then
    AArch64.AArch32SystemAccessTrap(EL3, 0x04);
  end if;
end if;
return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];

elsif CRm == '0101' then
  if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
      end
    elseif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        UNDEFINED;
      end
    elseif ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch32.TakeHypTrapException(0x00);
      end
    elseif EL2Enabled() && !ELUsingAArch32(EL1) && HSTR_EL2.T5 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elseif HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
      return Zeros();
    else
      return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
    end
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elsif !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
      AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
      AArch32.TakeHypTrapException(0x04);
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x04);
      end
    elseif HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
      return Zeros();
    else
      return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
    end
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      UNDEFINED;
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
      end
    end
  end
end
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x04);
elsif !IsHighestEL(PSTATE.EL) && !HighestELUsingAArch32() && AMCR_EL0.CG1RZ == '1' then
    return Zeros();
elsif !IsHighestEL(PSTATE.EL) && HighestELUsingAArch32() && AMCR.CG1RZ == '1' then
    return Zeros();
else
    return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
elsif PSTATE.EL == EL3 then
    return AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)];
else
    UNDEFINED;

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b010:n[3]</td>
<td>0b0:n[2:0]</td>
</tr>
</tbody>
</table>

if CRm == '0100' then
    if IsHighestEL(PSTATE.EL) then
        AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)] = R[t2]:R[t];
    else
        UNDEFINED;
elsif CRm == '0110' then
    if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif IsHighestEL(PSTATE.EL) then
        AMEVCNTR1[UInt(CRm<0>:opc1<2:0>)] = R[t2]:R[t];
    else
        UNDEFINED;
else
    UNDEFINED;

AMEVTYPER0<n>, Activity Monitors Event Type Registers 0, n = 0 - 15

The AMEVTYPER0<n> characteristics are:

**Purpose**

Provides information on the events that an architected activity monitor event counter AMEVCNTR0<n> counts.

**Configuration**

AArch32 System register AMEVTYPER0<n> bits [31:0] are architecturally mapped to AArch64 System register AMEVTYPER0<n>_EL0[31:0].

AArch32 System register AMEVTYPER0<n> bits [31:0] are architecturally mapped to External register AMEVTYPER0<n>[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER0<n> are UNDEFINED.

**Attributes**

AMEVTYPER0<n> is a 32-bit register.

**Field descriptions**

The AMEVTYPER0<n> bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>30 - 16</td>
<td>evtCount</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**evtCount, bits [15:0]**

Event to count. The event number of the event that is counted by the architected activity monitor event counter AMEVCNTR0<n>. The value of this field is architecturally mandated for each architected counter.

The following table shows the mapping between required event numbers and the corresponding counters:

<table>
<thead>
<tr>
<th>evtCount</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0011</td>
<td>Processor frequency cycles</td>
<td>When n == 0</td>
</tr>
<tr>
<td>0x4004</td>
<td>Constant frequency cycles</td>
<td>When n == 1</td>
</tr>
<tr>
<td>0x0008</td>
<td>Instructions retired</td>
<td>When n == 2</td>
</tr>
<tr>
<td>0x4005</td>
<td>Memory stall cycles</td>
<td>When n == 3</td>
</tr>
</tbody>
</table>

**Accessing the AMEVTYPER0<n>**

If <n> is greater than or equal to the number of architected activity monitor event counters, reads and writes of AMEVTYPER0<n> are UNDEFINED.

**Note**
AMCGC CR identifies the number of architected activity monitor event counters.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \text{<coproc>}, \{#\text{<opc1>}, \text{<Rt>}, \text{<CRn>}, \text{<CRm>}, \{#\text{<opc2>}}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b011:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && AMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end
else
  return AMEVTYPER0[UInt(CRm<0>:opc2<2:0>)];
end

elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return AMEVTYPER0[UInt(CRm<0>:opc2<2:0>)];
end

elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return AMEVTYPER0[UInt(CRm<0>:opc2<2:0>)];
end

elsif PSTATE.EL == EL3 then
  return AMEVTYPER0[UInt(CRm<0>:opc2<2:0>)];
else
  return AMEVTYPER0[UInt(CRm<0>:opc2<2:0>)];
end
AMEVTYPER1<n>, Activity Monitors Event Type Registers 1, n = 0 - 15

The AMEVTYPER1<n> characteristics are:

Purpose

Provides information on the events that an auxiliary activity monitor event counter AMEVCNTR1<n> counts.

Configuration

AArch32 System register AMEVTYPER1<n> bits [31:0] are architecturally mapped to AArch64 System register AMEVTYPER1<n>_EL0[31:0].

AArch32 System register AMEVTYPER1<n> bits [31:0] are architecturally mapped to External register AMEVTYPER1<n>[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER1<n> are UNDEFINED.

Attributes

AMEVTYPER1<n> is a 32-bit register.

Field descriptions

The AMEVTYPER1<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|     |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| evtCount |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Bits [31:16]

Reserved, RES0.

evtCount, bits [15:0]

Event to count. The event number of the event that is counted by the auxiliary activity monitor event counter AMEVCNTR1<n>.

It is IMPLEMENTATION DEFINED what values are supported by each counter.

If software writes a value to this field which is not supported by the corresponding counter AMEVCNTR1<n>, then:

- It is UNPREDICTABLE which event will be counted.
- The value read back is UNKNOWN.

The event counted by AMEVCNTR1<n> might be fixed at implementation. In this case, the field is read-only and writes are UNDEFINED.

If the corresponding counter AMEVCNTR1<n> is enabled, writes to this register have UNPREDICTABLE results.

Accessing the AMEVTYPER1<n>

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads and writes of AMEVTYPER1<n> are UNDEFINED.
**Note**

AMCGCR.CG1NC identifies the number of auxiliary activity monitor event counters.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\{, \{#\}<\text{opc2}\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b111:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && AMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        endif
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        endif
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTeN == '1') && HAFGRTR_EL2.AMEVTYPER1<n>._EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
    endif
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTeN == '1') && HAFGRTR_EL2.AMEVTYPER1<n>._EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
        endif
    else
        return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
    endif
elsif PSTATE.EL == EL3 then
    return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
else
    return AMEVTYPER1[UInt(CRm<0>:opc2<2:0>)];
endif
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b111:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL1 && EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif IsHighestEL(PSTATE.EL) && !boolean IMPLEMENTATION_DEFINED "AMEVCNTR1<n> is fixed" then
  AMEVTYPE1[UInt(CRm<0>:opc2<2:0>)] = R[t];
else
  UNDEFINED;

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AMUSERENR, Activity Monitors User Enable Register

The AMUSERENR characteristics are:

**Purpose**

Global user enable register for the activity monitors. Enables or disables EL0 access to the activity monitors. AMUSERENR is applicable to both the architected and the auxiliary counter groups.

**Configuration**

AArch32 System register AMUSERENR bits [31:0] are architecturally mapped to AArch64 System register AMUSERENR_EL0[31:0].

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMUSERENR are UNDEFINED.

**Attributes**

AMUSERENR is a 32-bit register.

**Field descriptions**

The AMUSERENR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
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<tr>
<td>21</td>
<td></td>
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<td>20</td>
<td></td>
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<tr>
<td>19</td>
<td></td>
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<td>18</td>
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<td>17</td>
<td></td>
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<td>16</td>
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<td>15</td>
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<td>14</td>
<td></td>
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<td>13</td>
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<tr>
<td>12</td>
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<tr>
<td>11</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
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<tr>
<td>9</td>
<td></td>
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<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>EN</td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reserved, RES0.

**EN, bit [0]**

Traps EL0 accesses to the activity monitors registers to EL1.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 accesses to the activity monitors registers are trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped. Software can access all activity monitor registers at EL0.</td>
</tr>
</tbody>
</table>

**Note**

- AMUSERENR can always be read at EL0 and is not governed by this bit.

**Accessing the AMUSERENR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \ <\text{coproc}, \ <\text{opc1}, \ <\text{CRn}, \ <\text{CRm}, \ <\text{opc2}\}\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return AMUSERENR;
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return AMUSERENR;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return AMUSERENR;
  end if;
elsif PSTATE.EL == EL3 then
  return AMUSERENR;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TAM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TAM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    else
        AMUSERENR = R[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TAM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    else
        AMUSERENR = R[t];
    end if;
elsif PSTATE.EL == EL3 then
    AMUSERENR = R[t];
end if;
APSR, Application Program Status Register

The APSR characteristics are:

**Purpose**

Hold program status and control information.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to APSR are UNDEFINED.

**Attributes**

APSR is a 32-bit register.

**Field descriptions**

The APSR bit assignments are:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| N  | Z  | C  | V  | Q  | RES0| GE | RES0| RES1| RES0|
```

**N, bit [31]**

Negative condition flag. Set to \( [31] \) of the result of the last flag-setting instruction. If the result is regarded as a two’s complement signed integer, then \( N \) is set to 1 if the result was negative, and \( N \) is set to 0 if the result was positive or zero.

**Z, bit [30]**

Zero condition flag. Set to 1 if the result of the last flag-setting instruction was zero, and to 0 otherwise. A result of zero often indicates an equal result from a comparison.

**C, bit [29]**

Carry condition flag. Set to 1 if the last flag-setting instruction resulted in a carry condition, for example an unsigned overflow on an addition.

**V, bit [28]**

Overflow condition flag. Set to 1 if the last flag-setting instruction resulted in an overflow condition, for example a signed overflow on an addition.

**Q, bit [27]**

Cumulative saturation bit. Set to 1 to indicate that overflow or saturation occurred in some instructions.

**Bits [26:20]**

Reserved, RES0.
**GE, bits [19:16]**

Greater than or Equal flags, for parallel addition and subtraction.

**Bits [15:5]**

Reserved, RES0.

**Bit [4]**

Reserved, RES1.

**Bits [3:0]**

Reserved, RES0.

It is permitted that, on a read of APSR:

- Bit[22] returns the value of PSTATE.PAN
- Bit[9] returns the value of PSTATE.E.
- Bit[4:0] returns the value of PSTATE.M[4:0]

---

**Note**

This is an exception to the general rule that an UNKNOWN field must not return information that cannot be obtained, at the current Privilege level, by an architected mechanism.

---

For more information see 'The Application Program Status Register, APSR'.

**Accessing the APSR**

APSR can be read using the MRS instruction and written using the MSR (register) or MSR (immediate) instructions.
ATS12NSOPR, Address Translate Stages 1 and 2 Non-secure Only PL1 Read

The ATS12NSOPR characteristics are:

**Purpose**

Performs stage 1 and 2 address translations as defined for PL1 and the Non-secure state, with permissions as if reading from the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS12NSOPR are **UNDEFINED**.

**Attributes**

ATS12NSOPR is a 32-bit System instruction.

**Field descriptions**

The ATS12NSOPR input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Input address for translation**

Bits [31:0]

Input address for translation. The resulting address can be read from the **PAR**.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the stage 2 translation.

**Executing the ATS12NSOPR instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
eelsif PSTATE_EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
eelsif PSTATE_EL == EL2 then
    ATS12NSOPR(R[t]);
eelsif PSTATE_EL == EL3 then
    ATS12NSOPR(R[t]);
ATS12NSOPW, Address Translate Stages 1 and 2 Non-secure Only PL1 Write

The ATS12NSOPW characteristics are:

**Purpose**

Performs stage 1 and 2 address translations as defined for PL1 and the Non-secure state, with permissions as if writing to the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS12NSOPW are UNDEFINED.

**Attributes**

ATS12NSOPW is a 32-bit System instruction.

**Field descriptions**

The ATS12NSOPW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

| Input address for translation |

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the stage 2 translation.

**Executing the ATS12NSOPW instruction**

Accesses to this instruction use the following encodings:

\[ \text{MCR}\{<c>\}{<q>} \{<coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>}} \}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  ATS12NSOPW(R[t]);
elsif PSTATE.EL == EL3 then
  ATS12NSOPW(R[t]);
The ATS12NSOUR characteristics are:

**Purpose**

Performs stage 1 and 2 address translations as defined for PL0 and the Non-secure state, with permissions as if reading from the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS12NSOUR are UNDEFINED.

**Attributes**

ATS12NSOUR is a 32-bit System instruction.

**Field descriptions**

The ATS12NSOUR input value bit assignments are:

```
  31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
    1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0   1   0
Input address for translation
```

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the stage 2 translation.

**Executing the ATS12NSOUR instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    ATS12NSOUR(R[t]);
elsif PSTATE.EL == EL3 then
    ATS12NSOUR(R[t]);
ATS12NSOUW, Address Translate Stages 1 and 2 Non-secure Only Unprivileged Write

The ATS12NSOUW characteristics are:

**Purpose**

Performs stage 1 and 2 address translations as defined for PL0 and the Non-secure state, with permissions as if writing to the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS12NSOUW are **UNDEFINED**.

**Attributes**

ATS12NSOUW is a 32-bit System instruction.

**Field descriptions**

The ATS12NSOUW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **Input address for translation** |

**Bits [31:0]**

Input address for translation. The resulting address can be read from the `PAR`.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the stage 2 translation.

**Executing the ATS12NSOUW instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th><code>coproc</code></th>
<th><code>opc1</code></th>
<th><code>CRn</code></th>
<th><code>CRm</code></th>
<th><code>opc2</code></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
elif !ELUsingAArch32(EL2) && SCR_EL2.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
elif PSTATE.EL == EL2 then
    ATS12NSOUW(R[t]);
elif PSTATE.EL == EL3 then
    ATS12NSOUW(R[t]);
ATS1CPR, Address Translate Stage 1 Current state PL1 Read

The ATS1CPR characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL1 and the current Security state, with permissions as if reading from the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1CPR are UNDEFINED.

**Attributes**

ATS1CPR is a 32-bit System instruction.

**Field descriptions**

The ATS1CPR input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Input address for translation

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CPR instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#\}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CPR(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1CPR(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1CPR(R[t]);
ATS1CPRP, Address Translate Stage 1 Current state
PL1 Read PAN

The ATS1CPRP characteristics are:

**Purpose**

Performs a stage 1 address translation at PL1 and in the current Security state, where the value of PSTATE.PAN determines if a read from a location will generate a permission fault for a privileged access.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level and FEAT_PAN2 is implemented. Otherwise, direct accesses to ATS1CPRP are UNDEFINED.

**Attributes**

ATS1CPRP is a 32-bit System instruction.

**Field descriptions**

The ATS1CPRP input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Input address for translation**

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CPRP instruction**

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CPRP(R[t]);
    end if
elsif PSTATE.EL == EL2 then
    ATS1CPRP(R[t]);
eisif PSTATE.EL == EL3 then
    ATS1CPRP(R[t]);

**ATS1CPW, Address Translate Stage 1 Current state PL1 Write**

The ATS1CPW characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL1 and the current Security state, with permissions as if writing to the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1CPW are UNDEFINED.

**Attributes**

ATS1CPW is a 32-bit System instruction.

**Field descriptions**

The ATS1CPW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Input address for translation**

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CPW instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{c\}\{q\} \text{<coproc>, } \{\#\text{<opc1>}, \text{<Rt>, } \text{<CRn>, } \text{<CRm>}, \{\#\text{<opc2>}}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CPW(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1CPW(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1CPW(R[t]);

The ATS1CPWP characteristics are:

**Purpose**

Performs a stage 1 address translation at PL1 and in the current Security state, where the value of PSTATE.PAN determines if a write to the location will generate a permission fault for a privileged access.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level and FEAT_PAN2 is implemented. Otherwise, direct accesses to ATS1CPWP are UNDEFINED.

**Attributes**

ATS1CPWP is a 32-bit System instruction.

**Field descriptions**

The ATS1CPWP input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Input address for translation |

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CPWP instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \text{<coproc>}, \{#\}\text{<opc1>}, \text{<Rt>}, \text{<CRn>}, \text{<CRm>}, \{#\}\text{<opc2>}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
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<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CPWP(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1CPWP(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1CPWP(R[t]);
The ATS1CUR characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL0 and the current Security state, with permissions as if reading from the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1CUR are UNDEFINED.

**Attributes**

ATS1CUR is a 32-bit System instruction.

**Field descriptions**

The ATS1CUR input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Input address for translation |

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CUR instruction**

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CUR(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1CUR(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1CUR(R[t]);

The ATS1CUW characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL0 and the current Security state, with permissions as if writing to the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1CUW are UNDEFINED.

**Attributes**

ATS1CUW is a 32-bit System instruction.

**Field descriptions**

The ATS1CUW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Input address for translation**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. If EL2 is implemented and enabled in the current Security state, the resulting address is the IPA that is the output address of the stage 1 translation. Otherwise, the resulting address is a PA.

**Executing the ATS1CUW instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} \text{<coproc>, \{#<opc1>, \text{<Rt>}, <CRn>, <CRm>\}, \{#<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
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<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1CUW(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1CUW(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1CUW(R[t]);
ATS1HR, Address Translate Stage 1 Hyp mode Read

The ATS1HR characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL2 and the Non-secure state, with permissions as if reading from the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1HR are UNDEFINED.

**Attributes**

ATS1HR is a 32-bit System instruction.

**Field descriptions**

The ATS1HR input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Input address for translation</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the translation.

**Executing the ATS1HR instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

MCR{<c>{<q}>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
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<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1HR(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ATS1HR(R[t]);
elsif PSTATE.EL == EL3 then
    ATS1HR(R[t]);

ATS1HW, Address Translate Stage 1 Hyp mode Write

The ATS1HW characteristics are:

**Purpose**

Performs stage 1 address translation as defined for PL2 and the Non-secure state, with permissions as if writing to the given virtual address.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ATS1HW are UNDEFINED.

**Attributes**

ATS1HW is a 32-bit System instruction.

**Field descriptions**

The ATS1HW input value bit assignments are:

```
31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
```

**Input address for translation**

Bits [31:0]

Input address for translation. The resulting address can be read from the PAR.

This System instruction takes a VA as input. The resulting address is the PA that is the output address of the translation.

**Executing the ATS1HW instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
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<td>0b100</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ATS1HW(R[t]);
    endif
elseif PSTATE.EL == EL2 then
    ATS1HW(R[t]);
elseif PSTATE.EL == EL3 then
    ATS1HW(R[t]);

BPIALL, Branch Predictor Invalidate All

The BPIALL characteristics are:

**Purpose**

Invalidate all entries from branch predictors.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to BPIALL are UNDEFINED.

In an implementation where the branch predictors are architecturally invisible, this instruction can execute as a NOP.

**Attributes**

BPIALL is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by \(<Rt>\) is ignored.

**Executing the BPIALL instruction**

The PE ignores the value of \(<Rt>\). Software does not have to write a value to this register before issuing this instruction.

When \(\text{HCR.FB} = 1\) at Non-secure EL1 this instruction executes as a BPIALLIS.

Accesses to this instruction use the following encodings:

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2>}
\]

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} = \text{EL0}\) then
    UNDEFINED;
elsif \(\text{PSTATE.EL} = \text{EL1}\) then
    if \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HSTR.EL2.T7} = '1'\) then
        \(\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)}\);
    elseif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HSTR.T7} = '1'\) then
        \(\text{AArch32.TakeHypTrapException(0x03)}\);
    elseif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HCR.FB} = '1'\) then
        \(\text{BPIALLIS()}\);
    else
        \(\text{BPIALL()}\);
    endif;
elsif \(\text{PSTATE.EL} = \text{EL2}\) then
    \(\text{BPIALL()}\);
elsif \(\text{PSTATE.EL} = \text{EL3}\) then
    \(\text{BPIALL()}\);
The BPIALLIS characteristics are:

**Purpose**

Invalidate all entries from branch predictors Inner Shareable.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to BPIALLIS are UNDEFINED.

In an implementation where the branch predictors are architecturally invisible, this instruction can execute as a NOP.

**Attributes**

BPIALLIS is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the BPIALLIS instruction**

The PE ignores the value of <Rt>. Software does not have to write a value to this register before issuing this instruction.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b011</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        BPIALLIS();
    end if
elsif PSTATE.EL == EL2 then
    BPIALLIS();
else
    BPIALLIS();
end if
BPIMVA, Branch Predictor Invalidate by VA

The BPIMVA characteristics are:

**Purpose**

Invalidate virtual address from branch predictors.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to BPIMVA are UNDEFINED.

In an implementation where the branch predictors are architecturally invisible, this instruction can execute as a NOP.

**Attributes**

BPIMVA is a 32-bit System instruction.

**Field descriptions**

The BPIMVA input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Virtual address to use</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Virtual address to use.

**Executing the BPIMVA instruction**

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} {coproc}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    BPIMVA(R[t]);
  endif
elsif PSTATE.EL == EL2 then
  BPIMVA(R[t]);
elsif PSTATE.EL == EL3 then
  BPIMVA(R[t]);
CCSIDR, Current Cache Size ID Register

The CCSIDR characteristics are:

**Purpose**

Provides information about the architecture of the currently selected cache.

When FEAT_CCIDX is implemented, this register is used in conjunction with CCSIDR2.

**Configuration**

AArch32 System register CCSIDR bits [31:0] are architecturally mapped to AArch64 System register CCSIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CCSIDR are UNDEFINED.

The implementation includes one CCSIDR for each cache that it can access. CSSELR and the Security state select which Cache Size ID Register is accessible.

**Attributes**

CCSIDR is a 32-bit register.

**Field descriptions**

The CCSIDR bit assignments are:

**When FEAT_CCIDX is implemented:**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Associativity, bits [23:3]**

(Associativity of cache) - 1, therefore a value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2.

**LineSize, bits [2:0]**

(Log₂(Number of bytes in cache line)) - 4. For example:

For a line length of 16 bytes: Log₂(16) = 4, LineSize entry = 0. This is the minimum line length.

**Note**

The parameters NumSets, Associativity, and LineSize in these registers define the architecturally visible parameters that are required for the cache maintenance by Set/Way instructions. They are not guaranteed to represent the actual microarchitectural features of a design. You cannot make any inference about the actual sizes of caches based on these parameters.
For a line length of 32 bytes: \( \log_2(32) = 5 \), LineSize entry = 1.

**Otherwise:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| UNKNOWN | NumSets | Associativity | LineSize |

**Note**

The parameters NumSets, Associativity, and LineSize in these registers define the architecturally visible parameters that are required for the cache maintenance by Set/Way instructions. They are not guaranteed to represent the actual microarchitectural features of a design. You cannot make any inference about the actual sizes of caches based on these parameters.

**Bits [31:28]**

Reserved, UNKNOWN.

**NumSets, bits [27:13]**

(Number of sets in cache) - 1, therefore a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

**Associativity, bits [12:3]**

(Associativity of cache) - 1, therefore a value of 0 indicates an associativity of 1. The associativity does not have to be a power of 2.

**LineSize, bits [2:0]**

\( \log_2(\text{Number of bytes in cache line}) \) - 4. For example:

For a line length of 16 bytes: \( \log_2(16) = 4 \), LineSize entry = 0. This is the minimum line length.

For a line length of 32 bytes: \( \log_2(32) = 5 \), LineSize entry = 1.

**Accessing the CCSIDR**

If CSSEL R Level is programmed to a cache level that is not implemented, then on a read of the CCSIDR the behavior is **CONSTRAINED UNPREDICTABLE**, and can be one of the following:

- The CCSIDR read is treated as NOP.
- The CCSIDR read is **UNDEFINED**.
- The CCSIDR read returns an **UNKNOWN** value.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \ <\text{coproc}>\, \{\#\}<\text{opc1}>\, \,<\text{Rt}>\, \,<\text{CRn}>\, \,<\text{CRm}>\{, \{\#\}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID4 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TID4 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        return CCSIDR;
    endif
else
    PSTATE.EL == EL2 then
        return CCSIDR;
    elsif PSTATE.EL == EL3 then
        return CCSIDR;
    endif
CCSIDR2, Current Cache Size ID Register 2

The CCSIDR2 characteristics are:

**Purpose**

When FEAT_CCIDX is implemented, in conjunction with CCSIDR, provides information about the architecture of the currently selected cache.

When FEAT_CCIDX is not implemented, this register is not implemented.

**Configuration**

AArch32 System register CCSIDR2 bits [31:0] are architecturally mapped to AArch64 System register CCSIDR2_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_CCIDX is implemented. Otherwise, direct accesses to CCSIDR2 are UNDEFINED.

The implementation includes one CCSIDR2 for each cache that it can access. CSSELR and the Security state select which Cache Size ID Register is accessible.

**Attributes**

CCSIDR2 is a 32-bit register.

**Field descriptions**

The CCSIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
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<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
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<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
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</tr>
<tr>
<td>NumSets</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**NumSets, bits [23:0]**

(Number of sets in cache) - 1, therefore a value of 0 indicates 1 set in the cache. The number of sets does not have to be a power of 2.

**Accessing the CCSIDR2**

If CSSELR. Level is programmed to a cache level that is not implemented, then on a read of the CCSIDR2 the behavior is CONSTRAINED UNPREDICTABLE, and can be one of the following:

- The CCSIDR2 read is treated as NOP.
- The CCSIDR2 read is UNDEFINED.
- The CCSIDR2 read returns an UNKNOWN value.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
</table>

Page 2095
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID4 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TID4 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return CCSIDR2;
    elsif PSTATE.EL == EL2 then
        return CCSIDR2;
    elsif PSTATE.EL == EL3 then
        return CCSIDR2;

The CFPRCTX characteristics are:

**Purpose**

Control Flow Prediction Restriction by Context applies to all Control Flow Prediction Resources that predict execution based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, control flow prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of prediction structures so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level and FEAT_SPECRES is implemented. Otherwise, direct accesses to CFPRCTX are UNDEFINED.

**Attributes**

CFPRCTX is a 32-bit System instruction.

**Field descriptions**

The CFPRCTX input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
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<th>13</th>
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<th>11</th>
<th>10</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>GVMID</td>
<td>NS</td>
<td>EL</td>
<td>VMID</td>
<td>RES0</td>
<td>GASID</td>
<td>ASID</td>
<td></td>
<td></td>
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<td></td>
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</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**GVMID, bit [27]**

Execution of this instruction applies to all VMIDs or a specified VMID.

<table>
<thead>
<tr>
<th>GVMID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified VMID for an EL0 or EL1 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all VMIDs for an EL0 or EL1 target execution context.</td>
</tr>
</tbody>
</table>
For target execution contexts other than EL0 or EL1, this field is RES0.

If the instruction is executed at EL0 or EL1, this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**NS, bit [26]**

Security State.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure state.</td>
</tr>
</tbody>
</table>

If the instruction is executed in Non-secure state, this field has an Effective value of 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1.</td>
</tr>
<tr>
<td>0b10</td>
<td>EL2.</td>
</tr>
</tbody>
</table>

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**VMID, bits [23:16]**

Only applies when bit[27] is 0 and the target execution context is either:

- EL1.
- EL0 when (HCR_EL2.E2H==0 or HCR_EL2.TGE==0) or EL2 is using AArch32 state.

Otherwise this field is RES0.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==0 or HCR_EL2.TGE==0 or ELUsingAArch32(EL2)), this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==1 and HCR_EL2.TGE==1 and !ELUsingAArch32(EL2)), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**Bits [15:9]**

Reserved, RES0.

**GASID, bit [8]**

Execution of this instruction applies to all ASIDs or a specified ASID.

<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0, this field is RES0.

If the instruction is executed at EL0, this field is treated as 0.
ASID, bits [7:0]

Only applies for an EL0 target execution context and when bit[8] is 0.

Otherwise, this field is RES0.

When the instruction is executed at EL0, this field is treated as the current ASID.

Executing the CFPRCTX instruction

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.EnRCTX == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && SCTLR_EL2.EnRCTX == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.NV == '1' then
        AArch64.SystemAccessTrap(EL2, 0x03);
    else
        CFPRCTX(R[t]);
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.NV == '1' then
            AArch64.SystemAccessTrap(EL2, 0x03);
        else
            CFPRCTX(R[t]);
    elsif PSTATE.EL == EL2 then
        CFPRCTX(R[t]);
    elsif PSTATE.EL == EL3 then
        CFPRCTX(R[t]);
```
The CLIDR characteristics are:

**Purpose**

Identifies the type of cache, or caches, that are implemented at each level and can be managed using the architected cache maintenance instructions that operate by set/way, up to a maximum of seven levels. Also identifies the Level of Coherence (LoC) and Level of Unification (LoU) for the cache hierarchy.

**Configuration**

AArch32 System register CLIDR bits [31:0] are architecturally mapped to AArch64 System register CLIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CLIDR are UNDEFINED.

**Attributes**

CLIDR is a 32-bit register:

**Field descriptions**

The CLIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ICB</td>
</tr>
<tr>
<td>30</td>
<td>LoUU</td>
</tr>
<tr>
<td>29</td>
<td>LoC</td>
</tr>
<tr>
<td>28</td>
<td>LoUIS</td>
</tr>
<tr>
<td>27</td>
<td>Ctype7</td>
</tr>
<tr>
<td>26</td>
<td>Ctype6</td>
</tr>
<tr>
<td>25</td>
<td>Ctype5</td>
</tr>
<tr>
<td>24</td>
<td>Ctype4</td>
</tr>
<tr>
<td>23</td>
<td>Ctype3</td>
</tr>
<tr>
<td>22</td>
<td>Ctype2</td>
</tr>
<tr>
<td>21</td>
<td>Ctype1</td>
</tr>
</tbody>
</table>

**ICB, bits [31:30]**

Inner cache boundary. This field indicates the boundary for caching Inner Cacheable memory regions.

The possible values are:

<table>
<thead>
<tr>
<th>ICB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not disclosed by this mechanism.</td>
</tr>
<tr>
<td>0b01</td>
<td>L1 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b10</td>
<td>L2 cache is the highest Inner Cacheable level.</td>
</tr>
<tr>
<td>0b11</td>
<td>L3 cache is the highest Inner Cacheable level.</td>
</tr>
</tbody>
</table>

**LoUU, bits [29:27]**

Level of Unification Uniprocessor for the cache hierarchy.

**Note**

When FEAT_S2FWB is implemented, the architecture requires that this field is zero so that no levels of data cache need to be cleaned in order to manage coherency with instruction fetches.

**LoC, bits [26:24]**

Level of Coherence for the cache hierarchy.
LoUIS, bits [23:21]

Level of Unification Inner Shareable for the cache hierarchy.

Note

When FEAT_S2FWB is implemented, the architecture requires that this field is zero so that no levels of data cache need to be cleaned in order to manage coherency with instruction fetches.

Ctype<n>, bits [3(n-1)+2:3(n-1)], for n = 7 to 1

Cache Type fields. Indicate the type of cache that is implemented and can be managed using the architected cache maintenance instructions that operate by set/way at each level, from Level 1 up to a maximum of seven levels of cache hierarchy. Possible values of each field are:

<table>
<thead>
<tr>
<th>Ctype&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>No cache.</td>
</tr>
<tr>
<td>0b001</td>
<td>Instruction cache only.</td>
</tr>
<tr>
<td>0b010</td>
<td>Data cache only.</td>
</tr>
<tr>
<td>0b011</td>
<td>Separate instruction and data caches.</td>
</tr>
<tr>
<td>0b100</td>
<td>Unified cache.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If software reads the Cache Type fields from Ctype1 upwards, once it has seen a value of 000, no caches that can be managed using the architected cache maintenance instructions that operate by set/way exist at further-out levels of the hierarchy. So, for example, if Ctype3 is the first Cache Type field with a value of 000, the values of Ctype4 to Ctype7 must be ignored.

**Accessing the CLIDR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b001</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & ELUsingAArch32(EL2) & HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR_EL2.TID2 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR_EL2.TID4 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return CLIDR;
  end if;
elsif PSTATE.EL == EL2 then
  return CLIDR;
elsif PSTATE.EL == EL3 then
  return CLIDR;
CNTFRQ, Counter-timer Frequency register

The CNTFRQ characteristics are:

**Purpose**

This register is provided so that software can discover the frequency of the system counter. It must be programmed with this value as part of system initialization. The value of the register is not interpreted by hardware.

**Configuration**

AArch32 System register CNTFRQ bits [31:0] are architecturally mapped to AArch64 System register CNTFRQ_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTFRQ are UNDEFINED.

**Attributes**

CNTFRQ is a 32-bit register.

**Field descriptions**

The CNTFRQ bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Clock frequency</td>
</tr>
</tbody>
</table>

Bits [31:0]

Clock frequency. Indicates the system counter clock frequency, in Hz.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTFRQ**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') &&
    CNTKCTL_EL1.<EL0PCTEN,EL0VCTEN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elseif ELUsingAArch32(EL1) && CNTKCTL.PL0PCTEN == '0' && CNTKCTL.PL0VCTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' &&
    CNTKCTL_EL2.<EL0PCTEN,EL0VCTEN> == '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    return CNTFRQ;
  elsif PSTATE.EL == EL1 then
    return CNTFRQ;
  elsif PSTATE.EL == EL2 then
    return CNTFRQ;
  elsif PSTATE.EL == EL3 then
    return CNTFRQ;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if IsHighestEL(PSTATE.EL) then
  CNTFRQ = R[t];
else
  UNDEFINED;
The CNTHCTL characteristics are:

**Purpose**

Controls the generation of an event stream from the physical counter, and access from Non-secure EL1 modes to the physical counter and the Non-secure EL1 physical timer.

**Configuration**

AArch32 System register CNTHCTL bits [31:0] are architecturally mapped to AArch64 System register CNTHCTL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTHCTL are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

CNTHCTL is a 32-bit register.

**Field descriptions**

The CNTHCTL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | EVNTIS | RES0 | EVNTI | EVNTDIR | EVNTEN | PL1PCEN | PL1PCTEN |

**Bits [31:18]**

Reserved, RES0.

**EVNTIS, bit [17]**

**When FEAT_ECV is implemented:**

Controls the scale of the generation of the event stream.

<table>
<thead>
<tr>
<th>EVNTIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CNTHCTL.EVNTI field applies to CNTPCT[15:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>The CNTHCTL.EVNTI field applies to CNTPCT[23:8].</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bits [16:8]**

Reserved, RES0.
**EVNTI, bits [7:4]**

Selects which bit of the counter register `CNTPCT` is the trigger for the event stream generated from that counter, when that stream is enabled.

If FEAT_ECV is implemented, and CNTHCTL.EVNTIS is 1, this field selects a trigger bit in the range 8 to 23 of the counter register `CNTPCT` is the trigger.

Otherwise, this field selects a trigger bit in the range 0 to 15 of the counter register.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTDIR, bit [3]**

Controls which transition of the counter register `CNTPCT` trigger bit, defined by EVNTI, generates an event when the event stream is enabled:

<table>
<thead>
<tr>
<th>EVNTDIR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A 0 to 1 transition of the trigger bit triggers an event.</td>
</tr>
<tr>
<td>0b1</td>
<td>A 1 to 0 transition of the trigger bit triggers an event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTEN, bit [2]**

Enables the generation of an event stream from the counter register `CNTPCT`:

<table>
<thead>
<tr>
<th>EVNTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables the event stream.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables the event stream.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PL1PCEN, bit [1]**

Traps Non-secure EL0 and EL1 accesses to the physical timer registers to Hyp mode.

<table>
<thead>
<tr>
<th>PL1PCEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL0 and EL1 accesses to the <code>CNTP_CTL</code>, <code>CNTP_CVAL</code>, and <code>CNTP_TVAL</code> are trapped to Hyp mode, unless the it is trapped by <code>CNTKCTL.PL0PTEN</code>.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PL1PCTEN, bit [0]**

Traps Non-secure EL0 and EL1 accesses to the physical counter register to Hyp mode.

<table>
<thead>
<tr>
<th>PL1PCTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL0 and EL1 accesses to the <code>CNTPCT</code> are trapped to Hyp mode, unless it is trapped by <code>CNTKCTL.PL0PCTEN</code>.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and EL2 is not implemented, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Accessing the CNTHCTL

Accesses to this register use the following encodings:

\[
\text{MRC}{\langle c \rangle}{\langle q \rangle} \langle \text{coproc} \rangle, \{\#\} \langle \text{opc1} \rangle, \langle \text{Rt} \rangle, \langle \text{CRn} \rangle, \langle \text{CRm} \rangle, \{\#\} \langle \text{opc2} \rangle
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then UNDEFINED;
elsif PSTATE.EL == EL1 then UNDEFINED;
elsif PSTATE.EL == EL2 then return CNTHCTL;
elsif PSTATE.EL == EL3 then return CNTHCTL;

\[
\text{MCR}{\langle c \rangle}{\langle q \rangle} \langle \text{coproc} \rangle, \{\#\} \langle \text{opc1} \rangle, \langle \text{Rt} \rangle, \langle \text{CRn} \rangle, \langle \text{CRm} \rangle, \{\#\} \langle \text{opc2} \rangle
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then UNDEFINED;
elsif PSTATE.EL == EL1 then UNDEFINED;
elsif PSTATE.EL == EL2 then CNTHCTL = R[t];
elsif PSTATE.EL == EL3 then CNTHCTL = R[t];
The CNTHP_CTL characteristics are:

**Purpose**

Control register for the Hyp mode physical timer.

**Configuration**

AArch32 System register CNTHP_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTHP_CTL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTHP_CTL are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_CTL is a 32-bit register.

**Field descriptions**

The CNTHP_CTL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 | ISTATUS | IMASK | ENABLE |

**Bits [31:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>
For more information, see the description of the ISTATUS bit.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTHP_TVAL** continues to count down.

---

**Note**

Disabling the output signal might be a power-saving option.

---

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### Accessing the CNTHP_CTL

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTHP_CTL;
elsif PSTATE.EL == EL3 then
    return CNTHP_CTL;
```

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTHP_CTL = R[t];
elsif PSTATE.EL == EL3 then
    CNTHP_CTL = R[t];
```

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif EL2Enabled() && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        endif
    endif
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccess Trap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_CTL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CTL_EL2;
    else
        return CNTP_CTL;
    endif
    elsif PSTATE.EL == EL1 then
        if !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTTHCTL_EL2.EL1PCEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTTHCTL_EL2.EL0PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTTHCTL.PL1PCEN == '0' then
            AArch32.TakeHypTrapException(0x03);
        elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
            return CNTP_CTL_NS;
        else
            return CNTP_CTL;
        endif
    elsif PSTATE.EL == EL2 then
        if !ELUsingAArch32(EL3) && SCR.NS == '0' then
            return CNTP_CTL_S;
        elseif SCR.NS == '0' then
            return CNTP_CTL_NS;
        else
            return CNTP_CTL_NS;
        endif
   侧结构性的处理器。

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

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<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
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</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif EL2Enabled() && CNTKCTL.PL0PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
  AArch32.TakeHypTrapException(0x00);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FeAT SEL2) then
  CNTHPS_CTL_EL2 = R[t];
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
  CNTHP_CTL_EL2 = R[t];
else
  CNTP_CTL = R[t];
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    CNTP_CTL_NS = R[t];
  else
    CNTP_CTL = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    CNTP_CTL_NS = R[t];
  else
    CNTP_CTL = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    CNTP_CTL_S = R[t];
  else
    CNTP_CTL_NS = R[t];
else
  CNTP_CTL = R[t];
The CNTHP_CVAL characteristics are:

**Purpose**

Holds the compare value for the Hyp mode physical timer.

**Configuration**

AArch32 System register CNTHP_CVAL bits [63:0] are architecturally mapped to AArch64 System register CNTHP_CVAL_EL2[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTHP_CVAL are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_CVAL is a 64-bit register.

**Field descriptions**

The CNTHP_CVAL bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CompareValue |
| CompareValue |

**CompareValue, bits [63:0]**

Holds the EL2 physical timer CompareValue.

When CNTPCT.ENABLE is 1, the timer condition is met when (CNTPCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHP_CTL.ISTATUS is set to 1.
- If CNTHP_CTL.IMASK is 0, an interrupt is generated.

When CNTHP_CTL.ENABLE is 0, the timer condition is not met, but CNTPCT continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHP_CVAL**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  return CNTHP_CVAL;
elsif PSTATE.EL == EL3 then
  return CNTHP_CVAL;

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  CNTHP_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
  CNTHP_CVAL = R[t2]:R[t];

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  CNTHP_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
  CNTHP_CVAL = R[t2]:R[t];
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
        endif
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        endif
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_CVAL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CVAL_EL2;
    else
        return CNTP_CVAL;
    endif
endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return CNTP_CVAL_NS;
    else
        return CNTP_CVAL;
    endif
endif
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return CNTP_CVAL_NS;
    else
        return CNTP_CVAL;
    endif
endif
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return CNTP_CVAL_S;
    else
        return CNTP_CVAL_NS;
    endif
endif
MCRR{<c>}{<q>}{<coproc>}, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    endif
  endif
else
  if EL2Enabled() && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
      else
        AArch32.TakeHypTrapException(0x00);
      endif
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    endif
  endif
else
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL1PCEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.E2H == '0' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.E2H == '1' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    elseif EL2Enabled() && SCR_EL3.NS == '0' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    elseif EL2Enabled() && SCR_EL3.NS == '1' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    else
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    endif
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    else
      CNTHPS_CVAL_EL2 = R[t2]:R[t];
    endif
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' then
      AArch32.TakeHypTrapException(0x04);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' then
      AArch32.TakeHypTrapException(0x04);
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_CVAL_NS = R[t2]:R[t];
    else
      CNTP_CVAL_NS = R[t2]:R[t];
    endif
  elseif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.E1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.E1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
      AArch32.TakeHypTrapException(0x04);
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_CVAL_NS = R[t2]:R[t];
    else
      CNTP_CVAL_NS = R[t2]:R[t];
    endif
  elseif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_CVAL_NS = R[t2]:R[t];
    else
      CNTP_CVAL_NS = R[t2]:R[t];
    endif
  elseif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
      CNTP_CVAL_NS = R[t2]:R[t];
    else
      CNTP_CVAL_NS = R[t2]:R[t];
    endif
  endif
endif
The CNTHP_TVAL characteristics are:

**Purpose**

Holds the timer value for the Hyp mode physical timer.

**Configuration**

AArch32 System register CNTHP_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTHP_TVAL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTHP_TVAL are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

CNTHP_TVAL is a 32-bit register.

**Field descriptions**

The CNTHP_TVAL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| TimerValue |

**TimerValue, bits [31:0]**

The TimerValue view of the EL2 physical timer.

On a read of this register:

- If CNTHP_CTL.ENABLE is 0, the value returned is UNKNOWN.
- If CNTHP_CTL.ENABLE is 1, the value returned is (CNTHP_CVAL - CNTPCT).

On a write of this register, CNTHP_CVAL is set to (CNTPCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHP_CTL.ENABLE is 1, the timer condition is met when (CNTPCT - CNTHP_CVAL) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHP_CTL.ISTATUS is set to 1.
- If CNTHP_CTL.IMASK is 0, an interrupt is generated.

When CNTHP_CTL.ENABLE is 0, the timer condition is not met, but CNTPCT continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHP_TVAL**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  return CNTHP_TVAL;
elsif PSTATE.EL == EL3 then
  return CNTHP_TVAL;
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        end if;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_TVAL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_TVAL_EL2;
    else
        return CNTP_TVAL;
    end if;
else
    return CNTP_TVAL;
end if;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
        return CNTHPS_TVAL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_TVAL_EL2;
    else
        return CNTP_TVAL;
    end if;
else
    return CNTP_TVAL;
end if;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return CNTP_TVAL_NS;
    else
        return CNTP_TVAL;
    end if;
else
    return CNTP_TVAL;
end if;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return CNTP_TVAL_S;
    else
        return CNTP_TVAL_NS;
    end if;
else
    return CNTP_TVAL_NS;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif !ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif !EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elsif !ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      CNTP_TVAL = R[t];
  elsif PSTATE.EL == EL1 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif !ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      CNTP_TVAL = R[t];
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_TVAL_NS = R[t];
    else
      CNTP_TVAL = R[t];
  elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
      CNTP_TVAL_S = R[t];
    else
      CNTP_TVAL_NS = R[t];
  else
    CNTP_TVAL = R[t];

CNTHPS_CTL, Counter-timer Secure Physical Timer Control Register (EL2)

The CNTHPS_CTL characteristics are:

**Purpose**

Provides AArch32 access from EL0 to the Secure EL2 physical timer.

**Configuration**

AArch32 System register CNTHPS_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTHPS_CTL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_CTL are **UNDEFINED**.

**Attributes**

CNTHPS_CTL is a 32-bit register.

**Field descriptions**

The CNTHPS_CTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>ISTATUS</td>
</tr>
<tr>
<td>29</td>
<td>IMASK</td>
</tr>
<tr>
<td>28</td>
<td>ENABLE</td>
</tr>
<tr>
<td>27</td>
<td></td>
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<td>26</td>
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<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the CNTHPS_CTL.ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the CNTHPS_CTL.ENABLE bit is 0, the ISTATUS field is **UNKNOWN**.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from **CNTHPS_TVAL_EL2** continues to count down.

---

**Note**

Disabling the output signal might be a power-saving option.

---

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTHPS_CTL**

This register is accessed using the encoding for **CNTP_CTL**.

Accesses to this register use the following encodings:

\[ \text{MRC} \{<c>\} \{<q>\} \text{ coproc, } \{#\text{ opc1}\}, \text{ <Rt>, <CRn>, <CRm}\{, \{#\text{ opc2}\}} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        endif
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        endif
    elsif !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHPS_CTL_EL2;
    elseif !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CTL_EL2;
    else
        return CNTP_CTL;
    endif
elsif PSTATE_EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x03);
    elseif !ELUsingAArch32(EL3) && ELUsingAArch32(EL3) then
        return CNTP_CTL_NS;
    else
        return CNTP_CTL;
    endif
elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return CNTP_CTL_NS;
    else
        return CNTP_CTL;
    endif
elsif PSTATE_EL == EL3 then
    if SCR.NS == '0' then
        return CNTP_CTL_S;
    else
        return CNTP_CTL_NS;
    endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.TGE == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    else
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
elsif EL2Enabled() && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
    else
        UNDEFINED;
    end
elsif EL2Enabled() && CNTKCTL.PL1PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        CNTP_CTL = R[t];
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    else
        CNTP_CTL = R[t];
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        CNTP_CTL_NS = R[t];
    else
        CNTP_CTL = R[t];
    end
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        CNTP_CTL_S = R[t];
    else
        CNTP_CTL_NS = R[t];
    end
end
The CNTHPS_CVAL characteristics are:

**Purpose**

Provides AArch32 access from EL0 to the compare value for the Secure EL2 physical timer.

**Configuration**

AArch32 System register CNTHPS_CVAL bits [63:0] are architecturally mapped to AArch64 System register CNTHPS_CVAL_EL2[63:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_CVAL are UNDEFINED.

**Attributes**

CNTHPS_CVAL is a 64-bit register.

**Field descriptions**

The CNTHPS_CVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CompareValue</td>
</tr>
<tr>
<td>62</td>
<td>CompareValue</td>
</tr>
<tr>
<td>61</td>
<td>CompareValue</td>
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<tr>
<td>60</td>
<td>CompareValue</td>
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<td>59</td>
<td>CompareValue</td>
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<tr>
<td>3</td>
<td>CompareValue</td>
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<tr>
<td>2</td>
<td>CompareValue</td>
</tr>
<tr>
<td>1</td>
<td>CompareValue</td>
</tr>
<tr>
<td>0</td>
<td>CompareValue</td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL2 physical timer CompareValue.

When CNTHPS_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHPS_CTL_EL2.ISTATUS is set to 1.
- If CNTHPS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHPS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTHPS_CVAL**

This register is accessed using the encoding for CNTP_CVAL.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    endif
else
    if !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif ELUsingAArch32(EL2) && CNTKCTL.PL0PTEN == '0' then
        AArch32.TakeHypTrapException(0x00);
    else
        UNDEFINED;
    endif
endif
else
    if EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch32.TakeHypTrapException(0x04);
    else
        UNDEFINED;
    endif
endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch32.TakeHypTrapException(0x04);
        endif
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && ELUsingAArch32(EL3) then
            return CNTP_CVAL_NS;
        else
            return CNTP_CVAL;
        endif
    elsif PSTATE.EL == EL3 then
        if SCR.NS == '0' then
            return CNTP_CVAL_S;
        else
            return CNTP_CVAL_NS;
        endif
    endif
else
    if SCR.NS == '0' then
        return CNTP_CVAL_S;
    else
        return CNTP_CVAL_NS;
    endif
endif
MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.TGE == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
    else
        CNTP_CVAL = R[t2]:R[t];
    end
else
    CNTHPS_CVAL = R[t2]:R[t];
end
elsif PSTATE.EL == EL1 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        CNTP_CVAL_NS = R[t2]:R[t];
    else
        CNTP_CVAL = R[t2]:R[t];
    end
elsif PSTATE.EL == EL2 then
    if SCR.NS == '0' then
        CNTP_CVAL_S = R[t2]:R[t];
    else
        CNTP_CVAL = R[t2]:R[t];
    end
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        CNTP_CVAL_NS = R[t2]:R[t];
    else
        CNTP_CVAL = R[t2]:R[t];
end

30/09/2020 15:07; ccead0cb9f089f9cced50268e82aee9c7e1047211
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CNTHPS_TVAL, Counter-timer Secure Physical Timer TimerValue Register (EL2)

The CNTHPS_TVAL characteristics are:

**Purpose**

Provides AArch32 access from EL0 to the timer value for the Secure EL2 physical timer.

**Configuration**

AArch32 System register CNTHPS_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTHPS_TVAL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHPS_TVAL are **UNDEFINED**.

**Attributes**

CNTHPS_TVAL is a 32-bit register.

**Field descriptions**

The CNTHPS_TVAL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TimerValue |

**TimerValue, bits [31:0]**

The TimerValue view of the EL2 physical timer.

On a read of this register:

- If CNTHPS_CTL_EL2.ENABLE is 0, the value returned is **UNKNOWN**.
- If CNTHPS_CTL_EL2.ENABLE is 1, the value returned is (CNTHPS_CVAL_EL2 - CNTPCT_EL0).

On a write of this register, CNTHPS_CVAL_EL2 is set to (CNTPCT_EL0 + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHPS_CTL_EL2.ENABLE is 1, the timer condition is met when (CNTPCT_EL0 - CNTHPS_CVAL_EL2) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHPS_CTL_EL2.ISTATUS is set to 1.
- If CNTHPS_CTL_EL2.IMASK is 0, an interrupt is generated.

When CNTHPS_CTL_EL2.ENABLE is 0, the timer condition is not met, but CNTPCT_EL0 continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTHPS_TVAL**

This register is accessed using the encoding for CNTP_TVAL.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  endif
elseif EL2Enabled() && HCR_EL2.TGE == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else
  UNDEFINED;
endif

if PSTATE.EL == EL1 then
  if !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  endif
elseif EL2Enabled() && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL0PTEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else
  UNDEFINED;
endif

if PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CNTP_TVAL_NS;
  else
    return CNTP_TVAL;
  endif
else
  return CNTP_TVAL_NS;
endif

if SCR.NS == '0' then
  return CNTP_TVAL_S;
else
  return CNTP_TVAL_NS;
endif
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.E2H,TGE == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch32.TakeHypTrapException(0x00);
  elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '10' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && SCR_EL3.NS == '0' && IsFeatureImplemented(Feat_SEL2) then
    CNTHPS_TVAL_EL2 = R[t];
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
    CNTHPS_TVAL_EL2 = R[t];
  else
    CNTNPS_TVAL = R[t];
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
      AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_TVAL_NS = R[t];
    else
      CNTP_TVAL = R[t];
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      CNTP_TVAL_NS = R[t];
    else
      CNTP_TVAL = R[t];
  elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
      CNTP_TVAL_S = R[t];
    else
      CNTP_TVAL_NS = R[t];

CNTHV_CTL, Counter-timer Virtual Timer Control register (EL2)

The CNTHV_CTL characteristics are:

Purpose

Provides AArch32 access to the control register for the EL2 virtual timer.

Configuration

AArch32 System register CNTHV_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTHV_CTL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_CTL are UNDEFINED.

Attributes

CNTHV_CTL is a 32-bit register.

Field descriptions

The CNTHV_CTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>ISTATUS</td>
</tr>
<tr>
<td>29</td>
<td>IMASK</td>
</tr>
<tr>
<td>28</td>
<td>ENABLE</td>
</tr>
</tbody>
</table>

Bits [31:3]

Reserved, RES0.

ISTATUS, bit [2]

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

IMASK, bit [1]

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
ENABLE, bit [0]

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from `CNTHV_TVAL` continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

---

Accessing the CNTHV_CTL

This register is accessed using the encoding for `CNTV_CTL`.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b000</td>
<td>0b110</td>
<td>0b001</td>
<td></td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif EL2Enabled() && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && IsFeatureImplemented(FEAT_SEL2) then
      return CNTHV_CTL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
      return CNTHV_CTL_EL2;
    else
      return CNTHV_CTL_EL2;
  else
    return CNTV_CTL;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1TVT == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      return CNTV_CTL;
  elsif PSTATE.EL == EL2 then
    return CNTV_CTL;
  elsif PSTATE.EL == EL3 then
    return CNTV_CTL;
```
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      UNDEFINED;
  elsif EL2Enabled() && CNTKCTL.PL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x00);
  else
    UNDEFINED;
  end if;
else
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && SCR_EL3.NS == '1' then
    CNTHV_CTL_EL2 = R[t];
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
    CNTHV_CTL_EL2 = R[t];
  else
    CNTV_CTL = R[t];
end if;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1VT = '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    CNTV_CTL = R[t];
end if;
elsif PSTATE.EL == EL2 then
  CNTV_CTL = R[t];
elsif PSTATE.EL == EL3 then
  CNTV_CTL = R[t];
CNTHV_CVAL, Counter-timer Virtual Timer CompareValue register (EL2)

The CNTHV_CVAL characteristics are:

**Purpose**

Provides AArch32 access to the compare value for the EL2 virtual timer.

**Configuration**

AArch32 System register CNTHV_CVAL bits [63:0] are architecturally mapped to AArch64 System register `CNTHV_CVAL_EL2[63:0]`.

This register is present only when FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_CVAL are **UNDEFINED**.

**Attributes**

CNTHV_CVAL is a 64-bit register.

**Field descriptions**

The CNTHV_CVAL bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
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<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
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<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
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<td>CompareValue</td>
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<td></td>
<td>CompareValue</td>
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<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
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<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL2 virtual timer CompareValue.

When `CNTHV_CTL_ENABLE` is 1, the timer condition is met when `(CNTVCT - CompareValue)` is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- `CNTHV_CTL.ISTATUS` is set to 1.
- If `CNTHV_CTL.IMASK` is 0, an interrupt is generated.

When `CNTHV_CTL_ENABLE` is 0, the timer condition is not met, but `CNTVCT` continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are `RES0`.

The value of this field is treated as zero-extended in all counter calculations.

**Accessing the CNTHV_CVAL**

Accesses to this register use the following encodings:

```
MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      AArch32.TakeHypTrapException(0x00);
  elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTKCTL_EL2.EL1VTEN == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3_NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    return CNTHV_CVAL_EL2;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3_NS == '1' then
    return CNTHV_CVAL_EL2;
  else
    return CNTV_CVAL;
  endif
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1VTEN == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    return CNTV_CVAL;
  endif
elseif PSTATE.EL == EL2 then
  return CNTV_CVAL;
elseif PSTATE.EL == EL3 then
  return CNTV_CVAL;
endif

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && SCR_EL3.NS == '1' then
        AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        CNTHV_CS_CVAL_EL2 = R[t2]:R[t];
    else
        CNTV_CVAL = R[t2]:R[t];
    endif
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1TVT == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
        CNTV_CVAL = R[t2]:R[t];
    endif
elsif PSTATE.EL == EL2 then
    CNTV_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
    CNTV_CVAL = R[t2]:R[t];

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The CNTHV_TVAL characteristics are:

### Purpose

Provides AArch32 access to the timer value for the EL2 virtual timer.

### Configuration

AArch32 System register CNTHV_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTHV_TVAL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_VHE is implemented. Otherwise, direct accesses to CNTHV_TVAL are **UNDEFINED**.

### Attributes

CNTHV_TVAL is a 32-bit register.

### Field descriptions

The CNTHV_TVAL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TimerValue |

### TimerValue, bits [31:0]

The TimerValue view of the EL2 virtual timer.

On a read of this register:

- If **CNTHV_CTL**.ENABLE is 0, the value returned is **UNKNOWN**.
- If **CNTHV_CTL**.ENABLE is 1, the value returned is (**CNTHV_CVAL** - **CNTVCT**).

On a write of this register, **CNTHV_CVAL** is set to (**CNTVCT** + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When **CNTHV_CTL**.ENABLE is 1, the timer condition is met when (**CNTVCT** - **CNTHV_CVAL**) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- **CNTHV_CTL**.ISTATUS is set to 1.
- If **CNTHV_CTL**.IMASK is 0, an interrupt is generated.

When **CNTHV_CTL**.ENABLE is 0, the timer condition is not met, but **CNTVCT** continues to count, so the TimerValue view appears to continue to count down.

### Accessing the CNTHV_TVAL

This register is accessed using the encoding for **CNTV_TVAL**.

Accesses to this register use the following encodings:
if `PSTATE.EL == EL0` then
  if `!ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0'` then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif `EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1'` then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif `EL2Enabled() && ELUsingAArch32(EL2) && HCR.EL2.TGE == '1'` then
    AArch32.TakeHypTrapException(0x00);
  else
    UNDEFINED;
  elsif `EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0'` then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    return CNTHV_TVAL_EL2;
  elsif `EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTKCTL_EL2.EL1VTEN == '1'` then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif `EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0'` then
    return CNTHVS_TVAL_EL2;
  elsif `EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1'` then
    return CNTHV_TVAL_EL2;
  else
    return CNTV_TVAL;
  elsif `PSTATE.EL == EL1` then
    if `!ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1VTEN == '1'` then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      return CNTV_TVAL;
    elsif `PSTATE.EL == EL2` then
      return CNTV_TVAL;
    elsif `PSTATE.EL == EL3` then
      return CNTV_TVAL;
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS.TVAL_EL2 = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        CNTHV_TVAL_EL2 = R[t];
    else
        CNTV_TVAL = R[t];
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1VTEN == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        CNTV_TVAL = R[t];
    end
elsif PSTATE.EL == EL2 then
    CNTV_TVAL = R[t];
elsif PSTATE.EL == EL3 then
    CNTV_TVAL = R[t];
CNTHVS_CTL, Counter-timer Secure Virtual Timer Control Register (EL2)

The CNTHVS_CTL characteristics are:

Purpose

Provides AArch32 access from EL0 to the Secure EL2 virtual timer.

Configuration

AArch32 System register CNTHVS_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTHVS_CTL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_CTL are undefined.

Attributes

CNTHVS_CTL is a 32-bit register.

Field descriptions

The CNTHVS_CTL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | ISTATUS | IMASK | ENABLE |

Bits [31:3]

Reserved, RES0.

ISTATUS, bit [2]

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is unknown.

This bit is read-only.

IMASK, bit [1]

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from \texttt{CNTHVS_TVAL} continues to count down.

---

**Note**

Disabling the output signal might be a power-saving option.

---

**Accessing the CNTHVS_CTL**

This register is accessed using the encoding for \texttt{CNTV_CTL}.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \text{<coproc>}, \{#\langle opc1 \rangle\}, \{<Rt>\}, \{<CRn>\}, \{<CRm>\}\{, \{#\langle opc2 \rangle\}\}
\]

<table>
<thead>
<tr>
<th>\text{coproc}</th>
<th>\text{opc1}</th>
<th>\text{CRn}</th>
<th>\text{CRm}</th>
<th>\text{opc2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  endif
else
  return CNTHVS_CTL_EL2;
endif

if PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL1VTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    endif
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      return CNTHVS_CTL_EL2;
    else
      return CNTHVS_CTL_EL2;
    endif
  endif
else
  return CNTV_CTL;
endif

if PSTATE.EL == EL2 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      return CNTV_CTL;
    endif
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      return CNTV_CTL;
    endif
  endif
else
  return CNTV_CTL;
endif
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            UNDEFINED;
    elsif EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && SCR_EL3.NS == '0' then
        CNTHVS_CTL_EL2 = R[t];
    elsif EL2Enabled() && SCR_EL3.NS == '1' then
        CNTHV_CTL_EL2 = R[t];
    else
        CNTV_CTL = R[t];
    elsif PSTATE.EL == EL1 then
        if !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            CNTV_CTL = R[t];
    elsif PSTATE.EL == EL2 then
        CNTV_CTL = R[t];
    elsif PSTATE.EL == EL3 then
        CNTV_CTL = R[t];
The CNTHVS_CVAL characteristics are:

**Purpose**

Provides AArch32 access to the compare value for the Secure EL2 virtual timer.

**Configuration**

AArch32 System register CNTHVS_CVAL bits [63:0] are architecturally mapped to AArch64 System register CNTHVS_CVAL_EL2[63:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_CVAL are UNDEFINED.

**Attributes**

CNTHVS_CVAL is a 64-bit register.

**Field descriptions**

The CNTHVS_CVAL bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| CompareValue | CompareValue |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |

**CompareValue, bits [63:0]**

Holds the EL2 virtual timer CompareValue.

When CNTHVS_CTL_ENABLE is 1, the timer condition is met when (CNTVCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTHVS_CTL_ISTATUS is set to 1.
- If CNTHVS_CTL.IMASK is 0, an interrupt is generated.

When CNTHVS_CTL_ENABLE is 0, the timer condition is not met, but CNTVCT continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

**Accessing the CNTHVS_CVAL**

This register is accessed using the encoding for CNTV_CVAL.

Accesses to this register use the following encodings:

```
MRRC{<c>}{<q>} <coproc>, {#<opc1>, <Rt>, <Rt2>, <CRm>
```

```markdown
<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
        endif
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        endif
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHV_CVAL_EL2 == '1' then
        return CNTHV_CVAL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        return CNTHVS_CVAL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHV_CVAL_EL2;
    else
        return CNTV_CVAL;
    endif
elsif PSTATE.EL == EL1 then
    if !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHV_CVAL_EL2 == '1' then
        return CNTHV_CVAL_EL2;
    else
        return CNTV_CVAL;
    endif
elsif PSTATE.EL == EL2 then
    return CNTV_CVAL;
elsif PSTATE.EL == EL3 then
    return CNTV_CVAL;
else
    return CNTV_CVAL;
endif

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VTEN == '1' then
            CNTV_CVAL = R[t2]:R[t];
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(Feat_SEL2) then
            CNTHVS_CVAL_EL2 = R[t2]:R[t];
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            CNTHV_CVAL_EL2 = R[t2]:R[t];
        else
            CNTV_CVAL = R[t2]:R[t];
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && CNTKCTL_EL2.EL1VTEN == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL2 then
        CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL3 then
        CNTV_CVAL = R[t2]:R[t];
The CNTHVS_TVAL characteristics are:

**Purpose**

Provides AArch32 access to the timer value for the Secure EL2 virtual timer.

**Configuration**

AArch32 System register CNTHVS_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTHVS_TVAL_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_SEL2 is implemented. Otherwise, direct accesses to CNTHVS_TVAL are UNDEFINED.

**Attributes**

CNTHVS_TVAL is a 32-bit register.

**Field descriptions**

The CNTHVS_TVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
</tr>
<tr>
<td>29</td>
<td>28</td>
</tr>
<tr>
<td>27</td>
<td>26</td>
</tr>
<tr>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td>21</td>
<td>20</td>
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<tr>
<td>19</td>
<td>18</td>
</tr>
<tr>
<td>17</td>
<td>16</td>
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<tr>
<td>15</td>
<td>14</td>
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<tr>
<td>13</td>
<td>12</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
</tr>
<tr>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**TimerValue, bits [31:0]**

The TimerValue view of the EL2 virtual timer.

On a read of this register:

- If CNTHVS_CTL.ENABLE is 0, the value returned is UNKNOWN.
- If CNTHVS_CTL.ENABLE is 1, the value returned is (CNTHVS_CVAL - CNTVCT).

On a write of this register, CNTHVS_CVAL is set to (CNTVCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTHVS_CTL.ENABLE is 1, the timer condition is met when (CNTVCT - CNTHVS_CVAL) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTHVS_CTL.ISTATUS is set to 1.
- If CNTHVS_CTL.IMASK is 0, an interrupt is generated.

When CNTHVS_CTL.ENABLE is 0, the timer condition is not met, but CNTVCT continues to count, so the TimerValue view appears to continue to count down.

**Accessing the CNTHVS_TVAL**

This register is accessed using the encoding for CNTV_TVAL.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  endif
else
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  endif
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    endif
  elseif PSTATE.EL == EL2 then
    return CNTV_TVAL;
  elseif PSTATE.EL == EL3 then
    return CNTV_TVAL;
  endif
endif

if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  endif
else
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  endif
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      UNDEFINED;
    endif
  elseif PSTATE.EL == EL2 then
    return CNTV_TVAL;
  elseif PSTATE.EL == EL3 then
    return CNTV_TVAL;
  endif
endif

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
   elsif ELUsingAArch32(EL1) && CNTHCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS_TVAL_EL2 = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
        CNTHV_TVAL_EL2 = R[t];
    else
        CNTV_TVAL = R[t];
elsif PSTATE.EL == EL1 then
    if !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        CNTV_TVAL = R[t];
elsif PSTATE.EL == EL2 then
    CNTV_TVAL = R[t];
elsif PSTATE.EL == EL3 then
    CNTV_TVAL = R[t];
CNTKCTL, Counter-timer Kernel Control register

The CNTKCTL characteristics are:

**Purpose**

Controls the generation of an event stream from the virtual counter, and access from EL0 modes to the physical counter, virtual counter, EL1 physical timers, and the virtual timer.

**Configuration**

AArch32 System register CNTKCTL bits [31:0] are architecturally mapped to AArch64 System register CNTKCTL_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTKCTL are UNDEFINED.

**Attributes**

CNTKCTL is a 32-bit register.

**Field descriptions**

The CNTKCTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>RESERVED</td>
</tr>
<tr>
<td>29</td>
<td>EVNTIS</td>
</tr>
<tr>
<td>28</td>
<td>RESERVED</td>
</tr>
<tr>
<td>27</td>
<td>PL0PTEN</td>
</tr>
<tr>
<td>26</td>
<td>RESERVED</td>
</tr>
<tr>
<td>25</td>
<td>PL0VTEN</td>
</tr>
<tr>
<td>24</td>
<td>EVNTI</td>
</tr>
<tr>
<td>23</td>
<td>RESERVED</td>
</tr>
<tr>
<td>22</td>
<td>EVNTDIR</td>
</tr>
<tr>
<td>21</td>
<td>EVNTEN</td>
</tr>
<tr>
<td>20</td>
<td>RESERVED</td>
</tr>
<tr>
<td>19</td>
<td>PL0VCTEN</td>
</tr>
<tr>
<td>18</td>
<td>RESERVED</td>
</tr>
<tr>
<td>17</td>
<td>PL0PCTEN</td>
</tr>
<tr>
<td>16</td>
<td>RESERVED</td>
</tr>
<tr>
<td>15</td>
<td>RESERVED</td>
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<td>14</td>
<td>RESERVED</td>
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<td>RESERVED</td>
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<tr>
<td>3</td>
<td>RESERVED</td>
</tr>
<tr>
<td>2</td>
<td>RESERVED</td>
</tr>
<tr>
<td>1</td>
<td>RESERVED</td>
</tr>
<tr>
<td>0</td>
<td>RESERVED</td>
</tr>
</tbody>
</table>

**Bits [31:18]**

Reserved, RES0.

**EVNTIS, bit [17]**

When FEAT_ECV is implemented:

Controls the scale of the generation of the event stream.

<table>
<thead>
<tr>
<th>EVNTIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CNTKCTL.EVNTI field applies to CNTVCT[15:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>The CNTKCTL.EVNTI field applies to CNTVCT[23:16].</td>
</tr>
</tbody>
</table>

This control applies regardless of the value of the CNTHCTL_EL2.ECV bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [16:10]**

Reserved, RES0.
**PLOPTEN, bit [9]**

Traps PL0 accesses to the physical timer registers to Undefined mode.

<table>
<thead>
<tr>
<th>PLOPTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PL0 accesses to the <strong>CNTP_CTL</strong>, <strong>CNTP_CVAL</strong>, and <strong>CNTP_TVAL</strong> registers are trapped to Undefined mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PLOVTEN, bit [8]**

Traps PL0 accesses to the virtual timer registers to Undefined mode.

<table>
<thead>
<tr>
<th>PLOVTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PL0 accesses to the <strong>CNTV_CTL</strong>, <strong>CNTV_CVAL</strong>, and <strong>CNTV_TVAL</strong> registers are trapped to Undefined mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTI, bits [7:4]**

Selects which bit of the counter register **CNTVCT** is the trigger for the event stream generated from that counter, when that stream is enabled.

If FEAT_ECV is implemented, and CNTKCTL.EVNTIS is 1, this field selects a trigger bit in the range 8 to 23 of the counter register **CNTVCT**.

Otherwise, this field selects a trigger bit in the range 0 to 15 of the counter register.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTDIR, bit [3]**

Controls which transition of the counter register **CNTVCT** trigger bit, defined by EVNTI, generates an event when the event stream is enabled:

<table>
<thead>
<tr>
<th>EVNTDIR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A 0 to 1 transition of the trigger bit triggers an event.</td>
</tr>
<tr>
<td>0b1</td>
<td>A 1 to 0 transition of the trigger bit triggers an event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EVNTEN, bit [2]**

Enables the generation of an event stream from the counter register **CNTVCT**:

<table>
<thead>
<tr>
<th>EVNTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables the event stream.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables the event stream.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PLOVCTEN, bit [1]**

Traps PL0 accesses to the frequency register and virtual counter register to Undefined mode.

<table>
<thead>
<tr>
<th>PLOVCTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PL0 accesses to the <strong>CNTVCT</strong> are trapped to Undefined mode.</td>
</tr>
<tr>
<td></td>
<td>PL0 accesses to the <strong>CNTFRQ</strong> register are trapped to Undefined mode, if CNTKCTL.PL0PCTEN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PLOPCTEN, bit [0]**

Traps PL0 accesses to the frequency register and physical counter register to Undefined mode.

<table>
<thead>
<tr>
<th>PLOPCTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PL0 accesses to the CNTPCT are trapped to Undefined mode.</td>
</tr>
<tr>
<td></td>
<td>PL0 accesses to the CNTFREQ register are trapped to</td>
</tr>
<tr>
<td></td>
<td>Undefined mode, if CNTKCTL.PL0VCTEN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTKCTL**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>\{, \{#\}<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  return CNTKCTL;
elsif PSTATE.EL == EL2 then
  return CNTKCTL;
elsif PSTATE.EL == EL3 then
  return CNTKCTL;

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>\{, \{#\}<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  CNTKCTL = R[t];
elsif PSTATE.EL == EL2 then
  CNTKCTL = R[t];
elsif PSTATE.EL == EL3 then
  CNTKCTL = R[t];

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The CNTP_CTL characteristics are:

**Purpose**

Control register for the EL1 physical timer.

**Configuration**

AArch32 System register CNTP_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTP_CTL_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTP_CTL are UNDEFINED.

**Attributes**

CNTP_CTL is a 32-bit register.

**Field descriptions**

The CNTP_CTL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ISTATUS | IMASK | ENABLE |

**Bits [31:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from \textit{CNTP\_TVAL} continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to 0.

**Accessing the CNTP\_CTL**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>\!, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FeaT SEL2) then
        return CNTHPS_CTL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        return CNTHP_CTL_EL2;
    else
        return CNTP_CTL;
    endif
else
    return CNTP_CTL;
else
    PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '0' && CNTHCTL_EL2.EL1PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
            AArch32.TakeHypTrapException(0x03);
        elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
            return CNTP_CTL_NS;
        else
            return CNTP_CTL;
        endif
    elseif PSTATE.EL == EL2 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
            AArch32.TakeHypTrapException(0x03);
        elseif HaveEL(EL3) && ELUsingAArch32(EL3) then
            return CNTP_CTL_NS;
        else
            return CNTP_CTL;
        endif
    elseif PSTATE.EL == EL3 then
        if SCR.NS == '0' then
            return CNTP_CTL_S;
        else
            return CNTP_CTL_NS;
        endif
    else
        return CNTP_CTL_NS;
    endif
    MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
else
    if EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
end if

if PSTATE.EL == EL1 then
    if !ELUsingAArch32(EL1) && EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
else
    if EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
end if

if PSTATE.EL == EL2 then
    if !ELUsingAArch32(EL1) && EL2Enabled() && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
else
    if EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
end if

if SCR.NS == '0' then
    CNTP_CTL_S = R[t];
else
    CNTP_CTL_NS = R[t];
end if

if SCR.NS == '1' then
    CNTP_CTL_NS = R[t];
else
    CNTP_CTL_S = R[t];
end if

CNTP_CTL, Counter-timer Physical Timer Control register
CNTP_CVAL, Counter-timer Physical Timer CompareValue register

The CNTP_CVAL characteristics are:

**Purpose**

Holds the compare value for the EL1 physical timer.

**Configuration**

AArch32 System register CNTP_CVAL bits [63:0] are architecturally mapped to AArch64 System register CNTP_CVAL_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTP_CVAL are **UNDEFINED**.

**Attributes**

CNTP_CVAL is a 64-bit register.

**Field descriptions**

The CNTP_CVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CompareValue</td>
</tr>
<tr>
<td>62</td>
<td>CompareValue</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>CompareValue</td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL1 physical timer CompareValue.

When CNTP_CTL.ENABLE is 1, the timer condition is met when (CNTPCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTP_CTL.ISTATUS is set to 1.
- If CNTP_CTL.IMASK is 0, an interrupt is generated.

When CNTP_CTL.ENABLE is 0, the timer condition is not met, but CNTPCT continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are **RES0**.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTP_CVAL**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x04);
  elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      UNDEFINED;
    end if;
  end if;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL0PTEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTHCTL_EL2.EL1PCEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0PTEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
  return CNTHPS_CVAL_EL2;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
  return CNTHP_CVAL_EL2;
else
  return CNTP_CVAL;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL1PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
  AArch32.TakeHypTrapException(0x04);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
  return CNTP_CVAL_NS;
else
  return CNTP_CVAL;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CNTP_CVAL_NS;
  else
    return CNTP_CVAL;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return CNTP_CVAL_S;
  else
    return CNTP_CVAL_NS;
endif;

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.TGE == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    end
elsif EL2Enabled() && CNTKCTL.PL0PTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
    else
        UNDEFINED;
    end
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL0PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
    AArch32.TakeHypTrapException(0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
    CNTHPS_CVAL_EL2 = R[t2]:R[t];
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && SCR_EL3.NS == '1' then
    CNTHP_CVAL_EL2 = R[t2]:R[t];
else
    CNTP_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CNTHCTL_EL2.EL0PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        CNTP_CVAL_NS = R[t2]:R[t];
    else
        CNTP_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        CNTP_CVAL_NS = R[t2]:R[t];
    else
        CNTP_CVAL = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        CNTP_CVAL_S = R[t2]:R[t];
    else
        CNTP_CVAL_NS = R[t2]:R[t];
CNTP_TVAL, Counter-timer Physical Timer TimerValue register

The CNTP_TVAL characteristics are:

**Purpose**

Holds the timer value for the EL1 physical timer.

**Configuration**

AArch32 System register CNTP_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTP_TVAL_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTP_TVAL are UNDEFINED.

**Attributes**

CNTP_TVAL is a 32-bit register.

**Field descriptions**

The CNTP_TVAL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TimerValue |

**TimerValue, bits [31:0]**

The TimerValue view of the EL1 physical timer.

On a read of this register:

- If CNTP_CTL,ENABLE is 0, the value returned is UNKNOWN.
- If CNTP_CTL,ENABLE is 1, the value returned is (CNTP_CVAL - CNTPCT).

On a write of this register, CNTP_CVAL is set to (CNTPCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTP_CTL,ENABLE is 1, the timer condition is met when (CNTPCT - CNTP_CVAL) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTP_CTL,ISTATUS is set to 1.
- If CNTP_CTL,IMASK is 0, an interrupt is generated.

When CNTP_CTL,ENABLE is 0, the timer condition is not met, but CNTPCT continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTP_TVAL**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.E2H == '11' &amp;&amp; CNTHCTL_EL1.E1PTEN == '0' then
    if EL2Enabled() &amp;&amp; HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elif EL2Enabled() &amp;&amp; HCR_EL2.E2H == '10' &amp;&amp; CNTHCTL_EL2.E1PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elif EL2Enabled() &amp;&amp; HCR_EL2.<E2H,TGE> == '11' &amp;&amp; CNTHCTL_EL2.E1PTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elif EL2Enabled() &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  else
    EL2Enabled() &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.E2H == '0' &amp;&amp; CNTHCTL_EL2.E1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.E2H == '10' &amp;&amp; CNTHCTL_EL2.E1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.<E2H,TGE> == '11' &amp;&amp; CNTHCTL_EL2.E1PTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.<E2H,TGE> == '11' &amp;&amp; HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNEDEFINED;
    end
  else
    PSTATE.EL == EL1 then
      if !ELUsingAArch32(EL1) &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.E2H == '11' &amp;&amp; CNTHCTL_EL1.E1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        UNDEFINED;
      end
    elsif PSTATE.EL == EL2 then
      if !ELUsingAArch32(EL1) &amp;&amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.E2H == '11' &amp;&amp; CNTHCTL_EL1.E1PTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        UNDEFINED;
      end
    elsif PSTATE.EL == EL3 then
      if SCR.NS == '0' then
        return CNTP_TVAL_S;
      else
        return CNTP_TVAL_NS;
      end
    else
      return CNTP_TVAL_NS;
    end
  else
    return CNTP_TVAL_NS;
end
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
            CNTHPS_TVAL_EL2 = R[t];
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            CNTHP_TVAL_EL2 = R[t];
        else
            CNTTP_TVAL = R[t];
    elsif PSTATE.EL == EL1 then
        if !EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTKCTL_EL2.EL1PCEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' && CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL1PTEN == '0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCEN == '0' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && SCR_EL3.NS == '1' then
            CNTHPS_TVAL_EL2 = R[t];
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
            CNTHP_TVAL_EL2 = R[t];
        else
            CNTP_TVAL_NS = R[t];
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && ELUsingAArch32(EL3) then
            CNTP_TVAL_NS = R[t];
        else
            CNTP_TVAL = R[t];
    elsif PSTATE.EL == EL3 then
        if SCR.NS == '0' then
            CNTP_TVAL_S = R[t];
        else
            CNTP_TVAL_NS = R[t];
CNTPCT, Counter-timer Physical Count register

The CNTPCT characteristics are:

**Purpose**

Holds the 64-bit physical count value.

**Configuration**

AArch32 System register CNTPCT bits [63:0] are architecturally mapped to AArch64 System register CNTPCT_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTPCT are UNDEFINED.

All reads to the CNTPCT occur in program order relative to reads to CNTPCTSS or CNTPCT.

**Attributes**

CNTPCT is a 64-bit register.

**Field descriptions**

The CNTPCT bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
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</thead>
<tbody>
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<td></td>
<td></td>
<td></td>
<td>Physical count value</td>
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<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Physical count value.

**Accessing the CNTPCT**

Accesses to this register use the following encodings:

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') &&
    CNTKCTL_EL1.EL0PCTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x04);
  elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PCTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' && CNTHCTL_EL2.EL1PCTEN ==
    '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' &&
    CNTHCTL_EL2.EL1PCTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' &&
    CNTHCTL_EL2.EL0PCTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL.PL1PCTEN == '0' then
    AArch32.TakeHypTrapException(0x04);
  else
    return CNTPCT;
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1PCTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCTEN == '0' then
      AArch32.TakeHypTrapException(0x04);
    else
      return CNTPCT;
  elsif PSTATE.EL == EL2 then
    return CNTPCT;
  elsif PSTATE.EL == EL3 then
    return CNTPCT;
CNTPCTSS, Counter-timer Self-Synchronized Physical Count register

The CNTPCTSS characteristics are:

**Purpose**

Holds the 64-bit physical count value.

**Configuration**

AArch32 System register CNTPCTSS bits [63:0] are architecturally mapped to AArch64 System register CNTPCTSS_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_ECV is implemented. Otherwise, direct accesses to CNTPCTSS are UNDEFINED.

All reads to the CNTPCTSS occur in program order relative to reads to CNTPCT or CNTPCTSS.

This register is a self-synchronised view of the CNTPCT counter, and cannot be read speculatively.

**Attributes**

CNTPCTSS is a 64-bit register.

**Field descriptions**

The CNTPCTSS bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Self-Synchronized Physical count value</td>
</tr>
<tr>
<td>62</td>
<td>Self-Synchronized Physical count value</td>
</tr>
<tr>
<td>61</td>
<td>Bits [63:0]</td>
</tr>
<tr>
<td>60</td>
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<td>59</td>
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</tbody>
</table>

**Accessing the CNTPCTSS**

Accesses to this register use the following encodings:

MRRC {<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b1000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') &&
        CNTKCTL_EL1.EL0PCTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0PCTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '0' &&
        CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '10' &&
        CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' &&
        CNTHCTL_EL2.EL0PCTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL.PL1PCTEN == '0' then
        AArch32.TakeHypTrapException(0x04);
    else
        return CNTPCTSS;
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1PCTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CNTHCTL.PL1PCTEN == '0' then
        AArch32.TakeHypTrapException(0x04);
    else
        return CNTPCTSS;
    end
elsif PSTATE.EL == EL2 then
    return CNTPCTSS;
elsif PSTATE.EL == EL3 then
    return CNTPCTSS;
CNTV_CTL, Counter-timer Virtual Timer Control register

The CNTV_CTL characteristics are:

**Purpose**

Control register for the virtual timer.

**Configuration**

AArch32 System register CNTV_CTL bits [31:0] are architecturally mapped to AArch64 System register CNTV_CTL_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTV_CTL are UNDEFINED.

**Attributes**

CNTV_CTL is a 32-bit register.

**Field descriptions**

The CNTV_CTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0</td>
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<td>27</td>
<td>Reserved, RES0</td>
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<td>7</td>
<td>Reserved, RES0</td>
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<td>6</td>
<td>Reserved, RES0</td>
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<td>5</td>
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<td>4</td>
<td>Reserved, RES0</td>
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<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ENABLE, bit [0]**

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from CNTV_TVAL continues to count down.

---

**Note**

Disabling the output signal might be a power-saving option.

---

On a Warm reset, this field resets to 0.

**Accessing the CNTV_CTL**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c}\}{<q}> \text{<coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '1') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VTEN == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VTEN != '11' && IsFeatureImplemented(FEAT_SEL2) then
      return CNTHV_CTL_EL2;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' then
      return CNTHV_CTL_EL2;
    else
      return CNTV_CTL;
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      return CNTHV_CTL_EL2;
    else
      return CNTV_CTL;
  else
    if PSTATE.EL == EL1 then
      if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        return CNTV_CTL;
      end
    elsif PSTATE.EL == EL2 then
      return CNTV_CTL;
    elsif PSTATE.EL == EL3 then
      return CNTV_CTL;
  end

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VT == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
      CNTHVS_CTL_EL2 = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
      CNTHV_CTL_EL2 = R[t];
    else
      CNTV_CTL_EL2 = R[t];
  else
    CNTV_CTL = R[t];
  endif
endif
else
  CNTV_CTL = R[t];
endif

if PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VT == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    CNTV_CTL_EL2 = R[t];
  endif
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
else
  CNTV_CTL = R[t];
endif
The CNTV_CVAL characteristics are:

**Purpose**

Holds the compare value for the virtual timer.

**Configuration**

AArch32 System register CNTV_CVAL bits [63:0] are architecturally mapped to AArch64 System register CNTV_CVAL_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTV_CVAL are UNDEFINED.

**Attributes**

CNTV_CVAL is a 64-bit register.

**Field descriptions**

The CNTV_CVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CompareValue</td>
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<tr>
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<tr>
<td>0</td>
<td>CompareValue</td>
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</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the EL1 virtual timer CompareValue.

When CNTV_CTL.ENABLE is 1, the timer condition is met when (CNTVCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTV_CTL.ISTATUS is set to 1.
- If CNTV_CTL.IMASK is 0, an interrupt is generated.

When CNTV_CTL.ENABLE is 0, the timer condition is not met, but CNTVCT continues to count.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are RES0.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTV_CVAL**

Accesses to this register use the following encodings:

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      UNDEFINED;
  else
    endif
  endif
else
  UNDEFINED;
endif

if PSTATE.EL == EL1 then
  if !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTKCTL_EL2.EL0VTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      UNDEFINED;
    endif
  else
    UNDEFINED;
  endif
endif

if PSTATE.EL == EL2 then
  return CNTV_CVAL;
endif

if PSTATE.EL == EL3 then
  return CNTV_CVAL;
endif

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

coproc  CRm  opc1
0b1111  0b1110  0b0011
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
        CNTHVS_CVAL_EL2 = R[t2]:R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
        CNTHV_CVAL_EL2 = R[t2]:R[t];
    else
        CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1TVT == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL2 then
        CNTV_CVAL = R[t2]:R[t];
    elsif PSTATE.EL == EL3 then
        CNTV_CVAL = R[t2]:R[t];
CNTV_TVAL, Counter-timer Virtual Timer TimerValue register

The CNTV_TVAL characteristics are:

**Purpose**

Holds the timer value for the virtual timer.

**Configuration**

AArch32 System register CNTV_TVAL bits [31:0] are architecturally mapped to AArch64 System register CNTV_TVAL_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTV_TVAL are UNDEFINED.

**Attributes**

CNTV_TVAL is a 32-bit register.

**Field descriptions**

The CNTV_TVAL bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<td>TimerValue</td>
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</tbody>
</table>

**TimerValue, bits [31:0]**

The TimerValue view of the virtual timer.

On a read of this register:

- If CNTV_CTL.ENABLE is 0, the value returned is UNKNOWN.
- If CNTV_CTL.ENABLE is 1, the value returned is (CNTV_CVAL - CNTVCT).

On a write of this register, CNTV_CVAL is set to (CNTVCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTP_CTL.ENABLE is 1, the timer condition is met when (CNTVCT - CNTP_CVAL) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTV_CTL.ISTATUS is set to 1.
- If CNTV_CTL.IMASK is 0, an interrupt is generated.

When CNTV_CTL.ENABLE is 0, the timer condition is not met, but CNTVCT continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTV_TVAL**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x00);
  else
    UNDEFINED;
  endif
else
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  endif
if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1VT != '1' then
  return CNTHVS_TVAL_EL2;
else
  return CNTV_TVAL_EL2;
endif
else
  return CNTV_TVAL;
endif
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1VT == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    return CNTV_TVAL;
  endif
if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeature Implemented(FEAT_SEL2) then
  return CNTHVS_TVAL_EL2;
else
  return CNTV_TVAL_EL2;
endif
else
  return CNTV_TVAL;
endif
elsif PSTATE.EL == EL2 then
  return CNTV_TVAL;
else
  return CNTV_TVAL;
endif
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  endif
else ELUsingAArch32(EL1) && CNTKCTL.PL0VTEN == '0' then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x00);
  else
    UNDEFINED;
  endif
else EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VTEN == '0' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVT == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
else EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '0' && IsFeatureImplemented(FEAT_SEL2) then
  CNTHVS_TVAL_EL2 = R[t];
else EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCR_EL3.NS == '1' then
  CNTHV_TVAL_EL2 = R[t];
else
  CNTV_TVAL = R[t];
else
  PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1TVT == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      CNTV_TVAL = R[t];
else
    PSTATE.EL == EL2 then
      CNTV_TVAL = R[t];
else
    PSTATE.EL == EL3 then
      CNTV_TVAL = R[t];
  endif
endif

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The CNTVCT characteristics are:

**Purpose**

Holds the 64-bit virtual count value. The virtual count value is equal to the physical count value minus the virtual offset visible in CNTVOFF.

**Configuration**

AArch32 System register CNTVCT bits [63:0] are architecturally mapped to AArch64 System register CNTVCT_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTVCT are UNDEFINED.

The value of this register is the same as the value of CNTPCT in the following conditions:

- When EL2 is not implemented.
- When EL2 is implemented and is using AArch64, HCR_EL2.E2H, TGE is {1, 1}, and this register is read from Non-secure EL0.

All reads to the CNTVCT occur in program order relative to reads to CNTVCTSS or CNTVCT.

**Attributes**

CNTVCT is a 64-bit register.

**Field descriptions**

The CNTVCT bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Virtual count value |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Virtual count value |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:0]**

Virtual count value.

**Accessing the CNTVCT**

Accesses to this register use the following encodings:

```
MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') &&
    CNTKCTL_EL1.EL0VCTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x04);
  elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VCTEN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' &&
    CNTHCTL_EL2.EL0VCTEN == '0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVCT
    == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    return CNTVCT;
  end
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1TVCT == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    return CNTVCT;
  endif
elsif PSTATE.EL == EL2 then
  return CNTVCT;
elsif PSTATE.EL == EL3 then
  return CNTVCT;

CNTVCTSS, Counter-timer Self-Synchronized Virtual Count register

The CNTVCTSS characteristics are:

**Purpose**

Holds the 64-bit virtual count value. The virtual count value is equal to the physical count value visible in `CNTPCT` minus the virtual offset visible in `CNTVOFF`.

**Configuration**

AArch32 System register CNTVCTSS bits [63:0] are architecturally mapped to AArch64 System register `CNTVCTSS_EL0[63:0]`.

This register is present only when AArch32 is supported at any Exception level and FEAT_ECV is implemented. Otherwise, direct accesses to CNTVCTSS are **UNDEFINED**.

All reads to the CNTVCTSS occur in program order relative to reads to `CNTVCT` or CNTVCTSS.

This register is a self-synchronised view of the `CNTVCT` counter, and cannot be read speculatively.

**Attributes**

CNTVCTSS is a 64-bit register.

**Field descriptions**

The CNTVCTSS bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td><strong>Self-Synchronized Virtual count value</strong></td>
</tr>
<tr>
<td>31</td>
<td><strong>Self-Synchronized Virtual count value</strong></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Self-Synchronized Virtual count value.

**Accessing the CNTVCTSS**

Accesses to this register use the following encodings:

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b1001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && CNTKCTL_EL1.EL0VCTEN == '0' then if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then AArch64.AArch32SystemAccessTrap(EL2, 0x04); else AArch64.AArch32SystemAccessTrap(EL1, 0x04); elsif ELUsingAArch32(EL1) && CNTKCTL.PL0VCTEN == '0' then if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then AArch64.AArch32SystemAccessTrap(EL2, 0x04); elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then AArch32.TakeHypTrapException(0x00); else UNDEFINED; elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && CNTHCTL_EL2.EL0VCTEN == '0' then AArch64.AArch32SystemAccessTrap(EL2, 0x04); elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && CNTHCTL_EL2.EL1TVCT == '1' then AArch64.AArch32SystemAccessTrap(EL2, 0x04); else return CNTVCTSS; elsif PSTATE.EL == EL1 then if EL2Enabled() && !ELUsingAArch32(EL2) && CNTHCTL_EL2.EL1TVCT == '1' then AArch64.AArch32SystemAccessTrap(EL2, 0x04); else return CNTVCTSS; elsif PSTATE.EL == EL2 then return CNTVCTSS; elsif PSTATE.EL == EL3 then return CNTVCTSS;
CNTVOFF, Counter-timer Virtual Offset register

The CNTVOFF characteristics are:

**Purpose**

Holds the 64-bit virtual offset. This is the offset between the physical count value visible in **CNTPCT** and the virtual count value visible in **CNTVCT**.

**Configuration**

AArch32 System register CNTVOFF bits [63:0] are architecturally mapped to AArch64 System register **CNTVOFF_EL2[63:0]**.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CNTVOFF are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3 and the virtual counter uses a fixed virtual offset of zero.

**Note**

When EL2 is implemented and is using AArch64, if **HCR_EL2.{E2H, TGE}** is \{1, 1\}, the virtual counter uses a fixed virtual offset of zero when **CNTVCT** is read from Non-secure EL0.

**Attributes**

CNTVOFF is a 64-bit register.

**Field descriptions**

The CNTVOFF bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual offset.

If the Generic counter is implemented at a size less than 64 bits, then this field is permitted to be implemented at the same width as the counter, and the upper bits are **RES0**.

The value of this field is treated as zero-extended in all counter calculations.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTVOFF**

Accesses to this register use the following encodings:

```
MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    return CNTVOFF;
elsif PSTATE.EL == EL3 then
    return CNTVOFF;

MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1110</td>
<td>0b0100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    CNTVOFF = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
    CNTVOFF = R[t2]:R[t];
CONTEXTIDR, Context ID Register

The CONTEXTIDR characteristics are:

**Purpose**

Identifies the current Process Identifier and, when using the Short-descriptor translation table format, the Address Space Identifier.

The value of the whole of this register is called the Context ID and is used by:

- The debug logic, for Linked and Unlinked Context ID matching.
- The trace logic, to identify the current process.

The significance of this register is for debug and trace use only.

**Configuration**

AArch32 System register CONTEXTIDR bits [31:0] are architecturally mapped to AArch64 System register CONTEXTIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CONTEXTIDR are undefined.

The register format depends on whether address translation is using the Long-descriptor or the Short-descriptor translation table format.

**Attributes**

CONTEXTIDR is a 32-bit register.

**Field descriptions**

The CONTEXTIDR bit assignments are:

**When TTBCR.EAE == 0:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**PROCID**, bits [31:8]

Process Identifier. This field must be programmed with a unique value that identifies the current process.

On a Warm reset, this field resets to an architecturally unknown value.

**ASID**, bits [7:0]

Address Space Identifier. This field is programmed with the value of the current ASID.

On a Warm reset, this field resets to an architecturally unknown value.

**When TTBCR.EAE == 1:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**PROCID**
**PROCID, bits [31:0]**

Process Identifier. This field must be programmed with a unique value that identifies the current process.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CONTEXTIDR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{ <coproc>, \{#}\text{<opc1>}, <Rt>, <CRn>, <CRm}\{, \{#\text{<opc2>}}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CONTEXTIDR_NS;
  else
    return CONTEXTIDR;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CONTEXTIDR_NS;
  else
    return CONTEXTIDR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return CONTEXTIDR_S;
  else
    return CONTEXTIDR_NS;
```

**MCR\{<c>\}{<q>} \text{ <coproc>, \{#\text{<opc1>}, <Rt>, <CRn}, <CRm}\{, \{#\text{<opc2>}}\}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        CONTEXTIDR_NS = R[t];
    else
        CONTEXTIDR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        CONTEXTIDR_NS = R[t];
    else
        CONTEXTIDR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        CONTEXTIDR_S = R[t];
    else
        CONTEXTIDR_NS = R[t];
CP15DMB, Data Memory Barrier System instruction

The CP15DMB characteristics are:

**Purpose**

Performs a Data Memory Barrier.

Arm deprecates any use of this System instruction, and strongly recommends that software use the DMB instruction instead.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CP15DMB are UNDEFINED.

**Attributes**

CP15DMB is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by \(<Rt>\) is ignored.

**Executing the CP15DMB instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \ <\text{coproc}>\, \{\#<\text{opc}1>, \ <Rt>, \ <\text{CRn}>, \ <\text{CRm}>\}, \ {\#}<\text{opc}2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b101</td>
</tr>
</tbody>
</table>


if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL1.CP15BEN == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.CP15BEN == '0' then
        UNDEFINED;
    elsif ELUsingAArch32(EL1) && SCTLR.CP15BEN == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        CP15DMB();
    end
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif SCTLR.CP15BEN == '0' then
        UNDEFINED;
    else
        CP15DMB();
    end
elsif PSTATE.EL == EL2 then
    if HSCTLR.CP15BEN == '0' then
        UNDEFINED;
    else
        CP15DMB();
    end
elsif PSTATE.EL == EL3 then
    if SCTLR.CP15BEN == '0' then
        UNDEFINED;
    else
        CP15DMB();
    end
CP15DSB, Data Synchronization Barrier System instruction

The CP15DSB characteristics are:

**Purpose**

Performs a Data Synchronization Barrier.

Arm deprecates any use of this System instruction, and strongly recommends that software use the DSB instruction instead.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CP15DSB are UNDEFINED.

**Attributes**

CP15DSB is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the CP15DSB instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{\langle c\rangle\}{\langle q\rangle}\ \langle\text{coproc}\rangle,\ {\#}\langle\text{opc1}\rangle,\ <\text{Rt}\rangle,\ <\text{CRn}\rangle,\ <\text{CRm}\rangle{\langle\#}\langle\text{opc2}\rangle}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL1.CP15BEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.CP15BEN == '0' then
    UNDEFINED;
  elsif ELUsingAArch32(EL1) && SCTLR.CP15BEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    CP15DSB();
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elseif SCTLR.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15DSB();
  elsif PSTATE.EL == EL2 then
    if HSCTLR.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15DSB();
  elsif PSTATE.EL == EL3 then
    if SCTLR.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15DSB();

The CP15ISB characteristics are:

**Purpose**

Performs an Instruction Synchronization Barrier.

Arm deprecates any use of this System instruction, and strongly recommends that software use the ISB instruction instead.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CP15ISB are UNDEFINED.

**Attributes**

CP15ISB is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the CP15ISB instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') && SCTLR_EL1.CP15BEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' && SCTLR_EL2.CP15BEN == '0' then
    UNDEFINED;
  elsif ELUsingAArch32(EL1) && SCTLR.CP15BEN == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    CP15ISB();
  elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif SCTLR.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15ISB();
  elsif PSTATE.EL == EL2 then
    if HSCTRL.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15ISB();
  elsif PSTATE.EL == EL3 then
    if SCTLR.CP15BEN == '0' then
      UNDEFINED;
    else
      CP15ISB();

CPACR, Architectural Feature Access Control Register

The CPACR characteristics are:

**Purpose**

Controls access to trace, and to Advanced SIMD and floating-point functionality from EL0, EL1, and EL3.

In an implementation that includes EL2, the CPACR has no effect on instructions executed at EL2.

**Configuration**

AArch32 System register CPACR bits [31:0] are architecturally mapped to AArch64 System register CPACR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CPACR are UNDEFINED.

Bits in the NSACR control Non-secure access to the CPACR fields. See the field descriptions for more information.

**Note**

In the register field descriptions, controls are described as applying at specified Privilege levels. This is because, in Secure state, a PL1 control:

- Applies to execution in a Secure EL3 mode when EL3 is using AArch32.
- Applies to execution in a Secure EL1 mode when EL3 is using AArch64.

See ‘Security state, Exception levels, and AArch32 execution privilege’.

**Attributes**

CPACR is a 32-bit register.

**Field descriptions**

The CPACR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ASE</td>
<td>DIS</td>
<td>RES</td>
<td>0</td>
<td>TRCDIS</td>
<td>RESO</td>
<td>cp11</td>
<td>cp10</td>
<td>RESO</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ASEDIS, bit [31]**

Disables PL0 and PL1 execution of Advanced SIMD instructions.

<table>
<thead>
<tr>
<th>ASEDIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control permits execution of Advanced SIMD instructions at PL0 and PL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>All instruction encodings that are Advanced SIMD instruction encodings, but are not also floating-point instruction encodings, are UNDEFINED at PL0 and PL1.</td>
</tr>
</tbody>
</table>

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0. Otherwise, it is IMPLEMENTATION DEFINED whether this field is implemented as a RW field. If it is not implemented as a RW field, it is RAZ/WI.

If EL3 is implemented and is using AArch32, and the value of NSACR.NSASEDIS is 1, this field behaves as RAO/WI in Non-secure state, regardless of its actual value. This applies even if the field is implemented as RAZ/WI.
For the list of instructions affected by this field, see 'Controls of Advanced SIMD operation that do not apply to floating-point operation'.

See the description of CPACR.cp10 for a list of other controls that can disable or trap execution of Advanced SIMD instructions in AArch32 state.

On a Warm reset, this field resets to 0.

Bits [30:29]

Reserved, RES0.

TRCDIS, bit [28]

Traps PL0 and PL1 System register accesses to all implemented trace registers to Undefined mode.

<table>
<thead>
<tr>
<th>TRCDIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on PL0 and PL1 System register accesses to trace registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>PL0 and PL1 System register accesses to all implemented trace registers are trapped to Undefined mode.</td>
</tr>
</tbody>
</table>

If the implementation does not include a PE trace unit, or does not include a System register interface to the PE trace unit registers, this field is RES0. Otherwise, it is IMPLEMENTATION DEFINED whether this field is implemented as a RW field. If it is not implemented as a RW field, it is RAZ/WI.

If EL3 is implemented and is using AArch32, and the value of NSACR.NSTRCDIS is 1, this field behaves as RAO/WI in Non-secure state, regardless of its actual value. This applies even if the field is implemented as RAZ/WI.

Note

- The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are UNDEFINED.
- The architecture does not provide traps on trace register accesses through the optional memory-mapped external debug interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [27:24]

Reserved, RES0.

cp11, bits [23:22]

The value of this field is ignored. If this field is programmed with a different value to the cp10 field then this field is UNKNOWN on a direct read of the CPACR.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0.

In Non-secure state, if EL3 is implemented and is using AArch32, when the value of NSACR.cp10 is 0, this field behaves as RAZ/WI, regardless of its actual value.

On a Warm reset, this field resets to 0.

cp10, bits [21:20]

Defines the access rights for the floating-point and Advanced SIMD functionality. Possible values of the field are:
<table>
<thead>
<tr>
<th>cp10</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>PL0 and PL1 accesses to floating-point and Advanced SIMD registers or instructions are UNDEFINED.</td>
</tr>
<tr>
<td>0b01</td>
<td>PL0 accesses to floating-point and Advanced SIMD registers or instructions are UNDEFINED.</td>
</tr>
<tr>
<td>0b10</td>
<td>Reserved. The effect of programming this field to this value is CONSTRAINED UNPREDICTABLE. See 'Handling of System register control fields for Advanced SIMD and floating-point operation'.</td>
</tr>
<tr>
<td>0b11</td>
<td>This control permits full access to the floating-point and Advanced SIMD functionality from PL0 and PL1.</td>
</tr>
</tbody>
</table>

The floating-point and Advanced SIMD features controlled by these fields are:

- Execution of any floating-point or Advanced SIMD instruction.
- Any access to the Advanced SIMD and floating-point registers D0-D31 and their views as S0-S31 and Q0-Q15.
- Any access to the FPSCR, FPSID, MVFR0, MVFR1, MVFR2, or FPEXC System registers.

**Note**

The CPACR has no effect on floating-point and Advanced SIMD accesses from PL2. These can be disabled by the HCPTR.TCP10 field.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0.

In Non-secure state, if EL3 is implemented and is using AArch32, when the value of NSACR.cp10 is 0, this field behaves as RAZ/WI, regardless of its actual value.

Execution of floating-point and Advanced SIMD instructions in AArch32 state can be disabled or trapped by the following controls:

- CPACR.cp10, or, if executing at EL0, CPACR_EL1.FPEN.
- FPEXC.EN.
- If executing in Non-secure state:
  - HCPTR.TCP10, or if EL2 is using AArch64, CPTR_EL2.TFP.
  - NSACR.cp10, or if EL3 is using AArch64, CPTR_EL3.TFP.
- For Advanced SIMD instructions only:
  - CPACR.ASEDIS.
  - If executing in Non-secure state, HCPTR.TASE and NSACR.NSTRCDIS.

See the descriptions of the controls for more information.

On a Warm reset, this field resets to 0.

**Bits [19:0]**

Reserved, RES0.

**Accessing the CPACR**

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\} \{<q>\} \text{<coproc>}, \{#\text{<opc1>\}, \text{<Rt>\}, \text{<CRn>\}, \text{<CRm>\}, \{#\text{<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b001</td>
<td>0b000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TCPAC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCPTR.TCPAC == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
      return CPACR;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      else
        return CPACR;
    elsif PSTATE.EL == EL3 then
      return CPACR;
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL2.TCPAC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CPTR_EL2.TCPAC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && CPTR_EL3.TCPAC == '1' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && CPTR_EL3.TCPAC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && CPTR_EL3.TCPAC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif PSTATE.EL == EL2 then
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if
        elsif PSTATE.EL == EL3 then
            CPACR = R[t];
        else
            CPACR = R[t];
        end if
    end if

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The CPPRCTX characteristics are:

**Purpose**

Cache Prefetch Prediction Restriction by Context applies to all Cache Allocation Resources that predict cache allocations based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, cache prefetch prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction applies to all:

- Instruction caches.
- Data caches.
- TLB prefetching hardware used by the executing PE that applies to the supplied context or contexts.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of Cache Allocation Resources so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level and FEAT_SPECRES is implemented. Otherwise, direct accesses to CPPRCTX are UNDEFINED.

**Attributes**

CPPRCTX is a 32-bit System instruction.

**Field descriptions**

The CPPRCTX input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>GVMIDNS</td>
</tr>
<tr>
<td>29</td>
<td>EL</td>
</tr>
<tr>
<td>28</td>
<td>VMID</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>GASID</td>
</tr>
<tr>
<td>25</td>
<td>ASID</td>
</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**GVMID, bit [27]**

Execution of this instruction applies to all VMIDs or a specified VMID.
For target execution contexts other than EL0 or EL1, this field is RES0.

If the instruction is executed at EL0 or EL1, then this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**NS, bit [26]**

Security State.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure state.</td>
</tr>
</tbody>
</table>

If the instruction is executed in Non-secure state, this field is treated as 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>EL0.</td>
</tr>
<tr>
<td>0b01</td>
<td>EL1.</td>
</tr>
<tr>
<td>0b10</td>
<td>EL2.</td>
</tr>
<tr>
<td>0b11</td>
<td>EL3.</td>
</tr>
</tbody>
</table>

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**VMID, bits [23:16]**

Only applies when bit[27] is 0 and the target execution context is either:

- EL1.
- EL0 when (HCR_EL2.E2H==0 or HCR_EL2.TGE==0) or EL2 is using AArch32 state.

Otherwise this field is RES0.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==0 or HCR_EL2.TGE==0 or ELUsingAArch32(EL2)), this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==1 and HCR_EL2.TGE==1 and !ELUsingAArch32(EL2)), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**Bits [15:9]**

Reserved, RES0.

**GASID, bit [8]**

Execution of this instruction applies to all ASIDs or a specified ASID.

<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

CPPRCTX, Cache Prefetch Prediction Restriction by Context
For target execution contexts other than EL0, this field is \texttt{RES0}.

If the instruction is executed at EL0, this field has an Effective value of 0.

**ASID, bits [7:0]**

Only applies for an EL0 target execution context and when bit[8] is 0.

Otherwise, this field is \texttt{RES0}.

When the instruction is executed at EL0, this field is treated as the current ASID.

**Executing the CPPRCTX instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} \{coproc\}, \{#<opc1>\}, \{<Rt>\}, \{<CRn>\}, \{<CRm>\}, \{#<opc2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0111</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !(EL2Enabled() && HCR_EL2.<E2H,TGE> == '11') &&! SCTL.R_EL1.EnRCTX == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  else
    ELUsingAArch32(EL1) && SCTL.R_EL1.EnRCTX == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        UNDEFINED;
      else
        !ELUsingAArch32(EL1) && HSTR_EL2.T7 == '1' then
          AArchEL3.FGTEn == '1' && HFGITR_EL2.CPPRCTX == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
          CPPRCTX(R[t]);
  else
    PSTATE.EL == EL1 then
      if !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
          AArch32.TakeHypTrapException(0x03);
        else
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      else
        EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
          AArch32.TakeHypTrapException(0x03);
      else
        EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
          AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
          CPPRCTX(R[t]);
  else
    PSTATE.EL == EL2 then
      CPPRCTX(R[t]);
    else
      PSTATE.EL == EL3 then
        CPPRCTX(R[t]);
CPSR, Current Program Status Register

The CPSR characteristics are:

**Purpose**

Holds PE status and control information.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CPSR are UNDEFINED.

**Attributes**

CPSR is a 32-bit register.

**Field descriptions**

The CPSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>N</td>
</tr>
<tr>
<td>30</td>
<td>Z</td>
</tr>
<tr>
<td>29</td>
<td>C</td>
</tr>
<tr>
<td>28</td>
<td>V</td>
</tr>
<tr>
<td>27</td>
<td>Q</td>
</tr>
<tr>
<td>26</td>
<td>RES0</td>
</tr>
<tr>
<td>25</td>
<td>SSBS</td>
</tr>
<tr>
<td>24</td>
<td>PAND</td>
</tr>
<tr>
<td>23</td>
<td>IT</td>
</tr>
<tr>
<td>22</td>
<td>RES1</td>
</tr>
<tr>
<td>21</td>
<td>GE</td>
</tr>
<tr>
<td>20</td>
<td>RES0</td>
</tr>
<tr>
<td>19</td>
<td>E</td>
</tr>
<tr>
<td>18</td>
<td>A</td>
</tr>
<tr>
<td>17</td>
<td>I</td>
</tr>
<tr>
<td>16</td>
<td>F</td>
</tr>
<tr>
<td>15</td>
<td>RES0</td>
</tr>
<tr>
<td>14</td>
<td>RES1</td>
</tr>
<tr>
<td>13</td>
<td>M</td>
</tr>
</tbody>
</table>

**N, bit [31]**

Negative condition flag. Set to bit[31] of the result of the last flag-setting instruction. If the result is regarded as a two's complement signed integer, then N is set to 1 if the result was negative, and N is set to 0 if the result was positive or zero.

**Z, bit [30]**

Zero condition flag. Set to 1 if the result of the last flag-setting instruction was zero, and to 0 otherwise. A result of zero often indicates an equal result from a comparison.

**C, bit [29]**

Carry condition flag. Set to 1 if the last flag-setting instruction resulted in a carry condition, for example an unsigned overflow on an addition.

**V, bit [28]**

Overflow condition flag. Set to 1 if the last flag-setting instruction resulted in an overflow condition, for example a signed overflow on an addition.

**Q, bit [27]**

Cumulative saturation bit. Set to 1 to indicate that overflow or saturation occurred in some instructions.

**Bits [26:24]**

Reserved, RES0.

**SSBS, bit [23]**
When FEAT_SSBS is implemented:

Speculative Store Bypass Safe.

Prohibits speculative loads or stores which might practically allow a cache timing side channel.

A cache timing side channel might be exploited where a load or store uses an address that is derived from a register that is being loaded from memory using a load instruction speculatively read from a memory location. If PSTATE.SSBS is enabled, the address derived from the load instruction might be from earlier in the coherence order than the latest store to that memory location with the same virtual address.

<table>
<thead>
<tr>
<th>SSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hardware is not permitted to load or store speculatively in the manner described.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hardware is permitted to load or store speculatively in the manner described.</td>
</tr>
</tbody>
</table>

The value of this bit is usually set to the value described by the SCTLR.DSSBS bit on exceptions to any mode except Hyp mode, and the value described by HSCTLR.DSSBS on exceptions to Hyp mode.

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never.

<table>
<thead>
<tr>
<th>PAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation system is the same as Armv8.0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Disables privileged read and write accesses to addresses accessible at EL0.</td>
</tr>
</tbody>
</table>

The value of this bit is usually preserved on taking an exception, except in the following situations:

- When the target of the exception is EL1, and the value of the SCTLR.SPAN bit for the current Security state is 0, this bit is set to 1.
- When the target of the exception is EL3, from Secure state, and the value of the Secure SCTLR.SPAN is 0, this bit is set to 1.
- When the target of the exception is EL3, from Non-secure state, this bit is set to 0 regardless of the value of the Secure SCTLR.SPAN bit.

Otherwise:

Reserved, RES0.

DIT, bit [21]

When FEAT_DIT is implemented:

Data Independent Timing.
The values of the data supplied in any of its
The architecture makes no statement about the timing properties of any instructions.

The architecture requires that:

- The timing of every load and store instruction is insensitive to the value of the data being loaded or stored.
- For certain data processing instructions, the instruction takes a time which is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- For certain data processing instructions, the response of the instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

The timing of every load and store instruction is insensitive to the value of the data being loaded or stored.

- For certain data processing instructions, the instruction takes a time which is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- For certain data processing instructions, the response of the instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

<table>
<thead>
<tr>
<th>DIT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The architecture makes no statement about the timing properties of any instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>The architecture requires that:</td>
</tr>
</tbody>
</table>

- The timing of every load and store instruction is insensitive to the value of the data being loaded or stored.
- For certain data processing instructions, the instruction takes a time which is independent of:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.
- For certain data processing instructions, the response of the instruction to asynchronous exceptions does not vary based on:
  - The values of the data supplied in any of its registers.
  - The values of the NZCV flags.

The processing instructions affected by this bit are:

- All cryptographic instructions. These instructions are:
  - AESD, AESE, AESIMC, AESMC, SHA1C, SHA1H, SHA1M, SHA1P, SHA1SU0, SHA1SU1, SHA256H, SHA256H2, SHA256SU0, and SHA256SU1.

- A subset of those instructions which use the general-purpose register file. For these instructions, the effects of CPSR.DIT apply only if they do not use R15 as either their source or destination and pass their condition execution check. The instructions are:

- A subset of those instructions which use the general-purpose register file. For these instructions, the effects of CPSR.DIT do not depend on these instructions passing their condition execution check. These instructions are:
  - ADC (immediate), ADC (register), ADCS (immediate), ADCS (register), ADD (immediate), ADD (register), ADDS (immediate), ADDS (register), AND (immediate), AND (register), ANDS (immediate), ANDS (register), ASR (immediate), ASR (register), ASRS (immediate), ASRS (register), BIC (immediate), BIC (register), BICS (immediate), BICS (register), EOR (immediate), EOR (register), EORS (immediate), EORS (register), LSL (immediate), LSL (register), LSLS (immediate), LSLS (register), LSR (immediate), LSR (register), LSLS (immediate), LSLS (register), MOV (immediate), MOV (register), MOV (register), MOV (register), MOV (register), MOV (register), MVN (immediate), MVN (register), MVNS (immediate), MVNS (register), MVNS (immediate), MVNS (register), ORR (immediate), ORR (register), ORR (register), ORRS (immediate), ORRS (register), ROR (immediate), RORS (register), RSB (immediate), RSB (register), RSB (register), RSC (immediate), RSC (register), RSC (register), RSCS (register), SBC (immediate), SBC (register), SBCS (immediate), SBCS (register), SUB (immediate), SUB (register), SUBS (immediate), and SUBS (register).

- A subset of those instructions which use the SIMD&FP register file. For these instructions, the effects of CPSR.DIT do not depend on whether they tagged or condition execution check. These instructions are:
  - CRC32B, CRC32H, CRC32W, CRC32CB, CRC32CW, VABA*, VABD*, VABS, VACGE, VACGT, VACLE, VAECTL, VADD (integer), VADDH, VADDL, VADDW, VAND, VBIC, VBIF, VBIT, VBLS, VCGE, VCOT, VCLE, VCLS, VCLT, VCLZ, VCMP, VCMPE, VCNT, VDUP, VEOR, VEXT, VHADD, VHADD, VHSH, VMAX (integer), VMIN (integer), VMIA (integer), VMLA (integer), VMAL, VMAS (integer), VMLS, VMOV, VMOV, VMOV, VMVNN, VMUL (integer and polynomial), VMULL (integer and polynomial), VMU, VMUG, VORN, VORR, VPADAL, VPADD (integer), VPADDL, VPMAX (integer), VPVMAX (integer), VPVMAX (integer), and VMU.
VPMIN (integer), VRADDHN, VREV*, VRHADD, VRSHL, VRSHR, VRSHRN, VRSRA, VRSUBHN, VSELEQ, VSELGE, VSELG, VSELVS, VSHL, VSHLL, VSHR, VSLI, VSRA, VSRI, VSUB (integer), VSUBHN, VSUBL, VSUBW, VSWP, VTBL, VTBX, VTRN, VTST, VUZP, and VZIP

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [20]

Reserved, RES0.

GE, bits [19:16]

Greater than or Equal flags, for parallel addition and subtraction.

Bits [15:10]

Reserved, RES0.

E, bit [9]

Endianness state bit. Controls the load and store endianness for data accesses:

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Little-endian operation</td>
</tr>
<tr>
<td>0b1</td>
<td>Big-endian operation</td>
</tr>
</tbody>
</table>

Instruction fetches ignore this bit.

If an implementation does not provide Big-endian support, this bit is RES0. If it does not provide Little-endian support, this bit is RES1.

If an implementation provides Big-endian support but only at EL0, this bit is RES0 for an exception return to any Exception level other than EL0.

Likewise, if it provides Little-endian support only at EL0, this bit is RES1 for an exception return to any Exception level other than EL0.

When the reset value of the SCTLR.EE bit is defined by a configuration input signal, that value also applies to the CPSR.E bit on reset, and therefore applies to software execution from reset.

A, bit [8]

SError interrupt mask bit. The possible values of this bit are:

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>

I, bit [7]

IRQ mask bit. The possible values of this bit are:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>
F, bit [6]

FIQ mask bit. The possible values of this bit are:

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception not masked.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception masked.</td>
</tr>
</tbody>
</table>

Bit [5]

Reserved, RES0.

Bit [4]

Reserved, RES1.

M, bits [3:0]

Current PE mode. Possible values are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>User.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b0010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Monitor.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b1111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Accessing the CPSR

CPSR can be read using the MRS instruction and written using the MSR (register) or MSR (immediate) instructions.
CSSELR, Cache Size Selection Register

The CSSELR characteristics are:

Purpose

Selects the current Cache Size ID Register, `CSSIDR`, by specifying the required cache level and the cache type, which is either instruction cache or data cache.

If `FEAT_CCIDX` is implemented, CSSELR also selects the current `CSSIDR2`.

Configuration

AArch32 System register CSSELR bits [31:0] are architecturally mapped to AArch64 System register `CSSELR_EL1[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CSSELR are UNDEFINED.

Attributes

CSSELR is a 32-bit register.

Field descriptions

The CSSELR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>Level</td>
<td>Cache level of required cache.</td>
</tr>
<tr>
<td>29</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>18</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Bits [31:4]

Reserved, RES0.

Level, bits [3:1]

Cache level of required cache. Permitted values are:

<table>
<thead>
<tr>
<th>Level</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Level 1 cache.</td>
</tr>
<tr>
<td>0b001</td>
<td>Level 2 cache.</td>
</tr>
<tr>
<td>0b010</td>
<td>Level 3 cache.</td>
</tr>
<tr>
<td>0b011</td>
<td>Level 4 cache.</td>
</tr>
<tr>
<td>0b100</td>
<td>Level 5 cache.</td>
</tr>
<tr>
<td>0b101</td>
<td>Level 6 cache.</td>
</tr>
<tr>
<td>0b110</td>
<td>Level 7 cache.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If CSSELR.Level is programmed to a cache level that is not implemented, then the value for this field on a read of CSSELR is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

InD, bit [0]

Instruction not Data bit. Permitted values are:
CSSELR, Cache Size Selection Register

<table>
<thead>
<tr>
<th>InD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Data or unified cache.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction cache.</td>
</tr>
</tbody>
</table>

If CSSELR.Level is programmed to a cache level that is not implemented, then the value for this field on a read of CSSELR is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the CSSELR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

### Table 1

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b010</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID4 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID2 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TID4 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CSSELR_NS;
  else
    return CSSELR;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return CSSELR_NS;
  else
    return CSSELR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return CSSELR_S;
  else
    return CSSELR_NS;
else
  if SCR.NS == '0' then
    return CSSELR_S;
  else
    return CSSELR_NS;

### Table 2

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b010</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID4 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TID4 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        CSSELR_NS = R[t];
    else
        CSSELR = R[t];
elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        CSSELR_NS = R[t];
    else
        CSSELR = R[t];
elsif PSTATE_EL == EL3 then
    if SCR.NS == '0' then
        CSSELR_S = R[t];
    else
        CSSELR_NS = R[t];
The CTR characteristics are:

**Purpose**

Provides information about the architecture of the caches.

**Configuration**

AArch32 System register CTR bits [31:0] are architecturally mapped to AArch64 System register `CTR_EL0[31:0]`. This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to CTR are UNDEFINED.

**Attributes**

CTR is a 32-bit register.

**Field descriptions**

The CTR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES1| RES0| DIC| IDC| CWG| ERG| DminLine| L1Ip| RES0| IminLine|

**Bit [31]**

Reserved, RES1.

**Bit [30]**

Reserved, RES0.

**DIC, bit [29]**

Instruction cache invalidation requirements for data to instruction coherence.

<table>
<thead>
<tr>
<th>DIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction cache invalidation to the Point of Unification is required for data to instruction coherence.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction cache invalidation to the Point of Unification is not required for data to instruction coherence.</td>
</tr>
</tbody>
</table>

**IDC, bit [28]**

Data cache clean requirements for instruction to data coherence. The meaning of this bit is:

<table>
<thead>
<tr>
<th>IDC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Data cache clean to the Point of Unification is required for instruction to data coherence, unless CLIDR.LoC == 0b000 or (CLIDR.LoUIS == 0b000 &amp;&amp; CLIDR.LoUU == 0b000).</td>
</tr>
<tr>
<td>0b1</td>
<td>Data cache clean to the Point of Unification is not required for instruction to data coherence.</td>
</tr>
</tbody>
</table>
**CWG, bits [27:24]**

Cache writeback granule. $\log_2$ of the number of words of the maximum size of memory that can be overwritten as a result of the eviction of a cache entry that has had a memory location in it modified.

A value of $0b0000$ indicates that this register does not provide Cache writeback granule information and either:

- The architectural maximum of 512 words (2KB) must be assumed.
- The Cache writeback granule can be determined from maximum cache line size encoded in the Cache Size ID Registers.

Values greater than $0b1001$ are reserved.

Arm recommends that an implementation that does not support cache write-back implements this field as $0b0001$. This applies, for example, to an implementation that supports only write-through caches.

**ERG, bits [23:20]**

Exclusives reservation granule. $\log_2$ of the number of words of the maximum size of the reservation granule that has been implemented for the Load-Exclusive and Store-Exclusive instructions.

The use of the value $0b0000$ is deprecated.

The value $0b0001$ and values greater than $0b1001$ are reserved.

**DminLine, bits [19:16]**

$\log_2$ of the number of words in the smallest cache line of all the data caches and unified caches that are controlled by the PE.

**L1Ip, bits [15:14]**

Level 1 instruction cache policy. Indicates the indexing and tagging policy for the L1 instruction cache. Possible values of this field are:

<table>
<thead>
<tr>
<th>L1Ip</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>VMID aware Physical Index, Physical tag (VPIPT)</td>
</tr>
<tr>
<td>0b01</td>
<td>ASID-tagged Virtual Index, Virtual Tag (AIIVT)</td>
</tr>
<tr>
<td>0b10</td>
<td>Virtual Index, Physical Tag (VIFT)</td>
</tr>
<tr>
<td>0b11</td>
<td>Physical Index, Physical Tag (PIPT)</td>
</tr>
</tbody>
</table>

The value $0b00$ is permitted only in an implementation that includes FEAT_VPIPT, otherwise the value is reserved.

The value $0b01$ is not permitted in Armv8.

**Bits [13:4]**

Reserved, RES0.

**IminLine, bits [3:0]**

$\log_2$ of the number of words in the smallest cache line of all the instruction caches that are controlled by the PE.

**Accessing the CTR**

Accesses to this register use the following encodings:

```
MRC{<c}<{q} <coproc>, {#<opc1>, <Rt>, <CRn>, <CRm>{, {#<opc2>}}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return CTR;
    endif
elsif PSTATE.EL == EL2 then
    return CTR;
elsif PSTATE.EL == EL3 then
    return CTR;
DACR, Domain Access Control Register

The DACR characteristics are:

**Purpose**

Defines the access permission for each of the sixteen memory domains.

**Configuration**

AArch32 System register DACR bits [31:0] are architecturally mapped to AArch64 System register DACR32_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DACR are UNDEFINED.

This register has no function when TTBCR.EAE is set to 1, to select the Long-descriptor translation table format.

**Attributes**

DACR is a 32-bit register.

**Field descriptions**

The DACR bit assignments are:

<table>
<thead>
<tr>
<th>D&lt;n&gt;, bits [2n+1:2n], for n = 15 to 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>D15</td>
</tr>
</tbody>
</table>

Domain n access permission, where n = 0 to 15. Permitted values are:

<table>
<thead>
<tr>
<th>D&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No access. Any access to the domain generates a Domain fault.</td>
</tr>
<tr>
<td>0b01</td>
<td>Client. Accesses are checked against the permission bits in the translation tables.</td>
</tr>
<tr>
<td>0b11</td>
<td>Manager. Accesses are not checked against the permission bits in the translation tables.</td>
</tr>
</tbody>
</table>

The value 0b10 is reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DACR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0011</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return DACR_NS;
    else
        return DACR;
else
    return DACR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return DACR_NS;
    else
        return DACR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        DACR_NS = R[t];
    else
        DACR_NS = R[t];
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b011</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        DACR_NS = R[t];
    else
        DACR = R[t];
else
    DACR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        DACR_NS = R[t];
    else
        DACR_NS = R[t];
else
    DACR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            DACR_S = R[t];
        else
            DACR_NS = R[t];
        endif
    endif
DBGAUTHSTATUS, Debug Authentication Status register

The DBGAUTHSTATUS characteristics are:

**Purpose**

Provides information about the state of the IMPLEMENTATION DEFINED authentication interface for debug.

**Configuration**

AArch32 System register DBGAUTHSTATUS bits [31:0] are architecturally mapped to AArch64 System register DBGAUTHSTATUS_EL1[31:0].

AArch32 System register DBGAUTHSTATUS bits [31:0] are architecturally mapped to External register DBGAUTHSTATUS_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGAUTHSTATUS are UNDEFINED.

This register is required in all implementations.

**Attributes**

DBGAUTHSTATUS is a 32-bit register.

**Field descriptions**

The DBGAUTHSTATUS bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SNID |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SID  |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | NSID |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | NSID |

**Bits [31:8]**

Reserved, RES0.

**SNID, bits [7:6]**

When FEAT_Debugv8p4 is implemented:

Secure Non-Invasive Debug.

This field has the same value as DBGAUTHSTATUS.SID.

Otherwise:

Secure Non-Invasive Debug.

<table>
<thead>
<tr>
<th>SNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>
All other values are reserved.

**SID, bits [5:4]**

Secure Invasive Debug.

<table>
<thead>
<tr>
<th>SID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSNID, bits [3:2]**

When FEAT_Debugv8p4 is implemented:

Non-secure Non-invasive debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR.NS is 0.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. EL3 is implemented or the Effective value of SCR.NS is 1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Otherwise:

Non-secure Non-Invasive Debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSID, bits [1:0]**

Non-secure Invasive Debug.

<table>
<thead>
<tr>
<th>NSID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented or the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Accessing the DBGAUTHSTATUS**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif;
    else
        return DBGAUTHSTATUS;
    endif;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif;
    else
        return DBGAUTHSTATUS;
    endif;
elsif PSTATE.EL == EL3 then
    return DBGAUTHSTATUS;
end if;
DBGBCR<n>, Debug Breakpoint Control Registers, n = 0 - 15

The DBGBCR<n> characteristics are:

**Purpose**

Holds control information for a breakpoint. Forms breakpoint n together with value register DBGVR<n>. If EL2 is implemented and this breakpoint supports Context matching, DBGVR<n> can be associated with a Breakpoint Extended Value Register DBGBXVR<n> for VMID matching.

**Configuration**

AArch32 System register DBGBCR<n> bits [31:0] are architecturally mapped to AArch64 System register DBGBCR<n>_EL1[31:0].

AArch32 System register DBGBCR<n> bits [31:0] are architecturally mapped to External register DBGBCR<n>_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGBCR<n> are UNDEFINED.

If breakpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGBCR<n> is a 32-bit register.

**Field descriptions**

The DBGBCR<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |

When the E field is zero, all the other fields in the register are ignored.

**Bits [31:24]**

Reserved, RES0.

**BT, bits [23:20]**

Breakpoint Type. Possible values are:
<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Unlinked instruction address match. <strong>DBGBVR&lt;n&gt;</strong> is the address of an instruction.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As 0b0000 with linking enabled.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Unlinked Context ID match. When FEAT_VHE is implemented, EL2 is using AArch64, and the Effective value of <strong>HCR_EL2 E2H</strong> is 1, if either the PE is executing at EL0 with <strong>HCR_EL2.TGE</strong> set to 1 or the PE is executing at EL2, then <strong>DBGBVR&lt;n&gt;</strong>.ContextID must match the <strong>CONTEXTIDR_EL2</strong> value. Otherwise, <strong>DBGBVR&lt;n&gt;</strong>.ContextID must match the <strong>CONTEXTIDR</strong> value.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010 with linking enabled.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Unlinked instruction address mismatch. <strong>DBGBVR&lt;n&gt;</strong> is the address of an instruction to be stepped.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As 0b0100 with linking enabled.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Unlinked <strong>CONTEXTIDR_EL1</strong> match. <strong>DBGBVR&lt;n&gt;</strong>.ContextID is a Context ID compared against <strong>CONTEXTIDR</strong>.</td>
</tr>
<tr>
<td>0b0111</td>
<td>As 0b0110 with linking enabled.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Unlinked VMID match. <strong>DBGBXVR&lt;n&gt;</strong>.VMID is a VMID compared against <strong>VTTBR</strong>.</td>
</tr>
<tr>
<td>0b1001</td>
<td>As 0b1000 with linking enabled.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Unlinked VMID and Context ID match. <strong>DBGBXVR&lt;n&gt;</strong>.ContextID is a Context ID compared against <strong>CONTEXTIDR</strong>, and <strong>DBGBXVR&lt;n&gt;</strong>.VMID is a VMID compared against <strong>VTTBR</strong>.</td>
</tr>
<tr>
<td>0b1011</td>
<td>As 0b1010 with linking enabled.</td>
</tr>
<tr>
<td>0b1100</td>
<td>Unlinked <strong>CONTEXTIDR_EL2</strong> match. <strong>DBGBXVR&lt;n&gt;</strong>.ContextID2 is a Context ID compared against <strong>CONTEXTIDR_EL2</strong>.</td>
</tr>
<tr>
<td>0b1101</td>
<td>As 0b1100 with linking enabled.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Unlinked Full Context ID match. <strong>DBGBVR&lt;n&gt;</strong>.ContextID is compared against <strong>CONTEXTIDR</strong>, and <strong>DBGBXVR&lt;n&gt;</strong>.ContextID2 is compared against <strong>CONTEXTIDR_EL2</strong>.</td>
</tr>
<tr>
<td>0b1111</td>
<td>As 0b1110 with linking enabled.</td>
</tr>
</tbody>
</table>

For more information on Breakpoints and their constraints, see 'Breakpoint exceptions' and 'Reserved **DBGBCR<n>**.BT values'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**LBN, bits [19:16]**

Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.

For all other breakpoint types this field is ignored and reads of the register return an **UNKNOWN** value.

This field is ignored when the value of **DBGBCR<n>**.E is 0.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**SSC, bits [15:14]**

Security state control. Determines the Security states under which a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields.

For more information, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions' and 'Reserved **DBGBCR<n>**.{SSC, HMC, PMC} values'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**HMC, bit [13]**

Higher mode control. Determines the debug perspective for deciding when a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields. For more information see the SSC, bits [15:14] description.
For more information on the operation of the SSC, HMC, and PMC fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [12:9]**

Reserved, RES0.

**BAS, bits [8:5]**

Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and Execution state.

The permitted values depend on the breakpoint type.

For Address match breakpoints, the permitted values are:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Match instruction at</th>
<th>Constraint for debuggers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0011</td>
<td>DBGBV&lt;n&gt;</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1100</td>
<td>DBGBV&lt;n&gt;+2</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1111</td>
<td>DBGBV&lt;n&gt;</td>
<td>Use for A32 instructions</td>
</tr>
</tbody>
</table>

All other values are reserved. For more information, see 'Reserved DBGBCR<n>.BAS values'.

For more information on using the BAS field in Address Match breakpoints, see 'Using the BAS field in Address Match breakpoints'.

For Address mismatch breakpoints in an AArch32 stage 1 translation regime, the permitted values are:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Step instruction at</th>
<th>Constraint for debuggers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>-</td>
<td>Use for a match anywhere breakpoint</td>
</tr>
<tr>
<td>0b0011</td>
<td>DBGBV&lt;n&gt;</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1100</td>
<td>DBGBV&lt;n&gt;+2</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1111</td>
<td>DBGBV&lt;n&gt;</td>
<td>Use for A32 instructions</td>
</tr>
</tbody>
</table>

All other values are reserved. For more information, see 'Reserved DBGBCR<n>.BAS values'.

For more information on using the BAS field in address mismatch breakpoints, see 'Using the BAS field in Address Match breakpoints'.

For Context matching breakpoints, this field is RES1 and ignored.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [4:3]**

Reserved, RES0.

**PMC, bits [2:1]**

Privilege mode control. Determines the Exception level or levels at which a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields. For more information see the DBGBCR<n>.SSC description.

For more information on the operation of the SSC, HMC, and PMC fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [0]**

Enable breakpoint **DBGBV<n>**. Possible values are:
Meaning

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Breakpoint disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Breakpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the **DBGBCR<n>**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
    elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
      Halt(DebugHalt_SoftwareAccess);
    else
      return DBGBCR[UInt(CRm<3:0>)];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
    elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
      Halt(DebugHalt_SoftwareAccess);
    else
      return DBGBCR[UInt(CRm<3:0>)];
  end
elsif PSTATE.EL == EL3 then
  if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    return DBGBCR[UInt(CRm<3:0>)];
  end
```

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    end if
else
    DBGBCR[UInt(CRm<3:0>)] = R[t];
end if
elseif PSTATE.EL == EL2 then
    if HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    end if
else
    DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        DBGBCR[UInt(CRm<3:0>)] = R[t];
    end if
else
    if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        DBGBCR[UInt(CRm<3:0>)] = R[t];
    end if
else
    DBGBCR[UInt(CRm<3:0>)] = R[t];
end if
The DBGBVR<n> characteristics are:

**Purpose**

Holds a value for use in breakpoint matching, either the virtual address of an instruction or a context ID. Forms breakpoint n together with control register DBGBCR<n>. If EL2 is implemented and this breakpoint supports Context matching, DBGBVR<n> can be associated with a Breakpoint Extended Value Register DBGBXVR<n> for VMID matching.

**Configuration**

AArch32 System register DBGBVR<n> bits [31:0] are architecturally mapped to AArch64 System register DBGBVR<n>_EL1[31:0].

AArch32 System register DBGBVR<n> bits [31:0] are architecturally mapped to External register DBGBVR<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGBVR<n> are UNDEFINED.

How this register is interpreted depends on the value of DBGBCR<n>.BT.

- When DBGBCR<n>.BT == 0b0x0x, this register holds a virtual address.
- When DBGBCR<n>.BT == 0bxx1x, this register holds a Context ID.

For other values of DBGBCR<n>.BT, this register is RES0.

Some breakpoints might not support Context ID comparison. For more information, see the description of the DBGDIDR.CTX_CMPs field.

If breakpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGBVR<n> is a 32-bit register.

**Field descriptions**

The DBGBVR<n> bit assignments are:

When DBGBCR<n>.BT == 0b0x0x:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VA[31:2] |    |    | RES0 |

VA[31:2], bits [31:2]

- Bits[31:2] of the address value for comparison.
- On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [1:0]**

Reserved, RES0.
When DBGBCR\textsubscript{n}.BT == 0b001x:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ContextID |

ContextID, bits [31:0]

Context ID value for comparison.

The value is compared against CONTEXTIDR\_EL2 when all of the following are true:

- FEAT\_VHE is implemented or FEAT\_Debugv8p2 is implemented.
- HCR\_EL2.\{E2H, TGE\} is \{1,1\}.
- The PE is executing at EL0.
- EL2 is using AArch64 and is enabled in the current Security state.

Otherwise, the value is compared against CONTEXTIDR.

On a Cold reset, this field reset to an architecturally UNKNOWN value.

When DBGBCR\textsubscript{n}.BT == 0b101x and EL2 is implemented:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ContextID |

ContextID, bits [31:0]

Context ID value for comparison against CONTEXTIDR.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR\textsubscript{n}.BT == 0bx11x, EL2 is implemented and (FEAT\_VHE is implemented or FEAT\_Debugv8p2 is implemented):

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ContextID |

ContextID, bits [31:0]

Context ID value for comparison against CONTEXTIDR.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Accessing the DBGBVR\textsubscript{n>}

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q}> <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
elif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
else
    return DBGBVR[UInt(CRm<3:0>)];
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
elif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
    return DBGBVR[UInt(CRm<3:0>)];
elif PSTATE.EL == EL3 then
    if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
    return DBGBVR[UInt(CRm<3:0>)];

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBVR[UInt(CRm<3:0>)] = R[t];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBVR[UInt(CRm<3:0>)] = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBVR[UInt(CRm<3:0>)] = R[t];
  end if;

DBGBXVR<n>, Debug Breakpoint Extended Value Registers, n = 0 - 15

The DBGBXVR<n> characteristics are:

**Purpose**

Holds a value for use in breakpoint matching, to support VMID matching. Used in conjunction with a control register DBGBCR<n> and a value register DBGBVR<n>, where EL2 is implemented and breakpoint n supports Context matching.

**Configuration**

AArch32 System register DBGBXVR<n> bits [31:0] are architecturally mapped to AArch64 System register DBGBVR<n>_EL1[63:32].

AArch32 System register DBGBXVR<n> bits [31:0] are architecturally mapped to External register DBGBVR<n>_EL1[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGBXVR<n> are UNDEFINED.

How this register is interpreted depends on the value of DBGBCR<n>.BT.

- When DBGBCR<n>.BT == 0b10xx, this register holds a VMID.
- When DBGBCR<n>.BT == 0b11xx, this register holds a Context ID.

For other values of DBGBCR<n>.BT, this register is RES0.

Accesses to this register are UNDEFINED in any of the following cases:

- Breakpoint n is not implemented.
- Breakpoint n does not support Context matching.
- EL2 is not implemented.

For more information, see the description of the DBGDIDR.CTX_CMPs field.

**Attributes**

DBGBXVR<n> is a 32-bit register.

**Field descriptions**

The DBGBXVR<n> bit assignments are:

**When DBGBCR<n>.BT == 0b10xx and EL2 is implemented:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RES0</td>
</tr>
<tr>
<td>15-8</td>
<td>VMID[15:8]</td>
</tr>
<tr>
<td>7-0</td>
<td>VMID[7:0]</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.
VMID[15:8], bits [15:8]

When FEAT_VMID16 is implemented and VTCR_EL2.VS == 1:

Extension to VMID[7:0]. See VMID[7:0] for more details.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

VMID[7:0], bits [7:0]

VMID value for comparison. The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR<n>.BT == 0b11xx and EL2 is implemented:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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</tbody>
</table>

ContextID2, bits [31:0]

When FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented:

Context ID value for comparison against CONTEXTIDR_EL2.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Accessing the DBGBXVR<n>

Accesses to this register use the following encodings:

\[
\text{MRC}\{\langle c\rangle\}\{\langle q\rangle\} \langle \text{coproc}\rangle, \{\#\}\langle \text{opc1}\rangle, \langle \text{Rt}\rangle, \langle \text{CRn}\rangle, \langle \text{CRm}\rangle, \{\#\}\langle \text{opc2}\rangle
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    end if
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
end if
elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
    return DBGBXVR[UInt(CRm<3:0>)];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    end if
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
end if
elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
    return DBGBXVR[UInt(CRm<3:0>)];
elsif PSTATE.EL == EL3 then
    if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        return DBGBXVR[UInt(CRm<3:0>)];
    end if
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
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</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0001</td>
<td>n[3:0]</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    endif
  elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBXVR[UInt(CRm<3:0>)] = R[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    endif
  elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBXVR[UInt(CRm<3:0>)] = R[t];
  endif
elsif PSTATE.EL == EL3 then
  if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
  else
    DBGBXVR[UInt(CRm<3:0>)] = R[t];
  endif
DBGCLAIMCLR, Debug CLAIM Tag Clear register

The DBGCLAIMCLR characteristics are:

**Purpose**

Used by software to read the values of the CLAIM tag bits, and to clear CLAIM tag bits to 0.

The architecture does not define any functionality for the CLAIM tag bits.

---

**Note**

CLAIM tags are typically used for communication between the debugger and target software.

---

Used in conjunction with the DBGCLAIMSET register.

**Configuration**

AArch32 System register DBGCLAIMCLR bits [31:0] are architecturally mapped to AArch64 System register DBGCLAIMCLR_EL1[31:0].

AArch32 System register DBGCLAIMCLR bits [31:0] are architecturally mapped to External register DBGCLAIMCLR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGCLAIMCLR are **UNDEFINED**.

An implementation must include eight CLAIM tag bits.

**Attributes**

DBGCLAIMCLR is a 32-bit register.

**Field descriptions**

The DBGCLAIMCLR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
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<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAZ/SBZ</td>
<td>CLAIM</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes.
Implementations must ignore writes.

**CLAIM, bits [7:0]**

Read or clear CLAIM tag bits. Reading this field returns the current value of the CLAIM tag bits.

Writing a 1 to one of these bits clears the corresponding CLAIM tag bit to 0. This is an indirect write to the CLAIM tag bits. A single write operation can clear multiple CLAIM tag bits to 0.

Writing 0 to one of these bits has no effect.

On a Cold reset, this field resets to 0.
Accessing the DBGCLAIMCLR

Accesses to this register use the following encodings:

\[
\text{MRC}\{\langle c\rangle\}{\langle q\rangle}\ <\text{coproc}>, \{\#\langle opc1\rangle, <\text{Rt}>}, <\text{CRn}>, <\text{CRm}>, \{\#\langle opc2\rangle\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} = \text{EL0}\) then
  \text{UNDEFINED};
elsif \(\text{PSTATE.EL} = \text{EL1}\) then
  if \(\text{Halted() \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} = '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD} = '1'" \&\& !\text{ELUsingAArch32(EL3)} \&\& \text{MDCR_EL3.TDA} = '1'\) then
    \text{UNDEFINED};
  elsif \(\text{EL2Enabled() \&\& !\text{ELUsingAArch32(EL2)} \&\& \text{MDCR_EL2.<TDE,TDA> != '00'}\) then
    \text{AArch64.AArch32SystemAccessTrap(EL2, 0x05)};
  elsif \(\text{EL2Enabled() \&\& !\text{ELUsingAArch32(EL2)} \&\& \text{HDCR.<TDE,TDA> != '00'}\) then
    \text{AArch32.TakeHypTrapException(0x05)};
  elsif \(\text{HaveEL(EL3)} \&\& !\text{ELUsingAArch32(EL3)} \&\& \text{MDCR_EL3.TDA = '1'}\) then
    if \(\text{Halted()} \&\& \text{EDSCR.SDD} = '1'\) then
      \text{UNDEFINED};
    else
      \text{AArch64.AArch32SystemAccessTrap(EL3, 0x05)};
    end if;
  else
    \text{return DBGCLAIMCLR};
  end if;
elsif \(\text{PSTATE.EL} = \text{EL2}\) then
  if \(\text{Halted()} \&\& \text{HaveEL(EL3)} \&\& \text{EDSCR.SDD} = '1' \&\& \text{boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD} = '1'" \&\& !\text{ELUsingAArch32(EL3)} \&\& \text{MDCR_EL3.TDA} = '1'\) then
    \text{UNDEFINED};
  elsif \(\text{HaveEL(EL3)} \&\& !\text{ELUsingAArch32(EL3)} \&\& \text{MDCR_EL3.TDA} = '1'\) then
    if \(\text{Halted()} \&\& \text{EDSCR.SDD} = '1'\) then
      \text{UNDEFINED};
    else
      \text{AArch64.AArch32SystemAccessTrap(EL3, 0x05)};
    end if;
  else
    \text{return DBGCLAIMCLR};
  end if;
elsif \(\text{PSTATE.EL} = \text{EL3}\) then
  \text{return DBGCLAIMCLR};
end if;

\[
\text{MCR}\{\langle c\rangle\}{\langle q\rangle}\ <\text{coproc}>, \{\#\langle opc1\rangle, <\text{Rt}>}, <\text{CRn}>, <\text{CRm}>, \{\#\langle opc2\rangle\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1001</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end
        else
            DBGCLAIMCLR = R[t];
        end
    elsif PSTATE.EL == EL3 then
        DBGCLAIMCLR = R[t];
    else
        DBGCLAIMCLR = R[t];
    end
else
    DBGCLAIMCLR = R[t];
elsif PSTATE.EL == EL3 then
    DBGCLAIMCLR = R[t];
DBGCLAIMSET, Debug CLAIM Tag Set register

The DBGCLAIMSET characteristics are:

**Purpose**

Used by software to set the CLAIM tag bits to 1.

The architecture does not define any functionality for the CLAIM tag bits.

**Note**

CLAIM tags are typically used for communication between the debugger and target software.

Used in conjunction with the DBGCLAIMCLR register.

**Configuration**

AArch32 System register DBGCLAIMSET bits [31:0] are architecturally mapped to AArch64 System register DBGCLAIMSET_EL1[31:0].

AArch32 System register DBGCLAIMSET bits [31:0] are architecturally mapped to External register DBGCLAIMSET_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGCLAIMSET are UNDEFINED.

An implementation must include eight CLAIM tag bits.

**Attributes**

DBGCLAIMSET is a 32-bit register.

**Field descriptions**

The DBGCLAIMSET bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     | RAZ|SBZ |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [31:8]**

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.

**CLAIM, bits [7:0]**

Set CLAIM tag bits.

This field is RAO.

Writing a 1 to one of these bits sets the corresponding CLAIM tag bit to 1. This is an indirect write to the CLAIM tag bits. A single write operation can set multiple CLAIM tag bits to 1.

Writing 0 to one of these bits has no effect.

On a Cold reset, this field resets to 0.
Accessing the DBGCLAIMSET

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>,\{<q>\}\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1000</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    else
      return DBGCLAIMSET;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
      else
        return DBGCLAIMSET;
  elsif PSTATE.EL == EL3 then
    return DBGCLAIMSET;

MRC\{<c>,\{<q>\}\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    DBGCLAIMSET = R[t];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    DBGCLAIMSET = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  DBGCLAIMSET = R[t];
else
  DBGCLAIMSET = R[t];
end if;
DBGDCCINT, DCC Interrupt Enable Register

The DBGDCCINT characteristics are:

**Purpose**

Enables interrupt requests to be signaled based on the DCC status flags.

**Configuration**

AArch32 System register DBGDCCINT bits [31:0] are architecturally mapped to AArch64 System register MDCCINT_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDCCINT are **UNDEFINED**.

**Attributes**

DBGDCCINT is a 32-bit register.

**Field descriptions**

The DBGDCCINT bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>RX</td>
<td></td>
<td>DCC interrupt request enable control for DTRRX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.</td>
</tr>
<tr>
<td>29</td>
<td>TX</td>
<td></td>
<td>DCC interrupt request enable control for DTRTX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.</td>
</tr>
<tr>
<td>28</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>RX</td>
<td></td>
<td></td>
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<tr>
<td>20</td>
<td>RX</td>
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<tr>
<td>19</td>
<td>RX</td>
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<tr>
<td>18</td>
<td>RX</td>
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<tr>
<td>17</td>
<td>RX</td>
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<td></td>
</tr>
<tr>
<td>16</td>
<td>RX</td>
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<td></td>
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<tr>
<td>15</td>
<td>RX</td>
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<tr>
<td>14</td>
<td>RX</td>
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<tr>
<td>13</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RX</td>
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<td></td>
</tr>
<tr>
<td>6</td>
<td>RX</td>
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<td></td>
</tr>
<tr>
<td>5</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RES0</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RES0</td>
<td>RX</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bit [31]**

Reserved, RES0.

**RX, bit [30]**

DCC interrupt request enable control for DTRRX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.

<table>
<thead>
<tr>
<th>RX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No interrupt request generated by DTRRX.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupt request will be generated on RXfull == 1.</td>
</tr>
</tbody>
</table>

If legacy COMMRX and COMMTX signals are implemented, then these are not affected by the value of this bit.

On a Warm reset, this field resets to 0.

**TX, bit [29]**

DCC interrupt request enable control for DTRTX. Enables a common COMMIRQ interrupt request to be signaled based on the DCC status flags.

<table>
<thead>
<tr>
<th>TX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No interrupt request generated by DTRTX.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupt request will be generated on TXfull == 0.</td>
</tr>
</tbody>
</table>

If legacy COMMRX and COMMTX signals are implemented, then these are not affected by the value of this bit.

On a Warm reset, this field resets to 0.
Bits [28:0]

Reserved, RES0.

**Accessing the DBGDCCINT**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}\}, <\text{Rt}>, <CRn>, <CRm>{, \{#<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b00</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b00</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDA != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDA != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    elsif EL2Enabled() && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endelse
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    elsif EL2Enabled() && ELUsingAArch32(EL3) && SDCR.TDA != '00' then
        AArch32.TakeHypTrapException(0x05);
    elseif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    elsif EL2Enabled() && ELUsingAArch32(EL3) && SDCR.TDA != '00' then
        AArch32.TakeMonitorTrapException();
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    else
        return DBGDCCINT;
    endelse
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDA != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDA != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    elsif EL2Enabled() && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endelse
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endelse
    else
        return DBGDCCINT;
    endelse
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return DBGDCCINT;
    endelse
else
    return DBGDCCINT;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDA != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA != '00' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    elsif PSTATE.EL == EL2 then
        if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        else
            DBGDCCINT = R[t];
        endif
    elsif PSTATE.EL == EL3 then
        if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        else
            DBGDCCINT = R[t];
        endif
    else
        DBGDCCINT = R[t];
    endif
else
    DBGDCCINT = R[t];
endif
DBGDEVID, Debug Device ID register 0

The DBGDEVID characteristics are:

**Purpose**

Adds to the information given by the DBGDIDR by describing other features of the debug implementation.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDEVID are UNDEFINED.

This register is required in all implementations.

**Attributes**

DBGDEVID is a 32-bit register.

**Field descriptions**

The DBGDEVID bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>CIDMask</td>
</tr>
<tr>
<td>27-24</td>
<td>AuxRegs</td>
</tr>
<tr>
<td>23-20</td>
<td>DoubleLock</td>
</tr>
<tr>
<td>19-16</td>
<td>VirtExtns</td>
</tr>
<tr>
<td>15-12</td>
<td>VectorCatch</td>
</tr>
<tr>
<td>11-8</td>
<td>BPAddrMask</td>
</tr>
<tr>
<td>7-4</td>
<td>WPAddrMask</td>
</tr>
<tr>
<td>3-0</td>
<td>PCSample</td>
</tr>
</tbody>
</table>

**CIDMask, bits [31:28]**

Indicates the level of support for the Context ID matching breakpoint masking capability. Defined values are:

<table>
<thead>
<tr>
<th>CIDMask</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Context ID masking is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Context ID masking is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved. The value of this for Armv8 is 0b0000.

**AuxRegs, bits [27:24]**

Indicates support for Auxiliary registers. Permitted values for this field are:

<table>
<thead>
<tr>
<th>AuxRegs</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for External Debug Auxiliary Control Register, EDACR.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**DoubleLock, bits [23:20]**

OS Double Lock implemented. Defined values are:

<table>
<thead>
<tr>
<th>DoubleLock</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>OS Double Lock is not implemented. DBGOSDLR is RAZ/WI.</td>
</tr>
<tr>
<td>0b0001</td>
<td>OS Double Lock is implemented. DBGOSDLR is RW.</td>
</tr>
</tbody>
</table>

FEAT_DoubleLock implements the functionality identified by the value 0b0001.
All other values are reserved.

**VirtExtns, bits [19:16]**

Indicates whether EL2 is implemented. Defined values are:

<table>
<thead>
<tr>
<th>VirtExtns</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL2 is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL2 is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**VectorCatch, bits [15:12]**

Defines the form of Vector Catch exception implemented. Defined values are:

<table>
<thead>
<tr>
<th>VectorCatch</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Address matching Vector Catch exception implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Exception matching Vector Catch exception implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**BPAddrMask, bits [11:8]**

Indicates the level of support for the instruction address matching breakpoint masking capability. Defined values are:

<table>
<thead>
<tr>
<th>BPAddrMask</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Breakpoint address masking might be implemented. If not implemented, DBGBCR&lt;8:4&gt; is RAZ/WI.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Breakpoint address masking is implemented.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Breakpoint address masking is not implemented. DBGBCR&lt;8:4&gt; is RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved. The value of this for Armv8 is 0b1111.

**WPAddrMask, bits [7:4]**

Indicates the level of support for the data address matching watchpoint masking capability. Defined values are:

<table>
<thead>
<tr>
<th>WPAddrMask</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Watchpoint address masking might be implemented. If not implemented, DBGWCR&lt;7:4&gt;.MASK (Address mask) is RAZ/WI.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Watchpoint address masking is implemented.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Watchpoint address masking is not implemented. DBGWCR&lt;7:4&gt;.MASK (Address mask) is RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved. The value of this for Armv8 is 0b0001.

**PCSample, bits [3:0]**

Indicates the level of PC Sample-based Profiling support using external debug registers. Defined values are:

<table>
<thead>
<tr>
<th>PCSample</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PC Sample-based Profiling Extension is not implemented in the external debug registers space.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Only EDPICR and EDCICR are implemented. This option is only permitted if EL3 and EL2 are not implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>EDPICR, EDCICR, and EDWICR are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

When FEAT_PCSRv8p2 is implemented, the only permitted value is 0b0000.
Note

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors register space, as indicated by the value of PMDEVID PCSample.

Accessing the DBGDEVID

Accesses to this register use the following encodings:

MRC{<c>{<q}> }<coproc>,{<opcl>, <Rt>, <CRn>, <CRm>{, {#}<opc2}>

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TDA != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDA != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDEVID;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDEVID;
  end
elsif PSTATE.EL == EL3 then
  return DBGDEVID;
DBGDEVID1, Debug Device ID register 1

The DBGDEVID1 characteristics are:

**Purpose**

Adds to the information given by the DBGDIDR by describing other features of the debug implementation.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDEVID1 are **UNDEFINED**.

This register is required in all implementations.

**Attributes**

DBGDEVID1 is a 32-bit register.

**Field descriptions**

The DBGDEVID1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
</tr>
<tr>
<td><strong>RES0</strong></td>
<td></td>
<td>PCSROffset</td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, **RES0**.

**PCSROffset, bits [3:0]**

This field indicates the offset applied to PC samples returned by reads of **EDPCSR**. Permitted values of this field in Armv8 are:

<table>
<thead>
<tr>
<th>PCSROffset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td><strong>EDPCSR</strong> is not implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td><strong>EDPCSR</strong> implemented. Samples have no offset applied and do not sample the instruction set state in AArch32 state.</td>
</tr>
</tbody>
</table>

When **FEAT_PCSRv8p2** is implemented, the only permitted value is 0b0000.

**Note**

**FEAT_PCSRv8p2** implements the PC Sample-based Profiling Extension in the Performance Monitors register space, as indicated by the value of **PMDEVID**. **PCSample**.

**Accessing the DBGDEVID1**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elseif EL2Enabled() && EDSCR.SDD == '1' then
    UNDEFINED;
  return DBGDEVID1;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elseif HaveEL(EL3) && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    return DBGDEVID1;
elsif PSTATE.EL == EL3 then
  return DBGDEVID1;
DBGDEVID2, Debug Device ID register 2

The DBGDEVID2 characteristics are:

**Purpose**

Reserved for future descriptions of features of the debug implementation.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDEVID2 are UNDEFINED.

**Attributes**

DBGDEVID2 is a 32-bit register.

**Field descriptions**

The DBGDEVID2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Reserved, RES0.

**Accessing the DBGDEVID2**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0000</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGDEVID2;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGDEVID2;
  end if;
elsif PSTATE.EL == EL3 then
  return DBGDEVID2;
The DBGIDR characteristics are:

**Purpose**

Specifies which version of the Debug architecture is implemented, and some features of the debug implementation.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGIDR are **UNDEFINED**.

If EL1 cannot use AArch32 then the implementation of this register is **OPTIONAL** and deprecated.

**Attributes**

DBGIDR is a 32-bit register.

**Field descriptions**

The DBGIDR bit assignments are:

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15</th>
<th>14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>WRPs</td>
<td>BRPs</td>
</tr>
</tbody>
</table>

**WRPs, bits [31:28]**

The number of watchpoints implemented, minus 1.

Permitted values of this field are from 0b0001 for 2 implemented watchpoints, to 0b1111 for 16 implemented watchpoints.

The value of 0b0000 is reserved.

If AArch64 is implemented, this field has the same value as **ID_AA64DFR0_EL1**.WRPs.

**BRPs, bits [27:24]**

The number of breakpoints implemented, minus 1.

Permitted values of this field are from 0b0001 for 2 implemented breakpoint, to 0b1111 for 16 implemented breakpoints.

The value of 0b0000 is reserved.

If AArch64 is implemented, this field has the same value as **ID_AA64DFR0_EL1**.BRPs.

**CTX_CMPs, bits [23:20]**

The number of breakpoints that can be used for Context matching, minus 1.

Permitted values of this field are from 0b0000 for 1 Context matching breakpoint, to 0b1111 for 16 Context matching breakpoints.

The Context matching breakpoints must be the highest addressed breakpoints. For example, if six breakpoints are implemented and two are Context matching breakpoints, they must be breakpoints 4 and 5.

If AArch64 is implemented, this field has the same value as **ID_AA64DFR0_EL1**.CTX_CMPs.
**Version, bits [19:16]**

The Debug architecture version. Defined values are:

<table>
<thead>
<tr>
<th>Version</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv6, v6 Debug architecture.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv6, v6.1 Debug architecture.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv7, v7 Debug architecture, with baseline CP14 registers implemented.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv7, v7 Debug architecture, with all CP14 registers implemented.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv7, v7.1 Debug architecture.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv8, v8 Debug architecture.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv8.1, v8 Debug architecture, with Virtualization Host Extensions.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Armv8.2, v8.2 Debug architecture.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Armv8.4, v8.4 Debug architecture.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In any Armv8 implementation, the values 0b0001, 0b0010, 0b0011, 0b0100, and 0b0101 are not permitted.

- If FEAT_VHE is not implemented, the only permitted value is 0b0110.
- In an Armv8.0 implementation, the value 0b1000 or higher is not permitted.

**Bit [15]**

Reserved, RES1.

**nSUHD_imp, bit [14]**

In Armv7-A, was Secure User Halting Debug not implemented.

The value of this bit must match the value of the SE_imp bit.

**Bit [13]**

Reserved, RES0.

**SE_imp, bit [12]**

EL3 implemented. The meanings of the values of this bit are:

<table>
<thead>
<tr>
<th>SE_imp</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL3 not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL3 implemented.</td>
</tr>
</tbody>
</table>

The value of this bit must match the value of the nSUHD_imp bit.

**Bits [11:0]**

Reserved, RES0.

**Accessing the DBGDIDR**

Arm deprecates any access to this register from EL0.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if Halted() & HaveEL(EL3) & & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) & & MDSCR_EL1.TDCC == '1' then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x05);
    end
  elsif EL2Enabled() & & DBGDSExt.UDCCdis == '1' then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end
  elsif EL2Enabled() & & !ELUsingAArch32(EL2) & (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDA> != '00') then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() & & !ELUsingAArch32(EL2) & (HCR_EL2.TGE == '1' || HDCR.<TDE,TDA> != '00') then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    if Halted() & & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDIDR;
  end
elsif PSTATE.EL == EL1 then
  if Halted() & & HaveEL(EL3) & & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    if Halted() & & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDIDR;
  end
elsif PSTATE.EL == EL2 then
  if Halted() & & HaveEL(EL3) & & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) & & !ELUsingAArch32(EL3) & & MDCR_EL3.TDA == '1' then
    if Halted() & & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDIDR;
  end
elsif PSTATE.EL == EL3 then
  return DBGDIDR;

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
DBGDRAR, Debug ROM Address Register

The DBGDRAR characteristics are:

**Purpose**

Defines the base physical address of a 4KB-aligned memory-mapped debug component, usually a ROM table that locates and describes the memory-mapped debug components in the system. Armv8 deprecates any use of this register.

**Configuration**

AArch32 System register DBGDRAR bits [63:0] are architecturally mapped to AArch64 System register MDRAR_EL1[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDRAR are **UNDEFINED**.

DBGDRAR is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, bits [31:0] are read.

If EL1 cannot use AArch32 then the implementation of this register is **OPTIONAL** and deprecated.

**Attributes**

DBGDRAR is a 64-bit register.

**Field descriptions**

The DBGDRAR bit assignments are:

|   63  |   62  |   61  |   60  |   59  |   58  |   57  |   56  |   55  |   54  |   53  |   52  |   51  |   50  |   49  |   48  |   47  |   46  |   45  |   44  |   43  |   42  |   41  |   40  |   39  |   38  |   37  |   36  |   35  |   34  |   33  |   32  |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| RES0  | RES0  | ROMADDR[47:12] | RES0 | Valid |
| 31    | 30    | 29    | 28    | 27    | 26    | 25    | 24    | 23    | 22    | 21    | 20    | 19    | 18    | 17    | 16    | 15    | 14    | 13    | 12    | 11    | 10    |  9   |  8   |  7   |  6   |  5   |  4   |  3   |  2   |  1   |  0   |

**Bits [63:48]**

Reserved, RES0.

**ROMADDR[47:12], bits [47:12]**

Bits[47:12] of the ROM table physical address.

If the physical address size in bits (PAsize) is less than 48 then the register bits corresponding to ROMADDR [47:PAsize] are RES0.

Bits [11:0] of the ROM table physical address are zero.

Arm strongly recommends that bits ROMADDR[(PAsize-1):32] are zero in any system that supports AArch32 at the highest implemented Exception level.

In an implementation that includes EL3, ROMADDR is an address in Non-secure memory. It is **IMPLEMENTATION DEFINED** whether the ROM table is also accessible in Secure memory.

If DBGDRAR.Valid == 0b00, then this field is **UNKNOWN**.
 Bits [11:2]  
Reserved, RES0.

Valid, bits [1:0]  
This field indicates whether the ROM Table address is valid.

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>ROM Table address is not valid. Software must ignore ROMADDR.</td>
</tr>
<tr>
<td>0b11</td>
<td>ROM Table address is valid.</td>
</tr>
</tbody>
</table>

Other values are reserved.

Accessing the DBGDRAR

Accesses to this register use the following encodings:

MRC{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then UNDEFINED;
    elsif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x05);
        end if
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
            AArch32.TakeHypTrapException(0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end if
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end if
        else
            return DBGDRAR<31:0>;
        end if
    elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
            AArch32.TakeHypTrapException(0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end if
        else
            return DBGDRAR<31:0>;
        end if
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end if
        else
            return DBGDRAR<31:0>;
        end if
    elsif PSTATE.EL == EL3 then
        return DBGDRAR<31:0>;
    end if

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b0001</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x0C);
        end if;
    elsif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        end if;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDRA> != '00') then
        AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
    end if;
else
    return DBGDRAR;
end if;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
        AArch32.TakeHypTrapException(0x0C);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
        end if;
    else
        return DBGDRAR;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
        end if;
    else
        return DBGDRAR;
    end if;
elsif PSTATE.EL == EL3 then
    return DBGDRAR;
end if;
The DBGDSAR characteristics are:

**Purpose**

In earlier versions of the Arm Architecture, this register defines the offset from the base address defined in DBGDRAR of the physical base address of the debug registers for the PE. Armv8 deprecates any use of this register.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDSAR are **undefined**.

DBGDSAR is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, bits [31:0] are read.

If EL1 cannot use AArch32 then the implementation of this register is **optional** and deprecated.

**Attributes**

DBGDSAR is a 64-bit register.

**Field descriptions**

The DBGDSAR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | RAZ |

Bits [63:2]

Reserved, RES0.

Bits [1:0]

Reserved, RAZ.

This field indicates whether the debug self address offset is valid. For ARMv8, this field is always 0b00, the offset is not valid.

**Accessing the DBGDSAR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && MDBSCR EL1.TDCC == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x05);
    end
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x05);
  end
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x05);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
  AArch32.TakeHypTrapException(0x05);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  end
else
  return DBGDSAR<31:0>;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDSAR<31:0>;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  else
    return DBGDSAR<31:0>;
elsif PSTATE.EL == EL3 then
  return DBGDSAR<31:0>;

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b0010</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x0C);
        endif
    elseif EL2Enabled() && MDGDSRExt.UDCCdis == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
        elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        endif
    elseif EL2Enabled() && ELUsingAArch32(EL2) && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDRA> != '00') then
        AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
    elseif EL2Enabled() && HCR_EL2.TGE == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
        endif
    else
        return DBGDSAR;
    endif
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
        elseif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
            AArch32.TakeHypTrapException(0x0C);
        elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
            endif
        else
            return DBGDSAR;
        endif
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDRA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x0C);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDRA> != '00' then
        AArch32.TakeHypTrapException(0x0C);
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
        endif
    else
        return DBGDSAR;
    endif
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDSCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x0C);
        endif
    else
        return DBGDSAR;
    endif
elseif PSTATE.EL == EL3 then
    return DBGDSAR;
The DBGDSCRext characteristics are:

**Purpose**
Main control register for the debug implementation.

**Configuration**
AArch32 System register DBGDSCRext bits [31:0] are architecturally mapped to AArch64 System register MDSCR_EL1[31:0].

AArch32 System register DBGDSCRext bits [15:2] are architecturally mapped to AArch32 System register DBGDSRint[15:2].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDSCRext are UNDEFINED.

This register is required in all implementations.

**Attributes**
DBGDSCRext is a 32-bit register.

**Field descriptions**
The DBGDSCRext bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TFO | RXfull | TXfull | RES0 | RXOTXU | RES0 | INTdis | TDA | RES0 | SC2 | NS | SPNIdis | SPiDdis | MDBGen | HDE | RES0 | UDCCdis | RES0 | ERR | MOE | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 |

**TFO, bit [31]**
When FEAT_TRF is implemented:
Trace Filter override. Used for save/restore of EDSCR.TFO.

When the OS Lock is unlocked, DBGOSLSR.OSLK == 0, software must treat this bit as UNK/SBZP.

When the OS Lock is locked, DBGOSLSR.OSLK == 1, this bit holds the value of EDSCR.TFO. Reads and writes of this bit are indirect accesses to EDSCR.TFO.

Accessing this field has the following behavior:
- When DBGOSLSR.OSLK == 1, access to this field is RW.
- When DBGOSLSR.OSLK == 0, access to this field is RO.

**RXfull, bit [30]**
DTRRX full. Used for save/restore of EDSCR.RXfull.
When `DBGOSLSR.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `DBGOSLSR.OSLK == 1`, this bit holds the value of `EDSCR.RXfull`. Reads and writes of this bit are indirect accesses to `EDSCR.RXfull`.

Arm deprecates use of this bit other than for save/restore. Use `DBGDSCRint` to access the DTRRX full status.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `DBGOSLSR.OSLK == 1`, access to this field is **RW**.
- When `DBGOSLSR.OSLK == 0`, access to this field is **RO**.

**TXfull, bit [29]**

DTRTX full. Used for save/restore of `EDSCR.TXfull`.

When `DBGOSLSR.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `DBGOSLSR.OSLK == 1`, this bit holds the value of `EDSCR.TXfull`. Reads and writes of this bit are indirect accesses to `EDSCR.TXfull`.

Arm deprecates use of this bit other than for save/restore. Use `DBGDSCRint` to access the DTRTX full status.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `DBGOSLSR.OSLK == 1`, access to this field is **RW**.
- When `DBGOSLSR.OSLK == 0`, access to this field is **RO**.

**Bit [28]**

Reserved, RES0.

**RXO, bit [27]**

Used for save/restore of `EDSCR.RXO`.

When `DBGOSLSR.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `DBGOSLSR.OSLK == 1`, this bit holds the value of `EDSCR.RXO`. Reads and writes of this bit are indirect accesses to `EDSCR.RXO`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `DBGOSLSR.OSLK == 1`, access to this field is **RW**.
- When `DBGOSLSR.OSLK == 0`, access to this field is **RO**.

**TXU, bit [26]**

Used for save/restore of `EDSCR.TXU`.

When `DBGOSLSR.OSLK == 0`, software must treat this bit as UNK/SBZP.

When `DBGOSLSR.OSLK == 1`, this bit holds the value of `EDSCR.TXU`. Reads and writes of this bit are indirect accesses to `EDSCR.TXU`.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When `DBGOSLSR.OSLK == 1`, access to this field is **RW**.
- When `DBGOSLSR.OSLK == 0`, access to this field is **RO**.
Bits [25:24]  
Reserved, RES0.

INTdis, bits [23:22]  
Used for save/restore of EDSCR.INTdis.  
When DBGOSLR.OSLK == 0, this field is RO, and software must treat it as UNK/SBZP.  
When DBGOSLR.OSLK == 1, this field is RW and holds the value of EDSCR.INTdis. Reads and writes of this field are indirect accesses to EDSCR.INTdis.  
The architected behavior of this field determines the value it returns after a reset.  
Accessing this field has the following behavior:  
• When DBGOSLR.OSLK == 1, access to this field is RW.  
• When DBGOSLR.OSLK == 0, access to this field is RO.

TDA, bit [21]  
Used for save/restore of EDSCR.TDA.  
When DBGOSLR.OSLK == 0, software must treat this bit as UNK/SBZP.  
When DBGOSLR.OSLK == 1, this bit holds the value of EDSCR.TDA. Reads and writes of this bit are indirect accesses to EDSCR.TDA.  
The architected behavior of this field determines the value it returns after a reset.  
Accessing this field has the following behavior:  
• When DBGOSLR.OSLK == 1, access to this field is RW.  
• When DBGOSLR.OSLK == 0, access to this field is RO.

Bit [20]  
Reserved, RES0.

SC2, bit [19]  
When FEAT_PCSRv8 is implemented, FEAT_VHE is implemented and FEAT_PCSRv8p2 is not implemented:  
Used for save/restore of EDSCR.SC2.  
When DBGOSLR.OSLK == 0, software must treat this bit as UNK/SBZP.  
When DBGOSLR.OSLK == 1, this bit holds the value of EDSCR.SC2. Reads and writes of this bit are indirect accesses to EDSCR.SC2.  
Accessing this field has the following behavior:  
• When DBGOSLR.OSLK == 1, access to this field is RW.  
• When DBGOSLR.OSLK == 0, access to this field is RO.

Otherwise:  
Reserved, RES0.

NS, bit [18]  
Non-secure status. Returns the inverse of IsSecure().
Arm deprecates use of this field.

Access to this field is RO.

**SPNIDdis, bit [17]**

*When EL3 is implemented:*

Secure privileged profiling disabled status bit.

<table>
<thead>
<tr>
<th>SPNIDdis</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Profiling allowed in Secure privileged modes.</td>
</tr>
<tr>
<td>0b1</td>
<td>Profiling prohibited in Secure privileged modes.</td>
</tr>
</tbody>
</table>

This field reads as 0 if any of the following applies, and reads as 1 otherwise:

- FEAT_Debugv8p2 is not implemented and ExternalSecureNoninvasiveDebugEnabled() returns TRUE.
- EL3 is using AArch32 and the value of SDCR.SPME is 1.
- EL3 is using AArch64 and the value of MDCR_EL3.SPME is 1.

Arm deprecates use of this field.

Access to this field is RO.

**Otherwise:**

Reserved, RES0.

**SPIDdis, bit [16]**

*When EL3 is implemented:*

Secure privileged AArch32 invasive self-hosted debug disabled status bit. The value of this bit depends on the value of SDCR.SPD and the pseudocode function AArch32.SelfHostedSecurePrivilegedInvasiveDebugEnabled().

<table>
<thead>
<tr>
<th>SPIDdis</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Self-hosted debug enabled in Secure privileged AArch32 modes.</td>
</tr>
<tr>
<td>0b1</td>
<td>Self-hosted debug disabled in Secure privileged AArch32 modes.</td>
</tr>
</tbody>
</table>

This bit reads as 1 if any of the following is true and reads as 0 otherwise:

- EL3 is using AArch32 and SDCR.SPD has the value 0b10.
- EL3 is using AArch64 and MDCR_EL3.SPD32 has the value 0b10.
- EL3 is using AArch32, SDCR.SPD has the value 0b00, and AArch32.SelfHostedSecurePrivilegedInvasiveDebugEnabled() returns FALSE.
- EL3 is using AArch64, MDCR_EL3.SPD32 has the value 0b00, and AArch32.SelfHostedSecurePrivilegedInvasiveDebugEnabled() returns FALSE.

Arm deprecates use of this field.

Access to this field is RO.

**Otherwise:**

Reserved, RES0.

**MDBGen, bit [15]**

Monitor debug events enable. Enable Breakpoint, Watchpoint, and Vector Catch exceptions.
### MDBGen

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

### HDE, bit [14]

Used for save/restore of EDSCR.HDE.

When DBGOSLSR.OSLK == 0, software must treat this bit as UNK/SBZP.

When DBGOSLSR.OSLK == 1, this bit holds the value of EDSCR.HDE. Reads and writes of this bit are indirect accesses to EDSCR.HDE.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:

- When DBGOSLSR.OSLK == 1, access to this field is RW.
- When DBGOSLSR.OSLK == 0, access to this field is RO.

### Bit [13]

Reserved, RES0.

### UDCCdis, bit [12]

Traps EL0 accesses to the DCC registers to Undefined mode.

<table>
<thead>
<tr>
<th>UDCCdis</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 accesses to the DBGDSCRint, DBGDTRRXint, DBGDTRTXint,DBGDIDR, DBGDSAR, and DBGDRAR are trapped to Undefined mode.</td>
</tr>
</tbody>
</table>

Note

All accesses to these registers are trapped, including LDC and STC accesses to DBGDTRTXint and DBGDTRRXint, and MRRC accesses to DBGDSAR and DBGDRAR.

Traps of EL0 accesses to the DBGDTRRXint and DBGDTRTXint are ignored in Debug state.

On a Warm reset, this field resets to 0.

### Bits [11:7]

Reserved, RES0.

### ERR, bit [6]

Used for save/restore of EDSCR.ERR.

When DBGOSLSR.OSLK == 0, software must treat this bit as UNK/SBZP.

When DBGOSLSR.OSLK == 1, this bit holds the value of EDSCR.ERR. Reads and writes of this bit are indirect accesses to EDSCR.ERR.

The architected behavior of this field determines the value it returns after a reset.

Accessing this field has the following behavior:
• When DBGOSLSR.OSLK == 1, access to this field is **RW**.
• When DBGOSLSR.OSLK == 0, access to this field is **RO**.

**MOE, bits [5:2]**

Method of Entry for debug exception. When a debug exception is taken to an Exception level using AArch32, this field is set to indicate the event that caused the exception:

<table>
<thead>
<tr>
<th>MOE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Breakpoint.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Software breakpoint (BKPT) instruction.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Vector catch.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Watchpoint.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [1:0]**

Reserved, **RES0**.

**Accessing the DBGDSCRext**

Individual fields within this register might have restricted accessibility when the OS lock is unlocked, **DBGOSLSR.OSLK == 0**. See the field descriptions for more detail.

Accesses to this register use the following encodings:

```plaintext
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && EDSCR.SDD == '1' then
    UNDEFINED;
elsif EL2Enabled() && EDSCR.SDD == '1' && MDCR_EL2.TDA == '1' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x05);
else
  return DBGDSCRext;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && EDSCR.SDD == '1' then
    UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x05);
else
  return DBGDSCRext;
elsif PSTATE.EL == EL3 then
  return DBGDSCRext;
```

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if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  end if;
elsif PSTATE.EL == EL3 then
  DBGDSCRext = R[t];
elsif PSTATE.EL == EL4 then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  end if;
elsif PSTATE.EL == EL5 then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  end if;
else
  DBGDSCRext = R[t];
end if;
The DBGDSCRint characteristics are:

**Purpose**

Main control register for the debug implementation. This is an internal, read-only view.

**Configuration**

AArch32 System register DBGDSCRint bits [30:29] are architecturally mapped to AArch64 System register MDCCSR_EL0[30:29].

AArch32 System register DBGDSCRint bits [15:2] are architecturally mapped to AArch32 System register DBGDSCRext[15:2].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDSCRint are **UNDEFINED**.

This register is required in all implementations.

DBGDSCRint.\{NS, SPNIDdis, SPIDdis, MDBGen, UDCCdis, MOE\} are **UNKNOWN** when the register is accessed at EL0. However, although these values are not accessible at EL0 by instructions that are neither **UNPREDICTABLE** nor return **UNKNOWN** values, it is permissible for an implementation to return the values of DBGDSCRext.\{NS, SPNIDdis, SPIDdis, MDBGen, UDCCdis, MOE\} for these fields at EL0.

It is also permissible for an implementation to return the same values as defined for a read of DBGDSCRint at EL1 or above. (This is the case even if the implementation does not support AArch32 at EL1 or above.)

**Attributes**

DBGDSCRint is a 32-bit register.

**Field descriptions**

The DBGDSCRint bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES0 | RXfull | TXfull | RES0 | NS | SPNIDdis | SPIDdis | MDBGen | RES0 | UDCCdis | RES0 | MOE | RES0 |

**Bit [31]**

Reserved, RES0.

**RXfull, bit [30]**

DTRRX full. Read-only view of the equivalent bit in the EDSCR.

**TXfull, bit [29]**

DTRTX full. Read-only view of the equivalent bit in the EDSCR.

**Bits [28:19]**

Reserved, RES0.
NS, bit [18]
Non-secure status.
Read-only view of the equivalent bit in the DBGDSCR. Arm deprecates use of this field.

SPNIdis, bit [17]
Secure privileged non-invasive debug disable.
Read-only view of the equivalent bit in the DBGDSCR. Arm deprecates use of this field.

SPIDdis, bit [16]
Secure privileged invasive debug disable.
Read-only view of the equivalent bit in the DBGDSCR. Arm deprecates use of this field.

MDBGen, bit [15]
Monitor debug events enable.
Read-only view of the equivalent bit in the DBGDSCR.

Bits [14:13]
Reserved, RES0.

UDCCdis, bit [12]
User mode access to Debug Communications Channel disable.
Read-only view of the equivalent bit in the DBGDSCR. Arm deprecates use of this field.

Bits [11:6]
Reserved, RES0.

MOE, bits [5:2]
Method of Entry for debug exception. When a debug exception is taken to an Exception level using AArch32, this field is set to indicate the event that caused the exception:

<table>
<thead>
<tr>
<th>MOE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Breakpoint</td>
</tr>
<tr>
<td>0b0001</td>
<td>Software breakpoint (BKPT) instruction</td>
</tr>
<tr>
<td>0b0101</td>
<td>Vector catch</td>
</tr>
<tr>
<td>0b1010</td>
<td>Watchpoint</td>
</tr>
</tbody>
</table>

Read-only view of the equivalent bit in the DBGDSCR.

Bits [1:0]
Reserved, RES0.

**Accessing the DBGDSCR**

Accesses to this register use the following encodings:
MRC{<c>{<q>}}<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>} |

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x05);
    end if;
  elsif !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    else
      UNDEFINED;
    end if;
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x05);
  end if;
elsif ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
    AArch32.TakeHypTrapException(0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGDSCRint;
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
    AArch32.TakeHypTrapException(0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGDSCRint;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
    AArch32.TakeHypTrapException(0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE>TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGDSCRint;
  end if;
AArch64.AArch32SystemAccessTrap(EL3, 0x05);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif;
elsif !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  endif;
else
  return DBGDSCRint;
endif;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
  priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif;
elsif !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  endif;
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x05);
  endif;
else
  return DBGDSCRint;
endif;
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return DBGDSCRint;
  endif;
else
  return DBGDSCRint;
endif;
The DBGDTRRXext characteristics are:

**Purpose**

Used for save/restore of DBGDTRRXint. It is a component of the Debug Communications Channel.

**Configuration**

AArch32 System register DBGDTRRXext bits [31:0] are architecturally mapped to AArch64 System register OSDTRRX_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDTRRXext are UNDEFINED.

**Attributes**

DBGDTRRXext is a 32-bit register.

**Field descriptions**

The DBGDTRRXext bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **Update DTRRX without side-effect** |

**Bits [31:0]**

Update DTRRX without side-effect.

Writes to this register update the value in DTRRX and do not change RXfull.

Reads of this register return the last value written to DTRRX and do not change RXfull.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGDTRRXext**

Arm deprecates reads and writes of DBGDTRRXext through the System register interface when the OS Lock is unlocked, DBGOSLSR.OSLK == 0.

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>}, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2}>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        return DBGDTRRXext;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        return DBGDTRRXext;
    end if
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return DBGDTRRXext;
    end if
else
    return DBGDTRRXext;
end if
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
    AArch32.TakeHypTrapException(0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDA != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL3Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    DBGDTRRXext = R[t];
end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    DBGDTRRXext = R[t];
end if;
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
    AArch32.TakeMonitorTrapException();
  else
    DBGDTRRXext = R[t];
end if;
else
  DBGDTRRXext = R[t];
end if;
DBGDTRRXnt, Debug Data Transfer Register, Receive

The DBGDTRRXnt characteristics are:

**Purpose**

Transfers data from an external debugger to the PE. For example, it is used by a debugger transferring commands and data to a debug target. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communications Channel.

**Configuration**

AArch32 System register DBGDTRRXnt bits [31:0] are architecturally mapped to AArch64 System register DBGDTRRX_EL0[31:0].

AArch32 System register DBGDTRRXnt bits [31:0] are architecturally mapped to External register DBGDTRRX_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDTRRXnt are UNDEFINED.

**Attributes**

DBGDTRRXnt is a 32-bit register.

**Field descriptions**

The DBGDTRRXnt bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [31:0]**

Update DTRRX.

Reads of this register:

- If RXfull is set to 1, return the last value written to DTRRX.
- If RXfull is set to 0, return an UNKNOWN value.

After the read, RXfull is cleared to 0.

For the full behavior of the Debug Communications Channel, see ‘The Debug Communication Channel and Instruction Transfer Register’.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGDTRRXnt**

Data can be stored to memory from this register using STC.

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

| coproc | opc1 | CRn | CRm | opc2 |
if Halted() then
    return DBGDTRRXint;
elsif PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x05);
        end if;
    elsif ELUsingAArch32(EL1) && DBGDSCRext.UDCCdis == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        else
            UNDEFINED;
        end if;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && SDCR.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        else
            return DBGDTRRXint;
        end if;
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
            AArch32.TakeHypTrapException(0x05);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
            AArch32.TakeHypTrapException(0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        else
            return DBGDTRRXint;
        end if;
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        else
            return DBGDTRRXint;
        end if;
    elsif PSTATE.EL == EL3 then
        if PSTATE.M != M32_Monitor & SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        else
            return DBGDTRRXint;
        end if;
    else
        return DBGDTRRXint;
    end if;
The DBGDTRTXext characteristics are:

**Purpose**

Used for save/restore of DBGDTRTXint. It is a component of the Debug Communication Channel.

**Configuration**

AArch32 System register DBGDTRTXext bits [31:0] are architecturally mapped to AArch64 System register OSDTRTX_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDTRTXext are `UNDEFINED`.

**Attributes**

DBGDTRTXext is a 32-bit register.

**Field descriptions**

The DBGDTRTXext bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Return DTRTX without side-effect**

**Bits [31:0]**

Return DTRTX without side-effect.

Reads of this register return the value in DTRTX and do not change TXfull.

 Writes of this register update the value in DTRTX and do not change TXfull.

For the full behavior of the Debug Communications Channel, see ‘The Debug Communication Channel and Instruction Transfer Register’.

On a Cold reset, this field resets to an architecturally `UNKNOWN` value.

**Accessing the DBGDTRTXext**

Arm deprecates reads and writes of DBGDTRTXext through the System register interface when the OS Lock is unlocked, DBGOSLSR.OSLK == 0.

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elseif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        return DBGDTRTXext;
    end
elseif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        return DBGDTRTXext;
    end
elseif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return DBGDTRTXext;
    end
else
    return DBGDTRTXext;
MCR{<c>}{<q>} <coproc>, (#)<opc1>, <Rt>, <CRn>, <CRm>{, (#)<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

DBGDTXTxext, Debug OS Lock Data Transfer Register, Transmit
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif
    else
        DBGDTRXText = R[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        endif
    else
        DBGDTRXText = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
        AArch32.TakeMonitorTrapException();
    else
        DBGDTRXText = R[t];
    endif
else
    DBGDTRXText = R[t];
endif
DBGDTRTXint, Debug Data Transfer Register, Transmit

The DBGDTRTXint characteristics are:

**Purpose**

Transfers data from the PE to an external debugger. For example, it is used by a debug target to transfer data to the debugger. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communication Channel.

**Configuration**

AArch32 System register DBGDTRTXint bits [31:0] are architecturally mapped to AArch64 System register DBGDTRTX_EL0[31:0].

AArch32 System register DBGDTRTXint bits [31:0] are architecturally mapped to External register DBGDTRTX_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGDTRTXint are UNDEFINED.

**Attributes**

DBGDTRTXint is a 32-bit register.

**Field descriptions**

The DBGDTRTXint bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Return DTRTX</td>
</tr>
<tr>
<td>30</td>
<td>Write to this register:</td>
</tr>
<tr>
<td>29</td>
<td>- If TXfull is set to 1, set DTRTX to UNKNOWN.</td>
</tr>
<tr>
<td>28</td>
<td>- If TXfull is set to 0, update the value in DTRTX.</td>
</tr>
<tr>
<td>27</td>
<td>After the write, TXfull is set to 1.</td>
</tr>
</tbody>
</table>

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGDTRTXint**

Data can be loaded from memory into this register using 'LDC (immediate)' and 'LDC (literal)'.

Accesses to this register use the following encodings:

MCR{<c}>{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

| coproc | opc1 | CRn | CRm | opc2 |
if Halted() then
    DBGDTRXTint = R[t];
elsif PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && MDSCR_EL1.TDCC == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x05);
    elsif ELUsingAArch32(EL1) && DBGDSCRext.UDCCdis == '1' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x05);
        else
            UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
        AArch32.TakeHypTrapException(0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && (HCR_EL2.TGE == '1' || MDCR_EL2.<TDE,TDA> != '00') then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
        AArch32.TakeMonitorTrapException();
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    else
        DBGDTRXTint = R[t];
    elsif PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TDCC == '1' then
            AArch32.TakeHypTrapException(0x05);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x05);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
            AArch32.TakeHypTrapException(0x05);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        else
            DBGDTRXTint = R[t];
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDCC == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        else
            DBGDTRXTint = R[t];
    elsif PSTATE.EL == EL3 then
        if PSTATE.M != M32_Monitor && SDCR.TDCC == '1' then
            AArch32.TakeMonitorTrapException();
        else
            DBGDTRXTint = R[t];
The DBGOSDLR characteristics are:

**Purpose**

Locks out the external debug interface.

**Configuration**

AArch32 System register DBGOSDLR bits [31:0] are architecturally mapped to AArch64 System register OSDLR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGOSDLR are **UNDEFINED**.

**Attributes**

DBGOSDLR is a 32-bit register.

**Field descriptions**

The DBGOSDLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
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<tr>
<td>28</td>
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<td>27</td>
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</tr>
<tr>
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</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reserved, RES0.

**DLK, bit [0]**

*When FEAT_DoubleLock is implemented:*

OS Double Lock control bit.

<table>
<thead>
<tr>
<th>DLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Double Lock unlocked.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Double Lock locked, if DBGPRCR.CORENPDREQ (Core no powerdown request) bit is set to 0 and the PE is in Non-debug state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

*Otherwise:*

Reserved, RAZ/WI.

**Accessing the DBGOSDLR**

Accesses to this register use the following encodings:
### The section contains code related to exception handling in a processor.

#### Table 1: MCR Format

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDOSA == '00' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL2.TDOSA") then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.TDOSA == '00' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by HDCR.TDOSA") then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGOSDLR;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
    (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA") then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  else
    return DBGOSDLR;
  end if;
elsif PSTATE.EL == EL3 then
  return DBGOSDLR;
end if;

MCR{<c}>{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        UNDEFINED;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDOSA> != '00' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by HDCR.TDOSA")
        then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDOSA> != '00' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by HDCR.TDOSA")
        then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        DBGOSDLR = R[t];
    end if
else
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        UNDEFINED;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        DBGOSDLR = R[t];
    end if
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        UNDEFINED;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' &&
        (IsFeatureImplemented(FEAT_DoubleLock) || boolean IMPLEMENTATION_DEFINED "Trapped by MDCR_EL3.TDOSA")
        then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        DBGOSDLR = R[t];
    end if
elif PSTATE.EL == EL3 then
    DBGOSDLR = R[t];
DBGOSECCR, Debug OS Lock Exception Catch Control Register

The DBGOSECCR characteristics are:

**Purpose**

Provides a mechanism for an operating system to access the contents of EDECCR that are otherwise invisible to software, so it can save/restore the contents of EDECCR over powerdown on behalf of the external debugger.

**Configuration**

AArch32 System register DBGOSECCR bits [31:0] are architecturally mapped to AArch64 System register OSECCR_EL1[31:0].

AArch32 System register DBGOSECCR bits [31:0] are architecturally mapped to External register EDECCR[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGOSECCR are UNDEFINED.

If DBGOSLSR.OSLK == 0 then DBGOSECCR returns an UNKNOWN value on reads and ignores writes.

**Attributes**

DBGOSECCR is a 32-bit register.

**Field descriptions**

The DBGOSECCR bit assignments are:

**When DBGOSLSR.OSLK == 1:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**EDECCR, bits [31:0]**

Used for save/restore to EDECCR over powerdown.

Reads or writes to this field are indirect accesses to EDECCR.

**Accessing the DBGOSECCR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
else
  HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  end
else
  return DBGOSECCR;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  end
else
  return DBGOSECCR;
elsif PSTATE.EL == EL3 then
  return DBGOSECCR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
else
  HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  end
else
  return DBGOSECCR;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
  end
else
  return DBGOSECCR;
elsif PSTATE.EL == EL3 then
  return DBGOSECCR;
DBGOSLAR, Debug OS Lock Access Register

The DBGOSLAR characteristics are:

**Purpose**

Provides a lock for the debug registers. The OS Lock also disables some debug exceptions and debug events.

**Configuration**

AArch32 System register DBGOSLAR bits [31:0] are architecturally mapped to AArch64 System register OSLAR_EL1[31:0].

AArch32 System register DBGOSLAR bits [31:0] are architecturally mapped to External register OSLAR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGOSLAR are UNDEFINED.

**Attributes**

DBGOSLAR is a 32-bit register.

**Field descriptions**

The DBGOSLAR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**OSLA, bits [31:0]**

OS Lock Access. Writing the value 0xC5ACCE55 to the DBGOSLAR sets the OS lock to 1. Writing any other value sets the OS lock to 0.

Use DBGOSLRSR.OSLK to check the current status of the lock.

**Accessing the DBGOSLAR**

Accesses to this register use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDOSA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDOSA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        DBGOSLAR = R[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    else
        DBGOSLAR = R[t];
    end if
elsif PSTATE.EL == EL3 then
    DBGOSLAR = R[t];
The DBGOSLSR characteristics are:

**Purpose**

Provides status information for the OS Lock.

**Configuration**

AArch32 System register DBGOSLSR bits [31:0] are architecturally mapped to AArch64 System register OSLSR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGOSLSR are UNDEFINED.

The OS Lock status is also visible in the external debug interface through EDPRSR.

**Attributes**

DBGOSLSR is a 32-bit register.

**Field descriptions**

The DBGOSLSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>OSLM[1]</td>
</tr>
<tr>
<td>29</td>
<td>nTT</td>
</tr>
<tr>
<td>28</td>
<td>OSLK</td>
</tr>
<tr>
<td>27</td>
<td>OSLM[0]</td>
</tr>
<tr>
<td>26</td>
<td>8</td>
</tr>
<tr>
<td>25</td>
<td>7</td>
</tr>
<tr>
<td>24</td>
<td>6</td>
</tr>
<tr>
<td>23</td>
<td>5</td>
</tr>
<tr>
<td>22</td>
<td>4</td>
</tr>
<tr>
<td>21</td>
<td>3</td>
</tr>
<tr>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td>19</td>
<td>1</td>
</tr>
<tr>
<td>18</td>
<td>0</td>
</tr>
</tbody>
</table>

- **RES0**: Reserved, RES0.

- **OSLM, bits [3, 0]**
  
  OS lock model implemented. Identifies the form of OS save and restore mechanism implemented.

<table>
<thead>
<tr>
<th>OSLM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>OS Lock not implemented.</td>
</tr>
<tr>
<td>0b10</td>
<td>OS Lock implemented.</td>
</tr>
</tbody>
</table>

  All other values are reserved. In an Armv8 implementation the value 0b00 is not permitted.

  The OSLM field is split as follows:

  - OSLM[1] is DBGOSLSR[3].
  - OSLM[0] is DBGOSLSR[0].

- **nTT, bit [2]**

  Not 32-bit access. This bit is always RAZ. It indicates that a 32-bit access is needed to write the key to the OS Lock Access Register.

- **OSLK, bit [1]**

  OS Lock Status. The possible values are:
### OSLK

<table>
<thead>
<tr>
<th>OSLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Lock unlocked.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Lock locked.</td>
</tr>
</tbody>
</table>

The OS Lock is locked and unlocked by writing to the OS Lock Access Register.

On a Cold reset, this field resets to 1.

### Accessing the DBGOSLSR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}> \\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b110</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
      UNDEFINED;
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDOSA> != '00' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x05);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDOSA> != '00' then
      AArch32.TakeHypTrapException(0x05);
   elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
      if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
      else
         AArch64.AArch32SystemAccessTrap(EL3, 0x05);
      end if;
   else
      return DBGOSLSR;
   end if;
elsif PSTATE.EL == EL2 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
      UNDEFINED;
   elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
      if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
      else
         AArch64.AArch32SystemAccessTrap(EL3, 0x05);
      end if;
   else
      return DBGOSLSR;
   end if;
elsif PSTATE.EL == EL3 then
   return DBGOSLSR;
DBGPRCR, Debug Power Control Register

The DBGPRCR characteristics are:

**Purpose**

Controls behavior of the PE on powerdown request.

**Configuration**

AArch32 System register DBGPRCR bits [31:0] are architecturally mapped to AArch64 System register DBGPRCR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGPRCR are UNDEFINED.

Bit [0] of this register is mapped to EDPSCR, CORENPDRQ, bit [0] of the external view of this register.

The other bits in these registers are not mapped to each other.

**Attributes**

DBGPRCR is a 32-bit register.

**Field descriptions**

The DBGPRCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CORENPDRQ |

**Bits [31:1]**

Reserved, RES0.

**CORENPDRQ, bit [0]**

*When FEAT_DoPD is implemented:*

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to the Cold reset value on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states see 'Core power domain power states'.

**Note**
 Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, if the powerup request is implemented and the powerup request has been asserted, this field is set to an IMPLEMENTATION DEFINED choice of 0 or 1. If the powerup request is not asserted, this field is set to 0.

Otherwise:

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
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<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to the value of EDPRCR.COREPURQ on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states see 'Core power domain power states'.

Note

Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, this field resets to the value in EDPRCR.COREPURQ.

Accessing the DBGPRCR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{<coproc>}, \{#\}<\text{opc1}>, \text{<Rt>}, \text{<CRn>}, \text{<CRm>}\{, \{#\}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDOSA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDOSA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end
       .defaultProps = R[t];
    elsif PSTATE.EL == EL3 then
        DBGPRCR = R[t];
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDOSA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDOSA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && MDCR_EL3.TDOSA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDOSA == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x05);
            end
       .defaultProps = R[t];
    elsif PSTATE.EL == EL3 then
        DBGPRCR = R[t];
else
    DBGPRCR = R[t];
elsif PSTATE.EL == EL3 then
    DBGPRCR = R[t];
end
DBGVCR, Debug Vector Catch Register

The DBGVCR characteristics are:

**Purpose**

Controls Vector Catch debug events.

**Configuration**

AArch32 System register DBGVCR bits [31:0] are architecturally mapped to AArch64 System register DBGVCR32_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGVCR are UNDEFINED.

This register is required in all implementations.

**Attributes**

DBGVCR is a 32-bit register.

**Field descriptions**

The DBGVCR bit assignments are:

**When EL3 is implemented and EL3 is using AArch32:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
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<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NSF</td>
<td>NSI</td>
<td>RES0</td>
<td>NSD</td>
<td>NSP</td>
<td>NSS</td>
<td>NSU</td>
<td>RES0</td>
<td>MFSI</td>
<td>RES0</td>
<td>MD</td>
<td>MP</td>
<td>MS</td>
<td>RES0</td>
<td>SF</td>
<td>SI</td>
<td>RES0</td>
<td>SD</td>
<td>SP</td>
<td>SS</td>
<td>SU</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NSF, bit [31]**

FIQ vector catch enable in Non-secure state.

The exception vector offset is 0x1C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**NSI, bit [30]**

IRQ vector catch enable in Non-secure state.

The exception vector offset is 0x18.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [29]**

Reserved, RES0.

**NSD, bit [28]**

Data Abort vector catch enable in Non-secure state.

The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NSP, bit [27]**

Prefetch Abort vector catch enable in Non-secure state.

The exception vector offset is 0x0C.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NSS, bit [26]**

Supervisor Call (SVC) vector catch enable in Non-secure state.

The exception vector offset is 0x08.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NSU, bit [25]**

Undefined Instruction vector catch enable in Non-secure state.

The exception vector offset is 0x04.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [24:16]**

Reserved, RES0.

**MF, bit [15]**

FIQ vector catch enable in Monitor mode.

The exception vector offset is 0x1C.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**MI, bit [14]**

IRQ vector catch enable in Monitor mode.

The exception vector offset is 0x18.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [13]**

Reserved, RES0.

**MD, bit [12]**

Data Abort vector catch enable in Monitor mode.

The exception vector offset is 0x10.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**MP, bit [11]**

Prefetch Abort vector catch enable in Monitor mode.
The exception vector offset is 0x0C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**MS, bit [10]**

Secure Monitor Call (SMC) vector catch enable in Monitor mode.

The exception vector offset is 0x08.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [9:8]**

Reserved, RES0.

**SF, bit [7]**

FIQ vector catch enable in Secure state.

The exception vector offset is 0x1C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SI, bit [6]**

IRQ vector catch enable in Secure state.

The exception vector offset is 0x18.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [5]**

Reserved, RES0.

**SD, bit [4]**

Data Abort vector catch enable in Secure state.

The exception vector offset is 0x10.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SP, bit [3]**

Prefetch Abort vector catch enable in Secure state.

The exception vector offset is 0x0C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SS, bit [2]**

Supervisor Call (SVC) vector catch enable in Secure state.

The exception vector offset is 0x08.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
SU, bit [1]

Undefined Instruction vector catch enable in Secure state.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [0]

Reserved, RES0.

When EL3 is implemented and EL3 is using AArch64:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NSF | NSI | RES0 | NSD | NSP | NSS | NSF | RES0 | SF | SI | RES0 | SD | SP | SS | SU | RES0 |

NSF, bit [31]

FIQ vector catch enable in Non-secure state.
The exception vector offset is 0x1C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSI, bit [30]

IRQ vector catch enable in Non-secure state.
The exception vector offset is 0x18.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [29]

Reserved, RES0.

NSD, bit [28]

Data Abort vector catch enable in Non-secure state.
The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSP, bit [27]

Prefetch Abort vector catch enable in Non-secure state.
The exception vector offset is 0x0C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

NSS, bit [26]

Supervisor Call (SVC) vector catch enable in Non-secure state.
The exception vector offset is 0x08.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
NSU, bit [25]

Undefined Instruction vector catch enable in Non-secure state.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [24:8]

Reserved, RES0.

SF, bit [7]

FIQ vector catch enable in Secure state.
The exception vector offset is 0x1C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SI, bit [6]

IRQ vector catch enable in Secure state.
The exception vector offset is 0x18.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.

SD, bit [4]

Data Abort vector catch enable in Secure state.
The exception vector offset is 0x10.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SP, bit [3]

Prefetch Abort vector catch enable in Secure state.
The exception vector offset is 0x0C.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SS, bit [2]

Supervisor Call (SVC) vector catch enable in Secure state.
The exception vector offset is 0x08.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

SU, bit [1]

Undefined Instruction vector catch enable in Secure state.
The exception vector offset is 0x04.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [0]

Reserved, RES0.

When EL3 is not implemented:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>F</td>
<td>I</td>
<td>RES0</td>
<td>D</td>
<td>P</td>
<td>S</td>
<td>U</td>
<td>RES0</td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [31:8]

Reserved, RES0.

F, bit [7]

FIQ vector catch enable.

The exception vector offset is 0x1C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [6]

IRQ vector catch enable.

The exception vector offset is 0x18.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [5]

Reserved, RES0.

D, bit [4]

Data Abort vector catch enable.

The exception vector offset is 0x10.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

P, bit [3]

Prefetch Abort vector catch enable.

The exception vector offset is 0x0C.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

S, bit [2]

Supervisor Call (SVC) vector catch enable.

The exception vector offset is 0x08.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

U, bit [1]

Undefined Instruction vector catch enable.
The exception vector offset is 0x04.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [0]**

Reserved, RES0.

**Accessing the DBGVCR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if;
    else
        return DBGVCR;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if;
    else
        return DBGVCR;
    end if;
elsif PSTATE.EL == EL3 then
    return DBGVCR;
else
    return DBGVCR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end elsif
    else
        DBGVCR = R[t];
    end elsif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end elsif
    else
        DBGVCR = R[t];
    end elsif
elsif PSTATE.EL == EL3 then
    DBGVCR = R[t];
else
    DBGVCR = R[t];
end if
### DBGWCR<n>, Debug Watchpoint Control Registers, n = 0 - 15

The DBGWCR<n> characteristics are:

**Purpose**

Holds control information for a watchpoint. Forms watchpoint n together with value register DBGWVR<n>.

**Configuration**

AArch32 System register DBGWCR<n> bits [31:0] are architecturally mapped to AArch64 System register DBGWCR<n>_EL1[31:0].

AArch32 System register DBGWCR<n> bits [31:0] are architecturally mapped to External register DBGWCR<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGWCR<n> are UNDEFINED.

If watchpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGWCR<n> is a 32-bit register.

**Field descriptions**

The DBGWCR<n> bit assignments are:

```
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| MASK| RES0| WT  | LBN | SSC | HMC | BAS | LSC | PAC | E   |
```

When the E field is zero, all the other fields in the register are ignored.

**Bits [31:29]**

Reserved, RES0.

**MASK, bits [28:24]**

Address mask. Only objects up to 2GB can be watched using a single mask.

<table>
<thead>
<tr>
<th>MASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>No mask.</td>
</tr>
<tr>
<td>0b000001</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b000010</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

If programmed with a reserved value, a watchpoint must behave as if either:

- MASK has been programmed with a defined value, which might be 0 (no mask), other than for a direct read of DBGWCRn_EL1.
- The watchpoint is disabled.

Software must not rely on this property because the behavior of reserved values might change in a future revision of the architecture.

Other values mask the corresponding number of address bits, from 0b00001 masking 3 address bits (0x00000007 mask for address) to 0b111111 masking 31 address bits (0x7FFFFFFF mask for address).
On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [23:21]**

Reserved, RES0.

**WT, bit [20]**

Watchpoint type. Possible values are:

<table>
<thead>
<tr>
<th>WT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unlinked data address match.</td>
</tr>
<tr>
<td>0b1</td>
<td>Linked data address match.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**LBN, bits [19:16]**

Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**SSC, bits [15:14]**

Security state control. Determines the Security states under which a Watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.

For more information, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions', and 'Reserved DBGBCR<n>.{SSC, HMC, PMC} values'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**HMC, bit [13]**

Higher mode control. Determines the debug perspective for deciding when a Watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.

For more information on the operation of the SSC, HMC, and PAC fields, see 'Execution conditions for which a watchpoint generates Watchpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**BAS, bits [12:5]**

Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n> is being watched.

<table>
<thead>
<tr>
<th>BAS</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxxxxxxx1</td>
<td>Match byte at DBGWVR&lt;n&gt;</td>
</tr>
<tr>
<td>0bxxxxx1xx</td>
<td>Match byte at DBGWVR&lt;n&gt;+1</td>
</tr>
<tr>
<td>0bxxxx1xxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+2</td>
</tr>
<tr>
<td>0bxxxx1xxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+3</td>
</tr>
</tbody>
</table>

In cases where DBGWVR<n> addresses a double-word:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Description, if DBGWVR&lt;n&gt;[2] == 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxx1xxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+4</td>
</tr>
<tr>
<td>0bx1xxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+5</td>
</tr>
<tr>
<td>0bx1xxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+6</td>
</tr>
<tr>
<td>0b1xxxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;+7</td>
</tr>
</tbody>
</table>

The valid values for BAS are non-zero binary numbers all of whose set bits are contiguous. All other values are reserved and must not be used by software. See ‘Reserved DBGWCR<n>.BAS values’.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**LSC, bits [4:3]**

Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are:

<table>
<thead>
<tr>
<th>LSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>Match instructions that load from a watchpointed address.</td>
</tr>
<tr>
<td>0b10</td>
<td>Match instructions that store to a watchpointed address.</td>
</tr>
<tr>
<td>0b11</td>
<td>Match instructions that load from or store to a watchpointed address.</td>
</tr>
</tbody>
</table>

All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**PAC, bits [2:1]**

Privilege of access control. Determines the Exception level or levels at which a Watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and HMC fields.

For more information on the operation of the SSC, HMC, and PAC fields, see ‘Execution conditions for which a watchpoint generates Watchpoint exceptions’.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**E, bit [0]**

Enable watchpoint n. Possible values are:

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Watchpoint disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Watchpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGWCR<n>**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{<coproc>}, \{#<opc1>\}, \text{<Rt>}, \text{<CRn>}, \text{<CRm>}{, \{#<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> == '00' then
        AArch32.TakeHypTrapException(0x05);
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end
elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
    return DBGWCR[UInt(CRm<3:0>)];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
else
    return DBGWCR[UInt(CRm<3:0>)];
elsif PSTATE.EL == EL3 then
    if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
else
    return DBGWCR[UInt(CRm<3:0>)];
end

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  # Remaining code...
elsif PSTATE.EL == EL2 then
  # Remaining code...
elsif PSTATE.EL == EL3 then
  # Remaining code...
else
  DBGWCR[UInt(CRm<3:0>)] = R[t];
endif

DBGWFAR, Debug Watchpoint Fault Address Register

The DBGWFAR characteristics are:

**Purpose**

Previously returned information about the address of the instruction that accessed a watchpointed address. Is now deprecated and RES0.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGWFAR are UNDEFINED.

**Attributes**

DBGWFAR is a 32-bit register.

**Field descriptions**

The DBGWFAR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Reserved, RES0.

**Accessing the DBGWFAR**

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\} \{<q>\} \text{<coproc>}, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        return DBGWFAR;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        return DBGWFAR;
    end
elsif PSTATE.EL == EL3 then
    return DBGWFAR;
end

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0110</td>
<td>0b0000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        DBGWFAR = R[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end
    else
        DBGWFAR = R[t];
    end
elsif PSTATE.EL == EL3 then
    DBGWFAR = R[t];
DBGWVR<n>, Debug Watchpoint Value Registers, n = 0 - 15

The DBGWVR<n> characteristics are:

**Purpose**

Holds a data address value for use in watchpoint matching. Forms watchpoint n together with control register DBGWCR<n>.

**Configuration**

AArch32 System register DBGWVR<n> bits [31:0] are architecturally mapped to AArch64 System register DBGWVR<n>_EL1[31:0].

AArch32 System register DBGWVR<n> bits [31:0] are architecturally mapped to External register DBGWVR<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DBGWVR<n> are UNDEFINED.

If watchpoint n is not implemented then accesses to this register are UNDEFINED.

**Attributes**

DBGWVR<n> is a 32-bit register.

**Field descriptions**

The DBGWVR<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| VA | RES0 |

VA, bits [31:2]

Bits[31:2] of the address value for comparison.


On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [1:0]

Reserved, RES0.

**Accessing the DBGWVR<n>**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.<TDE,TDA> != '00' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
        AArch32.TakeHypTrapException(0x05);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        return DBGWVR[UInt(CRm<3:0>)];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x05);
        end if
    elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        return DBGWVR[UInt(CRm<3:0>)];
    end if
elsif PSTATE.EL == EL3 then
    if DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
        Halt(DebugHalt_SoftwareAccess);
    else
        return DBGWVR[UInt(CRm<3:0>)];
    end if
end if

MCR{<c>{<q>} <coproc>, {#<opc1>, <Rt>, <CRn>, <CRm>{, {#<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b000</td>
<td>0b0000</td>
<td>n[3:0]</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.<TDE,TDA> != '00' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x05);
  elsif EL2Enabled() && ELUsingAArch32(EL3) && HDCR.<TDE,TDA> != '00' then
    AArch32.TakeHypTrapException(0x05);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x05);
    end if;
  elsif DBGOSLSR.OSLK == '0' && HaltingAllowed() && EDSCR.TDA == '1' then
    Halt(DebugHalt_SoftwareAccess);
else
  DBGWVR[UInt(CRm<3:0>)] = R[t];
endif;
else
  DBGWVR[UInt(CRm<3:0>)] = R[t];
eendif;
else
  DBGWVR[UInt(CRm<3:0>)] = R[t];
eendif;
DCCIMVAC, Data Cache line Clean and Invalidate by VA to PoC

The DCCIMVAC characteristics are:

**Purpose**

Clean and Invalidate data or unified cache line by virtual address to PoC.

**Configuration**

AArch32 System instruction DCCIMVAC performs the same function as AArch64 System instruction DCCIVAC.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCCIMVAC are UNDEFINED.

**Attributes**

DCCIMVAC is a 32-bit System instruction.

**Field descriptions**

The DCCIMVAC input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DCCIMVAC instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'AArch32 data cache maintenance instructions (DC*)'.

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.TPCP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAAArch32(EL2) && HCR.TPC == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        DCCIMVAC(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    DCCIMVAC(R[t]);
elsif PSTATE.EL == EL3 then
    DCCIMVAC(R[t]);
else
    DCCIMVAC(R[t]);
DCCISW, Data Cache line Clean and Invalidate by Set/Way

The DCCISW characteristics are:

**Purpose**

Clean and Invalidate data or unified cache line by set/way.

**Configuration**

AArch32 System instruction DCCISW performs the same function as AArch64 System instruction DCCISW.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCCISW are UNDEFINED.

**Attributes**

DCCISW is a 32-bit System instruction.

**Field descriptions**

The DCCISW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SetWay |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Level | RES0 |

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = Log2(ASSOCIATIVITY), L = Log2(LINELEN), B = (L + S), S = Log2(NSETS).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.

**Executing the DCCISW instruction**

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED
The instruction performs cache maintenance on one of:
- No cache lines.
- A single arbitrary cache line.
- Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>}\ <\text{coproc}\},\ \{#\}<\text{opc1}\>,\ <\text{Rt}\>,\ <\text{CRn}\>,\ <\text{CRm}\>{,\ \{#\}<\text{opc2}\>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TSW == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TSW == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    DCCISW(R[t]);
  end
elsif PSTATE.EL == EL2 then
  DCCISW(R[t]);
elsif PSTATE.EL == EL3 then
  DCCISW(R[t]);
DCCMVAC, Data Cache line Clean by VA to PoC

The DCCMVAC characteristics are:

**Purpose**

Clean data or unified cache line by virtual address to PoC.

**Configuration**

AArch32 System instruction DCCMVAC performs the same function as AArch64 System instruction DC.CVAC.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCCMVAC are UNDEFINED.

**Attributes**

DCCMVAC is a 32-bit System instruction.

**Field descriptions**

The DCCMVAC input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Virtual address to use**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DCCMVAC instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'AArch32 data cache maintenance instruction (DC*)' in the Arm® Architecture Reference Manual, Armv8, for Armv8-A architecture profile.

Accesses to this instruction use the following encodings:

\[
\text{MCR}<c>{q}<c> \text{<coproc>}, \{#<opc1>}, \text{<Rt>}, \text{<CRn>}, \text{<CRm>{, \{#<opc2>}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TPCP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPC == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        DCCMVAC(R[t]);
    end
elsif PSTATE.EL == EL2 then
    DCCMVAC(R[t]);
elsif PSTATE.EL == EL3 then
    DCCMVAC(R[t]);

DCCMVAU, Data Cache line Clean by VA to PoU

The DCCMVAU characteristics are:

**Purpose**

Clean data or unified cache line by virtual address to PoU.

**Configuration**

AArch32 System instruction DCCMVAU performs the same function as AArch64 System instruction DC CVAU.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCCMVAU are undefined.

**Attributes**

DCCMVAU is a 32-bit System instruction.

**Field descriptions**

The DCCMVAU input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Virtual address to use</td>
<td>Bits [31:0] Virtual address to use. No alignment restrictions apply to this VA.</td>
</tr>
</tbody>
</table>

**Executing the DCCMVAU instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'AArch32 data cache maintenance instructions (DC*)'.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TPU == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TOCU == '1' then
    AArch32.TakeHypTrapException(0x03);
else
  DCCMVAU(R[t]);
elsif PSTATE.EL == EL2 then
  DCCMVAU(R[t]);
elsif PSTATE.EL == EL3 then
  DCCMVAU(R[t]);
DCCSW, Data Cache line Clean by Set/Way

The DCCSW characteristics are:

**Purpose**

Clean data or unified cache line by set/way.

**Configuration**

AArch32 System instruction DCCSW performs the same function as AArch64 System instruction DC CSW.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCCSW are UNDEFINED.

**Attributes**

DCCSW is a 32-bit System instruction.

**Field descriptions**

The DCCSW input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    | SetWay |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Level | RES0 |

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = \(\log_2(\text{ASSOCIATIVITY})\), \(L = \log_2(\text{LINELEN})\), \(B = (L + S)\), \(S = \log_2(\text{NSETS})\).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.

**Executing the DCCSW instruction**

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED
- The instruction performs cache maintenance on one of:
  - No cache lines.
Accesses to this instruction use the following encodings:

\[
\text{MCR\{<c>\}<q>} <\text{coproc}>\{\text{<opc1>}, \text{<Rt>}, \text{<CRn>}, \text{<CRm}>\}\{\text{<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b1010</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TSW == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TSW == '1' then
    AArch32.TakeHypTrapException(0x03);
else
  DCCSW(R[t]);
elsif PSTATE.EL == EL2 then
  DCCSW(R[t]);
elsif PSTATE.EL == EL3 then
  DCCSW(R[t]);
DCIMVAC, Data Cache line Invalidate by VA to PoC

The DCIMVAC characteristics are:

**Purpose**

Invalidate data or unified cache line by virtual address to PoC.

**Configuration**

AArch32 System instruction DCIMVAC performs the same function as AArch64 System instruction DC IVAC.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCIMVAC are **UNDEFINED**.

**Attributes**

DCIMVAC is a 32-bit System instruction.

**Field descriptions**

The DCIMVAC input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

Virtual address to use.

**Bits [31:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the DCIMVAC instruction**

It is **IMPLEMENTATION DEFINED** whether, when this instruction is executed, it can generate a watchpoint. If this instruction can generate a watchpoint this is prioritized in the same way as other watchpoints.

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see ‘AArch32 data cache maintenance instructions (DC*)’.

Accesses to this instruction use the following encodings:

MCR{<c>{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TPCP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<DC,VM> != '00' then
        DCCIMVAC(R[t]);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.<DC,VM> != '00' then
        DCCIMVAC(R[t]);
    else
        DCIMVAC(R[t]);
elsif PSTATE.EL == EL2 then
    DCIMVAC(R[t]);
else if PSTATE.EL == EL3 then
    DCIMVAC(R[t]);
The DCISW characteristics are:

**Purpose**

Invalidate data or unified cache line by set/way.

**Configuration**

AArch32 System instruction DCISW performs the same function as AArch64 System instruction DCISW. This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DCISW are UNDEFINED.

**Attributes**

DCISW is a 32-bit System instruction.

**Field descriptions**

The DCISW input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-2</td>
<td>SetWay</td>
<td>Contains two fields: Way, bits[31:32-A], the number of the way to operate on. Set, bits[B-1:L], the number of the set to operate on. Bits[L-1:4] are RES0.</td>
</tr>
<tr>
<td>3-1</td>
<td>Level</td>
<td>Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.</td>
</tr>
<tr>
<td>0</td>
<td>Bit</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**SetWay, bits [31:4]**

Contains two fields:

- Way, bits[31:32-A], the number of the way to operate on.
- Set, bits[B-1:L], the number of the set to operate on.

Bits[L-1:4] are RES0.

A = \( \log_2(\text{ASSOCIATIVITY}) \), L = \( \log_2(\text{LINELEN}) \), B = (L + S), S = \( \log_2(\text{NSETS}) \).

ASSOCIATIVITY, LINELEN (line length, in bytes), and NSETS (number of sets) have their usual meanings and are the values for the cache level being operated on. The values of A and S are rounded up to the next integer.

**Level, bits [3:1]**

Cache level to operate on, minus 1. For example, this field is 0 for operations on L1 cache, or 1 for operations on L2 cache.

**Bit [0]**

Reserved, RES0.

**Executing the DCISW instruction**

If this instruction is executed with a set, way or level argument that is larger than the value supported by the implementation then the behavior is CONSTRAINED UNPREDICTABLE and one of the following occurs:

- The instruction is UNDEFINED
- The instruction performs cache maintenance on one of:
  - No cache lines.
A single arbitrary cache line.

Multiple arbitrary cache lines.

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b011</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && HSTR_EL2.T7 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && HSTR_EL2.T7 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && HCR_EL2.TSW == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && HCR_EL2.SWIO == '1' then
    DCCISW(R[t]);
  elsif EL2Enabled() && HCR_EL2.<DC,VM> != '00' then
    DCCISW(R[t]);
  elsif PSTATE.EL == EL2 then
    DCISW(R[t]);
elsif PSTATE.EL == EL3 then
  DCISW(R[t]);
DFAR, Data Fault Address Register

The DFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Data Abort exception.

**Configuration**

AArch32 System register DFAR bits [31:0] are architecturally mapped to AArch64 System register FAR_EL1[31:0].

AArch32 System register DFAR bits [31:0] (S) are architecturally mapped to AArch32 System register HDFAR[31:0] when EL2 is implemented, EL3 is implemented and the highest implemented Exception level is using AArch32 state.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DFAR are UNDEFINED.

**Attributes**

DFAR is a 32-bit register.

**Field descriptions**

The DFAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>VA of faulting address of synchronous Data Abort exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

VA of faulting address of synchronous Data Abort exception.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DFAR**

Accesses to this register use the following encodings:

\[
MRC\{<c>\}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return DFAR_NS;
    else
        return DFAR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return DFAR_NS;
    else
        return DFAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return DFAR_S;
    else
        return DFAR_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        DFAR_NS = R[t];
    else
        DFAR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        DFAR_NS = R[t];
    else
        DFAR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        DFAR_S = R[t];
    else
        DFAR_NS = R[t];
DFSR, Data Fault Status Register

The DFSR characteristics are:

**Purpose**

Holds status information about the last data fault.

**Configuration**

AArch32 System register DFSR bits [31:0] are architecturally mapped to AArch64 System register ESR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DFSR are UNDEFINED.

The current translation table format determines which format of the register is used.

**Attributes**

DFSR is a 32-bit register.

**Field descriptions**

The DFSR bit assignments are:

**When TTBCR.EAE == 0:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | FnV | AET | CM | ExT | WnR | FS[4] | LPAE | RES0 | Domain | FS[3:0] |

**Bits [31:17]**

Reserved, RES0.

**FnV, bit [16]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>DFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>DFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is RES0 for all other Data Abort exceptions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**AET, bits [15:14]**

**When FEAT_RAS is implemented:**

Asynchronous Error Type. When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception. Possible values are:
AET | Meaning
---|---
0b00 | Uncontainable (UC).
0b01 | Unrecoverable state (UEU).
0b10 | Restartable state (UEO).
0b11 | Recoverable state (UER).

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other aborts.

In the event of multiple errors taken as a single SError interrupt exception, the overall PE error state is reported.

**Note**

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**CM, bit [13]**

Cache maintenance fault. For synchronous faults, this bit indicates whether a cache maintenance instruction generated the fault. The possible values of this bit are:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort not caused by execution of a cache maintenance instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by execution of a cache maintenance instruction, or on an address translation.</td>
</tr>
</tbody>
</table>

On a synchronous Data Abort on a translation table walk, this bit is UNKNOWN.

On an asynchronous fault, this bit is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ExT, bit [12]**

External abort type. This bit can be used to provide an IMPLEMENTATION DEFINED classification of External aborts.

In an implementation that does not provide any classification of External aborts, this bit is RES0.

For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**WnR, bit [11]**

Write not Read bit. Indicates whether the abort was caused by a write or a read instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by a read instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by a write instruction.</td>
</tr>
</tbody>
</table>

For faults on the cache maintenance and address translation System instructions in the (coproc==0b1111) encoding space this bit always returns a value of 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**FS, bits [10, 3:0]**

Fault status bits. Possible values of FS[4:0] are:

<table>
<thead>
<tr>
<th>FS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00001</td>
<td>Alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b00010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b00011</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00100</td>
<td>Fault on instruction cache maintenance.</td>
<td></td>
</tr>
<tr>
<td>0b00101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00110</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b00111</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b01001</td>
<td>Domain fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01011</td>
<td>Domain fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01100</td>
<td>Synchronous External abort, on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01110</td>
<td>Synchronous External abort, on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01111</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b10000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b10100</td>
<td>IMPLEMENTATION DEFINED fault (Lockdown fault).</td>
<td></td>
</tr>
<tr>
<td>0b10101</td>
<td>IMPLEMENTATION DEFINED fault (Unsupported Exclusive access fault).</td>
<td></td>
</tr>
<tr>
<td>0b10110</td>
<td>SError interrupt.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11000</td>
<td>SError interrupt, from a parity or ECC error on memory access.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11001</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11100</td>
<td>Synchronous parity or ECC error on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11110</td>
<td>Synchronous parity or ECC error on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Short-descriptor translation table lookup'.

The FS field is split as follows:

- FS[4] is DFSR[10].
- FS[3:0] is DFSR[3:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**LPAE, bit [9]**

On taking a Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>

Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [8]

Reserved, RES0.

Domain, bits [7:4]

The domain of the fault address.

Arm deprecates any use of this field, see 'The Domain field in the DFSR'.

This field is UNKNOWN for certain faults where the DFSR is updated and reported using the Short-descriptor FSR encodings, see 'Validity of Domain field on faults that update the DFSR when using the Short-descriptor encodings'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When TTBCR.EAE == 1:

Bits [31:17]

Reserved, RES0.

FnV, bit [16]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>DFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>DFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is RES0 for all other Data Abort exceptions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

AET, bits [15:14]

When FEAT_RAS is implemented:

Asynchronous Error Type. When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception. Possible values are:

<table>
<thead>
<tr>
<th>AET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Uncontainable (UC).</td>
</tr>
<tr>
<td>0b01</td>
<td>Unrecoverable state (UEU).</td>
</tr>
<tr>
<td>0b10</td>
<td>Restartable state (UEO).</td>
</tr>
<tr>
<td>0b11</td>
<td>Recoverable state (UER).</td>
</tr>
</tbody>
</table>

This field is valid only if the DFSC code is 0b010001. It is RES0 for all other aborts.

In the event of multiple errors taken as a single SError interrupt exception, the overall PE error state is reported.

Note

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**CM, bit [13]**

Cache maintenance fault. For synchronous faults, this bit indicates whether a cache maintenance instruction generated the fault. The possible values of this bit are:

<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort not caused by execution of a cache maintenance instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by execution of a cache maintenance instruction.</td>
</tr>
</tbody>
</table>

On a synchronous Data Abort on a translation table walk, this bit is **UNKNOWN**.

On an asynchronous fault, this bit is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ExT, bit [12]**

External abort type. This bit can be used to provide an **IMPLEMENTATION DEFINED** classification of External aborts.

In an implementation that does not provide any classification of External aborts, this bit is RES0.

For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**WnR, bit [11]**

Write not Read bit. Indicates whether the abort was caused by a write or a read instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by a read instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by a write instruction.</td>
</tr>
</tbody>
</table>

For faults on the cache maintenance and address translation System instructions in the (coproc==0b1111) encoding space this bit always returns a value of 1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [10]**

Reserved, RES0.

**LPAE, bit [9]**

On taking a Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>

Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [8:6]**

Reserved, RES0.
**STATUS, bits [5:0]**

Fault status bits. Possible values of this field are:

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault in translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
<td></td>
</tr>
<tr>
<td>0b010100</td>
<td>Synchronous External abort on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011001</td>
<td>Asynchronous SError interrupt, from a parity or ECC error on memory access.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b100000</td>
<td>Alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b110100</td>
<td>IMPLEMENTATION DEFINED fault (Lockdown).</td>
<td></td>
</tr>
<tr>
<td>0b110101</td>
<td>IMPLEMENTATION DEFINED fault (Unsupported Exclusive access).</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Long-descriptor translation table lookup'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DFSR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return DFSR_NS;
else
  return DFSR;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return DFSR_NS;
else
  return DFSR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return DFSR_S;
else
  return DFSR_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    DFSR_NS = R[t];
else
  DFSR = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    DFSR_NS = R[t];
else
  DFSR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    DFSR_S = R[t];
else
  DFSR_NS = R[t];
DISR, Deferred Interrupt Status Register

The DISR characteristics are:

**Purpose**

Records that an SError interrupt has been consumed by an ESB instruction.

**Configuration**

AArch32 System register DISR bits [31:0] are architecturally mapped to AArch64 System register DISR_EL1[31:0] when the highest implemented Exception level is using AArch64.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to DISR are UNDEFINED.

**Attributes**

DISR is a 32-bit register.

**Field descriptions**

The DISR bit assignments are:

**When the ESB instruction is executed at EL2:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| A  | RES0 | AET | EA | RES0 | DFSC |

**A, bit [31]**

Set to 1 when an ESB instruction defers an asynchronous SError interrupt. If the implementation does not include any sources of SError interrupt that can be synchronized by an Error Synchronization Barrier, then this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [30:12]**

Reserved, RES0.

**AET, bits [11:10]**

Asynchronous Error Type. See the description of HSR.AET for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EA, bit [9]**

External abort Type. See the description of HSR.EA for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [8:6]**

Reserved, RES0.
DFSC, bits [5:0]

Fault Status Code. See the description of HSR.DFSC for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When the ESB instruction is executed at EL0 or EL1 and where TTBCR.EAE == 0:

<table>
<thead>
<tr>
<th>31</th>
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<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>RES0</td>
<td>AET</td>
<td>RES0</td>
<td>ExT</td>
<td>RES0</td>
<td>FS[4]</td>
<td>LPAE</td>
<td>RES0</td>
<td>FS[3:0]</td>
<td></td>
<td></td>
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</tbody>
</table>

A, bit [31]

Set to 1 when an ESB instruction defers an asynchronous SError interrupt. If the implementation does not include any sources of SError interrupt that can be synchronized by an Error Synchronization Barrier, then this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [30:16]

Reserved, RES0.

AET, bits [15:14]

Asynchronous Error Type. See the description of DFSR.AET for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [13]

Reserved, RES0.

ExT, bit [12]

External abort Type. See the description of DFSR.ExT for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [11]

Reserved, RES0.

FS, bits [10, 3:0]

Fault Status Code. See the description of DFSR.FS for an SError interrupt.

The FS field is split as follows:

- FS[4] is DISR[10].
- FS[3:0] is DISR[3:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

LPAE, bit [9]

Format.

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
## Bits [8:4]

Reserved, RES0.

### When the ESB instruction is executed at EL0 or EL1 and where TTBCR.EAE == 1:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>A</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
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<td>24</td>
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<td>22</td>
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<td>15</td>
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<td>14</td>
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<td>5</td>
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</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
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<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

### A, bit [31]

Set to 1 when an ESB instruction defers an asynchronous SError interrupt. If the implementation does not include any sources of SError interrupt that can be synchronized by an Error Synchronization Barrier, then this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Bits [30:16]

Reserved, RES0.

### AET, bits [15:14]

Asynchronous Error Type. See the description of DFSR.AET for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Bit [13]

Reserved, RES0.

### ExT, bit [12]

External abort Type. See the description of DFSR.ExT for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Bits [11:10]

Reserved, RES0.

### LPAE, bit [9]

Format.

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Bits [8:6]

Reserved, RES0.

### STATUS, bits [5:0]

Fault Status Code. See the description of DFSR.FS for an SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the DISR

An indirect write to DISR made by an ESB instruction does not require an explicit synchronization operation for the value that is written to be observed by a direct read of DISR occurring in program order after the ESB instruction.

DISR is RAZ/WI if EL3 is implemented, the PE is in Non-debug state, and any of the following apply:

- EL3 is using AArch64, SCR_EL3.EA == 1, and any of the following apply:
  - The PE is executing at EL2.
  - The PE is executing at EL1 and ((SCR_EL3.NS == 0 && SCR_EL3.EEL2 == 0) || HCR_EL2.AMO == 0).
- EL3 is using AArch32, SCR.EA == 1, and any of the following apply:
  - The PE is executing at EL2.
  - The PE is executing at EL1 and (SCR.NS == 0 || HCR.AMO == 0).

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elseif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elseself EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
elseself EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.AMO == '1' then
    VDISR_EL2 = R[t];
elseself EL2Enabled() && ELUsingAAArch32(EL2) && HCR.AMO == '1' then
    VDISR = R[t];
  else
    DISR = R[t];
elseself PSTATE.EL == EL2 then
    DISR = R[t];
elseself PSTATE.EL == EL3 then
    DISR = R[t];
```

```
MCR{<c>}{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elseself PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elseself EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
elseself EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.AMO == '1' then
    VDISR_EL2 = R[t];
elseself EL2Enabled() && ELUsingAAArch32(EL2) && HCR.AMO == '1' then
    VDISR = R[t];
  else
    DISR = R[t];
elseself PSTATE.EL == EL2 then
    DISR = R[t];
elseself PSTATE.EL == EL3 then
    DISR = R[t];
DLR, Debug Link Register

The DLR characteristics are:

**Purpose**

In Debug state, holds the address to restart from.

**Configuration**

AArch32 System register DLR bits [31:0] are architecturally mapped to AArch64 System register DLR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DLR are UNDEFINED.

**Attributes**

DLR is a 32-bit register.

**Field descriptions**

The DLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Restart address</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Restart address.

**Accessing the DLR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !Halted() then
  UNDEFINED;
else
  return DLR;

\[
\text{MCR}\{<c>\}\{<q>\} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if !Halted() then
  UNDEFINED;
else
  DLR = R[t];
DSPSR, Debug Saved Program Status Register

The DSPSR characteristics are:

**Purpose**

Holds the saved process state for Debug state. On entering Debug state, PSTATE information is written to this register. On exiting Debug state, values are copied from this register to PSTATE.

**Configuration**

AArch32 System register DSPSR bits [31:0] are architecturally mapped to AArch64 System register `DSPSR_EL0[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DSPSR are UNDEFINED.

**Attributes**

DSPSR is a 32-bit register.

**Field descriptions**

The DSPSR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
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<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>Z</td>
<td>C</td>
<td>V</td>
<td>Q</td>
<td>IT[1:0]</td>
<td>DIT</td>
<td>SSBS</td>
<td>PAN</td>
<td>SS</td>
<td>IL</td>
<td>GE</td>
<td>IT[7:2]</td>
<td>E</td>
<td>A</td>
<td>I</td>
<td>F</td>
<td>T</td>
<td>M[4:0]</td>
<td></td>
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</tbody>
</table>

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on entering Debug state, and copied to PSTATE.N on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on entering Debug state, and copied to PSTATE.Z on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on entering Debug state, and copied to PSTATE.C on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on entering Debug state, and copied to PSTATE.V on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on entering Debug state, and copied to PSTATE.Q on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on entering Debug state, and copied to PSTATE.IT[1:0] on exiting Debug state.

On exiting Debug state DSPSR.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DIT, bit [24]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on entering Debug state, and copied to PSTATE.DIT on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on entering Debug state, and copied to PSTATE.SSBS on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on entering Debug state, and copied to PSTATE.PAN on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**SS, bit [21]**

Software Step. Set to the value of PSTATE.SS on entering Debug state, and conditionally copied to PSTATE.SS on exiting Debug state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on entering Debug state, and copied to PSTATE.IL on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on entering Debug state, and copied to PSTATE.GE on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on entering Debug state, and copied to PSTATE.IT[7:2] on exiting Debug state.

DSPSR.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on entering Debug state, and copied to PSTATE.E on exiting Debug state.

If the implementation does not support big-endian operation, DSPSR.E is RES0. If the implementation does not support little-endian operation, DSPSR.E is RES1. On exiting Debug state, if the implementation does not support big-endian operation at the Exception level being returned to, DSPSR.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, DSPSR.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on entering Debug state, and copied to PSTATE.A on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on entering Debug state, and copied to PSTATE.I on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on entering Debug state, and copied to PSTATE.F on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on entering Debug state, and copied to PSTATE.T on exiting Debug state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**M[4:0], bits [4:0]**

Mode. Set to the value of PSTATE.M[4:0] on entering Debug state, and copied to PSTATE.M[4:0] on exiting Debug state.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10110</td>
<td>Monitor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If DSPSR.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, exiting Debug state is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the DSPSR**

Accesses to this register use the following encodings:

**MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !Halted() then
  UNDEFINED;
else
  return DSPSR;

**MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b011</td>
<td>0b0100</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if !Halted() then
  UNDEFINED;
else
  DSPSR = R[t];
DTLBIALL, Data TLB Invalidate All

The DTLBIALL characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from data TLBs that are from any level of the translation table walk. The entries that are invalidated are as follows:

- If executed at EL1, all entries that:
  - Would be required for the EL1&0 translation regime.
  - Match the current VMID, if EL2 is implemented and enabled in the current Security state.
- If executed in Secure state when EL3 is using AArch32, all entries that would be required for the Secure PL1&0 translation regime.
- If executed at EL2, and if EL2 is enabled in the current Security state, the stage 1 or stage 2 translation table entries that would be required for the Non-secure PL1&0 translation regime and matches the current VMID.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DTLBIALL are **UNDEFINED**.

**Attributes**

DTLBIALL is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the DTLBIALL instruction**

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    DTLBIALL();
  end
elsif PSTATE.EL == EL2 then
  DTLBIALL();
elsif PSTATE.EL == EL3 then
  DTLBIALL();
end
DTLBIASID, Data TLB Invalidate by ASID match

The DTLBIASID characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from data TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DTLBIASID are **UNDEFINED**.

**Attributes**

DTLBIASID is a 32-bit System instruction.

**Field descriptions**

The DTLBIASID input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries for non-global pages that match the ASID values will be affected by this System instruction.

**Executing the DTLBIASID instruction**

Accesses to this instruction use the following encodings:
DTLBIASID, Data TLB Invalidate by ASID match

MCR{<c>{<q>}{coproc}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    DTLBIASID(R[t]);
  end if
elsif PSTATE.EL == EL2 then
  DTLBIASID(R[t]);
elsif PSTATE.EL == EL3 then
  DTLBIASID(R[t]);
DTLBIMVA, Data TLB Invalidate by VA

The DTLBIMVA characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from data TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to DTLBIMVA are **undefined**.

**Attributes**

DTLBIMVA is a 32-bit System instruction.

**Field descriptions**

The DTLBIMVA input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>RES0</td>
<td>ASID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

**Executing the DTLBIMVA instruction**

Accesses to this instruction use the following encodings:

\[
MCR\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.TTLB == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
      AArch32.TakeHypTrapException(0x03);
   else
      DTLBIMVA(R[t]);
   endif;
elsif PSTATE.EL == EL2 then
   DTLBIMVA(R[t]);
elsif PSTATE.EL == EL3 then
   DTLBIMVA(R[t]);

**DVPRCTX, Data Value Prediction Restriction by Context**

The DVPRCTX characteristics are:

**Purpose**

Data Value Prediction Restriction by Context applies to all Data Value Prediction Resources that predict execution based on information gathered within the target execution context or contexts.

When this instruction is complete and synchronized, data value prediction does not permit later speculative execution within the target execution context to be observable through side channels.

This instruction is guaranteed to be complete following a DSB that covers both read and write behavior on the same PE as executed the original restriction instruction, and a subsequent context synchronization event is required to ensure that the effect of the completion of the instructions is synchronized to the current execution.

**Note**

This instruction does not require the invalidation of prediction structures so long as the behavior described for completion of this instruction is met by the implementation.

On some implementations the instruction is likely to take a significant number of cycles to execute. This instruction is expected to be used very rarely, such as on the roll-over of an ASID or VMID, but should not be used on every context switch.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level and FEAT_SPECRES is implemented. Otherwise, direct accesses to DVPRCTX are UNDEFINED.

**Attributes**

DVPRCTX is a 32-bit System instruction.

**Field descriptions**

The DVPRCTX input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
</tr>
<tr>
<td>27</td>
</tr>
<tr>
<td>26-1</td>
</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**GVMID, bit [27]**

Execution of this instruction applies to all VMIDs or a specified VMID.

<table>
<thead>
<tr>
<th>GVMID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Applies to specified VMID for an EL0 or EL1 target execution context.</td>
</tr>
<tr>
<td>0b1</td>
<td>Applies to all VMIDs for an EL0 or EL1 target execution context.</td>
</tr>
</tbody>
</table>
For target execution contexts other than EL0 or EL1, this field is RES0.

If the instruction is executed at EL0 or EL1, this field has an Effective value of 0.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**NS, bit [26]**

Security State.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Secure state.</td>
</tr>
<tr>
<td>1</td>
<td>Non-secure state.</td>
</tr>
</tbody>
</table>

If the instruction is executed in Non-secure state, this field has an Effective value of 1.

**EL, bits [25:24]**

Exception Level. Indicates the Exception level of the target execution context.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>EL0.</td>
</tr>
<tr>
<td>01</td>
<td>EL1.</td>
</tr>
<tr>
<td>10</td>
<td>EL2.</td>
</tr>
<tr>
<td>11</td>
<td>EL3.</td>
</tr>
</tbody>
</table>

If the instruction is executed at an Exception level lower than the specified level, this instruction is treated as a NOP.

**VMID, bits [23:16]**

Only applies when bit[27] is 0 and the target execution context is either:

- EL1.
- EL0 when (HCR_EL2.E2H==0 or HCR_EL2.TGE==0) or EL2 is using AArch32 state.

Otherwise this field is RES0.

When the instruction is executed at EL1, this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==0 or HCR_EL2.TGE==0 or ELUsingAArch32(EL2)), this field is treated as the current VMID.

When the instruction is executed at EL0 and (HCR_EL2.E2H==1 and HCR_EL2.TGE==1 and !ELUsingAArch32(EL2)), this field is ignored.

If EL2 is not implemented or not enabled for the target Security state, this field is RES0.

**Bits [15:9]**

Reserved, RES0.

**GASID, bit [8]**

Execution of this instruction applies to all ASIDs or a specified ASID.

<table>
<thead>
<tr>
<th>GASID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Applies to specified ASID for an EL0 target execution context.</td>
</tr>
<tr>
<td>1</td>
<td>Applies to all ASID for an EL0 target execution context.</td>
</tr>
</tbody>
</table>

For target execution contexts other than EL0, this field is RES0.

If the instruction is executed at EL0, this field has an Effective value of 0.
**ASID, bits [7:0]**

Only applies for an EL0 target execution context and when bit[8] is 0.

Otherwise, this field is RES0.

When the instruction is executed at EL0, this field is treated as the current ASID.

**Executing theDVPRCTX instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opcl}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#\}<\text{opc2}\rangle
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.<E2H,TGE> == '11' && !EL3Enabled() && HCR_EL3.NV == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && EL3Enabled() && !ELUsingAArch32(EL3) && HCR_EL3.NV == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
else
  if PSTATE.EL == EL1 then
    if !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    DVPRCTX(R[t]);
  if PSTATE.EL == EL2 then
  DVPRCTX(R[t]);
  elsif PSTATE.EL == EL3 then
  DVPRCTX(R[t]);

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ELR_hyp, Exception Link Register (Hyp mode)

The ELR_hyp characteristics are:

**Purpose**

When taking an exception to Hyp mode, holds the address to return to.

**Configuration**

AArch32 System register ELR_hyp bits [31:0] are architecturally mapped to AArch64 System register ELR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ELR_hyp are UNDEFINED.

**Attributes**

ELR_hyp is a 32-bit register.

**Field descriptions**

The ELR_hyp bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:0]**

Return address.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ELR_hyp**

ELR_hyp is accessible only at Hyp mode and Monitor mode.

Accesses to this register use the following encodings:

- **MRS{<c>}{<q>} <Rd>, ELR_hyp**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>0b1110</td>
</tr>
</tbody>
</table>

- **MSR{<c>}{<q>} ELR_hyp, <Rn>**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>0b1110</td>
</tr>
</tbody>
</table>
ERRIDR, Error Record ID Register

The ERRIDR characteristics are:

**Purpose**

Defines the highest numbered index of the error records that can be accessed through the Error Record System registers.

**Configuration**

AArch32 System register ERRIDR bits [31:0] are architecturally mapped to AArch64 System register \texttt{ERRIDR_EL1[31:0]}.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERRIDR are \texttt{UNDEFINED}.

**Attributes**

ERRIDR is a 32-bit register.

**Field descriptions**

The ERRIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>\texttt{RES0}</td>
</tr>
<tr>
<td>15-0</td>
<td>\texttt{NUM}</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, \texttt{RES0}.

**NUM, bits [15:0]**

Highest numbered index of the records that can be accessed through the Error Record System registers plus one. Zero indicates that no records can be accessed through the Error Record System registers.

Each implemented record is owned by a node. A node might own multiple records.

**Accessing the ERRIDR**

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>\}\{<q>\} \text{<coproc}, \{#}\text{<opc1>, <Rt>, <CRn>, <CRm>{, \{#}\text{<opc2>}}} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    return ERRIDR;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    return ERRIDR;
  end if
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ERRIDR;
  end if
ERRSELR, Error Record Select Register

The ERRSELR characteristics are:

**Purpose**

Selects an error record to be accessed through the Error Record System registers.

**Configuration**

AArch32 System register `ERRSELR` bits [31:0] are architecturally mapped to AArch64 System register `ERRSELR_EL1[31:0]`.

This register is present only when `FEAT_RAS` is implemented. Otherwise, direct accesses to ERRSELR are **UNDEFINED**.

If `ERRIDR` indicates that zero error records are implemented, then it is **IMPLEMENTATION DEFINED** whether ERRSELR is **UNDEFINED** or **RES0**.

**Attributes**

ERRSELR is a 32-bit register.

**Field descriptions**

The ERRSELR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SEL |

**Bits [31:16]**

Reserved, RES0.

**SEL, bits [15:0]**

Selects the error record accessed through the ERX registers.

For example, if `ERRSELR.SEL` is set to `0x0004`, then direct reads and writes of `ERXSTATUS` access `ERR4STATUS`.

If `ERRSELR.SEL` is set to a value greater than or equal to `ERRIDR.NUM`, then all of the following apply:

- The value read back from `ERRSELR.SEL` is **UNKNOWN**.
- One of the following occurs:
  - An **UNKNOWN** error record is selected.
  - The ERX* registers are RAZ/WI.
  - ERX* register reads and writes are NOPs.
  - ERX* register reads and writes are **UNDEFINED**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the ERRSELR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
</table>

Page 2365
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.TERR == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end
  else
    return ERRSELR;
  end
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.TERR == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end
  else
    return ERRSELR;
  end
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor & SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ERRSELR;
  end

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    elsif Halted() && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if
    else
      AArch32.TakeMonitorTrapException();
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    elsif Halted() && SCR.EL3.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ERRSELR = R[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ERRSELR = R[t];
  end if
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERRSELR = R[t];
  end if
}
ERXADDR, Selected Error Record Address Register

The ERXADDR characteristics are:

**Purpose**

Accesses bits [31:0] of \(\text{ERR}_n\text{ADDR}\) for the error record \(n\) selected by \(\text{ERRSELR}.\text{SEL}\).

**Configuration**

AArch32 System register ERXADDR bits [31:0] are architecturally mapped to AArch64 System register \(\text{ERXADDR}_{\text{EL1}}[31:0]\).

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXADDR are UNDEFINED.

**Attributes**

ERXADDR is a 32-bit register.

**Field descriptions**

The ERXADDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:0]**

ERXADDR accesses bits [31:0] of \(\text{ERR}_n\text{ADDR}\), where \(n\) is the value in \(\text{ERRSELR}.\text{SEL}\).

**Accessing the ERXADDR**

If \(\text{ERRIDR}.\text{NUM} == 0x0000\) or \(\text{ERRSELR}.\text{SEL}\) is set to a value greater than or equal to \(\text{ERRIDR}.\text{NUM}\), then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXADDR is RAZ/WI.
- Direct reads and writes of ERXADDR are NOPs.
- Direct reads and writes of ERXADDR are UNDEFINED.

\(\text{ERR}_n\text{ADDR}\) describes additional constraints that also apply when \(\text{ERR}_n\text{ADDR}\) is accessed through ERXADDR.

Accesses to this register use the following encodings:

\[\text{MRC\{<c>\}{<q>}} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\} \{,#\}<\text{opc2}>\]

<table>
<thead>
<tr>
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<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
extif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
extif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
extif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
extif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
estif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
estif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
estif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
extelse
        return ERXADDR;
estif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
estif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
estif EL2Enabled() && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
estelse
        return ERXADDR;
estif PSTATE.EL == EL3 then
    if Halted() && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
estelse
    return ERXADDR;
else
    if PSTATE.EL == EL1 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
estelse
    return ERXADDR;
estif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
estelse
    return ERXADDR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

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<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
   elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      UNDEFINED;
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
      else
         AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
         if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
         else
            ERXADDR = R[t];
         else
            AArch32.TakeMonitorTrapException();
      else
         if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
         else
            AArch32.AArch32SystemAccessTrap(EL3, 0x03);  
         elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
            if Halted() && EDSCR.SDD == '1' then
               UNDEFINED;
            else
               ERXADDR = R[t];
            else
               if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
                  AArch32.TakeMonitorTrapException();
               else
                  ERXADDR = R[t];
               else
                  ERXADDR = R[t];
ERXADDR2, Selected Error Record Address Register 2

The ERXADDR2 characteristics are:

**Purpose**

Accesses bits [63:32] of ERXADDR for the error record <n> selected by ERRSELR.SEL.

**Configuration**

AArch32 System register ERXADDR2 bits [31:0] are architecturally mapped to AArch64 System register ERXADDR_EL1[63:32].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXADDR2 are UNDEFINED.

**Attributes**

ERXADDR2 is a 32-bit register.

**Field descriptions**

The ERXADDR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:32]**

ERXADDR2 accesses bits [63:32] of ERR<n>ADDR, where <n> is the value in ERRSELR.SEL.

**Accessing the ERXADDR2**

If ERRDR.NUM == 0x0000 or ERRSELR.SEL is set to a value greater than or equal to ERRDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXADDR2 is RAZ/WI.
- Direct reads and writes of ERXADDR2 are NOPs.
- Direct reads and writes of ERXADDR2 are UNDEFINED.

**ERR<n>ADDR** describes additional constraints that also apply when ERR<n>ADDR is accessed through ERXADDR2.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && \boolean \text{IMPLEMENTATION DEFINED} \text{"EL3 trap priority when SDD == '1"} && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && \boolean \text{IMPLEMENTATION DEFINED} \text{"EL3 trap priority when SDD == '1"} && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return ERXADDR2;
        endif
    else
        return ERXADDR2;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && \boolean \text{IMPLEMENTATION DEFINED} \text{"EL3 trap priority when SDD == '1"} && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && \boolean \text{IMPLEMENTATION DEFINED} \text{"EL3 trap priority when SDD == '1"} && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return ERXADDR2;
        endif
    else
        AArch32.TakeMonitorTrapException();
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXADDR2;
    endif
else
    return ERXADDR2;
endif

MCR{<c>}{<q>}{<coproc>}{,#}{<opc1>},{<Rt>},{<CRn>},{<CRm>}{,#}{<opc2>}

<table>
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<tr>
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<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
else
  ERXADDR2 = R[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
else
  ERXADDR2 = R[t];
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
else
  ERXADDR2 = R[t];
ERXCTLR, Selected Error Record Control Register

The ERXCTLR characteristics are:

**Purpose**

Accesses bits [31:0] of ERR<\text{n}>CTRL for the error record <\text{n}> selected by ERRSEL<\text{R}.SEL.

**Configuration**

AArch32 System register ERXCTLR bits [31:0] are architecturally mapped to AArch64 System register ERXCTLR_EL1[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXCTLR are UNDEFINED.

**Attributes**

ERXCTLR is a 32-bit register.

**Field descriptions**

The ERXCTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>Bits [31:0] of ERR&lt;\text{n}&gt;CTRL</td>
</tr>
</tbody>
</table>

**Accessing the ERXCTLR**

If ERRIDR.NUM == 0x0000 or ERRSEL<\text{R}.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXCTLR is RAZ/WI.
- Direct reads and writes of ERXCTLR are NOPs.
- Direct reads and writes of ERXCTLR are UNDEFINED.

If ERRSEL<\text{R}.SEL is not the index of the first error record owned by a node, then ERR<\text{n}>CTRL[31:0] is not present, meaning reads and writes of ERXCTLR are RES0.

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>}} \text{<coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.TERR == '1' then
            if Halted() & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            end if
        end if
    else
        return ERXCTRLR;
    end if
elsif PSTATE_EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.TERR == '1' then
            if Halted() & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            end if
        end if
    else
        return ERXCTRLR;
    end if
elsif PSTATE_EL == EL3 then
    if PSTATE.M != M32_Monitor & SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXCTRLR;
    end if
end if

MCR{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  endif
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2_enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL2.TERR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  endif
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && SCR.TERR == '1' then
    UNDEFINED;
  endif
else
  ERXCTLR = R[t];
endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  endif
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  endif
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  if Halted() && SCR.TERR == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif
else
  ERXCTLR = R[t];
endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
else
  ERXCTLR = R[t];
endif
ERXCTRL2, Selected Error Record Control Register 2

The ERXCTRL2 characteristics are:

**Purpose**

Accesses bits [63:32] of ERR<n>CTRL for the error record <n> selected by ERRSEL<SEL>.

**Configuration**

AArch32 System register ERXCTRL2 bits [31:0] are architecturally mapped to AArch64 System register ERXCTRL_EL1[63:32].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXCTRL2 are UNDEFINED.

**Attributes**

ERXCTRL2 is a 32-bit register.

**Field descriptions**

The ERXCTRL2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bits [63:32] of ERR<n>CTRL |

**Bits [31:0]**

ERXCTRL2 accesses bits [63:32] of ERR<n>CTRL, where <n> is the value in ERRSEL<SEL>.

**Accessing the ERXCTRL2**

If ERRIDR NUM == 0x0000 or ERRSEL<SEL> is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXCTRL2 is RAZ/WI.
- Direct reads and writes of ERXCTRL2 are NOPs.
- Direct reads and writes of ERXCTRL2 are UNDEFINED.

If ERRSEL<SEL> is not the index of the first error record owned by a node, then ERR<n>CTRL[63:32] is not present, meaning reads and writes of ERXCTRL2 are RES0.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXCTLR2;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXCTLR2;
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXCTLR2;
    endif
else
    return ERXCTLR2;
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        ERXCTRL2 = R[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        ERXCTRL2 = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor & SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        ERXCTRL2 = R[t];
    endif
ERXFR, Selected Error Record Feature Register

The ERXFR characteristics are:

**Purpose**

Accesses bits \([31:0]\) of ERR\(<n>\)FR for the error record \(<n>\) selected by ERRSELR.SEL.

**Configuration**

AArch32 System register ERXFR bits \([31:0]\) are architecturally mapped to AArch64 System register ERXFR_EL1[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXFR are UNDEFINED.

**Attributes**

ERXFR is a 32-bit register.

**Field descriptions**

The ERXFR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Bits [31:0] of ERR\(<n>\)FR |

**Bits [31:0]**

ERXFR accesses bits [31:0] of ERR\(<n>\)FR, where \(<n>\) is the value in ERRSELR.SEL.

**Accessing the ERXFR**

If ERRIDR.NUM == 0x0000 or ERRSELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXFR is RAZ.
- Direct reads of ERXFR are NOPs.
- Direct reads of ERXFR are UNDEFINED.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXFR;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXFR;
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXFR;
    endif
ERXFR2, Selected Error Record Feature Register 2

The ERXFR2 characteristics are:

**Purpose**

Accesses bits [63:32] of ERR<n>FR for the error record <n> selected by ERRSELR.SEL.

**Configuration**

AArch32 System register ERXFR2 bits [31:0] are architecturally mapped to AArch64 System register ERXFR_EL1[63:32].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXFR2 are UNDEFINED.

**Attributes**

ERXFR2 is a 32-bit register.

**Field descriptions**

The ERXFR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:32]**

ERXFR2 accesses bits [63:32] of ERR<n>FR, where <n> is the value in ERRSELR.SEL.

**Accessing the ERXFR2**

If ERRIDR.NUM == 0x0000 or ERRSELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXFR2 is RAZ.
- Direct reads of ERXFR2 are NOPs.
- Direct reads of ERXFR2 are UNDEFINED.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
   elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      UNDEFINED;
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
         UNDEFINED;
      else
         AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
         if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
         else
            return ERXFR2;
         elsif PSTATE.EL == EL2 then
            if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
               UNDEFINED;
            elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
               UNDEFINED;
            elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
               if Halted() && EDSCR.SDD == '1' then
                  UNDEFINED;
               else
                  AArch64.AArch32SystemAccessTrap(EL3, 0x03);
               elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
                  if Halted() && EDSCR.SDD == '1' then
                     UNDEFINED;
                  else
                     return ERXFR2;
                  elsif PSTATE.EL == EL3 then
                     if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
                        AArch32.TakeMonitorTrapException();
                     else
                        return ERXFR2;
                     end if
                  end if
               else
                  return ERXFR2;
               end if
            else
               AArch32.TakeMonitorTrapException();
            end if
         else
            return ERXFR2;
         end if
      end if
   end if
else
   return ERXFR2;
end if
ERXMISC0, Selected Error Record Miscellaneous Register 0

The ERXMISC0 characteristics are:

**Purpose**

Accesses bits [31:0] of \( \text{ERR}<n>\text{MISC0} \) for the error record \(<n>\) selected by \( \text{ERRSELR}.\ SEL \).

**Configuration**

AArch32 System register ERXMISC0 bits [31:0] are architecturally mapped to AArch64 System register \( \text{ERXMISC0}_{\ EL1}[31:0] \).

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC0 are UNDEFINED.

**Attributes**

ERXMISC0 is a 32-bit register.

**Field descriptions**

The ERXMISC0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Bits [31:0] of \( \text{ERR}<n>\text{MISC0} \) |

**Bits [31:0]**

ERXMISC0 accesses bits [31:0] of \( \text{ERR}<n>\text{MISC0} \), where \(<n>\) is the value in \( \text{ERRSELR}.\ SEL \).

**Accessing the ERXMISC0**

If \( \text{ERRIDR}.\ NUM == 0x0000 \) or \( \text{ERRSELR}.\ SEL \) is set to a value greater than or equal to \( \text{ERRIDR}.\ NUM \), then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC0 is RAZ/WI.
- Direct reads and writes of ERXMISC0 are NOPs.
- Direct reads and writes of ERXMISC0 are UNDEFINED.

\( \text{ERR}<n>\text{MISC0} \) describes additional constraints that also apply when \( \text{ERR}<n>\text{MISC0} \) is accessed through ERXMISC0.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>\} \text{<coproc>, \{#<opc1>, \ <Rt>, \ <CRn>, \ <CRm>{, \ {#<opc2>}}}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    else
        return ERXMISC0;
    end else
else
    return ERXMISC0;
end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    else
        return ERXMISC0;
    end if
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXMISC0;
    end if
else
    return ERXMISC0;
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC0 = R[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC0 = R[t];
  endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERXMISC0 = R[t];
  endif
ERXMISC1, Selected Error Record Miscellaneous Register 1

The ERXMISC1 characteristics are:

**Purpose**

Accesses bits [63:32] of ERR\(n\)MISC0 for the error record \(n\) selected by ERXSELR.SEL.

**Configuration**

AArch32 System register ERXMISC1 bits [31:0] are architecturally mapped to AArch64 System register ERXMISC0_EL1[63:32].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC1 are UNDEFINED.

**Attributes**

ERXMISC1 is a 32-bit register.

**Field descriptions**

The ERXMISC1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
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</tr>
</tbody>
</table>

*Bits [63:32] of ERR\(n\)MISC0*

**Bits [31:0]**

ERXMISC1 accesses bits [63:32] of ERR\(n\)MISC0, where \(n\) is the value in ERXSELR.SEL.

**Accessing the ERXMISC1**

If ERRIDR.NUM == 0x0000 or ERXSELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC1 is RAZ/WI.
- Direct reads and writes of ERXMISC1 are NOPs.
- Direct reads and writes of ERXMISC1 are UNDEFINED.

ERR\(n\)MISC0 describes additional constraints that also apply when ERR\(n\)MISC0 is accessed through ERXMISC1.

Accesses to this register use the following encodings:

\[ \text{MRC\{<c>\}{<q>}} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>}} \}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            end else
                return ERXMISC1;
        end if
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && ELUsingAArch32(EL3) && SCR.TERR == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch32.TakeMonitorTrapException();
                end if
            else
                return ERXMISC1;
        end if
    elsif PSTATE.EL == EL3 then
        if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
            AArch32.TakeMonitorTrapException();
        else
            return ERXMISC1;
        end if
end if

MCR{<c>}{<q> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm}, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
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<th>CRn</th>
<th>CRm</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elselse
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elselse
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC1 = R[t];
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elselse
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elselse
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC1 = R[t];
  elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC1 = R[t];
The ERXMISC2 characteristics are:

**Purpose**

Accesses bits [31:0] of ERR<n>MISC1 for the error record <n> selected by ERRSELR.SEL.

**Configuration**

AArch32 System register ERXMISC2 bits [31:0] are architecturally mapped to AArch64 System register ERXMISC1_EL1[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC2 are UNDEFINED.

**Attributes**

ERXMISC2 is a 32-bit register.

**Field descriptions**

The ERXMISC2 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [31:0] of ERR&lt;n&gt;MISC1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:0]**

ERXMISC2 accesses bits [31:0] of ERR<n>MISC1, where <n> is the value in ERRSELR.SEL.

**Accessing the ERXMISC2**

If ERRIDR.NUM == 0x0000 or ERRSELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC2 is RAZ/WI.
- Direct reads and writes of ERXMISC2 are NOPs.
- Direct reads and writes of ERXMISC2 are UNDEFINED.

ERR<n>MISC1 describes additional constraints that also apply when ERR<n>MISC1 is accessed through ERXMISC2.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  UNDEFINED;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() == M32_Monitor && SCR.TERR == '1' then
    UNDEFINED;
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  if Halted() & EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch32.TakeMonitorTrapException();
else
  return ERXMISC2;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
else
  AArch32.TakeMonitorTrapException();
else
  return ERXMISC2;
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
else
  return ERXMISC2;

MCR{<c>}{<q>}: coproc, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC2 = R[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC2 = R[t];
  endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERXMISC2 = R[t];
  endif
The ERXMISC3 characteristics are:

**Purpose**

Accesses bits [63:32] of ERR<n>MISC1 for the error record <n> selected by ERRSEL.R SEL.

**Configuration**

AArch32 System register ERXMISC3 bits [31:0] are architecturally mapped to AArch64 System register ERXMISC1_EL1[63:32].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXMISC3 are UNDEFINED.

**Attributes**

ERXMISC3 is a 32-bit register.

**Field descriptions**

The ERXMISC3 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:0]**

ERXMISC3 accesses bits [63:32] of ERR<n>MISC1, where <n> is the value in ERRSEL.R SEL.

**Accessing the ERXMISC3**

If ERRIDR.NUM == 0x0000 or ERRSEL.R SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC3 is RAZ/WI.
- Direct reads and writes of ERXMISC3 are NOPs.
- Direct reads and writes of ERXMISC3 are UNDEFINED.

ERR<n>MISC1 describes additional constraints that also apply when ERR<n>MISC1 is accessed through ERXMISC3.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXMISC3;
    endif
else
    AArch32.TakeMonitorTrapException();
else
    return ERXMISC3;
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeHypTrapException(0x03);
      endif
    endif
  endif
else
  AArch32.TakeMonitorTrapException();
endif
else
  if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      endif
    endif
  else
    AArch32.TakeMonitorTrapException();
  endif
else
  ERXMISC3 = R[t];
else
  if PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC3 = R[t];
    endif
  else
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC3 = R[t];
    endif
  endif
endif
ERXMISC4, Selected Error Record Miscellaneous Register 4

The ERXMISC4 characteristics are:

**Purpose**

Accesses bits [31:0] of ERR<n>MISC2 for the error record <n> selected by ERRELR.SEL.

**Configuration**

AArch32 System register ERXMISC4 bits [31:0] are architecturally mapped to AArch64 System register ERXMISC2_EL1[31:0].

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXMISC4 are UNDEFINED.

**Attributes**

ERXMISC4 is a 32-bit register.

**Field descriptions**

The ERXMISC4 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ERR&lt;n&gt;MISC2[31]</td>
<td>Access bit</td>
</tr>
<tr>
<td>30</td>
<td>ERR&lt;n&gt;MISC2[29]</td>
<td>Access bit</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>ERR&lt;n&gt;MISC2[0]</td>
<td>Access bit</td>
</tr>
</tbody>
</table>

**Accessing the ERXMISC4**

If ERRIDR.NUM == 0x0000 or ERRELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC4 is RAZ/WI.
- Direct reads and writes of ERXMISC4 are NOPs.
- Direct reads and writes of ERXMISC4 are UNDEFINED.

ERR<n>MISC2 describes additional constraints that also apply when ERR<n>MISC2 is accessed through ERXMISC4.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc}>\,\{#<opc1>\},\ <Rt>,\ <CRn>,\ <CRm>\{,\ \{#<opc2>\}\}
\]

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      return ERXMISC4;
    end;
  else
    return ERXMISC4;
  endif
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end;
    else
      AArch32.TakeMonitorTrapException();
    end;
  else
    return ERXMISC4;
  endif
elseif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end;
    else
      return ERXMISC4;
    endif
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end;
    else
      return ERXMISC4;
    endif
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end;
    else
      return ERXMISC4;
    endif
end;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<p>| | | | | |</p>
<table>
<thead>
<tr>
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<td>0b0101</td>
<td>0b0101</td>
<td>0b010</td>
</tr>
</tbody>
</table>

ERXMISC4, Selected Error Record Miscellaneous Register 4
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        ERXMISC4 = R[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        ERXMISC4 = R[t];
    end if;
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        ERXMISC4 = R[t];
    end if;
else
    ERXMISC4 = R[t];
end if;
ERXMISC5, Selected Error Record Miscellaneous Register 5

The ERXMISC5 characteristics are:

**Purpose**

Accesses bits [63:32] of \(\text{ERR}<n>MISC2\) for the error record \(<n>\) selected by \(\text{ERRSELR}.\SEL\).

**Configuration**

AArch32 System register ERXMISC5 bits [31:0] are architecturally mapped to AArch64 System register \(\text{ERXMISC2_EL1}[63:32]\).

This register is present only when \(\text{FEAT_RASv1p1}\) is implemented. Otherwise, direct accesses to ERXMISC5 are UNDEFINED.

**Attributes**

ERXMISC5 is a 32-bit register.

**Field descriptions**

The ERXMISC5 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|                |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [31:0]**

ERXMISC5 accesses bits [63:32] of \(\text{ERR}<n>MISC2\), where \(<n>\) is the value in \(\text{ERRSELR}.\SEL\).

**Accessing the ERXMISC5**

If \(\text{ERRIDR}.\NUM == 0x0000\) or \(\text{ERRSELR}.\SEL\) is set to a value greater than or equal to \(\text{ERRIDR}.\NUM\), then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC5 is RAZ/WI.
- Direct reads and writes of ERXMISC5 are NOPs.
- Direct reads and writes of ERXMISC5 are UNDEFINED.

\(\text{ERR}<n>MISC2\) describes additional constraints that also apply when \(\text{ERR}<n>MISC2\) is accessed through ERXMISC5.

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\{, \{#\}<\text{opc2}\}} \]

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<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    return ERXMISC5;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    return ERXMISC5;
  endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ERXMISC5;
  endif
else
  return ERXMISC5;
endif

 designate
\[ \text{MCR}\{<c>}\{<q>\} <\text{coproc}, \{\#}\{\text{opc1}\}, <\text{Rt}, <\text{CRn}, <\text{CRm}\{, \{\#}\{\text{opc2}\}\}\} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ERXMISC5 = R[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ERXMISC5 = R[t];
  end if
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERXMISC5 = R[t];
  end if
The ERXMISC6 characteristics are:

**Purpose**

Accesses bits [31:0] of \( \text{ERR}<n>MISC3 \) for the error record \(<n>\) selected by ERRELR.SEL.

**Configuration**

AArch32 System register ERXMISC6 bits [31:0] are architecturally mapped to AArch64 System register \( \text{ERXMISC3\_EL1}[31:0] \).

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXMISC6 are UNDEFINED.

**Attributes**

ERXMISC6 is a 32-bit register.

**Field descriptions**

The ERXMISC6 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Bits [31:0] of ( \text{ERR}&lt;n&gt;MISC3 )</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

ERXMISC6 accesses bits [31:0] of \( \text{ERR}<n>MISC3 \), where \(<n>\) is the value in ERRELR.SEL.

**Accessing the ERXMISC6**

If ERRIDR.NUM == 0x0000 or ERRELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An UNKNOWN error record is selected.
- ERXMISC6 is RAZ/WI.
- Direct reads and writes of ERXMISC6 are NOPs.
- Direct reads and writes of ERXMISC6 are UNDEFINED.

\( \text{ERR}<n>MISC3 \) describes additional constraints that also apply when \( \text{ERR}<n>MISC3 \) is accessed through ERXMISC6.

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\} \{<q>\} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
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<tbody>
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<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TERR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR2.TERR == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXMISC6;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.TERR == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ERXMISC6;
    endif
elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor & SCR.TERR == '1' then
        AArch32.TakeMonitorTrapException();
    else
        return ERXMISC6;
    endif
else
    return ERXMISC6;
end

MCR{<c>}{<q>}{<coproc>}{(#)<opc1>},{<Rt>},{<CRn>},{(#)<CRm>}{(<#)<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
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<th>CRm</th>
<th>opc2</th>
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<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ERXMISC6 = R[t];
  end if
else
  PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end if
    else
      ERXMISC6 = R[t];
    end if
  elsif PSTATE.EL == EL3 then
    if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
      AArch32.TakeMonitorTrapException();
    else
      ERXMISC6 = R[t];
    end if
  else
    ERXMISC6 = R[t];
  end if
**ERXMISC7, Selected Error Record Miscellaneous Register 7**

The ERXMISC7 characteristics are:

### Purpose

Accesses bits [63:32] of ERR<n>MISC3 for the error record <n> selected by ERRSELR.SEL.

### Configuration

AArch32 System register ERXMISC7 bits [31:0] are architecturally mapped to AArch64 System register ERXMISC3_EL1[63:32].

This register is present only when FEAT_RASv1p1 is implemented. Otherwise, direct accesses to ERXMISC7 are **UNDEFINED**.

### Attributes

ERXMISC7 is a 32-bit register.

### Field descriptions

The ERXMISC7 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [63:32] of ERR<n>MISC3**

**Bits [31:0]**

ERXMISC7 accesses bits [63:32] of ERR<n>MISC3, where <n> is the value in ERRSELR.SEL.

### Accessing the ERXMISC7

If ERRIDR.NUM == 0x0000 or ERRSELR.SEL is set to a value greater than or equal to ERRIDR.NUM, then one of the following occurs:

- An **UNKNOWN** error record is selected.
- ERXMISC7 is RAZ/WI.
- Direct reads and writes of ERXMISC7 are NOPs.
- Direct reads and writes of ERXMISC7 are **UNDEFINED**.

ERR<n>MISC3 describes additional constraints that also apply when ERR<n>MISC3 is accessed through ERXMISC7.

Accesses to this register use the following encodings:

\[\text{MRC}\{<c}\}{<q}>\ <\text{coproc}, \{#}\<\text{opc1}, \ <\text{Rt}, \ <\text{CRn}, \ <\text{CRm}\{, \{#}\<\text{opc2}\}\}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0101</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end
    return ERXMISC7;
  else
    AArch32.TakeMonitorTrapException();
    return ERXMISC7;
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end
    return ERXMISC7;
  else
    return ERXMISC7;
  end
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ERXMISC7;
  end
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}</c>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC7 = R[t];
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    ERXMISC7 = R[t];
  endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERXMISC7 = R[t];
  endif
else
  ERXMISC7 = R[t];
The ERXSTATUS characteristics are:

**Purpose**

Accesses bits [31:0] of \texttt{ERR<n>STATUS} for the error record selected by \texttt{ERRSELR.SEL}.

**Configuration**

AArch32 System register ERXSTATUS bits [31:0] are architecturally mapped to AArch64 System register \texttt{ERXSTATUS_EL1[31:0]}.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to ERXSTATUS are UNDEFINED.

**Attributes**

ERXSTATUS is a 32-bit register.

**Field descriptions**

The ERXSTATUS bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**Bits [31:0]**

ERXSTATUS accesses bits [31:0] of \texttt{ERR<n>STATUS}, where \(n\) is the value in \texttt{ERRSELR.SEL}.

**Accessing the ERXSTATUS**

If \texttt{ERRIDR.NUM} == 0 or \texttt{ERRSELR.SEL} is set to a value greater than or equal to \texttt{ERRIDR.NUM}, then one of the following occurs:

- An \texttt{UNKNOWN} record is selected.
- ERXSTATUS is RAZ/WI.
- Direct reads and writes of ERXSTATUS are NOPs.
- Direct reads and writes of ERXSTATUS are UNDEFINED.

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\} \{<q>\} <\text{coproc}>, \{#<opc1>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<opc2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end;
else
  return ERXSTATUS;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end;
else
  return ERXSTATUS;
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ERXSTATUS;
end;

MCR{<c>{<q> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

ERXSTATUS, Selected Error Record Primary Status Register
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TERR == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TERR == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  end if
else
  ERXSTATUS = R[t];
end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL3) && SCR_EL3.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif EL2Enabled() && ELUsingAArch32(EL3) && SCR.TERR == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  end if
else
  ERXSTATUS = R[t];
end if
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SCR.TERR == '1' then
    AArch32.TakeMonitorTrapException();
  else
    ERXSTATUS = R[t];
  end if
end if
FCSEIDR, FCSE Process ID register

The FCSEIDR characteristics are:

**Purpose**

Identifies whether the Fast Context Switch Extension (FCSE) is implemented.

From Armv8, the FCSE is not implemented, so this register is RAZ/WI. Software can access this register to determine that the implementation does not include the FCSE.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to FCSEIDR are UNDEFINED.

**Attributes**

FCSEIDR is a 32-bit register.

**Field descriptions**

The FCSEIDR bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9  | Bit 8  | Bit 7  | Bit 6  | Bit 5  | Bit 4  | Bit 3  | Bit 2  | Bit 1  | Bit 0  |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
|        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
| RAZ/WI |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

**Bits [31:0]**

Reserved, RAZ/WI.

**Accessing the FCSEIDR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} {coproc}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

```java
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
      AArch32.TakeHypTrapException(0x03);
   else
      return FCSEIDR;
   endif
elsif PSTATE.EL == EL2 then
   return FCSEIDR;
elsif PSTATE.EL == EL3 then
   return FCSEIDR;
```

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FCSEIDR, FCSE Process ID register

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    FCSEIDR = R[t];
  end
elsif PSTATE.EL == EL2 then
  FCSEIDR = R[t];
elsif PSTATE.EL == EL3 then
  FCSEIDR = R[t];

FPEXC, Floating-Point Exception Control register

The FPEXC characteristics are:

**Purpose**

Provides a global enable for the implemented Advanced SIMD and floating-point functionality, and reports floating-point status information.

**Configuration**

AArch32 System register FPEXC bits [31:0] are architecturally mapped to AArch64 System register FPEXC32_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to FPEXC are UNDEFINED.

Implemented only if the implementation includes the Advanced SIMD and floating-point functionality.

**Attributes**

FPEXC is a 32-bit register.

**Field descriptions**

The FPEXC bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EX | EN | DEX | FP2V | VV | TFV | RES0 | VECITR | DF | RES0 | XF | UFF | OFF | DZF | IOF |

**EX, bit [31]**

Exception bit. From Armv8, this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EN, bit [30]**

Enables access to the Advanced SIMD and floating-point functionality from all Exception levels, except that setting this field to 0 does not disable the following:

- VMSR accesses to the FPEXC or FPSID.
- VMRS accesses from the FPEXC, FPSID, MVFR0, MVFR1, or MVFR2.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to the FPSR, and any of the SIMD and floating-point registers Q0-Q15, including their views as D0-D31 registers or S0-S31 registers, are UNDEFINED at all Exception levels.</td>
</tr>
<tr>
<td>0b1</td>
<td>This control permits access to the Advanced SIMD and floating-point functionality at all Exception levels.</td>
</tr>
</tbody>
</table>

Execution of floating-point and Advanced SIMD instructions in AArch32 state can be disabled or trapped by the following controls:

- CPACR.cp10, or, if executing at EL0, CPACR_EL1.FPEN.
- FPEXC.EN.
- If executing in Non-secure state:
  - HCPR.TCP10, or if EL2 is using AArch64, CPTR_EL2.TFP.
  - NSACR.cp10, or if EL3 is using AArch64, CPTR_EL3.TFP.
- For Advanced SIMD instructions only:
See the descriptions of the controls for more information.

Note

When executing at EL0 using AArch32:

- If EL1 is using AArch64 then behavior is as if the value of FPEXC.EN is 1.
- If EL2 is using AArch64 and enabled in the current Security state, and the value of HCR_EL2.{RW, TGE} is \{1, 1\}, then the behavior is as if the value of FPEXC.EN is 1.
- If EL2 is using AArch64 and enabled in the current Security state, and the value of HCR_EL2.{RW, TGE} is \{0, 1\}, then it is IMPLEMENTATION DEFINED whether the behavior is:
  - As if the value of FPEXC.EN is 1.
  - Determined by the value of FPEXC.EN, as described in this field description. However, Arm deprecates using the value of FPEXC.EN to determine behavior.

On a Warm reset, this field resets to 0.

**DEX, bit [29]**

Defined synchronous exception on floating-point execution.

This field identifies whether a synchronous exception generated by the attempted execution of an instruction was generated by an unallocated encoding. The instruction must be in the encoding space that is identified by the pseudocode function ExecutingCP10or11Instr() returning TRUE. This field also indicates whether the FPEXC.TFV field is valid.

The meaning of this bit is:

<table>
<thead>
<tr>
<th>DEX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The exception was generated by the attempted execution of an unallocated instruction in the encoding space that is identified by the pseudocode function ExecutingCP10or11Instr(). If FPEXC.TFV is RW then it is invalid and UNKNOWN. If FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} are RW then they are invalid and UNKNOWN.</td>
</tr>
<tr>
<td>0b1</td>
<td>The exception was generated during the execution of an unallocated encoding. FPEXC.TFV is valid and indicates the cause of the exception.</td>
</tr>
</tbody>
</table>

On an exception that sets this bit to 1 the exception-handling routine must clear this bit to 0.

On an implementation that both does not support trapping of floating-point exceptions and implements the FPSCR.{Stride, Len} fields as RAZ, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**FP2V, bit [28]**

FPINST2 instruction valid bit. From Armv8, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VV, bit [27]**

VECITR valid bit. From Armv8, this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**TFV, bit [26]**

Trapped Fault Valid bit. Valid only when the value of FPEXC.DEX is 1. When valid, it indicates the cause of the exception and therefore whether the FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} bits are valid.

<table>
<thead>
<tr>
<th>TFV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The exception was caused by the execution of a floating-point VABS, VADD, VDIV, VFMA, VFMS, VFNMA, VFNMS, VMLA, VMLS, VMOV, VMUL, VNEG, VNMLA, VNMLS, VNMUL, VSQRT, or VSUB instruction when one or both of FPSCR.{Stride, Len} was non-zero. If the FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} bits are RW then they are invalid and UNKNOWN.</td>
</tr>
<tr>
<td>0b1</td>
<td>FPEXC.{IDF, IXF, UFF, OFF, DZF, IOF} indicate the presence of trapped floating-point exceptions that had occurred at the time of the exception. Bits are set for all trapped exceptions that had occurred at the time of the exception.</td>
</tr>
</tbody>
</table>

This bit returns a status value and ignores writes.

When the value of FPEXC.DEX is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On an implementation that supports the trapping of floating-point exceptions and implements FPSCR.{Stride, Len} as RAZ, this bit is RAO/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [25:11]**

Reserved, RES0.

**VECITR, bits [10:8]**

Vector iteration count. From Armv8, this field is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IDF, bit [7]**

Input Denormal trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Input Denormal exception occurred while FPSCR.IDE was 1:

<table>
<thead>
<tr>
<th>IDF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input Denormal exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input Denormal exception has occurred.</td>
</tr>
</tbody>
</table>

Input Denormal exceptions can occur only when FPSCR.FZ is 1.

**Note**

A half-precision floating-point value that is flushed to zero because the value of FPSCR.FZ16 is 1 does not generate an Input Denormal exception.

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and UNKNOWN.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [6:5]**

Reserved, RES0.
**IXF, bit [4]**

Inexact trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Inexact exception occurred while FPSCR.IXE was 1:

<table>
<thead>
<tr>
<th>IXF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Inexact exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Inexact exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and **UNKNOWN**.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**UFF, bit [3]**

Underflow trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Underflow exception occurred while FPSCR.UFE was 1:

<table>
<thead>
<tr>
<th>UFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow exception has occurred.</td>
</tr>
</tbody>
</table>

Underflow trapped exceptions can occur:

- On half-precision data-processing instructions only when FPSCR.FZ16 is 0.
- Otherwise only when FPSCR.FZ is 0.

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and **UNKNOWN**.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**OFF, bit [2]**

Overflow trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Overflow exception occurred while FPSCR.OFE was 1:

<table>
<thead>
<tr>
<th>OFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Overflow exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overflow exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and **UNKNOWN**.

On an implementation that does not support the trapping of floating-point exceptions this bit is RAZ/WI.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DZF, bit [1]**

Divide by Zero trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether a Divide by Zero exception occurred while FPSCR.DZE was 1:

<table>
<thead>
<tr>
<th>DZF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Divide by Zero exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Divide by Zero exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.
When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and **UNKNOWN**.

On an implementation that does not support the trapping of floating-point exceptions this bit is **RAZ/WI**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IOF, bit [0]**

Invalid Operation trapped exception bit. Valid only when the value of FPEXC.TFV is 1. When valid, it indicates whether an Invalid Operation exception occurred while **FPSCR.IOE** was 1:

<table>
<thead>
<tr>
<th>IOF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalid Operation exception has not occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalid Operation exception has occurred.</td>
</tr>
</tbody>
</table>

This bit must be cleared to 0 by the exception-handling routine.

When the value of FPEXC.TFV is 0 and this bit is RW, this bit is invalid and **UNKNOWN**.

On an implementation that does not support the trapping of floating-point exceptions this bit is **RAZ/WI**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the FPEXC**

Accesses to this register use the following encodings:

```
VMRS{<c>}{<q>} <Rt>, <spec_reg>
```

<table>
<thead>
<tr>
<th>reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1000</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x07);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x07);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
    AArch32.TakeHypTrapException(0x08);
  else
    return FPEXC;
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
      AArch32.TakeHypTrapException(0x00);
    else
      return FPEXC;
  elsif PSTATE.EL == EL3 then
    if CPACR.cp10 == '00' then
      UNDEFINED;
    else
      return FPEXC;
```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') ||
        HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    else
        FPEXC = R[t];
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') ||
            HCPTR.TCP10 == '1') then
            AArch32.TakeHypTrapException(0x00);
        else
            FPEXC = R[t];
        elsif PSTATE.EL == EL3 then
            if CPACR.cp10 == '00' then
                UNDEFINED;
            else
                FPEXC = R[t];
            end
        end
FPSCR, Floating-Point Status and Control Register

The FPSCR characteristics are:

**Purpose**

Provides floating-point system status information and control.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to FPSCR are UNDEFINED.

The named fields in this register map to the equivalent fields in the AArch64 FPCR and FPSR.

It is IMPLEMENTATION DEFINED whether the Len and Stride fields can be programmed to non-zero values, which will cause some AArch32 floating-point instruction encodings to be UNDEFINED, or whether these fields are RAZ.

Implemented only if the implementation includes the Advanced SIMD and floating-point functionality.

**Attributes**

FPSCR is a 32-bit register.

**Field descriptions**

The FPSCR bit assignments are:

```
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31
N Z C V QC AH D N FZRMode Stride FZ16 Len DERES0 I XE UF E0 F DZE10E IDCR E0 X C U F C O F CD ZC IO C
```

**N, bit [31]**

Negative condition flag. This is updated by floating-point comparison operations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero condition flag. This is updated by floating-point comparison operations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry condition flag. This is updated by floating-point comparison operations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow condition flag. This is updated by floating-point comparison operations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**QC, bit [27]**

Cumulative saturation bit, Advanced SIMD only. This bit is set to 1 to indicate that an Advanced SIMD integer operation has saturated since 0 was last written to this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**AHP, bit [26]**

Alternative half-precision control bit:

<table>
<thead>
<tr>
<th>AHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IEEE half-precision format selected.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alternative half-precision format selected.</td>
</tr>
</tbody>
</table>

This bit is used only for conversions between half-precision floating-point and other floating-point formats.

The data-processing instructions added as part of the FEAT_FP16 extension always use the IEEE half-precision format, and ignore the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DN, bit [25]**

Default NaN mode control bit:

<table>
<thead>
<tr>
<th>DN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>NaN operands propagate through to the output of a floating-point operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any operation involving one or more NaNs returns the Default NaN.</td>
</tr>
</tbody>
</table>

The value of this bit controls only scalar floating-point arithmetic. Advanced SIMD arithmetic always uses the Default NaN setting, regardless of the value of the DN bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**FZ, bit [24]**

Flush-to-zero mode control bit:

<table>
<thead>
<tr>
<th>FZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Flush-to-zero mode disabled. Behavior of the floating-point system is fully compliant with the IEEE 754 standard.</td>
</tr>
<tr>
<td>0b1</td>
<td>Flush-to-zero mode enabled.</td>
</tr>
</tbody>
</table>

The value of this bit controls only scalar floating-point arithmetic. Advanced SIMD arithmetic always uses the Flush-to-zero setting, regardless of the value of the FZ bit.

This bit has no effect on half-precision calculations.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**RMode, bits [23:22]**

Rounding Mode control field. The encoding of this field is:

<table>
<thead>
<tr>
<th>RMode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Round to Nearest (RN) mode.</td>
</tr>
<tr>
<td>0b01</td>
<td>Round towards Plus Infinity (RP) mode.</td>
</tr>
<tr>
<td>0b10</td>
<td>Round towards Minus Infinity (RM) mode.</td>
</tr>
<tr>
<td>0b11</td>
<td>Round towards Zero (RZ) mode.</td>
</tr>
</tbody>
</table>

The specified rounding mode is used by almost all scalar floating-point instructions. Advanced SIMD arithmetic always uses the Round to Nearest setting, regardless of the value of the RMode bits.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Stride, bits [21:20]**

It is **IMPLEMENTATION DEFINED** whether this field is RW or RAZ.

If this field is RW and is set to a value other than zero, some floating-point instruction encodings are **UNDEFINED**. The instruction pseudocode identifies these instructions.

Arm strongly recommends that software never sets this field to a value other than zero.

The value of this field is ignored when processing Advanced SIMD instructions.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**FZ16, bit [19]**

*When FEAT_FP16 is implemented:*

Flush-to-zero mode control bit on half-precision data-processing instructions:

<table>
<thead>
<tr>
<th>FZ16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Flush-to-zero mode disabled. Behavior of the floating-point system is fully compliant with the IEEE 754 standard.</td>
</tr>
<tr>
<td>0b1</td>
<td>Flush-to-zero mode enabled.</td>
</tr>
</tbody>
</table>

The value of this bit applies to both scalar and Advanced SIMD floating-point half-precision calculations.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**Len, bits [18:16]**

It is **IMPLEMENTATION DEFINED** whether this field is RW or RAZ.

If this field is RW and is set to a value other than zero, some floating-point instruction encodings are **UNDEFINED**. The instruction pseudocode identifies these instructions.

Arm strongly recommends that software never sets this field to a value other than zero.

The value of this field is ignored when processing Advanced SIMD instructions.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IDE, bit [15]**

Input Denormal floating-point exception trap enable.

<table>
<thead>
<tr>
<th>IDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the IDC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the IDC bit.</td>
</tr>
</tbody>
</table>

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.


**Bits [14:13]**

Reserved, RES0.

**IXE, bit [12]**

Inexact floating-point exception trap enable.

<table>
<thead>
<tr>
<th>IXE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the IXC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the IXC bit.</td>
</tr>
</tbody>
</table>

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**UFE, bit [11]**

Underflow floating-point exception trap enable.

<table>
<thead>
<tr>
<th>UFE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the UFC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs and Flush-to-zero is not enabled, the PE does not update the UFC bit.</td>
</tr>
</tbody>
</table>

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**OFE, bit [10]**

Overflow floating-point exception trap enable.

<table>
<thead>
<tr>
<th>OFE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Untrapped exception handling selected. If the floating-point exception occurs, the OFC bit is set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the OFC bit.</td>
</tr>
</tbody>
</table>

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DZE, bit [9]**

Divide by Zero floating-point exception trap enable.
### DZE, bit [9]

Input Denormal cumulative floating-point exception bit. This bit is set to 1 to indicate that the Input Denormal floating-point exception has occurred since 0 was last written to this bit.

- **0b0**: Untrapped exception handling selected. If the floating-point exception occurs, the DZE bit is set to 1.
- **0b1**: Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the DZE bit.

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### IOE, bit [8]

Invalid Operation floating-point exception trap enable.

- **0b0**: Untrapped exception handling selected. If the floating-point exception occurs, the IOC bit is set to 1.
- **0b1**: Trapped exception handling selected. If the floating-point exception occurs, the PE does not update the IOC bit.

This bit is RW only if the implementation supports the trapping of floating-point exceptions. In an implementation that does not support floating-point exception trapping, this bit is RAZ/WI.

When this bit is RW, it applies only to floating-point operations. Advanced SIMD operations always use untrapped floating-point exception handling in AArch32 state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### IDC, bit [7]

Input Denormal cumulative floating-point exception bit. This bit is set to 1 to indicate that the Input Denormal floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the IDE bit.

Advanced SIMD instructions set this bit if the Input Denormal floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, regardless of the value of the IDE bit.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [6:5]

Reserved, **RES0**.

### IXC, bit [4]

Inexact cumulative floating-point exception bit. This bit is set to 1 to indicate that the Inexact floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the IXE bit.

Advanced SIMD instructions set this bit if the Inexact floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, regardless of the value of the IXE bit.

The criteria for the Inexact floating-point exception to occur are different in Flush-to-zero mode. For details, see 'Flush-to-zero'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
**UFC, bit [3]**

Underflow cumulative floating-point exception bit. This bit is set to 1 to indicate that the Underflow floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the UFE bit.

Advanced SIMD instructions set this bit if the Underflow floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, if FPSCR.UFE is 0 or if Flush-to-zero is enabled.

The criteria for the Underflow floating-point exception to occur are different in Flush-to-zero mode. For details, see 'Flush-to-zero'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**OFC, bit [2]**

Overflow cumulative floating-point exception bit. This bit is set to 1 to indicate that the Overflow floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the OFE bit.

Advanced SIMD instructions set this bit if the Overflow floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, regardless of the value of the OFE bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**DZC, bit [1]**

Divide by Zero cumulative floating-point exception bit. This bit is set to 1 to indicate that the Divide by Zero floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the DZE bit.

Advanced SIMD instructions set this bit if the Divide by Zero floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, regardless of the value of the DZE bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IOC, bit [0]**

Invalid Operation cumulative floating-point exception bit. This bit is set to 1 to indicate that the Invalid Operation floating-point exception has occurred since 0 was last written to this bit.

How VFP instructions update this bit depends on the value of the IOE bit.

Advanced SIMD instructions set this bit if the Invalid Operation floating-point exception occurs in one or more of the floating-point calculations performed by the instruction, regardless of the value of the IOE bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the FPSCR**

Accesses to this register use the following encodings:

\[
\text{VMRS\{<c>\}{<q>\}} \ <Rt>, \ <\text{spec\_reg}> 
\]

<table>
<thead>
<tr>
<th>reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x00);
  else
    AArch64.AArch32SystemAccessTrap(EL1, 0x07);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x07);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x07);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x07);
  elsif EL2Enabled() && ELUsingAArch32(EL1) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
    AArch32.TakeHypTrapException(0x08);
  else
    return FPSCR;
else
  elsif PSTATE.EL == EL1 then
    if CPACR_EL1.FPEN == 'x0' then
      AArch64.AArch32SystemAccessTrap(EL1, 0x07);
    elsif (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
      UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
      AArch32.TakeHypTrapException(0x08);
    else
      return FPSCR;
else
  elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00') then
      AArch32.TakeHypTrapException(0x08);
    else
      return FPSCR;
else
  elsif PSTATE.EL == EL3 then
    if CPACR.cp10 == '00' then
      UNDEFINED;
    else
      return FPSCR;
end if

VMSR{<c>}{<q>} <spec_reg>, <Rt>

<table>
<thead>
<tr>
<th>reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
</tr>
</tbody>
</table>

FPSCR, Floating-Point Status and Control Register
if PSTATE.EL == EL0 then
    if !ELUsingAArch32(EL1) && !EL2Enabled() && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x00);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x07);
    end if
    else EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '11' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    else
default
    end if
else
    if PSTATE.EL == EL1 then
        if CPACR_EL1.FPEN == '0x' then
            AArch64.AArch32SystemAccessTrap(EL1, 0x07);
        else
            if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '0x' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL2, 0x07);
            end if
        end if
    else
        if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        else
            if HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x07);
            else
                if EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
                    AArch32.TakeHypTrapException(0x08);
                else
                    FPSCR = R[t];
                end if
            end if
        end if
    else
        if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        else
            if HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x07);
            else
                if EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
                    AArch32.TakeHypTrapException(0x08);
                else
                    FPSCR = R[t];
                end if
            end if
        end if
    else
        if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        else
            if HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x07);
            else
                if EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
                    AArch32.TakeHypTrapException(0x08);
                else
                    FPSCR = R[t];
                end if
            end if
        end if
    end if
end if

The FPSID characteristics are:

**Purpose**

Provides top-level information about the floating-point implementation.

This register largely duplicates information held in the MIDR. Arm deprecates use of it.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to FPSID are UNDEFINED.

Implemented only if the implementation includes the Advanced SIMD and floating-point functionality.

**Attributes**

FPSID is a 32-bit register.

**Field descriptions**

The FPSID bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Implementer</td>
</tr>
<tr>
<td>30</td>
<td>SW</td>
</tr>
<tr>
<td>29</td>
<td>Subarchitecture</td>
</tr>
<tr>
<td>28</td>
<td>PartNum</td>
</tr>
<tr>
<td>27</td>
<td>Variant</td>
</tr>
<tr>
<td>26</td>
<td>Revision</td>
</tr>
</tbody>
</table>

**Implementer, bits [31:24]**

Implementer codes are the same as those used for the MIDR.

For an implementation by Arm this field is 0x41, the ASCII code for A.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SW, bit [23]**

Software bit. Defined values are:

<table>
<thead>
<tr>
<th>SW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation provides a hardware implementation of the floating-point instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports only software emulation of the floating-point instructions.</td>
</tr>
</tbody>
</table>

In Armv8-A, the only permitted value is 0b0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Subarchitecture, bits [22:16]**

Subarchitecture version number. For an implementation by Arm, defined values are:
### Subarchitecture

<table>
<thead>
<tr>
<th>Subarchitecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000000</td>
<td>VFPv1 architecture with an IMPLEMENTATION DEFINED subarchitecture.</td>
</tr>
<tr>
<td>0b00000001</td>
<td>VFPv2 architecture with Common VFP subarchitecture v1.</td>
</tr>
<tr>
<td>0b00000100</td>
<td>VFPv3 architecture, or later, with Common VFP subarchitecture v2. The VFP architecture version is indicated by the MVFR0 and MVFR1 registers.</td>
</tr>
<tr>
<td>0b00000111</td>
<td>VFPv3 architecture, or later, with Null subarchitecture. The entire floating-point implementation is in hardware, and no software support code is required. The VFP architecture version is indicated by the MVFR0 and MVFR1 registers. This value can be used only by an implementation that does not support the trap enable bits in the FPSCR.</td>
</tr>
<tr>
<td>0b00001000</td>
<td>VFPv3 architecture, or later, with Common VFP subarchitecture v3, and support for trap enable bits in FPSCR. The VFP architecture version is indicated by the MVFR0 and MVFR1 registers.</td>
</tr>
</tbody>
</table>

For a subarchitecture designed by Arm the most significant bit of this field, register bit[22], is 0. Values with a most significant bit of 0 that are not listed here are reserved.

When the subarchitecture designer is not Arm, the most significant bit of this field, register bit[22], must be 1. Each implementer must maintain its own list of subarchitectures it has designed, starting at subarchitecture version number 0x40.

In Armv8-A, the permitted values are 0b00000111 and 0b00001000.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### PartNum, bits [15:8]

An IMPLEMENTATION DEFINED part number for the floating-point implementation, assigned by the implementer.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Variant, bits [7:4]

An IMPLEMENTATION DEFINED variant number. Typically, this field distinguishes between different production variants of a single product.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Revision, bits [3:0]

An IMPLEMENTATION DEFINED revision number for the floating-point implementation.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the FPSID

Accesses to this register use the following encodings:

```
VMRS{<c>}{<q>} <Rt>, <spec_reg>
```

| reg | 0b0000 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsf PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' &&
        NSACR.cp10 == '0') || (CPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x08);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR.NS == '1' && NSACR.cp10 == '0') || CPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    else
        return FPSID;
    elsif PSTATE.EL == EL2 then
        if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x07);
        elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' &&
            NSACR.cp10 == '0') || CPTR.TCP10 == '1') then
            AArch32.TakeHypTrapException(0x08);
        else
            return FPSID;
    elsif PSTATE.EL == EL3 then
        if CPACR.cp10 == '00' then
            UNDEFINED;
        else
            return FPSID;

VMSR{<c>}{<q>} <spec_reg>, <Rt>

| reg | 0b0000 |
if PSTATE.EL == EL0 then
UNDEFINED;
elseif PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    else
        //no operation
    endif
elseif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elseif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    else
        //no operation
    endif
elseif PSTATE.EL == EL3 then
    if CPACR.cp10 == '00' then
        UNDEFINED;
    else
        //no operation
    endif
HACR, Hyp Auxiliary Configuration Register

The HACR characteristics are:

**Purpose**

Controls trapping to Hyp mode of IMPLEMENTATION DEFINED aspects of Non-secure EL1 or EL0 operation.

**Configuration**

AArch32 System register HACR bits [31:0] are architecturally mapped to AArch64 System register HACR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HACR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HACR is a 32-bit register.

**Field descriptions**

The HACR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HACR**

Accesses to this register use the following encodings:

MRC{<c>{<q>}} proc, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b001</td>
<td>0b001</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return HACR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HACR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    HACR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HACR = R[t];
HACTLR, Hyp Auxiliary Control Register

The HACTLR characteristics are:

Purpose

Controls IMPLEMENTATION DEFINED features of Hyp mode operation.

Configuration

AArch32 System register HACTLR bits [31:0] are architecturally mapped to AArch64 System register ACTLR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HACTLR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

Attributes

HACTLR is a 32-bit register.

Field descriptions

The HACTLR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the HACTLR

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#<opc1>}, <Rt>, <CRn>, <CRm>{, {#<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 2433
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return HACTLR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HACTLR;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    HACTLR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HACTLR = R[t];
end if;
HACTLR2, Hyp Auxiliary Control Register 2

The HACTLR2 characteristics are:

**Purpose**

Provides additional space to the HACTLR register to hold IMPLEMENTATION DEFINED trap functionality.

**Configuration**

AArch32 System register HACTLR2 bits [31:0] are architecturally mapped to AArch64 System register ACTLR_EL2[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HACTLR2 are UNDEFINED.

In Armv8.0 and Armv8.1, it is IMPLEMENTATION DEFINED whether this register is implemented, or whether it causes UNDEFINED exceptions when accessed. The implementation of this register can be detected by examining ID_MMFR4.AC2.

From Armv8.2 this register must be implemented.

**Attributes**

HACTLR2 is a 32-bit register.

**Field descriptions**

The HACTLR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td>IMPLEMENTATION DEFINED, bits [31:0]</td>
</tr>
<tr>
<td>29</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>28</td>
<td>On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>

**Accessing the HACTLR2**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return HACTLR2;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HACTLR2;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    HACTLR2 = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HACTLR2 = R[t];
end if;

30/09/2020 15:07; ccadd0cbf0890cecc50268e82aee9e71047211
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HADFSR, Hyp Auxiliary Data Fault Status Register

The HADFSR characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED syndrome information for Data Abort exceptions taken to Hyp mode.

**Configuration**

AArch32 System register HADFSR bits [31:0] are architecturally mapped to AArch64 System register AFSR0_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HADFSR are UNDEFINED.

This is an optional register. An implementation that does not require this register can implement it as RES0.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HADFSR is a 32-bit register.

**Field descriptions**

The HADFSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ![IMPLEMENTATION DEFINED](image.png) |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HADFSR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HADFSR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HADFSR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HADFSR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HADFSR = R[t];
**HAIFSR, Hyp Auxiliary Instruction Fault Status Register**

The HAIFSR characteristics are:

**Purpose**

Provides additional IMPLEMENTATION DEFINED syndrome information for Prefetch Abort exceptions taken to Hyp mode.

**Configuration**

AArch32 System register HAIFSR bits [31:0] are architecturally mapped to AArch64 System register AFSR1_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HAIFSR are UNDEFINED.

This is an optional register. An implementation that does not require this register can implement it as RES0.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HAIFSR is a 32-bit register.

**Field descriptions**

The HAIFSR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HAIFSR**

Accesses to this register use the following encodings:

\[ \text{MRC}\{\langle c\rangle, \langle q\rangle \} \langle \text{coproc}\rangle, \{\#\langle opc1\rangle, \langle Rt\rangle, \langle \text{CRn}\rangle, \langle \text{CRm}\rangle, \{\#\langle opc2\rangle\} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HAIFSR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HAIFSR;
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HAIFSR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HAIFSR = R[t];
endif
HAMAIR0, Hyp Auxiliary Memory Attribute Indirection Register 0

The HAMAIR0 characteristics are:

**Purpose**

Provides implementation defined memory attributes for the memory attribute encodings defined by HMAIR0. These implementation defined attributes can only provide additional qualifiers for the memory attribute encodings, and cannot change the memory attributes defined in HMAIR0.

**Configuration**

AArch32 System register HAMAIR0 bits [31:0] are architecturally mapped to AArch64 System register AMAIR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HAMAIR0 are undefined.

If EL2 is not implemented, this register is res0 from EL3.

**Attributes**

HAMAIR0 is a 32-bit register.

**Field descriptions**

The HAMAIR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>29</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>28</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>27</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>26</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>25</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>24</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>23</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>22</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>21</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>20</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>19</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>18</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>17</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>16</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>15</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>14</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>13</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>12</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>11</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>10</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>9</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>8</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>7</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>6</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>5</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>4</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>3</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>2</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>1</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

If an implementation does not provide any implementation defined memory attributes, this register is res0.

**IMPLEMENTATION DEFINED, bits [31:0]**

- IMPLEMENTATION DEFINED.
- On a Warm reset, this field resets to an architecturally unknown value.

**Accessing the HAMAIR0**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HAMAIR0;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HAMAIR0;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HAMAIR0 = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HAMAIR0 = R[t];
HAMAIR1, Hyp Auxiliary Memory Attribute Indirection Register 1

The HAMAIR1 characteristics are:

**Purpose**

Provides IMPLEMENTATION DEFINED memory attributes for the memory attribute encodings defined by HMAIR1. These IMPLEMENTATION DEFINED attributes can only provide additional qualifiers for the memory attribute encodings, and cannot change the memory attributes defined in HMAIR1.

**Configuration**

AArch32 System register HAMAIR1 bits [31:0] are architecturally mapped to AArch64 System register AMAIR_EL2[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HAMAIR1 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HAMAIR1 is a 32-bit register.

**Field descriptions**

The HAMAIR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED

If an implementation does not provide any IMPLEMENTATION DEFINED memory attributes, this register is RES0.

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HAMAIR1**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 2443
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HAMAIR1;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HAMAIR1;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HAMAIR1 = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HAMAIR1 = R[t];
HCPtr, Hyp Architectural Feature Trap Register

The HCPtr characteristics are:

**Purpose**

Controls:

- Trapping to Hyp mode of Non-secure access, at EL1 or EL0, to trace, and to Advanced SIMD and floating-point functionality.
- Hyp mode access to trace, and to Advanced SIMD and floating-point functionality.

**Note**

Accesses to this functionality:

- From Non-secure modes other than Hyp mode are also affected by settings in the **CPACR** and **NSACR**.
- From Hyp mode are also affected by settings in the **NSACR**.

Exceptions generated by the **CPACR** and **NSACR** controls are higher priority than those generated by the HCPtr controls.

**Configuration**

AArch32 System register HCPtr bits [31:0] are architecturally mapped to AArch64 System register **CPTR_EL2[31:0]**.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HCPtr are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

HCPtr is a 32-bit register.

**Field descriptions**

The HCPtr bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TCPAC | TAM | RES0 | TTA | RES0 | TASE | RES0 | RES1 | TCP11 | TCP10 | RES1 |

**TCPAC, bit [31]**

Traps Non-secure EL1 accesses to the **CPACR** to Hyp mode.

<table>
<thead>
<tr>
<th>TCPAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to the <strong>CPACR</strong> are trapped to Hyp mode.</td>
</tr>
</tbody>
</table>

**Note**

The **CPACR** is not accessible at EL0.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.
TAM, bit [30]

When FEAT_AMUv1 is implemented:

Trap Activity Monitor access. Traps Non-secure EL1 and EL0 accesses to all Activity Monitor registers to EL2.

<table>
<thead>
<tr>
<th>TAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses from Non-secure EL1 and EL0 to Activity Monitor registers are not trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses from Non-secure EL1 and EL0 to Activity Monitor registers are trapped to Hyp mode.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

Bits [29:21]

Reserved, RES0.

TTA, bit [20]

Traps Non-secure System register accesses to all implemented trace registers to Hyp mode.

<table>
<thead>
<tr>
<th>TTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1  | Any Non-secure System register access to an implemented trace register is trapped to Hyp mode, unless the access is trapped to EL1 by a CPACR or NSACR control, or the access is from Non-secure EL0 and the definition of the register in the appropriate trace architecture specification indicates that the register is not accessible from EL0. A trapped instruction generates:  
• A Hyp Trap exception, if the exception is taken from Non-secure EL0 or EL1.  
• An Undefined Instruction exception taken to Hyp mode, if the exception is taken from Hyp mode. |

If the implementation does not include a PE trace unit, or does not include a System register interface to the PE trace unit registers, it is IMPLEMENTATION DEFINED whether this bit:

• Is RES0.
• Is RES1.
• Can be written from Hyp mode, and from Secure Monitor mode when SCR.NS is 1.

If EL3 is implemented and is using AArch32, and the value of NSACR.NSTRCDIS is 1, in Non-secure state this field behaves as RAO/WI, regardless of its actual value.

Note

• The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are UNDEFINED, and a resulting Undefined Instruction exception is higher priority than a HCPT.TTA Hyp Trap exception.  
• The architecture does not provide traps on trace register accesses through the optional memory-mapped debug interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Bits [19:16]

Reserved, RES0.
TASE, bit [15]

Traps Non-secure execution of Advanced SIMD instructions to Hyp mode when the value of HCPTR.TCP10 is 0.

<table>
<thead>
<tr>
<th>TASE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1  | When the value of HCPTR.TCP10 is 0, any attempt to execute an Advanced SIMD instruction in Non-secure state is trapped to Hyp mode, unless it is trapped to EL1 by a CPACR or NSACR control. A trapped instruction generates:  
  • A Hyp Trap exception, if the exception is taken from Non-secure EL0 or EL1.  
  • An Undefined Instruction exception taken to Hyp mode, if the exception is taken from Hyp mode. |

When the value of HCPTR.TCP10 is 1, the value of this field is ignored.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is res1. Otherwise, it is IMPLEMENTATION DEFINED whether this field is implemented as a RW field. If it is not implemented as a RW field, then it is RAZ/WI.

If EL3 is implemented and is using AArch32, and the value of NSACR_NSASEDIS is 1, in Non-secure state this field behaves as RAO/WI, regardless of its actual value. This applies even if the field is implemented as RAZ/WI.

For the list of instructions affected by this field, see ‘Controls of Advanced SIMD operation that do not apply to floating-point operation’.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Bit [14]

Reserved, res0.

Bits [13:12]

Reserved, res1.

TCP11, bit [11]

The value of this field is ignored. If this field is programmed with a different value to the TCP10 bit then this field is UNKNOWN on a direct read of the HCPTR.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is res1.

If EL3 is implemented and is using AArch32, and the value of NSACR_cp10 is 0, in Non-secure state this field behaves as RAO/WI, regardless of its actual value.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

TCP10, bit [10]

Trap Non-secure accesses to Advanced SIMD and floating-point functionality to Hyp mode:

<table>
<thead>
<tr>
<th>TCP10</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
</tbody>
</table>
| 0b1   | Any attempted access to Advanced SIMD and floating-point functionality from Non-secure state is trapped to Hyp mode, unless it is trapped to EL1 by a CPACR or NSACR control. A trapped instruction generates:  
  • A Hyp Trap exception, if the exception is taken from Non-secure EL0 or EL1.  
  • An Undefined Instruction exception taken to Hyp mode, if the exception is taken from Hyp mode. |

The Advanced SIMD and floating-point features controlled by these fields are:
• Execution of any floating-point or Advanced SIMD instruction.
• Any access to the Advanced SIMD and floating-point registers D0-D31 and their views as S0-S31 and Q0-Q15.
• Any access to the FPSCR, FPSID, MVFR0, MVFR1, MVFR2, or FPEXC System registers.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES1.

If EL3 is implemented and is using AArch32, and the value of NSACR.cp10 is 0, in Non-secure state this field behaves as RAO/WI, regardless of its actual value.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Bits [9:0]**

Reserved, RES1.

**Accessing the HCPTR**

Accesses to this register use the following encodings:

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return HCPTR;
  end if;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HCPTR;
  end if;
else
  return HCPTR;
end if;

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && CPTR_EL3.TCPAC == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    HCPTR = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HCPTR = R[t];
  end if;
HCR, Hyp Configuration Register

The HCR characteristics are:

**Purpose**

Provides configuration controls for virtualization, including defining whether various Non-secure operations are trapped to Hyp mode.

**Configuration**

AArch32 System register HCR bits [31:0] are architecturally mapped to AArch64 System register HCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HCR is a 32-bit register.

**Field descriptions**

The HCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES | TRVM | HCD | RES | TGET | TVMTTLB | TMPUPCT | TSWT | TACT | IDCPT | TSC | TID3 | TID2 | TID1 | TID0 | TWE | TWI | DCBSU | FB | VA | VF | AMO | IMO | FMO | PTW | SWIO | VM |

**Bit [31]**

Reserved, RES0.

**TRVM, bit [30]**

Trap Reads of Virtual Memory controls. Traps Non-secure EL1 reads of the virtual memory control registers to EL2, when EL2 is enabled in the current Security state.

The registers for which read accesses are trapped are as follows:

SCTLB, TTBR0, TTBR1, TTBCR, TTBCR2, DACR, DFSR, JFSR, DFAR, IFAR, ADFSR, AIFSAR, PRRR, NMRR, MAIR0, MAIR1, AMAIR0, AMAIR1, CONTEXTIDR.

<table>
<thead>
<tr>
<th>TRVM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 read accesses to the specified Virtual Memory controls are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**HCD, bit [29]**

When EL3 is not implemented:

HVC instruction disable. Disables Non-secure EL1 and EL2 execution of HVC instructions, when EL2 is enabled in the current Security state.
HVC instruction execution is enabled at EL2 and EL1.

Note

HVC instructions are always UNDEFINED at EL0.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [28]

Reserved, RES0.

TGE, bit [27]

Trap General Exceptions, from Non-secure EL0.

TGE | Meaning
---|---
0b0 | This control has no effect on execution at EL0.
0b1 | When EL2 is not enabled in the current Security state, this control has no effect on execution at EL0.
When EL2 is enabled in the current Security state, then:
• All exceptions that would be routed to EL1 are routed to EL2.
• The SCTLR.M bit is treated as being 0 for all purposes other than returning the result of a direct read of SCTLR.
• The HCR.{FMO, IMO, AMO} bits are treated as being 1 for all purposes other than returning the result of a direct read of HCR.
• All virtual interrupts are disabled.
• Any IMPLEMENTATION DEFINED mechanisms for signaling virtual interrupts are disabled.
• An exception return to EL1 is treated as an illegal exception return.
• Monitor mode execution of an MSR or CPS instruction that changes PSTATE.M to a Non-secure EL1 mode is an illegal change to PSTATE.M. For more information see ‘Illegal changes to PSTATE.M’.

Also, when HCR.TGE is 1:

• If EL3 is using AArch32, an attempt to change from a Secure PL1 mode to a Non-secure EL1 mode by changing SCR.NS from 0 to 1 results in SCR.NS remaining as 0.
• The HDCR.{TDRA, TDOSA, TDA, TDE} bits are ignored and treated as being 1 other than for the purpose of a direct read of HDCR.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

TVM, bit [26]

Trap Virtual Memory controls. Traps Non-secure EL1 writes to the virtual memory control registers to EL2, when EL2 is enabled in the current Security state.

The registers for which write accesses are trapped are as follows:

SCTLR, TTBR0, TTBR1, TTBCR, TTBCR2, DACR, DFSR, IFSR, DFAR, IFAR, ADFSR, AIFSR, PRRR, NMRR, MAIR0, MAIR1, AMAIR0, AMAIR1, CONTEXTIDR.
On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TTLB, bit [25]**

Trap TLB maintenance instructions. Traps Non-secure EL1 execution of a TLBI instruction to EL2, when EL2 is enabled in the current Security state.

This applies to the following instructions:

- TLBIALL, TLBIIMVA, TLBIASID, TLBIMVAA, TLBIMVAI, TLBIMVAI, TLBIALL, TLBIMVA, TLBIASID, DTLBIALL, DTLBIMVA, DTLBIMVAA, DTLBIMVAI, DTLBIMVA.

<table>
<thead>
<tr>
<th>TTLB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to the specified TLB maintenance instructions are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TPU, bit [24]**

Trap cache maintenance instructions that operate to the Point of Unification. Traps Non-secure EL1 execution of those cache maintenance instructions to EL2, when EL2 is enabled in the current Security state.

This applies to the following instructions:

- ICIMVAU, ICIALLU, ICIALLUS, DCCMVAA.

**Note**

An Undefined Instruction exception generated at EL0 is higher priority than this trap to EL2, and these instructions are always UNDEFINED at EL0.

<table>
<thead>
<tr>
<th>TPU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 execution of the specified cache maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of data cache, it is IMPLEMENTATION DEFINED whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is IMPLEMENTATION DEFINED whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TPC, bit [23]**

Trap data or unified cache maintenance instructions that operate to the Point of Coherency. Traps Non-secure EL1 execution of those cache maintenance instructions to EL2, when EL2 is enabled in the current Security state.

This applies to the following instructions:

- DCIMVAC, DCCIMVAC, DCCMVAC.

**Note**

An Undefined Instruction exception generated at EL0 is higher priority than this trap to EL2, and these instructions are always UNDEFINED at EL0.
### TPC

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0                      This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1                      Non-secure EL1 execution of the specified cache maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Coherency is before any level of data cache, it is **IMPLEMENTATION DEFINED** whether the execution of any data or unified cache clean, invalidate, or clean and invalidate instruction that operates by VA to the point of coherency can be trapped when the value of this control is 1.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TSW, bit [22]

Trap data or unified cache maintenance instructions that operate by Set/Way. Traps non-secure EL1 execution of those cache maintenance instructions by set/way to EL2, when EL2 is enabled in the current Security state.

This applies to the following instructions:

- DCISW, DCCSW, DCCISW.

**Note**

An Undefined Instruction exception generated at EL0 is higher priority than this trap to EL2, and these instructions are always **UNDEFINED** at EL0.

### TSW

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0                      This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1                      Non-secure EL1 execution of the specified cache maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TAC, bit [21]

Trap Auxiliary Control Registers. Traps non-secure EL1 accesses to the Auxiliary Control Registers to EL2, when EL2 is enabled in the current Security state, from both Execution states.

This applies to the following register accesses:

- ACTLR and, if implemented, ACTLR2.

### TAC

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0                      This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1                      Non-secure EL1 accesses to the specified registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TIDCP, bit [20]

Trap **IMPLEMENTATION DEFINED** functionality. Traps non-secure EL1 accesses to the encodings for **IMPLEMENTATION DEFINED** System Registers to EL2, when EL2 is enabled in the current Security state.

MCR and MRC instructions accessing the following encodings:

- All coproc==p15, CRn==c9, Opcode1 = {0-7}, CRm == {c0-c2, c5-c8}, opcode2 == {0-7}.
- All coproc==p15, CRn==c10, Opcode1 == {0-7}, CRm == {c0, c1, c4, c8}, opcode2 == {0-7}.
- All coproc==p15, CRn==c11, Opcode1=={0-7}, CRm == {c0-c8, c15}, opcode2 == {0-7}.

When HCR.TIDCP is set to 1, it is **IMPLEMENTATION DEFINED** whether any of this functionality accessed from Non-secure EL0 is trapped to EL2. Otherwise, it is **UNDEFINED** and the PE takes an Undefined Instruction exception to Non-secure Undefined mode.
TIDCP

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TSC, bit [19]**

Trap SMC instructions. Traps Non-secure EL1 execution of SMC instructions to Hyp mode.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

The Armv8-A architecture permits, but does not require, this trap to apply to conditional SMC instructions that fail their condition code check, in the same way as with traps on other conditional instructions.

**Note**
- This trap is only implemented if the implementation includes EL3.
- SMC instructions are always UNDEFINED at PL0.
- This bit traps execution of the SMC instruction. It is not a routing control for the SMC exception. Hyp Trap exceptions and SMC exceptions have different preferred return addresses.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TID3, bit [18]**

Trap ID group 3. Traps Non-secure EL1 reads of the following registers to EL2, when EL2 is enabled in the current Security state as follows:

- VMRS access to MVFR0, MVFR1, and MVFR2, reported using EC syndrome value 0x08, unless access is also trapped by HCPTR which takes priority.
- MRC access to the following registers are reported using EC syndrome value 0x03:
  - If FEAT_FGT is implemented:
    - ID_MMFR4 and ID_MMFR5 are trapped to EL2.
    - ID_ISAR6 is trapped to EL2.
    - ID_DFR1 is trapped to EL2.
    - This field traps all MRC accesses to registers in the following range that are not already mentioned in this field description: coproc == p15, opc1 == 0, CRn == c0, CRm == {c2-c7}, opc2 == {0-7}.
  - If FEAT_FGT is not implemented:
    - ID_MMFR4 and ID_MMFR5 are trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_MMFR4 or ID_MMFR5 are trapped.
    - ID_ISAR6 is trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_ISAR6 are trapped to EL2.
    - ID_DFR1 is trapped to EL2, unless implemented as RAZ, when it is IMPLEMENTATION DEFINED whether accesses to ID_DFR1 are trapped to EL2.
    - Otherwise, it is IMPLEMENTATION DEFINED whether this bit traps MRC accesses to registers not already mentioned, with coproc == p15, opc1 == 0, CRn == c0, CRm == {c2-c7}, opc2 == {0-7}. 

Page 2454
### TID3

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  The specified Non-secure EL1 read accesses to ID group 3 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TID2, bit [17]

Trap ID group 2. Traps the following register accesses to EL2, when EL2 is enabled in the current Security state:

- Non-secure EL1 and EL0 reads of the **CTR**, **CCSIDR**, **CCSIDR2**, **CLIDR**, and **CSSELr**.
- Non-secure EL1 and EL0 writes to the **CSSELr**.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  The specified Non-secure EL1 and EL0 accesses to ID group 2 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TID1, bit [16]

Trap ID group 1. Traps Non-secure EL1 reads of the following registers to EL2, when EL2 is enabled in the current Security state:

**TCMTR**, **TLBTR**, **REVIDR**, **AIDR**.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  The specified Non-secure EL1 read accesses to ID group 1 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TID0, bit [15]

Trap ID group 0. Traps the following register accesses to EL2, when EL2 is enabled in the current Security state:

- Non-secure EL1 reads of the **JIDR** and **FPSID**.
- If the **JIDR** is RAZ from Non-secure EL0, Non-secure EL0 reads of the **JIDR**.

**Note**

- It is IMPLEMENTATION DEFINED whether the **JIDR** is RAZ or **UNDEFINED** at EL0. If it is **UNDEFINED** at EL0 then the Undefined Instruction exception takes precedence over this trap.
- The **FPSID** is not accessible at EL0.
- Writes to the **FPSID** are ignored, and not trapped by this control.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  The specified Non-secure EL1 read accesses to ID group 0 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### TWE, bit [14]

Traps Non-secure EL0 and EL1 execution of WFE instructions to EL2, when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  Any attempt to execute a WFE instruction at Non-secure EL0 or EL1 is trapped to EL2, if the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by <strong>SCTLr</strong> nTWE.</td>
</tr>
</tbody>
</table>

---

Page 2455
The attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE can complete at any time, even without a Wakeup event, the traps on WFE are not guaranteed to be taken, even if the WFE is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TWI, bit [13]**

Traps Non-secure EL0 and EL1 execution of WFI instructions to EL2, when EL2 is enabled in the current Security state.

<table>
<thead>
<tr>
<th>TWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFI instruction at Non-secure EL0 or EL1 is trapped to EL2, if the instruction would otherwise have caused the PE to enter a low-power state and it is not trapped by SCTLR.nTWI.</td>
</tr>
</tbody>
</table>

The attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFI can complete at any time, even without a Wakeup event, the traps on WFI are not guaranteed to be taken, even if the WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**DC, bit [12]**

Default Cacheability.

<table>
<thead>
<tr>
<th>DC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the Non-secure EL1&amp;0 translation regime.</td>
</tr>
</tbody>
</table>
| 0b1 | In Non-secure state:  
  • The SCTLR M field behaves as 0 for all purposes other than a direct read of the value of the field.  
  • The HCR.VM field behaves as 1 for all purposes other than a direct read of the value of the field.  
  • The memory type produced by the first stage of the EL1&0 translation regime is Normal Non-Shareable, Inner Write-Back Read-Allocate Write-Allocate, Outer Write-Back Read-Allocate Write-Allocate. |

This field has no effect on the EL2 and EL3 translation regimes.

This field is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**BSU, bits [11:10]**

Barrier Shareability upgrade. This field determines the minimum shareability domain that is applied to any barrier instruction executed from Non-secure EL1 or Non-secure EL0:
BSU | Meaning
--- | ---
0b00 | No effect.
0b01 | Inner Shareable.
0b10 | Outer Shareable.
0b11 | Full system.

This value is combined with the specified level of the barrier held in its instruction, using the same principles as combining the shareability attributes from two stages of address translation.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**FB, bit [9]**

Force broadcast. Causes the following instructions to be broadcast within the Inner Shareable domain when executed from Non-secure EL1:

- **BPIALL, TLBIALL, TLBIMVA, TLBISID, DTLBIALL, DTLIMVA, DTLBISID, ITLBIALL, ITLIMVA, ITLBISID, TLBIMVAA, ICIALLU, TLBIMAL, TLBIMVAAL.**

| FB | Meaning |
--- | --- |
0b0 | This field has no effect on the operation of the specified instructions. |
0b1 | When one of the specified instruction is executed at Non-secure EL1, the instruction is broadcast within the Inner Shareable shareability domain. |

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**VA, bit [8]**

Virtual SError interrupt exception.

| VA | Meaning |
--- | --- |
0b0 | This mechanism is not making a virtual SError interrupt pending. |
0b1 | A virtual SError interrupt is pending because of this mechanism. |

The virtual SError interrupt is enabled only when the value of HCR.{TGE, AMO} is {0, 1}.

The Guest OS cannot distinguish the virtual exception from the corresponding physical exception.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**VI, bit [7]**

Virtual IRQ exception.

| VI | Meaning |
--- | --- |
0b0 | This mechanism is not making a virtual IRQ pending. |
0b1 | A virtual IRQ is pending because of this mechanism. |

The virtual IRQ is enabled only when the value of HCR.{TGE, IMO} is {0, 1}.

The Guest OS cannot distinguish the virtual exception from the corresponding physical exception.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**VF, bit [6]**

Virtual FIQ exception.

| VF | Meaning |
--- | --- |
0b0 | This mechanism is not making a virtual FIQ pending. |
0b1 | A virtual FIQ is pending because of this mechanism. |

The virtual FIQ is enabled only when the value of HCR.{TGE, FMO} is {0, 1}.
The Guest OS cannot distinguish the virtual exception from the corresponding physical exception.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**AMO, bit [5]**

SError interrupt Mask Override. When this bit is set to 1, it overrides the effect of PSTATE.A, and enables virtual exception signaling by the VA bit.

If the value of HCR.TGE is 0, then virtual SError interrupts are enabled in Non-secure state.

If the value of HCR.TGE is 1, then in Non-secure state the HCR.AMO bit behaves as 1 for all purposes other than a direct read of the value of the bit.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**IMO, bit [4]**

IRQ Mask Override. When this bit is set to 1, it overrides the effect of PSTATE.I, and enables virtual exception signaling by the VI bit.

If the value of HCR.TGE is 0, then Virtual IRQ interrupts are enabled in the Non-secure state.

If the value of HCR.TGE is 1, then in Non-secure state the HCR.IMO bit behaves as 1 for all purposes other than a direct read of the value of the bit.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**FMO, bit [3]**

FIQ Mask Override. When this bit is set to 1, it overrides the effect of PSTATE.F, and enables virtual exception signaling by the VF bit.

If the value of HCR.TGE is 0, then Virtual FIQ interrupts are enabled in the Non-secure state.

If the value of HCR.TGE is 1, then in Non-secure state the HCR.FMO bit behaves as 1 for all purposes other than a direct read of the value of the bit.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**PTW, bit [2]**

Protected Table Walk. In the Non-secure PL1&0 translation regime, a translation table access made as part of a stage 1 translation table walk is subject to a stage 2 translation. The combining of the memory type attributes from the two stages of translation means the access might be made to a type of Device memory. If this occurs then the value of this bit determines the behavior:

<table>
<thead>
<tr>
<th>PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table walk occurs as if it is to Normal Non-cachable memory. This means it can be made speculatively.</td>
</tr>
<tr>
<td>0b1</td>
<td>The memory access generates a stage 2 Permission fault.</td>
</tr>
</tbody>
</table>

This field is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**SWIO, bit [1]**

Set/Way Invalidation Override. Causes Non-secure EL1 execution of the data cache invalidate by set/way instructions to perform a data cache clean and invalidate by set/way.

<table>
<thead>
<tr>
<th>SWIO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on the operation of data cache invalidate by set/way instructions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Data cache invalidate by set/way instructions perform a data cache clean and invalidate by set/way.</td>
</tr>
</tbody>
</table>
When this bit is set to 1, \texttt{DCISW} performs the same invalidation as a \texttt{DCCISW} instruction. As a result of changes to the behavior of \texttt{DCISW}, this bit is redundant in Armv8. This bit can be implemented as \texttt{RES1}.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

\textbf{VM, bit [0]}

Virtualization enable. Enables stage 2 address translation for the Non-secure EL1&0 translation regime.

<table>
<thead>
<tr>
<th>VM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1&amp;0 stage 2 address translation disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1&amp;0 stage 2 address translation enabled.</td>
</tr>
</tbody>
</table>

If the HCR.DC bit is set to 1, then the behavior of the PE when executing in a Non-secure mode other than Hyp mode is consistent with HCR.VM being 1, regardless of the actual value of HCR.VM, other than the value returned by an explicit read of HCR.VM.

When the value of this bit is 1, data cache invalidate instructions executed at Non-secure EL1 perform a data cache clean and invalidate. For the invalidate by set/way instruction this behavior applies regardless of the value of the HCR.SWIO bit.

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

\textbf{Accessing the HCR}

Accesses to this register use the following encodings:

\begin{verbatim}
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
\end{verbatim}

\begin{verbatim}
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
\end{verbatim}

\begin{verbatim}
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HCR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HCR;
\end{verbatim}

\begin{verbatim}
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
\end{verbatim}

\begin{verbatim}
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
\end{verbatim}
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    HCR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HCR = R[t];
HCR2, Hyp Configuration Register 2

The HCR2 characteristics are:

**Purpose**

Provides additional configuration controls for virtualization.

**Configuration**

AArch32 System register HCR2 bits [31:0] are architecturally mapped to AArch64 System register HCR_EL2[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HCR2 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HCR2 is a 32-bit register.

**Field descriptions**

The HCR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TTLBIS | RES0 | TOCU | RES0 | TICAB | ID4 | RES0 | MIOCNC | TEA | TERR | RES0 | IDCD |

**Bits [31:23]**

Reserved, RES0.

**TTLBIS, bit [22]**

**When FEAT_EVT is implemented:**

Trap TLB maintenance instructions that operate on the Inner Shareable domain. Traps execution of the following TLB maintenance instructions at EL1 to EL2:

**TLBIALLIS, TLBIMVAIS, TLBIASIDIS, TLBIMVAAIS, TLBIMVALIS, TLBIMVAALIS**

<table>
<thead>
<tr>
<th>TTLBIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 execution of the specified TLB maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

When FEAT_VHE and the value of HCR_EL2.{E2H, TGE} is {1, 1}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

**Otherwise:**

Reserved, RES0.

**Bit [21]**

Reserved, RES0.
**TOCU, bit [20]**

*When FEAT_EVT is implemented:*

Trap cache maintenance instructions that operate to the Point of Unification. Traps execution of those cache maintenance instructions at EL1 or EL0 using AArch64, and at EL1 using AArch32, to EL2.

This applies to the following instructions:

- When Non-secure EL0 is using AArch64, **IC IVAU**, **DC CVAU**. However, if the value of **SCTLR_EL1.UCI** is 0 these instructions are *UNDEFINED* at EL0 and any resulting exception is higher priority than this trap to EL2.
- When EL1 is using AArch64, **IC IVAU**, **IC IALLU**, **DC CVAU**.
- When Non-secure EL1 is using AArch32, **ICIMVAU**, **ICIALLU**, **DCCMVAU**.

**Note**

An exception generated because an instruction is *UNDEFINED* at EL0 is higher priority than this trap to EL2. In addition:

- **IC IALLUIS** and **IC IALLU** are always *UNDEFINED* at EL0 using AArch64.
- **ICIMVAU**, **ICIALLU**, **ICIALLUIS**, and **DCCMVAU** are always *UNDEFINED* at EL0 using AArch32.

<table>
<thead>
<tr>
<th>TOCU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure execution of the specified cache maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of data cache, it is *IMPLEMENTATION DEFINED* whether the execution of any data or unified cache clean by VA to the Point of Unification instruction can be trapped when the value of this control is 1.

If the Point of Unification is before any level of instruction cache, it is *IMPLEMENTATION DEFINED* whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.

When **FEAT_VHE** is implemented, and the value of **HCR_EL2.E2H, TGE** is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

**Otherwise:**

Reserved, **RES0**.

**Bit [19]**

Reserved, **RES0**.

**TICAB, bit [18]**

*When FEAT_EVT is implemented:*

Trap **ICIALLUIS** cache maintenance instructions. Traps execution of those cache maintenance instructions at EL1 to EL2.

This applies to the following instruction:

**ICIALLUIS**.

<table>
<thead>
<tr>
<th>TICAB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 execution of the specified cache maintenance instructions is trapped to EL2.</td>
</tr>
</tbody>
</table>

If the Point of Unification is before any level of instruction cache, it is *IMPLEMENTATION DEFINED* whether the execution of any instruction cache invalidate to the Point of Unification instruction can be trapped when the value of this control is 1.
When FEAT_VHE and the value of \texttt{HCR_EL2}.\{E2H, TGE\} is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

Otherwise:

Reserved, RES0.

TID4, bit [17]

When FEAT_EVT is implemented:

Trap ID group 4. Traps the following register accesses to EL2:

- EL1 reads of \texttt{CCSIDR}, \texttt{CCSIDR2}, \texttt{CLIDR}, and \texttt{CSSELR}.
- EL1 writes to \texttt{CSSELR}.

<table>
<thead>
<tr>
<th>TID4</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>The specified Non-secure EL1 and EL0 accesses to ID group 4 registers are trapped to EL2.</td>
</tr>
</tbody>
</table>

When FEAT_VHE is implemented and the value of \texttt{HCR_EL2}.\{E2H, TGE\} is \{1, 1\}, this field behaves as 0 for all purposes other than a direct read of the value of this bit.

Otherwise:

Reserved, RES0.

Bits [16:7]

Reserved, RES0.

MIOCNCE, bit [6]

Mismatched Inner/Outer Cacheable Non-Coherency Enable, for the Non-secure PL1&0 translation regime.

<table>
<thead>
<tr>
<th>MIOCNCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For the Non-secure PL1&amp;0 translation regime, for permitted accesses to a memory location that use a common definition of the Shareability and Cacheability of the location, there must be no loss of coherency if the Inner Cacheability attribute for those accesses differs from the Outer Cacheability attribute.</td>
</tr>
<tr>
<td>0b1</td>
<td>For the Non-secure PL1&amp;0 translation regime, for permitted accesses to a memory location that use a common definition of the Shareability and Cacheability of the location, there might be a loss of coherency if the Inner Cacheability attribute for those accesses differs from the Outer Cacheability attribute.</td>
</tr>
</tbody>
</table>

For more information, see 'Mismatched memory attributes'.

This field can be implemented as RAZ/WI.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally \texttt{UNKNOWN} value.

TEA, bit [5]

When FEAT_RAS is implemented:

Route synchronous External abort exceptions from EL0 and EL1 to EL2.
### TEA

<table>
<thead>
<tr>
<th>TEA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not route synchronous External abort exceptions from Non-secure EL0 and EL1 to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Route synchronous External abort exceptions from Non-secure EL0 and EL1 to EL2, if not routed to EL3.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### TERR, bit [4]

**When FEAT_RAS is implemented:**

Trap Error record accesses from EL1 to EL2. Trap accesses to the following registers from EL1 to EL2:

- ERRIDR
- ERRSELR
- ERXADDR
- ERXADDR2
- ERXCTLR
- ERXCTLR2
- ERXFR
- ERXFR2
- ERXMISC0
- ERXMISC1
- ERXMISC2
- ERXMISC3
- ERXSTATUS

When FEAT_RASv1p1 is implemented, ERXMISC4, ERXMISC5, ERXMISC6, and ERXMISC7.

<table>
<thead>
<tr>
<th>TERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to the specified registers from EL1 generate a Trap exception to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Otherwise:**

Reserved, RES0.

### Bits [3:2]

Reserved, RES0.

### ID, bit [1]

Stage 2 Instruction access cacheability disable. For the Non-secure PL1&0 translation regime, when `HCR.VM==1`, this control forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable.

<table>
<thead>
<tr>
<th>ID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on stage 2 of the Non-secure PL1&amp;0 translation regime.</td>
</tr>
<tr>
<td>0b1</td>
<td>For the Non-secure PL1&amp;0 translation regime, forces all stage 2 translations for instruction accesses to Normal memory to be Non-cacheable.</td>
</tr>
</tbody>
</table>

This bit has no effect on the EL2 translation regime.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

### CD, bit [0]

Stage 2 Data access cacheability disable. When `HCR.VM==1`, this forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable for the Non-secure PL1&0 translation regime.
This control has no effect on stage 2 of the Non-secure PL1&0 translation regime for data accesses and translation table walks.

For the Non-secure PL1&0 translation regime, forces all stage 2 translations for data accesses and translation table walks to Normal memory to be Non-cacheable.

This bit has no effect on the EL2 translation regime.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Accessing the HCR2**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{<\text{opc}1>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{<\text{opc}2>\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
\[
\text{UNDEFINED};
\]
elsif PSTATE.EL == EL1 then
\[
\text{if EL2Enabled()} \&\& \text{ELUsingAArch32}(EL2) \&\& \text{HSTR_EL2}.T1 == '1' then
\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
\text{elsif EL2Enabled()} \&\& \text{ELUsingAArch32}(EL2) \&\& \text{HSTR.T1} == '1' then
\text{AArch32.TakeHypTrapException(0x03)};
\text{else}
\text{UNDEFINED};
\]
elsif PSTATE.EL == EL2 then
\text{return HCR2;}
elsif PSTATE.EL == EL3 then
\text{if SCR.NS == '0' then}
\text{UNDEFINED;}
\text{else}
\text{return HCR2;}
\text{MCR}\{<c>\}{<q>} <\text{coproc}>, \{<\text{opc}1>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{<\text{opc}2>\}\}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
\[
\text{UNDEFINED};
\]
elsif PSTATE.EL == EL1 then
\[
\text{if EL2Enabled()} \&\& \text{ELUsingAArch32}(EL2) \&\& \text{HSTR_EL2}.T1 == '1' then
\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
\text{elsif EL2Enabled()} \&\& \text{ELUsingAArch32}(EL2) \&\& \text{HSTR.T1} == '1' then
\text{AArch32.TakeHypTrapException(0x03)};
\text{else}
\text{UNDEFINED};
\]
elsif PSTATE.EL == EL2 then
\text{HCR2 = R[t];}
elsif PSTATE.EL == EL3 then
\text{if SCR.NS == '0' then}
\text{UNDEFINED;}
\text{else}
\text{HCR2 = R[t];}
HDCR, Hyp Debug Control Register

The HDCR characteristics are:

**Purpose**

Controls the trapping to Hyp mode of Non-secure accesses, at EL1 or lower, to functions provided by the debug and trace architectures and the Performance Monitors Extension.

**Configuration**

AArch32 System register HDCR bits [31:0] are architecturally mapped to AArch64 System register MDCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HDCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3, and other than for a direct read of the register, the PE behaves as if HDCR.HPMN == PMCR.N.

**Attributes**

HDCR is a 32-bit register.

**Field descriptions**

The HDCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>29</td>
<td>HPMFZO</td>
<td>Hyp Performance Monitors Freeze-on-overflow. Stop event counters on overflow.</td>
</tr>
<tr>
<td>28</td>
<td>MTPME</td>
<td>Event counters do not count when PMOVSR[(PMCR.N-1):HDCR.HPMN] is nonzero.</td>
</tr>
<tr>
<td>27</td>
<td>TDCC</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>HLP</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>TTRF</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>TTRF</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>RES0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:30]**

Reserved, RES0.

**HPMFZO, bit [29]**

When FEAT_PMu3p7 is implemented:

Hyp Performance Monitors Freeze-on-overflow. Stop event counters on overflow.

<table>
<thead>
<tr>
<th>HPMFZO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on overflow.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters do not count when PMOVSR[(PMCR.N-1):HDCR.HPMN] is nonzero.</td>
</tr>
</tbody>
</table>

If HDCR.HPMN is less than PMCR.N, this bit affects the operation of event counters in the range [HDCR.HPMN .. (PMCR.N-1)].

If HDCR.HPMN is equal to PMCR.N, this bit has no effect.

This bit does not affect the operation of event counters in the range [0 .. (HDCR.HPMN-1)] and PMCCNTR.

The operation of this bit ignores the values of PMOVSR[(HDCR.HPMN-1):0].

The operation of this bit applies even when EL2 is disabled in the current Security state.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**MTPME, bit [28]**

When FEAT_MTPMU is implemented and EL3 is not implemented:

Multi-threaded PMU Enable. Enables use of the PMEVTYPERx<MT> bits.

<table>
<thead>
<tr>
<th>MTPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FEAT_MTPMU is disabled. The Effective value of PMEVTYPERx&lt;MT&gt; is zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMEVTYPERx&lt;MT&gt; bits not affected by this bit.</td>
</tr>
</tbody>
</table>

If FEAT_MTPMU is disabled for any other PE in the system that has the same level 1 Affinity as the PE, it is IMPLEMENTATION DEFINED whether the PE behaves as if this bit is 0b0.

On a Cold reset, in a system where the PE resets into EL2 or EL3, this field resets to 1.

Otherwise:

Reserved, RES0.

**TDCC, bit [27]**

When FEAT_FGT is implemented:

Trap DCC. Traps use of the Debug Comms Channel at EL1 and EL0 to EL2.

<table>
<thead>
<tr>
<th>TDCC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any register accesses to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL2 is implemented and enabled in the current Security state, accesses to the DCC registers at EL1 and EL0 generate a Hyp Trap exception, unless the access also generates a higher priority exception. Traps on the DCC data transfer registers are ignored when the PE is in Debug state.</td>
</tr>
</tbody>
</table>

The DCC registers trapped by this control are:

- DBGDTRRXext, DBGDTRTXext, DBGDSCRint, DBGDCCINT, and, when the PE is in Non-debug state, DBGDTRRXint and DBGDTRTXint.

The traps are reported with EC syndrome value:

- 0x05 for trapped MRC and MCR accesses with coproc == 0b1110.
- 0x06 for trapped LDC to DBGDTRTXint and STC from DBGDTRRXint.

When the PE is in Debug state, HDCR.TDCC does not trap any accesses to:

- DBGDTRRXint and DBGDTRTXint.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

**HLP, bit [26]**

When FEAT_PMUv3p5 is implemented:

Hypervisor Long event counter enable. Determines when unsigned overflow is recorded by a counter overflow bit.
### HLP

<table>
<thead>
<tr>
<th>HLP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;\text{n}&gt;[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;\text{n}&gt;[63:0].</td>
</tr>
</tbody>
</table>

If the highest implemented Exception level is using AArch32, it is IMPLEMENTATION DEFINED whether this bit is read/write or RAZ/WI.

If HDCR.HPMN is less than PMCR.N, this bit affects the operation of event counters in the range \([\text{HDCR.HPMN..(PMCR.N-1)}]\). Otherwise this bit has no effect on the operation of the event counters.

**Note**

The effect of HDCR.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state.

For more information see the description of the HDCR.HPMN field.

**Note**

PMEVCNTR<\text{n}>[63:32] cannot be accessed directly in AArch32 state.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bits [25:24]**

Reserved, RES0.

**HCCD, bit [23]**

**When FEAT_PMUv3p5 is implemented:**

Hypervisor Cycle Counter Disable. Prohibits PMCCNTR from counting at EL2.

<table>
<thead>
<tr>
<th>HCCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counting by PMCCNTR is prohibited at EL2.</td>
</tr>
</tbody>
</table>

This bit does not affect the CPU_CYCLES event or any other event that counts cycles.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**Bits [22:20]**

Reserved, RES0.
TTRF, bit [19]

When FEAT_TRF is implemented:

Traps use of the Trace Filter Control registers at EL1 to EL2.

<table>
<thead>
<tr>
<th>TTRF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to TRFCR at EL1 are not affected by this control bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to TRFCR at EL1 generate a Hyp Trap exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

Bit [18]

Reserved, RES0.

HPMD, bit [17]

When FEAT_PMUv3p1 is implemented:

Guest Performance Monitors Disable. This control prohibits event counting at EL2.

<table>
<thead>
<tr>
<th>HPMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting allowed in Hyp mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting prohibited in Hyp mode.</td>
</tr>
</tbody>
</table>

If FEAT_Debugv8p2 is not implemented, event counting is prohibited unless enabled by the IMPLEMENTATION DEFINED authentication interface ExternalSecureNoninvasiveDebugEnabled().

This control applies only to:

- The event counters in the range [0..(HDCR.HPMN-1)].
- If PMCR.DP is set to 1, PMCCNTR.

The other event counters are unaffected. When PMCR.DP is set to 0, PMCCNTR is unaffected.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

Bits [16:12]

Reserved, RES0.

TDRA, bit [11]

Trap Debug ROM Address register access. Traps Non-secure EL0 and EL1 System register accesses to the Debug ROM registers to Hyp mode.

<table>
<thead>
<tr>
<th>TDRA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL0 and EL1 System register accesses to the DebugROM registers are trapped to Hyp mode, unless it is trapped by DBGDSCRx.UDCCdis.</td>
</tr>
</tbody>
</table>

If HCR.TGE or HDCR.TDE is 1, behavior is as if this bit is 1 other than for the purpose of a direct read.
On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

TDOSA, bit [10]

When FEAT_DoubleLock is implemented:

Trap debug OS-related register access. Traps Non-secure EL1 System register accesses to the powerdown debug registers to Hyp mode.

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 System register accesses to the powerdown debug registers are trapped to Hyp mode.</td>
</tr>
</tbody>
</table>

The registers for which accesses are trapped are as follows:

- DBGOSLSR, DBGOSLAR, DBGOSD, and DBGPRCR.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

Note

These registers are not accessible at EL0.

If HCR.TGE or HDCR.TDE is 1, behavior is as if this bit is 1 other than for the purpose of a direct read.

Otherwise:

Trap debug OS-related register access. Traps Non-secure EL1 System register accesses to the powerdown debug registers to Hyp mode.

<table>
<thead>
<tr>
<th>TDOSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 System register accesses to the powerdown debug registers are trapped to Hyp mode.</td>
</tr>
</tbody>
</table>

The registers for which accesses are trapped are as follows:

- DBGOSLSR, DBGOSLAR, and DBGPRCR.
- Any IMPLEMENTATION DEFINED register with similar functionality that the implementation specifies as trapped by this bit.

It is IMPLEMENTATION DEFINED whether accesses to DBGOSDLR are trapped.

Note

These registers are not accessible at EL0.

If HCR.TGE or HDCR.TDE is 1, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

TDA, bit [9]

Trap debug access. Traps Non-secure EL0 and EL1 System register accesses to those debug System registers in the (coproc==0b1110) encoding space that are not trapped by either of the following:

- HDCR.TDRA.
- HDCR.TDOSA.
TDA

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1  Non-secure EL0 or EL1 System register accesses to the debug</td>
</tr>
<tr>
<td>registers, other than the registers trapped by HDCR.TDRA and</td>
</tr>
<tr>
<td>HDCR.TDOSA, are trapped to Hyp mode, unless it is trapped by</td>
</tr>
<tr>
<td>DBGDSCRegext.UDCCdis.</td>
</tr>
</tbody>
</table>

Traps of AArch32 accesses to DBGDTRRXint and DBGDTRTXint are ignored in Debug state.

If HCR.TGE or HDCR.TDE is 1, behavior is as if this bit is 1 other than for the purpose of a direct read.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**TDE, bit [8]**

Trap Debug exceptions. Controls routing of Debug exceptions, and defines the debug target Exception level, EL_D.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  The debug target Exception level is EL1.</td>
</tr>
<tr>
<td>0b1  If EL2 is enabled for the current Effective value of SCR.NS, the</td>
</tr>
<tr>
<td>debug target Exception level is EL2, otherwise the debug target</td>
</tr>
<tr>
<td>Exception level is EL1.</td>
</tr>
<tr>
<td>The HDCR. (TDRA, TDOSA, TDA) fields are treated as being 1 for</td>
</tr>
<tr>
<td>all purposes other than returning the result of a direct read of</td>
</tr>
<tr>
<td>the register.</td>
</tr>
</tbody>
</table>

For more information, see 'Routing debug exceptions'.

When HCR.TGE == 1, the PE behaves as if the value of this field is 1 for all purposes other than returning the value of a direct read of the register.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**HPME, bit [7]**

*When FEAT_PMUv3 is implemented:*

[HDCR.HPMN.(N-1)] event counters enable.

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0  Event counters in the range [HDCR.HPMN..(PMCR.N-1)] are</td>
</tr>
<tr>
<td>disabled.</td>
</tr>
<tr>
<td>0b1  Event counters in the range [HDCR.HPMN..(PMCR.N-1)] are</td>
</tr>
<tr>
<td>enabled by PMCNTENSET.</td>
</tr>
</tbody>
</table>

If HDCR.HPMN is less than PMCR.N, the event counters in the range [HDCR.HPMN..(PMCR.N-1)], are enabled and disabled by this bit. Otherwise this bit has no effect on the operation of the event counters.

**Note**

The effect of HDCR.HPMN on the operation of this bit applies regardless of whether EL2 is enabled in the current Security state.

For more information see the description of the HPMN field.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally unknown value.

**Otherwise:**

Reserved, RES0.
TPM, bit [6]

When FEAT_PMUv3 is implemented:

Trap Performance Monitors accesses. Traps Non-secure EL0 and EL1 accesses to all Performance Monitors registers to Hyp mode.

<table>
<thead>
<tr>
<th>TPM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL0 and EL1 accesses to all Performance Monitors registers are trapped to Hyp mode.</td>
</tr>
</tbody>
</table>

Note

EL2 does not provide traps on Performance Monitor register accesses through the optional memory-mapped external debug interface.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

TPMCR, bit [5]

When FEAT_PMUv3 is implemented:

Trap PMCR accesses. Traps Non-secure EL0 and EL1 accesses to the PMCR to Hyp mode.

<table>
<thead>
<tr>
<th>TPM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL0 and EL1 accesses to the PMCR are trapped to Hyp mode, unless it is trapped by PMUSERENR.EN.</td>
</tr>
</tbody>
</table>

Note

EL2 does not provide traps on Performance Monitor register accesses through the optional memory-mapped external debug interface.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

HPMN, bits [4:0]

When FEAT_PMUv3 is implemented:

Defines the number of event counters that are accessible from Non-secure EL1 modes, and from Non-secure EL0 modes if unprivileged access is enabled.

If HPMN is less than PMCR.N, HPMN divides the event counters into two ranges, [0..(HPMN-1)] and [HPMN..(PMCR.N-1)].

For an event counter in the range [0..(HPMN-1)]:

- The counter is accessible from EL1 and EL2, and from EL0 if unprivileged access to the counters is enabled.
- If FEAT_PMUv3p5 is implemented, PMCR.LP determines whether the counter overflows at PMEVCNTR<n>[31:0] or PMEVCNTR<n>[63:0].
- PMCR.E enables the operation of counters in this range.

Note
If HPMN is equal to PMCR.N, this applies to all event counters.

If HPMN is less than PMCR.N, for an event counter in the range [HPMN..(PMCR.N-1)]:

- The counter is accessible only from EL2 and from Secure state.
- If FEAT_PMUv3p5 is implemented, HDCR.HLP determines whether the counter overflows at PMEVCNTR<n>[31:0] or PMEVCNTR<n>[63:0].
- HDCR.HPME enables the operation of counters in this range.

If this field is set to 0, or to a value larger than PMCR.N, then the following constrained unpredictable behaviors apply:

- The value returned by a direct read of HDCR.HPMN is unknown.
- Either:
  - An unknown number of counters are reserved for EL2 use. That is, the PE behaves as if HDCR.HPMN is set to an unknown non-zero value less than or equal to PMCR.N.
  - All counters are reserved for EL2 use, meaning no counters are accessible from Non-secure EL1 and Non-secure EL0.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in PMCR.N.

Otherwise:

Reserved, RES0.

## Accessing the HDCR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\} \{, \{#\}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b001</td>
<td>0b001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return HDCR;
  end
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HDCR;
  end
MCR{<c>}{<q>}{<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TDA == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    HDCR = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HDCR = R[t];
  end if;
The HDFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Data Abort exception that is taken to Hyp mode.

**Configuration**

AArch32 System register HDFAR bits [31:0] are architecturally mapped to AArch64 System register `FAR_EL2[31:0]`.

AArch32 System register HDFAR bits [31:0] are architecturally mapped to AArch32 System register `DFAR[31:0] (S)` when EL2 is implemented, EL3 is implemented and the highest implemented Exception level is using AArch32 state.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HDFAR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HDFAR is a 32-bit register.

**Field descriptions**

The HDFAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VA of faulting address of synchronous Data Abort exception taken to Hyp mode</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
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<tr>
<td>28</td>
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<td>27</td>
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<tr>
<td>3</td>
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<tr>
<td>2</td>
<td></td>
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<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:0]**

VA of faulting address of synchronous Data Abort exception taken to Hyp mode.

On a Prefetch Abort exception, this register is UNKNOWN.

Any execution in a Non-secure EL1 or Non-secure EL0 mode makes this register UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HDFAR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} \text{ coproc}, \{#}\text{opc1}, <Rt>, <CRn>, <CRm}\{(,#)\text{opc2}}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        return HDFAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HDFAR;

MCR{{c}}{q} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        HDFAR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HDFAR = R[t];
HIFAR, Hyp Instruction Fault Address Register

The HIFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Prefetch Abort exception that is taken to Hyp mode.

**Configuration**

AArch32 System register HIFAR bits [31:0] are architecturally mapped to AArch64 System register `FAR_EL2[63:32]`.

AArch32 System register HIFAR bits [31:0] are architecturally mapped to AArch32 System register `IFAR[31:0]` when EL2 is implemented, EL3 is implemented and the highest implemented Exception level is using AArch32 state.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HIFAR are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

HIFAR is a 32-bit register.

**Field descriptions**

The HIFAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td><strong>VA of faulting address of synchronous Prefetch Abort exception taken to Hyp mode</strong></td>
</tr>
<tr>
<td>30</td>
<td></td>
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<tr>
<td>29</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:0]**

- **VA of faulting address of synchronous Prefetch Abort exception taken to Hyp mode**.
- On a Data Abort exception, this register is **UNKNOWN**.
- Any execution in a Non-secure EL1 or Non-secure EL0 mode makes this register **UNKNOWN**.
- On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the HIFAR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HIFAR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HIFAR;

MCR{'c'}{'q'} <coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HIFAR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HIFAR = R[t];

HMAIR0, Hyp Memory Attribute Indirection Register 0

The HMAIR0 characteristics are:

**Purpose**

Along with HMAIR1, provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations for memory accesses from Hyp mode.

AttrIndx[2] indicates the HMAIR register to be used:

- When AttrIndx[2] is 0, HMAIR0 is used.
- When AttrIndx[2] is 1, HMAIR1 is used.

**Configuration**

AArch32 System register HMAIR0 bits [31:0] are architecturally mapped to AArch64 System register MAIR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HMAIR0 are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HMAIR0 is a 32-bit register.

**Field descriptions**

The HMAIR0 bit assignments are:

**When TTBCR.EAE == 1:**

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
| Attr3 | Attr2 | Attr1 | Attr0 |

Attr<n>, bits [8n+7:8n], for n = 3 to 0

The memory attribute encoding for an AttrIndx[2:0] entry in a Long descriptor format translation table entry, where:

- AttrIndx[2:0] gives the value of <n> in Attr<n>.
- AttrIndx[2] defines which MAIR to access. Attr7 to Attr4 are in MAIR1, and Attr3 to Attr0 are in MAIR0.

Bits [7:4] are encoded as follows:

<table>
<thead>
<tr>
<th>Attr&lt;n&gt;[7:4]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device memory. See encoding of Attr&lt;n&gt;[3:0] for the type of Device memory.</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Outer Write-Through Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Outer Write-Back Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Outer Write-Through Non-transient.</td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Outer Write-Back Non-transient.</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Outer Write-Back Non-transient.</td>
</tr>
</tbody>
</table>

R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

The meaning of bits [3:0] depends on the value of bits [7:4]:

Page 2480
### Accessing the HMAIR0

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2}\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
AArch32.TakeHypTrapException(0x03);
else
UNDEFINED;
elsif PSTATE.EL == EL2 then
return HMAIR0;
elsif PSTATE.EL == EL3 then
if SCR.NS == '0' then
UNDEFINED;
else
return HMAIR0;
\]

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2}\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    HMAIR0 = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HMAIR0 = R[t];
    end if;

HMAIR1, Hyp Memory Attribute Indirection Register 1

The HMAIR1 characteristics are:

**Purpose**

Along with HMAIR0, provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations for memory accesses from Hyp mode.

AttrIndx[2] indicates the HMAIR register to be used:
- When AttrIndx[2] is 0, HMAIR0 is used.
- When AttrIndx[2] is 1, HMAIR1 is used.

**Configuration**

AArch32 System register HMAIR1 bits [31:0] are architecturally mapped to AArch64 System register MAIR_EL2[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HMAIR1 are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

HMAIR1 is a 32-bit register.

**Field descriptions**

The HMAIR1 bit assignments are:

**When TTBCR.EAE == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Attr7, bits [8(7)+7:7(4)], for n = 7 to 4</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>0b0000: Device memory. See encoding of Attr&lt;n&gt;[3:0] for the type of Device memory.</td>
</tr>
<tr>
<td>0</td>
<td>0b00RW, RW, Normal memory, Outer Write-Through Transient.</td>
</tr>
<tr>
<td></td>
<td>not0b00</td>
</tr>
<tr>
<td>0</td>
<td>0b01RW, RW, Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td></td>
<td>not0b01</td>
</tr>
<tr>
<td>0</td>
<td>0b10RW, RW, Normal memory, Outer Write-Back Transient.</td>
</tr>
<tr>
<td></td>
<td>not0b10</td>
</tr>
<tr>
<td>0</td>
<td>0b11RW, Normal memory, Outer Write-Through Non-transient.</td>
</tr>
<tr>
<td></td>
<td>not0b11</td>
</tr>
</tbody>
</table>

R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

The meaning of bits [3:0] depends on the value of bits [7:4]:

---

Page 2483
### Accessing the HMAIR1

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \ <\text{coproc}\>, \{#<\text{opc1}>\}, \ <\text{Rt}\>, \ <\text{CRn}\>, \ <\text{CRm}\>{, \{#<\text{opc2}>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HMAIR1;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HMAIR1;

\[
\text{MCR}\{<c>\}{<q>} \ <\text{coproc}\>, \{#<\text{opc1}>\}, \ <\text{Rt}\>, \ <\text{CRn}\>, \ <\text{CRm}\>{, \{#<\text{opc2}>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HMAIR1 = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HMAIR1 = R[t];
HPFAR, Hyp IPA Fault Address Register

The HPFAR characteristics are:

**Purpose**

Holds the faulting IPA for some aborts on a stage 2 translation taken to Hyp mode.

**Configuration**

AArch32 System register HPFAR bits [31:0] are architecturally mapped to AArch64 System register `HPFAR_EL2[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HPFAR are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

HPFAR is a 32-bit register.

**Field descriptions**

The HPFAR bit assignments are:

```
   31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
```

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bits [3:0]</td>
<td>RES0</td>
</tr>
</tbody>
</table>

Execution in any Non-secure mode other than Hyp mode makes this register **UNKNOWN**.

**FIPA[39:12], bits [31:4]**

Bits [39:12] of the faulting intermediate physical address.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [3:0]**

Reserved, RES0.

**Accessing the HPFAR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
eslif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        return HPFAR;
eslif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HPFAR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
eslif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        HPFAR = R[t];
eslif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HPFAR = R[t];
HRMR, Hyp Reset Management Register

The HRMR characteristics are:

**Purpose**

If EL2 is the highest implemented Exception level and this register is implemented:

- A write to the register at EL2 can request a Warm reset.
- If EL2 can use AArch32 and AArch64, this register specifies the Execution state that the PE boots into on a Warm reset.

**Configuration**

AArch32 System register HRMR bits [31:0] are architecturally mapped to AArch64 System register \texttt{RMR\_EL2[31:0]}.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HRMR are UNDEFINED.

Only implemented if EL2 is the highest implemented Exception level. In this case:

- If EL2 can use AArch32 and AArch64 then this register must be implemented.
- If EL2 cannot use AArch64 then it is IMPLEMENTATION DEFINED whether the register is implemented.

**Attributes**

HRMR is a 32-bit register.

**Field descriptions**

The HRMR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>30</td>
<td>RR</td>
</tr>
<tr>
<td>29</td>
<td>AArch64</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [31:2]**

Reserved, RES0.

**RR, bit [1]**

Reset Request. Setting this bit to 1 requests a Warm reset.

On a Warm reset, this field resets to 0.

**AA64, bit [0]**

When EL2 can use AArch64, determines which Execution state the PE boots into after a Warm reset:

<table>
<thead>
<tr>
<th>AA64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>AArch64.</td>
</tr>
</tbody>
</table>

On coming out of the Warm reset, execution starts at the IMPLEMENTATION DEFINED reset vector address of the specified Execution state.

If EL2 cannot use AArch64 this bit is RAZ/WI.

When implemented as a RW field, this field resets to 0 on a Cold reset.
Accessing the HRMR

Accesses to this register use the following encodings:

\[
\text{MRC\{c\}{\langle q\rangle} \coproc, \{\langle opc1\rangle, \langle Rt\rangle, \langle CRn\rangle, \langle CRm\rangle\}, \{\langle opc2\rangle\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif PSTATE.EL == EL2 && IsHighestEL(EL2) then
    return HRMR;
else
    UNDEFINED;
```

\[
\text{MCR\{c\}{\langle q\rangle} \coproc, \{\langle opc1\rangle, \langle Rt\rangle, \langle CRn\rangle, \langle CRm\rangle\}, \{\langle opc2\rangle\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif PSTATE.EL == EL1 && EL2Enabled() && IsHighestEL(EL2) && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif PSTATE.EL == EL2 && IsHighestEL(EL2) then
    HRMR = R[t];
else
    UNDEFINED;
```
HSCTRL, Hyp System Control Register

The HSCTRL characteristics are:

**Purpose**

Provides top level control of the system operation in Hyp mode.

**Configuration**

AArch32 System register HSCTRL bits [31:0] are architecturally mapped to AArch64 System register SCTLR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HSCTRL are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HSCTRL is a 32-bit register.

**Field descriptions**

The HSCTRL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DSSBS | TE | RES1 | RES0 | EEE | RES0 | RES0 | WXN | RES1 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | SED | TD | RES0 | RES0 | CP15B | LSMAOE | hTLS |

**DSSBS, bit [31]**

When FEAT_SSBS is implemented:

Default PSTATE.SSBS value on Exception Entry. The defined values are:

<table>
<thead>
<tr>
<th>DSSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.SSBS is set to 0 on an exception to Hyp mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>PSTATE.SSBS is set to 1 on an exception to Hyp mode.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an IMPLEMENTATION DEFINED value.

**Otherwise:**

Reserved, RES0.

**TE, bit [30]**

T32 Exception Enable. This bit controls whether exceptions to EL2 are taken to A32 or T32 state:

<table>
<thead>
<tr>
<th>TE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exceptions, including reset, taken to A32 state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exceptions, including reset, taken to T32 state.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.
Bits [29:28]
Reserved, RES1.

Bits [27:26]
Reserved, RES0.

EE, bit [25]

The value of the PSTATE.E bit on entry to Hyp mode, the endianness of stage 1 translation table walks in the EL2 translation regime, and the endianness of stage 2 translation table walks in the PL1&0 translation regime.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Little-endian. PSTATE.E is cleared to 0 on entry to Hyp mode. Stage 1 translation table walks in the EL2 translation regime, and stage 2 translation table walks in the PL1&amp;0 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Big-endian. PSTATE.E is set to 1 on entry to Hyp mode. Stage 1 translation table walks in the EL2 translation regime, and stage 2 translation table walks in the PL1&amp;0 translation regime are big-endian.</td>
</tr>
</tbody>
</table>

If an implementation does not provide Big-endian support at Exception Levels higher than EL0, this bit is RES0.

If an implementation does not provide Little-endian support at Exception Levels higher than EL0, this bit is RES1.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Bit [24]
Reserved, RES0.

Bits [23:22]
Reserved, RES1.

Bits [21:20]
Reserved, RES0.

WXN, bit [19]

Write permission implies XN (Execute-never). For the EL2 translation regime, this bit can force all memory regions that are writable to be treated as XN. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable in the EL2 translation regime is forced to XN for accesses from software executing at EL2.</td>
</tr>
</tbody>
</table>

This bit applies only when HSCTL.R.M bit is set.

The WXN bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

Bit [18]
Reserved, RES1.
**Bit [17]**

Reserved, RES0.

**Bit [16]**

Reserved, RES1.

**Bits [15:13]**

Reserved, RES0.

**I, bit [12]**

Instruction access Cacheability control, for accesses at EL2:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction access to Normal memory from EL2 are Non-cacheable for all levels of instruction and unified cache. If the value of HSCTLR.M is 0, instruction accesses from stage 1 of the EL2 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>All instruction access to Normal memory from EL2 can be cached at all levels of instruction and unified cache. If the value of HSCTLR.M is 0, instruction accesses from stage 1 of the EL2 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

This bit has no effect on the PL1&0 translation regime.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

**Bit [11]**

Reserved, RES1.

**Bits [10:9]**

Reserved, RES0.

**SED, bit [8]**

SETEND instruction disable. Disables SETEND instructions at EL2.

<table>
<thead>
<tr>
<th>SED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SETEND instruction execution is enabled at EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>SETEND instructions are UNDEFINED at EL2.</td>
</tr>
</tbody>
</table>

If the implementation does not support mixed-endian operation at EL2, this bit is RES1.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

**ITD, bit [7]**

IT Disable. Disables some uses of IT instructions at EL2.
### ITD

<table>
<thead>
<tr>
<th>ITD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All IT instruction functionality is enabled at EL2.</td>
</tr>
</tbody>
</table>
| 0b1 | Any attempt at EL2 to execute any of the following is UNDEFINED:  
  - All encodings of the IT instruction with hw1[3:0]! = 1000.  
  - All encodings of the subsequent instruction with the following values for hw1:  
    - 11xxxxxxxxxxxx: All 32-bit instructions, and the 16-bit instructions B, UDF, SVC, LDM, and STM.  
    - 1011xxxxxxxxxxxx: All instructions in 'Miscellaneous 16-bit instructions'.  
    - 10100xxxxxxxxxxx: ADD Rd, PC, #imm  
    - 01001xxxxxxxxxxx: LDR Rd, [PC, #imm]  
    - 010011xxx1111xxx: ADD Rdn, PC; CMP Rn, PC; MOV Rd, PC; BX PC; BLX PC.  
    - 0100011xxxx111: ADD PC, Rm; CMP PC, Rm; MOV PC, Rm. This pattern also covers unpredictable cases with BLX Rn.  

These instructions are always UNDEFINED, regardless of whether they would pass or fail the condition code check that applies to them as a result of being in an IT block.  
It is IMPLEMENTATION DEFINED whether the IT instruction is treated as:  
  - A 16-bit instruction, that can only be followed by another 16-bit instruction.  
  - The first half of a 32-bit instruction.  

This means that, for the situations that are UNDEFINED, either the second 16-bit instruction or the 32-bit instruction is UNDEFINED. An implementation might vary dynamically as to whether IT is treated as a 16-bit instruction or the first half of a 32-bit instruction. |

If an instruction in an active IT block that would be disabled by this field sets this field to 1 then behavior is CONSTRAINED UNPREDICTABLE. For more information, see 'Changes to an ITD control by an instruction in an IT block'.

ITD is optional, but if it is implemented in the SCTLR then it must also be implemented in the HSCTLR. If it is not implemented then this bit is RAZ/WI.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

### Bit [6]

Reserved, RES0.

### CP15BEN, bit [5]

System instruction memory barrier enable. Enables accesses to the DMB, DSB, and ISB System instructions in the (coproc==0b1111) encoding space from EL2:

<table>
<thead>
<tr>
<th>CP15BEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is enabled.</td>
</tr>
</tbody>
</table>

CP15BEN is optional, but if it is implemented in the SCTLR then it must also be implemented in the HSCTLR. If it is not implemented then this bit is RAO/WI.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

### LSMAOE, bit [4]

When FEAT_LSMAOC is implemented:

Load Multiple and Store Multiple Atomicity and Ordering Enable.
For all memory accesses at EL2, A32 and T32 Load Multiple and Store Multiple can have an interrupt taken during the sequence memory accesses, and the memory accesses are not required to be ordered.

The ordering and interrupt behavior of A32 and T32 Load Multiple and Store Multiple at EL2 is as defined for Armv8.0.

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 1.

Otherwise:

Reserved, RES1.

When FEAT_LSMAOC is implemented:

No Trap Load Multiple and Store Multiple to Device-nGRE/Device-nGnRE/Device-nGnRnE memory.

All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL2 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are trapped and generate a stage 1 Alignment fault.

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 1.

Otherwise:

Reserved, RES1.

Cacheability control, for data accesses at EL2:

All data access to Normal memory from EL2, and all accesses to the EL2 translation tables, are Non-cacheable for all levels of data and unified cache.

All data access to Normal memory from EL2, and all accesses to the EL2 translation tables, can be cached at all levels of data and unified cache.

This bit has no effect on the PL1&0 translation regime.

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Alignment check enable. This is the enable bit for Alignment fault checking at EL2:
Meaning

0b0 Alignment fault checking disabled when executing at EL2. Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element or data elements being accessed.

0b1 Alignment fault checking enabled when executing at EL2. All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element or data elements being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception.

Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.

On a Warm reset, in a system where the PE resets into EL2, this field resets to an architecturally UNKNOWN value.

M, bit [0]

MMU enable for EL2 stage 1 address translation. Possible values of this bit are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL2 stage 1 address translation disabled.</td>
</tr>
<tr>
<td></td>
<td>See the HSCTLR.I field for the behavior of instruction accesses to Normal memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL2 stage 1 address translation enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2, this field resets to 0.

Accessing the HSCTLR

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
endif;
elsif PSTATE.EL == EL2 then
  return HSCTLR;
else
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HSCTLR;
endif;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    HSCTRL = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        HSCTRL = R[t];

HSR, Hyp Syndrome Register

The HSR characteristics are:

**Purpose**

Holds syndrome information for an exception taken to Hyp mode.

**Configuration**

AArch32 System register HSR bits [31:0] are architecturally mapped to AArch64 System register ESR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HSR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HSR is a 32-bit register.

**Field descriptions**

The HSR bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| EC  | IL  | ISS |

Execution in any Non-secure PE mode other than Hyp mode makes this register UNKNOWN.

When an UNPREDICTABLE instruction is treated as UNDEFINED, and the exception is taken to EL2, the value of HSR is UNKNOWN. The value written to HSR must be consistent with a value that could be created as a result of an exception from the same Exception level that generated the exception as a result of a situation that is not UNPREDICTABLE at that Exception level, in order to avoid the possibility of a privilege violation.

**EC, bits [31:26]**

Exception Class. Indicates the reason for the exception that this register holds information about. Possible values of this field are:
<table>
<thead>
<tr>
<th>EC</th>
<th>Meaning</th>
<th>ISS</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Unknown reason.</td>
<td>ISS encoding for exceptions with an unknown reason</td>
</tr>
<tr>
<td>0b000001</td>
<td>Trapped WFI or WFE instruction execution. Conditional WFE and WFI instructions that fail their condition code check do not cause an exception.</td>
<td>ISS encoding for Exception from a WFI or WFE instruction</td>
</tr>
<tr>
<td>0b000111</td>
<td>Trapped MCR or MRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for Exception from an MCR or MRC access</td>
</tr>
<tr>
<td>0b000100</td>
<td>Trapped MCRR or MRRRC access with (coproc==0b1111) that is not reported using EC 0b000000.</td>
<td>ISS encoding for Exception from an MCRR or MRRRC access</td>
</tr>
<tr>
<td>0b000101</td>
<td>Trapped MCR or MRC access with (coproc==0b1110).</td>
<td>ISS encoding for Exception from an MCR or MRC access</td>
</tr>
<tr>
<td>0b001100</td>
<td>Trapped LDC or STC access. The only architected uses of these instructions are: An STC to write data to memory from DBGDTRRXint. An LDC to read data from memory to DBGDTRTXint.</td>
<td>ISS encoding for Exception from an LDC or STC instruction</td>
</tr>
<tr>
<td>0b001111</td>
<td>Access to Advanced SIMD or floating-point functionality trapped by a HCPTR {TASE, TCP10} control. Excludes exceptions generated because Advanced SIMD and floating-point are not implemented. These are reported with EC value 0b000000.</td>
<td>ISS encoding for Exception from an access to SIMD or floating-point functionality, resulting from HCPTR</td>
</tr>
<tr>
<td>0b001000</td>
<td>Trapped VMRS access, from ID group trap, that is not reported using EC 0b000111.</td>
<td>ISS encoding for Exception from an MCR or MRC access</td>
</tr>
<tr>
<td>0b001100</td>
<td>Trapped MRRRC access with (coproc==0b1110).</td>
<td>ISS encoding for Exception from an MCRR or MRRRC access</td>
</tr>
<tr>
<td>0b001110</td>
<td>Illegal exception return to AArch32 state.</td>
<td>ISS encoding for Exception from an Illegal state or PC alignment fault</td>
</tr>
<tr>
<td>0b010001</td>
<td>Exception on SVC instruction execution in AArch32 state routed to EL2.</td>
<td>ISS encoding for Exception from HVC or SVC instruction execution</td>
</tr>
<tr>
<td>0b010010</td>
<td>HVC instruction execution in AArch32 state, when HVC is not disabled.</td>
<td>ISS encoding for Exception from HVC or SVC instruction execution</td>
</tr>
<tr>
<td>0b010011</td>
<td>Trapped execution of SMC instruction in AArch32 state.</td>
<td>ISS encoding for Exception from SMC instruction execution</td>
</tr>
<tr>
<td>0b100000</td>
<td>Prefetch Abort from a lower Exception level.</td>
<td>ISS encoding for Exception from a Prefetch Abort</td>
</tr>
<tr>
<td>0b100001</td>
<td>Prefetch Abort taken without a change in Exception level.</td>
<td>ISS encoding for Exception from a Prefetch Abort</td>
</tr>
<tr>
<td>0b100010</td>
<td>PC alignment fault exception.</td>
<td>ISS encoding for Exception from an Illegal state or PC alignment fault</td>
</tr>
</tbody>
</table>
Data Abort from a lower Exception level.

Data Abort taken without a change in Exception level.

All other EC values are reserved by Arm, and:

- Unused values in the range 0b000000 - 0b101100 (0x00 - 0x2C) are reserved for future use for synchronous exceptions.
- Unused values in the range 0b101101 - 0b111111 (0x2D - 0x3F) are reserved for future use, and might be used for synchronous or asynchronous exceptions.

The effect of programming this field to a reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IL, bit [25]**

Instruction length bit. Indicates the size of the instruction that has been trapped to Hyp mode. When this bit is valid, possible values of this bit are:

<table>
<thead>
<tr>
<th>IL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>16-bit instruction trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>32-bit instruction trapped.</td>
</tr>
</tbody>
</table>

This field is RES1 and not valid for the following cases:

- When the EC field is 0b000000, indicating an exception with an unknown reason.
- Prefetch Aborts.
- Data Aborts for which the HSR.ISS.ISV field is 0.
- When the EC value is 0b001110, indicating an Illegal state exception.

Note

This is a change from the behavior in Armv7, where the IL field is UNK/SBZP for the corresponding cases.

The IL field is not valid and is UNKNOWN on an exception from a PC alignment fault.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ISS, bits [24:0]**

Instruction Specific Syndrome. Architecturally, this field can be defined independently for each defined Exception class. However, in practice, some ISS encodings are used for more than one Exception class.

**ISS encoding for exceptions with an unknown reason**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |

**Bits [24:0]**

Reserved, RES0.

This EC code is used for all exceptions that are not covered by any other EC value. This includes exceptions that are generated in the following situations:

- The attempted execution of an instruction bit pattern that has no allocated instruction or is not accessible in the current PE mode in the current Security state, including:
  - A read access using a System register encoding pattern that is not allocated for reads or that does not permit reads in the current PE mode and Security state.
A write access using a System register encoding pattern that is not allocated for writes or that does not permit writes in the current PE mode and Security state.

Instruction encodings that are unallocated.

Instruction encodings for instructions not implemented in the implementation.

- In Debug state, the attempted execution of an instruction bit pattern that is not accessible in Debug state.
- In Non-debug state, the attempted execution of an instruction bit pattern that is not accessible in Non-debug state.
- The attempted execution of a short vector floating-point instruction.
- In an implementation that does not include Advanced SIMD and floating-point functionality, an attempted access to Advanced SIMD or floating-point functionality under conditions where that access would be permitted if that functionality was present. This includes the attempted execution of an Advanced SIMD or floating-point instruction, and attempted accesses to Advanced SIMD and floating-point System registers.
- An exception generated because of the value of one of the SCTLR.{ITD, SED, CP15BEN} control bits.
- Attempted execution of:
  - An HVC instruction when disabled by HCR.HCD, SCR.HCE, or SCR_EL3.HCE.
  - An SMC instruction when disabled by SCR.SCD or SCR_EL3.SMD.
  - An HLT instruction when disabled by EDSCR.HDE.
- An HVC instruction when disabled by HCR.HCD, SCR.HCE, or SCR_EL3.HCE.
- An SMC instruction when disabled by SCR.SCD or SCR_EL3.SMD.
- An HLT instruction when disabled by EDSCR.HDE.
- An exception generated because of the attempted execution of an MSR (Banked register) or MRS (Banked register) instruction that would access a Banked register that is not accessible from the Security state and PE mode at which the instruction was executed.

**Note**

An exception is generated only if the CONSTRAINED UNPREDICTABLE behavior of the instruction is that it is UNDEFINED, see 'MSR (banked register) and MRS (banked register)'.

- Attempted execution, in Debug state, of:
  - A DCPS1 instruction in Non-secure state from EL0 when EL2 is using AArch32 and the value of HCR.TGE is 1.
  - A DCPS2 instruction at EL1 or EL0 when EL2 is not implemented, or when EL3 is using AArch32 and the value of SCR.NS is 0, or when EL3 is using AArch64 and the value of SCR_EL3.NS is 0.
  - A DCPS3 instruction when EL3 is not implemented, or when the value of EDSCR.SDD is 1.
- In Debug state when the value of EDSCR.SDD is 1, the attempted execution at EL2, EL1, or EL0 of an instruction that is configured to trap to EL3.

'Undefined Instruction exception, when the value of HCR.TGE is 1' describes the configuration settings for a trap that returns an HSR.EC value of 0b000000.

**ISS encoding for Exception from a WFI or WFE instruction**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | RES0 | Ti |

**CV, bit [24]**

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

The condition code for the trapped instruction.
When an A32 instruction is trapped, CV is set to 1 and:

- If the instruction is conditional, COND is set to the condition code field value from the instruction.
- If the instruction is unconditional, COND is set to 0b1110.

A conditional A32 instruction that is known to pass its condition code check can be presented either:

- With COND set to 0b1110, the value for unconditional.
- With the COND value held in the instruction.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:

- CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
- CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [19:1]**

Reserved, RES0.

**TI, bit [0]**

Trapped instruction. Possible values of this bit are:

<table>
<thead>
<tr>
<th>TI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>WFI trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>WFE trapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

‘Traps to Hyp mode of Non-secure EL0 and EL1 execution of WFE and WFI instructions’ describes the configuration settings for this trap.

**ISS encoding for Exception from an MCR or MRC access**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | Opc2 | Opc1 | CRn | RES0 | Rt | CRm | Direction |

**CV, bit [24]**

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

The condition code for the trapped instruction.

When an A32 instruction is trapped, CV is set to 1 and:
If the instruction is conditional, COND is set to the condition code field value from the instruction.
If the instruction is unconditional, COND is set to 0b1110.

A conditional A32 instruction that is known to pass its condition code check can be presented either:
• With COND set to 0b1110, the value for unconditional.
• With the COND value held in the instruction.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:
• CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
• CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Opc2, bits [19:17]**

The Opc2 value from the issued instruction.
For a trapped VMRS access, holds the value 0b000.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Opc1, bits [16:14]**

The Opc1 value from the issued instruction.
For a trapped VMRS access, holds the value 0b111.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRn, bits [13:10]**

The CRn value from the issued instruction.
For a trapped VMRS access, holds the reg field from the VMRS instruction encoding.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [9]**

Reserved, RES0.

**Rt, bits [8:5]**

The Rt value from the issued instruction, the general-purpose register used for the transfer.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.
For a trapped VMRS access, holds the value 0b0000.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Direction, bit [0]**

Indicates the direction of the trapped instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRC or VMRS instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following sections describe configuration settings for traps that are reported using EC value `0b000011`:

- 'Traps to Hyp mode of Non-secure EL0 and EL1 accesses to the ID registers'.
- 'Traps to Hyp mode of Non-secure EL0 and EL1 accesses to lockdown, DMA, and TCM operations'.
- 'Traps to Hyp mode of Non-secure EL1 execution of cache maintenance instructions'.
- 'Traps to Hyp mode of Non-secure EL1 execution of TLB maintenance instructions'.
- 'Traps to Hyp mode of Non-secure EL1 accesses to the Auxiliary Control Register'.
- 'Traps to Hyp mode of Non-secure EL0 and EL1 accesses to Performance Monitors registers'.
- 'Traps to Hyp mode of Non-secure EL0 and EL1 accesses to Activity Monitors registers'.
- 'Traps to Hyp mode of Non-secure EL1 accesses to the CPACR'.
- 'Traps to Hyp mode of Non-secure EL1 accesses to virtual memory control registers'.
- 'General trapping to Hyp mode of Non-secure EL0 and EL1 accesses to System registers in the (coproc == 1111) encoding space'.

The following sections describe configuration settings for traps that are reported using EC value `0b000101`:

- 'ID group 0, Primary device identification registers'.
- 'Traps to Hyp mode of Non-secure System register accesses to trace registers'.
- 'Trapping Non-secure System register accesses to Debug ROM registers'.
- 'Trapping Non-secure System register accesses to powerdown debug registers'.
- 'Trapping general Non-secure System register accesses to debug registers'.

The following sections describe configuration settings for traps that are reported using EC value `0b001000`:

- 'ID group 0, Primary device identification registers'.
- 'ID group 3, Detailed feature identification registers'.

**ISS encoding for Exception from an MCRR or MRRC access**

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV | COND | Opc1 | RES0 | Rt2 | RES0 | Rt | CRm | Direction |

**CV, bit [24]**

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**COND, bits [23:20]**

The condition code for the trapped instruction.

When an A32 instruction is trapped, CV is set to 1 and:

- If the instruction is conditional, COND is set to the condition code field value from the instruction.
- If the instruction is unconditional, COND is set to `0b1110`. 
A conditional A32 instruction that is known to pass its condition code check can be presented either:

- With COND set to \(0b1110\), the value for unconditional.
- With the COND value held in the instruction.

When a T32 instruction is trapped, it is **IMPLEMENTATION DEFINED** whether:

- CV is set to 0 and COND is set to an **UNKNOWN** value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
- CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is **IMPLEMENTATION DEFINED** whether the COND field is set to \(0b1110\), or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Opc1, bits [19:16]**

The Opc1 value from the issued instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [15:14]**

Reserved, **RES0**.

**Rt2, bits [13:10]**

The Rt2 value from the issued instruction, the second general-purpose register used for the transfer.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [9]**

Reserved, **RES0**.

**Rt, bits [8:5]**

The Rt value from the issued instruction, the first general-purpose register used for the transfer.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**CRm, bits [4:1]**

The CRm value from the issued instruction.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Direction, bit [0]**

Indicates the direction of the trapped instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to System register space. MCRR instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from System register space. MRRC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The following sections describe configuration settings for traps that are reported using EC value \(0b000100\):

- ‘Traps to Hyp mode of Non-secure EL1 accesses to virtual memory control registers’.
- ‘Traps to Hyp mode of Non-secure EL0 and EL1 accesses to Performance Monitors registers’.
• ‘Traps to Hyp mode of Non-secure EL0 and EL1 accesses to Activity Monitors registers’.
• ‘Traps to Hyp mode of Non-secure EL0 and EL1 accesses to the Generic Timer registers’.
• ‘General trapping to Hyp mode of Non-secure EL0 and EL1 accesses to System registers in the (coproc == 1111) encoding space’.

The following sections describe configuration settings for traps that are reported using EC value 0b001100:

• ‘Traps to Hyp mode of Non-secure System register accesses to trace registers’.
• ‘Trapping Non-secure System register accesses to Debug ROM registers’.

ISS encoding for Exception from an LDC or STC instruction

<table>
<thead>
<tr>
<th>CV</th>
<th>COND</th>
<th>imm8</th>
<th>RES0</th>
<th>Rn</th>
<th>Offset</th>
<th>AM</th>
<th>Direction</th>
</tr>
</thead>
</table>

**CV, bit [24]**

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**COND, bits [23:20]**

The condition code for the trapped instruction.

When an A32 instruction is trapped, CV is set to 1 and:

• If the instruction is conditional, COND is set to the condition code field value from the instruction.
• If the instruction is unconditional, COND is set to 0b1110.

A conditional A32 instruction that is known to pass its condition code check can be presented either:

• With COND set to 0b1110, the value for unconditional.
• With the COND value held in the instruction.

When a T32 instruction is trapped, it is IMPLEMENTATION DEFINED whether:

• CV is set to 0 and COND is set to an UNKNOWN value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
• CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is IMPLEMENTATION DEFINED whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**imm8, bits [19:12]**

The immediate value from the issued instruction.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [11:9]**

Reserved, RES0.
Rn, bits [8:5]

The Rn value from the issued instruction. Valid only when AM[2] is 0, indicating an immediate form of the
LDC or STC instruction.

When AM[2] is 1, indicating a literal form of the LDC or STC instruction, this field is \textit{UNKNOWN}.

On a Warm reset, this field resets to an architecturally unknown value.

Offset, bit [4]

Indicates whether the offset is added or subtracted:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Subtract offset.</td>
</tr>
<tr>
<td>0b1</td>
<td>Add offset.</td>
</tr>
</tbody>
</table>

This bit corresponds to the U bit in the instruction encoding.

On a Warm reset, this field resets to an architecturally unknown value.

AM, bits [3:1]

Addressing mode. The permitted values of this field are:

<table>
<thead>
<tr>
<th>AM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Immediate unindexed.</td>
</tr>
<tr>
<td>0b01</td>
<td>Immediate post-indexed.</td>
</tr>
<tr>
<td>0b10</td>
<td>Immediate offset.</td>
</tr>
<tr>
<td>0b11</td>
<td>Immediate pre-indexed.</td>
</tr>
<tr>
<td>0b100</td>
<td>Literal unindexed.</td>
</tr>
<tr>
<td></td>
<td>LDC instruction in A32 instruction set only.</td>
</tr>
<tr>
<td></td>
<td>For a trapped STC instruction or a trapped</td>
</tr>
<tr>
<td></td>
<td>T32 LDC instruction this encoding is reserved.</td>
</tr>
<tr>
<td>0b110</td>
<td>Literal offset.</td>
</tr>
<tr>
<td></td>
<td>LDC instruction only.</td>
</tr>
<tr>
<td></td>
<td>For a trapped STC instruction, this encoding is reserved.</td>
</tr>
</tbody>
</table>

The values 0b101 and 0b111 are reserved. The effect of programming this field to a reserved value is that behavior is \textit{CONSTRAINED UNPREDICTABLE}.

Bit [2] in this subfield indicates the instruction form, immediate or literal.

Bits [1:0] in this subfield correspond to the bits \{P, W\} in the instruction encoding.

On a Warm reset, this field resets to an architecturally unknown value.

Direction, bit [0]

Indicates the direction of the trapped instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>Direction</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Write to memory. STC instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read from memory. LDC instruction.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

'\textit{Trapping general Non-secure System register accesses to debug registers}' describes the configuration settings for the trap that is reported using EC value 0b000110.

\textbf{ISS encoding for Exception from an access to SIMD or floating-point functionality, resulting from HCPTR}

| 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CV |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
Excludes exceptions that occur because Advanced SIMD and floating-point functionality is not implemented, or because the value of HCR.TGE or HCR_EL2.TGE is 1. These are reported with EC value 0b000000.

**CV, bit [24]**

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.

When a T32 instruction is trapped, it is implementation defined whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

On a Warm reset, this field resets to an architecturally unknown value.

**COND, bits [23:20]**

The condition code for the trapped instruction.

When an A32 instruction is trapped, CV is set to 1 and:

- If the instruction is conditional, COND is set to the condition code field value from the instruction.
- If the instruction is unconditional, COND is set to 0b1110.

A conditional A32 instruction that is known to pass its condition code check can be presented either:

- With COND set to 0b1110, the value for unconditional.
- With the COND value held in the instruction.

When a T32 instruction is trapped, it is implementation defined whether:

- CV is set to 0 and COND is set to an unknown value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
- CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is implementation defined whether the COND field is set to 0b1110, or to the value of any condition that applied to the instruction.

On a Warm reset, this field resets to an architecturally unknown value.

**Bits [19:6]**

Reserved, RES0.

**TA, bit [5]**

Indicates trapped use of Advanced SIMD functionality. The possible values of this bit are:

<table>
<thead>
<tr>
<th>TA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception was not caused by trapped use of Advanced SIMD functionality.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception was caused by trapped use of Advanced SIMD functionality.</td>
</tr>
</tbody>
</table>

Any use of an Advanced SIMD instruction that is not also a floating-point instruction that is trapped to Hyp mode because of a trap configured in the HCPTR sets this bit to 1.

For a list of these instructions, see 'Controls of Advanced SIMD operation that do not apply to floating-point operation'.

On a Warm reset, this field resets to an architecturally unknown value.
Bit [4]

Reserved, RES0.

coproc, bits [3:0]

When the HSR.TA field returns the value 1, this field returns the value 0b1010. Otherwise, this field is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following sections describe the configuration settings for the traps that are reported using EC value 0b000111:

- 'General trapping to Hyp mode of Non-secure accesses to the SIMD and floating-point registers'.
- 'Traps to Hyp mode of Non-secure accesses to Advanced SIMD functionality'.

ISS encoding for Exception from HVC or SVC instruction execution

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>imm16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [24:16]

Reserved, RES0.

imm16, bits [15:0]

The value of the immediate field from the HVC or SVC instruction.

For an HVC instruction, this is the value of the imm16 field of the issued instruction.

For an SVC instruction:

- If the instruction is unconditional, then:
  - For the T32 instruction, this field is zero-extended from the imm8 field of the instruction.
  - For the A32 instruction, this field is the bottom 16 bits of the imm24 field of the instruction.
- For the T32 instruction, this field is zero-extended from the imm8 field of the instruction. For the A32 instruction, this field is the bottom 16 bits of the imm24 field of the instruction.
- If the instruction is conditional, this field is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The HVC instruction is unconditional, and a conditional SVC instruction generates an exception only if it passes its condition code check. Therefore, the syndrome information for these exceptions does not require conditionality information.

'Supervisor Call exception, when the value of HCR.TGE is 1' describes the configuration settings for the trap reported with EC value 0b010001.

ISS encoding for Exception from SMC instruction execution

<table>
<thead>
<tr>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CV</td>
<td>COND</td>
<td>CCKNOWNPASS</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

CV, bit [24]

Condition code valid. Possible values of this bit are:

<table>
<thead>
<tr>
<th>CV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The COND field is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The COND field is valid.</td>
</tr>
</tbody>
</table>

When an A32 instruction is trapped, CV is set to 1.
When a T32 instruction is trapped, it is \texttt{IMPLEMENTATION DEFINED} whether CV is set to 1 or set to 0. For more information, see the description of the COND field.

This field is valid only if CCKNOWPASS is 1, otherwise it is \texttt{RES0}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{COND, bits [23:20]}

The condition code for the trapped instruction.

When an A32 instruction is trapped, CV is set to 1 and:

\begin{itemize}
  \item If the instruction is conditional, COND is set to the condition code field value from the instruction.
  \item If the instruction is unconditional, COND is set to \texttt{0b1110}.
\end{itemize}

A conditional A32 instruction that is known to pass its condition code check can be presented either:

\begin{itemize}
  \item With COND set to \texttt{0b1110}, the value for unconditional.
  \item With the COND value held in the instruction.
\end{itemize}

When a T32 instruction is trapped, it is \texttt{IMPLEMENTATION DEFINED} whether:

\begin{itemize}
  \item CV is set to 0 and COND is set to an \texttt{UNKNOWN} value. Software must examine the SPSR.IT field to determine the condition, if any, of the T32 instruction.
  \item CV is set to 1 and COND is set to the condition code for the condition that applied to the instruction.
\end{itemize}

For an implementation that, for both A32 and T32 instructions, takes an exception on a trapped conditional instruction only if the instruction passes its condition code check, these definitions mean that when CV is set to 1 it is \texttt{IMPLEMENTATION DEFINED} whether the COND field is set to \texttt{0b1110}, or to the value of any condition that applied to the instruction.

This field is valid only if CCKNOWPASS is 1, otherwise it is \texttt{RES0}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{CCKNOWPASS, bit [19]}

Indicates whether the instruction might have failed its condition code check.

\begin{table}[h]
\centering
\begin{tabular}{ll}
  \hline
  \textbf{CCKNOWPASS} & \textbf{Meaning}                                \\
  \hline
  \texttt{0b0}     & The instruction was unconditional, or was    \\
                   & conditional and passed its condition code  \\
                   & check.                                      \\
  \texttt{0b1}     & The instruction was conditional, and might   \\
                   & have failed its condition code check.       \\
  \hline
\end{tabular}
\end{table}

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{Bits [18:0]}

Reserved, \texttt{RES0}.

'Traps to Hyp mode of Non-secure EL1 execution of SMC instructions' describes the configuration settings for this trap, for instructions executed in Non-secure EL1.

\textbf{ISS encoding for Exception from a Prefetch Abort}

\begin{table}[h]
\centering
\begin{tabular}{cccccccccccccccc}
  \hline
  \texttt{24} & \texttt{23} & \texttt{22} & \texttt{21} & \texttt{20} & \texttt{19} & \texttt{18} & \texttt{17} & \texttt{16} & \texttt{15} & \texttt{14} & \texttt{13} & \texttt{12} & \texttt{11} & \texttt{10} & \texttt{9} & \texttt{8} & \texttt{7} & \texttt{6} & \texttt{5} & \texttt{4} & \texttt{3} & \texttt{2} & \texttt{1} & \texttt{0} \\
  \hline
  \texttt{RES0} & \texttt{FnVEA} & \texttt{RES0} & \texttt{S1PTW} & \texttt{RES0} & \texttt{IFSC}  \\
  \hline
\end{tabular}
\end{table}

\textbf{Bits [24:11]}

Reserved, \texttt{RES0}.
FnV, bit [10]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>HIFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>HIFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is valid only if the IFSC code is 0b010000. It is RES0 for all other aborts.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EA, bit [9]

External abort type. This bit can provide an IMPLEMENTATION DEFINED classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [8]

Reserved, RES0.

S1PTW, bit [7]

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [6]

Reserved, RES0.

IFSC, bits [5:0]

Instruction Fault Status Code. Possible values of this field are:
For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Long-descriptor translation table lookup'.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following sections describe cases where Prefetch Abort exceptions can be routed to Hyp mode, generating exceptions that are reported in the HSR with EC value 0b100000:

- 'Abort exceptions, when the value of HCR.TGE is 1'.
- 'Routing debug exceptions to EL2 using AArch32'.

**ISS encoding for Exception from an Illegal state or PC alignment fault**

<table>
<thead>
<tr>
<th>Bits [24:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

Reserved, RES0.

For more information about the Illegal state exception, see:
• 'Illegal changes to PSTATE.M'.
• 'Illegal return events from AArch32 state'.
• 'Legal returns that set PSTATE.IL to 1'.
• 'The Illegal Execution state exception'.

For more information about the PC alignment fault exception, see 'Branching to an unaligned PC'.

### ISS encoding for Exception from a Data Abort

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>24</td>
<td>Instruction Syndrome Valid (ISV)</td>
</tr>
<tr>
<td>23-22</td>
<td>Syndrome Access Size (SAS)</td>
</tr>
<tr>
<td>19-18</td>
<td>Access Size (SSE)</td>
</tr>
<tr>
<td>15-14</td>
<td>Reservation (RES0)</td>
</tr>
<tr>
<td>13</td>
<td>Return Size (SRT)</td>
</tr>
<tr>
<td>12</td>
<td>Return Address (RES0AR)</td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
</tbody>
</table>

#### ISV, bit [24]

Instruction syndrome valid. Indicates whether the syndrome information in ISS[23:14] is valid.

<table>
<thead>
<tr>
<th>ISV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No valid instruction syndrome. ISS[23:14] are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>ISS[23:14] hold a valid instruction syndrome.</td>
</tr>
</tbody>
</table>

This bit is 0 for all faults except Data Aborts generated by stage 2 address translations for which all the following apply to the instruction that generated the Data Abort exception:

- The instruction is an LDR, LDA, LDRT, LDRSH, LDRSHT, LDRH, LDAH, LDRHT, LDRSB, LDRSBT, LDRB, LDB, LDBRT, STR, STL, STRT, STRH, STLB, STRH, STR, or STRBT instruction.
- The instruction is not performing register writeback.
- The instruction is not using the PC as a source or destination register.

For these cases, ISV is UNKNOWN if the exception was generated in Debug state in memory access mode, as described in 'Data Aborts in Memory access mode', and otherwise indicates whether ISS[23:14] hold a valid syndrome.

#### Note

In the A32 instruction set, LDR*T and STR*T instructions always perform register writeback and therefore never return a valid instruction syndrome.

When FEAT_RAS is implemented, ISV is 0 for any synchronous External abort.

ISV is set to 0 on a stage 2 abort on a stage 1 translation table walk.

When FEAT_RAS is not implemented, it is IMPLEMENTATION DEFINED whether ISV is set to 1 or 0 on a synchronous External abort on a stage 2 translation table walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

#### SAS, bits [23:22]

Syndrome Access Size. When ISV is 1, indicates the size of the access attempted by the faulting operation.

<table>
<thead>
<tr>
<th>SAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Byte</td>
</tr>
<tr>
<td>0b01</td>
<td>Halfword</td>
</tr>
<tr>
<td>0b10</td>
<td>Word</td>
</tr>
<tr>
<td>0b11</td>
<td>Doubleword</td>
</tr>
</tbody>
</table>

This field is UNKNOWN when the value of ISV is UNKNOWN.

This field is RES0 when the value of ISV is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**SSE, bit [21]**

Syndrome Sign Extend. When ISV is 1, for a byte, halfword, or word load operation, indicates whether the data item must be sign extended. For these cases, the possible values of this bit are:

<table>
<thead>
<tr>
<th>SSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sign-extension not required.</td>
</tr>
<tr>
<td>0b1</td>
<td>Data item must be sign-extended.</td>
</tr>
</tbody>
</table>

For all other operations this bit is 0.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

This field is **RES0** when the value of ISV is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [20]**

Reserved, **RES0**.

**SRT, bits [19:16]**

Syndrome Register transfer. When ISV is 1, the register number of the Rt operand of the faulting instruction.

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

This field is **RES0** when the value of ISV is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bit [15]**

Reserved, **RES0**.

**AR, bit [14]**

Acquire/Release. When ISV is 1, the possible values of this bit are:

<table>
<thead>
<tr>
<th>AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Instruction did not have acquire/release semantics.</td>
</tr>
<tr>
<td>0b1</td>
<td>Instruction did have acquire/release semantics.</td>
</tr>
</tbody>
</table>

This field is **UNKNOWN** when the value of ISV is **UNKNOWN**.

This field is **RES0** when the value of ISV is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [13:12]**

Reserved, **RES0**.

**AET, bits [11:10]**

*When FEAT_RAS is implemented:*

Asynchronous Error Type. When DFSC is 0b010001, describes the PE error state after taking the SError interrupt exception. The possible values of this field are:
### AET

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b00</th>
<th>0b01</th>
<th>0b10</th>
<th>0b11</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncontainable (UC).</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unrecoverable state (UEU)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Restartable state (UEO)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Recoverable state (UER)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

On a synchronous Data Abort, this field is `RES0`.

In the event of multiple errors taken as a single SError interrupt exception, the overall PE error state is reported.

**Note**

Software can use this information to determine what recovery might be possible. The recovery software must also examine any implemented fault records to determine the location and extent of the error.

When `FEAT_RAS` is not implemented, or when `DFSC` is not `0b010001`:

- Bit[11] is `RES0`.
- Bit[10] forms the FnV field.

**Note**

Armv8.2 requires the implementation of `FEAT_RAS`.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

### FnV

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>HDFAR is valid.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HDFAR is not valid, and holds an <code>UNKNOWN</code> value.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

When `FEAT_RAS` is not implemented, this field is valid only if `DFSC` is `0b010000`. It is `RES0` for all other aborts.

When `FEAT_RAS` is implemented:

- If `DFSC` is `0b010000`, this field is valid.
- If `DFSC` is `0b010001`, this bit forms part of the AET field, becoming AET[0].
- This field is `RES0` for all other aborts.

**Note**

Armv8.2 requires the implementation of `FEAT_RAS`.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

### EA, bit [9]

External abort type. This bit can provide an `IMPLEMENTATION DEFINED` classification of External aborts.

For any abort other than an External abort this bit returns a value of 0.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

### CM, bit [8]

Cache maintenance. For a synchronous fault, identifies fault that comes from a cache maintenance or address translation instruction. For synchronous faults, the possible values of this bit are:
<table>
<thead>
<tr>
<th>CM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not generated by a cache maintenance or address translation instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault generated by a cache maintenance or address translation instruction.</td>
</tr>
</tbody>
</table>

For an asynchronous Data Abort exception, this bit is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**S1PTW, bit [7]**

For a stage 2 fault, indicates whether the fault was a stage 2 fault on an access made for a stage 1 translation table walk:

<table>
<thead>
<tr>
<th>S1PTW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault not on a stage 2 translation for a stage 1 translation table walk.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault on the stage 2 translation of an access for a stage 1 translation table walk.</td>
</tr>
</tbody>
</table>

For any abort other than a stage 2 fault this bit is **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**WnR, bit [6]**

Write not Read. Indicates whether a synchronous abort was caused by a write instruction or a read instruction. The possible values of this bit are:

<table>
<thead>
<tr>
<th>WnR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Abort caused by a read instruction.</td>
</tr>
<tr>
<td>0b1</td>
<td>Abort caused by a write instruction.</td>
</tr>
</tbody>
</table>

For faults on cache maintenance and address translation instructions, this bit always returns a value of 1.

On an asynchronous Data Abort:

- When **FEAT_RAS** is not implemented, this bit is **UNKNOWN**.
- When **FEAT_RAS** is implemented, this bit is **RES0**.

**Note**

Armv8.2 requires the implementation of **FEAT_RAS**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DFSC, bits [5:0]**

Data Fault Status Code. Possible values of this field are:
<table>
<thead>
<tr>
<th>DFSC</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault in translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011001</td>
<td>Asynchronous SError interrupt, from a parity or ECC error on memory access.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b100001</td>
<td>Alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b110100</td>
<td>IMPLEMENTATION DEFINED fault (Lockdown).</td>
<td></td>
</tr>
<tr>
<td>0b110101</td>
<td>IMPLEMENTATION DEFINED fault (Unsupported Exclusive access).</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults on a Long-descriptor translation table lookup’.

If the S1PTW bit is set, then the level refers the level of the stage2 translation that is translating a stage 1 translation walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The following describe cases where Data Abort exceptions can be routed to Hyp mode, generating exceptions that are reported in the HSR with EC value 0b100000:

- ‘Abort exceptions, when the value of HCR.TGE is 1’.
- ‘Routing debug exceptions to EL2 using AArch32’.

The following describe cases that can cause a Data Abort exception that is taken to Hyp mode, and reported in the HSR with EC value of 0b100000 or 0b100100:
Accessing the HSR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, \{#\}<\text{CRm}>, \{#\}<\text{opc2}> \\
\text{MCR}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, \{#\}<\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HSR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HSR;

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HSR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HSR = R[t];
HSTR, Hyp System Trap Register

The HSTR characteristics are:

**Purpose**

Controls trapping to Hyp mode of Non-secure accesses, at EL1 or lower, to System registers in the coproc == 0b1111 encoding space:

- By the CRn value used to access the register using MCR or MRC instruction.
- By the CRm value used to access the register using MCRR or MRRC instruction.

**Configuration**

AArch32 System register HSTR bits [31:0] are architecturally mapped to AArch64 System register HSTR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HSTR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HSTR is a 32-bit register.

**Field descriptions**

The HSTR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>T15</td>
<td>RES0</td>
<td>T13</td>
<td>T12</td>
<td>T11</td>
<td>T10</td>
<td>T9</td>
<td>T8</td>
<td>T7</td>
<td>T6</td>
<td>T5</td>
<td>RES0</td>
<td>T3</td>
<td>T2</td>
<td>T1</td>
<td>T0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16, 14, 4]**

Reserved, RES0.

**T<n>, bit [n], for n = 15, 13 to 5, 3 to 0**

The remaining fields control whether Non-secure EL0 and EL1 accesses, using MCR, MRC, MCRR, and MRRC instructions, to the System registers in the coproc == 0b1111 encoding space are trapped to Hyp mode:

<table>
<thead>
<tr>
<th>T&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on Non-secure EL0 or EL1 accesses to System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any Non-secure EL1 MCR or MRC access with coproc == 0b1111 and CRn == &lt;n&gt; is trapped to Hyp mode. A Non-secure EL0 MCR or MRC access with these values is trapped to Hyp mode only if the access is not UNDEFINED when the value of this field is 0. Any Non-secure EL1 MCRR or MRRC access with coproc == 0b1111 and CRm == &lt;n&gt; is trapped to Hyp mode. A Non-secure EL0 MCRR or MRRC access with these values is trapped to Hyp mode only if the access is not UNDEFINED when the value of this field is 0.</td>
</tr>
</tbody>
</table>

For example, when HSTR.T7 is 1, for instructions executed at Non-secure EL1:

- An MCR or MRC instruction with coproc set to 0b1111 and <CRn> set to c7 is trapped to Hyp mode.
- An MCRR or MRRC instruction with coproc set to 0b1111 and <CRm> set to c7 is trapped to Hyp mode.
On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Accessing the HSTR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HSTR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HSTR;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HSTR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HSTR = R[t];
```

---

HSTR, Hyp System Trap Register
HTCR, Hyp Translation Control Register

The HTCR characteristics are:

Purpose

The control register for stage 1 of the EL2 translation regime.

Note

This stage of translation always uses the Long-descriptor translation table format.

Configuration

AArch32 System register HTCR bits [31:0] are architecturally mapped to AArch64 System register TCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HTCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

Attributes

HTCR is a 32-bit register.

Field descriptions

The HTCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES1 | IMPLEMENTATION DEFINED | RES0 | HWU62 | HWU61 | HWU60 | HWU59 | HPD | RES1 | RES0 | RES0 | SH0 | ORGN0 | IRGN0 | RES0 | T0SZ |

Bit [31]

Reserved, RES1.

IMPLEMENTATION DEFINED, bit [30]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [29]

Reserved, RES0.

HWU62, bit [28]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry.
Meaning

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of HTCR.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of HTCR.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU61, bit [27]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of HTCR.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of HTCR.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU60, bit [26]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry.

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of HTCR.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of HTCR.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU59, bit [25]**
When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU59</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of HTCR.HPD is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of HTCR.HPD is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HPD, bit [24]

When FEAT_AA32HPD is implemented:

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, XNTable, and PXNTable, in the PL2 translation regime.

<table>
<thead>
<tr>
<th>HPD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are zero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Bit [23]

Reserved, RES1.

Bits [22:14]

Reserved, RES0.

SH0, bits [13:12]

Shareability attribute for memory associated with translation table walks using HTTBR.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**ORGN0, bits [11:10]**

Outer cacheability attribute for memory associated with translation table walks using HTTBR.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IRGN0, bits [9:8]**

Inner cacheability attribute for memory associated with translation table walks using HTTBR.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [7:3]**

Reserved, RES0.

**T0SZ, bits [2:0]**

The size offset of the memory region addressed by HTTBR. The region size is \(2^{32-\text{T0SZ}}\) bytes.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HTCR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{\text{<c>}\}\{\text{<q>}\} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HTCR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HTCR = R[t];
end if;

MCR{coproc}, {opc1}, {CRn}, {CRm}, {opc2}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HTCR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HTCR = R[t];
The HTPIDR characteristics are:

**Purpose**

Provides a location where software running in Hyp mode can store thread identifying information that is not visible to Non-secure software executing at EL0 or EL1, for hypervisor management purposes.

The PE makes no use of this register.

**Configuration**

AArch32 System register HTPIDR bits [31:0] are architecturally mapped to AArch64 System register `TPIDR_EL2[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HTPIDR are UNDEFINED.

If EL2 is not implemented, this register is `RES0` from EL3.

**Note**

The PE never updates this register.

**Attributes**

HTPIDR is a 32-bit register.

**Field descriptions**

The HTPIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Thread ID</td>
<td>0b1111</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>0b100</td>
</tr>
<tr>
<td>29</td>
<td></td>
<td>0b1101</td>
</tr>
<tr>
<td>28</td>
<td></td>
<td>0b0000</td>
</tr>
<tr>
<td>27</td>
<td></td>
<td>0b010</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the HTPIDR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{<coproc>}, \{#\text{<opc1>}, \text{<Rt>}, \text{<CRn>}, \text{<CRm>}, \{#\text{<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsf PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    if PSTATE.EL == EL2 then
        return HTPIDR;
elsf PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
elsf SCR.NS == '1' then
        HTPIDR = R[t];
    else
        HTPIDR = R[t];

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsf PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    if PSTATE.EL == EL2 then
        HTPIDR = R[t];
elsf PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
elsf SCR.NS == '1' then
        HTPIDR = R[t];
    else
        HTPIDR = R[t];
HTRFCR, Hyp Trace Filter Control Register

The HTRFCR characteristics are:

Purpose

Provides EL2 controls for Trace.

Configuration

AArch32 System register HTRFCR bits [31:0] are architecturally mapped to AArch64 System register TRFCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_TRF is implemented. Otherwise, direct accesses to HTRFCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from Monitor mode when SCR_NS == 1.

Attributes

HTRFCR is a 32-bit register.

Field descriptions

The HTRFCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>TS</td>
</tr>
<tr>
<td>29</td>
<td>RES0</td>
</tr>
<tr>
<td>28</td>
<td>CX</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>E2TRE</td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td>E0HTRE</td>
</tr>
</tbody>
</table>

Reserved, RES0.

TS, bits [6:5]

Timestamp Control. Controls which timebase is used for trace timestamps.

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>The timestamp is controlled by TRFCR.TS.</td>
</tr>
<tr>
<td>01</td>
<td>Virtual timestamp. The traced timestamp is the physical counter value minus the value of CNTVOFF.</td>
</tr>
<tr>
<td>11</td>
<td>Physical timestamp. The traced timestamp is the physical counter value.</td>
</tr>
</tbody>
</table>

When SelfHostedTraceEnabled() == FALSE, this field is ignored.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

Bit [4]

Reserved, RES0.

CX, bit [3]

VMID Trace Enable.
Meaning

<table>
<thead>
<tr>
<th>CX</th>
<th>0b0</th>
<th>VMID tracing is not allowed.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b1</td>
<td>VMID tracing is allowed.</td>
</tr>
</tbody>
</table>

When `SelfHostedTraceEnabled()` == FALSE, this field is ignored.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Bit [2]**

Reserved, RES0.

**E2TRE, bit [1]**

EL2 Trace Enable.

<table>
<thead>
<tr>
<th>E2TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tracing is prohibited at EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tracing is allowed at EL2.</td>
</tr>
</tbody>
</table>

When `SelfHostedTraceEnabled()` == FALSE, this field is ignored.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**E0HTRE, bit [0]**

EL0 Trace Enable.

<table>
<thead>
<tr>
<th>E0HTRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tracing is prohibited at EL0 when <code>HCR.TGE == 1</code>.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tracing is allowed at EL0 when <code>HCR.TGE == 1</code>.</td>
</tr>
</tbody>
</table>

This field is ignored if any of the following are true:

- The PE is in Secure state.
- `SelfHostedTraceEnabled()` == FALSE.
- `HCR.TGE == 0`.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

**Accessing the HTRFCR**

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>\}\{<q>\} \ <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    else
        return HTRFCR;
    end if
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HTRFCR;
    end if
else
    return HTRFCR;
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
else
  PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      end if;
    else
      AArch32.HTRFCR = R[t];
    end if;
  else
    HTRFCR = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HTRFCR = R[t];
  end if;
else
  HTRFCR = R[t];
end if;
The HTTBR characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 1 of an address translation in the EL2 translation regime, and other information for this translation regime.

**Configuration**

AArch32 System register HTTBR bits [47:1] are architecturally mapped to AArch64 System register TTBR0_EL2[47:1].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HTTBR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

HTTBR is a 64-bit register.

**Field descriptions**

The HTTBR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RESO</td>
</tr>
<tr>
<td>62</td>
<td>BADDR</td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
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<tr>
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<td>12</td>
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<tr>
<td>11</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
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<td>9</td>
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<td>8</td>
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<td>7</td>
<td></td>
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<tr>
<td>6</td>
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</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:48]**

Reserved, RES0.

**BADDR, bits [47:1]**

Translation table base address, bits[47:x]. Bits [x:1] are RES0, with the additional requirement that if bits[x:1] are not all zero, this is a misaligned translation table base address, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Register bits [x:1] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

x is determined from the value of HTCR.T0SZ as follows:

- If HTCR.T0SZ is 0 or 1, x = 5 - HTCR.T0SZ.
- If HTCR.T0SZ is greater than 1, x = 14 - HTCR.T0SZ.

If bits[47:40] of the translation table base address are not zero, an Address size fault is generated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**CnP, bit [0]**

When FEAT_TTCNP is implemented:

Common not Private. This bit indicates whether each entry that is pointed to by HTTBR is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of HTTBR.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table entries pointed to by HTTBR are permitted to differ from corresponding entries for HTTBR for other PEs in the Inner Shareable domain. This is not affected by the value of HTTBR.CnP on those other PEs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The translation table entries pointed to by HTTBR are the same as the translation table entries pointed to by HTTBR on every other PE in the Inner Shareable domain for which the value of HTTBR.CnP is 1.</td>
</tr>
</tbody>
</table>

**Note**

If the value of the HTTBR.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those HTTBRs do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are **CONSTRAINED UNPREDICTABLE**, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Accessing the HTTBR**

Accesses to this register use the following encodings:

**MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>**

```plaintext
<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0010</td>
<td>0b0100</td>
</tr>
</tbody>
</table>
```

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x04);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    return HTTBR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return HTTBR;
    end if;
```

**MCRR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>**

```plaintext
<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
</table>
```
if PSTATE.EL == EL0 then
   UNDEFINED;
elif PSTATE.EL == EL1 then
   if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
      AArch32.TakeHypTrapException(0x04);
   else
      UNDEFINED;
   endif
elsif PSTATE.EL == EL2 then
   HTTBR = R[t2]:R[t];
elif PSTATE.EL == EL3 then
   if SCR.NS == '0' then
      UNDEFINED;
   else
      HTTBR = R[t2]:R[t];
   endif
HVBAR, Hyp Vector Base Address Register

The HVBAR characteristics are:

**Purpose**

Holds the vector base address for any exception that is taken to Hyp mode.

**Configuration**

AArch32 System register HVBAR bits [31:0] are architecturally mapped to AArch64 System register `VBAR_EL2[31:0]`. This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to HVBAR are **UNDEFINED**.

If EL2 is not implemented, this register is `RES0` from EL3.

**Attributes**

HVBAR is a 32-bit register.

**Field descriptions**

The HVBAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-5</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>4-0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [31:5]**

Vector Base Address. Bits[31:5] of the base address of the exception vectors for exceptions taken to this Exception level. Bits[4:0] of an exception vector are the exception offset.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [4:0]**

Reserved, RES0.

**Accessing the HVBAR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return HVBAR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    return HVBAR;
endif

MCR{<c>{<q>}}<coproc>, {#}<opc1>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  HVBAR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    HVBAR = R[t];
endif
The ICC_AP0R<n> characteristics are:

Purpose

Provides information about Group 0 active priorities.

Configuration

AArch32 System register ICC_AP0R<n> bits [31:0] are architecturally mapped to AArch64 System register ICC_AP0R<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_AP0R<n> are(undefined).

Attributes

ICC_AP0R<n> is a 32-bit register.

Field descriptions

The ICC_AP0R<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

Accessing the ICC_AP0R<n>

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 0 active priorities) might result in UNPREDICTABLE behavior of the interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICC_AP0R1 is only implemented in implementations that support 6 or more bits of preemption. ICC_AP0R2 and ICC_AP0R3 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are UNDEFINED.

Note

The number of bits of preemption is indicated by ICH_VTR.PREbits.

Writing to the active priority registers in any order other than the following order will result in UNPREDICTABLE behavior:

- ICC_AP0R<n>.
- Secure ICC_AP1R<n>.
- Non-secure ICC_AP1R<n>.

Accesses to this register use the following encodings:

\[ \text{MRC\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>, \{#\}<opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  else
    return ICC_AP0R[UInt(opc2<1:0>)];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  else
    return ICC_AP0R[UInt(opc2<1:0>)];
  end if;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_AP0R[UInt(opc2<1:0>)];
  end if;
else
  return ICC_AP0R[UInt(opc2<1:0>)];
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b1:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elseif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elself Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
    UNDEFINED;
elself EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elself EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T12 == '1' then
      AArch32.TakeHypTrapException(0x03);
elself ICC_SRE.SRE == '0' then
    UNDEFINED;
elself ICC_SRE.SRE == '0' then
    else
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elself HaveEL(EL3) && ELUsingAAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elself ICC_HASRE.SRE == '0' then
    else
      ICC_AP0R[UInt(opc2<1:0>)] = R[t];
elself ICC_MSRE.SRE == '0' then
  else
    AArch32.TakeMonitorTrapException();
else
  ICC_AP0R[UInt(opc2<1:0>)] = R[t];
elself PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elself Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
elself ICC_HASRE.SRE == '0' then
  else
    ICC_AP0R[UInt(opc2<1:0>)] = R[t];
elself PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
elself ICC_AP0R[UInt(opc2<1:0>)] = R[t];
ICC_AP1R<n>, Interrupt Controller Active Priorities
Group 1 Registers, n = 0 - 3

The ICC_AP1R<n> characteristics are:

**Purpose**

Provides information about Group 1 active priorities.

**Configuration**

AArch32 System register ICC_AP1R<n> bits [31:0] (S) are architecturally mapped to AArch64 System register ICC_AP1R<n>_EL1[31:0] (S).

AArch32 System register ICC_AP1R<n> bits [31:0] (NS) are architecturally mapped to AArch64 System register ICC_AP1R<n>_EL1[31:0] (NS).

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_AP1R<n> are UNDEFINED.

**Attributes**

ICC_AP1R<n> is a 32-bit register.

**Field descriptions**

The ICC_AP1R<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICC_AP1R<n>**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 1 active priorities) might result in UNPREDICTABLE behavior of the interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICC_AP1R1 is only implemented in implementations that support 6 or more bits of preemption. ICC_AP1R2 and ICC_AP1R3 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are UNDEFINED.

**Note**

The number of bits of preemption is indicated by ICH_VTR.PREbits.
Writing to the active priority registers in any order other than the following order will result in **UNPREDICTABLE** behavior:

- ICC_AP0R<n>
- Secure ICC_AP1R<n>
- Non-secure ICC_AP1R<n>

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{ <coproc>, } \{#\text{<opc1>}, \text{<Rt>, } \text{<CRn>, } \text{<CRm>{, }(#\text{<opc2>}} \text{)}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR.IRQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR.IRQ == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif ICC_SRE.SRE == '0' then
  UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR.IMO == '1' then
  return ICV_APIR[UInt(opc2<1:0>)];
elsif ICC_HSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    elsif ICC_MSRE.SRE == '0' then
      return ICC_APIR_NS[UInt(opc2<1:0>)];
    else
      if SCR.NS == '0' then
        return ICC_APIR_S[UInt(opc2<1:0>)];
      else
        return ICC_APIR_NS[UInt(opc2<1:0>)];
      endif
    endif
  endif
endif
if PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR.IRQ == '1' then
    UNDEFINED;
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      return ICC_APIR_S[UInt(opc2<1:0>)];
    else
      return ICC_APIR_NS[UInt(opc2<1:0>)];
    endif
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    elsif ICC_MSRE.SRE == '0' then
      return ICC_APIR_NS[UInt(opc2<1:0>)];
    else
      if SCR.NS == '0' then
        return ICC_APIR_S[UInt(opc2<1:0>)];
      else
        return ICC_APIR_NS[UInt(opc2<1:0>)];
      endif
endif
if PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
elsif SCR.NS == '0' then
  return ICC_APIR_S[UInt(opc2<1:0>)];
else
  return ICC_APIR_NS[UInt(opc2<1:0>)];
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
elsif PSTATE.EL == EL3 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
elsif PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    else
        ICC_AP1R[UInt(opc2<1:0>)] = R[t];
    end if;
The ICC_ASGI1R characteristics are:

**Purpose**

Generates Group 1 SGIs for the Security state that is not the current Security state.

**Configuration**

AArch32 System register ICC_ASGI1R performs the same function as AArch64 System register ICC_ASGI1R_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_ASGI1R are UNDEFINED.

Under certain conditions a write to ICC_ASGI1R can generate Group 0 interrupts, see 'Forwarding an SGI to a target PE' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_ASGI1R is a 64-bit register.

**Field descriptions**

The ICC_ASGI1R bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| RES0   | Aff3   | RS     | RES0   | IRM    | Aff2   | TargetList |

**Bits [63:56]**

Reserved, RES0.

**Aff3, bits [55:48]**

The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**

RangeSelector

Controls which group of 16 values is represented by the TargetList field.

TargetList[n] represents aff0 value ((RS * 16) + n).

When ICC_CTLR_EL1.RSS==0, RS is RES0.

When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a CONSTRAINED UNPREDICTABLE choice of:

- The write is ignored.
- The RS field is treated as 0.
Bits [43:41]
Reserved, RES0.

IRM, bit [40]
Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1.&lt;target list&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding &quot;self&quot;.</td>
</tr>
</tbody>
</table>

Aff2, bits [39:32]
The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

Bits [31:28]
Reserved, RES0.

INTID, bits [27:24]
The INTID of the SGI.

Aff1, bits [23:16]
The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

TargetList, bits [15:0]
Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.
If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is IMPLEMENTATION DEFINED whether, in such cases, a Distributor can signal a system error.

Note
This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16. If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs.
Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.
If the IRM bit is 1, this field is RES0.

Accessing the ICC_ASGI1R
This register allows software executing in a Secure state to generate Non-secure Group 1 SGIs. It will also allow software executing in a Non-secure state to generate Secure Group 1 SGIs, if permitted by the settings of GICR_NSACR in the Redistributor corresponding to the target PE.

When GICD_CTLR.DS==0, Non-secure writes do not generate an interrupt for a target PE if not permitted by the GICR_NSACR register associated with the target PE. For more information, see 'Use of control registers for SGI.
forwarding’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**

Accesses from Secure Monitor mode are treated as Secure regardless of the value of SCR.NS.

Accesses to this register use the following encodings:

\[
\text{MCRR}\{\langle c \rangle\}\{\langle q \rangle\} \langle \text{coproc} \rangle, \{\#\}\langle \text{opc1} \rangle, \langle \text{Rt} \rangle, \langle \text{Rt2} \rangle, \langle \text{CRm} \rangle
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1100</td>
<td>0b0001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif ICC_SRE.SRE == '0' then
    ICC_ASGI1R = R[t2]:R[t];
elsif ICC_MSRE.SRE == '0' then
  UNDEFINED;
else
  ICC_ASGI1R = R[t2]:R[t];
endif
else
  ICC_ASGI1R = R[t2]:R[t];
endif
The ICC_BPR0 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 0 interrupt preemption.

**Configuration**

AArch32 System register ICC_BPR0 bits [31:0] are architecturally mapped to AArch64 System register ICC_BPR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_BPR0 are UNDEFINED.

**Attributes**

ICC_BPR0 is a 32-bit register.

**Field descriptions**

The ICC_BPR0 bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     | RES0 | BinaryPoint |

**Bits [31:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

The value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>[7:1]</td>
<td>[0]</td>
<td>gggggg.s</td>
</tr>
<tr>
<td>1</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>2</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>gggggg.sss</td>
</tr>
<tr>
<td>3</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>ggggg.ssss</td>
</tr>
<tr>
<td>4</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sssss</td>
</tr>
<tr>
<td>5</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>gg.ssssss</td>
</tr>
<tr>
<td>6</td>
<td>[7]</td>
<td>[6:0]</td>
<td>g.sssssss</td>
</tr>
<tr>
<td>7</td>
<td>No preemption</td>
<td>[7:0]</td>
<td>.ssssssss</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICC_BPR0**

The minimum binary point value is derived from the number of implemented priority bits. The number of priority bits is IMPLEMENTATION DEFINED, and reported by ICC_CTLR.PRIbits and ICC_MCTLR.PRIbits.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is set to the minimum supported value.
Accesses to this register use the following encodings:

\[ \text{MRC}\{c\}\{q\} \ <\text{coproc}>, \ \{\#\}<\text{opc1}>, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}>, \ \{\#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsi if PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elsi if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif ICC_BPR0 then
    return ICC_BPR0;
  else if Requirements not met then
    return ICC_BPR0;
  end if
end if

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_BPR0 = R[t];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_BPR0 = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_BPR0 = R[t];
  end if;
else
  ICC_BPR0 = R[t];
end if;
ICC_BPR1, Interrupt Controller Binary Point Register 1

The ICC_BPR1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption.

**Configuration**

AArch32 System register ICC_BPR1 bits [31:0] (S) are architecturally mapped to AArch64 System register ICC_BPR1_EL1[31:0] (S).

AArch32 System register ICC_BPR1 bits [31:0] (NS) are architecturally mapped to AArch64 System register ICC_BPR1_EL1[31:0] (NS).

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_BPR1 are UNDEFINED.

In GIC implementations supporting two Security states, this register is Banked.

**Attributes**

ICC_BPR1 is a 32-bit register.

**Field descriptions**

The ICC_BPR1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
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<td>RES0</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>BinaryPoint</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

If the GIC is configured to use separate binary point fields for Group 0 and Group 1 interrupts, the value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. For more information about priorities, see 'Priority grouping' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Writing 0 to this field will set this field to its reset value.

If EL3 is implemented and ICC_MCTLR_CBPRI_EL1S is 1:

- Accesses to this register at EL3 not in Monitor mode access the state of ICC_BPR0.
- When SCR_EL3.EEL2 is 1 and HCR_EL2.IMO is 1, Secure accesses to this register at EL1 access the state of ICC_BPR0.
- Otherwise, Secure accesses to this register at EL1 access the state of ICC_BPR0.

If EL3 is implemented and ICC_MCTLR_CBPRI_EL1NS is 1, Non-secure accesses to this register at EL1 or EL2 behave as follows, depending on the values of HCR.IMO and SCR.IRQ:
If EL3 is not implemented and ICC_CTLR.CBPR is 1, Non-secure accesses to this register at EL1 or EL2 behave as follows, depending on the values of HCR.IMO:

<table>
<thead>
<tr>
<th>HCR.IMO</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1 and EL2 reads return ICC_BPR0 + 1 saturated to 0b111. Non-secure EL1 and EL2 writes are ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses affect virtual interrupts. Non-secure EL2 reads return ICC_BPR0 + 1 saturated to 0b111. Non-secure EL2 writes ignored.</td>
</tr>
</tbody>
</table>

This field resets to an IMPLEMENTATION DEFINED non-zero value.

### Accessing the ICC_BPR1

When the PE resets into an Exception level that is using AArch32, the reset value is equal to:

- For the Secure copy of the register, the minimum value of ICC_BPR0 plus one.
- For the Non-secure copy of the register, the minimum value of ICC_BPR0.

Where the minimum value of ICC_BPR0 is IMPLEMENTATION DEFINED.

If EL3 is not implemented:

- If the PE is Secure this reset value is (minimum value of ICC_BPR0 plus one).
- If the PE is Non-secure this reset value is (minimum value of ICC_BPR0).

An attempt to program the binary point field to a value less than the reset value sets the field to the reset value.

Accesses to this register use the following encodings:

\[
\text{MRC\{}\langle c\rangle\text{\{}\langle q\rangle\text{\{}coproc\rangle, \{#\}\langle opc1\rangle, <Rt>, <CRn>, <CRm}\{, \{#\}\langle opc2\rangle\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elseif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      return ICC_BPR1_S;
    else
      return ICC_BPR1_NS;
  endif
else
  if SCR.NS == '0' then
    return ICC_BPR1_S;
  else
    return ICC_BPR1_NS;
endif
else
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    UNDEFINED;
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      return ICC_BPR1_S;
    else
      return ICC_BPR1_NS;
  endif
endif
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_TALL1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) then
        ICC_BPR1_NS = R[t];
    else
        ICC_BPR1 = R[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) then
        ICC_BPR1_NS = R[t];
    else
        ICC_BPR1 = R[t];
    end if
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            ICC_BPR1_S = R[t];
        else
            ICC_BPR1_NS = R[t];
        end if
The ICC_CTLR characteristics are:

**Purpose**

Controls aspects of the behavior of the GIC CPU interface and provides information about the features implemented.

**Configuration**

AArch32 System register ICC_CTLR bits [31:0] (S) are architecturally mapped to AArch64 System register ICC_CTLR_EL1[31:0] (S).

AArch32 System register ICC_CTLR bits [31:0] (NS) are architecturally mapped to AArch64 System register ICC_CTLR_EL1[31:0] (NS).

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_CTLR are UNDEFINED.

**Attributes**

ICC_CTLR is a 32-bit register.

**Field descriptions**

The ICC_CTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>ExtRange</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>RSS</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td>A3V</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>SEIS</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td>IDbits</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td>PRIbits</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>RES0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>PMHE</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>RES0</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>EOImode</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>CBPR</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td></td>
<td>1</td>
<td>Extended INTID range (read-only).</td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
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<tr>
<td>0</td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:20]**

Reserved, RES0.

**ExtRange, bit [19]**

Extended INTID range (read-only).

- **0b0**: CPU interface does not support INTIDs in the range 1024..8191. Behaviour is UNPREDICTABLE if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface.

  **Note**
  Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them.

- **0b1**: CPU interface supports INTIDs in the range 1024..8191. All INTIDs in the range 1024..8191 are treated as requiring deactivation.

If EL3 is implemented, ICC_CTLR_EL1.ExtRange is an alias of ICC_CTLR_EL3.ExtRange.

**RSS, bit [18]**

Range Selector Support. Possible values are:
### RSS

<table>
<thead>
<tr>
<th>RSS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 15 are supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 255 are supported.</td>
</tr>
</tbody>
</table>

This bit is read-only.

### Bits [17:16]

Reserved, RES0.

### A3V, bit [15]

Affinity 3 Valid. Read-only and writes are ignored. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and using AArch32, this bit is an alias of ICC_MCTLR.A3V.

If EL3 is implemented and using AArch64, this bit is an alias of ICC_CTLR_EL3.A3V.

### SEIS, bit [14]

SEI Support. Read-only and writes are ignored. Indicates whether the CPU interface supports local generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support local generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports local generation of SEIs.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and using AArch32, this bit is an alias of ICC_MCTLR.SEIS.

If EL3 is implemented and using AArch64, this bit is an alias of ICC_CTLR_EL3.SEIS.

### IDbits, bits [13:11]

Identifier bits. Read-only and writes are ignored. The number of physical interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b01</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If EL3 is implemented and using AArch32, this field is an alias of ICC_MCTLR.IDbits.

If EL3 is implemented and using AArch64, this field is an alias of ICC_CTLR_EL3.IDbits.

### PRIbits, bits [10:8]

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one.

An implementation that supports two Security states must implement at least 32 levels of physical priority (5 priority bits).

An implementation that supports only a single Security state must implement at least 16 levels of physical priority (4 priority bits).

---

**Note**
This field always returns the number of priority bits implemented, regardless of the Security state of the access or the value of GICD_CTLR.DS.

The division between group priority and subpriority is defined in the binary point registers ICC_BPR0 and ICC_BPR1.

If EL3 is implemented and using AArch32, physical accesses return the value from ICC_MCTLR.PRIbits.

If EL3 is implemented and using AArch64, physical accesses return the value from ICC_CTLR_EL3.PRIbits.

If EL3 is not implemented, physical accesses return the value from this field.

**Bit [7]**

Reserved, RES0.

**PMHE, bit [6]**

Priority Mask Hint Enable. Controls whether the priority mask register is used as a hint for interrupt distribution:

<table>
<thead>
<tr>
<th>PMHE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables use of ICC_PMR as a hint for interrupt distribution.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables use of ICC_PMR as a hint for interrupt distribution.</td>
</tr>
</tbody>
</table>

If EL3 is implemented:

- If EL3 is using AArch32, this bit is an alias of ICC_MCTLR.PMHE.
- If EL3 is using AArch64, this bit is an alias of ICC_CTLR_EL3.PMHE.
- If GICD_CTLR.DS == 0, this bit is read-only.
- If GICD_CTLR.DS == 1, this bit is read/write.

If EL3 is not implemented, it is **IMPLEMENTATION DEFINED** whether this bit is read-only or read-write:

- If this bit is read-only, an implementation can choose to make this field RAZ/WI or RAO/WI.
- If this bit is read/write, it resets to zero.

**Bits [5:2]**

Reserved, RES0.

**EOImode, bit [1]**

EOI mode for the current Security state. Controls whether a write to an End of Interrupt register also deactivates the interrupt:

<table>
<thead>
<tr>
<th>EOImode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide priority drop functionality only. ICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

If EL3 is implemented:

- If EL3 is using AArch32, this bit is an alias of ICC_MCTLR.EOImode_EL1{S, NS} where S or NS corresponds to the current Security state.
- If EL3 is using AArch64, this bit is an alias of ICC_CTLR_EL3.EOImode_EL1{S, NS} where S or NS corresponds to the current Security state.

If EL3 is not implemented, it is **IMPLEMENTATION DEFINED** whether this bit is read-only or read-write:

- If this bit is read-only, an implementation can choose to make this field RAZ/WI or RAO/WI.
- If this bit is read/write, it resets to zero.
**CBPR, bit [0]**

Common Binary Point Register. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_BPR0 determines the preemption group for Group 0 interrupts only. ICC_BPR1 determines the preemption group for Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_BPR0 determines the preemption group for both Group 0 and Group 1 interrupts.</td>
</tr>
</tbody>
</table>

If EL3 is implemented:

- If EL3 is using AArch32, this bit is an alias of ICC_MCTLR.CBPR_EL1{S,NS} where S or NS corresponds to the current Security state.
- If EL3 is using AArch64, this bit is an alias of ICC_CTLR_EL3.CBPR_EL1{S,NS} where S or NS corresponds to the current Security state.
- If GICD_CTLR.DS == 0, this bit is read-only.
- If GICD_CTLR.DS == 1, this bit is read/write.

If EL3 is not implemented, it is IMPLEMENTATION DEFINED whether this bit is read-only or read-write:

- If this bit is read-only, an implementation can choose to make this field RAZ/WI or RAO/WI.
- If this bit is read/write, it resets to zero.

**Accessing the ICC_CTLR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && !ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
else
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1":' && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
elsif ICC_MSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  end if;
elsif ICC_HSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeSystemAccessTrap(EL3, 0x03);
  end if;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  end if;
elsif ICC_CTBLR.SRE == '0' then
  UNDEFINED;
elsif ICC_CTBLR.SRE == '0' then
  UNDEFINED;
elsif ICC_CTBLR.SRE == '0' then
  UNDEFINED;
elsif SCR.NS == '0' then
  return ICC_CTBLR;
else
    return ICC_CTLR_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL3) & & ICH_HCR.TC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HCR_EL2.FMO == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HCR.FMO == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HCR.IMO == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HCR.IMO == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & & ELUsingAArch32(EL3) & & SCR_EL3.<IRQ,FIQ> == '11' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) & & ELUsingAArch32(EL3) & & SCR_EL3.<IRQ,FIQ> == '11' then
        AArch32.TakeSystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) & & ELUsingAArch32(EL3) & & PSTATE.M != M32_Monitor & & SCR.<IRQ,FIQ> == '11' then
        if Halted() & & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeSystemAccessTrap(EL3, 0x03);
        if HaveEL(EL3) & & ELUsingAArch32(EL3) & & SCR.<IRQ,FIQ> == '11' then
            if Halted() & & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeSystemAccessTrap(EL3, 0x03);
            ICC_CTLR = R[t];
        else
            ICC_CTLR = R[t];
        elsif ICC_HSRE.SRE == '0' then
            ICC_CTLR_S = R[t];
        else
            ICC_CTLR = R[t];
        elsif ICC_MSRE.SRE == '0' then
            ICC_CTLR_S = R[t];
        else
            ICC_CTLR = R[t];
else
  ICC_CTRLR_NS = R[t];
**ICC_DIR, Interrupt Controller Deactivate Interrupt Register**

The ICC_DIR characteristics are:

**Purpose**

When interrupt priority drop is separated from interrupt deactivation, a write to this register deactivates the specified interrupt.

**Configuration**

AArch32 System register ICC_DIR performs the same function as AArch64 System register ICC_DIR_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_DIR are UNDEFINED.

**Attributes**

ICC_DIR is a 32-bit register.

**Field descriptions**

The ICC_DIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>RES0</td>
</tr>
<tr>
<td>23-0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the interrupt to be deactivated.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_DIR**

There are two cases when writing to ICC_DIR_EL1 that were UNPREDICTABLE for a corresponding GICv2 write to GICC_DIR:

- When EOImode == 0. GICv3 implementations must ignore such writes. In systems supporting system error generation, an implementation might generate an SEI.
- When EOImode == 1 but no EOI has been issued. The interrupt will be de-activated by the Distributor; however the active priority in the CPU interface for the interrupt will remain set (because no EOI was issued).

Accesses to this register use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b100</td>
<td>0b101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    else
        ICC_DIR = R[t];
    endif
else
    ICC_DIR = R[t];
endif

if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        ICC_DIR = R[t];
    endif
else
    ICC_DIR = R[t];
endif

if PSTATE.EL == EL3 then
    if ICC_MSR.E = '0' then
        UNDEFINED;
    else
        ICC_DIR = R[t];
    endif
else
    ICC_DIR = R[t];
endif
ICC_EOIR0, Interrupt Controller End Of Interrupt Register 0

The ICC_EOIR0 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified Group 0 interrupt.

**Configuration**

AArch32 System register ICC_EOIR0 performs the same function as AArch64 System register ICC_EOIR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_EOIR0 are UNDEFINED.

**Attributes**

ICC_EOIR0 is a 32-bit register.

**Field descriptions**

The ICC_EOIR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|  RES0  |             | INTID |

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICC_IAR0 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the EOImode bit for the current Exception level and Security state is 0, a write to this register drops the priority for the interrupt, and also deactivates the interrupt.

If the EOImode bit for the current Exception level and Security state is 1, a write to this register only drops the priority for the interrupt. Software must write to ICC_DIR to deactivate the interrupt.

The appropriate EOImode bit varies as follows:

- If EL3 is not implemented, the appropriate bit is ICC_CTLR.EOImode.
- If EL3 is implemented and the software is executing in Monitor mode, the appropriate bit is ICC_MCTLR.EOImode_EL3.
- If EL3 is implemented and the software is not executing in Monitor mode, the bit depends on the current Security state:
  - If the software is executing in Secure state, the bit is ICC_CTLR.EOImode in the Secure instance of ICC_CTLR. This is an alias of ICC_MCTLR.EOImode_EL1S.
  - If the software is executing in Non-secure state, the bit is ICC_CTLR.EOImode in the Non-secure instance of ICC_CTLR. This is an alias of ICC_MCTLR.EOImode_EL1NS.
**Accessing the ICC_EOIR0**

A write to this register must correspond to the most recent valid read by this PE from an Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICC_IAR0, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

A write of a Special INTID is ignored. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Accesses to this register use the following encodings:

\[
\text{MCR\{<c>\}{<q>\} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
        UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
elif ICC_SRE.SRE == '0' then
    UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
        ICV_EOIR0 = R[t];
elif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        ICV_EOIR0 = R[t];
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif ICC_MSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
else
    ICC_EOIR0 = R[t];
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
elif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
else
    AArch32.TakeMonitorTrapException();
else
    ICC_EOIR0 = R[t];
elif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
elif ICC_EOIR0 == R[t];
The ICC_EOIR1 characteristics are:

**Purpose**
A PE writes to this register to inform the CPU interface that it has completed the processing of the specified Group 1 interrupt.

**Configuration**
AArch32 System register ICC_EOIR1 performs the same function as AArch64 System register ICC_EOIR1_EL1.
This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_EOIR1 are **UNDEFINED**.

**Attributes**
ICC_EOIR1 is a 32-bit register.

**Field descriptions**
The ICC_EOIR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>RES0</td>
</tr>
<tr>
<td>23-0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**
Reserved, RES0.

**INTID, bits [23:0]**
The INTID from the corresponding ICC_IAR1 access.
This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.
If the EOI mode bit for the current Exception level and Security state is 0, a write to this register drops the priority for the interrupt, and also deactivates the interrupt.
If the EOI mode bit for the current Exception level and Security state is 1, a write to this register only drops the priority for the interrupt. Software must write to ICC_DIR to deactivate the interrupt.

The appropriate EOI mode bit varies as follows:

- If EL3 is not implemented, the appropriate bit is ICC_CTLR.EOI mode.
- If EL3 is implemented and the software is executing in Monitor mode, the appropriate bit is ICC_MCTLR.EOI mode_EL3.
- If EL3 is implemented and the software is not executing in Monitor mode, the bit depends on the current Security state:
  - If the software is executing in Secure state, the bit is ICC_CTLR.EOI mode in the Secure instance of ICC_CTLR. This is an alias of ICC_MCTLR.EOI mode_EL1 S.
  - If the software is executing in Non-secure state, the bit is ICC_CTLR.EOI mode in the Non-secure instance of ICC_CTLR. This is an alias of ICC_MCTLR.EOI mode_EL1 NS.
Accessing the ICC_EOIR1

A write to this register must correspond to the most recent valid read by this PE from an Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICC_IAR1, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

A write of a Special INTID is ignored. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

Accesses to this register use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} <\text{coproc}, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#<\text{opc2}>\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
        ICC_EOIR1 = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        ICC_EOIR1 = R[t];
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
end
else
    ICC_EOIR1 = R[t];
end
elsif PSTATE_EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
end
else
    ICC_EOIR1 = R[t];
end
elsif PSTATE_EL == EL3 then
    if ICC_MSBRE.SRE == '0' then
        UNDEFINED;
    else
        ICC_EOIR1 = R[t];
end
ICC_HPPIR0, Interrupt Controller Highest Priority Pending Interrupt Register 0

The ICC_HPPIR0 characteristics are:

**Purpose**

Indicates the highest priority pending Group 0 interrupt on the CPU interface.

**Configuration**

AArch32 System register ICC_HPPIR0 performs the same function as AArch64 System register ICC_HPPIR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_HPPIR0 are **UNDEFINED**.

**Attributes**

ICC_HPPIR0 is a 32-bit register.

**Field descriptions**

The ICC_HPPIR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>23-0</td>
<td><strong>INTID</strong></td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, **RES0**.

**INTID, bits [23:0]**

The INTID of the highest priority pending interrupt, if that interrupt is observable at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are **RES0**.

**Accessing the ICC_HPPIR0**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>}, {#<opc1>, <CRn>, <CRm>{, {#<opc2>}}}
```

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
UNDEFINED;
elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.FIQ == '1' then
UNDEFINED;
elsif EL2Enabled() & !ELUsingAArch32(EL2) & & HSTR_EL2.T12 == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & & HSTR.T12 == '1' then
AArch32.TakeHypTrapException(0x03);
elsif ICC_SRE.SRE == '0' then
UNDEFINED;
elsif EL2Enabled() & !ELUsingAArch32(EL2) & ICH_HCR_EL2.TALL0 == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & ICH.TALL0 == '1' then
AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.FMO == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR.FMO == '1' then
return ICC_HPPIR0;
elsif ICC_HSRE.SRE == '0' then
UNDEFINED;
elsif ICC_MSRE.SRE == '0' then
UNDEFINED;
else
AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch32.TakeMonitorTrapException();
end if;
elsif ICC_MSRE.SRE == '0' then
UNDEFINED;
elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
if Halted() & EDSCR.SDD == '1' then
UNDEFINED;
else
AArch32.TakeMonitorTrapException();
end if;
else
return ICC_HPPIR0;
end if;
else
return ICC_HPPIR0;
end if;
elsif PSTATE.EL == EL3 then
if ICC_MSRE.SRE == '0' then
UNDEFINED;
else
return ICC_HPPIR0;
end if;
The ICC_HPPIR1 characteristics are:

**Purpose**

Indicates the highest priority pending Group 1 interrupt on the CPU interface.

**Configuration**

AArch32 System register ICC_HPPIR1 performs the same function as AArch64 System register ICC_HPPIR1_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_HPPIR1 are undefined.

**Attributes**

ICC_HPPIR1 is a 32-bit register.

**Field descriptions**

The ICC_HPPIR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending interrupt, if that interrupt is observable at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_HPPIR1**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#<opc1>}, <Rt>, <CRn>, <CRm>{, {#<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH.HCR.TALL1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif ICC_HPPR1 then
        ICC_HPPIR1, Interrupt Controller Highest Priority Pending Interrupt Register 1
    endif
else
    return ICC.HPPR1;
endif
else
    PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
            UNDEFINED;
        elsif ICC_HSRE.SRE == '0' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            endif
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            endif
        elseif ICC_HPPR1 then
            ICC_HPPIR1, Interrupt Controller Highest Priority Pending Interrupt Register 1
        endif
    endif
else
    PSTATE.EL == EL3 then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            return ICC.HPPR1;
        endif
else
    return ICC.HPPR1;
endif
The ICC_HSRE characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL2.

**Configuration**

AArch32 System register ICC_HSRE bits [31:0] are architecturally mapped to AArch64 System register ICC_SRE_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_HSRE are **UNDEFINED**.

**Attributes**

ICC_HSRE is a 32-bit register.

**Field descriptions**

The ICC_HSRE bit assignments are:

- **RES0**
  - Bits [31:4]: Reserved, RES0.
- **Enable**
  - **Meaning**
    - 0b0: Non-secure EL1 accesses to ICC_SRE trap to EL2.
    - 0b1: Non-secure EL1 accesses to ICC_SRE do not trap to EL2.
  
  If ICC_HSRE.SRE is RAO/WI, an implementation is permitted to make the Enable bit RAO/WI.
  
  If ICC_HSRE.SRE is 0, the Enable bit behaves as 1 for all purposes other than reading the value of the bit.
  
  On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
- **DIB**
  - **Meaning**
    - 0b0: IRQ bypass enabled.
    - 0b1: IRQ bypass disabled.
  
  If EL3 is implemented and GICD_CTLR.DS is 0, this field is a read-only alias of ICC_MSRE.DIB.
If EL3 is implemented and `GICD_CTLR.DS` is 1, this field is a read-write alias of `ICC_MSRE.DIB`. In systems that do not support IRQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

### DFB, bit [1]
Disabling FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and `GICD_CTLR.DS` is 0, this field is a read-only alias of `ICC_MSRE.DFB`. If EL3 is implemented and `GICD_CTLR.DS` is 1, this field is a read-write alias of `ICC_MSRE.DFB`. In systems that do not support FIQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

### SRE, bit [0]
System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used. Accesses at EL2 or below to any ICH_* System register, or any EL1 or EL2 ICC_* register other than <code>ICC_SRE</code> or ICC_HSRE, are UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface to the ICH_* registers and the EL1 and EL2 ICC_* registers is enabled for EL2.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0, the results are UNPREDICTABLE.

If an implementation supports only a System register interface to the GIC CPU interface, this bit is RAO/WI.

If EL3 is implemented and using AArch64:

- When `ICC_SRE_EL3.SRE==0` this bit is RAZ/WI.

If EL3 is implemented using AArch32:

- When `ICC_MSRE.SRE==0` this bit is RAZ/WI.

On a Warm reset, this field resets to 0.

### Accessing the ICC_HSRE
The GIC architecture permits, but does not require, that registers can be shared between memory-mapped registers and the equivalent System registers. This means that if the memory-mapped registers have been accessed while `ICC_HSRE.SRE==0`, then the System registers might be modified. Therefore, software must only rely on the reset values of the System registers if there has been no use of the GIC functionality while the memory-mapped registers are in use. Otherwise, the System register values must be treated as UNKNOWN.

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elseif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  else
    ICC_MSRE.Enable == '0' then
      UNDEFINED;
  else
    return ICC_HSRE;
elseif PSTATE.EL == EL3 then
  if !EL2Enabled() then
    UNDEFINED;
  else
    ICC_HSRE = R[t];
else
  ICC_HSRE = R[t];
The ICC_IAR0 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled Group 0 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch32 System register ICC_IAR0 performs the same function as AArch64 System register ICC_IAR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_IAR0 are UNDEFINED.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_IAR0 is a 32-bit register.

**Field descriptions**

The ICC_IAR0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
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<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>INTID</td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

This is the INTID of the highest priority pending interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. These special INTIDs can be one of: 1020, 1021, or 1023. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_IAR0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.FIQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & ICH_HCR.TALL0 == '1' then
        return ICC_IAR0;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        return ICC_IAR0;
    end if;
else
    ICC_IAR0;
end if;
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        return ICC_IAR0;
    end if;
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_IAR0;
    end if;
end if;
The ICC_IAR1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled Group 1 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch32 System register ICC_IAR1 performs the same function as AArch64 System register ICC_IAR1_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_IAR1 are **UNDEFINED**.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see ‘Observability of the effects of accesses to the GIC registers’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_IAR1 is a 32-bit register.

**Field descriptions**

The ICC_IAR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

This is the INTID of the highest priority pending interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged at the current Security state and Exception level.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICC_CTLR.IDbits and ICC_MCTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICC_IAR1**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
   priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
      UNDEFINED;
   elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap
   priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
      UNDEFINED;
   elseif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elseif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elseif ICC_SRE.SRE == '0' then
      UNDEFINED;
   elseif ICC_SRE.SRE == '0' then
      UNDEFINED;
   else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
   endif
   return ICC_IAR1;
elsif ICC_HSRE.SRE == '0' then
   UNDEFINED;
elsif ICC_MSRE.SRE == '0' then
   UNDEFINED;
else
   return ICC_IAR1;
endif
else
   return ICC_IAR1;
else
   if ICC_MSRE.SRE == '0' then
      UNDEFINED;
   else
      return ICC_IAR1;
elese
      return ICC_IAR1;
endif
The ICC_IGRPEN0 characteristics are:

**Purpose**

Controls whether Group 0 interrupts are enabled or not.

**Configuration**

AArch32 System register ICC_IGRPEN0 bits [31:0] are architecturally mapped to AArch64 System register ICC_IGRPEN0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_IGRPEN0 are **UNDEFINED**.

**Attributes**

ICC_IGRPEN0 is a 32-bit register.

**Field descriptions**

The ICC_IGRPEN0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>0b0</td>
<td>Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td>0b1</td>
<td>Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

Virtual accesses to this register update ICH_VMCR.VENG0.

On a Warm reset, this field resets to 0.

**Accessing the ICC_IGRPEN0**

The lowest Exception level at which this register can be accessed is governed by the Exception level to which FIQ is routed. This routing depends on SCR.FIQ, SCR.NS and HCR.FMO.

If an interrupt is pending within the CPU interface when Enable becomes 0, the interrupt must be released to allow the Distributor to forward the interrupt to a different PE.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
    return ICV_IGRPEN0;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
    return ICV_IGRPEN0;
else
  if HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
      if Halted() && EDSR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      else
        return ICC_IGRPEN0;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
      UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
      if Halted() && EDSR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      else
        return ICC_IGRPEN0;
  elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
      UNDEFINED;
    else
      return ICC_IGRPEN0;
  elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
      UNDEFINED;
    else
      return ICC_IGRPEN0;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        ICC_IGRPEN0 = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        ICC_IGRPEN0 = R[t];
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        ICC_IGRPEN0 = R[t];
    end if;
else PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        ICC_IGRPEN0 = R[t];
    end if;
else PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        ICC_IGRPEN0 = R[t];
    end if;
ICC_IGRPEN1, Interrupt Controller Interrupt Group 1 Enable register

The ICC_IGRPEN1 characteristics are:

**Purpose**

Controls whether Group 1 interrupts are enabled for the current Security state.

**Configuration**

AArch32 System register ICC_IGRPEN1 bits [31:0] (S) are architecturally mapped to AArch64 System register ICC_IGRPEN1_EL1[31:0] (S).

AArch32 System register ICC_IGRPEN1 bits [31:0] (NS) are architecturally mapped to AArch64 System register ICC_IGRPEN1_EL1[31:0] (NS).

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_IGRPEN1 are **UNDEFINED**.

**Attributes**

ICC_IGRPEN1 is a 32-bit register.

**Field descriptions**

The ICC_IGRPEN1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit No.</th>
<th>Field Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-30</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>29-21</td>
<td>Enable</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reserved, RES0.

**Enable, bit [0]**

Enables Group 1 interrupts for the current Security state.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupts are disabled</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupts are enabled</td>
</tr>
</tbody>
</table>

Virtual accesses to this register update ICH_VMCR.VENG1.

If EL3 is present:

- This bit is a read/write alias of ICC_MGRPEN1.EnableGrp1 {S, NS} as appropriate if EL3 is using AArch32, or ICC_IGRPEN1_EL3.EnableGrp1 {S, NS} as appropriate if EL3 is using AArch64.
- When this register is accessed at EL3, the copy of this register appropriate to the current setting of SCR.NS is accessed.

On a Warm reset, this field resets to 0.
**Accessing the ICC_IGRPEN1**

The lowest Exception level at which this register can be accessed is governed by the Exception level to which IRQ is routed. This routing depends on SCR.IRC, SCR.NS and HCR.IMO.

If an interrupt is pending within the CPU interface when Enable becomes 0, the interrupt must be released to allow the Distributor to forward the interrupt to a different PE.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
else
    return ICC_IGRPEN1_NS;
end
else
    if PSTATE_EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
            UNDEFINED;
        elsif ICC_HSRE.SRE == '0' then
            UNDEFINED;
        elsif ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    end
else
    if PSTATE_EL == EL3 then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            if SCR_NS == '0' then
                return ICC_IGRPEN1_S;
            else
                return ICC_IGRPEN1_NS;
            end
        end
    end
else
    if SCR_NS == '0' then
        return ICC_IGRPEN1_S;
    else
        return ICC_IGRPEN1_NS;
end

ICC_IGRPEN1, Interrupt Controller Interrupt Group 1 Enable register
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b11</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
else
    ICC_IGRPEN1 = R[t];
end if;
else
    ICC_IGRPEN1_NS = R[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
else
    ICC_IGRPEN1 = R[t];
elsif PSTATE.EL == EL3 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
else
    if SCR.NS == '0' then
        ICC_IGRPEN1_S = R[t];
    else
        ICC_IGRPEN1_NS = R[t];
    endif
endif
The ICC_MCTLR characteristics are:

**Purpose**

Controls aspects of the behavior of the GIC CPU interface and provides information about the features implemented.

**Configuration**

AArch32 System register ICC_MCTLR bits [31:0] can be mapped to AArch64 System register ICC_CTLR_EL3[31:0], but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_MCTLR are UNDEFINED.

**Attributes**

ICC_MCTLR is a 32-bit register.

**Field descriptions**

The ICC_MCTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved, UNDEFINED</td>
</tr>
<tr>
<td>30</td>
<td>ExtRange</td>
<td>Extended INTID range (read-only).</td>
</tr>
<tr>
<td>19</td>
<td>RSS</td>
<td>Range Selector Support. Possible values are:</td>
</tr>
<tr>
<td>18</td>
<td>nDS</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>A3V</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>SEIS</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>PRIbits</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>PMHE</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>RM</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>EOImode_EL1NS</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>EOImode_EL1S</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>EOImode_EL3</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>CBPR_EL1NS</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>CBPR_EL1S</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:20]**

Reserved, RES0.

**ExtRange, bit [19]**

Extended INTID range (read-only).

<table>
<thead>
<tr>
<th>ExtRange</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CPU interface does not support INTIDs in the range 1024..8191. Behavior is UNPREDICTABLE if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface.</td>
</tr>
<tr>
<td>0b1</td>
<td>CPU interface supports INTIDs in the range 1024..8191. All INTIDs in the range 1024..8191 are treated as requiring deactivation.</td>
</tr>
</tbody>
</table>

**Note**

Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them.

**RSS, bit [18]**

Range Selector Support. Possible values are:
Meaning

0b0 Targeted SGIs with affinity level 0 values of 0 - 15 are supported.
0b1 Targeted SGIs with affinity level 0 values of 0 - 255 are supported.

This bit is read-only.

**nDS, bit [17]**

Disable Security not supported. Read-only and writes are ignored.

<table>
<thead>
<tr>
<th>nDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic supports disabling of security.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic does not support disabling of security, and requires that security is not disabled.</td>
</tr>
</tbody>
</table>

**Bit [16]**

Reserved, RES0.

**A3V, bit [15]**

Affinity 3 Valid. Read-only and writes are ignored.

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support non-zero values of the Aff3 field in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports non-zero values of the Aff3 field in SGI generation System registers.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR.A3V is an alias of ICC_MCTLR.A3V.

**SEIS, bit [14]**

SEI Support. Read-only and writes are ignored. Indicates whether the CPU interface supports generation of SEIs.

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic does not support generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic supports generation of SEIs.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR.SEIS is an alias of ICC_MCTLR.SEIS.

**IDbits, bits [13:11]**

Identifier bits. Read-only and writes are ignored. Indicates the number of physical interrupt identifier bits supported.

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

If EL3 is present, ICC_CTLR.IDbits is an alias of ICC_MCTLR.IDbits.

**PRIbits, bits [10:8]**

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one.

An implementation that supports two Security states must implement at least 32 levels of physical priority (5 priority bits).

An implementation that supports only a single Security state must implement at least 16 levels of physical priority (4 priority bits).
Note

This field always returns the number of priority bits implemented, regardless of the value of SCR.NS or the value of GICD_CTRLR.DS.

The division between group priority and subpriority is defined in the binary point registers ICC_BPR0 and ICC_BPR1. This field determines the minimum value of ICC_BPR0.

**Bit [7]**

Reserved, RES0.

**PMHE, bit [6]**

Priority Mask Hint Enable.

<table>
<thead>
<tr>
<th>PMHE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disables use of the priority mask register as a hint for interrupt distribution.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enables use of the priority mask register as a hint for interrupt distribution.</td>
</tr>
</tbody>
</table>

Software must write ICC_PMR to 0xFF before clearing this field to 0.

An implementation might choose to make this field RAO/WI.

If EL3 is present, ICC_CTRLR.PMHE is an alias of ICC_MCTLR.PMHE.

On a Warm reset, this field resets to 0.

**RM, bit [5]**

SBZ.

The equivalent bit in AArch64 is the Routing Modifier bit. This feature is not supported when EL3 is using AArch32.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EOImode_EL1NS, bit [4]**

EOI mode for interrupts handled at Non-secure EL1 and EL2. Controls whether a write to an End of Interrupt register also deactivates the interrupt.

<table>
<thead>
<tr>
<th>EOImode_EL1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide priority drop functionality only. ICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTRLR(NS).EOImode is an alias of ICC_MCTLR.EOImode_EL1NS.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EOImode_EL1S, bit [3]**

EOI mode for interrupts handled at Secure EL1. Controls whether a write to an End of Interrupt register also deactivates the interrupt.
EOImode_EL1S | Meaning
---|---
0b0 | ICC_EOIR0 and ICC_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR are UNPREDICTABLE.
0b1 | ICC_EOIR0 and ICC_EOIR1 provide priority drop functionality only. ICC_DIR provides interrupt deactivation functionality.

If EL3 is present, ICC_CTLR(S).EOImode is an alias of ICC_MCTLR.EOImode_EL1S.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### EOImode_EL3, bit [2]

EOI mode for interrupts handled at EL3. Controls whether a write to an End of Interrupt register also deactivates the interrupt.

<table>
<thead>
<tr>
<th>EOImode_EL3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_EOIR0 and ICC_EOIR1 provide priority drop functionality only. ICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### CBPR_EL1NS, bit [1]

Common Binary Point Register, EL1 Non-secure. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 Non-secure interrupts at EL1 and EL2.

<table>
<thead>
<tr>
<th>CBPR_EL1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_BPR0 determines the preemption group for Group 0 interrupts only. ICC_BPR1 determines the preemption group for Non-secure Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_BPR0 determines the preemption group for Group 0 and Non-secure Group 1 interrupts. Non-secure accesses to GICC_BPR and ICC_BPR1 access the state of ICC_BPR0.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR(NS).CBPR is an alias of ICC_MCTLR.CBPR_EL1NS.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### CBPR_EL1S, bit [0]

Common Binary Point Register, EL1 Secure. Controls whether the same register is used for interrupt preemption of both Group 0 and Group 1 Secure interrupts in Secure non-Monitor modes.

<table>
<thead>
<tr>
<th>CBPR_EL1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICC_BPR0 determines the preemption group for Group 0 interrupts only. ICC_BPR1 determines the preemption group for Secure Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICC_BPR0 determines the preemption group for Group 0 interrupts and Secure Group 1 interrupts. Secure EL1 accesses, or EL3 accesses when not in Monitor mode, to ICC_BPR1 access the state of ICC_BPR0.</td>
</tr>
</tbody>
</table>

If EL3 is present, ICC_CTLR(S).CBPR is an alias of ICC_MCTLR.CBPR_EL1S.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the ICC_MCTLR

This register is only accessible when executing in Monitor mode.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
else
  PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_MCTLR;

\[
\text{MCR}\{<c>\}\{<q>\} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
else
  PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_MCTLR = R[t];
ICC_MGRPEN1, Interrupt Controller Monitor Interrupt Group 1 Enable register

The ICC_MGRPEN1 characteristics are:

**Purpose**

Controls whether Group 1 interrupts are enabled or not.

**Configuration**

AArch32 System register ICC_MGRPEN1 bits [31:0] can be mapped to AArch64 System register ICC_IGRPEN1_EL3[31:0], but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_MGRPEN1 are UNDEFINED.

**Attributes**

ICC_MGRPEN1 is a 32-bit register.

**Field descriptions**

The ICC_MGRPEN1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>EnableGrp1S</td>
<td>EnableGrp1NS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:2]**

Reserved, RES0.

**EnableGrp1S, bit [1]**

Enables Group 1 interrupts for the Secure state.

<table>
<thead>
<tr>
<th>EnableGrp1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

The Secure ICC_IGRPEN1.Enable bit is a read/write alias of the ICC_MGRPEN1.EnableGrp1S bit.

If the highest priority pending interrupt for that PE is a Group 1 interrupt using 1 of N model, then the interrupt will target another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.

**EnableGrp1NS, bit [0]**

Enables Group 1 interrupts for the Non-secure state.

<table>
<thead>
<tr>
<th>EnableGrp1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

The Non-secure ICC_IGRPEN1.Enable bit is a read/write alias of the ICC_MGRPEN1.EnableGrp1NS bit.
If the highest priority pending interrupt for that PE is a Group 1 interrupt using 1 of N model, then the interrupt will target another PE as a result of the Enable bit changing from 1 to 0.

On a Warm reset, this field resets to 0.

## Accessing the ICC_MGRPEN1

If an interrupt is pending within the CPU interface when an Enable bit becomes 0, the interrupt must be released to allow the Distributor to forward the interrupt to a different PE.

This register is only accessible when executing in Monitor mode.

Accesses to this register use the following encodings:

```
MRC<<q>> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_MGRPEN1;

MCR<<q>> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_MGRPEN1 = R[t];
ICC_MSRE, Interrupt Controller Monitor System Register Enable register

The ICC_MSRE characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL3.

**Configuration**

AArch32 System register ICC_MSRE bits [31:0] can be mapped to AArch64 System register ICC_SRE_EL3[31:0], but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_MSRE are UNDEFINED.

**Attributes**

ICC_MSRE is a 32-bit register.

**Field descriptions**

The ICC_MSRE bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:4]**

Reserved, RES0.

**Enable, bit [3]**

Enable. Enables lower Exception level access to ICC_SRE and ICC_HSRE.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure EL1 accesses to Secure ICC_SRE trap to EL3. EL2 accesses to Non-secure ICC_SRE and ICC_HSRE trap to EL3. Non-secure EL1 accesses to ICC_SRE trap to EL3, unless these accesses are trapped to EL2 as a result of ICC_HSRE.Enable == 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure EL1 accesses to Secure ICC_SRE do not trap to EL3. EL2 accesses to Non-secure ICC_SRE and ICC_HSRE do not trap to EL3. Non-secure EL1 accesses to ICC_SRE do not trap to EL3.</td>
</tr>
</tbody>
</table>

If ICC_MSRE.SRE is RAO/WI, an implementation is permitted to make the Enable bit RAO/WI.

If ICC_MSRE.SRE is 0, the Enable bit behaves as 1 for all purposes other than reading the value of the bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**DIB, bit [2]**

Disable IRQ bypass.

<table>
<thead>
<tr>
<th>DIB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>IRQ bypass disabled.</td>
</tr>
</tbody>
</table>

In systems that do not support IRQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

**DFB, bit [1]**

Disable FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

In systems that do not support FIQ bypass, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

**SRE, bit [0]**

System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used.</td>
</tr>
<tr>
<td></td>
<td>Accesses at EL3 or below to any ICH_* System</td>
</tr>
<tr>
<td></td>
<td>register, or any EL1, EL2, or EL3 ICC_*</td>
</tr>
<tr>
<td></td>
<td>register other than ICC_SRE, ICC_HSRE, or ICC_MSRE, are UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface to the ICH_*</td>
</tr>
<tr>
<td></td>
<td>registers and the EL1, EL2, and EL3 ICC_*</td>
</tr>
<tr>
<td></td>
<td>registers is enabled for EL3.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0, the results are UNPREDICTABLE.

If an implementation supports only a System register interface to the GIC CPU interface, this bit is RAO/WI.

On a Warm reset, this field resets to 0.

**Accessing the ICC_MSRE**

This register is always System register accessible.

The GIC architecture permits, but does not require, that registers can be shared between memory-mapped registers and the equivalent System registers. This means that if the memory-mapped registers have been accessed while ICC_MSRE.SRE==0, then the System registers might be modified. Therefore, software must only rely on the reset values of the System registers if there has been no use of the GIC functionality while the memory-mapped registers are in use. Otherwise, the System register values must be treated as UNKNOWN.

This register is only accessible when executing in Monitor mode.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  return ICC_MSRE;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b110</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' && CP15SDISABLE2 == HIGH then
    UNDEFINED;
  else
    ICC_MSRE = R[t];
**ICC_PMR, Interrupt Controller Interrupt Priority Mask Register**

The ICC_PMR characteristics are:

**Purpose**

Provides an interrupt priority filter. Only interrupts with a higher priority than the value in this register are signaled to the PE.

**Configuration**

AArch32 System register ICC_PMR bits [31:0] are architecturally mapped to AArch64 System register ICC_PMR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_PMR are undefined.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that writes to this register are self-synchronising. This ensures that no interrupts below the written PMR value will be taken after a write to this register is architecturally executed. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_PMR is a 32-bit register.

**Field descriptions**

The ICC_PMR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Implemented priority bits</th>
<th>Possible priority field values</th>
<th>Number of priority levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>[0]</td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>[31:1]</td>
<td>Priority</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The priority mask level for the CPU interface. If the priority of an interrupt is higher than the value indicated by this field, the interface signals the interrupt to the PE.

The possible priority field values are as follows:
Unimplemented priority bits are RAZ/WI.

On a Warm reset, this field resets to 0.

**Accessing the ICC_PMR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \ <\text{coproc}>, \ {#}<\text{opc}1>, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}>\{, \ {#}<\text{opc}2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b010</td>
<td>0b010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE_EL == EL0 then
    UNDEFINED;
elsif PSTATE_EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        return ICV_PMR;
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        return ICV_PMR;
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        return ICV_PMR;
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        return ICV_PMR;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_PMR;
    endif
elsif PSTATE_EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_PMR;
    endif
elsif PSTATE_EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_PMR;
    endif
else
    return ICC_PMR;
endif
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_CR.TC == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
    ICC_PMR = R[t];
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
    ICC_PMR = R[t];
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
    ICC_PMR = R[t];
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
    ICC_PMR = R[t];
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ICC_PMR = R[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  else
    ICC_PMR = R[t];
  end if
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICC_PMR = R[t];
  end if
else
  ICC_PMR = R[t];
The ICC_RPR characteristics are:

**Purpose**

Indicates the Running priority of the CPU interface.

**Configuration**

AArch32 System register ICC_RPR performs the same function as AArch64 System register ICC_RPR_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_RPR are **UNDEFINED**.

**Attributes**

ICC_RPR is a 32-bit register.

**Field descriptions**

The ICC_RPR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The current running priority on the CPU interface. This is the group priority of the current active interrupt.

The priority returned is the group priority as if the BPR for the current Exception level and Security state was set to the minimum value of BPR for the number of implemented priority bits.

**Note**

If 8 bits of priority are implemented the group priority is bits[7:1] of the priority.

**Accessing the ICC_RPR**

If there are no active interrupts on the CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

Software cannot determine the number of implemented priority bits from a read of this register.

Accesses to this register use the following encodings:
MRC{{c}{q}} {coproc}, {#}<{opc1}, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        return ICC_RPR;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        return ICC_RPR;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        return ICC_RPR;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        return ICC_RPR;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_RPR;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_RPR;
    endif
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_RPR;
    endif
else
    return ICC_RPR;
end if

ICC_RPR, Interrupt Controller Running Priority Register
The ICC_SGI0R characteristics are:

**Purpose**
Generates Secure Group 0 SGIs.

**Configuration**
AArch32 System register ICC_SGI0R performs the same function as AArch64 System register ICC_SGI0R_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_SGI0R are UNDEFINED.

**Attributes**
ICC_SGI0R is a 64-bit register.

**Field descriptions**
The ICC_SGI0R bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
<td>0</td>
</tr>
<tr>
<td>62</td>
<td>Affinity 3 (Aff3)</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>RangeSelector (RS)</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td>Reserved, RES0</td>
<td>0</td>
</tr>
<tr>
<td>59</td>
<td>IRM</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td>Affinity 2 (Aff2)</td>
<td></td>
</tr>
<tr>
<td>57</td>
<td>TargetList</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td>Reserved, RES0</td>
<td>0</td>
</tr>
<tr>
<td>55</td>
<td>INTID</td>
<td></td>
</tr>
<tr>
<td>54</td>
<td>Reserved, RES0</td>
<td>0</td>
</tr>
<tr>
<td>53</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td>Reserved</td>
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<td>49</td>
<td>Reserved</td>
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<tr>
<td>48</td>
<td>Reserved</td>
<td></td>
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<tr>
<td>47</td>
<td>Reserved</td>
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<td>46</td>
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<td>43</td>
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<tr>
<td>42</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>40</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>39</td>
<td>Reserved</td>
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<td>38</td>
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<tr>
<td>37</td>
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<tr>
<td>36</td>
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</tr>
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<td>35</td>
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<td>34</td>
<td>Reserved</td>
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</tr>
<tr>
<td>33</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:56]**
Reserved, RES0.

**Aff3, bits [55:48]**
The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**
RangeSelector
Controls which group of 16 values is represented by the TargetList field.
TargetList[n] represents aff0 value ((RS * 16) + n).
When ICC_CTLR_EL1.RSS==0, RS is RES0.
When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a CONSTRAINED UNPREDICTABLE choice of:

- The write is ignored.
- The RS field is treated as 0.
Bits [43:41]
Reserved, RES0.

IRM, bit [40]
Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1.&lt;target list&gt;</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding &quot;self&quot;</td>
</tr>
</tbody>
</table>

Aff2, bits [39:32]
The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

Bits [31:28]
Reserved, RES0.

INTID, bits [27:24]
The INTID of the SGI.

Aff1, bits [23:16]
The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.
If the IRM bit is 1, this field is RES0.

TargetList, bits [15:0]
Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.
If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is IMPLEMENTATION DEFINED whether, in such cases, a Distributor can signal a system error.

Note
This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16. If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs. Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.
If the IRM bit is 1, this field is RES0.

Accessing the ICC_SGI0R
This register allows software executing in a Secure state to generate Group 0 SGIs. It will also allow software executing in a Non-secure state to generate Group 0 SGIs, if permitted by the settings of GICR_NSACR in the Redistributor corresponding to the target PE.

When GICD_CTLR.DS==0, Non-secure writes do not generate an interrupt for a target PE if not permitted by the GICR_NSACR register associated with the target PE. For more information, see 'Use of control registers for SGI
forwarding' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**

Accesses from Secure Monitor mode are treated as Secure regardless of the value of SCR.NS.

Accesses to this register use the following encodings:

\[ \text{MCRR}\{<c>\}{<q>} \{<coproc>, \{#<opc1>, <Rt>, <Rt2>, <CRm> \}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1100</td>
<td>0b0010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
elsif ICC_SGI0R = R[t2]:R[t];
elsif ICC_HSRE.SRE == '0' then
  UNDEFINED;
else
  AArch32.TakeMonitorTrapException();
else
 ICC_SGI0R = R[t2]:R[t];
elsif ICC_MSRE.SRE == '0' then
  UNDEFINED;
else
  AArch32.TakeMonitorTrapException();
else
  ICC_SGI0R = R[t2]:R[t];
elsif ICC_MSRE.SRE == '0' then
  UNDEFINED;
else
  ICC_SGI0R = R[t2]:R[t];
The ICC_SGI1R characteristics are:

**Purpose**

Generates Group 1 SGIs for the current Security state.

**Configuration**

AArch32 System register ICC_SGI1R performs the same function as AArch64 System register ICC_SGI1R_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_SGI1R are UNDEFINED.

Under certain conditions a write to ICC_SGI1R can generate Group 0 interrupts, see ‘Forwarding an SGI to a target PE’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICC_SGI1R is a 64-bit register.

**Field descriptions**

The ICC_SGI1R bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>62</td>
<td>Aff3</td>
</tr>
<tr>
<td>61</td>
<td>RS</td>
</tr>
<tr>
<td>60</td>
<td>TargetList</td>
</tr>
<tr>
<td>59</td>
<td>RES0</td>
</tr>
<tr>
<td>58</td>
<td>INTID</td>
</tr>
<tr>
<td>57</td>
<td>Aff1</td>
</tr>
<tr>
<td>56</td>
<td>RES0</td>
</tr>
<tr>
<td>55</td>
<td>IRM</td>
</tr>
<tr>
<td>54</td>
<td>Aff2</td>
</tr>
<tr>
<td>53</td>
<td></td>
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<td>36</td>
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<tr>
<td>34</td>
<td></td>
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<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:56]**

Reserved, RES0.

**Aff3, bits [55:48]**

The affinity 3 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**RS, bits [47:44]**

RangeSelector

Controls which group of 16 values is represented by the TargetList field.

TargetList[n] represents aff0 value ((RS * 16) + n).

When ICC_CTLR_EL1.RSS==0, RS is RES0.

When ICC_CTLR_EL1.RSS==1 and GICD_TYPER.RSS==0, writing this register with RS != 0 is a CONSTRAINED UNPREDICTABLE choice of:

- The write is ignored.
- The RS field is treated as 0.
**Bits [43:41]**

Reserved, RES0.

**IRM, bit [40]**

Interrupt Routing Mode. Determines how the generated interrupts are distributed to PEs. Possible values are:

<table>
<thead>
<tr>
<th>IRM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PEs specified by Aff3.Aff2.Aff1.&lt;target list&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to all PEs in the system, excluding &quot;self&quot;.</td>
</tr>
</tbody>
</table>

**Aff2, bits [39:32]**

The affinity 2 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**Bits [31:28]**

Reserved, RES0.

**INTID, bits [27:24]**

The INTID of the SGI.

**Aff1, bits [23:16]**

The affinity 1 value of the affinity path of the cluster for which SGI interrupts will be generated.

If the IRM bit is 1, this field is RES0.

**TargetList, bits [15:0]**

Target List. The set of PEs for which SGI interrupts will be generated. Each bit corresponds to the PE within a cluster with an Affinity 0 value equal to the bit number.

If a bit is 1 and the bit does not correspond to a valid target PE, the bit must be ignored by the Distributor. It is **IMPLEMENTATION DEFINED** whether, in such cases, a Distributor can signal a system error. 

**Note**

This restricts a system to sending targeted SGIs to PEs with an affinity 0 number that is less than 16. If SRE is set only for Secure EL3, software executing at EL3 might use the System register interface to generate SGIs. Therefore, the Distributor must always be able to receive and acknowledge Generate SGI packets received from CPU interface regardless of the ARE settings for a Security state. However, the Distributor might discard such packets.

If the IRM bit is 1, this field is RES0.

**Accessing the ICC_SGI1R**

**Note**

Accesses from Secure Monitor mode are treated as Secure regardless of the value of SCR.NS.
Accesses to this register use the following encodings:

\[
\text{MCRR}\{c\}\{q\} \text{ <coproc>, \{#\}<opc1>, <Rt>, <Rt2>, <CRm>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1100</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elskill PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
elskill Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
elskill EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elskill EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
            AArch32.TakeHypTrapException(0x03);
elskill ICC_SRE.SRE == '0' then
    UNDEFINED;
elskill EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elskill EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TC == '1' then
            AArch32.TakeHypTrapException(0x03);
elskill EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elskill EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elskill ICC_HSRE.SRE == '0' then
    UNDEFINED;
elskill ICC_SGI1R = R[t2]:R[t];
elskill ICC_SGI1R, Interrupt Controller Software Generated Interrupt Group 1 Register
else
    ICC_SGIIR = R[t2]:R[t];
elskill PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
elskill Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
elskill ICC_MSRE.SRE == '0' then
    UNDEFINED;
elskill HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elskill HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elskill ICC_SGIIR = R[t2]:R[t];
elskill ICC_SGIIR = R[t2]:R[t];
elskill PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
elskill ICC_SGIIR = R[t2]:R[t];
ICC_SRE, Interrupt Controller System Register Enable register

The ICC_SRE characteristics are:

**Purpose**

Controls whether the System register interface or the memory-mapped interface to the GIC CPU interface is used for EL0 and EL1.

**Configuration**

AArch32 System register ICC_SRE bits [31:0] (S) are architecturally mapped to AArch64 System register ICC_SRE_EL1[31:0] (S).

AArch32 System register ICC_SRE bits [31:0] (NS) are architecturally mapped to AArch64 System register ICC_SRE_EL1[31:0] (NS).

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICC_SRE are UNDEFINED.

**Attributes**

ICC_SRE is a 32-bit register.

**Field descriptions**

The ICC_SRE bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>DIB</td>
</tr>
<tr>
<td>29</td>
<td>DFBSRE</td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
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<tr>
<td>26</td>
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<tr>
<td>3</td>
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<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Reserved, RES0.

**DIB, bit [2]**

Disable IRQ bypass.

If EL3 is implemented and GICD_CTLR.DS == 0, this field is a read-only alias of ICC_MSRE.DIB.

If EL3 is implemented and GICD_CTLR.DS == 1, and EL2 is not implemented, this field is a read-write alias of ICC_MSRE.DIB.

If EL3 is not implemented and EL2 is implemented, this field is a read-only alias of ICC_HSRE.DIB.

If GICD_CTLR.DS == 1 and EL2 is implemented, this field is a read-only alias of ICC_HSRE.DIB.

In systems that do not support IRQ bypass, this field is RAO/WI.

On a Warm reset, this field resets to 0.
DFB, bit [1]

Disable FIQ bypass.

<table>
<thead>
<tr>
<th>DFB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQ bypass enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQ bypass disabled.</td>
</tr>
</tbody>
</table>

If EL3 is implemented and `GICD_CTLR.DS == 0`, this field is a read-only alias of `ICC_MSRE.DFB`.

If EL3 is implemented and `GICD_CTLR.DS == 1`, and EL2 is not implemented, this field is a read-write alias of `ICC_MSRE.DFB`.

If EL3 is not implemented and EL2 is implemented, this field is a read-only alias of `ICC_HSRE.DFB`.

If EL3 is not implemented and EL2 is implemented, this field is a read-only alias of `ICC_HSRE.DFB`.

In systems that do not support FIQ bypass, this field is RAO/WI.

On a Warm reset, this field resets to 0.

SRE, bit [0]

System Register Enable.

<table>
<thead>
<tr>
<th>SRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The memory-mapped interface must be used. Accesses at EL1 to any ICC_* System register other than ICC_SRE are UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>The System register interface for the current Security state is enabled.</td>
</tr>
</tbody>
</table>

If software changes this bit from 1 to 0 in the Secure instance of this register, the results are UNPREDICTABLE.

If an implementation supports only a System register interface to the GIC CPU interface, this bit is RAO/WI.

If EL3 is implemented and using AArch64:

- When `ICC_SRE_EL3.SRE==0` the Secure copy of this bit is RAZ/WI.
- When `ICC_SRE_EL3.SRE==0` the Non-secure copy of this bit is RAZ/WI.

If EL3 is implemented and using AArch32:

- When `ICC_MSRE.SRE==0` the Secure copy of this bit is RAZ/WI.
- When `ICC_MSRE.SRE==0` the Non-secure copy of this bit is RAZ/WI.

If EL2 is implemented and using AArch64:

- When `ICC_SRE_EL2.SRE==0` the Non-secure copy of this bit is RAZ/WI.

If EL2 is implemented and using AArch32:

- When `ICC_HSRE.SRE==0` the Non-secure copy of this bit is RAZ/WI.

On a Warm reset, this field resets to 0.

Accessing the ICC_SRE

The GIC architecture permits, but does not require, that registers can be shared between memory-mapped registers and the equivalent System registers. This means that if the memory-mapped registers have been accessed while ICC_SRE.SRE==0, then the System registers might be modified. Therefore, software must only rely on the reset values of the System registers if there has been no use of the GIC functionality while the memory-mapped registers are in use. Otherwise, the System register values must be treated as UNKNOWN.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  elsif ICC_MSRE.Enable == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) then
    if SCR_EL3.NS == '0' then
      return ICC_SRE_S;
    else
      return ICC_SRE_NS;
    end if;
  else
    return ICC_SRE;
  end if;
elsif PSTATE.EL == EL3 then
  if SCR_EL3.NS == '0' then
    return ICC_SRE_S;
  else
    return ICC_SRE_NS;
end if;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1''" && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && ICC_SRE_EL3.Enable == '0' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif ICC_MSRE.Enable == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) then
        if SCR_EL3.NS == '0' then
            ICC_SRE_S = R[t];
        else
            ICC_SRE_NS = R[t];
        end if;
    else
        ICC_SRE = R[t];
    end if;
else
    ICC_SRE_NS = R[t];
elsif PSTATE.EL == EL3 then
    if SCR_EL3.NS == '0' then
        ICC_SRE_S = R[t];
    else
        ICC_SRE_NS = R[t];
    end if;
else
    ICC_SRE_NS = R[t];
end if;
The ICH_AP0R<n> characteristics are:

**Purpose**

Provides information about Group 0 active priorities for EL2.

**Configuration**

AArch32 System register ICH_AP0R<n> bits [31:0] are architecturally mapped to AArch64 System register ICH_AP0R<n>_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_AP0R<n> are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

ICH_AP0R<n> is a 32-bit register.

**Field descriptions**

The ICH_AP0R<n> bit assignments are:

\[
\begin{array}{cccccccccccccccccccccc}
\end{array}
\]

**P<x>, bit \([x]\), for \(x = 31 \text{ to } 0\)**

Provides the access to the virtual active priorities for Group 0 interrupts. Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no Group 0 interrupt active at the priority corresponding to that bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>There is a Group 0 interrupt active at the priority corresponding to that bit.</td>
</tr>
</tbody>
</table>

The correspondence between priority levels and bits depends on the number of bits of priority that are implemented.

If 5 bits of preemption are implemented (bits [7:3] of priority), then there are 32 preemption levels, and the active state of these preemption levels are held in ICH_AP0R0 in the bits corresponding to Priority[7:3].

If 6 bits of preemption are implemented (bits [7:2] of priority), then there are 64 preemption levels, and:

- The active state of preemption levels 0 - 124 are held in ICH_AP0R0 in the bits corresponding to 0:Priority[6:2].
- The active state of preemption levels 128 - 252 are held in ICH_AP0R1 in the bits corresponding to 1:Priority[6:2].

If 7 bits of preemption are implemented (bits [7:1] of priority), then there are 128 preemption levels, and:

- The active state of preemption levels 0 - 62 are held in ICH_AP0R0 in the bits corresponding to 00:Priority[5:1].
- The active state of preemption levels 64 - 126 are held in ICH_AP0R1 in the bits corresponding to 01:Priority[5:1].
- The active state of preemption levels 128 - 190 are held in ICH_AP0R2 in the bits corresponding to 10:Priority[5:1].
• The active state of preemption levels 192 - 254 are held in ICH_AP0R3 in the bits corresponding to 11:Priority[5:1].

Note

Having the bit corresponding to a priority set to 1 in both ICH_AP0R<n> and ICH_AP1R<n> might result in UNPREDICTABLE behavior of the interrupt prioritization system for virtual interrupts.

On a Warm reset, this field resets to 0.

Accessing the ICH_AP0R<n>

ICH_AP0R1 is only implemented in implementations that support 6 or more bits of preemption. ICH_AP0R2 and ICH_AP0R3 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are UNDEFINED.

Note

The number of bits of preemption is indicated by ICH_VTR.PREbits.

Writing to the active priority registers in any order other than the following order will result in UNPREDICTABLE behavior:

- ICH_AP0R<n>
- ICH_AP1R<n>

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_AP0R[UInt(opc2<1:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_AP0R[UInt(opc2<1:0>)];

MCR{<c>}{<q>} <coproc>, {#<opc1>}, <Rt>, <CRn>, <CRm>{, #<opc2>}
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elseif PSTATE.EL == EL2 then
    if ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_AP0R[UInt(opc2<1:0>)] = R[t];
    endif
elseif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_AP0R[UInt(opc2<1:0>)] = R[t];
    endif
endif
ICH_AP1R<n>, Interrupt Controller Hyp Active Priorities Group 1 Registers, n = 0 - 3

The ICH_AP1R<n> characteristics are:

**Purpose**

Provides information about Group 1 active priorities for EL2.

**Configuration**

AArch32 System register ICH_AP1R<n> bits [31:0] are architecturally mapped to AArch64 System register ICH_AP1R<n>._EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_AP1R<n> are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

ICH_AP1R<n> is a 32-bit register.

**Field descriptions**

The ICH_AP1R<n> bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>P31</td>
</tr>
<tr>
<td>30</td>
<td>P30</td>
</tr>
<tr>
<td>29</td>
<td>P29</td>
</tr>
<tr>
<td>28</td>
<td>P28</td>
</tr>
<tr>
<td>27</td>
<td>P27</td>
</tr>
<tr>
<td>26</td>
<td>P26</td>
</tr>
<tr>
<td>25</td>
<td>P25</td>
</tr>
<tr>
<td>24</td>
<td>P24</td>
</tr>
<tr>
<td>23</td>
<td>P23</td>
</tr>
<tr>
<td>22</td>
<td>P22</td>
</tr>
<tr>
<td>21</td>
<td>P21</td>
</tr>
<tr>
<td>20</td>
<td>P20</td>
</tr>
<tr>
<td>19</td>
<td>P19</td>
</tr>
<tr>
<td>18</td>
<td>P18</td>
</tr>
<tr>
<td>17</td>
<td>P17</td>
</tr>
<tr>
<td>16</td>
<td>P16</td>
</tr>
<tr>
<td>15</td>
<td>P15</td>
</tr>
<tr>
<td>14</td>
<td>P14</td>
</tr>
<tr>
<td>13</td>
<td>P13</td>
</tr>
<tr>
<td>12</td>
<td>P12</td>
</tr>
<tr>
<td>11</td>
<td>P11</td>
</tr>
<tr>
<td>10</td>
<td>P10</td>
</tr>
<tr>
<td>9</td>
<td>P9</td>
</tr>
<tr>
<td>8</td>
<td>P8</td>
</tr>
<tr>
<td>7</td>
<td>P7</td>
</tr>
<tr>
<td>6</td>
<td>P6</td>
</tr>
<tr>
<td>5</td>
<td>P5</td>
</tr>
<tr>
<td>4</td>
<td>P4</td>
</tr>
<tr>
<td>3</td>
<td>P3</td>
</tr>
<tr>
<td>2</td>
<td>P2</td>
</tr>
<tr>
<td>1</td>
<td>P1</td>
</tr>
<tr>
<td>0</td>
<td>P0</td>
</tr>
</tbody>
</table>

P<x>, bit [x], for x = 31 to 0

Group 1 interrupt active priorities. Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no Group 1 interrupt active at the priority corresponding to that bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>There is a Group 1 interrupt active at the priority corresponding to that bit.</td>
</tr>
</tbody>
</table>

The correspondence between priority levels and bits depends on the number of bits of priority that are implemented.

If 5 bits of preemption are implemented (bits [7:3] of priority), then there are 32 preemption levels, and the active state of these preemption levels are held in ICH_AP1R0 in the bits corresponding to Priority[7:3].

If 6 bits of preemption are implemented (bits [7:2] of priority), then there are 64 preemption levels, and:

- The active state of preemption levels 0 - 124 are held in ICH_AP1R0 in the bits corresponding to 0:Priority[6:2].
- The active state of preemption levels 128 - 252 are held in ICH_AP1R1 in the bits corresponding to 1:Priority[6:2].

If 7 bits of preemption are implemented (bits [7:1] of priority), then there are 128 preemption levels, and:

- The active state of preemption levels 0 - 62 are held in ICH_AP1R0 in the bits corresponding to 00:Priority[5:1].
- The active state of preemption levels 64 - 126 are held in ICH_AP1R1 in the bits corresponding to 01:Priority[5:1].
- The active state of preemption levels 128 - 190 are held in ICH_AP1R2 in the bits corresponding to 10:Priority[5:1].
• The active state of preemption levels 192 - 254 are held in ICH_AP1R3 in the bits corresponding to 11:Priority[5:1].

**Note**

Having the bit corresponding to a priority set to 1 in both ICH_AP0R<n> and ICH_AP1R<n> might result in **UNPREDICTABLE** behavior of the interrupt prioritization system for virtual interrupts.

On a Warm reset, this field resets to 0.

### Accessing the ICH_AP1R<n>

ICH_AP1R1 is only implemented in implementations that support 6 or more bits of preemption. ICH_AP1R2 and ICH_AP1R3 are only implemented in implementations that support 7 bits of preemption. Unimplemented registers are **UNDEFINED**.

**Note**

The number of bits of preemption is indicated by ICH_VTR.PREbits

Writing to the active priority registers in any order other than the following order will result in **UNPREDICTABLE** behavior:

- ICH_AP0R<n>
- ICH_AP1R<n>

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}<\text{coproc}>,\{#<opc1>,<Rt>,<CRn>,<CRm}\{,#<opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then

    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if ICC_HSRE.SRE == '0' then
            UNDEFINED;
        else
            return ICH_AP1R[UInt(opc2<1:0>)];
        end if;
    else
        return ICH_AP1R[UInt(opc2<1:0>)];
    end if;
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICH_AP1R[ UInt(opc2<1:0>) ];
    end if;
else
    return ICH_AP1R[ UInt(opc2<1:0>) ];
end if;
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    if ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_AP1R[UInt(opc2<1:0>)] = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_AP1R[UInt(opc2<1:0>)] = R[t];
    endif
endif
ICH_EISR, Interrupt Controller End of Interrupt Status Register

The ICH_EISR characteristics are:

**Purpose**

Indicates which List registers have outstanding EOI maintenance interrupts.

**Configuration**

AArch32 System register ICH_EISR bits [31:0] are architecturally mapped to AArch64 System register ICH_EISR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_EISR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

ICH_EISR is a 32-bit register.

**Field descriptions**

The ICH_EISR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>RES0</th>
<th>Status15</th>
<th>Status14</th>
<th>Status13</th>
<th>Status12</th>
<th>Status11</th>
<th>Status10</th>
<th>Status9</th>
<th>Status8</th>
<th>Status7</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**Status<n>, bit [n], for n = 15 to 0**

EOI maintenance interrupt status bit for List register <n>:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List register &lt;n&gt;, ICH_LR&lt;n&gt;, does not have an EOI maintenance interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>List register &lt;n&gt;, ICH_LR&lt;n&gt;, has an EOI maintenance interrupt that has not been handled.</td>
</tr>
</tbody>
</table>

For any ICH_LR<n>, the corresponding status bit is set to 1 if all of the following are true:

- ICH_LRC<n>.State is 0b00.
- ICH_LRC<n>.HW is 0.
- ICH_LRC<n>.EOI (bit [9]) is 1, indicating that when the interrupt corresponding to that List register is deactivated, a maintenance interrupt is asserted.

On a Warm reset, this field resets to 0.

**Accessing the ICH_EISR**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elseif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_EISR;
elseif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_EISR;

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b011</td>
</tr>
</tbody>
</table>
ICH_ELRSR, Interrupt Controller Empty List Register Status Register

The ICH_ELRSR characteristics are:

Purpose

Indicates which List registers contain valid interrupts.

Configuration

AArch32 System register ICH_ELRSR bits [31:0] are architecturally mapped to AArch64 System register ICH_ELRSR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_ELRSR are UNDEFINED.

If EL2 is not implemented, this register is res0 from EL3.

Attributes

ICH_ELRSR is a 32-bit register.

Field descriptions

The ICH_ELRSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Status15 | Status14 | Status13 | Status12 | Status11 | Status10 | Status9 | Status8 | Status7 |

Bits [31:16]

Reserved, RES0.

Status<n>, bit [n], for n = 15 to 0

Status bit for List register <n>, ICH_LR<n>:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List register ICH_LR&lt;n&gt;, if implemented, contains a valid interrupt. Using this List register can result in overwriting a valid interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>List register ICH_LR&lt;n&gt; does not contain a valid interrupt. The List register is empty and can be used without overwriting a valid interrupt or losing an EOI maintenance interrupt.</td>
</tr>
</tbody>
</table>

For any List register <n>, the corresponding status bit is set to 1 if ICH_LRC<n>.State is 0b00 and either ICH_LRC<n>.HW is 1 or ICH_LRC<n>.EOI (bit [9]) is 0.

Accessing the ICH_ELRSR

Accesses to this register use the following encodings:
MRC{c}<q> coproc>, {#}opc1>, <Rt>, <CRn>, <CRm>{, {#}opc2>

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b1011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_ELRSR;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_ELRSR;
ICH_HCR, Interrupt Controller Hyp Control Register

The ICH_HCR characteristics are:

**Purpose**

Controls the environment for VMs.

**Configuration**

AArch32 System register ICH_HCR bits [31:0] are architecturally mapped to AArch64 System register ICH_HCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_HCR are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

**Attributes**

ICH_HCR is a 32-bit register.

**Field descriptions**

The ICH_HCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EOIcount | RES0 | TDIR | TSE | TALL1 | TALL0 | TCRES0 | vSGIEOICount | vGrp1DIE | vGrp1EIE | vGrp0DIE | vGrp0EIE | NPIE | LRENPIE | UIE | En |

**EOIcount, bits [31:27]**

This field is incremented whenever a successful write to a virtual EOIR or DIR register would have resulted in a virtual interrupt deactivation. That is either:

- A virtual write to EOIR with a valid interrupt identifier that is not in the LPI range (that is < 8192) when EOI mode is zero and no List Register was found.
- A virtual write to DIR with a valid interrupt identifier that is not in the LPI range (that is < 8192) when EOI mode is one and no List Register was found.

This allows software to manage more active interrupts than there are implemented List Registers.

It **is constrained unpredictable** whether a virtual write to EOIR that does not clear a bit in the Active Priorities registers (ICH_AP0R<n>/ICH_AP1R<n>) increments EOIcount. Permitted behaviors are:

- Increment EOIcount.
- Leave EOIcount unchanged.

On a Warm reset, this field resets to 0.

**Bits [26:15]**

Reserved, RES0.

**TDIR, bit [14]**

Trap Non-secure EL1 writes to ICC_DIR and ICV_DIR.
ICH_HCR, Interrupt Controller Hyp Control Register

<table>
<thead>
<tr>
<th>TDIR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1 writes of ICC_DIR and ICV_DIR are not trapped to EL2, unless trapped by other mechanisms.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 writes of ICV_DIR are trapped to EL2. It is IMPLEMENTATION DEFINED whether Non-secure writes of ICC_DIR are trapped. Not trapping ICC_DIR writes is DEPRECATED.</td>
</tr>
</tbody>
</table>

Support for this bit is OPTIONAL, with support indicated by ICH_VTR.

If the implementation does not support this trap, this bit is RES0.

Arm deprecates not including this trap bit.

On a Warm reset, this field resets to 0.

**TSEI, bit [13]**

Trap all locally generated SEIs. This bit allows the hypervisor to intercept locally generated SEIs that would otherwise be taken at Non-secure EL1.

<table>
<thead>
<tr>
<th>TSEI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Locally generated SEIs do not cause a trap to EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Locally generated SEIs trap to EL2.</td>
</tr>
</tbody>
</table>

If ICH_VTR.SEIS is 0, this bit is RES0.

On a Warm reset, this field resets to 0.

**TALL1, bit [12]**

Trap all Non-secure EL1 accesses to ICC_* and ICV_* System registers for Group 1 interrupts to EL2.

<table>
<thead>
<tr>
<th>TALL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1 accesses to ICC_* and ICV_* registers for Group 1 interrupts proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to ICC_* and ICV_* registers for Group 1 interrupts trap to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**TALL0, bit [11]**

Trap all Non-secure EL1 accesses to ICC_* and ICV_* System registers for Group 0 interrupts to EL2.

<table>
<thead>
<tr>
<th>TALL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1 accesses to ICC_* and ICV_* registers for Group 0 interrupts proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to ICC_* and ICV_* registers for Group 0 interrupts trap to EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**TC, bit [10]**

Trap all Non-secure EL1 accesses to System registers that are common to Group 0 and Group 1 to EL2.

<table>
<thead>
<tr>
<th>TC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure EL1 accesses to common registers proceed as normal.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure EL1 accesses to common registers trap to EL2.</td>
</tr>
</tbody>
</table>

This affects accesses to ICC_SGI0R, ICC_SGI1R, ICC_ASGI1R, ICC_CTLR, ICC_DIR, ICC_PMR, ICC_RPR, ICV_CTLR, ICV_DIR, ICV_PMR, and ICV_RPR.

On a Warm reset, this field resets to 0.
Bit [9]

Reserved, RES0.

vSGIEOICount, bit [8]

When FEAT_GICv4p1 is implemented:

Controls whether deactivation of virtual SGIs can increment ICH_HCR_EL2.EOIcount

<table>
<thead>
<tr>
<th>vSGIEOICount</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Deactivation of virtual SGIs can increment ICH_HCR_EOIcount.</td>
</tr>
<tr>
<td>0b1</td>
<td>Deactivation of virtual SGIs does not increment ICH_HCR_EOIcount.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

VGrp1DIE, bit [7]

VM Group 1 Disabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected vPE is disabled:

<table>
<thead>
<tr>
<th>VGrp1DIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR.VENG1 is 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

VGrp1EIE, bit [6]

VM Group 1 Enabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected vPE is enabled:

<table>
<thead>
<tr>
<th>VGrp1EIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR.VENG1 is 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

VGrp0DIE, bit [5]

VM Group 0 Disabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 0 interrupts from the virtual CPU interface to the connected vPE is disabled:

<table>
<thead>
<tr>
<th>VGrp0DIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR.VENG0 is 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

VGrp0EIE, bit [4]

VM Group 0 Enabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 0 interrupts from the virtual CPU interface to the connected vPE is enabled:
<table>
<thead>
<tr>
<th>VGrp0EIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled when ICH_VMCR.VENG0 is 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**NPIE, bit [3]**

No Pending Interrupt Enable. Enables the signaling of a maintenance interrupt when there are no List registers with the State field set to 0b01 (pending):

<table>
<thead>
<tr>
<th>NPIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt signaled while the List registers contain no interrupts in the pending state.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**LRENPIE, bit [2]**

List Register Entry Not Present Interrupt Enable. Enables the signaling of a maintenance interrupt while the virtual CPU interface does not have a corresponding valid List register entry for an EOI request:

<table>
<thead>
<tr>
<th>LRENPIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt is asserted while the EOIcount field is not 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**UIE, bit [1]**

Underflow Interrupt Enable. Enables the signaling of a maintenance interrupt when the List registers are empty, or hold only one valid entry:

<table>
<thead>
<tr>
<th>UIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Maintenance interrupt is asserted if none, or only one, of the List register entries is marked as a valid interrupt.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**En, bit [0]**

Enable. Global enable bit for the virtual CPU interface:

<table>
<thead>
<tr>
<th>En</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual CPU interface operation disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual CPU interface operation enabled.</td>
</tr>
</tbody>
</table>

When this field is set to 0:

- The virtual CPU interface does not signal any maintenance interrupts.
- The virtual CPU interface does not signal any virtual interrupts.
- A read of ICV_IAR0, ICV_IAR1, GICV_IAR or GICV_AIAR returns a spurious interrupt ID.

On a Warm reset, this field resets to 0.

**Accessing the ICH_HCR**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    return ICH_HCR;
elsif PSTATE.EL == EL2 then
    if ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_HCR = R[t];
    elsif PSTATE.EL == EL3 then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            ICH_HCR = R[t];
        end if
    end if
end if

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    return ICH_HCR;
elsif PSTATE.EL == EL2 then
    if ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        ICH_HCR = R[t];
    elsif PSTATE.EL == EL3 then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            ICH_HCR = R[t];
        end if
    end if
end if

ICH_HCR, Interrupt Controller Hyp Control Register

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b000</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
ICH_LRC<n>, Interrupt Controller List Registers, n = 0 - 15

The ICH_LRC<n> characteristics are:

**Purpose**

Provides interrupt context information for the virtual CPU interface.

**Configuration**

AArch32 System register ICH_LRC<n> bits [31:0] are architecturally mapped to AArch64 System register ICH_LR<n>_EL2[63:32].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_LRC<n> are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

If list register n is not implemented, then accesses to this register are UNDEFINED.

**Attributes**

ICH_LRC<n> is a 32-bit register.

**Field descriptions**

The ICH_LRC<n> bit assignments are:

<table>
<thead>
<tr>
<th>State</th>
<th>HW</th>
<th>Group</th>
<th>Priority</th>
<th>pINTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**State, bits [31:30]**

The state of the interrupt:

<table>
<thead>
<tr>
<th>State</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Invalid (Inactive).</td>
</tr>
<tr>
<td>0b01</td>
<td>Pending.</td>
</tr>
<tr>
<td>0b10</td>
<td>Active.</td>
</tr>
<tr>
<td>0b11</td>
<td>Pending and active</td>
</tr>
</tbody>
</table>

The GIC updates these state bits as virtual interrupts proceed through the interrupt life cycle. Entries in the invalid state are ignored, except for the purpose of generating virtual maintenance interrupts.

For hardware interrupts, the pending and active state is held in the physical Distributor rather than the virtual CPU interface. A hypervisor must only use the pending and active state for software originated interrupts, which are typically associated with virtual devices, or SGIs.

On a Warm reset, this field resets to 0.

**HW, bit [29]**

Indicates whether this virtual interrupt maps directly to a hardware interrupt, meaning that it corresponds to a physical interrupt. Deactivation of the virtual interrupt also causes the deactivation of the physical interrupt with the INTID that the pINTID field indicates.
The interrupt is triggered entirely by software. No notification is sent to the Distributor when the virtual interrupt is deactivated.

The interrupt maps directly to a hardware interrupt. A deactivate interrupt request is sent to the Distributor when the virtual interrupt is deactivated, using the pINTID field from this register to indicate the physical INTID. If ICH_VMCR VEOIM is 0, this request corresponds to a write to ICC_EOIR0 or ICC_EOIR1. Otherwise, it corresponds to a write to ICC_DIR.

On a Warm reset, this field resets to 0.

### Group, bit [28]

Indicates the group for this virtual interrupt.

<table>
<thead>
<tr>
<th>Group</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This is a Group 0 virtual interrupt. ICH_VMCR VFIQEn determines whether it is signaled as a virtual IRQ or as a virtual FIQ, and ICH_VMCR VENG0 enables signaling of this interrupt to the virtual machine.</td>
</tr>
<tr>
<td>0b1</td>
<td>This is a Group 1 virtual interrupt, signaled as a virtual IRQ. ICH_VMCR VENG1 enables the signaling of this interrupt to the virtual machine. If ICH_VMCR VCBPR is 0, then ICC_BPR1 determines if a pending Group 1 interrupt has sufficient priority to preempt current execution. Otherwise, ICH_LR&lt;n&gt; determines preemption.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

### Bits [27:24]

Reserved, RES0.

### Priority, bits [23:16]

The priority of this interrupt.

It is IMPLEMENTATION DEFINED how many bits of priority are implemented, though at least five bits must be implemented. Unimplemented bits are RES0 and start from bit[16] up to bit[18]. The number of implemented bits can be discovered from ICH_VTR PRIBits.

On a Warm reset, this field resets to 0.

### Bits [15:13]

Reserved, RES0.

### pINTID, bits [12:0]

Physical INTID, for hardware interrupts.

When ICH_LRC<n>.HW is 0 (there is no corresponding physical interrupt), this field has the following meaning:

- Bits[12:10] : RES0.
- Bit[9] : EOI. If this bit is 1, then when the interrupt identified by vINTID is deactivated, an EOI maintenance interrupt is asserted.
- Bits[8:0] : Reserved, RES0.

When ICH_LRC<n>.HW is 1 (there is a corresponding physical interrupt):

- This field indicates the physical INTID. This field is only required to implement enough bits to hold a valid value for the implemented INTID size. Any unused higher order bits are RES0.
• When ICC_CTLR_EL1.ExtRange is 0, then bits[44:42] of this field are RES0.
• If the value of pINTID is not a valid INTID, behavior is UNPREDICTABLE. If the value of pINTID indicates a PPI, this field applies to the PPI associated with this same physical PE ID as the virtual CPU interface requesting the deactivation.

A hardware physical identifier is only required in List Registers for interrupts that require deactivation. This means only 13 bits of Physical INTID are required, regardless of the number specified by ICC_CTLR.IDbits.

On a Warm reset, this field resets to 0.

**Accessing the ICH_LRC<n>**

ICH_LR<n> and ICH_LRC<n> can be updated independently.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b111:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_LRC[UInt(CRm<0>:opc2<2:0>)];
  endif
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_LRC[UInt(CRm<0>:opc2<2:0>)];
  endif
else
  return ICH_LRC[UInt(CRm<0>:opc2<2:0>)];
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b111:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_LRC[UInt(CRm<0>:opc2<2:0>)] = R[t];
  endif
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_LRC[UInt(CRm<0>:opc2<2:0>)] = R[t];
  endif

ICH_LR<n>, Interrupt Controller List Registers, n = 0 - 15

The ICH_LR<n> characteristics are:

**Purpose**

Provides interrupt context information for the virtual CPU interface.

**Configuration**

AArch32 System register ICH_LR<n> bits [31:0] are architecturally mapped to AArch64 System register ICH_LR<n>_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_LR<n> are **UNDEFINED**.

If EL2 is not implemented, this register is **RES0** from EL3.

If list register n is not implemented, then accesses to this register are **UNDEFINED**.

**Attributes**

ICH_LR<n> is a 32-bit register.

**Field descriptions**

The ICH_LR<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**vINTID**, bits [31:0]

Virtual INTID of the interrupt.

If the value of vINTID is 1020-1023 and ICH_LRC<n>.State!=0b00 (Inactive), behavior is **UNPREDICTABLE**.

Behavior is **UNPREDICTABLE** if two or more List Registers specify the same vINTID when:

- ICH_LRC<n>.State == 01.
- ICH_LRC<n>.State == 10.
- ICH_LRC<n>.State == 11.

It is **IMPLEMENTATION DEFINED** how many bits are implemented, though at least 16 bits must be implemented. Unimplemented bits are **RES0**. The number of implemented bits can be discovered from ICH_VTR.IDbits.

**Note**

When a VM is using memory-mapped access to the GIC, software must ensure that the correct source PE ID is provided in bits[12:10].

On a Warm reset, this field resets to 0.

**Accessing the ICH_LR<n>**

ICH_LR<n> and ICH_LRC<n> can be updated independently.
Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#<opc1>, <Rt>, <CRn>, <CRm>{, {#<opc2>}}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b110:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_LR[UInt(CRm<0>:opc2<2:0>)];
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_LR[UInt(CRm<0>:opc2<2:0>)];

MCR{<c>}{<q>} <coproc>, {#<opc1>, <Rt>, <CRn>, <CRm>{, {#<opc2>}}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b110:n[3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_LR[UInt(CRm<0>:opc2<2:0>)] = R[t];
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_LR[UInt(CRm<0>:opc2<2:0>)] = R[t];
ICH_MISR, Interrupt Controller Maintenance Interrupt State Register

The ICH_MISR characteristics are:

**Purpose**

Indicates which maintenance interrupts are asserted.

**Configuration**

AArch32 System register ICH_MISR bits [31:0] are architecturally mapped to AArch64 System register ICH_MISR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_MISR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

ICH_MISR is a 32-bit register.

**Field descriptions**

The ICH_MISR bit assignments are:

|            | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|------------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|            | RES0 | VGrp1D | VGrp1E | VGrp0D | VGrp0E | NP | LRENP | U | EOI |

**Bits [31:8]**

Reserved, RES0.

**VGrp1D, bit [7]**

vPE Group 1 Disabled.

<table>
<thead>
<tr>
<th>VGrp1D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 1 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 1 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when ICH_HCR.VGrp1DIE is 1 and ICH_VMCR.VENG0 is 0.

On a Warm reset, this field resets to 0.

**VGrp1E, bit [6]**

vPE Group 1 Enabled.

<table>
<thead>
<tr>
<th>VGrp1E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 1 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 1 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when ICH_HCR.VGrp1EIE is 1 and ICH_VMCR.VENG1 is 1.

On a Warm reset, this field resets to 0.
ICH_MISR, Interrupt Controller Maintenance Interrupt State Register

**VGrp0D, bit [5]**

vPE Group 0 Disabled.

<table>
<thead>
<tr>
<th>VGrp0D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when **ICH_HCR.VGrp0DIE** is 1 and **ICH_VMCR.VENG0** is 0.

On a Warm reset, this field resets to 0.

**VGrp0E, bit [4]**

vPE Group 0 Enabled.

<table>
<thead>
<tr>
<th>VGrp0E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when **ICH_HCR.VGrp0EIE** is 1 and **ICH_VMCR.VENG0** is 1.

On a Warm reset, this field resets to 0.

**NP, bit [3]**

No Pending.

<table>
<thead>
<tr>
<th>NP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Pending maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>No Pending maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when **ICH_HCR.NPIE** is 1 and no List register is in pending state.

On a Warm reset, this field resets to 0.

**LRENP, bit [2]**

List Register Entry Not Present.

<table>
<thead>
<tr>
<th>LRENP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List Register Entry Not Present maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>List Register Entry Not Present maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when **ICH_HCR.LRENPIE** is 1 and **ICH_HCR.EOIcount** is non-zero.

On a Warm reset, this field resets to 0.

**U, bit [1]**

Underflow.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when **ICH_HCR.UIE** is 1 and zero or one of the List register entries are marked as a valid interrupt, that is, if the corresponding **ICH_LRC<n>.State** bits do not equal 0x0.

On a Warm reset, this field resets to 0.
**EOI, bit [0]**

End Of Interrupt.

<table>
<thead>
<tr>
<th>EOI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>End Of Interrupt maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>End Of Interrupt maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when at least one bit in **ICH_EISR** is 1.

On a Warm reset, this field resets to 0.

**Accessing the ICH_MISR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
    if ICC_HSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICH_MISR;
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICH_MISR;
ICH_VMCR, Interrupt Controller Virtual Machine Control Register

The ICH_VMCR characteristics are:

**Purpose**

Enables the hypervisor to save and restore the virtual machine view of the GIC state.

**Configuration**

AArch32 System register ICH_VMCR bits [31:0] are architecturally mapped to AArch64 System register ICH_VMCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICH_VMCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

ICH_VMCR is a 32-bit register.

**Field descriptions**

The ICH_VMCR bit assignments are:

| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|----------------------------------------|--------|--------|--------|--------|--------|
| VPMR        | VBPR0 | VBPR1  | RES0   | VEOIM  | RES0   | VCBPR  | VFIQEn | VAckCtl | VENG1 | VENG0 |

**VPMR, bits [31:24]**

Virtual Priority Mask. The priority mask level for the virtual CPU interface. If the priority of a pending virtual interrupt is higher than the value indicated by this field, the interface signals the virtual interrupt to the PE.

This field is an alias of ICV_PMR.Priority.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VBPR0, bits [23:21]**

Virtual Binary Point Register, Group 0. Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 0 interrupt preemption, and also determines Group 1 interrupt preemption if ICH_VMCR.VCBPR == 1.

This field is an alias of ICV_BPR0.BinaryPoint.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VBPR1, bits [20:18]**

Virtual Binary Point Register, Group 1. Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption if ICH_VMCR.VCBPR == 0.

This field is an alias of ICV_BPR1.BinaryPoint.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Bits [17:10]**

Reserved, RES0.

**VEOIM, bit [9]**

Virtual EOI mode. Controls whether a write to an End of Interrupt register also deactivates the virtual interrupt:

<table>
<thead>
<tr>
<th>VEOIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICV_EOIR0 and ICV_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICV_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICV_EOIR0 and ICV_EOIR1 provide priority drop functionality only. ICV_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

This bit is an alias of ICV_CTLR.EOImode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [8:5]**

Reserved, RES0.

**VCBPR, bit [4]**

Virtual Common Binary Point Register. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VCBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICV_BPR0 determines the preemption group for virtual Group 0 interrupts only. ICV_BPR1 determines the preemption group for virtual Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICV_BPR0 determines the preemption group for both virtual Group 0 and virtual Group 1 interrupts. Reads of ICV_BPR1 return ICV_BPR0 plus one, saturated to 0b111. Writes to ICV_BPR1 are ignored.</td>
</tr>
</tbody>
</table>

This field is an alias of ICV_CTLR.CBPR.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VFIQEn, bit [3]**

Virtual FIQ enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VFIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupts are presented as virtualIRQs.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 virtual interrupts are presented as virtual FIQs.</td>
</tr>
</tbody>
</table>

This bit is an alias of GICV_CTLR.FIQEn.

In implementations where the Non-secure copy of ICC_SRE.SRE is always 1, this bit is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VAckCtl, bit [2]**

Virtual AckCtl. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VAckCtl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns an INTID of 1022.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns the INTID of the corresponding interrupt.</td>
</tr>
</tbody>
</table>
This bit is an alias of GICV_CTLR.AckCtl.

This field is supported for backwards compatibility with GICv2. Arm deprecates the use of this field.

In implementations where the Non-secure copy of ICC_SRE.SRE is always 1, this bit is res0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VENG1, bit [1]**

Virtual Group 1 interrupt enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

This bit is an alias of ICV_IGRPEN1.Enable.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**VENG0, bit [0]**

Virtual Group 0 interrupt enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

This bit is an alias of ICV_IGRPEN0.Enable.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICH_VMCR**

When EL2 is using System register access, EL1 using either System register or memory-mapped access must be supported.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}, <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        if ICC_HSRE.SRE == '0' then
            UNDEFINED;
        else
            return ICH_VMCR;
        elsif PSTATE.EL == EL3 then
            if ICC_MSRE.SRE == '0' then
                UNDEFINED;
            else
                return ICH_VMCR;
            endif
        endif
    endif
else
    return ICH_VMCR;
### MCR coproc, {#}opc1, <Rt>, <CRn>, <CRm>{, {#}opc2}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_VMCR = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    ICH_VMCR = R[t];
  end if;
end if;
```
ICH_VTR, Interrupt Controller VGIC Type Register

The ICH_VTR characteristics are:

**Purpose**

Reports supported GIC virtualization features.

**Configuration**

AArch32 System register ICH_VTR bits [31:0] are architecturally mapped to AArch64 System register
ICH_VTR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to
ICH_VTR are **UNDEFINED**.

If EL2 is not implemented, all bits in this register are RES0 from EL3, except for nV4, which is RES1 from EL3.

**Attributes**

ICH_VTR is a 32-bit register.

**Field descriptions**

The ICH_VTR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| PRIbits | PREbits | IDbits | SEISA3VnV4TDS | RES0 | ListRegs |

**PRIbits, bits [31:29]**

Priority bits. The number of virtual priority bits implemented, minus one.

An implementation must implement at least 32 levels of virtual priority (5 priority bits).

This field is an alias of ICV_CTLR.PRIbits.

**PREbits, bits [28:26]**

The number of virtual preemption bits implemented, minus one.

An implementation must implement at least 32 levels of virtual preemption priority (5 preemption bits).

The value of this field must be less than or equal to the value of ICH_VTR.PRIbits.

**IDbits, bits [25:23]**

The number of virtual interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is an alias of ICV_CTLR.IDbits.
SEIS, bit [22]

SEI Support. Indicates whether the virtual CPU interface supports generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic does not support generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports generation of SEIs.</td>
</tr>
</tbody>
</table>

This bit is an alias of `ICV_CTLR:SEIS`.

A3V, bit [21]

Affinity 3 Valid. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

This bit is an alias of `ICV_CTLR:A3V`.

nV4, bit [20]

Direct injection of virtual interrupts not supported. Possible values are:

<table>
<thead>
<tr>
<th>nV4</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The CPU interface logic supports direct injection of virtual interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>The CPU interface logic does not support direct injection of virtual interrupts.</td>
</tr>
</tbody>
</table>

If FEAT_GICv4 is not implemented, this bit is RES1.

TDS, bit [19]

Separate trapping of Non-secure EL1 writes to `ICV_DIR` supported.

<table>
<thead>
<tr>
<th>TDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Implementation does not support <code>ICH_HCR:TDIR</code>.</td>
</tr>
<tr>
<td>0b1</td>
<td>Implementation supports <code>ICH_HCR:TDIR</code>.</td>
</tr>
</tbody>
</table>

Bits [18:5]

Reserved, RES0.

ListRegs, bits [4:0]

The number of implemented List registers, minus one. For example, a value of 0b01111 indicates that the maximum of 16 List registers are implemented.

**Accessing the ICH_VTR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  if ICC_HSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_VTR;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICH_VTR;
ICIALLU, Instruction Cache Invalidate All to PoU

The ICIALLU characteristics are:

**Purpose**

Invalidate all instruction caches to PoU. If branch predictors are architecturally visible, also flush branch predictors.

**Configuration**

AArch32 System instruction ICIALLU performs the same function as AArch64 System instruction IC IALLU.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICIALLU are UNDEFINED.

**Attributes**

ICIALLU is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by \(<Rt>\) is ignored.

**Executing the ICIALLU instruction**

The PE ignores the value of \(<Rt>\). Software does not have to write a value to this register before issuing this instruction.

When \(HCR.FB\) is 1, at Non-secure EL1 this instruction executes as a ICIALLUIS.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>}\{<q>\} \ <\text{coproc}, \ {#}<\text{opc1}>, \ <Rt>, \ <CRn>, \ <CRm}\{, \ {#}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsf if PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TPU == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TOCU == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPU == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TOCU == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FB == '1' then
      ICIALLUIS();
    else
      ICIALLU();
  elsf if PSTATE.EL == EL2 then
    ICIALLU();
  elsf if PSTATE.EL == EL3 then
    ICIALLU();
ICIALLUIS, Instruction Cache Invalidate All to PoU, Inner Shareable

The ICIALLUIS characteristics are:

Purpose

Invalidate all instruction caches Inner Shareable to PoU. If branch predictors are architecturally visible, also flush branch predictors.

Configuration

AArch32 System instruction ICIALLUIS performs the same function as AArch64 System instruction IC IALLUIS.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICIALLUIS are UNDEFINED.

Attributes

ICIALLUIS is a 32-bit System instruction.

Field descriptions

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

Executing the ICIALLUIS instruction

The PE ignores the value of <Rt>. Software does not have to write a value to this register before issuing this instruction.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \ <\text{coproc}>, \{#\}<\text{opc1}>, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}\}{, \{#\}<\text{opc2}>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>


if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TPU == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TICAB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TOCU == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPU == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TICAB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TOCU == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ICIALLUIS();
    end if;
elsif PSTATE.EL == EL2 then
    ICIALLUIS();
elsif PSTATE.EL == EL3 then
    ICIALLUIS();
ICIMVAU, Instruction Cache line Invalidate by VA to PoU

The ICIMVAU characteristics are:

**Purpose**

Invalidate instruction cache line by virtual address to PoU.

**Configuration**

AArch32 System instruction ICIMVAU performs the same function as AArch64 System instruction IC IVAU.

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICIMVAU are UNDEFINED.

**Attributes**

ICIMVAU is a 32-bit System instruction.

**Field descriptions**

The ICIMVAU input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Virtual address to use</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
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<td>25</td>
<td></td>
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<tr>
<td>24</td>
<td></td>
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<td>23</td>
<td></td>
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<td>22</td>
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<td>21</td>
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<td>20</td>
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<td>19</td>
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<td>18</td>
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<td>17</td>
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<td>16</td>
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<td>15</td>
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<tr>
<td>14</td>
<td></td>
</tr>
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<td>13</td>
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<td>12</td>
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<td>11</td>
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<tr>
<td>10</td>
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<td>9</td>
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<td>8</td>
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<td>7</td>
<td></td>
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<td>6</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
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<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Virtual address to use. No alignment restrictions apply to this VA.

**Executing the ICIMVAU instruction**

Execution of this instruction might require an address translation from VA to PA, and that translation might fault. For more information, see 'AArch32 instruction cache maintenance instructions (IC*)'.

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{{, {#}<opc2>}}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TPU == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TOCU == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPU == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TOCU == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ICIMVAU(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ICIMVAU(R[t]);
eelsif PSTATE.EL == EL3 then
    ICIMVAU(R[t]);
ICV_AP0R<n>, Interrupt Controller Virtual Active Priorities Group 0 Registers, n = 0 - 3

The ICV_AP0R<n> characteristics are:

**Purpose**

Provides information about virtual Group 0 active priorities.

**Configuration**

AArch32 System register ICV_AP0R<n> bits [31:0] are architecturally mapped to AArch64 System register ICV_AP0R<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_AP0R<n> are undefined.

**Attributes**

ICV_AP0R<n> is a 32-bit register.

**Field descriptions**

The ICV_AP0R<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  |

IMPLEMENTATION DEFINED

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICV_AP0R<n>**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 0 active priorities) might result in UNPREDICTABLE behavior of the virtual interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICV_AP0R1 is only implemented in implementations that support 6 or more bits of priority. ICV_AP0R2 and ICV_AP0R3 are only implemented in implementations that support 7 bits of priority. Unimplemented registers are UNDEFINED.

Writing to the active priority registers in any order other than the following order might result in UNPREDICTABLE behavior of the interrupt prioritization system:

- ICV_AP0R<n>.
- ICV_AP1R<n>.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH.HCR.TALL0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_AP0R[UInt(opc2<1:0>)];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        return ICC_AP0R[UInt(opc2<1:0>)];
    endif
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_AP0R[UInt(opc2<1:0>)];
    endif
else
    return ICC_AP0R[UInt(opc2<1:0>)];
endif
if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
AArch32.TakeHypTrapException(0x03);
elif ICC_SRE.SRE == '0' then
UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
AArch32.TakeHypTrapException(0x03);
elif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
ICV_AP0R[UInt(opc2<1:0>)] = R[t];
elif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
ICV_AP0R[UInt(opc2<1:0>)] = R[t];
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif ICC_HSRE.SRE == '0' then
UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif ICC_HSRE.SRE == '0' then
UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif ICC_MSRE.SRE == '0' then
UNDEFINED;
elif ICC_MSRE.SRE == '0' then
UNDEFINED;
elif IIIC_AP0R[UInt(opc2<1:0>)] == R[t];
elif PSTATE.EL == EL2 then
if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
UNDEFINED;
elif ICC_HSRE.SRE == '0' then
UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
if Halted() && EDSCR.SDD == '1' then
UNDEFINED;
elif ICC_MSRE.SRE == '0' then
UNDEFINED;
elif ICC_MSRE.SRE == '0' then
UNDEFINED;
elif IIIC_AP0R[UInt(opc2<1:0>)] == R[t];
ICV_AP1R<n>, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3

The ICV_AP1R<n> characteristics are:

**Purpose**

Provides information about virtual Group 1 active priorities.

**Configuration**

AArch32 System register ICV_AP1R<n> bits [31:0] are architecturally mapped to AArch64 System register ICV_AP1R<n>_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_AP1R<n> are UNDEFINED.

**Attributes**

ICV_AP1R<n> is a 32-bit register.

**Field descriptions**

The ICV_AP1R<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

**Accessing the ICV_AP1R<n>**

Writing to these registers with any value other than the last read value of the register (or 0x00000000 when there are no Group 1 active priorities) might result in UNPREDICTABLE behavior of the virtual interrupt prioritization system, causing:

- Interrupts that should preempt execution to not preempt execution.
- Interrupts that should not preempt execution to preempt execution.

ICV_AP1R1 is only implemented in implementations that support 6 or more bits of priority. ICV_AP1R2 and ICV_AP1R3 are only implemented in implementations that support 7 bits of priority. Unimplemented registers are UNDEFINED.

Writing to the active priority registers in any order other than the following order might result in UNPREDICTABLE behavior of the interrupt prioritization system:

- ICV_AP0R<n>.
- ICV_AP1R<n>.

Accesses to this register use the following encodings:
ICV_AP1R<n>, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elseif EL2Enabled() && !ELUsingAArch32(EL2) && ICC_HCR_EL2.TALL1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && ICC_HCR.TALL1 == '1' then
    return ICC_API1R[UInt(opc2<1:0>)];
  elsif EL2Enabled() && ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      elseif HaveEL(EL3) then
        return ICC_API1R_NS[UInt(opc2<1:0>)];
      else
        return ICC_API1R[UInt(opc2<1:0>)];
  elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elseif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    UNDEFINED;
  elseif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
  elseif HaveEL(EL3) then
    return ICC_API1R[UInt(opc2<1:0>)];
  else
    return ICC_API1R_NS[UInt(opc2<1:0>)];
else if PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    if SCR_NS == '0' then
      return ICC_API1R_NS[UInt(opc2<1:0>)];
    else
      return ICC_API1R_NS[UInt(opc2<1:0>)];
ICV_AP1R<n>, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1001</td>
<td>0b0:n[1:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        ICV_API1R[UInt(opc2<1:0>)] = R[t];
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) then
        ICC_AP1R_NS[UInt(opc2<1:0>)] = R[t];
    else
        ICC_API1R[UInt(opc2<1:0>)] = R[t];
    end if
else
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    elsif HaveEL(EL3) then
        ICC_API1R_NS[UInt(opc2<1:0>)] = R[t];
    else
        ICC_API1R[UInt(opc2<1:0>)] = R[t];
    end if
else
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            ICC_API1R_S[UInt(opc2<1:0>)] = R[t];
        else
            ICC_API1R_NS[UInt(opc2<1:0>)] = R[t];
        end if
    end if
else
    if SCR.NS == '0' then
        ICC_API1R_S[UInt(opc2<1:0>)] = R[t];
    else
        ICC_API1R_NS[UInt(opc2<1:0>)] = R[t];
    end if
end if

ICV_API1R<n>, Interrupt Controller Virtual Active Priorities Group 1 Registers, n = 0 - 3
ICV_BPR0, Interrupt Controller Virtual Binary Point Register 0

The ICV_BPR0 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines virtual Group 0 interrupt preemption.

**Configuration**

AArch32 System register ICV_BPR0 bits [31:0] are architecturally mapped to AArch64 System register ICV_BPR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_BPR0 are UNDEFINED.

**Attributes**

ICV_BPR0 is a 32-bit register.

**Field descriptions**

The ICV_BPR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bits [31:3]</th>
<th>RES0</th>
<th>BinaryPoint</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>RES0</td>
<td>BinaryPoint</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**BinaryPoint, bits [2:0]**

The value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>[7:1]</td>
<td>[0]</td>
<td>ggggggg.s</td>
</tr>
<tr>
<td>1</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>2</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>gggggg.sss</td>
</tr>
<tr>
<td>3</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>ggggg.sssss</td>
</tr>
<tr>
<td>4</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sssssss</td>
</tr>
<tr>
<td>5</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>g.sssssssss</td>
</tr>
<tr>
<td>6</td>
<td>[7]</td>
<td>[6:0]</td>
<td>.ssssssssss</td>
</tr>
<tr>
<td>7</td>
<td>No preemption</td>
<td>[7:0]</td>
<td>.ssssssssss</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICV_BPR0**

The minimum binary point value is derived from the number of implemented priority bits. The number of priority bits is IMPLEMENTATION DEFINED, and reported by ICV_CTLR.PRIbits.
An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is set to the minimum supported value.

Accesses to this register use the following encodings:

\[
\text{MRC\{}<c>{<q}>\{} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm\}{, \{#\}<opc2>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
            AArch32.TakeHypTrapException(0x03);
elif ICC_SRE.SRE == '0' then
    UNDEFINED;
elif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
            AArch32.TakeHypTrapException(0x03);
elif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif ICC_MSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif ICC_BPR0;
elif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
elif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
elif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
elif ICC_BPR0;
elif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
    UNDEFINED;
elif ICC_BPR0;
else
    return ICC_BPR0;
else
    return ICC_BPR0;
end if;

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        ICC_BPR0 = R[t];
    endif
else
    ICC_BPR0 = R[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elseif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elseif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    else
        ICC_BPR0 = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        ICC_BPR0 = R[t];
    endif
ICV_BPR1, Interrupt Controller Virtual Binary Point Register 1

The ICV_BPR1 characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines virtual Group 1 interrupt preemption.

**Configuration**

AArch32 System register ICV_BPR1 bits [31:0] are architecturally mapped to AArch64 System register ICV_BPR1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_BPR1 are UNDEFINED.

**Attributes**

ICV_BPR1 is a 32-bit register.

**Field descriptions**

The ICV_BPR1 bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>BinaryPoint</td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Bits [31:3]

Reserved, RES0.

**BinaryPoint, bits [2:0]**

If the GIC is configured to use separate binary point fields for virtual Group 0 and virtual Group 1 interrupts, the value of this field controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. This is done as follows:

<table>
<thead>
<tr>
<th>Binary point value</th>
<th>Group priority field</th>
<th>Subpriority field</th>
<th>Field with binary point</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>.</td>
<td>.</td>
<td>.</td>
</tr>
<tr>
<td>1</td>
<td>[7:1]</td>
<td>[0]</td>
<td>ggggggg.s</td>
</tr>
<tr>
<td>2</td>
<td>[7:2]</td>
<td>[1:0]</td>
<td>gggggg.ss</td>
</tr>
<tr>
<td>3</td>
<td>[7:3]</td>
<td>[2:0]</td>
<td>ggggg.sss</td>
</tr>
<tr>
<td>4</td>
<td>[7:4]</td>
<td>[3:0]</td>
<td>gggg.sssss</td>
</tr>
<tr>
<td>5</td>
<td>[7:5]</td>
<td>[4:0]</td>
<td>ggg.sssssss</td>
</tr>
<tr>
<td>6</td>
<td>[7:6]</td>
<td>[5:0]</td>
<td>gg.sssssss</td>
</tr>
<tr>
<td>7</td>
<td>[7]</td>
<td>[6:0]</td>
<td>g.sssssssss</td>
</tr>
</tbody>
</table>

Writing 0 to this field will set this field to its reset value.

If ICV_CTLR.CBPR is set to 1, Non-secure EL1 reads return ICV_BPR0 + 1 saturated to 0b111. Non-secure EL1 writes are ignored.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the ICV_BPR1

The minimum value of this register is equal to the minimum value of ICV_BPR0 plus one.

An attempt to program the binary point field to a value less than the minimum value sets the field to the minimum value. On a reset, the binary point field is UNKNOWN.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc},\ \{#\}<\text{opc1},\ <\text{Rt},\ <\text{CRn},\ <\text{CRm}\{,\ \{#\}<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif ICC_BPR1 then
        return ICC_BPR1_NS;
    else
        return ICC_BPR1;
    endif
elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
    if Halted() && SCR.IRQ == '1' then
        UNDEFINED;
    else
        ICC_BPR1_NS;
    endif
else
    return ICC_BPR1;
endif
else
    if SCR.NS == '0' then
        return ICC_BPR1_S;
    else
        return ICC_BPR1_NS;
    endif
endif
MCR\{<c>\}{<q>\} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elseif ICC_BPR1_NS = R[t];
else
    ICC_BPR1 = R[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elseif ICC_BPR1_NS = R[t];
else
    ICC_BPR1 = R[t];
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elseif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    if SCR_NS == '0' then
        ICC_BPR1_S = R[t];
    else
        ICC_BPR1_NS = R[t];
ICV_CTLR, Interrupt Controller Virtual Control Register

The ICV_CTLR characteristics are:

**Purpose**

Controls aspects of the behavior of the GIC virtual CPU interface and provides information about the features implemented.

**Configuration**

AArch32 System register ICV_CTLR bits [31:0] are architecturally mapped to AArch64 System register ICV_CTLR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_CTLR are **UNDEFINED**.

**Attributes**

ICV_CTLR is a 32-bit register.

**Field descriptions**

The ICV_CTLR bit assignments are:

| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---------------------------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| RES0                           | ExtRange        | RSS             | A3V             | SEIS            | IDbits          | PRIbits         | RES0            | EOImode         | CBPR            |

**Bits [31:20]**

Reserved, RES0.

**ExtRange, bit [19]**

Extended INTID range (read-only).

<table>
<thead>
<tr>
<th>ExtRange</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CPU interface does not support INTIDs in the range 1024..8191. Behaviour is <strong>UNPREDICTABLE</strong> if the IRI delivers an interrupt in the range 1024 to 8191 to the CPU interface.</td>
</tr>
<tr>
<td><strong>Note</strong></td>
<td>Arm strongly recommends that the IRI is not configured to deliver interrupts in this range to a PE that does not support them.</td>
</tr>
<tr>
<td>0b1</td>
<td>CPU interface supports INTIDs in the range 1024..8191. All INTIDs in the range 1024..8191 are treated as requiring deactivation.</td>
</tr>
</tbody>
</table>

ICV_CTLR.ExtRange is an alias of ICC_CTLR.ExtRange.

**RSS, bit [18]**

Range Selector Support. Possible values are:
<table>
<thead>
<tr>
<th>RSS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 15 are supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Targeted SGIs with affinity level 0 values of 0 - 255 are supported.</td>
</tr>
</tbody>
</table>

This bit is read-only.

**Bits [17:16]**

Reserved, RES0.

**A3V, bit [15]**

Affinity 3 Valid. Read-only and writes are ignored. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic only supports zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports non-zero values of Affinity 3 in SGI generation System registers.</td>
</tr>
</tbody>
</table>

**SEIS, bit [14]**

SEI Support. Read-only and writes are ignored. Indicates whether the virtual CPU interface supports local generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic does not support local generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports local generation of SEIs.</td>
</tr>
</tbody>
</table>

**IDbits, bits [13:11]**

Identifier bits. Read-only and writes are ignored. The number of virtual interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**PRIbits, bits [10:8]**

Priority bits. Read-only and writes are ignored. The number of priority bits implemented, minus one.

An implementation must implement at least 32 levels of physical priority (5 priority bits).

**Note**

This field always returns the number of priority bits implemented.

The division between group priority and subpriority is defined in the binary point registers ICV_BPR0 and ICV_BPR1.

**Bits [7:2]**

Reserved, RES0.

**EOImode, bit [1]**

Virtual EOI mode. Controls whether a write to an End of Interrupt register also deactivates the virtual interrupt:
<table>
<thead>
<tr>
<th>EOImode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICV_EOIR0 and ICV_EOIR1 provide both priority drop and interrupt deactivation functionality. Accesses to ICV_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICV_EOIR0 and ICV_EOIR1 provide priority drop functionality only. ICV_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CBPR, bit [0]**

Common Binary Point Register. Controls whether the same register is used for interrupt preemption of both virtual Group 0 and virtual Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ICV_BPR0 determines the preemption group for virtual Group 0 interrupts only. ICV_BPR1 determines the preemption group for virtual Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>ICV_BPR0 determines the preemption group for both virtual Group 0 and virtual Group 1 interrupts. Reads of ICV_BPR1 return ICV_BPR0 plus one, saturated to 0b111. Writes to ICV_BPR1 are ignored.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ICV_CTLR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>}} \ <\text{coproc}, \ \text{\#<opc1>}, \ <\text{Rt}, \ <\text{CRn}}, \ <\text{CRm}{, \ \text{\#<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH.HCR.TC == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
    return ICV_CTLR;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
    return ICV_CTLR;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
    return ICV_CTLR;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
    return ICV_CTLR;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
      UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
      UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
      UNDEFINED;
    else
      return ICC_CTLR_NS;
    end if
  elseif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      return ICC_CTLR_S;
    end if
  end if
else
    return ICC_CTLR_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR.TC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        ICV_CTLR = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        ICV_CTLR = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        ICV_CTLR = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        ICV_CTLR = R[t];
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) then
        ICC_CTLR_NS = R[t];
    else
        ICC_CTLR = R[t];
    endif
else
    PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
            UNDEFINED;
        elsif ICC_HSRE.SRE == '0' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) then
        ICC_CTLR_NS = R[t];
    else
        ICC_CTLR = R[t];
    endif
else
    PSTATE.EL == EL3 then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            if SCR.NS == '0' then
                ICC_CTLR_S = R[t];
            else
                ICC_CTLR = R[t];
            endif
        endif
    else
        ICC_CTLR = R[t];
    endif
endif
else
    ICC_CTLR_NS = R[t];
ICV_DIR, Interrupt Controller Deactivate Virtual Interrupt Register

The ICV_DIR characteristics are:

**Purpose**

When interrupt priority drop is separated from interrupt deactivation, a write to this register deactivates the specified virtual interrupt.

**Configuration**

AArch32 System register ICV_DIR bits [31:0] performs the same function as AArch64 System register ICV_DIR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_DIR are UNDEFINED.

**Attributes**

ICV_DIR is a 32-bit register.

**Field descriptions**

The ICV_DIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>RESERVED, RES0</td>
</tr>
<tr>
<td>23-0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the virtual interrupt to be deactivated.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_DIR**

When EOImode == 0, writes are ignored. In systems supporting system error generation, an implementation might generate an SEI.

Accesses to this register use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap
    priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> ==
    '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TDIR == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TC == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        ICV_DIR = R[t];
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        ICV_DIR = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        ICV_DIR = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        ICV_DIR = R[t];
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        else
            ICC_DIR = R[t];
    if ICC_MSRE.SRE == '0' then
        ICC_DIR = R[t];
    elsif ICC_HSRE.SRE == '0' then
        ICC_DIR = R[t];
    elsif ICC_MSRE.SRE == '0' then
        ICC_DIR = R[t];
    else
        ICC_DIR = R[t];
ICV_EOIR0, Interrupt Controller Virtual End Of Interrupt Register 0

The ICV_EOIR0 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified virtual Group 0 interrupt.

**Configuration**

AArch32 System register ICV_EOIR0 performs the same function as AArch64 System register ICV_EOIR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_EOIR0 are UNDEFINED.

**Attributes**

ICV_EOIR0 is a 32-bit register.

**Field descriptions**

The ICV_EOIR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | INTID|

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICV_IAR0 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

If the ICV_CTLR.EOImode bit is 0, a write to this register drops the priority for the virtual interrupt, and also deactivates the virtual interrupt.

If the ICV_CTLR.EOImode bit is 1, a write to this register only drops the priority for the virtual interrupt. Software must write to ICV_DIR to deactivate the virtual interrupt.

**Accessing the ICV_EOIR0**

A write to this register must correspond to the most recent valid read by this vPE from a Virtual Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICV_IAR0, otherwise the system behavior is UNPREDICTABLE. A valid read is a read that returns a valid INTID that is not a special INTID.

Accesses to this register use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

| coproc | opc1 | CRn | CRm | opc2 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.FIQ == '1' then
        UNDEFINED;
elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
elsif EL2Enabled() & !ELUsingAArch32(EL2) & ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & ICH_HCR.TALL0 == '1' then
        AArch32.TakeHypTrapException(0x03);
elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
elsif ICC_MSRE.SRE == '0' then
    else
        ICC_EOIR0 = R[t];
elsel
        ICC_EOIR0 = R[t];
elsel
        ICC_EOIR0 = R[t];
elsel
    else
        ICC_EOIR0 = R[t];
elsel
else
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
elsel
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        UNDEFINED;
elsel
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
elsel
    ICC_EOIR0 = R[t];
elsel
else
    ICC_EOIR0 = R[t];
ICV_EOIR1, Interrupt Controller Virtual End Of Interrupt Register 1

The ICV_EOIR1 characteristics are:

**Purpose**

A PE writes to this register to inform the CPU interface that it has completed the processing of the specified virtual Group 1 interrupt.

**Configuration**

AArch32 System register ICV_EOIR1 performs the same function as AArch64 System register ICV_EOIR1_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_EOIR1 are **UNDEFINED**.

**Attributes**

ICV_EOIR1 is a 32-bit register.

**Field descriptions**

The ICV_EOIR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>24</td>
<td><strong>INTID</strong></td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID from the corresponding ICV_IAR1 access.

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are **RES0**.

If the ICV_CTLR.EOImode bit is 0, a write to this register drops the priority for the virtual interrupt, and also deactivates the virtual interrupt.

If the ICV_CTLR.EOImode bit is 1, a write to this register only drops the priority for the virtual interrupt. Software must write to ICV_DIR to deactivate the virtual interrupt.

**Accessing the ICV_EOIR1**

A write to this register must correspond to the most recent valid read by this vPE from a Virtual Interrupt Acknowledge Register, and must correspond to the INTID that was read from ICV_IAR1, otherwise the system behavior is **UNPREDICTABLE**. A valid read is a read that returns a valid INTID that is not a special INTID.

Accesses to this register use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

| coproc | opc1 | CRn | CRm | opc2 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.IMO == '1' then
        ICC_EOIR1 = R[t];
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR.IMO == '1' then
        ICC_EOIR1 = R[t];
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end
    else
        ICC_EOIR1 = R[t];
    end
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end
    else
        ICC_EOIR1 = R[t];
    end
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        ICC_EOIR1 = R[t];
    end
else
    ICC_EOIR1 = R[t];
ICV_HPPIR0, Interrupt Controller Virtual Highest Priority Pending Interrupt Register 0

The ICV_HPPIR0 characteristics are:

**Purpose**

Indicates the highest priority pending virtual Group 0 interrupt on the virtual CPU interface.

**Configuration**

AArch32 System register ICV_HPPIR0 performs the same function as AArch64 System register ICV_HPPIR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_HPPIR0 are UNDEFINED.

**Attributes**

ICV_HPPIR0 is a 32-bit register.

**Field descriptions**

The ICV_HPPIR0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
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<th>3</th>
<th>2</th>
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<tbody>
<tr>
<td></td>
<td>RES0</td>
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</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending virtual interrupt.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR_IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_HPPIR0**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.FIQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() & !ELUsingAArch32(EL2) &_index_12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif ICC_SRE.SRE == '0' then
  UNDEFINED;
elsif EL2Enabled() & !ELUsingAArch32(EL2) & ICH_HCR_EL2.TALL0 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & ELUsingAArch32(EL2) & ICH_HCR.TALL0 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif ICC_HSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
  if Halted() & EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.FIQ == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  else
    return ICC_HPPIR0;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
    UNDEFINED;
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
  if Halted() & EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
    if Halted() & EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    end if;
  else
    return ICC_HPPIR0;
else
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_HPPIR0;
  end if;
ICV_HPPR1, Interrupt Controller Virtual Highest Priority Pending Interrupt Register 1

The ICV_HPPR1 characteristics are:

**Purpose**

Indicates the highest priority pending virtual Group 1 interrupt on the virtual CPU interface.

**Configuration**

AArch32 System register ICV_HPPR1 performs the same function as AArch64 System register ICV_HPPR1_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_HPPR1 are UNDEFINED.

**Attributes**

ICV_HPPR1 is a 32-bit register.

**Field descriptions**

The ICV_HPPR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
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<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>INTID, bits [23:0]</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the highest priority pending virtual interrupt.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_HPPR1**

Accesses to this register use the following encodings:

MRC{<-q>}{<r>}, <coproc>, {#<opc1>}, <Rt>, <CRn>, <CRm>{, {#<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.TALL1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.TALL1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.IMO == '1' then
        return ICV_HPPIR1;
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR.IMO == '1' then
        return ICV_HPPIR1;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & PSTATE.M != M32_Monitor & SCR.IRQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elseif ICC_MSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        UNDEFINED;
else
    return ICC_HPPIR1;
else
    if PSTATE.EL == EL2 then
        if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
            UNDEFINED;
        elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
            UNDEFINED;
        elsif ICC_HSRE.SRE == '0' then
            UNDEFINED;
        elseif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.IRQ == '1' then
            if Halted() & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            endif
        elseif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.IRQ == '1' then
            if Halted() & EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            endif
        else
            return ICC_HPPIR1;
        else
            if PSTATE.EL == EL3 then
                if ICC_MSRE.SRE == '0' then
                    UNDEFINED;
                else
                    return ICC_HPPIR1;
                endif
            else
                return ICC_HPPIR1;
            endif
            return ICC_HPPIR1;
ICV_IAR0, Interrupt Controller Virtual Interrupt Acknowledge Register 0

The ICV_IAR0 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled virtual Group 0 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch32 System register ICV_IAR0 performs the same function as AArch64 System register ICV_IAR0_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_IAR0 are UNDEFINED.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_IAR0 is a 32-bit register.

**Field descriptions**

The ICV_IAR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| INTID | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled virtual interrupt.

This is the INTID of the highest priority pending virtual interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_IAR0**

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.FIQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL0 == '1' then
    return ICC_IAR0;
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_IAR0;
  endif
endif

if PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_IAR0;
  endif
endif

if PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_IAR0;
  endif
endif
ICV_IAR1, Interrupt Controller Virtual Interrupt Acknowledge Register 1

The ICV_IAR1 characteristics are:

**Purpose**

The PE reads this register to obtain the INTID of the signaled virtual Group 1 interrupt. This read acts as an acknowledge for the interrupt.

**Configuration**

AArch32 System register ICV_IAR1 performs the same function as AArch64 System register ICV_IAR1_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_IAR1 are **UNDEFINED**.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that reads of this register are self-synchronising when interrupts are masked by the PE (that is when PSTATE.{I,F} == {0,0}). This ensures that the effect of activating an interrupt on the signaling of interrupt exceptions is observed when a read of this register is architecturally executed so that no spurious interrupt exception occurs if interrupts are unmasked by an instruction immediately following the read. For more information, see ‘Observability of the effects of accesses to the GIC registers’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_IAR1 is a 32-bit register.

**Field descriptions**

The ICV_IAR1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>RES0</td>
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</tr>
<tr>
<td>INTID</td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled virtual interrupt.

This is the INTID of the highest priority pending virtual interrupt, if that interrupt is of sufficient priority for it to be signaled to the PE, and if it can be acknowledged.

If the highest priority pending interrupt is not observable, this field contains a special INTID to indicate the reason. This special INTID can take the value 1023 only. For more information, see ‘Special INTIDs’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field has either 16 or 24 bits implemented. The number of implemented bits can be found in ICV_CTLR.IDbits. If only 16 bits are implemented, bits [23:16] of this register are RES0.

**Accessing the ICV_IAR1**

Accesses to this register use the following encodings:
MRC{{<c>}}{<q>}{coproc}, {#}{opc1}, <Rt>, <CRn>, <CRm>{, {#}{opc2}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
  return ICC_IAR1;
elsif ICC_HSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  elsif Halted() && SCR.IRQ == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return ICC_IAR1;
elsif ICC_MSRE.SRE == '0' then
  UNDEFINED;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
  if Halted() && SCR.IRQ == '1' then
    UNDEFINED;
else
  return ICC_IAR1;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
else
  return ICC_IAR1;
ICV_IGRPEN0, Interrupt Controller Virtual Interrupt Group 0 Enable register

The ICV_IGRPEN0 characteristics are:

Purpose

Controls whether virtual Group 0 interrupts are enabled or not.

Configuration

AArch32 System register ICV_IGRPEN0 bits [31:0] are architecturally mapped to AArch64 System register ICV_IGRPEN0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_IGRPEN0 are UNDEFINED.

Attributes

ICV_IGRPEN0 is a 32-bit register.

Field descriptions

The ICV_IGRPEN0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RES0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

Enable, bit [0]

Enables virtual Group 0 interrupts.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Accessing the ICV_IGRPEN0

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & ICH_HCR_EL2.TALL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & ICH_HCR.TALL0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    else
        return ICC_IGRPEN0;
    end if
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        UNDEFINED;
    elsif Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & SCR_EL3.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif HaveEL(EL3) & ELUsingAArch32(EL3) & SCR.FIQ == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if
    else
        return ICC_IGRPEN0;
    end if
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_IGRPEN0;
    end if
else
    return ICC_IGRPEN0;
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
  UNDEFINED;
else if ICC_SRE.SRE == '0' then
  UNDEFINED;
else if ICC_SRE.SRE == '0' then
  ICV_IGRPEN0 = R[t];
else
  ICC_IGRPEN0 = R[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR_EL3.FIQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.FIQ == '1' then
    UNDEFINED;
  else if ICC_HSRE.SRE == '0' then
    UNDEFINED;
else if ICC_HSRE.SRE == '0' then
  ICV_IGRPEN0 = R[t];
else
  ICC_IGRPEN0 = R[t];
else if ICC_MSRE.SRE == '0' then
  UNDEFINED;
else
  ICC_IGRPEN0 = R[t];
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
else
  ICC_IGRPEN0 = R[t];
ICV_IGRPEN1, Interrupt Controller Virtual Interrupt Group 1 Enable register

The ICV_IGRPEN1 characteristics are:

**Purpose**

Controls whether virtual Group 1 interrupts are enabled for the current Security state.

**Configuration**

AArch32 System register ICV_IGRPEN1 bits [31:0] are architecturally mapped to AArch64 System register ICV_IGRPEN1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_IGRPEN1 are UNDEFINED.

**Attributes**

ICV_IGRPEN1 is a 32-bit register.

**Field descriptions**

The ICV_IGRPEN1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>Enable</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Enable, bit [0]**

Enables virtual Group 1 interrupts.

<table>
<thead>
<tr>
<th>Enable</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the ICV_IGRPEN1**

Accesses to this register use the following encodings:

MRC{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_SRE.SRE == '0' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TALL1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR.TALL1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif ICC_HSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  elsif HaveEL(EL3) then
    return ICC_IGRPEN1_NS;
  else
    return ICC_IGRPEN1;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    UNDEFINED;
  elsif ICC_MSRE.SRE == '0' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  elsif HaveEL(EL3) then
    return ICC_IGRPEN1_NS;
  else
    return ICC_IGRPEN1;
  endif
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      return ICC_IGRPEN1_S;
    else
      return ICC_IGRPEN1_NS;
    endif
  endif
MCR\{<c>\}{<q>\} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm}{, {#}<opc2>\}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.IRQ == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif ICC_SRE.SRE == '0' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        ICC_IGRPEN1 = R[t];
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) && SCR.IRQ == '1' then
        ICC_IGRPEN1_NS = R[t];
    else
        ICC_IGRPEN1 = R[t];
    endif
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.IRQ == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        endif
    elsif HaveEL(EL3) && SCR.IRQ == '1' then
        ICC_IGRPEN1_NS = R[t];
    else
        ICC_IGRPEN1 = R[t];
    endif
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            ICC_IGRPEN1_S = R[t];
        else
            ICC_IGRPEN1_NS = R[t];
        endif
    endif
ICV_IGRPEN1, Interrupt Controller Virtual Interrupt Group 1 Enable register
ICV_PMR, Interrupt Controller Virtual Interrupt Priority Mask Register

The ICV_PMR characteristics are:

**Purpose**

Provides a virtual interrupt priority filter. Only virtual interrupts with a higher priority than the value in this register are signaled to the PE.

**Configuration**

AArch32 System register ICV_PMR bits [31:0] are architecturally mapped to AArch64 System register ICV_PMR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_PMR are UNDEFINED.

To allow software to ensure appropriate observability of actions initiated by GIC register accesses, the PE and CPU interface logic must ensure that writes to this register are self-synchronising. This ensures that no interrupts below the written PMR value will be taken after a write to this register is architecturally executed. For more information, see 'Observability of the effects of accesses to the GIC registers' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

ICV_PMR is a 32-bit register.

**Field descriptions**

The ICV_PMR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The priority mask level for the virtual CPU interface. If the priority of a virtual interrupt is higher than the value indicated by this field, the interface signals the virtual interrupt to the PE.

The possible priority field values are as follows:

<table>
<thead>
<tr>
<th>Implemented priority bits</th>
<th>Possible priority field values</th>
<th>Number of priority levels</th>
</tr>
</thead>
<tbody>
<tr>
<td>[7:0]</td>
<td>0x00-0xFFFF (0-255), all values</td>
<td>256</td>
</tr>
<tr>
<td>[7:1]</td>
<td>0x00-0xFE (0-254), even values only</td>
<td>128</td>
</tr>
<tr>
<td>[7:2]</td>
<td>0x00-0xFC (0-252), in steps of 4</td>
<td>64</td>
</tr>
<tr>
<td>[7:3]</td>
<td>0x00-0xF8 (0-248), in steps of 8</td>
<td>32</td>
</tr>
<tr>
<td>[7:4]</td>
<td>0x00-0xF0 (0-240), in steps of 16</td>
<td>16</td>
</tr>
</tbody>
</table>
Unimplemented priority bits are RAZ/WI.

On a Warm reset, this field resets to 0.

**Accessing the ICV_PMR**

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\}{<q>} \ <\text{coproc}>, \ {#}<\text{opc1}>, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}>({#}<\text{opc2}>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        return ICV_PMR;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
        return ICV_PMR;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
        return ICV_PMR;
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
        return ICV_PMR;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        return ICC_PMR;
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch32.TakeMonitorTrapException();
        end if;
    else
        return ICC_PMR;
    end if;
elsif PSTATE.EL == EL3 then
    if ICC_MSRE.SRE == '0' then
        UNDEFINED;
    else
        return ICC_PMR;
    end if;
MCR\{<c>\}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0100</td>
<td>0b0110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
        ICV_PMR = R[t];
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ICH_HCR_EL2.TC == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR.<IRQ,FIQ> == '11' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
            UNDEFINED;
        elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
            UNDEFINED;
        elsif ICC_HSRE.SRE == '0' then
            UNDEFINED;
        elsif ICC_MSRE.SRE == '0' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch32.SystemAccessTrap(EL3, 0x03);
            end if
        elsif ICC_MSRE.SRE == '0' then
            if Halted() && SCR.<IRQ,FIQ> == '11' then
                UNDEFINED;
            else
                AArch32.TakeMonitorTrapException();
            end if
        else
            ICC_PMR = R[t];
        end if
    elsif ICC_HSRE.SRE == '0' then
        UNDEFINED;
    elsif ICC_MSRE.SRE == '0' then
        if ICC_MSRE.SRE == '0' then
            UNDEFINED;
        else
            ICC_PMR = R[t];
        end if
    else
        ICC_PMR = R[t];
    end if

ICV_RPR, Interrupt Controller Virtual Running Priority Register

The ICV_RPR characteristics are:

**Purpose**

Indicates the Running priority of the virtual CPU interface.

**Configuration**

AArch32 System register ICV_RPR performs the same function as AArch64 System register ICV_RPR_EL1.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ICV_RPR are UNDEFINED.

**Attributes**

ICV_RPR is a 32-bit register.

**Field descriptions**

The ICV_RPR bit assignments are:

|   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|
|   | RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The current running priority on the virtual CPU interface. This is the group priority of the current active virtual interrupt.

The priority returned is the group priority as if the BPR for the current Exception level and Security state was set to the minimum value of BPR for the number of implemented priority bits.

**Note**

If 8 bits of priority are implemented the group priority is bits[7:1] of the priority.

**Accessing the ICV_RPR**

If there are no active interrupts on the virtual CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

Software cannot determine the number of implemented priority bits from a read of this register.

Accesses to this register use the following encodings:
ICV_RPR, Interrupt Controller Virtual Running Priority Register

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b1011</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  endif
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.FMO == '1' then
  return ICV_RPR;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.IMO == '1' then
  return ICV_RPR;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FMO == '1' then
  return ICV_RPR;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.IMO == '1' then
  return ICV_RPR;
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  endif
elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SCR.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif
else
  return ICC_RPR;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && !ELUsingAArch32(EL3) && SCR_EL3.<IRQ,FIQ> == '11' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1"' && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  endif
elsif Halted() && ELUsingAArch32(EL3) && SCR.<IRQ,FIQ> == '11' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch32.TakeMonitorTrapException();
  endif
else
  return ICC_RPR;
elsif PSTATE.EL == EL3 then
  if ICC_MSRE.SRE == '0' then
    UNDEFINED;
  else
    return ICC_RPR;
else
  return ICC_RPR;
The ID_AFR0 characteristics are:

**Purpose**

Provides information about the IMPLEMENTATION DEFINED features of the PE in AArch32 state.

Must be interpreted with the Main ID Register, MIDR.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_AFR0 bits [31:0] are architecturally mapped to AArch64 System register ID_AFR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_AFR0 are UNDEFINED.

**Attributes**

ID_AFR0 is a 32-bit register.

**Field descriptions**

The ID_AFR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED |

**Bits [31:16]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [15:12]**

IMPLEMENTATION DEFINED.

**IMPLEMENTATION DEFINED, bits [11:8]**

IMPLEMENTATION DEFINED.

**IMPLEMENTATION DEFINED, bits [7:4]**

IMPLEMENTATION DEFINED.

**IMPLEMENTATION DEFINED, bits [3:0]**

IMPLEMENTATION DEFINED.
Accessing the ID_AFR0

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc}\},\ {#}\<\text{opc1}\>,\ <\text{Rt}\>,\ <\text{CRn}\>,\ <\text{CRm}\}{,\ {#}\<\text{opc2}\>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b011</td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_AFR0;
    endif
else
    return ID_AFR0;
endif
```

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**ID_DFR0, Debug Feature Register 0**

The ID_DFR0 characteristics are:

**Purpose**

Provides top level information about the debug system in AArch32 state.

Must be interpreted with the Main ID Register, **MIDR**.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_DFR0 bits [31:0] are architecturally mapped to AArch64 System register **ID_DFR0_EL1[31:0]**.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_DFR0 are **UNDEFINED**.

**Attributes**

ID_DFR0 is a 32-bit register.

**Field descriptions**

The ID_DFR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TraceFilt | PerfMon | MProfDbg | MMapTrc | CopTrc | MMapDbg | CopSDbg | CopDbg |

**TraceFilt, bits [31:28]**

Armv8.4 Self-hosted Trace Extension version. Defined values are:

<table>
<thead>
<tr>
<th>TraceFilt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Armv8.4 Self-hosted Trace Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Armv8.4 Self-hosted Trace Extension implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TRF implements the functionality added by the value 0b0001.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

**PerfMon, bits [27:24]**

Performance Monitors Extension version.

This field does not follow the standard ID scheme, but uses the alternative ID scheme described in 'Alternative ID scheme used for the Performance Monitors Extension version'.

Defined values are:
<table>
<thead>
<tr>
<th>PerfMon</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Performance Monitors Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Performance Monitors Extension, PMUv1 implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Performance Monitors Extension, PMUv2 implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Performance Monitors Extension, PMUv3 implemented.</td>
</tr>
<tr>
<td>0b0100</td>
<td>PMUv3 for Armv8.1. As 0b0011, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• Extended 16-bit PMEVTYPER&lt;n&gt;.evtCount field.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the HDCR, HPMD control bit.</td>
</tr>
<tr>
<td>0b0101</td>
<td>PMUv3 for Armv8.4. As 0b0100, and also includes support for the PMMIR register.</td>
</tr>
<tr>
<td>0b0110</td>
<td>PMUv3 for Armv8.5. As 0b0101, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• 64-bit event counters.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the HDCR, HCCD control bit.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the SDCR, SCCD control bit.</td>
</tr>
<tr>
<td>0b0111</td>
<td>PMUv3 for Armv8.7. As 0b0110, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• The PMCR, FZO and, if EL2 is implemented, HDCR, HPMFZO control bits.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented and using AArch64, the MDCR_EL3, {MPMX, MCCD} control bits.</td>
</tr>
<tr>
<td>0b1111</td>
<td>IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. Arm does not recommend this value for new implementations.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PMUv3 implements the functionality identified by the value 0b0011.

FEAT_PMUv3p1 implements the functionality identified by the value 0b0100.

FEAT_PMUv3p4 implements the functionality identified by the value 0b0101.

FEAT_PMUv3p5 implements the functionality identified by the value 0b0110.

FEAT_PMUv3p7 implements the functionality identified by the value 0b0111.

In any Armv8 implementation, the values 0b0001 and 0b0010 are not permitted.

From Armv8.1, if FEAT_PMUv3 is implemented, the value 0b0011 is not permitted.

From Armv8.4, if FEAT_PMUv3 is implemented, the value 0b0100 is not permitted.

From Armv8.5, if FEAT_PMUv3 is implemented, the value 0b0101 is not permitted.

From Armv8.7, if FEAT_PMUv3 is implemented, the value 0b0110 is not permitted.

**Note**

In Armv7, the value 0b0000 can mean that PMUv1 is implemented. PMUv1 is not permitted in an Armv8 implementation.

**MProfDbg, bits [23:20]**

M Profile Debug. Support for memory-mapped debug model for M profile processors. Defined values are:

<table>
<thead>
<tr>
<th>MProfDbg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for M profile Debug architecture, with memory-mapped access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.
**MMAPTrc, bits [19:16]**

Memory Mapped Trace. Support for memory-mapped trace model. Defined values are:

<table>
<thead>
<tr>
<th>MMapTrc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Arm trace architecture, with memory-mapped access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

See the ETM Architecture Specification for more information.

**CopTrc, bits [15:12]**

Support for System registers-based trace model, using registers in the coproc == 0b1110 encoding space. Defined values are:

<table>
<thead>
<tr>
<th>CopTrc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Arm trace architecture, with System registers access.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

See the ETM Architecture Specification for more information.

**MMapDbg, bits [11:8]**

Memory Mapped Debug. Support for v7 memory-mapped debug model, for A and R profile processors.

In Armv8-A, this field is RES0.

The optional memory map defined by Armv8 is not compatible with Armv7.

**CopSDbg, bits [7:4]**

Support for a System registers-based Secure debug model, using registers in the coproc = 0b1110 encoding space, for an A profile processor that includes EL3.

If EL3 is not implemented and the implemented Security state is Non-secure state, this field is RES0. Otherwise, this field reads the same as bits [3:0].

**CopDbg, bits [3:0]**

Support for System registers-based debug model, using registers in the coproc == 0b1110 encoding space, for A and R profile processors. Defined values are:
All other values are reserved.

FEAT_Debugv8p2 adds the functionality identified by the value 0b1000.

FEAT_Debugv8p4 adds the functionality identified by the value 0b1001.

In Armv8.0, the only permitted value is 0b0110.

In Armv8.1, the only permitted value is 0b0111.

In Armv8.2, the only permitted value is 0b1000.

From Armv8.4, the only permitted value is 0b1001.

### Accessing the ID_DFR0

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ID_DFR0;
  end if;
elsif PSTATE.EL == EL2 then
  return ID_DFR0;
elsif PSTATE.EL == EL3 then
  return ID_DFR0;
```
The ID_DFR1 characteristics are:

**Purpose**

Provides top level information about the debug system in AArch32.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_DFR1 bits [31:0] are architecturally mapped to AArch64 System register ID_DFR1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_DFR1 are UNDEFINED.

**Note**

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_DFR1 is a 32-bit register.

**Field descriptions**

The ID_DFR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MTPMU |

**Bits [31:4]**

Reserved, RES0.

**MTPMU, bits [3:0]**

Multi-threaded PMU extension. Defined values are:

<table>
<thead>
<tr>
<th>MTPMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, it is IMPLEMENTATION DEFINED whether PMEVTYPER&lt;n&gt;.MT are read/write or RES0.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_MTPMU and FEAT_PMUv3 implemented. PMEVTYPER&lt;n&gt;.MT are read/write. When FEAT_MTPMU is disabled, the Effective values of PMEVTYPER&lt;n&gt;.MT are 0.</td>
</tr>
<tr>
<td>0b1111</td>
<td>FEAT_MTPMU not implemented. If FEAT_PMUv3 is implemented, PMEVTYPER&lt;n&gt;.MT are RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_MTPMU implements the functionality identified by the value 0b0001.

From Armv8.6, in an implementation that includes FEAT_PMUv3, the value 0b0000 is not permitted.
In an implementation that does not include FEAT_PMUv3, the value 0b0001 is not permitted.

**Accessing the ID_DFR1**

Accesses to this register use the following encodings:

\[
\text{MRC}\{c\}\{q\} \langle\text{coproc}\rangle, \{\#\langle\text{opc1}\rangle, \langle\text{Rt}\rangle, \langle\text{CRn}\rangle, \langle\text{CRm}\rangle, \{\#\langle\text{opc2}\rangle}\}
\]

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```python
if PSTATE.EL == EL0 then
    UNDEFINED;
elif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
elif EL2Enabled() && !ELUsingAArch32(EL2) && (!IsZero(ID_DFR1) || boolean IMPLEMENTATION_DEFINED "ID_DFR1 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() && ELUsingAArch32(EL2) && (!IsZero(ID_DFR1) || boolean IMPLEMENTATION_DEFINED "ID_DFR1 trapped by HCR.TID3") && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
else
    return ID_DFR1;
elif PSTATE.EL == EL2 then
    return ID_DFR1;
elif PSTATE.EL == EL3 then
    return ID_DFR1;
```

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The ID_ISAR0 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR1, ID_ISAR2, ID_ISAR3, ID_ISAR4, and ID_ISAR5.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR0 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR0 are UNDEFINED.

**Attributes**

ID_ISAR0 is a 32-bit register.

**Field descriptions**

The ID_ISAR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Divide | Debug | Coproc | CmpBranch | BitField | BitCount | Swap |

**Bits [31:28]**

Reserved, RES0.

**Divide, bits [27:24]**

Indicates the implemented Divide instructions. Defined values are:

<table>
<thead>
<tr>
<th>Divide</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds SDIV and UDIV in the T32 instruction set.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds SDIV and UDIV in the A32 instruction set.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**Debug, bits [23:20]**

Indicates the implemented Debug instructions. Defined values are:

<table>
<thead>
<tr>
<th>Debug</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds BKPT.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Coproc, bits [19:16]**

Indicates the implemented System register access instructions. Defined values are:

<table>
<thead>
<tr>
<th>Coproc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented, except for instructions separately attributed by the architecture to provide access to AArch32 System registers and System instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds generic CDP, LDC, MCR, MRC, and STC.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds generic CDP2, LDC2, MCR2, MRC2, and STC2.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds generic MCRR and MRRC.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds generic MCRR2 and MRRC2.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**CmpBranch, bits [15:12]**

Indicates the implemented combined Compare and Branch instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>CmpBranch</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds CBNZ and CBZ.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**BitField, bits [11:8]**

Indicates the implemented BitField instructions. Defined values are:

<table>
<thead>
<tr>
<th>BitField</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds BFC, BFI, SBFX, and UBFX.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**BitCount, bits [7:4]**

Indicates the implemented Bit Counting instructions. Defined values are:

<table>
<thead>
<tr>
<th>BitCount</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds CLZ.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Swap, bits [3:0]**

Indicates the implemented Swap instructions in the A32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>Swap</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds SWP and SWPB.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0000}.

**Accessing the ID_ISAR0**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2>}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_ISAR0;
    endif
elsif PSTATE.EL == EL2 then
    return ID_ISAR0;
elsif PSTATE.EL == EL3 then
    return ID_ISAR0;
ID_ISAR1, Instruction Set Attribute Register 1

The ID_ISAR1 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR2, ID_ISAR3, ID_ISAR4, and ID_ISAR5.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR1 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR1 are UNDEFINED.

**Attributes**

ID_ISAR1 is a 32-bit register.

**Field descriptions**

The ID_ISAR1 bit assignments are:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Jazelle | Interwork | Immediate | IfThen | Extend | Except_AR | Except | Endian |
```

**Jazelle, bits [31:28]**

Indicates the implemented Jazelle extension instructions. Defined values are:

<table>
<thead>
<tr>
<th>Jazelle</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No support for Jazelle.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the BXJ instruction, and the J bit in the PSR. This setting might indicate a trivial implementation of the Jazelle extension.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Interwork, bits [27:24]**

Indicates the implemented Interworking instructions. Defined values are:

<table>
<thead>
<tr>
<th>Interwork</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the BX instruction, and the T bit in the PSR.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the BLX instruction. PC loads have BX-like behavior.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and guarantees that data-processing instructions in the A32 instruction set with the PC as the destination and the S bit clear have BX-like behavior.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0011.

**Immediate, bits [23:20]**

Indicates the implemented data-processing instructions with long immediates. Defined values are:

<table>
<thead>
<tr>
<th>Immediate</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds:</td>
</tr>
<tr>
<td></td>
<td>• The MOVT instruction</td>
</tr>
<tr>
<td></td>
<td>• The MOV instruction encodings with zero-extended 16-bit immediates.</td>
</tr>
<tr>
<td></td>
<td>• The T32 ADD and SUB instruction encodings with zero-extended 12-bit immediates, and the other ADD, ADR, and SUB encodings cross-referenced by the pseudocode for those encodings.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**IfThen, bits [19:16]**

Indicates the implemented If-Then instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>IfThen</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the IT instructions, and the IT bits in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Extend, bits [15:12]**

Indicates the implemented Extend instructions. Defined values are:

<table>
<thead>
<tr>
<th>Extend</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No scalar sign-extend or zero-extend instructions are implemented, where scalar instructions means non-Advanced SIMD instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SXTB, SXTH, UXTB, and UXTH instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the SXTB16, SXTAB, SXTAB16, SXTAH, UXTB16, UXTAB, UXTAB16, and UXTAH instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**Except_AR, bits [11:8]**

Indicates the implemented A and R profile exception-handling instructions. Defined values are:

<table>
<thead>
<tr>
<th>Except_AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SRS and RFE instructions, and the A and R profile forms of the CPS instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Except, bits [7:4]**

Indicates the implemented exception-handling instructions in the A32 instruction set. Defined values are:
All other values are reserved.

In Armv8-A, the only permitted value is `0b0001`.

**Endian, bits [3:0]**

Indicates the implemented Endian instructions. Defined values are:

<table>
<thead>
<tr>
<th>Endian</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>0b0000</code></td>
<td>None implemented.</td>
</tr>
<tr>
<td><code>0b0001</code></td>
<td>Adds the SETEND instruction, and the E bit in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are `0b0000` and `0b0001`.

**Accessing the ID_ISAR1**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

```
<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>0b1111</code></td>
<td><code>0b000</code></td>
<td><code>0b0000</code></td>
<td><code>0b0010</code></td>
<td><code>0b001</code></td>
</tr>
</tbody>
</table>
```

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_ISAR1;
    endif
elsif PSTATE.EL == EL2 then
    return ID_ISAR1;
elsif PSTATE.EL == EL3 then
    return ID_ISAR1;
```

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**ID_ISAR2, Instruction Set Attribute Register 2**

The ID_ISAR2 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR3, ID_ISAR4, and ID_ISAR5.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR2 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR2_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR2 are UNDEFINED.

**Attributes**

ID_ISAR2 is a 32-bit register.

**Field descriptions**

The ID_ISAR2 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reversal</td>
<td>PSR_AR</td>
<td>MultU</td>
<td>MultS</td>
<td>Mult</td>
<td>MultiAccessInt</td>
<td>MemHint</td>
<td>LoadStore</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Reversal, bits [31:28]**

Indicates the implemented Reversal instructions. Defined values are:

<table>
<thead>
<tr>
<th>Reversal</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the REV, REV16, and REVSH instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the RBIT instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**PSR_AR, bits [27:24]**

Indicates the implemented A and R profile instructions to manipulate the PSR. Defined values are:

<table>
<thead>
<tr>
<th>PSR_AR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the MRS and MSR instructions, and the exception return forms of data-processing instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

The exception return forms of the data-processing instructions are:
In the A32 instruction set, data-processing instructions with the PC as the destination and the S bit set. These instructions might be affected by the WithShifts attribute.
In the T32 instruction set, the SUBS PC,LR,#N instruction.

**MultU, bits [23:20]**

Indicates the implemented advanced unsigned Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>MultU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the UMULL and UMLAL instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the UMAAL instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0010.

**MultS, bits [19:16]**

Indicates the implemented advanced signed Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>MultS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SMULL and SMLAL instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the SMLABB, SMLABT, SMLALBB, SMLALBT, SMLALTB, SMLALTT, SMLATB, SMLATT, SMLAWB, SMLAWT, SMLUBB, SMUBLT, SMULBT, SMULTB, SMULTT, SMULWB, and SMULWT instructions. Also adds the Q bit in the PSRs.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds the SMLAD, SMLADX, SMLALD, SMLALDX, SMLSD, SMLSDX, SMLSLD, SMLSLDX, SMMLA, SMMLAR, SMMLS, SMMLSR, SMMUL, SMMULR, SMUAD, SMUADX, SMUSD, and SMUSDX instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0011.

**Mult, bits [15:12]**

Indicates the implemented additional Multiply instructions. Defined values are:

<table>
<thead>
<tr>
<th>Mult</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No additional instructions implemented. This means only MUL is implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the MLA instruction.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the MLS instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0010.

**MultiAccessInt, bits [11:8]**

Indicates the support for interruptible multi-access instructions. Defined values are:

<table>
<thead>
<tr>
<th>MultiAccessInt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No support. This means the LDM and STM instructions are not interruptible.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LDM and STM instructions are restartable.</td>
</tr>
<tr>
<td>0b0010</td>
<td>LDM and STM instructions are continuable.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0000.
MemHint, bits [7:4]

Indicates the implemented Memory Hint instructions. Defined values are:

<table>
<thead>
<tr>
<th>MemHint</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the PLD instruction.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Adds the PLD instruction. (0b0001 and 0b0010 have identical effects.)</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001 (or 0b0010), and adds the PLI instruction.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds the PLDW instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0100.

LoadStore, bits [3:0]

Indicates the implemented additional load/store instructions. Defined values are:

<table>
<thead>
<tr>
<th>LoadStore</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No additional load/store instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the LDRD and STRD instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the Load Acquire (LDAB, LDAH, LDA, LDAEXB, LDAEXH, LDAEX, LDAEXD) and Store Release (STLB, STLH, STL, STLEXB, STLEXH, STLEX, STLEXD) instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

Accessing the ID_ISAR2

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{ coproc}, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b0100</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if \text{PSTATE.EL} == \text{EL0} then
    \text{UNDEFINED};
elsif \text{PSTATE.EL} == \text{EL1} then
    if \text{EL2Enabled()} && !\text{ELUsingAArch32(EL2)} && \text{HSTR_EL2.T0} == '1' then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HSTR.T0} == '1' then
        \text{AArch32.TakeHypTrapException(0x03)};
    elsif \text{EL2Enabled()} && !\text{ELUsingAArch32(EL2)} && \text{HCR_EL2.TID3} == '1' then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HCR.TID3} == '1' then
        \text{AArch32.TakeHypTrapException(0x03)};
    else
        return \text{ID_ISAR2};
    endif
elsif \text{PSTATE.EL} == \text{EL2} then
    return \text{ID_ISAR2};
elsif \text{PSTATE.EL} == \text{EL3} then
    return \text{ID_ISAR2};
ID_ISAR3, Instruction Set Attribute Register 3

The ID_ISAR3 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR4, and ID_ISAR5.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR3 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR3_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR3 are UNDEFINED.

**Attributes**

ID_ISAR3 is a 32-bit register.

**Field descriptions**

The ID_ISAR3 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| T32EE | TrueNOP | T32Copy | TabBranch | SynchPrim | SVC | SIMD | Saturate |

**T32EE, bits [31:28]**

Indicates the implemented T32EE instructions. Defined values are:

<table>
<thead>
<tr>
<th>T32EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the ENTERX and LEAVEX instructions, and modifies the load behavior to include null checking.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**TrueNOP, bits [27:24]**

Indicates the implemented true NOP instructions. Defined values are:

<table>
<thead>
<tr>
<th>TrueNOP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. This means there are no NOP instructions that do not have any register dependencies.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds true NOP instructions in both the T32 and A32 instruction sets. This also permits additional NOP-compatible hints.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.
T32Copy, bits [23:20]

Indicates the support for T32 non flag-setting MOV instructions. Defined values are:

<table>
<thead>
<tr>
<th>T32Copy</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported. This means that in the T32 instruction set, encoding T1 of the MOV (register) instruction does not support a copy from a low register to a low register.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for T32 instruction set encoding T1 of the MOV (register) instruction, copying from a low register to a low register.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

TabBranch, bits [19:16]

Indicates the implemented Table Branch instructions in the T32 instruction set. Defined values are:

<table>
<thead>
<tr>
<th>TabBranch</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the TBB and TBH instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

SynchPrim, bits [15:12]

Used in conjunction with ID_ISAR4.SynchPrim_frac to indicate the implemented Synchronization Primitive instructions. Defined values are:

<table>
<thead>
<tr>
<th>SynchPrim</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If SynchPrim_frac == 0b000, no Synchronization Primitives implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>If SynchPrim_frac == 0b000, adds the LDREX and STREX instructions. If SynchPrim_frac == 0b011, also adds the CLREX, LDREXB, STREXB, and STREXH instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>If SynchPrim_frac == 0b000, as for [0b001, 0b011] and also adds the LDREXD and STREXD instructions.</td>
</tr>
</tbody>
</table>

All other combinations of SynchPrim and SynchPrim_frac are reserved.

In Armv8-A, the only permitted value is 0b0010.

SVC, bits [11:8]

Indicates the implemented SVC instructions. Defined values are:

<table>
<thead>
<tr>
<th>SVC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SVC instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

SIMD, bits [7:4]

Indicates the implemented SIMD instructions. Defined values are:
### SIMD

<table>
<thead>
<tr>
<th>SIMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SSAT and USAT instructions, and the Q bit in the PSRs.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001, and adds the PKHTB, PKHTB, QADD16, QADD8, QASX, QSUB16, QSUB8, QSAX, SADD16, SADD8, SASX, SEL, SHADD16, SHADD8, SHASX, SHSUB16, SHSUB8, SHSAX, SSAT16, SSUB16, SSUB8, SSAX, SXTAB16, SXTB16, UADD16, UADD8, UAXS, UHADD16, UHADD8, UHASX, UHSUB16, UHSUB8, UHSAX, UQADD16, UQADD8, UQASX, UQSUB16, UQSUB8, UQSAX, USAD8, USADA8, USAT16, USUB16, USUB8, USAX, UXTAB16, and UXTB16 instructions. Also adds support for the GE[3:0] bits in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0011.

The SIMD field relates only to implemented instructions that perform SIMD operations on the general-purpose registers. In an implementation that supports floating-point and Advanced SIMD instructions, MVFR0, MVFR1, and MVFR2 give information about the implemented Advanced SIMD instructions.

### Saturate, bits [3:0]

Indicates the implemented Saturate instructions. Defined values are:

<table>
<thead>
<tr>
<th>Saturate</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. This means no non-Advanced SIMD saturate instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the QADD, QDADD, QDSUB, and QSUB instructions, and the Q bit in the PSRs.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

## Accessing the ID_ISAR3

Accesses to this register use the following encodings:

```c
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_ISAR3;
    elsif PSTATE.EL == EL2 then
        return ID_ISAR3;
    elsif PSTATE.EL == EL3 then
        return ID_ISAR3;
ID_ISAR4, Instruction Set Attribute Register 4

The ID_ISAR4 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, and ID_ISAR5.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR4 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR4_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR4 are UNDEFINED.

**Attributes**

ID_ISAR4 is a 32-bit register.

**Field descriptions**

The ID_ISAR4 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>SWP_frac</td>
<td>PSR_M</td>
<td>SynchPrim_frac</td>
<td>Barrier</td>
<td>SMC</td>
<td>Writeback</td>
<td>WithShifts</td>
<td>Unpriv</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**SWP_frac, bits [31:28]**

Indicates support for the memory system locking the bus for SWP or SWPB instructions. Defined values are:

<table>
<thead>
<tr>
<th>SWP_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SWP or SWPB instructions not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SWP or SWPB implemented but only in a uniprocessor context. SWP and SWPB do not guarantee whether memory accesses from other Requesters can come between the load memory access and the store memory access of the SWP or SWPB.</td>
</tr>
</tbody>
</table>

All other values are reserved. This field is valid only if ID_ISAR0.Swap is 0b0000.

In Armv8-A, the only permitted value is 0b0000.

**PSR_M, bits [27:24]**

Indicates the implemented M profile instructions to modify the PSRs. Defined values are:

<table>
<thead>
<tr>
<th>PSR_M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the M profile forms of the CPS, MRS, and MSR instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is 0b0000.

**SynchPrim_frac, bits [23:20]**

Used in conjunction with ID_ISAR3.SynchPrim to indicate the implemented Synchronization Primitive instructions. Possible values are:

<table>
<thead>
<tr>
<th>SynchPrim_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If SynchPrim == 0b0000, no Synchronization Primitives implemented. If SynchPrim == 0b0001, adds the LDREX and STREX instructions. If SynchPrim == 0b0010, also adds the CLREX, LDREXB, LDREXH, STREXB, STREXH, LDREXD, and STREXD instructions.</td>
</tr>
<tr>
<td>0b0011</td>
<td>If SynchPrim == 0b0001, adds the LDREX, STREX, CLREX, LDREXB, LDREXH, STREXB, and STREXH instructions.</td>
</tr>
</tbody>
</table>

All other combinations of SynchPrim and SynchPrim_frac are reserved.

In Armv8-A, the only permitted value is 0b0000.

**Barrier, bits [19:16]**

Indicates the implemented Barrier instructions in the A32 and T32 instruction sets. Defined values are:

<table>
<thead>
<tr>
<th>Barrier</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. Barrier operations are provided only as System instructions in the (coproc==0b1111) encoding space.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the DMB, DSB, and ISB barrier instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**SMC, bits [15:12]**

Indicates the implemented SMC instructions. Defined values are:

<table>
<thead>
<tr>
<th>SMC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the SMC instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Writeback, bits [11:8]**

Indicates the support for Writeback addressing modes. Defined values are:

<table>
<thead>
<tr>
<th>Writeback</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Basic support. Only the LDM, STM, PUSH, POP, SRS, and RFE instructions support writeback addressing modes. These instructions support all of their writeback addressing modes.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for all of the writeback addressing modes.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**WithShifts, bits [7:4]**

Indicates the support for instructions with shifts. Defined values are:
<table>
<thead>
<tr>
<th>WithShifts</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Nonzero shifts supported only in MOV and shift instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds support for shifts of loads and stores over the range LSL 0-3.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0001, and adds support for other constant shift options, both on load/store and other instructions.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds support for register-controlled shift options.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0100.

**Unpriv, bits [3:0]**

Indicates the implemented unprivileged instructions. Defined values are:

<table>
<thead>
<tr>
<th>Unpriv</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None implemented. No T variant instructions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Adds the LDRBT, LDRT, STRBT, and STRT instructions.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds the LDRHT, LDRSBT, LDRSHT, and STRHT instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

**Accessing the ID_ISAR4**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ID_ISAR4;
  elsif PSTATE.EL == EL2 then
    return ID_ISAR4;
elsif PSTATE.EL == EL3 then
  return ID_ISAR4;
```
**ID_ISAR5, Instruction Set Attribute Register 5**

The ID_ISAR5 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, and ID_ISAR4.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR5 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR5_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR5 are UNDEFINED.

**Attributes**

ID_ISAR5 is a 32-bit register.

**Field descriptions**

The ID_ISAR5 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VCMA | RDM | RES0 | CRC32 | SHA2 | SHA1 | AES | SEVL |

**VCMA, bits [31:28]**

Indicates AArch32 support for complex number addition and multiplication where numbers are stored in vectors. Defined values are:

<table>
<thead>
<tr>
<th>VCMA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The VCMLA and VCADD instructions are not implemented in AArch32.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The VCMLA and VCADD instructions are implemented in AArch32.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_FCMA implements the functionality identified by the value 0b0001.

From Armv8.3, the only permitted value is 0b0001.

**RDM, bits [27:24]**

Indicates support for the VQRDMLAH and VQRDMLSH instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>RDM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No VQRDMLAH and VQRDMLSH instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VQRDMLAH and VQRDMLSH instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RDM implements the functionality identified by the value 0b0001.
From Armv8.1, the only permitted value is 0b0001.

**Bits [23:20]**

Reserved, RES0.

**CRC32, bits [19:16]**

Indicates support for the CRC32 instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>CRC32</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No CRC32 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CRC32B, CRC32H, CRC32W, CRC32CB, CRC32CH, and CRC32CW instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.1, the only permitted value is 0b0001.

**SHA2, bits [15:12]**

Indicates support for the SHA2 instructions in AArch32 state.

<table>
<thead>
<tr>
<th>SHA2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA2 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SHA256H, SHA256H2, SHA256SU0, and SHA256SU1 implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**SHA1, bits [11:8]**

Indicates support for the SHA1 instructions are implemented in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>SHA1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No SHA1 instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SHA1C, SHA1P, SHA1M, SHA1H, SHA1SU0, and SHA1SU1 implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**AES, bits [7:4]**

Indicates support for the AES instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>AES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No AES instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AESE, AESD, AESMC, and AESIMC implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, plus VMULL (polynomial) instructions operating on 64-bit data quantities.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0010.

**SEVL, bits [3:0]**

Indicates support for the SEVL instruction in AArch32 state. Defined values are:
SEVL

<table>
<thead>
<tr>
<th>SEVL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SEVL is implemented as a NOP.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SEVL is implemented as Send Event Local.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Accessing the ID_ISAR5**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\}{, \{#<\text{opc2}>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if \(PSTATE.EL == EL0\) then
    UNDEFINED;
elsif \(PSTATE.EL == EL1\) then
    if \(EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HSTR.EL2.T0 == '1'\) then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif \(EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HSTR.T0 == '1'\) then
        AArch32.TakeHypTrapException(0x03);
    elsif \(EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HCR.EL2.TID3 == '1'\) then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif \(EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HCR.TID3 == '1'\) then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_ISAR5;
    endif
elsif \(PSTATE.EL == EL2\) then
    return ID ISAR5;
elsif \(PSTATE.EL == EL3\) then
    return ID_ISAR5;
The ID_ISAR6 characteristics are:

**Purpose**

Provides information about the instruction sets implemented by the PE in AArch32 state.

Must be interpreted with ID_ISAR0, ID_ISAR1, ID_ISAR2, ID_ISAR3, ID_ISAR4, and ID_ISAR5.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_ISAR6 bits [31:0] are architecturally mapped to AArch64 System register ID_ISAR6_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_ISAR6 are UNDEFINED.

**Note**

Prior to the introduction of the features described by this register, this register was unnamed and reserved, RES0 from EL1, EL2, and EL3.

**Attributes**

ID_ISAR6 is a 32-bit register.

**Field descriptions**

The ID_ISAR6 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | I8MM | BF16 | SPECRES | SB | FHM | DP | JSCVT |

**Bits [31:28]**

Reserved, RES0.

**I8MM, bits [27:24]**

Indicates support for Advanced SIMD and floating-point Int8 matrix multiplication instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>I8MM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Int8 matrix multiplication instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VSMMLA, VSUDOT, VUMMLA, VUSMMLA, and VUSDOT instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AA32I8MM implements the functionality identified by 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.
BF16, bits [23:20]

Indicates support for Advanced SIMD and floating-point BFloat16 instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>BF16</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>BFloat16 instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VCVT, VCVTB, VCVTT, VDOT, VFMAB, VFMAT, and VMMLA</td>
</tr>
<tr>
<td></td>
<td>instructions with BF16 operand or result types are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AA32BF16 implements the functionality identified by 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

SPECRES, bits [19:16]

Indicates support for Speculation invalidation instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>SPECRES</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>CFPRCTX, DVPRCTX, and CPPRCTX instructions are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>CFPRCTX, DVPRCTX, and CPPRCTX instructions are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8.5, the only permitted value is 0b0001.

SB, bits [15:12]

Indicates support for SB instruction in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>SB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SB instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SB instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

From Armv8.5, the only permitted value is 0b0001.

FHM, bits [11:8]

Indicates support for Advanced SIMD and floating-point VFMAL and VFMSL instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>FHM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>VFMAL and VMFSL instructions not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VFMAL and VMFSL instructions implemented.</td>
</tr>
</tbody>
</table>

FEAT_FHM implements the functionality identified by the value 0b0001.

DP, bits [7:4]

Indicates support for dot product instructions in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No dot product instructions implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>VUDOT and VSDOT instructions implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_DotProd implements the functionality identified by the value 0b0001.
**JSCVT, bits [3:0]**

Indicates support for the Javascript conversion instruction in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>JSCVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The VJCVT instruction is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The VJCVT instruction is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8.0, the only permitted value is 0b0000.

FEAT_JSCVT implements the functionality identified by 0b0001.

From Armv8.3, if Advanced SIMD or Floating-point is implemented, the only permitted value is 0b0001.

From Armv8.3, if Advanced SIMD or Floating-point is not implemented, the only permitted value is 0b0000.

**Accessing the ID_ISAR6**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && (!IsZero(ID_ISAR6) || boolean IMPLEMENTATION_DEFINED "ID_ISAR6 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && (!IsZero(ID_ISAR6) || boolean IMPLEMENTATION_DEFINED "ID_ISAR6 trapped by HCR.TID3") && HCR.TID3 == '1' then
    AArch32.TakeHypTrapException(0x03);
else
  return ID_ISAR6;
elsif PSTATE.EL == EL2 then
  return ID_ISAR6;
elsif PSTATE.EL == EL3 then
  return ID_ISAR6;
```
The ID_MMFR0 characteristics are:

### Purpose

Provides information about the implemented memory model and memory management support in AArch32 state. Must be interpreted with ID_MMFR1, ID_MMFR2, ID_MMFR3, and ID_MMFR4.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

### Configuration

AArch32 System register ID_MMFR0 bits [31:0] are architecturally mapped to AArch64 System register ID_MMFR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR0 are UNDEFINED.

### Attributes

ID_MMFR0 is a 32-bit register.

### Field descriptions

The ID_MMFR0 bit assignments are:

<table>
<thead>
<tr>
<th>InnerShr</th>
<th>FCSE</th>
<th>AuxReg</th>
<th>TCM</th>
<th>ShareLvl</th>
<th>OuterShr</th>
<th>PMSA</th>
<th>VMSA</th>
</tr>
</thead>
</table>

**InnerShr, bits [31:28]**

Innermost Shareability. Indicates the innermost shareability domain implemented. Defined values are:

<table>
<thead>
<tr>
<th>InnerShr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Implemented as Non-cacheable.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented with hardware coherency support.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Shareability ignored.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000, 0b0001, and 0b1111.

This field is valid only if the implementation supports two levels of shareability, as indicated by ID_MMFR0.ShareLvl having the value 0b0001.

When ID_MMFR0.ShareLvl is zero, this field is UNKNOWN.

**FCSE, bits [27:24]**

Indicates whether the implementation includes the FCSE. Defined values are:

<table>
<thead>
<tr>
<th>FCSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for FCSE.</td>
</tr>
</tbody>
</table>

All other values are reserved.
In Armv8-A, the only permitted value is \(0b0000\).

**AuxReg, bits [23:20]**

Auxiliary Registers. Indicates support for Auxiliary registers. Defined values are:

<table>
<thead>
<tr>
<th>AuxReg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Auxiliary Control Register only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for Auxiliary Fault Status Registers (AIFSR and ADFSR) and Auxiliary Control Register.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \(0b0010\).

**Note**

Accesses to unimplemented Auxiliary registers are **UNDEFINED**.

**TCM, bits [19:16]**

Indicates support for TCMs and associated DMAs. Defined values are:

<table>
<thead>
<tr>
<th>TCM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support is IMPLEMENTATION DEFINED. Armv7 requires this setting.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for TCM only, Armv6 implementation.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for TCM and DMA, Armv6 implementation.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \(0b0000\).

**ShareLvl, bits [15:12]**

Shareability Levels. Indicates the number of shareability levels implemented. Defined values are:

<table>
<thead>
<tr>
<th>ShareLvl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>One level of shareability implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Two levels of shareability implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \(0b0001\).

**OuterShr, bits [11:8]**

Outermost Shareability. Indicates the outermost shareability domain implemented. Defined values are:

<table>
<thead>
<tr>
<th>OuterShr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Implemented as Non-cacheable.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented with hardware coherency support.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Shareability ignored.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are \(0b0000\), \(0b0001\), and \(0b1111\).

**PMSA, bits [7:4]**

Indicates support for a PMSA. Defined values are:
### PMSA

<table>
<thead>
<tr>
<th>PMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for IMPLEMENTATION DEFINED PMSA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for PMSAv6, with a Cache Type Register implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for PMSAv7, with support for memory subsections. Armv7-R profile.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### VMSA, bits [3:0]

Indicates support for a VMSA. Defined values are:

<table>
<thead>
<tr>
<th>VMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for IMPLEMENTATION DEFINED VMSA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Support for VMSAv6, with Cache and TLB Type Registers implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Support for VMSAv7, with support for remapping and the Access flag. Armv7-A profile.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds support for the PXN bit in the Short-descriptor translation table format descriptors</td>
</tr>
<tr>
<td>0b0101</td>
<td>As for 0b0100, and adds support for the Long-descriptor translation table format.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0101.

### Accessing the ID_MMFR0

Accesses to this register use the following encodings:

\[
\text{MRC} \{<c>\}<q> <\text{coproc}>, \{#\}<\text{opc1}>\), <\text{Rt}>\), <\text{CRn}>\), <\text{CRm}>\}, \{#\}<\text{opc2}>\)}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ID_MMFR0;
  endif
elsif PSTATE.EL == EL2 then
  return ID_MMFR0;
elsif PSTATE.EL == EL3 then
  return ID_MMFR0;
ID_MMFR1, Memory Model Feature Register 1

The ID_MMFR1 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with [ID_MMFR0](#), [ID_MMFR2](#), [ID_MMFR3](#), and [ID_MMFR4](#).

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_MMFR1 bits [31:0] are architecturally mapped to AArch64 System register [ID_MMFR1_EL1][31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR1 are **UNDEFINED**.

**Attributes**

ID_MMFR1 is a 32-bit register.

**Field descriptions**

The ID_MMFR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| BPred | L1TstCln | L1Uni | L1Hvd | L1UniSW | L1HvdSW | L1UniVA | L1HvdVA |

**BPred, bits [31:28]**

Branch Predictor. Indicates branch predictor management requirements. Defined values are:

<table>
<thead>
<tr>
<th>BPred</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No branch predictor, or no MMU present. Implies a fixed MPU configuration.</td>
</tr>
</tbody>
</table>
| 0b0001 | Branch predictor requires flushing on:  
  • Enabling or disabling a stage of address translation.  
  • Writing new data to instruction locations.  
  • Writing new mappings to the translation tables.  
  • Changes to the TTBR0, TTBR1, or TTBCR registers.  
  • Changes to the ContextID or ASID, or to the FCSE ProcessID if this is supported. |
| 0b0010 | Branch predictor requires flushing on:  
  • Enabling or disabling a stage of address translation.  
  • Writing new data to instruction locations.  
  • Writing new mappings to the translation tables.  
  • Any change to the TTBR0, TTBR1, or TTBCR registers without a change to the corresponding ContextID or ASID, or FCSE ProcessID if this is supported. |
| 0b0011 | Branch predictor requires flushing only on writing new data to instruction locations. |
| 0b0100 | For execution correctness, branch predictor requires no flushing at any time. |

All other values are reserved.
In Armv8-A, the permitted values are 0b0010, 0b0011, or 0b0100. For values other than 0b0000 and 0b0100, the Arm Architecture Reference Manual, or the product documentation, might give more information about the required maintenance.

**L1TstCln, bits [27:24]**

Level 1 cache Test and Clean. Indicates the supported Level 1 data cache test and clean operations, for Harvard or unified cache implementations. Defined values are:

<table>
<thead>
<tr>
<th>L1TstCln</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 data cache test and clean operations are:</td>
</tr>
<tr>
<td></td>
<td>• Test and clean data cache.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Test, clean, and invalidate data cache.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**L1Uni, bits [23:20]**

Level 1 Unified cache. Indicates the supported entire Level 1 cache maintenance operations for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1Uni</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported entire Level 1 cache operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate cache, including branch predictor if appropriate.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor, if appropriate.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Clean cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**L1Hvd, bits [19:16]**

Level 1 Harvard cache. Indicates the supported entire Level 1 cache maintenance operations for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1Hvd</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported entire Level 1 cache operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache, including branch predictor if appropriate.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor, if appropriate.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache and instruction cache, including branch predictor if appropriate.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache, using a recursive model that uses the cache dirty status bit.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.
**L1UniSW, bits [15:12]**

Level 1 Unified cache by Set/Way. Indicates the supported Level 1 cache line maintenance operations by set/way, for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1UniSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 unified cache line maintenance operations by set/way are:</td>
</tr>
<tr>
<td></td>
<td>• Clean cache line by set/way.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate cache line by set/way.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate cache line by set/way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**L1HvdSW, bits [11:8]**

Level 1 Harvard cache by Set/Way. Indicates the supported Level 1 cache line maintenance operations by set/way, for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache line maintenance operations by set/way are:</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache line by set/way.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache line by set/way.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache line by set/way.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache line by set/way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**L1UniVA, bits [7:4]**

Level 1 Unified cache by Virtual Address. Indicates the supported Level 1 cache line maintenance operations by VA, for a unified cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1UniVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 unified cache line maintenance operations by VA are:</td>
</tr>
<tr>
<td></td>
<td>• Clean cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate cache line by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate cache line by VA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate branch predictor by VA, if branch predictor is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**L1HvdVA, bits [3:0]**

Level 1 Harvard cache by Virtual Address. Indicates the supported Level 1 cache line maintenance operations by VA, for a Harvard cache implementation. Defined values are:
None supported.

Supported Level 1 Harvard cache line maintenance operations by VA are:
- Clean data cache line by VA.
- Invalidate data cache line by VA.
- Clean and invalidate data cache line by VA.
- Clean instruction cache line by VA.

As for 0b0001, and adds:
- Invalidate branch predictor by VA, if branch predictor is implemented.

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**Accessing the ID_MMFR1**

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>\}{<q}> \text{ <coproc}, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2}\}} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_MMFR1;
    endif
elsif PSTATE.EL == EL2 then
    return ID_MMFR1;
elsif PSTATE.EL == EL3 then
    return ID_MMFR1;

ID_MMFR2, Memory Model Feature Register 2

The ID_MMFR2 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state. Must be interpreted with ID_MMFR0, ID_MMFR1, ID_MMFR3, and ID_MMFR4.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_MMFR2 bits [31:0] are architecturally mapped to AArch64 System register ID_MMFR2_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR2 are UNDEFINED.

**Attributes**

ID_MMFR2 is a 32-bit register.

**Field descriptions**

The ID_MMFR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| HWAccFlg | WFIStall | MemBarr | UniTLB | HvdTLB | L1HvdRng | L1HvdBG | L1HvdFG |

**HWAccFlg, bits [31:28]**

Hardware Access Flag. In earlier versions of the Arm Architecture, this field indicates support for a Hardware Access flag, as part of the VMSAv7 implementation. Defined values are:

<table>
<thead>
<tr>
<th>HWAccFlg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for VMSAv7 Access flag, updated in hardware.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**WFIStall, bits [27:24]**

Wait For Interrupt Stall. Indicates the support for Wait For Interrupt (WFI) stalling. Defined values are:

<table>
<thead>
<tr>
<th>WFIStall</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for WFI stalling.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.
MemBarr, bits [23:20]

Memory Barrier. Indicates the supported memory barrier System instructions in the (coproc == 1111) encoding space. Defined values are:

<table>
<thead>
<tr>
<th>MemBarr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported memory barrier System instructions are:</td>
</tr>
<tr>
<td></td>
<td>• Data Synchronization Barrier (DSB).</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Instruction Synchronization Barrier (ISB).</td>
</tr>
<tr>
<td></td>
<td>• Data Memory Barrier (DMB).</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

Arm deprecates the use of these operations. ID_ISAR4.BARRIER_INSTRS indicates the level of support for the preferred barrier instructions.

UniTLB, bits [19:16]

Unified TLB. Indicates the supported TLB maintenance operations, for a unified TLB implementation. Defined values are:

<table>
<thead>
<tr>
<th>UniTLB</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported unified TLB maintenance operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate all entries in the TLB.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate TLB entry by VA.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate TLB entries by ASID match.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction TLB and data TLB entries by VA All ASID. This is a shared unified TLB operation</td>
</tr>
<tr>
<td>0b0100</td>
<td>As for 0b0011, and adds:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate Hyp mode unified TLB entry by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate entire Non-secure PL1&amp;0 unified TLB.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate entire Hyp mode unified TLB.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As for 0b0100, and adds the following operations:</td>
</tr>
<tr>
<td></td>
<td>TLBIMVAALIS, TLBIMVAALIS, TLBIMVALHIS, TLBIMVAL, TLBIMVAAL, TLBIMVALH.</td>
</tr>
<tr>
<td>0b0110</td>
<td>As for 0b0101, and adds the following operations:</td>
</tr>
<tr>
<td></td>
<td>TLBIIPAS2IS, TLBIIPAS2LIS, TLBIIPAS2, TLBIIPAS2L.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0110.

HvdTLB, bits [15:12]

If the value of ID_MMFR2.UniTLB is not 0b0000, then the meaning of this field is IMPLEMENTATION DEFINED. Arm deprecates the use of this field by software.

L1HvdRng, bits [11:8]

Level 1 Harvard cache Range. Indicates the supported Level 1 cache maintenance range operations, for a Harvard cache implementation. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdRng</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported Level 1 Harvard cache maintenance range operations are:</td>
</tr>
<tr>
<td></td>
<td>• Invalidate data cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Invalidate instruction cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean data cache range by VA.</td>
</tr>
<tr>
<td></td>
<td>• Clean and invalidate data cache range by VA.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### L1HvdBG, bits [7:4]

Level 1 Harvard cache Background fetch. Indicates the supported Level 1 cache background fetch operations, for a Harvard cache implementation. When supported, background fetch operations are non-blocking operations. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
</tbody>
</table>
| 0b0001  | Supported Level 1 Harvard cache background fetch operations are:  
|         | • Fetch instruction cache range by VA.  
|         | • Fetch data cache range by VA. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### L1HvdFG, bits [3:0]

Level 1 Harvard cache Foreground fetch. Indicates the supported Level 1 cache foreground fetch operations, for a Harvard cache implementation. When supported, foreground fetch operations are blocking operations. Defined values are:

<table>
<thead>
<tr>
<th>L1HvdFG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
</tbody>
</table>
| 0b0001  | Supported Level 1 Harvard cache foreground fetch operations are:  
|         | • Fetch instruction cache range by VA.  
|         | • Fetch data cache range by VA. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### Accessing the ID_MMFR2

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>}\{<q}\} <\text{coproc}>, \{#}\text{opc1}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#}\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b110</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then  
  UNDEFINED;  
elsif PSTATE.EL == EL1 then  
  if EL2Enabled() & !ELUsingAArch32(EL2) & & HSTR_EL2.T0 == '1' then  
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);  
  elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HSTR.T0 == '1' then  
    AArch32.TakeHypTrapException(0x03);  
  elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TID3 == '1' then  
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);  
  elsif EL2Enabled() & & ELUsingAArch32(EL2) & & HCR.TID3 == '1' then  
    AArch32.TakeHypTrapException(0x03);  
  else  
    return ID_MMFR2;  
  endif  
elsif PSTATE.EL == EL2 then  
  return ID_MMFR2;  
elsif PSTATE.EL == EL3 then  
  return ID_MMFR2;
ID_MMFR3, Memory Model Feature Register 3

The ID_MMFR3 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with ID_MMFR0, ID_MMFR1, ID_MMFR2, and ID_MMFR4.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_MMFR3 bits [31:0] are architecturally mapped to AArch64 System register ID_MMFR3_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR3 are UNDEFINED.

**Attributes**

ID_MMFR3 is a 32-bit register.

**Field descriptions**

The ID_MMFR3 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Supersec | CMemSz | CohWalk | PAN | MaintBcst | BPMaint | CMaintSW | CMaintVA |

**Supersec, bits [31:28]**

Supersections. On a VMSA implementation, indicates whether Supersections are supported. Defined values are:

<table>
<thead>
<tr>
<th>Supersec</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Supersections supported.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Supersections not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b1111.

**CMemSz, bits [27:24]**

Cached Memory Size. Indicates the physical memory size supported by the caches. Defined values are:

<table>
<thead>
<tr>
<th>CMemSz</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>4GB, corresponding to a 32-bit physical address range.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64GB, corresponding to a 36-bit physical address range.</td>
</tr>
<tr>
<td>0b0010</td>
<td>1TB or more, corresponding to a 40-bit or larger physical address range.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000, 0b0001, and 0b0010.
CohWalk, bits [23:20]

Coherent Walk. Indicates whether Translation table updates require a clean to the Point of Unification. Defined values are:

<table>
<thead>
<tr>
<th>CohWalk</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Updates to the translation tables require a clean to the Point of Unification to ensure visibility by subsequent translation table walks.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Updates to the translation tables do not require a clean to the Point of Unification to ensure visibility by subsequent translation table walks.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

PAN, bits [19:16]

Privileged Access Never. Indicates support for the PAN bit in CPSR, SPSR, and DSPSR in AArch32 state. Defined values are:

<table>
<thead>
<tr>
<th>PAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PAN not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PAN supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>PAN supported and ATS1CPRP and ATS1CPWP instructions supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PAN implements the functionality identified by the value 0b0001.

FEAT_PAN2 implements the functionality added by the value 0b0010.

In Armv8.1, the value 0b0000 is not permitted.

From Armv8.2, the only permitted value is 0b0010.

MaintBcst, bits [15:12]

Maintenance Broadcast. Indicates whether Cache, TLB, and branch predictor operations are broadcast. Defined values are:

<table>
<thead>
<tr>
<th>MaintBcst</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Cache, TLB, and branch predictor operations only affect local structures.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Cache and branch predictor operations affect structures according to shareability and defined behavior of instructions. TLB operations only affect local structures.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Cache, TLB, and branch predictor operations affect structures according to shareability and defined behavior of instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

BPMaint, bits [11:8]

Branch Predictor Maintenance. Indicates the supported branch predictor maintenance operations in an implementation with hierarchical cache maintenance operations. Defined values are:
BPMaint

<table>
<thead>
<tr>
<th>BPMaint</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
</tbody>
</table>
| 0b0001  | Supported branch predictor maintenance operations are:  
|         | • Invalidate all branch predictors. |
| 0b0010  | As for 0b0001, and adds:  
|         | • Invalidate branch predictors by VA. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0010.

CMaintSW, bits [7:4]

Cache Maintenance by Set/Way. Indicates the supported cache maintenance operations by set/way, in an implementation with hierarchical caches. Defined values are:

<table>
<thead>
<tr>
<th>CMaintSW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
</tbody>
</table>
| 0b0001   | Supported hierarchical cache maintenance instructions by set/way are:  
|         | • Invalidate data cache by set/way.  
|         | • Clean data cache by set/way.  
|         | • Clean and invalidate data cache by set/way. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

In a unified cache implementation, the data cache maintenance operations apply to the unified caches.

CMaintVA, bits [3:0]

Cache Maintenance by Virtual Address. Indicates the supported cache maintenance operations by VA, in an implementation with hierarchical caches. Defined values are:

<table>
<thead>
<tr>
<th>CMaintVA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
</tbody>
</table>
| 0b0001   | Supported hierarchical cache maintenance operations by VA are:  
|         | • Invalidate data cache by VA.  
|         | • Clean data cache by VA.  
|         | • Clean and invalidate data cache by VA.  
|         | • Invalidate instruction cache by VA.  
|         | • Invalidate all instruction cache entries. |

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

In a unified cache implementation, data cache maintenance operations apply to the unified caches, and the instruction cache maintenance instructions are not implemented.

Accessing the ID_MMFR3

Accesses to this register use the following encodings:

\[
\text{MRC\{\langle c\rangle\{\langle q\rangle\} \langle coproc\rangle, \{\langle opc1\rangle, <Rt>, <CRn>, <CRm\rangle, \{\langle opc2\rangle\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_MMFR3;
    endif
elsif PSTATE.EL == EL2 then
    return ID_MMFR3;
elsif PSTATE.EL == EL3 then
    return ID_MMFR3;

The ID_MMFR4 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

Must be interpreted with ID_MMFR0, ID_MMFR1, ID_MMFR2, and ID_MMFR3.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_MMFR4 bits [31:0] are architecturally mapped to AArch64 System register ID_MMFR4_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR4 are UNDEFINED.

**Attributes**

ID_MMFR4 is a 32-bit register.

**Field descriptions**

The ID_MMFR4 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EVT | CCIDX | LSM | HPDS | CnP | XNX | AC2 | SpecSEI |

**EVT, bits [31:28]**

Enhanced Virtualization Traps. If EL2 is implemented, indicates support for the HCR2.\{TTLBIS, TOCU, TICAB, TID4\} traps. Defined values are:

<table>
<thead>
<tr>
<th>EVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>HCR2.{TTLBIS, TOCU, TICAB, TID4} traps are not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>HCR2.{TOCU, TICAB, TID4} traps are supported.</td>
</tr>
<tr>
<td></td>
<td>HCR2.TTLBIS trap is not supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>HCR2.{TTLBIS, TOCU, TICAB, TID4} traps are supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_EVT implements the functionality identified by the values 0b0001 and 0b0010.

If EL2 is not implemented supporting AArch32, the only permitted value is 0b0000.

In Armv8.2, the permitted values are 0b0000, 0b0001, and 0b0010.

From Armv8.5, the permitted values are:

- 0b0000 when EL2 is not implemented.
- 0b0010 when EL2 is implemented.

**CCIDX, bits [27:24]**

Support for use of the revised CCSIDR format and the presence of the CCSIDR2 is indicated. Defined values are:
CCIDX

<table>
<thead>
<tr>
<th>CCIDX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>32-bit format implemented for all levels of the CCSIDR, and the CCSIDR2 register is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>64-bit format implemented for all levels of the CCSIDR, and the CCSIDR2 register is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_CCIDX implements the functionality identified by 0b0001.

From Armv8.3, the permitted values are 0b0000 and 0b0001.

LSM, bits [23:20]

Indicates support for LSMAOE and nTLSMD bits in HSCTRL and SCTLR. Defined values are:

<table>
<thead>
<tr>
<th>LSM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>LSMAOE and nTLSMD bits not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>LSMAOE and nTLSMD bits supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_LSMAOC implements the functionality identified by the value 0b0001.

From Armv8.2, the permitted values are 0b0000 and 0b0001.

HPDS, bits [19:16]

Hierarchical permission disables bits in translation tables. Defined values are:

<table>
<thead>
<tr>
<th>HPDS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Disabling of hierarchical controls not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supports disabling of hierarchical controls using the TTBCR2, HPD0, TTBCR2, HPD1, and HTCR HPD bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for value 0b0001, and adds possible hardware allocation of bits[62:59] of the translation table descriptors from the final lookup level for IMPLEMENTATION DEFINED USE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AA32HPD implements the functionality identified by the value 0b0001.

FEAT_HPDS2 implements the functionality added by the value 0b010.

Note

The value 0b0000 implies that the encoding for TTBCR2 is UNDEFINED.

CnP, bits [15:12]

Common not Private translations. Defined values are:

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Common not Private translations not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Common not Private translations supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TTCNP implements the functionality identified by the value 0b0001.

From Armv8.2, the only permitted value is 0b0001.

XNX, bits [11:8]

Support for execute-never control distinction by Exception level at stage 2. Defined values are:
<table>
<thead>
<tr>
<th>XNX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Distinction between EL0 and EL1 execute-never control at stage 2 supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_XNX implements the functionality identified by the value 0b0001.

When FEAT_XNX is implemented:

- If all of the following conditions are true, it is IMPLEMENTATION DEFINED whether the value of ID_MMFR4.XNX is 0b0000 or 0b0001:
  - ID_AA64MMFR1_EL1.XNX ==1.
  - EL2 cannot use AArch32.
  - EL1 can use AArch32.
- If EL2 can use AArch32 then the only permitted value is 0b0001.

**AC2, bits [7:4]**

Indicates the extension of the ACTLR and HACTLR registers using ACTLR2 and HACTLR2. Defined values are:

<table>
<thead>
<tr>
<th>AC2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>ACTLR2 and HACTLR2 are not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>ACTLR2 and HACTLR2 are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.2, the only permitted value is 0b0001.

**SpecSEI, bits [3:0]**

Describes whether the PE can generate SError interrupt exceptions from speculative reads of memory, including speculative instruction fetches. The defined values of this field are:

<table>
<thead>
<tr>
<th>SpecSEI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The PE never generates an SError interrupt due to an External abort on a speculative read.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The PE might generate an SError interrupt due to an External abort on a speculative read.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Accessing the ID_MMFR4**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}  
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0010</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && (!IsZero(ID_MMFR4) || boolean IMPLEMENTATION_DEFINED "ID_MMFR4 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && (!IsZero(ID_MMFR4) || boolean IMPLEMENTATION_DEFINED "ID_MMFR4 trapped by HCR.TID3") && HCR.TID3 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ID_MMFR4;
  endif
elsif PSTATE.EL == EL2 then
  return ID_MMFR4;
elsif PSTATE.EL == EL3 then
  return ID_MMFR4;
The ID_MMFR5 characteristics are:

**Purpose**

Provides information about the implemented memory model and memory management support in AArch32 state.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_MMFR5 bits [31:0] are architecturally mapped to AArch64 System register ID_MMFR5_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_MMFR5 are UNDEFINED.

**Attributes**

ID_MMFR5 is a 32-bit register.

**Field descriptions**

The ID_MMFR5 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
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<tr>
<td>19</td>
<td></td>
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<tr>
<td>18</td>
<td></td>
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<tr>
<td>17</td>
<td></td>
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<tr>
<td>16</td>
<td></td>
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<tr>
<td>15</td>
<td></td>
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<tr>
<td>14</td>
<td></td>
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<tr>
<td>13</td>
<td></td>
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<tr>
<td>12</td>
<td></td>
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<tr>
<td>11</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, RES0.

**ETS, bits [3:0]**

Support for Enhanced Translation Synchronization. Defined values are:

<table>
<thead>
<tr>
<th>ETS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Enhanced Translation Synchronization is not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Enhanced Translation Synchronization is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ETS implements the functionality identified by the value 0b0001.

From Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.7, the only permitted value is 0b0001.

**Accessing the ID_MMFR5**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && (!IsZero(ID_MMFR5) || boolean IMPLEMENTATION_DEFINED "ID_MMFR5 trapped by HCR_EL2.TID3") && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && (!IsZero(ID_MMFR5) || boolean IMPLEMENTATION_DEFINED "ID_MMFR5 trapped by HCR.TID3") && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_MMFR5;
    end if;
elsif PSTATE.EL == EL2 then
    return ID_MMFR5;
elsif PSTATE.EL == EL3 then
    return ID_MMFR5;
The ID_PFR0 characteristics are:

**Purpose**

Gives top-level information about the instruction sets and other features supported by the PE in AArch32 state.

Must be interpreted with ID_PFR1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'

**Configuration**

AArch32 System register ID_PFR0 bits [31:0] are architecturally mapped to AArch64 System register ID_PFR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_PFR0 are UNDEFINED.

**Attributes**

ID_PFR0 is a 32-bit register.

**Field descriptions**

The ID_PFR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RAS | DIT | AMU | CSV2 | State3 | State2 | State1 | State0 |

**RAS, bits [31:28]**

RAS Extension version. Defined values are:

<table>
<thead>
<tr>
<th>RAS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No RAS Extension.</td>
</tr>
<tr>
<td>0b0001</td>
<td>RAS Extension present.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_RASv1p1 present. As 0b0001, and adds support for additional ERXMISC&lt;m&gt; System registers. Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ERR&lt;n&gt;STATUS and support for the optional RAS Timestamp Extension.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_RAS implements the functionality identified by the value 0b0001.

FEAT_RASv1p1 implements the functionality identified by the value 0b0010.

In Armv8.0 and Armv8.1, the permitted values are 0b0000 and 0b0001.

In Armv8.2, the only permitted value is 0b0001.

From Armv8.4, if FEAT_DoubleFault is implemented, the only permitted value is 0b0010.

From Armv8.4, when FEAT_DoubleFault is not implemented, and ERRIDR.NUM is 0, the permitted values are IMPLEMENTATION DEFINED 0b0001 or 0b010.
**Note**

When the value of this field is 0b0001, **ID_PFR2.RAS_frac** indicates whether **FEAT_RASv1p1** is implemented.

---

**DIT, bits [27:24]**

Data Independent Timing. Defined values are:

<table>
<thead>
<tr>
<th>DIT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>AArch32 does not guarantee constant execution time of any instructions.</td>
</tr>
<tr>
<td>0b0001</td>
<td>AArch32 provides the PSTATE.DIT mechanism to guarantee constant execution time of certain instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**FEAT_DIT** implements the functionality identified by the value 0b0001.

From Armv8.4, the only permitted value is 0b0001.

---

**AMU, bits [23:20]**

Indicates support for Activity Monitors Extension. Defined values are:

<table>
<thead>
<tr>
<th>AMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Activity Monitors Extension is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_AMUv1 is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_AMUv1p1 is implemented. As 0b0001 and adds support for virtualization of the activity monitor event counters.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**FEAT_AMUv1** implements the functionality identified by the value 0b0001.

**FEAT_AMUv1p1** implements the functionality identified by the value 0b0010.

In Armv8.0, the only permitted value is 0b0000.

In Armv8.4, the permitted values are 0b0000 and 0b0001.

From Armv8.6, the permitted values are 0b0000, 0b0001, and 0b0010.

---

**CSV2, bits [19:16]**

Speculative use of out of context branch targets. Defined values are:

<table>
<thead>
<tr>
<th>CSV2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>This Device does not disclose whether branch targets trained in one hardware described context can affect speculative execution in a different hardware described context.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Branch targets trained in one hardware described context can only affect speculative execution in a different hardware described context in a hard-to-determine way.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**FEAT_CSV2** implements the functionality identified by 0b0001.

From Armv8.5, the only permitted value is 0b0001.

---

**State3, bits [15:12]**

T32EE instruction set support. Defined values are:
### State3, Meaning

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>T32EE instruction set implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

### State2, bits [11:8]

Jazelle extension support. Defined values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Jazelle extension implemented, without clearing of JOSCR.CV on exception entry.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Jazelle extension implemented, with clearing of JOSCR.CV on exception entry.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

### State1, bits [7:4]

T32 instruction set support. Defined values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>T32 instruction set not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>T32 encodings before the introduction of Thumb-2 technology implemented:</td>
</tr>
<tr>
<td></td>
<td>• All instructions are 16-bit.</td>
</tr>
<tr>
<td></td>
<td>• A BL or BLX is a pair of 16-bit instructions</td>
</tr>
<tr>
<td></td>
<td>• 32-bit instructions other than BL and BLX cannot be encoded.</td>
</tr>
<tr>
<td>0b0011</td>
<td>T32 encodings after the introduction of Thumb-2 technology implemented, for all 16-bit and 32-bit T32 basic instructions.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0011.

### State0, bits [3:0]

A32 instruction set support. Defined values are:

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>A32 instruction set not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>A32 instruction set implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

## Accessing the ID_PFR0

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \ <\text{coproc}>{,\ <#<opc1>}, \ <\text{Rt}>}, \ <\text{CRn}>, \ <\text{CRm}>{,\ <#<opc2>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_PFR0;
    endif
elsif PSTATE.EL == EL2 then
    return ID_PFR0;
elsif PSTATE.EL == EL3 then
    return ID_PFR0;
ID_PFR1, Processor Feature Register 1

The ID_PFR1 characteristics are:

**Purpose**

Gives information about the AArch32 programmers' model.

Must be interpreted with ID_PFR0.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_PFR1 bits [31:0] are architecturally mapped to AArch64 System register ID_PFR1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_PFR1 are UNDEFINED.

**Attributes**

ID_PFR1 is a 32-bit register.

**Field descriptions**

The ID_PFR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| GIC | Virt_frac | Sec_frac | GenTimer | Virtualization | MProgMod | Security | ProgMod |

**GIC, bits [31:28]**

System register GIC CPU interface. Defined values are:

<table>
<thead>
<tr>
<th>GIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000</td>
<td>GIC CPU interface system registers not implemented.</td>
</tr>
<tr>
<td>0b00001</td>
<td>System register interface to versions 3.0 and 4.0 of the GIC</td>
</tr>
<tr>
<td></td>
<td>CPU interface is supported.</td>
</tr>
<tr>
<td>0b0011</td>
<td>System register interface to version 4.1 of the GIC CPU</td>
</tr>
<tr>
<td></td>
<td>interface is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Virt_frac, bits [27:24]**

Virtualization fractional field. When the Virtualization field is 0b0000, determines the support for features from the ARMv7 Virtualization Extensions. Defined values are:
### Virt_frac, bits [0:0]

<table>
<thead>
<tr>
<th>Virt_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No features from the ARMv7 Virtualization Extensions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The following features of the ARMv7 Virtualization Extensions are implemented:</td>
</tr>
<tr>
<td></td>
<td>• The <code>SCR</code>.SIF bit, if EL3 is implemented.</td>
</tr>
<tr>
<td></td>
<td>• The modifications to the <code>SCR</code>.AW and <code>SCR</code>.FW bits described in the Virtualization Extensions, if EL3 is implemented.</td>
</tr>
<tr>
<td></td>
<td>• The MSR (banked register) and MRS (banked register) instructions.</td>
</tr>
<tr>
<td></td>
<td>• The ERET instruction.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL2 is implemented.
- 0b0001 when EL2 is not implemented.

This field is only valid when the value of ID_PFR1.Virtualization is 0, otherwise it holds the value 0b0000.

**Note**

The ID_ISAR registers do not identify whether the instructions added by the ARMv7 Virtualization Extensions are implemented.

### Sec_frac, bits [23:20]

Security fractional field. When the Security field is 0b0000, determines the support for features from the ARMv7 Security Extensions. Defined values are:

<table>
<thead>
<tr>
<th>Sec_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No features from the ARMv7 Security Extensions are implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>The following features from the ARMv7 Security Extensions are implemented:</td>
</tr>
<tr>
<td></td>
<td>• The VBAR register.</td>
</tr>
<tr>
<td></td>
<td>• The <code>TTBCR</code>.PD0 and <code>TTBCR</code>.PD1 bits.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, plus the ability to access Secure or Non-secure physical memory is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 when EL3 is implemented.
- 0b0001 or 0b0010 when EL3 is not implemented.

This field is only valid when the value of ID_PFR1.Security is 0, otherwise it holds the value 0b0000.

### GenTimer, bits [19:16]

Generic Timer support. Defined values are:

<table>
<thead>
<tr>
<th>GenTimer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Generic Timer is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Generic Timer is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Generic Timer is implemented, and also includes support for <code>CNTHCTL</code>.EVNTIS and <code>CNTKCTL</code>.EVNTIS fields, and <code>CNTPCTSS</code> and <code>CNTVCTSS</code> counter views.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_ECV implements the functionality identified by the value 0b0010.

In Armv8.0 to Armv8.4, the only permitted value is 0b0001.
From Armv8.6, the only permitted value is \texttt{0b0010}.

**Virtualization, bits [15:12]**

Virtualization support. Defined values are:

<table>
<thead>
<tr>
<th>Virtualization</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0000}</td>
<td>EL2, Hyp mode, and the HVC instruction not implemented.</td>
</tr>
<tr>
<td>\texttt{0b0001}</td>
<td>EL2, Hyp mode, the HVC instruction, and all the features described by Virt_frac == \texttt{0b0001} implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- \texttt{0b0000} when EL2 is not implemented.
- \texttt{0b0001} when EL2 is implemented.

In an implementation that includes EL2, if EL2 cannot use AArch32 but EL1 can use AArch32 then this field has the value \texttt{0b0001}.

**Note**

The ID\_ISARs do not identify whether the HVC instruction is implemented.

**MProgMod, bits [11:8]**

M profile programmers' model support. Defined values are:

<table>
<thead>
<tr>
<th>MProgMod</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0000}</td>
<td>Not supported.</td>
</tr>
<tr>
<td>\texttt{0b0010}</td>
<td>Support for two-stack programmers' model.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is \texttt{0b0000}.

**Security, bits [7:4]**

Security support. Defined values are:

<table>
<thead>
<tr>
<th>Security</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0000}</td>
<td>EL3, Monitor mode, and the SMC instruction not implemented.</td>
</tr>
<tr>
<td>\texttt{0b0001}</td>
<td>EL3, Monitor mode, the SMC instruction, and all the features described by Sec_frac == \texttt{0b0001} implemented.</td>
</tr>
<tr>
<td>\texttt{0b0010}</td>
<td>As for \texttt{0b0001}, and adds the ability to set the NSACR_RFR bit. Not permitted in Armv8 as the NSACR_RFR bit is RES0.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- \texttt{0b0000} when EL3 is not implemented.
- \texttt{0b0001} when EL3 is implemented.

In an implementation that includes EL3, if EL3 cannot use AArch32 but EL1 can use AArch32 then this field has the value \texttt{0b0001}.

**ProgMod, bits [3:0]**

Support for the standard programmers' model for ARMv4 and later. Model must support User, FIQ, IRQ, Supervisor, Abort, Undefined, and System modes. Defined values are:
### ID_PFR1, Processor Feature Register 1

<table>
<thead>
<tr>
<th>ProgMod</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0001.

**Accessing the ID_PFR1**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>\
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b00</td>
<td>0b0000</td>
<td>0b001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ID_PFR1;
  endif
elsif PSTATE.EL == EL2 then
  return ID_PFR1;
elsif PSTATE.EL == EL3 then
  return ID_PFR1;
ID_PFR2, Processor Feature Register 2

The ID_PFR2 characteristics are:

**Purpose**

Gives information about the AArch32 programmers' model.

Must be interpreted with ID_PFR0 and ID_PFR1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register ID_PFR2 bits [31:0] are architecturally mapped to AArch64 System register ID_PFR2_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ID_PFR2 are UNDEFINED.

**Attributes**

ID_PFR2 is a 32-bit register.

**Field descriptions**

The ID_PFR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |    |    |    |    |    | RAS_frac |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | SSBS |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CSV3 |    |    |    |    |    |

**Bits [31:12]**

Reserved, RES0.

**RAS_frac, bits [11:8]**

RAS Extension fractional field.

<table>
<thead>
<tr>
<th>RAS_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>If ID_PFR0.RAS == 0b0001, RAS Extension implemented. If ID_PFR0.RAS == 0b0001, as 0b0000 and adds support for additional ERXMISC&lt;m&gt; System registers. Error records accessed through System registers conform to RAS System Architecture v1.1, which includes simplifications to ERR&lt;n&gt;STATUS and support for the optional RAS Timestamp Extension.</td>
</tr>
<tr>
<td>0b0001</td>
<td>All other values are reserved.</td>
</tr>
</tbody>
</table>

This field is valid only if ID_PFR0.RAS == 0b0001.

**SSBS, bits [7:4]**

Speculative Store Bypassing controls in AArch64 state. Defined values are:
SSBS | Meaning
---|---
0b0000 | AArch32 provides no mechanism to control the use of Speculative Store Bypassing.
0b0001 | AArch32 provides the PSTATE.SSBS mechanism to mark regions that are Speculative Store Bypass Safe.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

All other values are reserved.

CSV3, bits [3:0]

Speculative use of faulting data. Defined values are:

<table>
<thead>
<tr>
<th>CSV3</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0000 | This Device does not disclose whether data loaded under speculation with a permission or domain fault can be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence.
| 0b0001 | Data loaded under speculation with a permission or domain fault cannot be used to form an address or generate condition codes or SVE predicate values to be used by instructions newer than the load in the speculative sequence.

All other values are reserved.

FEAT_CSV3 implements the functionality identified by the value 0b0001.

In Armv8.0, the permitted values are 0b0000 and 0b0001.

From Armv8.5, the only permitted value is 0b0001.

If FEAT_E0PD is implemented, FEAT_CSV3 must be implemented.

Accessing the ID_PFR2

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>

```
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & ELUsingAArch32(EL2) & HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return ID_PFR2;
    endif
elsif PSTATE.EL == EL2 then
    return ID_PFR2;
elsif PSTATE.EL == EL3 then
    return ID_PFR2;
```
IFAR, Instruction Fault Address Register

The IFAR characteristics are:

**Purpose**

Holds the virtual address of the faulting address that caused a synchronous Prefetch Abort exception.

**Configuration**

AArch32 System register IFAR bits [31:0] are architecturally mapped to AArch64 System register `FAR_EL1[63:32]`.

AArch32 System register IFAR bits [31:0] (S) are architecturally mapped to AArch32 System register `HIFAR[31:0]` when EL2 is implemented, EL3 is implemented and the highest implemented Exception level is using AArch32 state.

AArch32 System register IFAR bits [31:0] (S) are architecturally mapped to AArch64 System register `FAR_EL2[63:32]` when EL2 is implemented.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to IFAR are UNDEFINED.

**Attributes**

IFAR is a 32-bit register.

**Field descriptions**

The IFAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VA of faulting address of synchronous Prefetch Abort exception</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

VA of faulting address of synchronous Prefetch Abort exception.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the IFAR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2>}
\]

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

Page 2798
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return IFAR_NS;
    else
        return IFAR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return IFAR_NS;
    else
        return IFAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        IFAR_S = R[t];
    else
        IFAR_NS = R[t];
else
    IFAR_NS = R[t];

MCR{<c>{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0110</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T6 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T6 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccess Trap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        IFAR_NS = R[t];
    else
        IFAR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        IFAR_NS = R[t];
    else
        IFAR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        IFAR_S = R[t];
    else
        IFAR_NS = R[t];
IFSР, Instruction Fault Status Register

The IFSР characteristics are:

**Purpose**

Holds status information about the last instruction fault.

**Configuration**

AArch32 System register IFSР [31:0] are architecturally mapped to AArch64 System register IFSР_32_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to IFSР are UNDEFINED.

The current translation table format determines which format of the register is used.

**Attributes**

IFSР is a 32-bit register.

**Field descriptions**

The IFSР bit assignments are:

**When TTBCR.EAE == 0:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Res0 | FnV | RES0 | ExT | RES0 | FS[4] | LPAE | RES0 | FS[3:0] |

**Bits [31:17]**

Reserved, RES0.

**FnV, bit [16]**

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>IFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is RES0 for all other Prefetch Abort exceptions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:13]**

Reserved, RES0.

**ExT, bit [12]**

External abort type. This bit can be used to provide an IMPLEMENTATION DEFINED classification of External aborts.

In an implementation that does not provide any classification of External aborts, this bit is RES0.
For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [11]**

Reserved, RES0.

**FS, bits [10, 3:0]**


<table>
<thead>
<tr>
<th>FS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00001</td>
<td>PC alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b00010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b00011</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b00110</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b00111</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b01001</td>
<td>Domain fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01011</td>
<td>Domain fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b01100</td>
<td>Synchronous External abort, on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b01101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b01110</td>
<td>Synchronous External abort, on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b01111</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b10000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
<tr>
<td>0b10100</td>
<td>IMPLEMENTATION DEFINED fault (Lockdown fault).</td>
<td></td>
</tr>
<tr>
<td>0b11001</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11100</td>
<td>Synchronous parity or ECC error on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b11110</td>
<td>Synchronous parity or ECC error on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information about the lookup level associated with a fault, see 'The level associated with MMU faults on a Short-descriptor translation table lookup'.

The FS field is split as follows:

- FS[4] is IFSR[10].
- FS[3:0] is IFSR[3:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**LPAE, bit [9]**

On taking a Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>

Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [8:4]

Reserved, RES0.

When TTBCR.EAE == 1:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>FnV RES0 Ext RES0 LPAE RES0 STATUS</td>
</tr>
</tbody>
</table>

Bits [31:17]

Reserved, RES0.

FnV, bit [16]

FAR not Valid, for a synchronous External abort other than a synchronous External abort on a translation table walk.

<table>
<thead>
<tr>
<th>FnV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IFAR is valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>IFAR is not valid, and holds an UNKNOWN value.</td>
</tr>
</tbody>
</table>

This field is only valid for a synchronous External abort other than a synchronous External abort on a translation table walk. It is RES0 for all other Prefetch Abort exceptions.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [15:13]

Reserved, RES0.

ExT, bit [12]

External abort type. This bit can be used to provide an IMPLEMENTATION DEFINED classification of External aborts.

In an implementation that does not provide any classification of External aborts, this bit is RES0.

For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [11:10]

Reserved, RES0.

LPAE, bit [9]

On taking a Data Abort exception, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table formats.</td>
</tr>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table formats.</td>
</tr>
</tbody>
</table>

Hardware does not interpret this bit to determine the behavior of the memory system, and therefore software can set this bit to 0 or 1 without affecting operation.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [8:6]

Reserved, RES0.
**STATUS, bits [5:0]**

Fault status bits. Possible values of this field are:

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault in translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000100</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010000</td>
<td>Synchronous External abort, not on translation table walk.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b011000</td>
<td>Synchronous parity or ECC error on memory access, not on translation table walk.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b100001</td>
<td>PC alignment fault.</td>
<td></td>
</tr>
<tr>
<td>0b100010</td>
<td>Debug exception.</td>
<td></td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

When FEAT_RAS is implemented, 0b011000, 0b011101, 0b011110, and 0b011111 are reserved.

For more information about the lookup level associated with a fault, see ‘The level associated with MMU faults on a Long-descriptor translation table lookup’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the IFSR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>\} <cogroc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b0101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAAArch32(EL3) then
    return IFSR_NS;
else
  return IFSR;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAAArch32(EL3) then
    return IFSR_NS;
  else
    return IFSR;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return IFSR_S;
  else
    return IFSR_NS;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0101</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAAArch32(EL2) && HSTR_EL2.T5 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T5 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAAArch32(EL3) then
    IFSR_NS = R[t];
else
  IFSR = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAAArch32(EL3) then
    IFSR_NS = R[t];
else
  IFSR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    IFSR_S = R[t];
else
  IFSR_NS = R[t];
ISR, Interrupt Status Register

The ISR characteristics are:

**Purpose**

Shows the pending status of the IRQ, FIQ, or SError.

When executing at EL2, EL3, or Secure EL1, when \( \text{SCR}_\text{EL3}.\text{EEL2} == 0b0 \), this shows the pending status of the physical interrupts.

When executing at Non-secure EL1, or at Secure EL1, when \( \text{SCR}_\text{EL3}.\text{EEL2} == 0b01 \):

- If the \( \text{HCR}.\{\text{IMO,FMO,AMO}\} \) bit has a value of 1, the corresponding ISR.\{I,F,A\} bit shows the pending status of the virtual IRQ, FIQ, or SError.
- If the \( \text{HCR}.\{\text{IMO,FMO,AMO}\} \) bit has a value of 0, the corresponding ISR.\{I,F,A\} bit shows the pending status of the physical IRQ, FIQ, or SError.

**Configuration**

AArch32 System register ISR bits [31:0] are architecturally mapped to AArch64 System register ISR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ISR are UNDEFINED.

**Attributes**

ISR is a 32-bit register.

**Field descriptions**

The ISR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30-22</td>
<td>Reserved</td>
</tr>
<tr>
<td>21-19</td>
<td>Reserved</td>
</tr>
<tr>
<td>18-16</td>
<td>Reserved</td>
</tr>
<tr>
<td>15-12</td>
<td>Reserved</td>
</tr>
<tr>
<td>11-8</td>
<td>A</td>
</tr>
<tr>
<td>7</td>
<td>I</td>
</tr>
<tr>
<td>6</td>
<td>F</td>
</tr>
<tr>
<td>5-0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**Bits [31:9]**

Reserved, RES0.

**A, bit [8]**

SError interrupt pending bit:

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending SError interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>An SError interrupt is pending.</td>
</tr>
</tbody>
</table>

If the SError interrupt is edge-triggered, this field is cleared to zero when the physical SError interrupt is taken.

**I, bit [7]**

IRQ pending bit. Indicates whether an IRQ interrupt is pending:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending IRQ.</td>
</tr>
<tr>
<td>0b1</td>
<td>An IRQ interrupt is pending.</td>
</tr>
</tbody>
</table>
F, bit [6]

FIQ pending bit. Indicates whether an FIQ interrupt is pending.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No pending FIQ.</td>
</tr>
<tr>
<td>0b1</td>
<td>An FIQ interrupt is pending.</td>
</tr>
</tbody>
</table>

Bits [5:0]

Reserved, RES0.

Accessing the ISR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{ <coproc>, } \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return ISR;
elsif PSTATE.EL == EL2 then
  return ISR;
elsif PSTATE.EL == EL3 then
  return ISR;
The ITLBIALL characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from instruction TLBs that are from any level of the translation table walk. The entries that are invalidated are as follows:

- If executed at EL1, all entries that:
  - Would be required for the EL1&0 translation regime.
  - Match the current VMID, if EL2 is implemented and enabled in the current Security state.
- If executed in Secure state when EL3 is using AArch32, all entries that would be required for the Secure PL1&0 translation regime.
- If executed at EL2, and if EL2 is enabled in the current Security state, the stage 1 or stage 2 translation table entries that would be required for the Non-secure PL1&0 translation regime and matches the current VMID.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ITLBIALL are **UNDEFINED**.

**Attributes**

ITLBIALL is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by `<Rt>` is ignored.

**Executing the ITLBIALL instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} \text{ <coproc>, \{#}<opc1>, <Rt>, <CRn>, <CRm>{, \{#}<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR_T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR_TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ITLBIALL();
    endif
elsif PSTATE.EL == EL2 then
    ITLBIALL();
elsif PSTATE.EL == EL3 then
    ITLBIALL();
30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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ITLBIASID, Instruction TLB Invalidate by ASID match

The ITLBIASID characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from instruction TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ITLBIASID are UNDEFINED.

**Attributes**

ITLBIASID is a 32-bit System instruction.

**Field descriptions**

The ITLBIASID input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | ASID |

**Bits [31:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries for non-global pages that match the ASID values will be affected by this System instruction.

**Executing the ITLBIASID instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ITLBIASID(R[t]);
    end if;
elsif PSTATE.EL == EL2 then
    ITLBIASID(R[t]);
elsif PSTATE.EL == EL3 then
    ITLBIASID(R[t]);
ITLBIMVA, Instruction TLB Invalidate by VA

The ITLBIMVA characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from instruction TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

Arm deprecates the use of this System instruction. It is only provided for backwards compatibility with earlier versions of the Arm architecture.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to ITLBIMVA are **UNDEFINED**.

**Attributes**

ITLBIMVA is a 32-bit System instruction.

**Field descriptions**

The ITLBIMVA input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>RES0</td>
<td>ASID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this operation, regardless of the value of the ASID field.
Executing the ITLBIMVA instruction

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{\text{<c>}\}\{\text{<q>}\} \text{<coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm}\{, \{#\}<opc2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0101</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        ITLBIMVA(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    ITLBIMVA(R[t]);
elsif PSTATE.EL == EL3 then
    ITLBIMVA(R[t]);
The JIDR characteristics are:

**Purpose**

A Jazelle register, which identified the Jazelle architecture version.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to JIDR are **UNDEFINED**.

**Attributes**

JIDR is a 32-bit register.

**Field descriptions**

The JIDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:0]**

Reserved, RAZ.

**Accessing the JIDR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b11</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if boolean IMPLEMENTATION_DEFINED "JIDR UNDEFINED at EL0" then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HCR_EL2.TID0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    else
        return JIDR;
    endif
else if PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x05);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID0 == '1' then
        AArch32.TakeHypTrapException(0x05);
    else
        return JIDR;
    endif
else if PSTATE.EL == EL2 then
    return JIDR;
else if PSTATE.EL == EL3 then
    return JIDR;
The JMCR characteristics are:

**Purpose**

A Jazelle register, which provides control of the Jazelle extension.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to JMCR are UNDEFINED.

**Attributes**

JMCR is a 32-bit register.

**Field descriptions**

The JMCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RAZ/WI |

**Bits [31:0]**

Reserved, RAZ/WI.

**Accessing the JMCR**

For accesses from EL0 it is IMPLEMENTATION DEFINED whether the register is RW or UNDEFINED.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b111</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  if boolean IMPLEMENTATION_DEFINED "JMCR UNDEFINED at EL0" then
    UNDEFINED;
  else
    return JMCR;
elsif PSTATE.EL == EL1 then
  return JMCR;
elsif PSTATE.EL == EL2 then
  return JMCR;
elsif PSTATE.EL == EL3 then
  return JMCR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if boolean IMPLEMENTATION_DEFINED "JMCR UNDEFINED at EL0" then
    UNDEFINED;
  else
    // no operation
elsif PSTATE.EL == EL1 then
  // no operation
elsif PSTATE.EL == EL2 then
  // no operation
elsif PSTATE.EL == EL3 then
  // no operation
The JOSCR characteristics are:

**Purpose**

A Jazelle register, which provides operating system control of the Jazelle Extension.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to JOSCR are **UNDEFINED**.

**Attributes**

JOSCR is a 32-bit register.

**Field descriptions**

The JOSCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RAZ/WI</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Reserved, RAZ/WI.

**Accessing the JOSCR**

Accesses to this register use the following encodings:

```assembly
if PSTATE.EL == EL0 then
    if boolean IMPLEMENTATION_DEFINED "JOSCR UNDEFINED at EL0" then
        UNDEFINED;
    else
        return JOSCR;
elsif PSTATE.EL == EL1 then
    return JOSCR;
elsif PSTATE.EL == EL2 then
    return JOSCR;
elsif PSTATE.EL == EL3 then
    return JOSCR;
```

```assembly
MCR{<c>{<q>}{<coproc>, {#}<op1>, <Rt>, <CRn>, <CRm>{, {#}<op2>}}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b11</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b00</td>
</tr>
</tbody>
</table>

```assembly
MRC{<c>{<q>}{<coproc>, {#}<op1>, <Rt>, <CRn>, <CRm>{, {#}<op2>}}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>op1</th>
<th>CRn</th>
<th>CRm</th>
<th>op2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1110</td>
<td>0b11</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b00</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if boolean IMPLEMENTATION_DEFINED "JOSCR UNDEFINED at EL0" then
    UNDEFINED;
  else
    // no operation
elsif PSTATE.EL == EL1 then
  // no operation
elsif PSTATE.EL == EL2 then
  // no operation
elsif PSTATE.EL == EL3 then
  // no operation
MAIR0, Memory Attribute Indirection Register 0

The MAIR0 characteristics are:

Purpose

Along with MAIR1, provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations.

AttrIndx[2] indicates the MAIR register to be used:

- When AttrIndx[2] is 0, MAIR0 is used.
- When AttrIndx[2] is 1, MAIR1 is used.

Configuration

AArch32 System register MAIR0 bits [31:0] are architecturally mapped to AArch64 System register MAIR_EL1[31:0] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register MAIR0 bits [31:0] are architecturally mapped to AArch32 System register PRRR[31:0] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register MAIR0 bits [31:0] (MAIR0_NS) are architecturally mapped to AArch32 System register PRRR[31:0] (PRRR_NS) when EL3 is using AArch32.

AArch32 System register MAIR0 bits [31:0] (MAIR0_S) are architecturally mapped to AArch32 System register PRRR[31:0] (PRRR_S) when EL3 is using AArch32.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MAIR0 are UNDEFINED.

MAIR0 and PRRR are the same register, with a different view depending on the value of TTBCR.EAE:

- When it is set to 0, the register is as described in PRRR.
- When it is set to 1, the register is as described in MAIR0.

When EL3 is using AArch32, write access to MAIR0(S) is disabled when the CP15SDISABLE signal is asserted HIGH.

Attributes

MAIR0 is a 32-bit register.

Field descriptions

The MAIR0 bit assignments are:

When TTBCR.EAE == 1:

| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|------------------------------------------|------------------------------------------|------------------------------------------|
| Attr3 | Attr2 | Attr1 | Attr0 |

Attr<n>, bits [8n+7:8n], for n = 3 to 0

The memory attribute encoding for an AttrIndx[2:0] entry in a Long descriptor format translation table entry, where:

- AttrIndx[2:0] gives the value of <n> in Attr<n>.
- AttrIndx[2] defines which MAIR to access. Attr7 to Attr4 are in MAIR1, and Attr3 to Attr0 are in MAIR0.

Bits [7:4] are encoded as follows:
### Attr<n>[7:4] Meaning

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device memory. See encoding of Attr&lt;n&gt;[3:0] for the type of Device memory.</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Outer Write-Through Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Outer Write-Back Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Outer Write-Through Non-transient.</td>
</tr>
<tr>
<td>0b11RW</td>
<td>Normal memory, Outer Write-Back Non-transient.</td>
</tr>
</tbody>
</table>

R = Outer Read-Allocate policy, W = Outer Write-Allocate policy.

The meaning of bits [3:0] depends on the value of bits [7:4]:

<table>
<thead>
<tr>
<th>Attr&lt;n&gt;[3:0]</th>
<th>Meaning when Attr&lt;n&gt;[7:4] is 0b0000</th>
<th>Meaning when Attr&lt;n&gt;[7:4] is not0b0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory</td>
<td>UNPREDICTABLE</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Through Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td>Device-nGnRE memory</td>
<td>Normal memory, Inner Non-cacheable</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Back Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td>Device-GRE memory</td>
<td>Normal memory, Inner Write-Through Non-transient (RW=0b00)</td>
</tr>
<tr>
<td>0b10RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Back Non-transient (RW=0b00)</td>
</tr>
<tr>
<td>not0b00</td>
<td>Device-GRnRnE memory</td>
<td>Normal memory, Inner Write-Through Non-transient (RW=0b00)</td>
</tr>
<tr>
<td>0b11RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Back Non-transient</td>
</tr>
<tr>
<td>not0b00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

R = Inner Read-Allocate policy, W = Inner Write-Allocate policy.

The R and W bits in some Attr<n> fields have the following meanings:

<table>
<thead>
<tr>
<th>R or W</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Allocate</td>
</tr>
<tr>
<td>0b1</td>
<td>Allocate</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the MAIR0

Accesses to this register use the following encodings:

\[
\text{MRC}\{\langle c\rangle\{\langle q\rangle\ \langle\text{coproc}\rangle, \{\#\langle\text{opc1}\rangle, \langle\text{Rt}\rangle, \langle\text{CRn}\rangle, \langle\text{CRm}\rangle, \{\#\langle\text{opc2}\rangle\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TRVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HCR.TRVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) & ELUsingAArch32(EL3) then
    if TTBCR.EAE == '1' then
      return MAIR0_NS;
    else
      return PRRR_NS;
    end
  else
    if TTBCR.EAE == '1' then
      return MAIR0;
    else
      return PRRR;
    end
  endif
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) & ELUsingAArch32(EL3) then
      if TTBCR.EAE == '1' then
        return MAIR0_NS;
      else
        return PRRR_NS;
      end
    else
      if TTBCR.EAE == '1' then
        return MAIR0;
      else
        return PRRR;
      end
    endif
  else
    if TTBCR.EAE == '1' then
      if SCR.NS == '0' then
        return MAIR0_S;
      else
        return MAIR0_NS;
      end
    else
      if SCR.NS == '0' then
        return PRRR_S;
      else
        return PRRR_NS;
      end
    endif
  endif
end

MCR{<c>{<q>}}<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      if HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
          MAIR0_NS = R[t];
        else
          PRRR_NS = R[t];
        endif
      else
        if TTBCR.EAE == '1' then
          MAIR0 = R[t];
        else
          PRRR = R[t];
        endif
      endif
    endif
  else
    if PSTATE.EL == EL2 then
      if HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
          MAIR0_NS = R[t];
        else
          PRRR_NS = R[t];
        endif
      else
        if TTBCR.EAE == '1' then
          MAIR0 = R[t];
        else
          PRRR = R[t];
        endif
      endif
    elseif PSTATE.EL == EL3 then
      if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
      elseif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
      else
        if TTBCR.EAE == '1' then
          if SCR.NS == '0' then
            MAIR0_S = R[t];
          else
            MAIR0_NS = R[t];
          endif
        else
          if SCR.NS == '0' then
            PRRR_S = R[t];
          else
            PRRR_NS = R[t];
          endif
        endif
      endif
    endif
  endif
endif
MAIR1, Memory Attribute Indirection Register 1

The MAIR1 characteristics are:

**Purpose**

Along with MAIR0, provides the memory attribute encodings corresponding to the possible AttrIndx values in a Long-descriptor format translation table entry for stage 1 translations.

AttrIndx[2] indicates the MAIR register to be used:

- When AttrIndx[2] is 0, MAIR0 is used.
- When AttrIndx[2] is 1, MAIR1 is used.

**Configuration**

AArch32 System register MAIR1 bits [31:0] are architecturally mapped to AArch64 System register MAIR_EL1[63:32] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register MAIR1 bits [31:0] are architecturally mapped to AArch32 System register NMRR[31:0] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register MAIR1 bits [31:0] (MAIR1_NS) are architecturally mapped to AArch32 System register NMRR[31:0] (NMRR_NS) when EL3 is using AArch32.

AARc32 System register MAIR1 bits [31:0] (MAIR1_S) are architecturally mapped to AArch32 System register NMRR[31:0] (NMRR_S) when EL3 is using AArch32.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MAIR1 are UNDEFINED.

MAIR1 and NMRR are the same register, with a different view depending on the value of TTBCR.EAE:

- When it is set to 0, the register is as described in NMRR.
- When it is set to 1, the register is as described in MAIR1.

When EL3 is using AArch32, write access to MAIR1(S) is disabled when the CP15SDISABLE signal is asserted HIGH.

**Attributes**

MAIR1 is a 32-bit register.

**Field descriptions**

The MAIR1 bit assignments are:

When TTBCR.EAE == 1:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Attr7</th>
<th>Attr6</th>
<th>Attr5</th>
<th>Attr4</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
</tr>
<tr>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
</tr>
<tr>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
</tr>
<tr>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
</tr>
<tr>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Attr<n>, bits [8(n-4)+7:8(n-4)], for n = 7 to 4

The memory attribute encoding for an AttrIndx[2:0] entry in a Long descriptor format translation table entry, where:

- AttrIndx[2:0] gives the value of <n> in Attr<n>.
- AttrIndx[2] defines which MAIR to access. Attr7 to Attr4 are in MAIR1, and Attr3 to Attr0 are in MAIR0.

Bits [7:4] are encoded as follows:
<table>
<thead>
<tr>
<th>Attr&lt;\text{n}&gt;[7:4]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device memory. See encoding of Attr&lt;\text{n}&gt;[3:0] for the type of Device memory.</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>Normal memory, Outer Write-Through Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>Normal memory, Outer Write-Back Transient.</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Outer Write-Through Non-transient.</td>
</tr>
<tr>
<td>0b10RW</td>
<td>Normal memory, Outer Write-Back Non-transient.</td>
</tr>
</tbody>
</table>

\textbf{R} = Outer Read-Allocate policy, \textbf{W} = Outer Write-Allocate policy.

The meaning of bits [3:0] depends on the value of bits [7:4]:

<table>
<thead>
<tr>
<th>Attr&lt;\text{n}&gt;[3:0]</th>
<th>Meaning when Attr&lt;\text{n}&gt;[7:4] is 0b0000</th>
<th>Meaning when Attr&lt;\text{n}&gt;[7:4] is not0b0000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory</td>
<td>UNPREDICTABLE</td>
</tr>
<tr>
<td>0b00RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Through Transient</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Inner Non-cacheable</td>
<td></td>
</tr>
<tr>
<td>0b01RW, RW</td>
<td>UNPREDICTABLE</td>
<td>Normal memory, Inner Write-Back Transient (RW=0b00)</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Inner Write-Through Non-transient (RW=0b00)</td>
<td></td>
</tr>
<tr>
<td>0b10RW</td>
<td>Device-GRE memory</td>
<td>Normal memory, Inner Write-Back Non-transient</td>
</tr>
<tr>
<td>not0b00</td>
<td>Normal memory, Inner Write-Back Non-transient</td>
<td></td>
</tr>
</tbody>
</table>

\textbf{R} = Inner Read-Allocate policy, \textbf{W} = Inner Write-Allocate policy.

The \textbf{R} and \textbf{W} bits in some Attr<\text{n}> fields have the following meanings:

<table>
<thead>
<tr>
<th>\textbf{R or W}</th>
<th>\textbf{Meaning}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Allocate</td>
</tr>
<tr>
<td>0b1</td>
<td>Allocate</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally \textbf{UNKNOWN} value.

**Accessing the MAIR1**

Accesses to this register use the following encodings:

\[ \text{MRC}\{<c>\}{<q>} \ <\text{coproc}> , \{#\}<\text{opc1}>, \ <\text{Rt}> , \ <\text{CRn}> , \ <\text{CRm}>, \{#\}<\text{opc2}> \]

<table>
<thead>
<tr>
<th>\textbf{coproc}</th>
<th>\textbf{opc1}</th>
<th>\textbf{CRn}</th>
<th>\textbf{CRm}</th>
<th>\textbf{opc2}</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
  if TTBCR.EAE == '1' then
    return MAIR1_NS;
  else
    return NMRR_NS;
else
  if TTBCR.EAE == '1' then
    return MAIR1;
  else
    return NMRR;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    if TTBCR.EAE == '1' then
      return MAIR1_NS;
    else
      return NMRR_NS;
  else
    if TTBCR.EAE == '1' then
      return MAIR1;
    else
      return NMRR;
elsif PSTATE.EL == EL3 then
  if TTBCR.EAE == '1' then
    if SCR.NS == '0' then
      return MAIR1_S;
    else
      return MAIR1_NS;
  else
    if SCR.NS == '0' then
      return NMRR_S;
    else
      return NMRR_NS;

MCR{c}{q} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
            MAIR1_NS = R[t];
        else
            NMRR_NS = R[t];
        end
else
    if TTBCR.EAE == '1' then
        MAIR1 = R[t];
    else
        NMRR = R[t];
else
    if TTBCR.EAE == '1' then
        MAIR1_NS = R[t];
    else
        NMRR_NS = R[t];
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
            MAIR1_NS = R[t];
        else
            NMRR_NS = R[t];
        end
else
    if TTBCR.EAE == '1' then
        MAIR1 = R[t];
    else
        NMRR = R[t];
else
    if TTBCR.EAE == '1' then
        MAIR1_NS = R[t];
    else
        NMRR_NS = R[t];
    end
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elseif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
else
    if TTBCR.EAE == '1' then
        if SCR.NS == '0' then
            MAIR1_S = R[t];
        else
            MAIR1_NS = R[t];
        end
    else
        MAIR1_S = R[t];
    end
    if SCR.NS == '0' then
        NMRR_S = R[t];
    else
        NMRR_NS = R[t];
    end

### MIDR, Main ID Register

The MIDR characteristics are:

#### Purpose

Provides identification information for the PE, including an implementer code for the device and a device ID number.

#### Configuration

AArch32 System register MIDR bits [31:0] are architecturally mapped to AArch64 System register `MIDR_EL1[31:0]`.

AArch32 System register MIDR bits [31:0] are architecturally mapped to External register `MIDR_EL1[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MIDR are UNDEFINED.

Some fields of the MIDR are IMPLEMENTATION DEFINED. For details of the values of these fields for a particular Armv8 implementation, and any implementation-specific significance of these values, see the product documentation.

#### Attributes

MIDR is a 32-bit register.

#### Field descriptions

The MIDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Implementer | Variant | Architecture | PartNum | Revision |

**Implementer, bits [31:24]**

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Implementer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Reserved for software use</td>
</tr>
<tr>
<td>0x01</td>
<td>Ampere Computing</td>
</tr>
<tr>
<td>0x41</td>
<td>Arm Limited</td>
</tr>
<tr>
<td>0x42</td>
<td>Broadcom Corporation</td>
</tr>
<tr>
<td>0x43</td>
<td>Cavium Inc.</td>
</tr>
<tr>
<td>0x44</td>
<td>Digital Equipment Corporation</td>
</tr>
<tr>
<td>0x46</td>
<td>Fujitsu Ltd.</td>
</tr>
<tr>
<td>0x49</td>
<td>Infineon Technologies AG</td>
</tr>
<tr>
<td>0x4A</td>
<td>Motorola or Freescale Semiconductor Inc.</td>
</tr>
<tr>
<td>0x4E</td>
<td>NVIDIA Corporation</td>
</tr>
<tr>
<td>0x50</td>
<td>Applied Micro Circuits Corporation</td>
</tr>
<tr>
<td>0x51</td>
<td>Qualcomm Inc.</td>
</tr>
<tr>
<td>0x56</td>
<td>Marvell International Ltd.</td>
</tr>
<tr>
<td>0x69</td>
<td>Intel Corporation</td>
</tr>
</tbody>
</table>

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.

**Variant, bits [23:20]**

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product.
Architecture, bits [19:16]

Architecture version. Defined values are:

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv4.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv4T.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv5 (obsolete).</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv5I.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv5TE.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv5TEJ.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv6.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Architectural features are individually identified in the ID * registers, see 'ID registers'.</td>
</tr>
</tbody>
</table>

All other values are reserved.

PartNum, bits [15:4]

An IMPLEMENTATION DEFINED primary part number for the device.

On processors implemented by Arm, if the top four bits of the primary part number are 0x0 or 0x7, the variant and architecture are encoded differently.

Revision, bits [3:0]

An IMPLEMENTATION DEFINED revision number for the device.

Accessing the MIDR

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp; HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp; HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() &amp; !ELUsingAArch32(EL2) then
    return VPIDR_EL2<31:0>;
  elsif EL2Enabled() &amp; ELUsingAArch32(EL2) then
    return VPIDR;
  else
    return MIDR;
elsif PSTATE.EL == EL2 then
  return MIDR;
elsif PSTATE.EL == EL3 then
  return MIDR;
The MPIDR characteristics are:

**Purpose**

In a multiprocessor system, provides an additional PE identification mechanism for scheduling purposes.

**Configuration**

AArch32 System register MPIDR bits [31:0] are architecturally mapped to AArch64 System register MPIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MPIDR are UNDEFINED.

In a uniprocessor system Arm recommends that each Aff<n> field of this register returns a value of 0.

**Attributes**

MPIDR is a 32-bit register.

**Field descriptions**

The MPIDR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>U</td>
<td>RES0</td>
<td>MT</td>
<td>Aff2</td>
<td>Aff1</td>
<td>Aff0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**M, bit [31]**

Indicates whether this implementation includes the functionality introduced by the ARMv7 Multiprocessing Extensions. The possible values of this bit are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This implementation does not include the ARMv7 Multiprocessing</td>
</tr>
<tr>
<td></td>
<td>Extensions functionality.</td>
</tr>
<tr>
<td>0b1</td>
<td>This implementation includes the ARMv7 Multiprocessing</td>
</tr>
<tr>
<td></td>
<td>Extensions functionality.</td>
</tr>
</tbody>
</table>

From Armv8, this bit is RAO.

**U, bit [30]**

Indicates a Uniprocessor system, as distinct from PE 0 in a multiprocessor system. The possible values of this bit are:

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Processor is part of a multiprocessor system.</td>
</tr>
<tr>
<td>0b1</td>
<td>Processor is part of a uniprocessor system.</td>
</tr>
</tbody>
</table>

**Bits [29:25]**

Reserved, RES0.
MT, bit [24]

Indicates whether the lowest level of affinity consists of logical PEs that are implemented using a multithreading type approach. See the description of Aff0 for more information about affinity levels. The possible values of this bit are:

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Performance of PEs at the lowest affinity level, or PEs with MPIDR.MT set to 1, different affinity level 0 values, and the same values for affinity level 1 and higher, is largely independent.</td>
</tr>
<tr>
<td>0b1</td>
<td>Performance of PEs at the lowest affinity level, or PEs with MPIDR.MT set to 1, different affinity level 0 values, and the same values for affinity level 1 and higher, is very interdependent.</td>
</tr>
</tbody>
</table>

Aff2, bits [23:16]

Affinity level 2. See the description of Aff0 for more information.

Aff1, bits [15:8]

Affinity level 1. See the description of Aff0 for more information.

Aff0, bits [7:0]

Affinity level 0. This is the affinity level that is most significant for determining PE behavior. Higher affinity levels are increasingly less significant in determining PE behavior. The assigned value of the MPIDR.{Aff2, Aff1, Aff0} or MPIDR_EL1.{Aff3, Aff2, Aff1, Aff0} set of fields of each PE must be unique within the system as a whole.

Accessing the MPIDR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} \text{ <coproc>, } \{#<opc1>, <Rt>, <CRn>, <CRm}\{, \{#<opc2>\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b000</td>
<td>0b000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() \&\& !ELUsingAArch32(EL2) then
    return VMPIDR_EL2<31:0>;
  elsif EL2Enabled() \&\& ELUsingAArch32(EL2) then
    return VMPIDR;
  else
    return MPIDR;
elsif PSTATE.EL == EL2 then
  return MPIDR;
elsif PSTATE.EL == EL3 then
  return MPIDR;
The MVBAR characteristics are:

**Purpose**

When EL3 is implemented and can use AArch32, holds the vector base address for any exception that is taken to Monitor mode.

Secure software must program the MVBAR with the required initial value as part of the PE boot sequence.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MVBAR are UNDEFINED.

It is IMPLEMENTATION DEFINED whether MVBAR[0] has a fixed value and ignored writes, or takes the last value written to it.

On a reset into EL3 using AArch32, the reset value of MVBAR is an IMPLEMENTATION DEFINED choice between the following:

- MVBAR[31:5] = an IMPLEMENTATION DEFINED value, which might be UNKNOWN, MVBAR[4:1] = RES0, and MVBAR[0] = 0.
- MVBAR[31:1] = an IMPLEMENTATION DEFINED value that is bits[31:1] of the AArch32 reset address, and MVBAR[0] = 1.

**Attributes**

MVBAR is a 32-bit register.

**Field descriptions**

The MVBAR bit assignments are:

**When programmed with a vector base address:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-5</td>
<td>Vector Base Address</td>
</tr>
<tr>
<td>4-0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Bits [31:5]**

Vector Base Address. Bits[31:5] of the base address of the exception vectors for exceptions taken to this Exception level. Bits[4:0] of an exception vector are the exception offset.

**Reserved, bits [4:0]**

Reserved, see Configurations.

**Accessing the MVBAR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if IsHighestEL(EL1) then
    return RVBAR;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  if IsHighestEL(EL2) then
    return RVBAR;
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL3 then
  return MVBAR;
end if;

MCR{<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

coproc    opc1    CRn    CRm    opc2
0b1111    0b0000  0b1100  0b0000  0b001

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' && CP15SDISABLE == HIGH then
    UNDEFINED;
  elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
    UNDEFINED;
  else
    MVBAR = R[t];
  end if;
The MVFR0 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation.

Must be interpreted with MVFR1 and MVFR2.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register MVFR0 bits [31:0] are architecturally mapped to AArch64 System register MVFR0_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MVFR0 are UNDEFINED.

Implemented only if the implementation includes Advanced SIMD and floating-point instructions.

**Attributes**

MVFR0 is a 32-bit register.

**Field descriptions**

The MVFR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| FPRound | FPShVec | FPSqrt | FPDivide | FPTrap | FPDP | FPSP | SIMDReg |

**FPRound, bits [31:28]**

Floating-Point Rounding modes. Indicates whether the floating-point implementation provides support for rounding modes. Defined values are:

<table>
<thead>
<tr>
<th>FPRound</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or only Round to Nearest mode supported, except that Round towards Zero mode is supported for VCVT instructions that always use that rounding mode regardless of the FPSCR setting.</td>
</tr>
<tr>
<td>0b0001</td>
<td>All rounding modes supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**FPShVec, bits [27:24]**

Short Vectors. Indicates whether the floating-point implementation provides support for the use of short vectors. Defined values are:

<table>
<thead>
<tr>
<th>FPShVec</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Short vectors not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Short vector operation supported.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**FPSqrt, bits [23:20]**

Square Root. Indicates whether the floating-point implementation provides support for the ARMv6 VFP square root operations. Defined values are:

<table>
<thead>
<tr>
<th>FPSqrt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

The VSQRT.F32 instruction also requires the single-precision floating-point attribute, bits [7:4], and the VSQRT.F64 instruction also requires the double-precision floating-point attribute, bits [11:8].

**FPDivide, bits [19:16]**

Indicates whether the floating-point implementation provides support for VFP divide operations. Defined values are:

<table>
<thead>
<tr>
<th>FPDivide</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

The VDIV.F32 instruction also requires the single-precision floating-point attribute, bits [7:4], and the VDIV.F64 instruction also requires the double-precision floating-point attribute, bits [11:8].

**FPTrap, bits [15:12]**

Floating Point Exception Trapping. Indicates whether the floating-point implementation provides support for exception trapping. Defined values are:

<table>
<thead>
<tr>
<th>FPTrap</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

A value of 0b0001 indicates that, when the corresponding trap is enabled, a floating-point exception generates an exception.

**FPDP, bits [11:8]**

Double Precision. Indicates whether the floating-point implementation provides support for double-precision operations. Defined values are:

<table>
<thead>
<tr>
<th>FPDP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Supported, VFPv2.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Supported, VFPv3, VFPv4, or Armv8. VFPv3 and Armv8 add an instruction to load a double-precision floating-point constant, and conversions between double-precision and fixed-point values.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0010.
A value of \texttt{0b0001} or \texttt{0b0010} indicates support for all VFP double-precision instructions in the supported version of VFP, except that, in addition to this field being nonzero:

- \texttt{VSQR.F64} is only available if the Square root field is \texttt{0b0001}.
- \texttt{VDIV.F64} is only available if the Divide field is \texttt{0b0001}.
- Conversion between double-precision and single-precision is only available if the single-precision field is nonzero.

### FPSP, bits [7:4]

Single Precision. Indicates whether the floating-point implementation provides support for single-precision operations. Defined values are:

<table>
<thead>
<tr>
<th>FPSP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0000}</td>
<td>Not supported in hardware.</td>
</tr>
<tr>
<td>\texttt{0b0001}</td>
<td>Supported, VFPv2.</td>
</tr>
<tr>
<td>\texttt{0b0010}</td>
<td>Supported, VFPv3 or VFPv4. VFPv3 adds an instruction to load a single-precision floating-point constant, and conversions between single-precision and fixed-point values.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are \texttt{0b0000} and \texttt{0b0010}.

A value of \texttt{0b0001} or \texttt{0b0010} indicates support for all VFP single-precision instructions in the supported version of VFP, except that, in addition to this field being nonzero:

- \texttt{VSQR.F32} is only available if the Square root field is \texttt{0b0001}.
- \texttt{VDIV.F32} is only available if the Divide field is \texttt{0b0001}.
- Conversion between double-precision and single-precision is only available if the double-precision field is nonzero.

### SIMDReg, bits [3:0]

Advanced SIMD registers. Indicates whether the Advanced SIMD and floating-point implementation provides support for the Advanced SIMD and floating-point register bank. Defined values are:

<table>
<thead>
<tr>
<th>SIMDReg</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0000}</td>
<td>The implementation has no Advanced SIMD and floating-point support.</td>
</tr>
<tr>
<td>\texttt{0b0001}</td>
<td>The implementation includes floating-point support with 16 x 64-bit registers.</td>
</tr>
<tr>
<td>\texttt{0b0010}</td>
<td>The implementation includes Advanced SIMD and floating-point support with 32 x 64-bit registers.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are \texttt{0b0000} and \texttt{0b0010}.

### Accessing the MVFR0

Accesses to this register use the following encodings:

\[ \text{VMRS}\{<c>\}{<q>} \{Rt\}, \{spec\_reg\} \]

<table>
<thead>
<tr>
<th>reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0111}</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' &&
            NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x08);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x08);
    else
        return MVFR0;
    end if;
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') ||
            HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    else
        return MVFR0;
    end if;
elsif PSTATE.EL == EL3 then
    if CPACR.cp10 == '00' then
        UNDEFINED;
    else
        return MVFR0;
    end if;
else
    return MVFR0;
end if;

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211
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The MVFR1 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation.

Must be interpreted with MVFR0 and MVFR2.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register MVFR1 bits [31:0] are architecturally mapped to AArch64 System register MVFR1_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MVFR1 are UNDEFINED.

Implemented only if the implementation includes Advanced SIMD and floating-point instructions.

**Attributes**

MVFR1 is a 32-bit register.

**Field descriptions**

The MVFR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| SIMDFMAC | FPHP | SIMDHP | SIMDSP | SIMDInt | SIMDLS | FPDNaN | FPfTZ |

**SIMDFMAC, bits [31:28]**

Advanced SIMD Fused Multiply-Accumulate. Indicates whether the Advanced SIMD implementation provides fused multiply accumulate instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDFMAC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

The Advanced SIMD and floating-point implementations must provide the same level of support for these instructions.

**FPHP, bits [27:24]**

Floating Point Half Precision. Indicates the level of half-precision floating-point support. Defined values are:
### FPHP

<table>
<thead>
<tr>
<th>FPHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Floating-point half-precision conversion instructions are supported for conversion between single-precision and half-precision.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds instructions for conversion between double-precision and half-precision.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As for 0b0010, and adds support for half-precision floating-point arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 in an implementation without floating-point support.
- 0b0010 in an implementation with floating-point support that does not include the FEAT_FP16 extension.
- 0b0011 in an implementation with floating-point support that includes the FEAT_FP16 extension.

The level of support indicated by this field must be equivalent to the level of support indicated by the SIMDHP field, meaning the permitted values are:

<table>
<thead>
<tr>
<th>Half Precision instructions supported</th>
<th>FPHP</th>
<th>SIMDHP</th>
</tr>
</thead>
<tbody>
<tr>
<td>No support</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
<tr>
<td>Conversions only</td>
<td>0b0010</td>
<td>0b0001</td>
</tr>
<tr>
<td>Conversions and arithmetic</td>
<td>0b0011</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

### SIMDHP, bits [23:20]

Advanced SIMD Half Precision. Indicates the level of half-precision floating-point support. Defined values are:

<table>
<thead>
<tr>
<th>SIMDHP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SIMD half-precision conversion instructions are supported for conversion between single-precision and half-precision.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As for 0b0001, and adds support for half-precision floating-point arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are:

- 0b0000 in an implementation without SIMD floating-point support.
- 0b0010 in an implementation with SIMD floating-point support that does not include the FEAT_FP16 extension.
- 0b0011 in an implementation with SIMD floating-point support that includes the FEAT_FP16 extension.

The level of support indicated by this field must be equivalent to the level of support indicated by the FPHP field, meaning the permitted values are:

<table>
<thead>
<tr>
<th>Half Precision instructions supported</th>
<th>FPHP</th>
<th>SIMDHP</th>
</tr>
</thead>
<tbody>
<tr>
<td>No support</td>
<td>0b0000</td>
<td>0b0000</td>
</tr>
<tr>
<td>Conversions only</td>
<td>0b0010</td>
<td>0b0001</td>
</tr>
<tr>
<td>Conversions and arithmetic</td>
<td>0b0011</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

### SIMDSP, bits [19:16]

Advanced SIMD Single Precision. Indicates whether the Advanced SIMD and floating-point implementation provides single-precision floating-point instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDSP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented. This value is permitted only if the SIMDInt field is 0b0001.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.
**SIMDInt, bits [15:12]**

Advanced SIMD Integer. Indicates whether the Advanced SIMD and floating-point implementation provides integer instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDInt</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**SIMDLS, bits [11:8]**

Advanced SIMD Load/Store. Indicates whether the Advanced SIMD and floating-point implementation provides load/store instructions. Defined values are:

<table>
<thead>
<tr>
<th>SIMDLS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**FPDNaN, bits [7:4]**

Default NaN mode. Indicates whether the floating-point implementation provides support only for the Default NaN mode. Defined values are:

<table>
<thead>
<tr>
<th>FPDNaN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or hardware supports only the Default NaN mode.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Hardware supports propagation of NaN values.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**FPFtZ, bits [3:0]**

Flush to Zero mode. Indicates whether the floating-point implementation provides support only for the Flush-to-Zero mode of operation. Defined values are:

<table>
<thead>
<tr>
<th>FPFtZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or hardware supports only the Flush-to-Zero mode of operation.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Hardware supports full denormalized number arithmetic.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0001.

**Accessing the MVFR1**

Accesses to this register use the following encodings:

```
VMRS{<c>}{<q>} <Rt>, <spec_reg>
```

<table>
<thead>
<tr>
<th>reg</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && (ELUsingAArch32(EL3) && SCR.NS == '1' &&
        NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x08);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x08);
    else
        return MVFR1;
    end
elsif PSTATE.EL == EL2 then
    if HCR_EL2.E2H == '0' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ((ELUsingAArch32(EL3) && SCR.NS == '1' &&
        HCPTR.TCP10 == '1') ||
        HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    else
        return MVFR1;
    end
elsif PSTATE.EL == EL3 then
    if CPACR.cp10 == '00' then
        UNDEFINED;
    else
        return MVFR1;
    end
end


**MVFR2, Media and VFP Feature Register 2**

The MVFR2 characteristics are:

**Purpose**

Describes the features provided by the AArch32 Advanced SIMD and Floating-point implementation.

Must be interpreted with MVFR0 and MVFR1.

For general information about the interpretation of the ID registers see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

AArch32 System register MVFR2 bits [31:0] are architecturally mapped to AArch64 System register MVFR2_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to MVFR2 are UNDEFINED.

Implemented only if the implementation includes Advanced SIMD and floating-point instructions.

**Attributes**

MVFR2 is a 32-bit register.

**Field descriptions**

The MVFR2 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**Bits [31:8]**

Reserved, RES0.

**FPMisc, bits [7:4]**

Indicates whether the floating-point implementation provides support for miscellaneous VFP features.

<table>
<thead>
<tr>
<th>FPMisc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or no support for miscellaneous features.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for Floating-point selection.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and Floating-point Conversion to Integer with Directed Rounding modes.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, and Floating-point Round to Integer Floating-point.</td>
</tr>
<tr>
<td>0b0100</td>
<td>As 0b0011, and Floating-point MaxNum and MinNum.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0100.

**SIMDMisc, bits [3:0]**

Indicates whether the Advanced SIMD implementation provides support for miscellaneous Advanced SIMD features.
<table>
<thead>
<tr>
<th>SIMDMisc</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Not implemented, or no support for miscellaneous features.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Floating-point Conversion to Integer with Directed Rounding modes.</td>
</tr>
<tr>
<td>0b0010</td>
<td>As 0b0001, and Floating-point Round to Integer Floating-point.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, and Floating-point MaxNum and MinNum.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the permitted values are 0b0000 and 0b0011.

**Accessing the MVFR2**

Accesses to this register use the following encodings:

```plaintext
VMRS{<c>}{<q>} <Rt>, <spec_reg>
```

<table>
<thead>
<tr>
<th>reg</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0101</td>
<td></td>
</tr>
</tbody>
</table>

```plaintext
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if (ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || CPACR.cp10 == '00' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H != '1' && CPTR_EL2.TFP == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.E2H == '1' && CPTR_EL2.FPEN == 'x0' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x07);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && ((ELUsingAArch32(EL3) && SCR.NS == '1' && NSACR.cp10 == '0') || HCPTR.TCP10 == '1') then
        AArch32.TakeHypTrapException(0x08);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID3 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x08);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID3 == '1' then
        AArch32.TakeHypTrapException(0x00);
    else
        return MVFR2;
    endif
else
    return MVFR2;
endif
```
NMRR, Normal Memory Remap Register

The NMRR characteristics are:

**Purpose**

Provides additional mapping controls for memory regions that are mapped as Normal memory by their entry in the PRRR.

Used in conjunction with the PRRR.

**Configuration**

AArch32 System register NMRR bits [31:0] are architecturally mapped to AArch64 System register MAIR_EL1[63:32] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register NMRR bits [31:0] are architecturally mapped to AArch32 System register MAIR1[31:0] when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register NMRR bits [31:0] (NMRR_S) are architecturally mapped to AArch32 System register MAIR1[31:0] (MAIR1_S) when EL3 is using AArch32.

AArch32 System register NMRR bits [31:0] (NMRR_NS) are architecturally mapped to AArch32 System register MAIR1[31:0] (MAIR1_NS) when EL3 is using AArch32.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to NMRR are UNDEFINED.

MAIR1 and NMRR are the same register, with a different view depending on the value of TTBCR.EAE:

- When it is set to 0, the register is as described in NMRR.
- When it is set to 1, the register is as described in MAIR1.

**Attributes**

NMRR is a 32-bit register.

**Field descriptions**

The NMRR bit assignments are:

**When TTBCR.EAE == 0:**

<table>
<thead>
<tr>
<th>OR7</th>
<th>OR6</th>
<th>OR5</th>
<th>OR4</th>
<th>OR3</th>
<th>OR2</th>
<th>OR1</th>
<th>OR0</th>
<th>IR7</th>
<th>IR6</th>
<th>IR5</th>
<th>IR4</th>
<th>IR3</th>
<th>IR2</th>
<th>IR1</th>
<th>IR0</th>
</tr>
</thead>
</table>

**OR<n>**, bits [2n+17:2n+16], for n = 7 to 0

Outer Cacheable property mapping for memory attributes n, if the region is mapped as Normal memory by the PRRR.TR<n> entry. n is the value of the TEX[0], C, and B bits concatenated. The possible values of this field are:

<table>
<thead>
<tr>
<th>OR&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Region is Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Region is Write-Back, Write-Allocate.</td>
</tr>
<tr>
<td>0b10</td>
<td>Region is Write-Through, no Write-Allocate.</td>
</tr>
<tr>
<td>0b11</td>
<td>Region is Write-Back, no Write-Allocate.</td>
</tr>
</tbody>
</table>

The meaning of the field with n = 6 is IMPLEMENTATION DEFINED and might differ from the meaning given here. This is because the meaning of the attribute combination {TEX[0] = 1, C = 1, B = 0} is IMPLEMENTATION DEFINED.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**IR\(<n>\>, \text{bits } [2n+1:2n], \text{for } n = 7 \text{ to } 0**

Inner Cacheable property mapping for memory attributes \(n\), if the region is mapped as Normal memory by the PRRR.TR\(<n>\) entry. \(n\) is the value of the TEX[0], C, and B bits concatenated. The possible values of this field are:

<table>
<thead>
<tr>
<th>IR(&lt;n&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Region is Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Region is Write-Back, Write-Allocate.</td>
</tr>
<tr>
<td>0b10</td>
<td>Region is Write-Through, no Write-Allocate.</td>
</tr>
<tr>
<td>0b11</td>
<td>Region is Write-Back, no Write-Allocate.</td>
</tr>
</tbody>
</table>

The meaning of the field with \(n = 6\) is IMPLEMENTATION DEFINED and might differ from the meaning given here. This is because the meaning of the attribute combination \{TEX[0] = 1, C = 1, B = 0\} is IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the NMRR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc}>, \{\#\}<\text{opc1}>, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}>, \{\#\}<\text{opc2}>\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    if TTBCR.EAE == '1' then
      return MAIR1_NS;
    else
      return NMRR_NS;
    end if;
  else
    if TTBCR.EAE == '1' then
      return MAIR1;
    else
      return NMRR;
    end if;
  end if;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    if TTBCR.EAE == '1' then
      return MAIR1_NS;
    else
      return NMRR_NS;
    end if;
  else
    if TTBCR.EAE == '1' then
      return MAIR1;
    else
      return NMRR;
    end if;
  endif;
else if PSTATE.EL == EL3 then
  if TTBCR.EAE == '1' then
    if SCR.NS == '0' then
      return MAIR1_S;
    else
      return MAIR1_NS;
    end if;
  else
    if SCR.NS == '0' then
      return NMRR_S;
    else
      return NMRR_NS;
  end if;
else
  return NMRR_NS;
end if;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
            MAIR1_NS = R[t];
        else
            NMRR_NS = R[t];
        end
    else
        if TTBCR.EAE == '1' then
            MAIR1 = R[t];
        else
            NMRR = R[t];
        end
    end
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
            MAIR1_NS = R[t];
        else
            NMRR_NS = R[t];
        end
    else
        if TTBCR.EAE == '1' then
            MAIR1 = R[t];
        else
            NMRR = R[t];
        end
    end
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    elsif TTBCR.EAE == '1' then
        if SCR.NS == '0' then
            MAIR1_S = R[t];
        else
            MAIR1_NS = R[t];
        end
    else
        if SCR.NS == '0' then
            NMRR_S = R[t];
        else
            NMRR_NS = R[t];
    end
NSACR, Non-Secure Access Control Register

The NSACR characteristics are:

**Purpose**

When EL3 is implemented and can use AArch32, defines the Non-secure access permissions to Trace, Advanced SIMD and floating-point functionality. Also includes IMPLEMENTATION DEFINED bits that can define Non-secure access permissions for IMPLEMENTATION DEFINED functionality.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to NSACR are UNDEFINED.

**Note**

In AArch64 state, the NSACR controls are replaced by controls in CPTR_EL3.

**Attributes**

NSACR is a 32-bit register.

**Field descriptions**

The NSACR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | NSTRCDIS | RES0 | IMPLEMENTATION DEFINED | NSASEDIS | RES0 | cp11 | cp10 | RES0 |

If EL3 is implemented and is using AArch64 then:

- Any read of the NSACR from Non-secure EL2 or Non-secure EL1 returns a value of 0x00000C00.
- Any read or write to NSACR from Secure EL1 is trapped as an exception to EL3.

If EL3 is not implemented, then any read of the NSACR from EL2 or EL1 returns a value of 0x00000C00.

**Bits [31:21]**

Reserved, RES0.

**NSTRCDIS, bit [20]**

Disables Non-secure System register accesses to all implemented trace registers.

<table>
<thead>
<tr>
<th>NSTRCDIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on:</td>
</tr>
<tr>
<td></td>
<td>• System register access to implemented trace registers.</td>
</tr>
<tr>
<td></td>
<td>• The behavior of CPACR TRCDIS and HCPTR TTA.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure System register accesses to all implemented trace registers are disabled, meaning:</td>
</tr>
<tr>
<td></td>
<td>• CPACR TRCDIS behaves as RAO/WI in Non-secure state, regardless of its actual value.</td>
</tr>
<tr>
<td></td>
<td>• HCPTR TTA behaves as RAO/WI, regardless of its actual value.</td>
</tr>
</tbody>
</table>
The implementation of this field must correspond to the implementation of the CPACR.TRCDIS field:

- If CPACR.TRCDIS is RAZ/WI, this field is RAZ/WI.
- If CPACR.TRCDIS is RW, this field is RW.

**Note**
- The ETMv4 architecture does not permit EL0 to access the trace registers. If the PE trace unit implements FEAT_ETMv4, EL0 accesses to the trace registers are **UNDEFINED**.
- The architecture does not provide Non-secure access controls on trace register accesses through the optional memory-mapped external debug interface.

System register accesses to the trace registers can have side-effects. When a System register access is trapped, any side-effects that are normally associated with the access do not occur before the exception is taken.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Bit [19]**

Reserved, RES0.

**IMPLEMENTATION DEFINED, bits [18:16]**

IMPLEMENTATION DEFINED.

**NSASEDIS, bit [15]**

Disables Non-secure access to the Advanced SIMD functionality.

<table>
<thead>
<tr>
<th>NSASEDIS</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0      | This control has no effect on:  
|          | • Non-secure access to Advanced SIMD functionality.  
|          | • The behavior of CPACR.ASEDIS and HCPTR.TASE. |
| 0b1      | Non-secure access to the Advanced SIMD functionality is disabled, meaning:  
|          | • CPACR.ASEDIS behaves as RAO/WI in Non-secure state, regardless of its actual value.  
|          | • HCPTR.TASE behaves as RAO/WI, regardless of its actual value. |

The implementation of this field must correspond to the implementation of the CPACR.ASEDIS field:

- If CPACR.ASEDIS is RES0, this field is RES0. If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0.
- If CPACR.ASEDIS is RAZ/WI, this field is RAZ/WI.
- If CPACR.ASEDIS is RW, this field is RW.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Bits [14:12]**

Reserved, RES0.

**cp11, bit [11]**

The value of this field is ignored. If this field is programmed with a different value to the cp10 field then this field is **UNKNOWN** on a direct read of the NSACR.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally **UNKNOWN** value.

Page 2848
 cp10, bit [10]

Enable Non-secure access to the Advanced SIMD and floating-point features. Possible values of the fields are:

<table>
<thead>
<tr>
<th>cp10</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0  | Advanced SIMD and floating-point features can be accessed only from Secure state. Any attempt to access this functionality from Non-secure state is UNDEFINED. When the PE is in Non-secure state:  
  - The CPACR (cp11, cp10) fields ignore writes and read as 0b00, access denied.  
  - The HCPTR (TCP11, TCP10) fields behave as RAO/WI, regardless of their actual values. |
| 0b1  | Advanced SIMD and floating-point features can be accessed from both Security states. |

If Non-secure access to the Advanced SIMD and floating-point functionality is enabled, the CPACR must be checked to determine the level of access that is permitted.

The Advanced SIMD and floating-point features controlled by these fields are:

- Execution of any floating-point or Advanced SIMD instruction.
- Any access to the Advanced SIMD and floating-point registers D0-D31 and their views as S0-S31 and Q0-Q15.
- Any access to the FPSCR, FPSID, MVFR0, MVFR1, MVFR2, or FPEXC System registers.

If the implementation does not include Advanced SIMD and floating-point functionality, this field is RES0.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally UNKNOWN value.

Bits [9:0]

Reserved, RES0.

**Accessing the NSACR**

Accesses to this register use the following encodings:

\[ MRC\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>{, \{#\}<opc2>} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp; HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp; HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif !ELUsingAArch32(EL2) &amp; SCR_EL3.<NS,EEL2> == '01' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif !ELUsingAArch32(EL3) &amp; SCR_EL3.NS == '0' then
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  elsif !HaveEL(EL3) || (!ELUsingAArch32(EL3) &amp; SCR_EL3.NS == '1') then
    return Zeros(20):'1100':Zeros(8);
  else
    return NSACR;
elsif PSTATE.EL == EL2 then
  if !EL2Enabled() &amp; ELUsingAArch32(EL3) &amp; SCR_EL3.NS == '1' then
    return Zeros(20):'1100':Zeros(8);
  else
    return NSACR;
elsif PSTATE.EL == EL3 then
  return NSACR;
endif
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif !ELUsingAAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    UNDEFINED;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        NSACR = R[t];
PAR, Physical Address Register

The PAR characteristics are:

**Purpose**

Returns the output address (OA) from an Address translation instruction that executed successfully, or fault information if the instruction did not execute successfully.

**Configuration**

AArch32 System register PAR bits [63:0] are architecturally mapped to AArch64 System register PAR_EL1[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to PAR are undefined.

PAR is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, accesses read and write bits[31:0] and do not modify bits[63:32].

The Configurations section specifies the cases where each PAR format is used.

PAR is accessed as a 32-bit value:

- When the PE is not in Hyp mode and is using the Short-descriptor translation table format.
- When the PE is in Hyp mode and executes an ATS12NSOPR, ATS12NSOPW, ATS12NSOUR, or ATS12NSOUW instruction and the value of HCR.VM is 0 and the value of TTBCR.EAE is 0.

In these cases, PAR[63:32] is RES0.

Otherwise, the PAR is accessed as a 64-bit value, if any of the following is true:

- When using the Long-descriptor translation table format.
- If the stage 1 address translation is disabled and TTBCR.EAE is set to 1.
- In an implementation that includes EL2, for the result of an ATS1Cxx instruction performed from Hyp mode.

For PL1&0 stage 1 translations, TTBCR.EAE selects the translation table format.

**Attributes**

PAR is a 64-bit register.

**Field descriptions**

The PAR bit assignments are:

**When the instruction returned a 32-bit value to the PAR, PAR.F==0:**

<table>
<thead>
<tr>
<th>PA</th>
<th>LPAE</th>
<th>NOS</th>
<th>NS</th>
<th>IMPLEMENTATION</th>
<th>DEFINED</th>
<th>SHInner[2:0]</th>
<th>Outer[1:0]</th>
<th>SS</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44</td>
<td>43 42 41 40</td>
<td>39 38 37 36</td>
<td>35 34 33 32</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12</td>
<td>11 10 9 8</td>
<td>7 6 5 4</td>
<td>3 2 1 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This section describes the register value returned by the successful execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

On a successful conversion, the PAR can return a value that indicates the resulting attributes, rather than the values that appear in the translation table descriptors. More precisely:
Memory attribute fields are permitted to report the resulting attributes, as determined by any permitted implementation choices and any applicable configuration bits, instead of reporting the values that appear in the translation table descriptors. This applies to the NOS, SH, Inner, and Outer fields.

- See the NS bit description for constraints on the value it returns.

**Bits [63:32]**

Reserved, RES0.

**PA, bits [31:12]**

Output address. The output address (OA) corresponding to the supplied input address. This field returns address bits[31:12].

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**LPAE, bit [11]**

When updating the PAR with the result of the translation operation, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Short-descriptor translation table format used. This means the PAR returned a 32-bit value.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NOS, bit [10]**

Not Outer Shareable. When the returned value of PAR.SH is 1, indicates the Shareability attribute for the physical memory region:

<table>
<thead>
<tr>
<th>NOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Memory region is Outer Shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory region is Inner Shareable.</td>
</tr>
</tbody>
</table>

When the returned value of PAR.SH is 0 the value returned to this field is **UNKNOWN**.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NS, bit [9]**

Non-secure. The NS attribute for a translation table entry from a Secure translation regime.

For a result from a Secure translation regime, this bit reflects the Security state of the physical address space of the translation. This means it reflects the effect of the NSTable bits of earlier levels of the translation table walk if those NSTable bits have an effect on the translation.

For a result from a Non-secure translation regime, this bit is **UNKNOWN**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IMPLEMENTATION DEFINED, bit [8]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**SH, bit [7]**

Shareability. Indicates whether the physical memory region is Non-shareable:
SH | Meaning
--- | ---
0b0 | Memory is Non-shareable.
0b1 | Memory is shareable, and PAR.NOS indicates whether the region is Outer Shareable or Inner Shareable.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Inner[2:0], bits [6:4]**

Inner cacheability attribute for the region. Permitted values are:

<table>
<thead>
<tr>
<th>Inner[2:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Non-cacheable.</td>
</tr>
<tr>
<td>0b001</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b011</td>
<td>Device-nGnRE.</td>
</tr>
<tr>
<td>0b101</td>
<td>Write-Back, Write-Allocate.</td>
</tr>
<tr>
<td>0b110</td>
<td>Write-Through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Write-Back, no Write-Allocate.</td>
</tr>
</tbody>
</table>

The values 0b010 and 0b100 are reserved.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Outer[1:0], bits [3:2]**

Outer cacheability attribute for the region. Permitted values are:

<table>
<thead>
<tr>
<th>Outer[1:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Write-Back, Write-Allocate.</td>
</tr>
<tr>
<td>0b10</td>
<td>Write-Through, no Write-Allocate.</td>
</tr>
<tr>
<td>0b11</td>
<td>Write-Back, no Write-Allocate.</td>
</tr>
</tbody>
</table>

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**SS, bit [1]**

Supersection. Used to indicate if the result is a Supersection:

<table>
<thead>
<tr>
<th>SS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Result is not a Supersection. PAR[31:12] contains OA[31:12].</td>
</tr>
</tbody>
</table>
| 0b1 | Result is a Supersection, and:
  • PAR[31:24] contains OA[31:24].
  • PAR[15:12] contains 0b0000.
  If an implementation supports less than 40 bits of physical address, the bits in the PAR field that correspond to physical address bits that are not implemented are UNKNOWN. |

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**F, bit [0]**

Indicates whether the instruction performed a successful address translation.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Address translation completed successfully.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## When the instruction returned a 32-bit value to the PAR, PAR.F==1:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-32</td>
<td>Reserved</td>
<td>RES0</td>
<td>IMPLEMENTATION DEFINED, bits [31:16]</td>
</tr>
<tr>
<td>31-24</td>
<td>Reserved</td>
<td>RES0</td>
<td>IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>23-22</td>
<td>LPAE</td>
<td>RES0</td>
<td>When updating the PAR with the result of the translation operation, this bit is set as follows:</td>
</tr>
<tr>
<td>21-12</td>
<td>Reserved</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>FS[5]</td>
<td>RES0</td>
<td>Fault status bits, external abort type. Provides an IMPLEMENTATION DEFINED classification of an External abort. Values are as in the DFSR.EXT field when using the Short-descriptor translation table format.</td>
</tr>
<tr>
<td>10-7</td>
<td>FS[4:0]</td>
<td>RES0</td>
<td>For aborts other than External aborts this bit always returns 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

---

This section describes the register value returned by a fault on the execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

### Bits [63:32]

- Reserved, RES0.

### IMPLEMENTATION DEFINED, bits [31:16]

- IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [15:12]

- Reserved, RES0.

### LPAE, bit [11]

- When updating the PAR with the result of the translation operation, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Short-descriptor translation table format used. This means the PAR returned a 32-bit value.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [10:7]

- Reserved, RES0.

### FS[5], bit [6]

- Fault status bits, external abort type. Provides an IMPLEMENTATION DEFINED classification of an External abort. Values are as in the DFSR.EXT field when using the Short-descriptor translation table format.

  In an implementation that does not provide any classification of External aborts, this bit is RES0.

  For aborts other than External aborts this bit always returns 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### FS[4:0], bits [5:1]

- Fault status bits. Values are as in the DFSR.FS field when using the Short-descriptor translation table format.
On a Warm reset, this field resets to an **UNKNOWN** value.

**F, bit [0]**

Indicates whether the instruction performed a successful address translation.

<table>
<thead>
<tr>
<th>F</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Address translation aborted.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When the instruction returned a 64-bit value to the PAR, PAR.F==0:**

<table>
<thead>
<tr>
<th>ATTR</th>
<th>RES0</th>
<th>PA</th>
<th>IMPLEMENTATION DEFINED</th>
<th>NS</th>
<th>SH</th>
<th>RES0</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
</tr>
<tr>
<td>55</td>
<td>54</td>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
</tr>
<tr>
<td>47</td>
<td>46</td>
<td>45</td>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
</tr>
<tr>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

This section describes the register value returned by the successful execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

On a successful conversion, the PAR can return a value that indicates the resulting attributes, rather than the values that appear in the translation table descriptors. More precisely:

- Memory attribute fields are permitted to report the resulting attributes, as determined by any permitted implementation choices and any applicable configuration bits, instead of reporting the values that appear in the translation table descriptors. This applies to the ATTR and SH fields.
- See the NS bit description for constraints on the value it returns.

**ATTR, bits [63:56]**

Memory attributes for the returned output address. This field uses the same encoding as the Attr<n> fields in **MAIR0** and **MAIR1**.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Bits [55:40]

Reserved, RES0.

PA, bits [39:12]

Output address. The output address (OA) corresponding to the supplied input address. This field returns address bits [39:12].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

LPAE, bit [11]

When updating the PAR with the result of the translation operation, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Long-descriptor translation table format used. This means the PAR returned a 64-bit value.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IMPLEMENTATION DEFINED, bit [10]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

NS, bit [9]

Non-secure. The NS attribute for a translation table entry from a Secure translation regime.

For a result from a Secure translation regime, this bit reflects the Security state of the physical address space of the translation. This means it reflects the effect of the NSTable bits of earlier levels of the translation table walk if those NSTable bits have an effect on the translation.

For a result from a Non-secure translation regime, this bit is UNKNOWN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

SH, bits [8:7]

Shareability attribute, for the returned output address. Permitted values are:

<table>
<thead>
<tr>
<th>SH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

The value 0b01 is reserved.

Note

This field returns the value 0b10 for:

- Any type of Device memory.
- Normal memory with both Inner Non-cacheable and Outer Non-cacheable attributes.

The value returned in this field can be the resulting attribute, as determined by any permitted implementation choices and any applicable configuration bits, instead of the value that appears in the translation table descriptor.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [6:1]
Reserved, RES0.

F, bit [0]
Indicates whether the instruction performed a successful address translation.

F

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

When the instruction returned a 64-bit value to the PAR, PAR.F==1:

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>RES0</td>
</tr>
</tbody>
</table>

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

This section describes the register value returned by a fault on the execution of an Address translation instruction. Software might subsequently write a different value to the register, and that write does not affect the operation of the PE.

IMPLEMENTATION DEFINED, bits [63:56]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IMPLEMENTATION DEFINED, bits [55:52]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IMPLEMENTATION DEFINED, bits [51:48]

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [47:12]
Reserved, RES0.

LPAE, bit [11]
When updating the PAR with the result of the translation operation, this bit is set as follows:

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Long-descriptor translation table format used. This means the PAR returned a 64-bit value.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [10]
Reserved, RES0.
FSTAGE, bit [9]

Indicates the translation stage at which the translation aborted:

<table>
<thead>
<tr>
<th>FSTAGE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Translation aborted because of a fault in the stage 1 translation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Translation aborted because of a fault in the stage 2 translation.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

S2WLK, bit [8]

If this bit is set to 1, it indicates the translation aborted because of a stage 2 fault during a stage 1 translation table walk.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [7]

Reserved, RES0.

FST, bits [6:1]

Fault status field. Values are as in the DFSR.STATUS and IFSR.STATUS fields when using the Long-descriptor translation table format.

<table>
<thead>
<tr>
<th>FST</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000000</td>
<td>Address size fault in translation table base register.</td>
<td></td>
</tr>
<tr>
<td>0b000001</td>
<td>Address size fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000010</td>
<td>Address size fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000011</td>
<td>Address size fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b000101</td>
<td>Translation fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b000110</td>
<td>Translation fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b000111</td>
<td>Translation fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001001</td>
<td>Access flag fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001010</td>
<td>Access flag fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001011</td>
<td>Access flag fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b001101</td>
<td>Permission fault, level 1.</td>
<td></td>
</tr>
<tr>
<td>0b001110</td>
<td>Permission fault, level 2.</td>
<td></td>
</tr>
<tr>
<td>0b001111</td>
<td>Permission fault, level 3.</td>
<td></td>
</tr>
<tr>
<td>0b010101</td>
<td>Synchronous External abort on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b010110</td>
<td>Synchronous External abort on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b010111</td>
<td>Synchronous External abort on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011101</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 1.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011110</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 2.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b011111</td>
<td>Synchronous parity or ECC error on memory access on translation table walk, level 3.</td>
<td>When FEAT_RAS is not implemented</td>
</tr>
<tr>
<td>0b110000</td>
<td>TLB conflict abort.</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [0]

Indicates whether the instruction performed a successful address translation.
Meaning

0b1  Address translation aborted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PAR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{c\}\{q\}\ <\text{coproc}\},\ \{\#\}\{\text{opc1}\},\ <\text{Rt}\},\ <\text{CRn}\},\ <\text{CRm}\},\ \{\#\}\{\text{opc2}\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0111</td>
<td>0b0100</td>
<td>0b000</td>
</tr>
</tbody>
</table>

\[
\text{if PSTATE.EL == EL0 then}
\]
\[
\text{UNDEFINED;}
\]
\[
\text{elsif PSTATE.EL == EL1 then}
\]
\[
\text{if EL2Enabled()} && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then}
\]
\[
\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03);}
\]
\[
\text{elsif EL2Enabled()} && ELUsingAArch32(EL2) && HSTR.T7 == '1' then}
\]
\[
\text{AArch32.TakeHypTrapException(0x03);}
\]
\[
\text{elsif HaveEL(EL3) && ELUsingAArch32(EL3) then}
\]
\[
\text{return PAR_NS<31:0>;}\]
\[
\text{elsif PSTATE.EL == EL2 then}
\]
\[
\text{if HaveEL(EL3) && ELUsingAArch32(EL3) then}
\]
\[
\text{return PAR_NS<31:0>;}\]
\[
\text{elsif PSTATE.EL == EL3 then}
\]
\[
\text{if SCR.NS == '0' then}
\]
\[
\text{return PAR_S<31:0>;}\]
\[
\text{elsif PSTATE.EL == EL0 then}
\]
\[
\text{UNDEFINED;}
\]
\[
\text{elsif PSTATE.EL == EL1 then}
\]
\[
\text{if EL2Enabled()} && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then}
\]
\[
\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03);}
\]
\[
\text{elsif EL2Enabled()} && ELUsingAArch32(EL2) && HSTR.T7 == '1' then}
\]
\[
\text{AArch32.TakeHypTrapException(0x03);}
\]
\[
\text{elsifHaveEL(EL3) && ELUsingAArch32(EL3) then}
\]
\[
\text{PAR_NS = ZeroExtend(R[t]);}
\]
\[
\text{else}
\]
\[
\text{PAR = ZeroExtend(R[t]);}
\]
\[
\text{elsif PSTATE.EL == EL2 then}
\]
\[
\text{if HaveEL(EL3) && ELUsingAArch32(EL3) then}
\]
\[
\text{PAR_NS = ZeroExtend(R[t]);}
\]
\[
\text{else}
\]
\[
\text{PAR = ZeroExtend(R[t]);}
\]
\[
\text{elsif PSTATE.EL == EL3 then}
\]
\[
\text{if SCR.NS == '0' then}
\]
\[
\text{PAR_S = ZeroExtend(R[t]);}
\]
\[
\text{else}
\]
\[
\text{PAR_NS = ZeroExtend(R[t]);}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return PAR_NS;
    else
        return PAR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return PAR_NS;
    else
        return PAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        PAR_S = R[t2]:R[t];
    else
        PAR_NS = R[t2]:R[t];
else
    PAR = R[t2]:R[t];

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T7 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T7 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        PAR_NS = R[t2]:R[t];
    else
        PAR = R[t2]:R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        PAR_NS = R[t2]:R[t];
    else
        PAR = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        PAR_S = R[t2]:R[t];
    else
        PAR_NS = R[t2]:R[t];
PMCCFILTR, Performance Monitors Cycle Count Filter Register

The PMCCFILTR characteristics are:

**Purpose**

Determines the modes in which the Cycle Counter, PMCCNTR, increments.

**Configuration**

AArch32 System register PMCCFILTR bits [31:0] are architecturally mapped to AArch64 System register PMCCFILTR_EL0[31:0].

AArch32 System register PMCCFILTR bits [31:0] are architecturally mapped to External register PMCCFILTR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCCFILTR are UNDEFINED.

**Attributes**

PMCCFILTR is a 32-bit register.

**Field descriptions**

The PMCCFILTR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| P  | U  | NSK | NSU | NSH | RES0 |

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMCCFILTR.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMCCFILTR.NSU bit.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.
**NSK, bit [29]**

*When EL3 is implemented:*

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of PMCCFILTR.P, cycles in Non-secure EL1 are counted.
Otherwise, cycles in Non-secure EL1 are not counted.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**NSU, bit [28]**

*When EL3 is implemented:*

Non-secure EL0 (Unprivileged) filtering. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of PMCCFILTR.U, cycles in Non-secure EL0 are counted.
Otherwise, cycles in Non-secure EL0 are not counted.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**NSH, bit [27]**

*When EL2 is implemented:*

EL2 (Hyp mode) filtering bit. Controls counting in EL2.

<table>
<thead>
<tr>
<th>NSH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not count cycles in EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count cycles in EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**Bits [26:0]**

Reserved, RES0.

**Accessing the PMCCFILTR**

PMCCFILTR can also be accessed by using PMXEVTYPER with PMSELR SEL set to 0b11111.

Accesses to this register use the following encodings:
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  end if
  elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end if
  end if
  elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGFR_EL2.PMCCFILTR_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    if Halted() && !ELUsingAArch32(EL1) && MDCR_EL2.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if
  end if
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    if EL2Enabled() && ELUsingAArch32(EL2) && HDFCR.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if
  end if
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCCFILTR;
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then UNDEFINED;
  elsif !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if
  end if
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCCFILTR;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCCFILTR;
  end if
elsif PSTATE.EL == EL3 then
  return PMCCFILTR;
end if

### Values for Table

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b1111</td>
<td>0b111</td>
</tr>
</tbody>
</table>

PMCCFILTR, Performance Monitors Cycle Count Filter Register
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL2.FGTen == '1' && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    if EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL1) && SCR_EL1.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  elsif PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif PMUSERENR.EN == '0' then
    if EL2Enabled() && SCR_EL1.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
  else
    UNDEFINED;
  elsif PMCCFILTR = R[t];
else if PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    if EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif PMCCFILTR = R[t];
else if PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SCR_EL3.TGE == '1' then
    if !ELUsingAArch32(EL2) && SCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  else
    if PMCCFILTR = R[t];
else if PSTATE.EL == EL3 then
  if PMCCFILTR = R[t];
PMCCNTR, Performance Monitors Cycle Count Register

The PMCCNTR characteristics are:

**Purpose**

Holds the value of the processor Cycle Counter, CCNT, that counts processor clock cycles. See 'Time as measured by the Performance Monitors cycle counter' for more information.

**Configuration**

AArch32 System register PMCCNTR bits [63:0] are architecturally mapped to AArch64 System register PMCCNTR_EL0[63:0].

AArch32 System register PMCCNTR bits [63:0] are architecturally mapped to External register PMCCNTR_EL0[63:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCCNTR are UNDEFINED.

PMCCNTR is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, accesses read and write bits [31:0] and do not modify bits [63:32].

All counters are subject to any changes in clock frequency, including clock stopping caused by the WFI and WFE instructions. This means that it is CONSTRAINED UNPREDICTABLE whether or not PMCCNTR continues to increment when clocks are stopped by WFI and WFE instructions.

**Attributes**

PMCCNTR is a 64-bit register.

**Field descriptions**

The PMCCNTR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| CCNT | CCNT |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**CCNT, bits [63:0]**

Cycle count. Depending on the values of PMCR_{LC,D}, this field increments in one of the following ways:

- Every processor clock cycle.
- Every 64th processor clock cycle.

Writing 1 to PMCR.C sets this field to 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMCCNTR**

Accesses to this register use the following encodings:
MRC{<c>}{<q>}  coproc, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then undefined;
    elsif !ELUsingAArch32(EL1) & PMUSERENR_EL0.<CR,EN> == '00' then
        if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        endif
    else
        UNDEFINED;
    endif
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.<E2H,TGE> != '11' & HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL1) & SCR_EL3.FGTeN == '1' & HDFGRT_EL2.PMCCTR_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        return PMCCNTR<31:0>;
    endif
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then undefined;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL1) & MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        endif
    else
        return PMCCNTR<31:0>;
    endif
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then undefined;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return PMCCNTR<31:0>;
    endif
elsif PSTATE.EL == EL3 then
    return PMCCNTR<31:0>;
MCR<<c>>{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1101</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR_SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    elsif ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch32.TakeHypTrapException(0x00);
        end if;
    elsif ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            UNDEFINED;
        end if;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && !HaveEL(EL3) || SCR_EL3.FGTEn == '1' || HDFGWR_EL2.PMCCNTR_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    else
        PMCCNTR = ZeroExtend(R[t]);
    end if;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    else
        PMCCNTR = ZeroExtend(R[t]);
    end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    else
        PMCCNTR = ZeroExtend(R[t]);
    end if;
elsif PSTATE.EL == EL3 then
    PMCCNTR = ZeroExtend(R[t]);
else
    PMCCNTR = ZeroExtend(R[t]);
MRRC(<<c>>{<q>}, {#}<opc1>, <Rt>, <Rt2>, <CRm>)

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1001</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.<CR,EN> == '00' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
        end
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x04);
        end
    else
        return PMCCNTR;
    end
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.<CR,EN> == '00' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x04);
        end
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return PMCCNTR;
        end
    else
        return PMCCNTR;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL3) && PMUSERENR_EL0.<CR,EN> == '00' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x04);
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x04);
        end
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x04);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return PMCCNTR;
        end
    else
        return PMCCNTR;
    end
elsif PSTATE.EL == EL3 then
    return PMCCNTR;
end
PMCCNTR, Performance Monitors Cycle Count Register

MCRR{<c>{<q}> <coproc>, #{<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b1001</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x04);
    end if
  end if
else ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  else
    AArch32.TakeHypTrapException(0x00);
  end if
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x04);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x04);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x04);
  end if
else
  PMCCNTR = R[t2]:R[t];
end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    end if
  else
    PMCCNTR = R[t2]:R[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x04);
    end if
else
  PMCCNTR = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
  PMCCNTR = R[t2]:R[t];
PMCEID0, Performance Monitors Common Event Identification register 0

The PMCEID0 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x0000 to 0x001F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

For more information about the common events and the use of the PMCEIDn registers see 'The PMU event number space and common events'.

**Configuration**

AArch32 System register PMCEID0 bits [31:0] are architecturally mapped to AArch64 System register PMCEID0_EL0[31:0].

AArch32 System register PMCEID0 bits [31:0] are architecturally mapped to External register PMCEID0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCEID0 are **UNDEFINED**.

**Attributes**

PMCEID0 is a 32-bit register.

**Field descriptions**

The PMCEID0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 |

**ID<n>**, bit [n], for n = 31 to 0

ID[n] corresponds to common event n.

For each bit:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**


Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCID<n> registers of that earlier version of the PMU architecture.

### Accessing the PMCID0

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c}\}{<q}> \text{<coproc>, } \{#\text{<opc1>}, \text{<Rt>, <CRn>, <CRm>{, }{#}\text{<opc2>}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch32.TakeHypTrapException(0x00);
    end if
    elsif ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        end if
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE != '1' && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x00);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if
        else
            return PMCEID0;
        end if
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if
        else
            return PMCEID0;
        end if
    elsif PSTATE.EL == EL3 then
        return PMCEID0;
    end if

PMCEID0, Performance Monitors Common Event Identification register 0
The PMCEID1 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x0020 to 0x003F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

---

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

---

For more information about the common events and the use of the PMCEIDn registers see 'The PMU event number space and common events'.

**Configuration**

AArch32 System register PMCEID1 bits [31:0] are architecturally mapped to AArch64 System register PMCEID1_EL0[31:0].

AArch32 System register PMCEID1 bits [31:0] are architecturally mapped to External register PMCEID1[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCEID1 are **UNDEFINED**.

**Attributes**

PMCEID1 is a 32-bit register.

**Field descriptions**

The PMCEID1 bit assignments are:

| 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**ID<n>, bit [n], for n = 31 to 0**

ID[n] corresponds to common event (0x0020 + n).

For each bit:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

---

**Note**
Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<\text{n}> registers of that earlier version of the PMU architecture.

## Accessing the PMCEID1

Accesses to this register use the following encodings:

\[
\text{MRC}\{c\}\{q\}\ <\text{coproc}, \{#\}\text{opc1}, <\text{Rt}, <\text{CRn}, <\text{CRm}\{, \{#\}\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b111</td>
</tr>
</tbody>
</table>

PMCEID1, Performance Monitors Common Event Identification register 1
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end;
    end;
    elsif EL2Enabled() && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        end;
    end;
else
    return PMCEID1;
end;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end;
    else
        return PMCEID1;
    end;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end;
    else
        return PMCEID1;
    end;
elsif PSTATE.EL == EL3 then
    return PMCEID1;
The PMCEID2 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x4000 to 0x401F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

---

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

For more information about the common events and the use of the PMCEIDn registers see 'The PMU event number space and common events'.

**Configuration**

AArch32 System register PMCEID2 bits [31:0] are architecturally mapped to AArch64 System register PMCEID0_EL0[63:32].

AArch32 System register PMCEID2 bits [31:0] are architecturally mapped to External register PMCEID2[63:32].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3p1 is implemented. Otherwise, direct accesses to PMCEID2 are **UNDEFINED**.

**Attributes**

PMCEID2 is a 32-bit register.

**Field descriptions**

The PMCEID2 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhi31</td>
<td>Dhi30</td>
<td>Dhi29</td>
<td>Dhi28</td>
<td>Dhi27</td>
<td>Dhi26</td>
<td>Dhi25</td>
<td>Dhi24</td>
<td>Dhi23</td>
<td>Dhi22</td>
<td>Dhi21</td>
<td>Dhi20</td>
<td>Dhi19</td>
<td>Dhi18</td>
<td>Dhi17</td>
<td>Dhi16</td>
<td>Dhi15</td>
</tr>
</tbody>
</table>

**IDhi<n>**, bit [n], for n = 31 to 0

IDhi[n] corresponds to common event (0x4000 + n).

For each bit:

<table>
<thead>
<tr>
<th>IDhi&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

---

**Note**
Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID\textless n\textgreater registers of that earlier version of the PMU architecture.

### Accessing the PMCEID2

Accesses to this register use the following encodings:

MRC\{c\}\{q\} \langle coproc \rangle, \{#\}\langle opc1 \rangle, \langle Rt \rangle, \langle CRn \rangle, \langle CRm \rangle, \{#\}\langle opc2 \rangle

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b101</td>
<td>0b110</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end
    else
      return PMCEID2;
    end
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end
    else
      return PMCEID2;
    end
  elsif PSTATE.EL == EL3 then
    return PMCEID2;
PMCEID3, Performance Monitors Common Event Identification register 3

The PMCEID3 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x4020 to 0x403F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

---

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

---

For more information about the common events and the use of the PMCEIDn registers see 'The PMU event number space and common events'.

**Configuration**

AArch32 System register PMCEID3 bits [31:0] are architecturally mapped to AArch64 System register PMCEID1_EL0[63:32].

AArch32 System register PMCEID3 bits [31:0] are architecturally mapped to External register PMCEID3[63:32].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3p1 is implemented. Otherwise, direct accesses to PMCEID3 are **UNDEFINED**.

**Attributes**

PMCEID3 is a 32-bit register.

**Field descriptions**

The PMCEID3 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhi31</td>
<td>Dhi30</td>
<td>Dhi29</td>
<td>Dhi28</td>
<td>Dhi27</td>
<td>Dhi26</td>
<td>Dhi25</td>
<td>Dhi24</td>
<td>Dhi23</td>
<td>Dhi22</td>
<td>Dhi21</td>
<td>Dhi20</td>
<td>Dhi19</td>
<td>Dhi18</td>
<td>Dhi17</td>
<td>Dhi16</td>
<td>Dhi15</td>
</tr>
</tbody>
</table>

IDhi<n>, bit [n], for n = 31 to 0

IDhi[n] corresponds to common event (0x4020 + n).

For each bit:

<table>
<thead>
<tr>
<th>IDhi&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

---

**Note**
Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n> registers of that earlier version of the PMU architecture.

## Accessing the PMCEID3

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \ <\text{coproc}, \{#\}<\text{opc1}, \ <Rt>, \ <\text{CRn}, \ <\text{CRm}\} \{, \{#\}<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b101</td>
<td>0b110</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERERN.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  elself ELUsingAArch32(EL1) && PMUSERERN.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end if
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCEID3;
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCEID3;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCEID3;
  end if
elsif PSTATE.EL == EL3 then
  return PMCEID3;
PMCNTENCLR, Performance Monitors Count Enable Clear register

The PMCNTENCLR characteristics are:

**Purpose**

Disables the Cycle Count Register, **PMCCNTR**, and any implemented event counters **PMEVCNTR<n>**. Reading this register shows which counters are enabled.

PMCNTENCLR is used in conjunction with the **PMCNTENSET** register.

**Configuration**

AArch32 System register PMCNTENCLR bits [31:0] are architecturally mapped to AArch64 System register **PMCNTENCLR_EL0[31:0]**.

AArch32 System register PMCNTENCLR bits [31:0] are architecturally mapped to External register **PMCNTENCLR_EL0[31:0]**.

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCNTENCLR are **UNDEFINED**.

**Attributes**

PMCNTENCLR is a 32-bit register.

**Field descriptions**

The PMCNTENCLR bit assignments are:

|---|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**C, bit [31]**

**PMCCNTR** disable bit. Disables the cycle counter register.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, disables the cycle counter.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**P<n>, bit [n], for n = 30 to 0**

Event counter disable bit for **PMEVCNTR<n>**.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in **MDCR_EL2.HPMN** if EL2 is using AArch64, or in **HDCR.HPMN** if EL2 is using AArch32. Otherwise, N is the value in **PMCR.N**.
### PMCNTENCLR, Performance Monitors Count Enable Clear register

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt; is enabled. When written, disables PMEVCNTR&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the PMCNTENCLR

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#<\text{opc2}>\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
    elsif EL2Enabled() && EL3 == '0' then
      if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
        AArch32.TakeHypTrapException(0x00);
      else
        UNDEFINED;
      end if
    end if
  elsif ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if
  elsif EL2Enabled() && !ELUsingAArch32(EL1) && HSTR_EL2.T9 == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
      else
        UNDEFINED;
      end if
    end if
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCNTENCLR;
  end if
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCNTENCLR;
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && EL3 == '0' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    return PMCNTENCLR;
  end if
elsif PSTATE.EL == EL3 then
  return PMCNTENCLR;
else
  return PMCNTENCLR;
end if

PMCNTENCLR, Performance Monitors Count Enable Clear register
MCR\{<c>\}{<q>} \{<coproc>, \{#}<opc1>, <Rt>, <CRn>, <CRm}\{, \{#}<opc2>\}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    elsef EL2Enabled() && ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
            AArch32.TakeHypTrapException(0x00);
        else
            UNDEFINED;
        end if;
    else
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.<E2H,TGE> != '1' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif PMCNTENCLR != R[t];
else
    AArch32SystemAccessTrap(EL3, 0x03);
end if;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && !EDSCR.SDD == '1' then
            UNDEFINED;
        elsif PMCNTENCLR != R[t];
else
    AArch32SystemAccessTrap(EL3, 0x03);
end if;
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
else
    PMCNTENCLR = R[t];
elsif PSTATE.EL == EL3 then
    PMCNTENCLR = R[t];
else
    PMCNTENCLR = R[t];
else
    PMCNTENCLR = R[t];
end if;
else
    PMCNTENCLR = R[t];
end if;
PMCNTENSET, Performance Monitors Count Enable Set register

The PMCNTENSET characteristics are:

**Purpose**

Enables the Cycle Count Register, PMCCNTR, and any implemented event counters PMEVCNTR<n>. Reading this register shows which counters are enabled.

PMCNTENSET is used in conjunction with the PMCNTENCLR register.

**Configuration**

AArch32 System register PMCNTENSET bits [31:0] are architecturally mapped to AArch64 System register PMCNTENSET_EL0[31:0].

AArch32 System register PMCNTENSET bits [31:0] are architecturally mapped to External register PMCNTENSET_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCNTENSET are **UNDEFINED**.

**Attributes**

PMCNTENSET is a 32-bit register.

**Field descriptions**

The PMCNTENSET bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**C, bit [31]**

**PMCCNTR** enable bit. Enables the cycle counter register.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, enables the cycle counter.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**P<n>, bit [n], for n = 30 to 0**

Event counter enable bit for PMEVCNTR<n>.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN if EL2 is using AArch64, or in HDCR.HPMN if EL2 is using AArch32. Otherwise, N is the value in PMCR.N.
<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt; event counter is enabled. When written, enables PMEVCNTR&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMCNTENSET**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 2899
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return PMCNTENSET;
  end if;
else
  if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && HDCR.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if;
    else
      return PMCNTENSET;
    end if;
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if;
    else
      return PMCNTENSET;
    end if;
  elsif PSTATE.EL == EL3 then
    return PMCNTENSET;
  end if;
else
  return PMCNTENSET;
end if;
PMCNTENSET, Performance Monitors Count Enable Set register

MCR<coproc>, <opc1>, <Rt>, <CRn>, <CRm>{, <opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    else
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if;
elsif EL2Enabled() && PMUSERENR_EL1.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
else
    AArch64.AArch32SystemAccessTrap(EL0, 0x03);
end if;
elsif EL2Enabled() && HSTR_EL2.T9 != '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
            if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x03);
            else
                AArch64.AArch32SystemAccessTrap(EL1, 0x03);
            end if;
        else
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        end if;
    elsif EL2Enabled() && PMUSERENR_EL1.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    else
        AArch64.AArch32SystemAccessTrap(EL0, 0x03);
    end if;
elsif EL2Enabled() && HSTR_EL2.T9 != '1' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if;
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
else
    PMCNTENSET = R[t];
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
else
    PMCNTENSET = R[t];
elsif PSTATE.EL == EL3 then
    PMCNTENSET = R[t];
else
    PMCNTENSET = R[t];
PMCR, Performance Monitors Control Register

The PMCR characteristics are:

**Purpose**

Provides details of the Performance Monitors implementation, including the number of counters implemented, and configures and controls the counters.

**Configuration**

AArch32 System register PMCR bits [31:0] are architecturally mapped to AArch64 System register PMCR_EL0[31:0].

AArch32 System register PMCR bits [7:0] are architecturally mapped to External register PMCR_EL0[7:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMCR are UNDEFINED.

**Attributes**

PMCR is a 32-bit register.

**Field descriptions**

The PMCR bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>IMP</th>
<th>IDCODE</th>
<th>N</th>
<th>RES0</th>
<th>FZO</th>
<th>RES0</th>
<th>LP</th>
<th>LC</th>
<th>DP</th>
<th>X</th>
<th>D</th>
<th>C</th>
<th>P</th>
<th>E</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**IMP, bits [31:24]**

When FEAT_PMUv3p7 is not implemented:

Implementer code.

If this field is zero, then PMCR.IDCODE is RES0 and software must use MIDR to identify the PE.

Otherwise, this field and PMCR.IDCODE identify the PMU implementation to software. The implementer codes are allocated by Arm. A non-zero value has the same interpretation as MIDR. Implementer.

Use of this field is deprecated.

This field reads as an IMPLEMENTATION DEFINED value.

Access to this field is RO.

Otherwise:

Reserved, RAZ.

**IDCODE, bits [23:16]**

When PMCR.IMP != 0x00:

Identification code. Use of this field is deprecated. This field has an IMPLEMENTATION DEFINED value.

Each implementer must maintain a list of identification codes that are specific to the implementer. A specific implementation is identified by the combination of the implementer code and the identification code.
Access to this field is **RO**.

**Otherwise:**

Reserved, **RES0**.

### N, bits [15:11]

Indicates the number of event counters implemented. This value is in the range of 0b00000-0b111111. If the value is 0b00000 then only **PMCCNTR** is implemented. If the value is 0b111111 **PMCCNTR** and 31 event counters are implemented.

In an implementation that includes EL2:

- If EL2 is using AArch32, reads of this field from Non-secure EL1 and Non-secure EL0 return the value of **HDCR.HPMN**.
- If EL2 is using AArch64 and enabled in the current Security state, reads of this field from EL1 and EL0 return the value of **MDCR_EL2.HPMN**.

Access to this field is **RO**.

**Bit [10]**

Reserved, **RES0**.

**FZO, bit [9]**

**When FEAT_PMUv3p7 is implemented:**

Freeze-on-overflow. Stop event counters on overflow.

<table>
<thead>
<tr>
<th>FZO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on overflow.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters do not count when <strong>PMOVSR[(N-1):0]</strong> is nonzero, where N is the value of <strong>HDCR.HPMN</strong> if EL2 is implemented, and <strong>PMCR.N</strong> otherwise.</td>
</tr>
</tbody>
</table>

If EL2 is implemented, then:

- This bit affects the operation of event counters in the range [0 .. **(HDCR.HPMN-1)**].
- If **HDCR.HPMN** is less than **PMCR.N**:
  - This bit does not affect the operation of event counters in the range [**HDCR.HPMN** .. **(PMCR.N-1)**].
  - The operation of this bit ignores the values of **PMOVSR[(PMCR.N-1):HDCR.HPMN]**.
- This applies even when EL2 is disabled in the current Security state.

This bit does not affect the operation of **PMCCNTR**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**Bit [8]**

Reserved, **RES0**.

**LP, bit [7]**

**When FEAT_PMUv3p5 is implemented:**

Long event counter enable. Determines when unsigned overflow is recorded by a counter overflow bit.
LP, bit [0]

Meaning

0b0  Event counter overflow on increment that causes unsigned overflow of PMEVCNTR<n>[31:0].

0b1  Event counter overflow on increment that causes unsigned overflow of PMEVCNTR<n>[63:0].

If the highest implemented Exception level is using AArch32, it is IMPLEMENTATION DEFINED whether this bit is RW or RAZ/WI.

If EL2 is implemented and HDCR.HPMN or MDCR_EL2.HPMN is less than PMCR.N, this bit does not affect the operation of event counters in the range [HDCR.HPMN..(PMCR.N-1)] or [MDCR_EL2.HPMN..(PMCR.N-1)].

PMEVCNTR<n>[63:32] cannot be accessed directly in AArch32 state.

Note

The effect of HDCR.HPMN or MDCR_EL2.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state. For more information, see the description of HDCR.HPMN or MDCR_EL2.HPMN.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

LC, bit [6]

Long cycle counter enable. Determines when unsigned overflow is recorded by the cycle counter overflow bit.

<table>
<thead>
<tr>
<th>LC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR[63:0].</td>
</tr>
</tbody>
</table>

Arm deprecates use of PMCR.LC = 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DP, bit [5]

When EL3 is implemented or (FEAT_PMUv3p1 is implemented and EL2 is implemented):

Disable cycle counter when event counting is prohibited.

<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by PMCCNTR is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>When event counting for counters in the range [0..(HDCR.HPMN-1)] or [0..(MDCR_EL2.HPMN-1)] is prohibited, cycle counting by PMCCNTR is disabled.</td>
</tr>
</tbody>
</table>

For more information see 'Prohibiting event counting'

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

X, bit [4]
When the implementation includes a PMU event export bus:

Enable export of events in an IMPLEMENTATION DEFINED PMU event export bus.

<table>
<thead>
<tr>
<th>X</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not export events.</td>
</tr>
<tr>
<td>0b1</td>
<td>Export events where not prohibited.</td>
</tr>
</tbody>
</table>

This field enables the exporting of events over an IMPLEMENTATION DEFINED PMU event export bus to another device, for example to an OPTIONAL PE trace unit.

No events are exported when counting is prohibited.

This field does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface (CTI) that can be implemented as signals exported from the PE.

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RAZ/WI.

D, bit [3]

Clock divider. The possible values of this bit are:

<table>
<thead>
<tr>
<th>D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When enabled, PMCCNTR counts every clock cycle.</td>
</tr>
<tr>
<td>0b1</td>
<td>When enabled, PMCCNTR counts once every 64 clock cycles.</td>
</tr>
</tbody>
</table>

If PMCR.LC == 1, this bit is ignored and the cycle counter counts every clock cycle.

Arm deprecates use of PMCR.D = 1.

On a Warm reset, this field resets to 0.

C, bit [2]

Cycle counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset PMCCNTR to zero.</td>
</tr>
</tbody>
</table>

Note

Resetting PMCCNTR does not change the cycle counter overflow bit.

The value of PMCR_EL0.LC is ignored, and bits [63:0] of all affected event counters are reset.

Access to this field is WO/RAZ.

P, bit [1]

Event counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset all event counters accessible in the current Exception level, not including PMCCNTR, to zero.</td>
</tr>
</tbody>
</table>

In EL0 and EL1:
If EL2 is implemented and enabled in the current Security state, and HDCR.HPMN or MDCR_EL2.HPMN is less than PMCR_EL0.N, a write of 1 to this bit does not reset event counters in the range [HDCR.HPMN..(PMN-1)] or [MDCR_EL2.HPMN..(PMN-1)].

If EL2 is not implemented, EL2 is disabled in the current Security state, or HDCR.HPMN or MDCR_EL2.HPMN is equal to PMCR_EL0.N, a write of 1 to this bit resets all the event counters.

In EL2 and EL3, a write of 1 to this bit resets all the event counters.

**Note**

Resetting the event counters does not change the event counter overflow bits.

If FEAT_PMUv3p5 is implemented, the values of HDCR.HLP and PMCR.LP are ignored and bits [63:0] of all affected event counters are reset.

Access to this field is **WO/RAZ**.

**E, bit [0]**

Enable.

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All event counters in the range [0..(PMN-1)] and PMCCNTR. are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>All event counters in the range [0..(PMN-1)] and PMCCNTR. are enabled by PMCNTENSET.</td>
</tr>
</tbody>
</table>

If EL2 is implemented then:

- If EL2 is using AArch32, PMN is HDCR.HPMN.
- If EL2 is using AArch64, PMN is MDCR_EL2.HPMN.
- If PMN is less than PMCR.N, this bit does not affect the operation of event counters in the range [PMN..(PMN-1)].

If EL2 is not implemented, PMN is PMCR.N.

**Note**

The effect of MDCR_EL2.HPMN or HDCR.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, regardless of whether EL2 is enabled in the current Security state. For more information, see the description of MDCR_EL2.HPMN or HDCR.HPMN.

On a Warm reset, this field resets to 0.

**Accessing the PMCR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>}{<coproc>}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSR.T9 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPMCR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPMCR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if;
else
  return PMCR;
end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSR.T9 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPMCR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPMCR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if;
else
  return PMCR;
end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL3) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSR.T9 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPMCR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPMCR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if;
else
  return PMCR;
end if;
elsif PSTATE.EL == EL3 then
    return PMCR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
  else
    UNDEFINED;
  end if
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPMCR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if
else
  PMCR = R[t];
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    UNDEFINED;
  end if
elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSR.T9 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPMCR == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPMCR == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  end if
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x03);
end if
else
  PMCR = R[t];
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    end if
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x03);
end if
AArch64.AArch32SystemAccessTrap(EL3, 0x03);

else
   PMCR = R[t];
elsif PSTATE.EL == EL3 then
   PMCR = R[t];
PMEVCNTR\(<n>\), Performance Monitors Event Count Registers, \(n = 0 - 30\)

The PMEVCNTR\(<n>\) characteristics are:

**Purpose**

Holds event counter \(n\), which counts events, where \(n\) is 0 to 30.

**Configuration**

AArch32 System register PMEVCNTR\(<n>\) bits [31:0] are architecturally mapped to AArch64 System register PMEVCNTR\(<n>_EL0[31:0]\).

AArch32 System register PMEVCNTR\(<n>\) bits [31:0] are architecturally mapped to External register PMEVCNTR\(<n>_EL0[31:0]\).

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMEVCNTR\(<n>\) are **UNDEFINED**.

**Attributes**

PMEVCNTR\(<n>\) is a 32-bit register.

**Field descriptions**

The PMEVCNTR\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>

**Bits [31:0]**

Event counter \(n\). Value of event counter \(n\), where \(n\) is the number of this register and is a number from 0 to 30.

If FEAT_PMUv3p5 is implemented, the event counter is 64 bits and only the least-significant part of the event counter is accessible in AArch32 state:

- Reads from PMEVCNTR\(<n>\) return bits [31:0] of the counter.
- Writes to PMEVCNTR\(<n>\) update bits [31:0] and leave bits [63:32] unchanged.
- There is no means to access bits [63:32] directly from AArch32 state.
- If the implementation does not support AArch64 at any Exception level, bits [63:32] are not required to be implemented.

If FEAT_PMUv3p5 is not implemented, the event counter is 32 bits.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMEVCNTR\(<n>\)**

PMEVCNTR\(<n>\) can also be accessed by using PMXEV CNTR with PMSEL.R.SEL set to the value of \(<n>\).

If FEAT_FGT is implemented and \(<n>\) is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMEVCNTR\(<n>\) is as follows:

- If \(<n>\) is an unimplemented event counter, the access is **UNDEFINED**.
• Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and \(<n>\) is greater than or equal to the number of accessible counters, then reads and writes of \(\text{PMEVCNTR}<n>\) are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

If \(<n>\) is greater than or equal to the number of accessible event counters, then reads and writes of \(\text{PMEVCNTR}<n>\) are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

• Accesses to the register are UNDEFINED.
• Accesses to the register behave as RAZ/WI.
• Accesses to the register execute as a NOP
• If EL2 is implemented and enabled in the current Security state, and \(<n>\) is less than the number of implemented counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

---

**Note**

In EL0, an access is permitted if it is enabled by \(\text{PMUSERENR}, \{\text{ER,EN}\}\) or \(\text{PMUSERENR_EL0}, \{\text{ER,EN}\}\).

If EL2 is implemented and enabled in the current Security state, at EL0 and EL1:

• If EL2 is using AArch32, \(\text{HDCR}, \text{HPMN}\) identifies the number of accessible event counters.
• If EL2 is using AArch64, \(\text{MDCR_EL2}, \text{HPMN}\) identifies the number of accessible event counters.

Otherwise, the number of accessible event counters is the number of implemented counters. See \(\text{HDCR}, \text{HPMN}\) and \(\text{MDCR_EL2}, \text{HPMN}\) for more details.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b10:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) & PMUSERENR EL0.<ER,EN> == '00' then
        if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if
    else
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    end if
    elsif !ELUsingAArch32(EL1) & HCR_EL2.<E2H,TGE> != '11' & (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') & HDFGRTR_EL2.PMEVCNTRn_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL1) & MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        return PMEVCNTR[UInt(CRm<1:0>:opc2<2:0>)];
    end if
elsif PSTATE.EL == EL1 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        return PMEVCNTR[UInt(CRm<1:0>:opc2<2:0>)];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'' & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        return PMEVCNTR[UInt(CRm<1:0>:opc2<2:0>)];
    end if
elsif PSTATE.EL == EL3 then
    return PMEVCNTR[UInt(CRm<1:0>:opc2<2:0>)];
else
    return PMEVCNTR[UInt(CRm<1:0>:opc2<2:0>)];
end if

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b10:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if
    elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && HDFGWTR_EL2.PMEVCNTRn_EL0 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end if
  elsif EL2Enabled() && HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if
    elsif PSTATE.EL == EL2 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
      elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if
    end if
  elsif PSTATE.EL == EL3 then
    PMEVCNTR[UInt(Crm<1:0>:opc2<2:0>)] = R[t];
  end if
else
  PMEVCNTR[UInt(Crm<1:0>:opc2<2:0>)] = R[t];
end if
The PMEVTPYPER<n> characteristics are:

**Purpose**

Configures event counter n, where n is 0 to 30.

**Configuration**

AArch32 System register PMEVTPYPER<n> bits [31:0] are architecturally mapped to AArch64 System register PMEVTPYPER<n>_EL0[31:0].

AArch32 System register PMEVTPYPER<n> bits [31:0] are architecturally mapped to External register PMEVTPYPER<n>_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMEVTPYPER<n> are UNDEFINED.

**Attributes**

PMEVTYPER<n> is a 32-bit register.

**Field descriptions**

The PMEVTPYPER<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| P  | U  | NSK | NSU | NSH | RES0 | RES0 | evtCount[15:10] | evtCount[9:0] |

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMEVTPYPER<n>.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events in EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count events in EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMEVTPYPER<n>.NSU bit.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events in EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count events in EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**NSK, bit [29]**

*When EL3 is implemented:*

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of PMEVTYPER<n>.P, events in Non-secure EL1 are counted.

Otherwise, events in Non-secure EL1 are not counted.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**NSU, bit [28]**

*When EL3 is implemented:*

Non-secure EL0 (Unprivileged) filtering. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of PMEVTYPER<n>.U, events in Non-secure EL0 are counted.

Otherwise, events in Non-secure EL0 are not counted.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**NSH, bit [27]**

*When EL2 is implemented:*

EL2 (Hyp mode) filtering bit. Controls counting in EL2.

<table>
<thead>
<tr>
<th>NSH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not count events in EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count events in EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**Bit [26]**

Reserved, RES0.

**MT, bit [25]**

*When FEAT_MTPMU is implemented or an IMPLEMENTATION DEFINED multi-threaded PMU extension is implemented:*

Multithreading.

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events only on controlling PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count events from any PE with the same affinity at level 1 and above as this PE.</td>
</tr>
</tbody>
</table>
From Armv8.6, the *IMPLEMENTATION DEFINED* multi-threaded PMU extension is not permitted, meaning if FEAT_MTPMU is not implemented, this bit is RES0. See ID_DFR1_MTPMU.

This bit is ignored by the PE and treated as zero when FEAT_MTPMU is implemented and Disabled.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**Bits [24:16]**

Reserved, RES0.

**evtCount[15:10], bits [15:10]**

When FEAT_PMUv3p1 is implemented:

Extension to(evtCount[9:0]. See evtCount[9:0] for more details.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**evtCount[9:0], bits [9:0]**

Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>. Software must program this field with an event that is supported by the PE being programmed.

The ranges of event numbers allocated to each type of event are shown in 'Allocation of the PMU event number space'.

If evtCount is programmed to an event that is reserved or not supported by the PE, the behavior depends on the value written:

- For the range 0x0000 to 0x003F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- If 16-bit evtCount is implemented, for the range 0x4000 to 0x403F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- For IMPLEMENTATION DEFINED events, it is **UNPREDICTABLE** what event, if any, is counted, and the value returned by a direct or external read of the evtCount field is **UNKNOWN**.

**Note**

**UNPREDICTABLE** means the event must not expose privileged information.

Arm recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMEVTYPER<n>**

PMEVTYPER<n> can also be accessed by using PMXEVTPYPER with PMSELR SEL set to n.

If FEAT_FGT is implemented and <n> is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMEVTYPER<n> is as follows:

- If <n> is an unimplemented event counter, the access is **UNDEFINED**.
• Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and \(<n>\) is greater than or equal to the number of accessible counters, then reads and writes of \(\text{PMEVTYPER}<n>\) are constrained unpredictable, and the following behaviors are permitted:

If \(<n>\) is greater or equal to the number of accessible event counters, then reads and writes of \(\text{PMEVTYPER}<n>\) are constrained unpredictable, and the following behaviors are permitted:

- Accesses to the register are undefined.
- Accesses to the register behave as RAZ/WI.
- Accesses to the register execute as a NOP.
- If EL2 is implemented and enabled in the current Security state, and \(<n>\) is less than the number of implemented counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

Note

In EL0, an access is permitted if it is enabled by \(\text{PMUSERENR}.\text{EN}\) or \(\text{PMUSERENR_EL0}.\text{EN}\).

If EL2 is implemented and enabled in the current Security state, at EL0 and EL1:

- If EL2 is using AArch32, \(\text{HDCR}.\text{HPMN}\) identifies the number of accessible event counters.
- If EL2 is using AArch64, \(\text{MDCR_EL2}.\text{HPMN}\) identifies the number of accessible event counters.

Otherwise, the number of accessible event counters is the number of implemented counters. See \(\text{HDCR}.\text{HPMN}\) and \(\text{MDCR_EL2}.\text{HPMN}\) for more details.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} \text{ coproc}, \{\#\text{opc1}\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{\#\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1110</td>
<td>0b11:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>

\(\text{PMEVTYPER}<n>\), Performance Monitors Event Type Registers, \(n = 0 - 30\)
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return PMEVTYPER[UInt(CRm<1:0>:opc2<2:0>)];
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return PMEVTYPER[UInt(CRm<1:0>:opc2<2:0>)];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EMERG(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return PMEVTYPER[UInt(CRm<1:0>:opc2<2:0>)];
  end
elsif PSTATE.EL == EL3 then
  return PMEVTYPER[UInt(CRm<1:0>:opc2<2:0>)];
end

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b1110</td>
<td>0b11:n[4:3]</td>
<td>n[2:0]</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() & haveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) & PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() & ELUsingAArch32(EL1) & PMUSERENR.EN == '0' then
    if Halted() & !ELUsingAArch32(EL1) & SCR_EL1.FGTE == '1' & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
      AArch32.TakeHypTrapException(0x03);
    else
      UNDEFINED;
    end if;
  elsif EL2Enabled() & !ELUsingAArch32(EL1) & SCR_EL1.FGTE == '1' & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    PSTATE.EL == EL1 then
      if Halted() & haveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        UNDEFINED;
      elseif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
      elseif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
      elseif haveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end if;
    elseif PSTATE.EL == EL2 then
      if Halted() & haveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        UNDEFINED;
      elseif haveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
        if Halted() & EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
      else
        PSTATE.EL == EL3 then
          PMEVENTYPER[UInt(Cr<1:0>:opc2<2:0>)] = R[t];
        elseif PSTATE.EL == EL3 then
          PMEVENTYPER[UInt(Cr<1:0>:opc2<2:0>)] = R[t];
        else
          PMEVENTYPER[UInt(Cr<1:0>:opc2<2:0>)] = R[t];
        end if;
    else
      PMEVENTYPER[UInt(Cr<1:0>:opc2<2:0>)] = R[t];
    end if;
  end if;
end if;
PMINTENCLR, Performance Monitors Interrupt Enable Clear register

The PMINTENCLR characteristics are:

**Purpose**

Disables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR, and the event counters PMEVCNTR<n>. Reading the register shows which overflow interrupt requests are enabled.

PMINTENCLR is used in conjunction with the PMINTENSET register.

**Configuration**

AArch32 System register PMINTENCLR bits [31:0] are architecturally mapped to AArch64 System register PMINTENCLR_EL1[31:0].

AArch32 System register PMINTENCLR bits [31:0] are architecturally mapped to External register PMINTENCLR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMINTENCLR are UNDEFINED.

**Attributes**

PMINTENCLR is a 32-bit register.

**Field descriptions**

The PMINTENCLR bit assignments are:

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

<table>
<thead>
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</tr>
</thead>
<tbody>
<tr>
<td>C, bit [31]</td>
<td>PMCCNTR overflow interrupt request disable bit.</td>
<td></td>
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<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

P<n>, bit [n], for n = 30 to 0

Event counter overflow interrupt request disable bit for PMEVCNTR<n>.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1, N is the value in MDCR_EL2.HPMN if EL2 is using AArch64, or in HDCR.HPMN if EL2 is using AArch32. Otherwise, N is the value in PMCR.N.
PMINTENCLR, Performance Monitors Interrupt Enable Clear register

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the <code>PMEVCNTR&lt;n&gt;</code> event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the <code>PMEVCNTR&lt;n&gt;</code> event counter interrupt request is enabled. When written, disables the <code>PMEVCNTR&lt;n&gt;</code> interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the PMINTENCLR

Accesses to this register use the following encodings:

```markdown
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
```

```c
if PSTATE.EL == EL0 then  
    UNDEFINED;
elsif PSTATE.EL == EL1 then  
    if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then  
        UNDEFINED;
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T9 == '1' then  
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T9 == '1' then  
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then  
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then  
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then  
        if Halted() & EDSCR.SDD == '1' then  
            UNDEFINED;
        else  
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
    elsif PSTATE.EL == EL2 then  
        if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then  
            UNDEFINED;
        elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then  
            if Halted() & EDSCR.SDD == '1' then  
                UNDEFINED;
            else  
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            end if;
        end if;
    elsif PSTATE.EL == EL3 then  
        return PMINTENCLR;
    end if;
elsif PSTATE.EL == EL3 then  
    return PMINTENCLR;
else  
    return PMINTENCLR;
end if;
```

```markdown
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        PMINTENCLR = R[t];
    end if
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        PMINTENCLR = R[t];
    end if
elsif PSTATE.EL == EL3 then
    PMINTENCLR = R[t];
end if
PMINTENSET, Performance Monitors Interrupt Enable Set register

The PMINTENSET characteristics are:

Purpose

Enables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR, and the event counters PMEVCNTR<n>. Reading the register shows which overflow interrupt requests are enabled.

PMINTENSET is used in conjunction with the PMINTENCLR register.

Configuration

AArch32 System register PMINTENSET bits [31:0] are architecturally mapped to AArch64 System register PMINTENSET_EL1[31:0].

AArch32 System register PMINTENSET bits [31:0] are architecturally mapped to External register PMINTENSET_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMINTENSET are UNDEFINED.

Attributes

PMINTENSET is a 32-bit register.

Field descriptions

The PMINTENSET bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

C, bit [31]

PMCCNTR overflow interrupt request enable bit.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>1</td>
<td>When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

P<n>, bit [n], for n = 30 to 0

Event counter overflow interrupt request enable bit for PMEVCNTR<n>.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1, N is the value in MDCR_EL2.HPMN if EL2 is using AArch64, or in HDCR.HPMN if EL2 is using AArch32. Otherwise, N is the value in PMCR.N.
### PMINTENSET, Performance Monitors Interrupt Enable Set register

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the PMEVCNTR&lt;n&gt; event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the PMEVCNTR&lt;n&gt; event counter interrupt request is enabled. When written, enables the PMEVCNTR&lt;n&gt; interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

## Accessing the PMINTENSET

Accesses to this register use the following encodings:

- **MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}**

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
elsif EL2Enabled() && ELUsingAArch32(EL2) && EDSCR.SDD == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && EVSC_EL2.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() && HSTR_EL2.T9 == '1' then
    AArch32.AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif HaveEL(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
elsif HaveEL(EL3) && EDSCR.SDD == '1' then
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
elsif PSTATE.EL == EL3 then
  return PMINTENSET;
else
  AArch64.AArch32SystemAccessTrap(EL3, 0x03);
else
  return PMINTENSET;
else
  return PMINTENSET;
else
  return PMINTENSET;
```

### Table

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b001</td>
</tr>
</tbody>
</table>

Page 2927
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
      PMINTENSET = R[t];
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      else
        PMINTENSET = R[t];
    elsif PSTATE.EL == EL3 then
      PMINTENSET = R[t];
PMMIR, Performance Monitors Machine Identification Register

The PMMIR characteristics are:

**Purpose**

Describes Performance Monitors parameters specific to the implementation to software.

**Configuration**

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3p4 is implemented. Otherwise, direct accesses to PMMIR are UNDEFINED.

**Attributes**

PMMIR is a 32-bit register.

**Field descriptions**

The PMMIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>BUS_WIDTH</th>
<th>BUS_SLOTS</th>
<th>SLOTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
</tr>
<tr>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
</tr>
<tr>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [31:20]**

Reserved, RES0.

**BUS_WIDTH, bits [19:16]**

*From Armv8.7:*

Bus width. Indicates the number of bytes each BUS_ACCESS event relates to. Encoded as Log2(number of bytes), plus one. Defined values are:

<table>
<thead>
<tr>
<th>BUS_WIDTH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>The information is not available.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Four bytes.</td>
</tr>
<tr>
<td>0b0100</td>
<td>8 bytes.</td>
</tr>
<tr>
<td>0b0101</td>
<td>16 bytes.</td>
</tr>
<tr>
<td>0b0110</td>
<td>32 bytes.</td>
</tr>
<tr>
<td>0b0111</td>
<td>64 bytes.</td>
</tr>
<tr>
<td>0b1000</td>
<td>128 bytes.</td>
</tr>
<tr>
<td>0b1001</td>
<td>256 bytes.</td>
</tr>
<tr>
<td>0b1010</td>
<td>512 bytes.</td>
</tr>
<tr>
<td>0b1011</td>
<td>1024 bytes.</td>
</tr>
<tr>
<td>0b1100</td>
<td>2048 bytes.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Each transfer is up to this number of bytes. An access might be smaller than the bus width.

When this field is nonzero, each access counted by BUS_ACCESS is at most BUS_WIDTH bytes. An implementation might treat a wide bus as multiple narrower buses, such that a wide access on the bus increments the BUS_ACCESS counter by more than one.
Otherwise:
Reserved, RAZ.

**BUS_SLOTS, bits [15:8]**

*From Armv8.7:*

Bus count. The largest value by which the BUS_ACCESS event might increment by in a single BUS_CYCLES cycle. If the information is not available, this field will read as zero.

Otherwise:
Reserved, RAZ.

**SLOTS, bits [7:0]**

Operation width. The largest value by which the STALL_SLOT event might increment by in a single cycle. If the STALL_SLOT event is not implemented, this field might read as zero.

**Accessing the PMMIR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    else
        return PMMIR;
    end
elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end
    else
        return PMMIR;
    end
elsif PSTATE.EL == EL3 then
    return PMMIR;

The PMOVSR characteristics are:

**Purpose**

Contains the state of the overflow bit for the Cycle Count Register, PMCCNTR, and each of the implemented event counters PMEVCNTR<n>. Writing to this register clears these bits.

**Configuration**

AArch32 System register PMOVSR bits [31:0] are architecturally mapped to AArch64 System register PMOVSCLR_EL0[31:0].

AArch32 System register PMOVSR bits [31:0] are architecturally mapped to External register PMOVSCLR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMVv3 is implemented. Otherwise, direct accesses to PMOVSR are UNDEFINED.

**Attributes**

PMOVSR is a 32-bit register.

**Field descriptions**

The PMOVSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>C</td>
</tr>
<tr>
<td>00</td>
<td>When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>01</td>
<td>When read, means the cycle counter has overflowed since this bit was last cleared. When written, clears the cycle counter overflow bit to 0.</td>
</tr>
</tbody>
</table>

PMCR.LC controls whether an overflow is detected from unsigned overflow of PMCCNTR[31:0] or unsigned overflow of PMCCNTR[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow clear bit for PMEVCNTR<n>.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN if EL2 is using AArch64, or in HDCR.HPMN if EL2 is using AArch32. Otherwise, N is the value in PMCR.N.
<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt; has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt; has overflowed since this bit was last cleared. When written, clears the PMEVCNTR&lt;n&gt; overflow bit to 0.</td>
</tr>
</tbody>
</table>

If FEAT_PMUv3p5 is implemented, MDCR_EL2.HLP, HDCR.HLP, and PMCR.LP control whether an overflow is detected from unsigned overflow of PMEVCNTR<n>[31:0] or unsigned overflow of PMEVCNTR<n>[63:0]. PMEVCNTR<n>[63:32] cannot be accessed directly in AArch32 state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMOVSR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return PMOVSR;
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return PMOVSR;
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    return PMOVSR;
  end if;
elsif PSTATE.EL == EL3 then
  return PMOVSR;
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    UNDEFINED;
  elsif Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    PMOVSR = R[t];
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR_EL2.TGE != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      PMOVSR = R[t];
    end if;
  else
    PMOVSR = R[t];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
    UNDEFINED;
  elsif Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    PMOVSR = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  PMOVSR = R[t];
else
  PMOVSR = R[t];
end if;
endif;

PMOVSR, Performance Monitors Overflow Flag Status Register

Page 2936
PMOVSSET, Performance Monitors Overflow Flag Status Set register

The PMOVSSET characteristics are:

**Purpose**

Sets the state of the overflow bit for the Cycle Count Register, **PMCCNTR**, and each of the implemented event counters **PMEVCNTR<n>**.

**Configuration**

AArch32 System register PMOVSSET bits [31:0] are architecturally mapped to AArch64 System register **PMOVSSET_EL0[31:0]**.

AArch32 System register PMOVSSET bits [31:0] are architecturally mapped to External register **PMOVSSET_EL0[31:0]**.

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMOVSSET are **UNDEFINED**.

**Attributes**

PMOVSSET is a 32-bit register.

**Field descriptions**

The PMOVSSET bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**C, bit [31]**

Cycle counter overflow set bit.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter has overflowed since this bit was last cleared. When written, sets the cycle counter overflow bit to 1.</td>
</tr>
</tbody>
</table>

**PMCR.LC** controls whether an overflow is detected from unsigned overflow of **PMCCNTR[31:0]** or unsigned overflow of **PMCCNTR[63:0]**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow set bit for **PMEVCNTR<n>**.

If N is less than 31, then bits [30:N] are RAZ/WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in **MDCR_EL2.HPMN** if EL2 is using AArch64, or in **HDCR.HPMN** if EL2 is using AArch32. Otherwise, N is the value in **PMCR.N**.
<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt; has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt; has overflowed since this bit was last cleared. When written, sets the PMEVCNTR&lt;n&gt; overflow bit to 1.</td>
</tr>
</tbody>
</table>

If FEAT_PMUv3p5 is implemented, MDCR_EL2_HLP, HDCR_HLP, and PMCR_LP control whether an overflow is detected from unsigned overflow of PMEVCNTR<n>[31:0] or unsigned overflow of PMEVCNTR<n>[63:0]. PMEVCNTR<n>[63:32] cannot be accessed directly in AArch32 state.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMOVSSET**

Accesses to this register use the following encodings:

\[
\text{MRC}\{\langle c\rangle}\{\langle q\rangle\} \langle\text{coproc}\rangle, \#\langle\text{opc1}\rangle, \langle R_t\rangle, \langle CR_n\rangle, \langle CR_m\rangle, \#\langle\text{opc2}\rangle
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        return PMOVSSET;
    end if
else if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        return PMOVSSET;
    end if
else if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && HaveEL(EL3) && EL3TrapPriority == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if
    else
        return PMOVSSET;
    end if
else if PSTATE.EL == EL3 then
    return PMOVSSET;
end if

PMOVSSET, Performance Monitors Overflow Flag Status Set register
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
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<tr>
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<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  elsif EL2Enabled() && PMUSERENR.EN == '0' then
    if EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end if;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    PMOVSSET = R[t];
  end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    PMOVSSET = R[t];
  end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
  else
    PMOVSSET = R[t];
  end if;
elsif PSTATE.EL == EL3 then
  PMOVSSET = R[t];
PMSELR, Performance Monitors Event Counter Selection Register

The PMSELR characteristics are:

**Purpose**

Selects the current event counter PMEVCNTR<n> or the cycle counter, CCNT.

PMSELR is used in conjunction with PMXEVTYPER to determine the event that increments a selected event counter, and the modes and states in which the selected counter increments.

It is also used in conjunction with PMXEVCNTR, to determine the value of a selected event counter.

**Configuration**

AArch32 System register PMSELR bits [31:0] are architecturally mapped to AArch64 System register PMSELR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMSELR are UNDEFINED.

**Attributes**

PMSELR is a 32-bit register.

**Field descriptions**

The PMSELR bit assignments are:

<table>
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<tr>
<th>31</th>
<th>30</th>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:5]**

Reserved, RES0.

**SEL, bits [4:0]**

Selects event counter PMEVCNTR<n>, where n is the value held in this field. This value identifies which event counter is accessed when a subsequent access to PMXEVTYPER or PMXEVCNTR occurs.

This field can take any value from 0 (0b00000) to (PMCR.N)-1, or 31 (0b11111).

When PMSELR.SEL is 0b11111, it selects the cycle counter and:

- A read of the PMXEVTYPER returns the value of PMCCFILTR.
- A write of the PMXEVTYPER writes to PMCCFILTR.
- A read or write of PMXEVCNTR has CONSTRAINED UNPREDICTABLE effects. See PMXEVCNTR for more details.

For details of the results of accesses to event counters, see PMXEVTYPER and PMXEVCNTR.

For information about the number of counters accessible at each Exception level, see HDCR.HPMN and MDCR_EL2.HPMN.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMSELR

Accesses to this register use the following encodings:

\[
\text{MRC}\{\langle c\rangle}\{\langle q\rangle\} \langle \text{coproc} \rangle, \{\#\langle \text{opc1} \rangle\}, \langle \text{Rt} \rangle, \langle \text{CRn} \rangle, \langle \text{CRm} \rangle, \{\#\langle \text{opc2} \rangle\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() &HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) & & PMUSERN.R EL0.<ER,EN> == '00' then
        if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end if;
    end if;
elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.<E2H,TGE> != '11' & & HSTR_EL2.<T9> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif !ELUsingAArch32(EL1) & & PMUSERN.<ER,EN> == '00' then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    end if;
elsif ELUsingAArch32(EL1) & & PMUSERN.<ER,EN> == '00' then
    if EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    end if;
elsif EL2Enabled() & & HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif ELUsingAArch32(EL2) & & HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif ELUsingAArch32(EL2) & & HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x00);
else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
end if;
elsif PSTATE.EL == EL1 then
    if Halted() & & HaveEL(EL3) & & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    end if;
elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR_EL2.TGE == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & & ELUsingAArch32(EL2) & & MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif EL2Enabled() & & !ELUsingAArch32(EL1) & & HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & & StoreTrapException(0x03);
elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() & & !ELUsingAArch32(EL2) & & HCR.TGE == '1' then
    AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) & & !ELUsingAArch32(EL3) & & MDCR_EL3.TPM == '1' then
    if Halted() & & EDSCR.SDD == '1' then
        UNDEFINED;
    else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
elseif PSTATE.EL == EL2 then
    if Halted() & & HaveEL(EL3) & & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & & MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif HaveEL(EL3) & & !ELUsingAArch32(EL3) & & MDCR_EL3.TPM == '1' then
        if Halted() & & EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        end if;
else
    return PMSELR;
else
    PSTATE.EL == EL3 then
        return PMSELR;
    end if;
MCR<cq> coproc, {#<opc1>, <Rt>, <CRn>, <CRm>}, {#<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.<ER,EN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end if;
  else
    UNDEFINED;
  end if;
elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
  AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
  AArch32.TakeHypTrapException(0x03);
elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
  if Halted() && EDSCR.SDD == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end if;
else
  PMSELR = R[t];
end if;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
else
  PMSELR = R[t];
end if;
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if;
else
  PMSELR = R[t];
end if;
elsif PSTATE.EL == EL3 then
  PMSELR = R[t];
else
  PMSELR = R[t];
end if;
PMSWINC, Performance Monitors Software Increment register

The PMSWINC characteristics are:

**Purpose**

Increments a counter that is configured to count the Software increment event, event 0x00. For more information, see SW_INCR.

**Configuration**

AArch32 System register PMSWINC bits [31:0] are architecturally mapped to AArch64 System register PMSWINC_EL0[31:0].

AArch32 System register PMSWINC bits [31:0] are architecturally mapped to External register PMSWINC_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMSWINC are UNDEFINED.

**Attributes**

PMSWINC is a 32-bit register.

**Field descriptions**

The PMSWINC bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>30-0</td>
<td>Event counter software increment bit for PMEVCNTR&lt;n&gt;. If N is less than 31, then bits [30:N] are WI. When EL2 is implemented and enabled in the current Security state, in EL1 and EL0, N is the value in MDCR_EL2.HPMN if EL2 is using AArch64, or in HDCR.HPMN if EL2 is using AArch32. Otherwise, N is the value in PMCR.N.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action. The write to this bit is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>If PMEVCNTR&lt;n&gt; is enabled and configured to count the software increment event, increments PMEVCNTR&lt;n&gt; by 1. If PMEVCNTR&lt;n&gt; is disabled, or not configured to count the software increment event, the write to this bit is ignored.</td>
</tr>
</tbody>
</table>

**Accessing the PMSWINC**

Accesses to this register use the following encodings:
MCR\{<c>\}{<q>\} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1100</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.<SW,EN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif EL2Enabled() && PMUSERENR.<SW,EN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.E2H.TGE != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    PMSWINC = R[t];
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    PMSWINC = R[t];
  end
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    PMSWINC = R[t];
  end
elsif PSTATE.EL == EL3 then
  PMSWINC = R[t];
PMUSERENR, Performance Monitors User Enable Register

The PMUSERENR characteristics are:

**Purpose**

Enables or disables User mode access to the Performance Monitors.

**Configuration**

AArch32 System register PMUSERENR bits [31:0] are architecturally mapped to AArch64 System register PMUSERENR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMUSERENR are UNDEFINED.

**Attributes**

PMUSERENR is a 32-bit register.

**Field descriptions**

The PMUSERENR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td>RES0 ER CR SW EN</td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, RES0.

**ER, bit [3]**

Event counter read trap control:

<table>
<thead>
<tr>
<th>ER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 reads of the PMXEVCNTR and PMEVCNTR&lt;n&gt;, and EL0 RW access to the PMSELR, are trapped to Undefined mode if PMUSERENR.EN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overrides PMUSERENR.EN and enables RO access to PMXEVCNTR and PMEVCNTR&lt;n&gt;, and RW access to PMSELR.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**CR, bit [2]**

Cycle counter read trap control:

<table>
<thead>
<tr>
<th>CR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 reads of the PMCCNTR are trapped to Undefined mode if PMUSERENR.EN is also 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Overrides PMUSERENR.EN and enables access to PMCCNTR.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.
**SW, bit [1]**

Software increment write trap control:

<table>
<thead>
<tr>
<th>SW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>EL0 writes to the PMSWINC are trapped to Undefined mode if PMUSERENR.EN is also 0.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>Overrides PMUSERENR.EN and enables access to PMSWINC.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**EN, bit [0]**

Traps EL0 accesses to the Performance Monitors registers to Undefined mode, as follows:

- PMCR, PMOVSR, PMSLR, PMCEID0, PMCEID1, PMCCNTR, PMXEVTYPER, PMXEVCTR, PMCENSET, PMCCNTRCLR, PMOVSSET, PMEVCTR<n>, PMEVTYPE<n>, PMCCFILT, PMSWINC.
- If FEAT_PMUv3p1 is implemented, PMCEID2, and PMCEID3.
- If FEAT_PMUv3p4 is implemented, PMMIR.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>While at EL0, accesses to the specified registers at EL0 are trapped to Undefined mode, unless overridden by one of PMUSERENR.{ER, CR, SW}.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>While at EL0, software can access all of the specified registers.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the PMUSERENR**

Accesses to this register use the following encodings:

\(\text{MRC\{<c>\}{<q>}} \text{<coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}}\)

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1001</td>
<td>0b1110</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMUSERENR_EL0 == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            return PMUSERENR;
    elsif PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
            AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                return PMUSERENR;
        elsif PSTATE.EL == EL2 then
            if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
                UNDEFINED;
            elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
                if Halted() && EDSCR.SDD == '1' then
                    UNDEFINED;
                else
                    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
           elsif PSTATE.EL == EL3 then
                return PMUSERENR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

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if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    PMUSERENR = R[t];
  end if
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end if
  else
    PMUSERENR = R[t];
  end if
elsif PSTATE.EL == EL3 then
  PMUSERENR = R[t];
PMXEVCNTR, Performance Monitors Selected Event Count Register

The PMXEVCNTR characteristics are:

**Purpose**

Reads or writes the value of the selected event counter, PMEVCNTR<n>. PMSELR.SEL determines which event counter is selected.

**Configuration**

AArch32 System register PMXEVCNTR bits [31:0] are architecturally mapped to AArch64 System register PMXEVCNTR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMXEVCNTR are UNDEFINED.

**Attributes**

PMXEVCNTR is a 32-bit register.

**Field descriptions**

The PMXEVCNTR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

PMEVCNTR<n>, bits [31:0]

Value of the selected event counter, PMEVCNTR<n>, where n is the value stored in PMSELR.SEL.

If FEAT_PMUv3p5 is implemented, the event counter is 64 bits and only the least-significant part of the event counter is accessible in AArch32 state:

- Reads from PMXEVCNTR return bits [31:0] of the counter.
- There is no means to access bits [63:32] directly from AArch32 state.
- If the implementation does not support AArch64 at any Exception level, bits [63:32] are not required to be implemented.

If FEAT_PMUv3p5 is not implemented, the event counter is 32 bits.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMXEVCNTR**

If FEAT_FGT is implemented and PMSELR SEL is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMXEVCNTR is as follows:

- If PMSELR.SEL selects an unimplemented event counter, the access is UNDEFINED.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented and PMSELR.SEL is greater than or equal to the number of accessible counters, then reads and writes of PMXEVCNTR are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:
Accesses to the register are UNDEFINED.
Accesses to the register behave as RAZ/WI.
Accesses to the register execute as a NOP.
Accesses to the register behave as if PMSELR_SEL has an UNKNOWN value less than the number of event counters accessible at the current Exception level and Security state.
If EL2 is implemented and enabled in the current Security state, and PMSELR_SEL is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.

**Note**

In EL0, an access is permitted if it is enabled by PMUSERENR:{ER,EN} or PMUSERENR_EL0:{ER,EN}.

If EL2 is implemented and enabled in the current Security state, at EL0 and EL1:

- If EL2 is using AArch32, HDCR.HPMN identifies the number of accessible event counters.
- If EL2 is using AArch64, MDCR_EL2.HPMN identifies the number of accessible event counters.

Otherwise, the number of accessible event counters is the number of implemented counters. See HDCR.HPMN and MDCR_EL2.HPMN for more details.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

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</table>
if PSTATE.EL == EL0 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.<ER,EN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end
  elsif ELUsingAArch32(EL1) && PMUSERENR.ER,EN> == '00' then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TGE == '1' then
      AArch32.TakeHypTrapException(0x00);
    else
      UNDEFINED;
    end
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.ER,EN> != '11' && HSTR_EL2.T9 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.ER,EN> == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.ER,EN> != '11' && (!HaveEL(EL3) || SCR_EL3.FGTEn == '1') && HDFGRTR_EL2.PMEVCNTRn_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    end
  else
    return PMXEVCNTR;
  end
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSR_EL2.ER,EN> == '1' then
    if EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.ER,EN> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.ER,EN> == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif HSTR_EL2.ER,EN> == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif HSTR_EL2.ER,EN> != '11' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end
    else
      return PMXEVCNTR;
    end
  elsif PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      UNDEFINED;
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
      end
    else
      return PMXEVCNTR;
    end
elsif PSTATE.EL == EL3 then
  return PMXEVCNTR;
PMXEVCTR, Performance Monitors Selected Event Count Register

MCR{<c>}{<q>}, {<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

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</tbody>
</table>
if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            PMXEVCNTR = R[t];
        endif
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        PMXEVCNTR = R[t];
    endif
else if PSTATE.EL == EL1 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.<E2H,TGE> != '11' && HSTR_EL2.T9 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T9 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TPM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        PMXEVCNTR = R[t];
    endif
else if PSTATE.EL == EL2 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        PMXEVCNTR = R[t];
    endif
else if PSTATE.EL == EL3 then
    PMXEVCNTR = R[t];
else
    PMXEVCNTR = R[t];
endif
PMXEVTPYPER, Performance Monitors Selected Event Type Register

The PMXEVTPYPER characteristics are:

**Purpose**

When PMSELR SEL selects an event counter, this accesses a PMEVTYPER<n> register. When PMSELR_SEL selects the cycle counter, this accesses PMCCFILTR.

**Configuration**

AArch32 System register PMXEVTPYPER bits [31:0] are architecturally mapped to AArch64 System register PMXEVTPYPER_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_PMUv3 is implemented. Otherwise, direct accesses to PMXEVTPYPER are UNDEFINED.

**Attributes**

PMXEVTPYPER is a 32-bit register.

**Field descriptions**

The PMXEVTPYPER bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Event type register or PMCCFILTR |

**Bits [31:0]**

Event type register or PMCCFILTR.

When PMSELR_SEL == 31, this register accesses PMCCFILTR.

Otherwise, this register accesses PMEVTYPER<n> where n is the value in PMSELR_SEL.

**Accessing the PMXEVTPYPER**

If FEAT_FGT is implemented, and PMSELR_SEL is not 31 and is greater than or equal to the number of accessible counters, then the behavior of permitted reads and writes of PMXEVTPYPER is as follows:

- If PMSELR_SEL selects an unimplemented event counter, the access is UNDEFINED.
- Otherwise, the access is trapped to EL2.

If FEAT_FGT is not implemented, and PMSELR_SEL is not 31 and is greater than or equal to the number of accessible counters, then reads and writes of PMXEVTPYPER are CONSTRAINED UNPREDICTABLE, and the following behaviors are permitted:

- Accesses to the register are UNDEFINED.
- Accesses to the register behave as RAZ/WI.
- Accesses to the register execute as a NOP
- Accesses to the register behave as if PMSELR_SEL has an UNKNOWN value less than the number of event counters accessible at the current Exception level and Security state.
- Accesses to the register behave as if PMSELR_SEL is 31.
- If EL2 is implemented and enabled in the current Security state, and PMSELR_SEL is less than the number of implemented event counters, accesses from EL1 or permitted accesses from EL0 are trapped to EL2.
Note

In EL0, an access is permitted if it is enabled by `PMUSERENR.EN` or `PMUSERENR_EL0.EN`.

If EL2 is implemented and enabled in the current Security state, at EL0 and EL1:

- If EL2 is using AArch32, `HDCR.HPMN` identifies the number of accessible event counters.
- If EL2 is using AArch64, `MDCR_EL2.HPMN` identifies the number of accessible event counters.

Otherwise, the number of accessible event counters is the number of implemented counters. See `HDCR.HPMN` and `MDCR_EL2.HPMN` for more details.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>\{, \{#\}<\text{opc2}>\}
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if PSTATE.EL == EL0 then
    if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
        UNDEFINED;
    elsif !ELUsingAArch32(EL1) && PMUSERENR_EL0.EN == '0' then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TGE == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        else
            AArch64.AArch32SystemAccessTrap(EL1, 0x03);
        end
    elsif EL2Enabled() && ELUsingAArch32(EL2) && SCR_EL3.FGTEn == '1' && HDFGFRTR_EL2.PMEVTYPERn_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TPM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
    else
        return PMXEVTYPER;
    endif
else
    if PSTATE.EL == EL1 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            if Halted() && EDSCR.SDD == '1' then
                UNDEFINED;
            else
                AArch64.AArch32SystemAccessTrap(EL3, 0x03);
            endif
        else
            return PMXEVTYPER;
        endif
    elsif PSTATE.EL == EL2 then
        if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TPM == '1' then
            UNDEFINED;
        elsif Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
        else
            AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        endif
    else
        return PMXEVTYPER;
    endif
else
    if PSTATE.EL == EL3 then
        return PMXEVTYPER;
    endif
end

PMXEVTYPER, Performance Monitors Selected Event Type Register
MCR{<c>{<q>} {coproc}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>{}}

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if PSTATE.EL == EL0 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif !ELUsingAArch32(EL1) & PMUSERREN_EL0.EN == '0' then
    if EL2Enabled() & !ELUsingAArch32(EL2) & HCR_EL2.TGE == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
      AArch64.AArch32SystemAccessTrap(EL1, 0x03);
    end;
  elsif EL2Enabled() & ELUsingAArch32(EL1) & HCR_EL2.<E2H,TGE> != '11' & SCRT_EL3.FGTEn == '1' & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  end;
else
  PMXEVTYPER = R[t];
elsif PSTATE.EL == EL1 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  end;
else
  PMXEVTYPER = R[t];
elsif PSTATE.EL == EL2 then
  if Halted() & HaveEL(EL3) & EDSCR.SDD == '1' & boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T9 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & !ELUsingAArch32(EL2) & MDCR_EL2.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HDCR.TPM == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() & ELUsingAArch32(EL2) & HDFGWTR_EL2.PMEVTYPERn_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  end;
else
  PMXEVTYPER = R[t];
elsif PSTATE.EL == EL3 then
  if Halted() & EDSCR.SDD == '1' then
    UNDEFINED;
  elseif PMXEVTYPER 
  PMXEVTYPER = R[t];
elsif PSTATE.EL == EL2 then
  if Halted() & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) & !ELUsingAArch32(EL3) & MDCR_EL3.TPM == '1' then
    UNDEFINED;
  else
    AArch64.AArch32SystemAccessTrap(EL3, 0x03);
  end;
else
  PMXEVTYPER = R[t];
elsif PSTATE.EL == EL3 then
  if Halted() & EDSCR.SDD == '1' then
    UNDEFINED;
  elseif PMXEVTYPER 
  PMXEVTYPER = R[t];
PRRR, Primary Region Remap Register

The PRRR characteristics are:

**Purpose**

Controls the top level mapping of the TEX[0], C, and B memory region attributes.

**Configuration**

AArch32 System register PRRR bits [31:0] are architecturally mapped to AArch64 System register `MAIR_EL1[31:0]` when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register PRRR bits [31:0] are architecturally mapped to AArch32 System register `MAIR0[31:0]` when EL3 is not implemented or EL3 is using AArch64.

AArch32 System register PRRR bits [31:0] (PRRR_S) are architecturally mapped to AArch32 System register `MAIR0[31:0]` (MAIR0_S) when EL3 is using AArch32.

AArch32 System register PRRR bits [31:0] (PRRR_NS) are architecturally mapped to AArch32 System register `MAIR0[31:0]` (MAIR0_NS) when EL3 is using AArch32.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to PRRR are UNDEFINED.

`MAIR0` and PRRR are the same register, with a different view depending on the value of `TTBCR.EAE`:

- When it is set to 0, the register is as described in PRRR.
- When it is set to 1, the register is as described in `MAIR0`.

**Attributes**

PRRR is a 32-bit register.

**Field descriptions**

The PRRR bit assignments are:

**When TTBCR.EAE == 0:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23222120 | 19 | 18 | 17 | 16 | 151413121110 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|-----------|----|----|----|----|----------------|---|---|---|---|---|---|---|---|---|---|---|
| NOS7 | NOS6 | NOS5 | NOS4 | NOS3 | NOS2 | NOS1 | NOS0 | RES0 | NS1 | NS0 | DS1 | DS0 | TR7 | TR6 | TR5 | TR4 | TR3 | TR2 | TR1 | TR0 |

**NOS<n>, bit [n+24], for n = 7 to 0**

Not Outer Shareable. NOS<n> is the Outer Shareable property for memory attributes n, if the region is mapped as Normal memory that is not Inner Non-cacheable, Outer Non-cacheable, and the appropriate PRRR.{NS0, NS1} field identifies the region as shareable. n is the value of the concatenation of the {TEX[0], C, B} bits from the translation table descriptor. The possible values of each NOS<n> field other than NOS6 are:

<table>
<thead>
<tr>
<th>NOS&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Memory region is Outer Shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory region is Inner Shareable.</td>
</tr>
</tbody>
</table>

The value of this bit is ignored if the region is:

- Device memory
- Normal memory that is at least one of:
  - Inner Non-cacheable, Outer Non-cacheable.
  - Identified by the appropriate PRRR.{NS0, NS1} field as Non-shareable.
The meaning of the NOS6 field is **IMPLEMENTATION DEFINED**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [23:20]**

Reserved, RES0.

**NS1, bit [19]**

Mapping of S = 1 attribute for Normal memory regions. This field is used in determining the Shareability of a memory region that is mapped to Normal memory and both:

- Is not Inner Non-cacheable, Outer Non-cacheable.
- Has the S bit in the translation table descriptor set to 1.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>NS1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Region is Non-shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Region is shareable. The value of the appropriate PRRR.NOS&lt;n&gt;</td>
</tr>
<tr>
<td></td>
<td>field determines whether the region is Inner Shareable or Outer</td>
</tr>
<tr>
<td></td>
<td>Shareable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NS0, bit [18]**

Mapping of S = 0 attribute for Normal memory regions. This field is used in determining the Shareability of a memory region that is mapped to Normal memory and both:

- Is not Inner Non-cacheable, Outer Non-cacheable.
- Has the S bit in the translation table descriptor set to 0.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>NS0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Region is Non-shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Region is shareable. The value of the appropriate PRRR.NOS&lt;n&gt;</td>
</tr>
<tr>
<td></td>
<td>field determines whether the region is Inner Shareable or Outer</td>
</tr>
<tr>
<td></td>
<td>Shareable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DS1, bit [17]**

Mapping of S = 1 attribute for Device memory. From Armv8, all types of Device memory are Outer Shareable, and therefore this bit is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**DS0, bit [16]**

Mapping of S = 0 attribute for Device memory. From Armv8, all types of Device memory are Outer Shareable, and therefore this bit is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**TR<n>, bits [2n+1:2n], for n = 7 to 0**

TR<n> is the primary TEX mapping for memory attributes n, and defines the mapped memory type for a region with attributes n. n is the value of the concatenation of the {TEX[0], C, B} bits from the translation table descriptor. The possible values for each field other than TR6 are:
The meaning of the TR6 field is IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the PRRR

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL3) then
        if TTBCR.EAE == '1' then
            return MAIR0_NS;
        else
            return PRRR_NS;
    else
        if TTBCR.EAE == '1' then
            return MAIR0;
        else
            return PRRR;
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && ELUsingAArch32(EL3) then
            if TTBCR.EAE == '1' then
                return MAIR0_NS;
            else
                return PRRR_NS;
        else
            if TTBCR.EAE == '1' then
                return MAIR0;
            else
                return PRRR;
    elsif PSTATE.EL == EL3 then
        if TTBCR.EAE == '1' then
            if SCR.NS == '0' then
                return MAIR0_S;
            else
                return MAIR0_NS;
        else
            if SCR.NS == '0' then
                return PRRR_S;
            else
                return PRRR_NS;
```
MCR{<c>}{<q>} {coproc}, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1010</td>
<td>0b0010</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
        UNDEFINED;
else if PSTATE.EL == EL1 then
        if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T10 == '1' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T10 == '1' then
                AArch32.TakeHypTrapException(0x03);
        elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
                AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
                AArch32.TakeHypTrapException(0x03);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
                if TTBCR.EAE == '1' then
                        MAIR0_NS = R[t];
                else
                        PRRR_NS = R[t];
                end if
        else
                if TTBCR.EAE == '1' then
                        MAIR0 = R[t];
                else
                        PRRR = R[t];
                end if
        end if
elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && ELUsingAArch32(EL3) then
                if TTBCR.EAE == '1' then
                        MAIR0_NS = R[t];
                else
                        PRRR_NS = R[t];
                end if
        else
                if TTBCR.EAE == '1' then
                        MAIR0 = R[t];
                else
                        PRRR = R[t];
                end if
        end if
elsif PSTATE.EL == EL3 then
        if SCR.NS == '0' && CP15SDISABLE == HIGH then
                UNDEFINED;
        elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
                UNDEFINED;
        else
                if TTBCR.EAE == '1' then
                        if SCR.NS == '0' then
                                MAIR0_S = R[t];
                        else
                                MAIR0_NS = R[t];
                        end if
                        if SCR.NS == '0' then
                                PRRR_S = R[t];
                        else
                                PRRR_NS = R[t];
                        end if
        end if
end if
REVIDR, Revision ID Register

The REVIDR characteristics are:

**Purpose**

Provides implementation-specific minor revision information.

**Configuration**

AArch32 System register REVIDR bits [31:0] are architecturally mapped to AArch64 System register `REVIDR_EL1[31:0]`.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to REVIDR are **UNDEFINED**.

If REVIDR has the same value as `MIDR`, then its contents have no significance.

**Attributes**

REVIDR is a 32-bit register.

**Field descriptions**

The REVIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>29</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>28</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>27</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>26</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>25</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>24</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>23</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>22</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>21</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>20</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>19</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>18</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>17</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>16</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>15</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>14</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>13</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>12</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>11</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>10</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>9</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>8</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>7</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>6</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>5</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>4</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>3</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>2</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>1</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**Accessing the REVIDR**

Accesses to this register use the following encodings:

```
MRC{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b110</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        return REVIDR;
    endif
elsif PSTATE.EL == EL2 then
    return REVIDR;
elsif PSTATE.EL == EL3 then
    return REVIDR;
end
The RMR characteristics are:

**Purpose**

If EL1 or EL3 is the highest implemented Exception level and this register is implemented:

- A write to the register at the highest implemented Exception level can request a Warm reset.
- If the highest implemented Exception level can use AArch32 and AArch64, this register specifies the Execution state that the PE boots into on a Warm reset.

**Configuration**

AArch32 System register RMR bits [31:0] are architecturally mapped to AArch64 System register RMR_EL1[31:0] when the highest implemented Exception level is EL1.

AArch32 System register RMR bits [31:0] are architecturally mapped to AArch64 System register RMR_EL3[31:0] when EL3 is implemented.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to RMR are UNDEFINED.

Only implemented if EL1 or EL3 is the highest implemented Exception level. In this case:

- If the highest implemented Exception level can use AArch32 and AArch64 then this register must be implemented.
- If the highest implemented Exception level cannot use AArch64 then it is IMPLEMENTATION DEFINED whether the register is implemented.

**Attributes**

RMR is a 32-bit register.

**Field descriptions**

The RMR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
<td></td>
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<tr>
<td>25</td>
<td></td>
<td></td>
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<td>24</td>
<td></td>
<td></td>
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<tr>
<td>23</td>
<td></td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0.</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
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<tr>
<td>15</td>
<td></td>
<td></td>
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<tr>
<td>14</td>
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<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Reset Request. Setting this bit to 1 requests a Warm reset.</td>
<td>1</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**AA64, bit [0]**

When the highest implemented Exception level can use AArch64, determines which Execution state the PE boots into after a Warm reset:

<table>
<thead>
<tr>
<th>AA64</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AArch32.</td>
</tr>
<tr>
<td>0b1</td>
<td>AArch64.</td>
</tr>
</tbody>
</table>
On coming out of the Warm reset, execution starts at the implementation defined reset vector address of the specified execution state.

If the highest implemented Exception level cannot use AArch64 this bit is RAZ/WI.

When implemented as a RW field, this field resets to 0 on a Cold reset.

### Accessing the RMR

When EL3 is implemented, Arm deprecates accessing this register from any PE mode other than Monitor mode.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc}_1>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc}_2> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL IN {EL1, EL3} && IsHighestEL(PSTATE.EL) then
  return RMR;
else
  UNDEFINED;

\[
\text{MCR}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc}_1>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc}_2> \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL IN {EL1, EL3} && IsHighestEL(PSTATE.EL) then
  RMR = R[t];
else
  UNDEFINED;
RVBAR, Reset Vector Base Address Register

The RVBAR characteristics are:

**Purpose**

If EL3 is not implemented, contains the IMPLEMENTATION DEFINED address that execution starts from after reset when executing in AArch32 state.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to RVBAR are UNDEFINED.

This register is only implemented if the highest Exception level implemented is capable of using AArch32, and is not EL3.

**Attributes**

RVBAR is a 32-bit register.

**Field descriptions**

The RVBAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Field Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-1</td>
<td>Reset Address[31:1]</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES1</td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reset Address[31:1]. Bits [31:1] of the IMPLEMENTATION DEFINED address that execution starts from after reset when executing in 32-bit state.

**Bit [0]**

Reserved, RES1.

**Accessing the RVBAR**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if IsHighestEL(EL1) then
        return RVBAR;
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    if IsHighestEL(EL2) then
        return RVBAR;
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL3 then
    return MVBAR;
SCR, Secure Configuration Register

The SCR characteristics are:

**Purpose**

When EL3 is implemented and can use AArch32, defines the configuration of the current Security state. It specifies:

- The Security state, either Secure or Non-secure.
- What mode the PE branches to if an IRQ, FIQ, or External abort occurs.
- Whether the PSTATE.F or PSTATE.A bits can be modified when SCR.NS==1.

**Configuration**

AArch32 System register SCR bits [31:0] can be mapped to AArch64 System register SCR_EL3[31:0], but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SCR are UNDEFINED.

**Attributes**

SCR is a 32-bit register.

**Field descriptions**

The SCR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>TERR</td>
<td>RES0</td>
<td>TW</td>
<td>RES0</td>
<td>SIF</td>
<td>HCE</td>
<td>SCD</td>
<td>nET</td>
<td>AWF</td>
<td>WEAF</td>
<td>FIQ</td>
<td>IRONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**TERR, bit [15]**

When FEAT_RAS is implemented:

Trap Error record accesses. Generate a Monitor Trap exception on accesses to the following registers from modes other than Monitor mode:

ERRIDR, ERRSELR, ERXADDR, ERXADDR2, ERXCTLR, ERXCTRLR2, ERXF, ERXFR2, ERXMISC0, ERXMISC1, ERXMISC2, ERXMISC3, and ERXSTATUS. When FEAT_RASv1p1 is implemented, ERXMISC4, ERXMISC5, ERXMISC6, ERXMISC7.

<table>
<thead>
<tr>
<th>TERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to the specified registers from modes other than Monitor mode generate a Monitor Trap exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Otherwise:**

Reserved, RES0.
**Bit [14]**

Reserved, RES0.

**TWE, bit [13]**

Traps WFE instructions to Monitor mode.

<table>
<thead>
<tr>
<th>TWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped. Any attempt to execute a WFE instruction in any mode other than Monitor mode is trapped to Monitor mode, if the instruction would otherwise have caused the PE to enter a low-power state and the attempted execution does not generate an exception that is taken to EL1 or EL2 by $\text{SCTLR.nTWE}$ or $\text{HCR.TWE}$. Any exception that is taken to EL1 or to EL2 has priority over this trap.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

The attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**TWI, bit [12]**

Traps WFI instructions to Monitor mode.

<table>
<thead>
<tr>
<th>TWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped. Any attempt to execute a WFI instruction in any mode other than Monitor mode is trapped to Monitor mode, if the instruction would otherwise have caused the PE to enter a low-power state and the attempted execution does not generate an exception that is taken to EL1 or EL2 by $\text{SCTLR.nTWI}$ or $\text{HCR.TWI}$. Any exception that is taken to EL1 or to EL2 has priority over this trap.</td>
</tr>
<tr>
<td>0b1</td>
<td></td>
</tr>
</tbody>
</table>

The attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Bits [11:10]**

Reserved, RES0.
**SIF, bit [9]**

Secure instruction fetch. When the PE is in Secure state, this bit disables instruction fetch from Non-secure memory. The possible values for this bit are:

<table>
<thead>
<tr>
<th>SIF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state instruction fetches from Non-secure memory are permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure state instruction fetches from Non-secure memory are not permitted.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**HCE, bit [8]**

Hypervisor Call instruction enable. If EL2 is implemented, enables execution of HVC instructions at Non-secure EL1 and EL2.

<table>
<thead>
<tr>
<th>HCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>HVC instructions are:</td>
</tr>
<tr>
<td></td>
<td>• UNDEFINED at Non-secure EL1. The Undefined Instruction exception is taken from PL1 to PL1.</td>
</tr>
<tr>
<td></td>
<td>• UNPREDICTABLE at EL2. Behavior is one of the following:</td>
</tr>
<tr>
<td></td>
<td>◦ The instruction is UNDEFINED.</td>
</tr>
<tr>
<td></td>
<td>◦ The instruction executes as a NOP.</td>
</tr>
<tr>
<td>0b1</td>
<td>HVC instructions are enabled at Non-secure EL1 and EL2.</td>
</tr>
</tbody>
</table>

**Note**

HVC instructions are always UNDEFINED at EL0 and in Secure state.

If EL2 is not implemented, this bit is RES0 and HVC is UNDEFINED.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**SCD, bit [7]**

Secure Monitor Call disable. Disables SMC instructions.

<table>
<thead>
<tr>
<th>SCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SMC instructions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>In Non-secure state, SMC instructions are UNDEFINED. The Undefined Instruction exception is taken from the current Exception level to the current Exception level. In Secure state, behavior is one of the following:</td>
</tr>
<tr>
<td></td>
<td>◦ The instruction is UNDEFINED.</td>
</tr>
<tr>
<td></td>
<td>◦ The instruction executes as a NOP.</td>
</tr>
</tbody>
</table>

**Note**

SMC instructions are always UNDEFINED at PL0.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**nET, bit [6]**

Not Early Termination. This bit disables early termination.

<table>
<thead>
<tr>
<th>nET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Early termination permitted. Execution time of data operations can depend on the data values.</td>
</tr>
<tr>
<td>0b1</td>
<td>Disable early termination. The number of cycles required for data operations is forced to be independent of the data values.</td>
</tr>
</tbody>
</table>
This implementation defined mechanism can disable data dependent timing optimizations from multiplies and data operations. It can provide system support against information leakage that might be exploited by timing correlation types of attack.

On implementations that do not support early termination or do not support disabling early termination, this bit is RES0.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**AW, bit [5]**

When the value of SCR.EA is 1 and the value of HCR.AMO is 0, this bit controls whether PSTATE.A masks an External abort taken from Non-secure state.

<table>
<thead>
<tr>
<th>AW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External aborts taken from Non-secure state are not masked by PSTATE.A, and are taken to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>External aborts taken from Secure state are masked by PSTATE.A. When PSTATE.A is 0, the abort is taken to EL3.</td>
</tr>
</tbody>
</table>

When SCR.EA is 0 or HCR.AMO is 1, this bit has no effect.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**FW, bit [4]**

When the value of SCR.FIQ is 1 and the value of HCR.FMO is 0, this bit controls whether PSTATE.F masks an FIQ interrupt taken from Non-secure state.

<table>
<thead>
<tr>
<th>FW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An FIQ taken from Non-secure state is not masked by PSTATE.F, and is taken to EL3.</td>
</tr>
<tr>
<td>0b1</td>
<td>An FIQ taken from Secure state is masked by PSTATE.F.</td>
</tr>
</tbody>
</table>

When SCR.FIQ is 0 or HCR.FMO is 1, this bit has no effect.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**EA, bit [3]**

External Abort handler. This bit controls which mode takes External aborts and SError interrupt exceptions.

<table>
<thead>
<tr>
<th>EA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External aborts taken to Abort mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>External aborts taken to Monitor mode.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**FIQ, bit [2]**

FIQ handler. This bit controls which mode takes FIQ exceptions.

<table>
<thead>
<tr>
<th>FIQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FIQs taken to FIQ mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>FIQs taken to Monitor mode.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**IRQ, bit [1]**

IRQ handler. This bit controls which mode takes IRQ exceptions.
**IRQ**

<table>
<thead>
<tr>
<th>IRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>IRQs taken to IRQ mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>IRQs taken to Monitor mode.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**NS, bit [0]**

Non-secure bit. Except when the PE is in Monitor mode, this bit determines the Security state of the PE:

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PE is in Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>PE is in Non-secure state.</td>
</tr>
</tbody>
</table>

If the HCR.TGE bit is set, an attempt to change from a Secure PL1 mode to a Non-secure EL1 mode by changing the SCR.NS bit from 0 to 1 results in the SCR.NS bit remaining as 0.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Accessing the SCR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>\{, \{#\}<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif !ELUsingAArch32(EL3) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif !ELUsingAArch32(EL3) && SCR_EL3.NS == '0' then
        AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        UNDEFINED;
elsif PSTATE.EL == EL3 then
    return SCR;

\[
\text{MCR\{<c>\}{<q>} <coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm>\{, \{#\}<opc2>\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif !ELUsingAArch32(EL2) && SCR_EL3.<NS,EEL2> == '01' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        UNDEFINED;
    elsif PSTATE.EL == EL2 then
        UNDEFINED;
    elseif PSTATE.EL == EL3 then
        SCR = R[t];
else
    UNDEFINED;
SCTLR, System Control Register

The SCTLR characteristics are:

**Purpose**

Provides the top level control of the system, including its memory system.

**Configuration**

AArch32 System register SCTLR bits [31:0] are architecturally mapped to AArch64 System register SCTLR_EL1[31:0]. This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SCTLR are UNDEFINED.

Some bits in the register are read-only. These bits relate to non-configurable features of an implementation, and are provided for compatibility with previous versions of the architecture.

**Attributes**

SCTLR is a 32-bit register.

**Field descriptions**

The SCTLR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| DSSBS | TE | AF | ET | RES0 | EE | RES0 | SPAN | RES1 | RES0 | UWXN | WXN | nTWE | RES0 | nTWI | RES0 | V | RES1 | EnRCTX | RES0 | SED | ITD | UNK | CP15BEN | LSMAOE | nTLSMD | C | A | M |

**DSSBS, bit [31]**

When FEAT_SSBS is implemented:

Default PSTATE.SSBS value on Exception Entry. The defined values are:

<table>
<thead>
<tr>
<th>DSSBS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PSTATE.SSBS is set to 0 on an exception to any mode in this security state except Hyp mode</td>
</tr>
<tr>
<td>0b1</td>
<td>PSTATE.SSBS is set to 1 on an exception to any mode in this security state except Hyp mode</td>
</tr>
</tbody>
</table>

**Note**

When EL3 is implemented and is using AArch32, this bit is banked between the two Security states.

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

**Otherwise:**

Reserved, RES0.

**TE, bit [30]**

T32 Exception Enable. This bit controls whether exceptions to an Exception Level that is executing at PL1 are taken to A32 or T32 state:
Meaning

| TE | Exceptions, including reset, taken to A32 state. |
|    | Exceptions, including reset, taken to T32 state. |

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

**AFE, bit [29]**

Access Flag Enable. When using the Short-descriptor translation table format for the PL1&0 translation regime, this bit enables use of the AP[0] bit in the translation descriptors as the Access flag, and restricts access permissions in the translation descriptors to the simplified model. The possible values of this bit are:

<table>
<thead>
<tr>
<th>AFE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>In the translation table descriptors, AP[0] is an access permissions bit. The full range of access permissions is supported. No Access flag is implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>In the translation table descriptors, AP[0] is the Access flag. Only the simplified model for access permissions is supported.</td>
</tr>
</tbody>
</table>

When using the Long-descriptor translation table format, the VMSA behaves as if this bit is set to 1, regardless of the value of this bit.

The AFE bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 0.

**TRE, bit [28]**

TEX remap enable. This bit enables remapping of the TEX[2:1] bits in the PL1&0 translation regime for use as two translation table bits that can be managed by the operating system. Enabling this remapping also changes the scheme used to describe the memory region attributes in the VMSA. The possible values of this bit are:

<table>
<thead>
<tr>
<th>TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TEX remap disabled. TEX[2:0] are used, with the C and B bits, to describe the memory region attributes.</td>
</tr>
<tr>
<td>0b1</td>
<td>TEX remap enabled. TEX[2:1] are reassigned for use as bits managed by the operating system. The TEX[0], C, and B bits are used to describe the memory region attributes, with the MMU remap registers.</td>
</tr>
</tbody>
</table>

When the value of TTBCR.EAE is 1, this bit is RES1.

The TRE bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 0.

**Bits [27:26]**

Reserved, RES0.

**EE, bit [25]**

The value of the PSTATE.E bit on branch to an exception vector or coming out of reset, and the endianness of stage 1 translation table walks in the PL1&0 translation regime.

The possible values of this bit are:

<table>
<thead>
<tr>
<th>EE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Little-endian. PSTATE.E is cleared to 0 on taking an exception or coming out of reset. Stage 1 translation table walks in the PL1&amp;0 translation regime are little-endian.</td>
</tr>
<tr>
<td>0b1</td>
<td>Big-endian. PSTATE.E is set to 1 on taking an exception or coming out of reset. Stage 1 translation table walks in the PL1&amp;0 translation regime are big-endian.</td>
</tr>
</tbody>
</table>
If an implementation does not provide Big-endian support for data accesses at Exception Levels higher than EL0, this bit is RES0.

If an implementation does not provide Little-endian support for data accesses at Exception Levels higher than EL0, this bit is RES1.

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

**Bit [24]**

Reserved, RES0.

**SPAN, bit [23]**

*When FEAT_PAN is implemented:*

Set Privileged Access Never, on taking an exception to EL1 from either Secure or Non-secure state, or to EL3 from Secure state when EL3 is using AArch32.

<table>
<thead>
<tr>
<th>SPAN</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0  | PSTATE.PAN is set to 1 in the following situations:  
  - In Non-secure state, on taking an exception to EL1.  
  - In Secure state, when EL3 is using AArch64, on taking an exception to EL1.  
  - In Secure state, when EL3 is using AArch32, on taking an exception to EL3. |
| 0b1  | The value of PSTATE.PAN is left unchanged on taking an exception to EL1. |

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES1.

**Bit [22]**

Reserved, RES1.

**Bit [21]**

Reserved, RES0.

**UWXN, bit [20]**

Unprivileged write permission implies PL1 XN (Execute-never). This bit can force all memory regions that are writable at PL0 to be treated as XN for accesses from software executing at PL1. The possible values of this bit are:

<table>
<thead>
<tr>
<th>UWXN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control has no effect on memory access permissions.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any region that is writable at PL0 forced to XN for accesses from software executing at PL1.</td>
</tr>
</tbody>
</table>

The UWXN bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 0.

**WXN, bit [19]**

Write permission implies XN (Execute-never). For the PL1&0 translation regime, this bit can force all memory regions that are writable to be treated as XN. The possible values of this bit are:
This bit applies only when SCTLR.M bit is set.

The WXN bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 0.

### nTWE, bit [18]

Traps EL0 execution of WFE instructions to Undefined mode.

<table>
<thead>
<tr>
<th>nTWE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFE instruction at EL0 is trapped to Undefined mode, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
</tbody>
</table>

The attempted execution of a conditional WFE instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, this field resets to 1.

### Bit [17]

Reserved, RES0.

### nTWI, bit [16]

Traps EL0 execution of WFI instructions to Undefined mode.

<table>
<thead>
<tr>
<th>nTWI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This control does not cause any instructions to be trapped.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt to execute a WFI instruction at EL0 is trapped to Undefined mode, if the instruction would otherwise have caused the PE to enter a low-power state.</td>
</tr>
</tbody>
</table>

The attempted execution of a conditional WFI instruction is only trapped if the instruction passes its condition code check.

**Note**

Since a WFE or WFI can complete at any time, even without a Wakeup event, the traps on WFE of WFI are not guaranteed to be taken, even if the WFE or WFI is executed when there is no Wakeup event. The only guarantee is that if the instruction does not complete in finite time in the absence of a Wakeup event, the trap will be taken.

On a Warm reset, this field resets to 1.
Bits [15:14]

Reserved, RES0.

V, bit [13]

Vectors bit. This bit selects the base address of the exception vectors for exceptions taken to a PE mode other than Monitor mode or Hyp mode:

<table>
<thead>
<tr>
<th>V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal exception vectors. Base address is held in <strong>VBAR</strong>.</td>
</tr>
<tr>
<td>0b1</td>
<td>High exception vectors (Hivecs), base address 0xFFFF0000. This base address cannot be remapped.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

I, bit [12]

Instruction access Cacheability control, for accesses at EL1 and EL0:

<table>
<thead>
<tr>
<th>I</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All instruction access to Normal memory from PL1 and PL0 are Non-cacheable for all levels of instruction and unified cache. If the value of SCTLR.M is 0, instruction accesses from stage 1 of the PL1&amp;0 translation regime are to Normal, Outer Shareable, Inner Non-cacheable, Outer Non-cacheable memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>All instruction access to Normal memory from PL1 and PL0 can be cached at all levels of instruction and unified cache. If the value of SCTLR.M is 0, instruction accesses from stage 1 of the PL1&amp;0 translation regime are to Normal, Outer Shareable, Inner Write-Through, Outer Write-Through memory.</td>
</tr>
</tbody>
</table>

Instruction accesses to Normal memory from EL1 and EL0 are Cacheable regardless of the value of the SCTLR.I bit if either:

- EL2 is using AArch32 and the value of **HCR.DC** is 1.
- EL2 is using AArch64 and the value of **HCR_EL2.DC** is 1.

On a Warm reset, this field resets to 0.

Bit [11]

Reserved, RES1.

EnRCTX, bit [10]

When FEAT_CSV2 is implemented:

Enable EL0 Access to the AArch32 CFPRCTX, DVPRCTX and CPPRCTX instructions. The defined values are:

<table>
<thead>
<tr>
<th>EnRCTX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL0 access to these instructions is disabled, and these instructions are trapped to EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL0 access to these instructions is enabled.</td>
</tr>
</tbody>
</table>

Note

When EL3 is implemented and is using AArch32, this bit is banked between the two Security states.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

Bit [9]

Reserved, RES0.

SED, bit [8]

SETEND instruction disable. Disables SETEND instructions at PL0 and PL1.

<table>
<thead>
<tr>
<th>SED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SETEND instruction execution is enabled at PL0 and PL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>SETEND instructions are UNDEFINED at PL0 and PL1.</td>
</tr>
</tbody>
</table>

If the implementation does not support mixed-endian operation at any Exception level, this bit is RES1.

On a Warm reset, this field resets to 0.

ITD, bit [7]

IT Disable. Disables some uses of IT instructions at PL1 and PL0.

<table>
<thead>
<tr>
<th>ITD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All IT instruction functionality is enabled at PL1 and PL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Any attempt at PL1 or PL0 to execute any of the following is UNDEFINED:</td>
</tr>
</tbody>
</table>

- All encodings of the IT instruction with hw1[3:0]!=1000.
- All encodings of the subsequent instruction with the following values for hw1:
  - 11xxxxxxxxxxxx: All 32-bit instructions, and the 16-bit instructions B, UDF, SVC, LDM, and STM.
  - 1011xxxxxxxxxx: All instructions in 'Miscellaneous 16-bit instructions'.
  - 10100xxxxxxxxxxx: ADD Rd, PC, #imm
  - 01001xxxxxxxxxxx: LDR Rd, [PC, #imm]
  - 01001xxx1111xxx: ADD Rdn, PC; CMP Rn, PC; MOV Rdr, PC; BX PC; BLX PC.
  - 010001x1xxxx111: ADD PC, Rm; CMP PC, Rm; MOV PC, Rm. This pattern also covers unpredictable cases with BLX Rm.

These instructions are always UNDEFINED, regardless of whether they would pass or fail the condition code check that applies to them as a result of being in an IT block.

It is IMPLEMENTATION DEFINED whether the IT instruction is treated as:

- A 16-bit instruction, that can only be followed by another 16-bit instruction.
- The first half of a 32-bit instruction.

This means that, for the situations that are UNDEFINED, either the second 16-bit instruction or the 32-bit instruction is UNDEFINED.

An implementation might vary dynamically as to whether IT is treated as a 16-bit instruction or the first half of a 32-bit instruction.

If an instruction in an active IT block that would be disabled by this field sets this field to 1 then behavior is CONSTRAINED UNPREDICTABLE. For more information see 'Changes to an ITD control by an instruction in an IT block'.

ITD is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAZ/WI.

On a Warm reset, this field resets to 0.
UNK, bit [6]

Writes to this bit are IGNORED. Reads of this bit return an UNKNOWN value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

CP15BEN, bit [5]

System instruction memory barrier enable. Enables accesses to the DMB, DSB, and ISB System instructions in the (coproc==0b1111) encoding space from PL1 and PL0:

<table>
<thead>
<tr>
<th>CP15BEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PL0 and PL1 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is UNDEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>PL0 and PL1 execution of the CP15DMB, CP15DSB, and CP15ISB instructions is enabled.</td>
</tr>
</tbody>
</table>

CP15BEN is optional, but if it is implemented in the SCTLR then it must also be implemented in the SCTLR_EL1. If it is not implemented then this bit is RAO/WI.

On a Warm reset, this field resets to 1.

LSMAOE, bit [4]

When FEAT_LSMAOC is implemented:

Load Multiple and Store Multiple Atomicity and Ordering Enable.

<table>
<thead>
<tr>
<th>LSMAOE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For all memory accesses at EL1 or EL0, A32 and T32 Load Multiple and Store Multiple can have an interrupt taken during the sequence memory accesses, and the memory accesses are not required to be ordered.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ordering and interrupt behavior of A32 and T32 Load Multiple and Store Multiple at EL1 or EL0 is as defined for Armv8.0.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 1.

Otherwise:

Reserved, RES1.

nTLSMD, bit [3]

When FEAT_LSMAOC is implemented:

No Trap Load Multiple and Store Multiple to Device-nGRE/Device-nGnRE/Device-nGnRnE memory.

<table>
<thead>
<tr>
<th>nTLSMD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL1 or EL0 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are trapped and generate a stage 1 Alignment fault.</td>
</tr>
<tr>
<td>0b1</td>
<td>All memory accesses by A32 and T32 Load Multiple and Store Multiple at EL1 or EL0 that are marked at stage 1 as Device-nGRE/Device-nGnRE/Device-nGnRnE memory are not trapped.</td>
</tr>
</tbody>
</table>

This bit is permitted to be cached in a TLB.

On a Warm reset, this field resets to 1.
Otherwise:

Reserved, RES1.

**C, bit [2]**

Cacheability control, for data accesses at EL1 and EL0:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All data access to Normal memory from PL1 and PL0, and all accesses to the PL1&amp;0 stage 1 translation tables, are Non-cacheable for all levels of data and unified cache.</td>
</tr>
<tr>
<td>0b1</td>
<td>All data access to Normal memory from PL1 and PL0, and all accesses to the PL1&amp;0 stage 1 translation tables, can be cached at all levels of data and unified cache.</td>
</tr>
</tbody>
</table>

The PE ignores SCTLR.C for Non-secure state and data accesses to Normal memory from EL1 and EL0 are Cacheable if either:

- EL2 is using AArch32 and the value of $HCR_{DC}$ is 1.
- EL2 is using AArch64 and the value of $HCR_{EL2}_{DC}$ is 1.

On a Warm reset, this field resets to 0.

**A, bit [1]**

Alignment check enable. This is the enable bit for Alignment fault checking at PL1 and PL0:

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Alignment fault checking disabled when executing at PL1 or PL0. Instructions that load or store one or more registers, other than load/store exclusive and load-acquire/store-release, do not check that the address being accessed is aligned to the size of the data element(s) being accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Alignment fault checking enabled when executing at PL1 or PL0. All instructions that load or store one or more registers have an alignment check that the address being accessed is aligned to the size of the data element(s) being accessed. If this check fails it causes an Alignment fault, which is taken as a Data Abort exception.</td>
</tr>
</tbody>
</table>

Load/store exclusive and load-acquire/store-release instructions have an alignment check regardless of the value of the A bit.

On a Warm reset, this field resets to 0.

**M, bit [0]**

MMU enable for EL1 and EL0 stage 1 address translation. Possible values of this bit are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>EL1 and EL0 stage 1 address translation disabled. See the SCTLR.I field for the behavior of instruction accesses to Normal memory.</td>
</tr>
<tr>
<td>0b1</td>
<td>EL1 and EL0 stage 1 address translation enabled.</td>
</tr>
</tbody>
</table>

In the Non-secure state the PE behaves as if the value of the SCTLR.M field is 0 for all purposes other than returning the value of a direct read of the field if either:

- EL2 is using AArch32 and the value of $HCR_{\{DC, TGE\}}$ is not {0, 0}.
- EL2 is using AArch64 and the value of $HCR_{EL2}\_{\{DC, TGE\}}$ is not {0, 0}.

On a Warm reset, this field resets to 0.
Accessing the SCTLR

Accesses to this register use the following encodings:

\[ \text{MRC\{}<c>{q}\}\ <\text{coproc}, \#<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\{, \#<\text{opc2}\}\} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return SCTLR_NS;
    else
        return SCTLR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return SCTLR_NS;
    else
        return SCTLR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return SCTLR_S;
    else
        return SCTLR_NS;

MCR\{}<c>{q}\}\ <\text{coproc}, \#<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\{, \#<\text{opc2}\}\} \]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        SCTLR_NS = R[t];
    else
        SCTLR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        SCTLR_NS = R[t];
    else
        SCTLR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR_NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR_NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR_NS == '0' then
            SCTLR_S = R[t];
        else
            SCTLR_NS = R[t];

SDCR, Secure Debug Control Register

The SDCR characteristics are:

**Purpose**

Provides EL3 configuration options for self-hosted debug, trace, and the Performance Monitors Extension.

**Configuration**

AArch32 System register SDCR bits [31:0] can be mapped to AArch64 System register MDCR_EL3[31:0], but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SDCR are UNDEFINED.

**Attributes**

SDCR is a 32-bit register.

**Field descriptions**

The SDCR bit assignments are:

```
31  30  29  28  27  26  25  24  23  22  21  20  19  18  17  16  15  14  13  12  11  10  9  8  7  6  5  4  3  2  1  0
RES0 MTPME|TDCC RES0 SCCD|RES0|EPMAD|EDAD|TT|TR|STE|SP|RES0|RES0|RES0|RES0|RES0|RES0|RES0|RES0
```

**Bits [31:29]**

Reserved, RES0.

**MTPME, bit [28]**

When FEAT_MTPMU is implemented:

Multi-threaded PMU Enable. Enables use of the PMEVTYPER<n>.MT bits.

<table>
<thead>
<tr>
<th>MTPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FEAT_MTPMU is disabled. The Effective value of PMEVTYPER&lt;n&gt;.MT is zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMEVTYPER&lt;n&gt;.MT bits not affected by this bit.</td>
</tr>
</tbody>
</table>

If FEAT_MTPMU is disabled for any other PE in the system that has the same level 1 Affinity as the PE, it is IMPLEMENTATION DEFINED whether the PE behaves as if this bit is 0b0.

On a Cold reset, in a system where the PE resets into EL3, this field resets to 1.

**Otherwise:**

Reserved, RES0.

**TDCC, bit [27]**

When FEAT_FGT is implemented:

Trap DCC. Traps use of the Debug Comms Channel in modes other than Monitor mode to Monitor mode.
The DCC registers trapped by this control are:

- **DBGDTRRXext**, **DBGDTRTXext**, **DBGDSCRInt**, **DBGDCCINT**, and, when the PE is in Non-debug state, **DBGDTRRXint** and **DBGDTRTXint**.

When the PE is in Debug state, SDCR.TDCC does not trap any accesses to:

- **DBGDTRRXint** and **DBGDTRTXint**.

On a Warm reset, in a system where the PE resets into EL3, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

- Reserved, RES0.

**Bits [26:24]**

- Reserved, RES0.

**SCCD, bit [23]**

When **FEAT_PMUv3p5** is implemented:

Secure Cycle Counter Disable. Prohibits **PMCCNTR** from counting in Secure state.

<table>
<thead>
<tr>
<th>SCCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by <strong>PMCCNTR</strong> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counting by <strong>PMCCNTR</strong> is prohibited in Secure state.</td>
</tr>
</tbody>
</table>

This bit does not affect the CPU_CYCLES event or any other event that counts cycles.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Otherwise:**

- Reserved, RES0.

**Bit [22]**

- Reserved, RES0.

**EPMAD, bit [21]**

When **FEAT_Debugv8p4** is implemented and **FEAT_PMUv3** is implemented:

External Performance Monitors Non-secure access disable. Controls Non-secure access to Performance Monitors registers by an external debugger.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure access to the Performance Monitors registers from an external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure access to the Performance Monitors registers from an external debugger is not permitted.</td>
</tr>
</tbody>
</table>

If the Performance Monitors Extension does not support external debug interface accesses this bit is **RES0**.
Otherwise, if EL3 is not implemented and the Effective value of `SCR.NS` is 0b0, then the Effective value of this field is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**When FEAT_PMUv3 is implemented:**

External Performance Monitors access disable. Controls access to Performance Monitors registers by an external debugger.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to Performance Monitors registers from an external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to Performance Monitors registers from an external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
</tbody>
</table>

If the Performance Monitors Extension does not support external debug interface accesses this bit is RES0.

Otherwise, if EL3 is not implemented and the Effective value of `SCR.NS` is 0b0, then the Effective value of this field is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**EDAD, bit [20]**

**When FEAT_Debugv8p4 is implemented:**

External debug Non-secure access disable. Controls Non-secure access to breakpoint, watchpoint, and `OSLAR_EL1` registers by an external debugger.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure access to debug registers from an external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure access to breakpoint registers, watchpoint registers, and <code>OSLAR_EL1</code> from an external debugger is not permitted.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of `SCR.NS` is 0b0, then the Effective value of this field is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**When FEAT_Debugv8p2 is implemented:**

External debug access disable. Controls access to breakpoint, watchpoint, and `OSLAR_EL1` registers by an external debugger.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to debug registers from an external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to breakpoint registers, watchpoint registers and <code>OSLAR_EL1</code> from an external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of `SCR.NS` is 0b0, then the Effective value of this field is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.
External debug access disable. Controls access to breakpoint, watchpoint, and optionally OSLAR_EL1 registers by an external debugger:

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Access to debug registers from an external debugger is permitted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access to breakpoint registers and watchpoint registers from an external debugger is not permitted, unless overridden by the IMPLEMENTATION DEFINED authentication interface. It is IMPLEMENTATION DEFINED whether access to the OSLAR_EL1 register from an external debugger is permitted or not permitted.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of SCR NS is 0b0, then the Effective value of this field is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

**TTRF, bit [19]**

When FEAT_TRF is implemented:

Trap Trace Filter controls. Controls whether accesses at EL2 and EL1 to the trace filter control registers are trapped to EL3.

<table>
<thead>
<tr>
<th>TTRF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to HTRFCR and TRFCR registers are not affected by this control bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>When not in Monitor mode, accesses to HTRFCR and TRFCR registers generate a Monitor Trap exception, unless the access generates a higher priority exception.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

**STE, bit [18]**

When FEAT_TRF is implemented:

Secure Trace Enable. This bit enables tracing in Secure state and controls the level of authentication required by an external debugger to enable external tracing.

<table>
<thead>
<tr>
<th>STE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Trace is prohibited in Secure state unless overridden by the IMPLEMENTATION DEFINED authentication interface.</td>
</tr>
<tr>
<td>0b1</td>
<td>Trace in Secure state is not affected by this bit.</td>
</tr>
</tbody>
</table>

This bit also controls the level of authentication required by an external debugger to enable external tracing. See 'Register controls to enable self-hosted trace'.

If EL3 is not implemented and the Effective value of SCR NS is 0b0, the PE behaves as if this bit is set to 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

**SPME, bit [17]**
When **FEAT_Debugv8p2** is implemented and **FEAT_PMUv3** is implemented:

Secure Performance Monitors enable. This allows event counting in Secure state.

<table>
<thead>
<tr>
<th>SPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting prohibited in Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting allowed in Secure state.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of **SCR.NS** is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

When **FEAT_PMUv3** is implemented:

Secure Performance Monitors enable. This allows event counting in Secure state.

<table>
<thead>
<tr>
<th>SPME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counting prohibited in Secure state, unless ExternalSecureNoninvasiveDebugEnabled() is TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counting allowed in Secure state.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the Effective value of **SCR.NS** is 0b0, then the Effective value of this bit is 0b1.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.

Otherwise:

Reserved, RES0.

**Bit [16]**

Reserved, RES0.

**SPD, bits [15:14]**

AArch32 Secure self-hosted Privileged Debug. Enables or disables debug exceptions from EL3, other than Breakpoint Instruction exceptions

<table>
<thead>
<tr>
<th>SPD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Legacy mode. Debug exceptions from EL3 are enabled by the authentication interface.</td>
</tr>
<tr>
<td>0b10</td>
<td>Secure privileged debug disabled. Debug exceptions from EL3 are disabled.</td>
</tr>
<tr>
<td>0b11</td>
<td>Secure privileged debug enabled. Debug exceptions from EL3 are enabled.</td>
</tr>
</tbody>
</table>

Other values are reserved, and have the **CONSTRAINED UNPREDICTABLE** behavior that they must have the same behavior as 0b00. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

This field has no effect on Breakpoint Instruction exceptions. These are always enabled.

This field is ignored in Non-secure state.

If debug exceptions from EL3 are enabled, then debug exceptions from Secure EL0 are also enabled.

Otherwise, debug exceptions from Secure EL0 are enabled only if the value of **SDER.SUIDEN** is 0b1.

If EL3 is not implemented and the Effective value of **SCR.NS** is 0b0, then the Effective value of this field is 0b11.

On a Warm reset, in a system where the PE resets into EL3, this field resets to 0.
Bits [13:0]

Reserved, RES0.

**Accessing the SDCR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} == \text{EL0}\) then
    UNDEFINED;
elsif \(\text{PSTATE.EL} == \text{EL1}\) then
    if \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HSTR.EL2.T1} == '1'\) then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HSTR.T1} == '1'\) then
        \text{AArch32.TakeHypTrapException(0x03)};
    elsif !\text{ELUsingAArch32(EL2)} \&\& \text{SCR.EL3.<NS,EEL2>} == '01' then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif !\text{ELUsingAArch32(EL3)} \&\& \text{SCR.EL3.NS} == '0' then
        \text{AArch64.AArch32SystemAccessTrap(EL3, 0x03)};
    else
        UNDEFINED;
    endif
elsif \(\text{PSTATE.EL} == \text{EL2}\) then
    if \(\text{!ELUsingAArch32(EL3)} \&\& \text{SCR.NS} == '0' \&\& \text{CP15SDISABLE2} == \text{HIGH}\) then
        UNDEFINED;
    else
        \(\text{SDCR} = \text{R[t]}\);
    endif
elsif \(\text{PSTATE.EL} == \text{EL3}\) then
    return \(\text{SDCR}\);
endif

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} == \text{EL0}\) then
    UNDEFINED;
elsif \(\text{PSTATE.EL} == \text{EL1}\) then
    if \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HSTR.EL2.T1} == '1'\) then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HSTR.T1} == '1'\) then
        \text{AArch32.TakeHypTrapException(0x03)};
    elsif !\text{ELUsingAArch32(EL2)} \&\& \text{SCR.EL3.<NS,EEL2>} == '01' then
        \text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)};
    elsif !\text{ELUsingAArch32(EL3)} \&\& \text{SCR.EL3.NS} == '0' then
        \text{AArch64.AArch32SystemAccessTrap(EL3, 0x03)};
    else
        UNDEFINED;
    endif
elsif \(\text{PSTATE.EL} == \text{EL2}\) then
    if \(\text{!ELUsingAArch32(EL3)} \&\& \text{SCR.NS} == '0' \&\& \text{CP15SDISABLE2} == \text{HIGH}\) then
        UNDEFINED;
    else
        \(\text{SDCR} = \text{R[t]}\);
    endif
elsif \(\text{PSTATE.EL} == \text{EL3}\) then
    if \(\text{SCR.NS} == '0' \&\& \text{CP15SDISABLE2} == \text{HIGH}\) then
        UNDEFINED;
    else
        \(\text{SDCR} = \text{R[t]}\);
    endif
endif

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SDER, Secure Debug Enable Register

The SDER characteristics are:

**Purpose**

Controls invasive and non-invasive debug in the Secure EL0 mode.

**Configuration**

AArch32 System register SDER bits [31:0] are architecturally mapped to AArch64 System register SDER32_EL3[31:0].

This register is present only when AArch32 is supported at any Exception level, or EL3 is implemented or the implemented Security state is Secure state. Otherwise, direct accesses to SDER are UNDEFINED.

This register is ignored by the PE when one or more of the following are true:

- The PE is in Non-secure state.
- EL1 is using AArch64.

**Attributes**

SDER is a 32-bit register.

**Field descriptions**

The SDER bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0          |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | SUNIDEN | SUIDEN |

**Bits [31:2]**

Reserved, RES0.

**SUNIDEN, bit [1]**

Secure User Non-Invasive Debug Enable.

<table>
<thead>
<tr>
<th>SUNIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect Performance Monitors event counting at Secure EL0</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL3 or EL1 is using AArch32, Performance Monitors event counting is allowed in Secure EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**SUIDEN, bit [0]**

Secure User Invasive Debug Enable.

<table>
<thead>
<tr>
<th>SUIDEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This bit does not affect the generation of debug exceptions at Secure EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>If EL3 or EL1 is using AArch32, debug exceptions from Secure EL0 are enabled.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to 0.

## Accessing the SDER

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>}\ <\text{coproc}, \{#\}<\text{opc1}, <\text{Rt}, <\text{CRn}, <\text{CRm}\{, \{#\}<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif (!HaveEL(EL3) || !ELUsingAArch32(EL3)) && SCR_EL3.NS == '0' then
    return SDER;
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' && CP15SDISABLE2 == HIGH then
    UNDEFINED;
  else
    SDER = R[t];

\[
\text{MCR}\{<c>\}{<q>}\ <\text{coproc}, \{#\}<\text{opc1}, <\text{Rt}, <\text{CRn}, <\text{CRm}\{, \{#\}<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif (!HaveEL(EL3) || !ELUsingAArch32(EL3)) && SCR_EL3.NS == '0' then
    SDER = R[t];
else
  UNDEFINED;
elsif PSTATE.EL == EL2 then
  UNDEFINED;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' && CP15SDISABLE2 == HIGH then
    UNDEFINED;
  else
    SDER = R[t];
SPSR, Saved Program Status Register

The SPSR characteristics are:

**Purpose**

Holds the saved process state for the current mode.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR are UNDEFINED.

**Attributes**

SPSR is a 32-bit register.

**Field descriptions**

The SPSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to the current mode, and copied to PSTATE.N on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to the current mode, and copied to PSTATE.Z on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to the current mode, and copied to PSTATE.C on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to the current mode, and copied to PSTATE.V on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to the current mode, and copied to PSTATE.Q on executing an exception return operation in the current mode.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to the current mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in the current mode.

On executing an exception return operation in the current mode SPSR.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**J, bit [24]**

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to the current mode, and copied to PSTATE.SSBS on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to the current mode, and copied to PSTATE.PAN on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**DIT, bit [21]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to the current mode, and copied to PSTATE.DIT on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.
IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to the current mode, and copied to PSTATE.IL on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to the current mode, and copied to PSTATE.GE on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to the current mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in the current mode.

SPSR.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to the current mode, and copied to PSTATE.E on executing an exception return operation in the current mode.

If the implementation does not support big-endian operation, SPSR.E is RES0. If the implementation does not support little-endian operation, SPSR.E is RES1. On executing an exception return operation in the current mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to the current mode, and copied to PSTATE.A on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to the current mode, and copied to PSTATE.I on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to the current mode, and copied to PSTATE.F on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to the current mode, and copied to PSTATE.T on executing an exception return operation in the current mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**M[4:0], bits [4:0]**

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to the current mode, and copied to PSTATE.M[4:0] on executing an exception return operation in the current mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10110</td>
<td>Monitor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in the current mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SPSR**

SPSR can be read using the MRS instruction and written using the MSR (register) or MSR (immediate) instructions.
**SPSR_abt, Saved Program Status Register (Abort mode)**

The SPSR_abt characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Abort mode.

**Configuration**

AArch32 System register SPSR_abt bits [31:0] are architecturally mapped to AArch64 System register SPSR_abt[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_abt are UNDEFINED.

**Attributes**

SPSR_abt is a 32-bit register.

**Field descriptions**

The SPSR_abt bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Abort mode, and copied to PSTATE.N on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Abort mode, and copied to PSTATE.Z on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Abort mode, and copied to PSTATE.C on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Abort mode, and copied to PSTATE.V on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]
Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Abort mode, and copied to PSTATE.Q on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]
If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Abort mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Abort mode.

On executing an exception return operation in Abort mode SPSR_abt.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

J, bit [24]
RES0.

In previous versions of the architecture, the {J, T} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]
When FEAT_SSBS is implemented:
Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Abort mode, and copied to PSTATE.SSBS on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

PAN, bit [22]
When FEAT_PAN is implemented:
Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Abort mode, and copied to PSTATE.PAN on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

DIT, bit [21]
When FEAT_DIT is implemented:
Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Abort mode, and copied to PSTATE.DIT on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Abort mode, and copied to PSTATE.IL on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Abort mode, and copied to PSTATE.GE on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Abort mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Abort mode.

SPSR_abt.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to Abort mode, and copied to PSTATE.E on executing an exception return operation in Abort mode.

If the implementation does not support big-endian operation, SPSR_abt.E is RES0. If the implementation does not support little-endian operation, SPSR_abt.E is RES1. On executing an exception return operation in Abort mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_abt.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_abt.E is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Abort mode, and copied to PSTATE.A on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Abort mode, and copied to PSTATE.I on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**F, bit [6]**

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Abort mode, and copied to PSTATE.F on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Abort mode, and copied to PSTATE.T on executing an exception return operation in Abort mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Abort mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Abort mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_abt.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Abort mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the SPSR_abt**

SPSR_abt is accessible in all modes other than User mode and Abort mode.

Accesses to this register use the following encodings:

**MRS{<c>}{<q>} <Rd>, SPSR_abt**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0100</td>
</tr>
</tbody>
</table>

**MSR{<c>}{<q>} SPSR_abt, <Rn>**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0100</td>
</tr>
</tbody>
</table>
SPSR_fiq, Saved Program Status Register (FIQ mode)

The SPSR_fiq characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to FIQ mode.

**Configuration**

AArch32 System register SPSR_fiq bits [31:0] are architecturally mapped to AArch64 System register SPSR_fiq[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_fiq are UNDEFINED.

**Attributes**

SPSR_fiq is a 32-bit register.

**Field descriptions**

The SPSR_fiq bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to FIQ mode, and copied to PSTATE.N on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to FIQ mode, and copied to PSTATE.Z on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to FIQ mode, and copied to PSTATE.C on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to FIQ mode, and copied to PSTATE.V on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to FIQ mode, and copied to PSTATE.Q on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to FIQ mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in FIQ mode.

On executing an exception return operation in FIQ mode SPSR_fiq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

J, bit [24]

RES0.

In previous versions of the architecture, the {J, T} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to FIQ mode, and copied to PSTATE.SSBS on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to FIQ mode, and copied to PSTATE.PAN on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

DIT, bit [21]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to FIQ mode, and copied to PSTATE.DIT on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to FIQ mode, and copied to PSTATE.IL on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to FIQ mode, and copied to PSTATE.GE on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to FIQ mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in FIQ mode.

SPSR_fiq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to FIQ mode, and copied to PSTATE.E on executing an exception return operation in FIQ mode.

If the implementation does not support big-endian operation, SPSR_fiq.E is RES0. If the implementation does not support little-endian operation, SPSR_fiq.E is RES1. On executing an exception return operation in FIQ mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_fiq.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_fiq.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to FIQ mode, and copied to PSTATE.A on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to FIQ mode, and copied to PSTATE.I on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to FIQ mode, and copied to PSTATE.F on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**T, bit [5]**

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to FIQ mode, and copied to PSTATE.T on executing an exception return operation in FIQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**M[4:0], bits [4:0]**

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to FIQ mode, and copied to PSTATE.M[4:0] on executing an exception return operation in FIQ mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_fiq.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in FIQ mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SPSR_fiq**

SPSR_fiq is accessible in all modes other than User mode and FIQ mode.

Accesses to this register use the following encodings:

\[
\text{MRS\{<c>\}{<q>} <Rd>, SPSR_fiq}
\]

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>0b1110</td>
</tr>
</tbody>
</table>

\[
\text{MSR\{<c>\}{<q>} SPSR_fiq, <Rn>}
\]

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>0b1110</td>
</tr>
</tbody>
</table>
SPSR_hyp, Saved Program Status Register (Hyp mode)

The SPSR_hyp characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Hyp mode.

**Configuration**

AArch32 System register SPSR_hyp bits [31:0] are architecturally mapped to AArch64 System register SPSR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_hyp are UNDEFINED.

**Attributes**

SPSR_hyp is a 32-bit register.

**Field descriptions**

The SPSR_hyp bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Hyp mode, and copied to PSTATE.N on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Hyp mode, and copied to PSTATE.Z on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Hyp mode, and copied to PSTATE.C on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Hyp mode, and copied to PSTATE.V on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Hyp mode, and copied to PSTATE.Q on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Hyp mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Hyp mode.

On executing an exception return operation in Hyp mode SPSR_hyp.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

J, bit [24]

RES0.

In previous versions of the architecture, the {J, T} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]

When FEAT_SSBS is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Hyp mode, and copied to PSTATE.SSBS on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Hyp mode, and copied to PSTATE.PAN on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

DIT, bit [21]

When FEAT_DIT is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Hyp mode, and copied to PSTATE.DIT on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Hyp mode, and copied to PSTATE.IL on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Hyp mode, and copied to PSTATE.GE on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Hyp mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Hyp mode.

SPSR_hyp.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to Hyp mode, and copied to PSTATE.E on executing an exception return operation in Hyp mode.

If the implementation does not support big-endian operation, SPSR_hyp.E is RES0. If the implementation does not support little-endian operation, SPSR_hyp.E is RES1. On executing an exception return operation in Hyp mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_hyp.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_hyp.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Hyp mode, and copied to PSTATE.A on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Hyp mode, and copied to PSTATE.I on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Hyp mode, and copied to PSTATE.F on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Hyp mode, and copied to PSTATE.T on executing an exception return operation in Hyp mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Hyp mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Hyp mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_hyp.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Hyp mode is an illegal return event, as described in ‘Illegal return events from AArch32 state’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_hyp

SPSR_hyp is accessible only in Monitor mode.

Accesses to this register use the following encodings:

\[
\text{MRS\{<c>\}{<q>}} <\text{Rd}>, \text{SPSR\_hyp}
\]

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b1110</td>
</tr>
</tbody>
</table>

\[
\text{MSR\{<c>\}{<q>}} \text{SPSR\_hyp}, <\text{Rn}>
\]

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b1110</td>
</tr>
</tbody>
</table>

30/09/2020 15:07; ccede0c90b0f99f9c0050268e820e80c0e7e17047211

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SPSR_irq, Saved Program Status Register (IRQ mode)

The SPSR_irq characteristics are:

### Purpose

Holds the saved process state when an exception is taken to IRQ mode.

### Configuration

AArch32 System register SPSR_irq bits [31:0] are architecturally mapped to AArch64 System register SPSR_irq[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_irq are UNDEFINED.

### Attributes

SPSR_irq is a 32-bit register.

### Field descriptions

The SPSR_irq bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Negative Condition flag. Set to the value of PSTATE.N on taking an exception to IRQ mode, and copied to PSTATE.N on executing an exception return operation in IRQ mode. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>30</td>
<td>Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to IRQ mode, and copied to PSTATE.Z on executing an exception return operation in IRQ mode. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>29</td>
<td>Carry Condition flag. Set to the value of PSTATE.C on taking an exception to IRQ mode, and copied to PSTATE.C on executing an exception return operation in IRQ mode. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>28</td>
<td>Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to IRQ mode, and copied to PSTATE.V on executing an exception return operation in IRQ mode. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
</tbody>
</table>
**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to IRQ mode, and copied to PSTATE.Q on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to IRQ mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in IRQ mode.

On executing an exception return operation in IRQ mode SPSR_irq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**J, bit [24]**

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state. Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

**SSBS, bit [23]**

When \texttt{FEAT\_SSBS} is implemented:

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to IRQ mode, and copied to PSTATE.SSBS on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**PAN, bit [22]**

When \texttt{FEAT\_PAN} is implemented:

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to IRQ mode, and copied to PSTATE.PAN on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**DIT, bit [21]**

When \texttt{FEAT\_DIT} is implemented:

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to IRQ mode, and copied to PSTATE.DIT on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to IRQ mode, and copied to PSTATE.IL on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to IRQ mode, and copied to PSTATE.GE on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to IRQ mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in IRQ mode.

SPSR_irq.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to IRQ mode, and copied to PSTATE.E on executing an exception return operation in IRQ mode.

If the implementation does not support big-endian operation, SPSR_irq.E is RES0. If the implementation does not support little-endian operation, SPSR_irq.E is RES1. On executing an exception return operation in IRQ mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_irq.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_irq.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to IRQ mode, and copied to PSTATE.A on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to IRQ mode, and copied to PSTATE.I on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to IRQ mode, and copied to PSTATE.F on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to IRQ mode, and copied to PSTATE.T on executing an exception return operation in IRQ mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to IRQ mode, and copied to PSTATE.M[4:0] on executing an exception return operation in IRQ mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_irq.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in IRQ mode is an illegal return event, as described in ‘Illegal return events from AArch32 state’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_irq

SPSR_irq is accessible in all modes other than User mode and IRQ mode.

Accesses to this register use the following encodings:

MRS{<c>}{<q>} <Rd>, SPSR_irq

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0000</td>
</tr>
</tbody>
</table>

MSR{<c>}{<q>} SPSR_irq, <Rn>

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
The SPSR_mon characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Monitor mode.

**Configuration**

AArch32 System register SPSR_mon bits [31:0] can be mapped to AArch64 System register `SPSR_EL3[31:0]`, but this is not architecturally mandated.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_mon are UNDEFINED.

**Attributes**

SPSR_mon is a 32-bit register.

**Field descriptions**

The SPSR_mon bit assignments are:

\[
\begin{array}{cccccccccccccccccccccccccccccccccc}
\end{array}
\]

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Monitor mode, and copied to PSTATE.N on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Monitor mode, and copied to PSTATE.Z on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Monitor mode, and copied to PSTATE.C on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Monitor mode, and copied to PSTATE.V on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]
Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Monitor mode, and copied to PSTATE.Q on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[1:0], bits [26:25]
If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Monitor mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Monitor mode.

On executing an exception return operation in Monitor mode SPSR_mon.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

J, bit [24]
RES0.

In previous versions of the architecture, the {J, T} bits determined the AArch32 Instruction set state.
Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

SSBS, bit [23]

When FEAT_SSBS is implemented:
Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Monitor mode, and copied to PSTATE.SSBS on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

PAN, bit [22]

When FEAT_PAN is implemented:
Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Monitor mode, and copied to PSTATE.PAN on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

DIT, bit [21]

When FEAT_DIT is implemented:
Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Monitor mode, and copied to PSTATE.DIT on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

**IL, bit [20]**

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Monitor mode, and copied to PSTATE.IL on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GE, bits [19:16]**

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Monitor mode, and copied to PSTATE.GE on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[7:2], bits [15:10]**

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Monitor mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Monitor mode.

SPSR_mon.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**E, bit [9]**

Endianness. Set to the value of PSTATE.E on taking an exception to Monitor mode, and copied to PSTATE.E on executing an exception return operation in Monitor mode.

If the implementation does not support big-endian operation, SPSR_mon.E is RES0. If the implementation does not support little-endian operation, SPSR_mon.E is RES1. On executing an exception return operation in Monitor mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_mon.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_mon.E is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**A, bit [8]**

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Monitor mode, and copied to PSTATE.A on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**I, bit [7]**

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Monitor mode, and copied to PSTATE.I on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**F, bit [6]**

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Monitor mode, and copied to PSTATE.F on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Monitor mode, and copied to PSTATE.T on executing an exception return operation in Monitor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Monitor mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Monitor mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10110</td>
<td>Monitor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11010</td>
<td>Hyp.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_mon.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Monitor mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SPSR_mon**

SPSR_mon is only accessible in EL3 modes other than Monitor mode.

Accesses to this register use the following encodings:

**MRS{<c>}{<q>} <Rd>, SPSR_mon**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b1100</td>
</tr>
</tbody>
</table>

**MSR{<c>}{<q>} SPSR_mon, <Rn>**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b1100</td>
</tr>
</tbody>
</table>
The SPSR_svc characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Supervisor mode.

**Configuration**

AArch32 System register SPSR_svc bits [31:0] are architecturally mapped to AArch64 System register SPSR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_svc are UNDEFINED.

**Attributes**

SPSR_svc is a 32-bit register.

**Field descriptions**

The SPSR_svc bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Supervisor mode, and copied to PSTATE.N on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Supervisor mode, and copied to PSTATE.Z on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Supervisor mode, and copied to PSTATE.C on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Supervisor mode, and copied to PSTATE.V on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Q, bit [27]**

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Supervisor mode, and copied to PSTATE.Q on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IT[1:0], bits [26:25]**

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Supervisor mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Supervisor mode.

On executing an exception return operation in Supervisor mode SPSR_svc.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**J, bit [24]**

RES0.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

**SSBS, bit [23]**

*When FEAT_SSBS is implemented:*

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Supervisor mode, and copied to PSTATE.SSBS on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**PAN, bit [22]**

*When FEAT_PAN is implemented:*

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Supervisor mode, and copied to PSTATE.PAN on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

*Otherwise:*

Reserved, RES0.

**DIT, bit [21]**

*When FEAT_DIT is implemented:*

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Supervisor mode, and copied to PSTATE.DIT on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
SPSR_svc, Saved Program Status Register (Supervisor mode)

Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Supervisor mode, and copied to PSTATE.IL on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Supervisor mode, and copied to PSTATE.GE on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Supervisor mode, and copied to PSTATE.IT[7:2] on executing an exception return operation in Supervisor mode.

SPSR_svc.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to Supervisor mode, and copied to PSTATE.E on executing an exception return operation in Supervisor mode.

If the implementation does not support big-endian operation, SPSR_svc.E is RES0. If the implementation does not support little-endian operation, SPSR_svc.E is RES1. On executing an exception return operation in Supervisor mode, if the implementation does not support big-endian operation at the Exception level being returned to, SPSR_svc.E is RES0, and if the implementation does not support little-endian operation at the Exception level being returned to, SPSR_svc.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Supervisor mode, and copied to PSTATE.A on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Supervisor mode, and copied to PSTATE.I on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Supervisor mode, and copied to PSTATE.F on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**T, bit [5]**

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Supervisor mode, and copied to PSTATE.T on executing an exception return operation in Supervisor mode.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**M[4:0], bits [4:0]**

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Supervisor mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Supervisor mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined</td>
</tr>
<tr>
<td>0b11111</td>
<td>System</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_svc.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Supervisor mode is an illegal return event, as described in 'Illegal return events from AArch32 state'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the SPSR_svc**

SPSR_svc is accessible in all modes other than User mode and Supervisor mode.

Accesses to this register use the following encodings:

**MRS{<c>}{<q>} <Rd>, SPSR_svc**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0010</td>
</tr>
</tbody>
</table>

**MSR{<c>}{<q>} SPSR_svc, <Rn>**

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0010</td>
</tr>
</tbody>
</table>
SPSR_und, Saved Program Status Register (Undefined mode)

The SPSR_und characteristics are:

**Purpose**

Holds the saved process state when an exception is taken to Undefined mode.

**Configuration**

AArch32 System register SPSR_und bits [31:0] are architecturally mapped to AArch64 System register SPSR_und[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to SPSR_und are UNDEFINED.

**Attributes**

SPSR_und is a 32-bit register.

**Field descriptions**

The SPSR_und bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**N, bit [31]**

Negative Condition flag. Set to the value of PSTATE.N on taking an exception to Undefined mode, and copied to PSTATE.N on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Z, bit [30]**

Zero Condition flag. Set to the value of PSTATE.Z on taking an exception to Undefined mode, and copied to PSTATE.Z on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**C, bit [29]**

Carry Condition flag. Set to the value of PSTATE.C on taking an exception to Undefined mode, and copied to PSTATE.C on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**V, bit [28]**

Overflow Condition flag. Set to the value of PSTATE.V on taking an exception to Undefined mode, and copied to PSTATE.V on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Q, bit [27]

Overflow or saturation flag. Set to the value of PSTATE.Q on taking an exception to Undefined mode, and copied to PSTATE.Q on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{IT}[1:0], bits [26:25]

If-Then. Set to the value of PSTATE.IT[1:0] on taking an exception to Undefined mode, and copied to PSTATE.IT[1:0] on executing an exception return operation in Undefined mode.

On executing an exception return operation in Undefined mode SPSR\textsubscript{und}.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

J, bit [24]

\texttt{RES0}.

In previous versions of the architecture, the \{J, T\} bits determined the AArch32 Instruction set state.

Armv8 does not support either Jazelle state or T32EE state, and the T bit determines the Instruction set state.

\textbf{SSBS, bit [23]}

\textbf{When FEAT\textsubscript{SSBS} is implemented:}

Speculative Store Bypass. Set to the value of PSTATE.SSBS on taking an exception to Undefined mode, and copied to PSTATE.SSBS on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{Otherwise:}

Reserved, \texttt{RES0}.

\textbf{PAN, bit [22]}

\textbf{When FEAT\textsubscript{PAN} is implemented:}

Privileged Access Never. Set to the value of PSTATE.PAN on taking an exception to Undefined mode, and copied to PSTATE.PAN on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\textbf{Otherwise:}

Reserved, \texttt{RES0}.

\textbf{DIT, bit [21]}

\textbf{When FEAT\textsubscript{DIT} is implemented:}

Data Independent Timing. Set to the value of PSTATE.DIT on taking an exception to Undefined mode, and copied to PSTATE.DIT on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.
Otherwise:

Reserved, RES0.

IL, bit [20]

Illegal Execution state. Set to the value of PSTATE.IL on taking an exception to Undefined mode, and copied to
PSTATE.IL on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

GE, bits [19:16]

Greater than or Equal flags. Set to the value of PSTATE.GE on taking an exception to Undefined mode, and copied to
PSTATE.GE on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IT[7:2], bits [15:10]

If-Then. Set to the value of PSTATE.IT[7:2] on taking an exception to Undefined mode, and copied to PSTATE.IT[7:2]
on executing an exception return operation in Undefined mode.

SPSR_und.IT must contain a value that is valid for the instruction being returned to.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

E, bit [9]

Endianness. Set to the value of PSTATE.E on taking an exception to Undefined mode, and copied to PSTATE.E on
executing an exception return operation in Undefined mode.

If the implementation does not support big-endian operation, SPSR_und.E is RES0. If the implementation does not
support little-endian operation, SPSR_und.E is RES1. On executing an exception return operation in Undefined mode, if
the implementation does not support big-endian operation at the Exception level being returned to, SPSR_und.E is
RES0, and if the implementation does not support little-endian operation at the Exception level being returned to,
SPSR_und.E is RES1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

A, bit [8]

SError interrupt mask. Set to the value of PSTATE.A on taking an exception to Undefined mode, and copied to PSTATE.A on
executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

I, bit [7]

IRQ interrupt mask. Set to the value of PSTATE.I on taking an exception to Undefined mode, and copied to PSTATE.I
on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

F, bit [6]

FIQ interrupt mask. Set to the value of PSTATE.F on taking an exception to Undefined mode, and copied to PSTATE.F
on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
T, bit [5]

T32 Instruction set state. Set to the value of PSTATE.T on taking an exception to Undefined mode, and copied to PSTATE.T on executing an exception return operation in Undefined mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

M[4:0], bits [4:0]

Mode. Set to the value of PSTATE.M[4:0] on taking an exception to Undefined mode, and copied to PSTATE.M[4:0] on executing an exception return operation in Undefined mode.

<table>
<thead>
<tr>
<th>M[4:0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10000</td>
<td>User.</td>
</tr>
<tr>
<td>0b10001</td>
<td>FIQ.</td>
</tr>
<tr>
<td>0b10010</td>
<td>IRQ.</td>
</tr>
<tr>
<td>0b10011</td>
<td>Supervisor.</td>
</tr>
<tr>
<td>0b10111</td>
<td>Abort.</td>
</tr>
<tr>
<td>0b11011</td>
<td>Undefined.</td>
</tr>
<tr>
<td>0b11111</td>
<td>System.</td>
</tr>
</tbody>
</table>

Other values are reserved. If SPSR_und.M[4:0] has a Reserved value, or a value for an unimplemented Exception level, executing an exception return operation in Undefined mode is an illegal return event, as described in ‘Illegal return events from AArch32 state’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the SPSR_und

SPSR_und is accessible in all modes other than User mode and Undefined mode.

Accesses to this register use the following encodings:

MRS{<c>}{<q>} <Rd>, SPSR_und

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0110</td>
</tr>
</tbody>
</table>

MSR{<c>}{<q>} SPSR_und, <Rn>

<table>
<thead>
<tr>
<th>R</th>
<th>M</th>
<th>M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>0b0110</td>
</tr>
</tbody>
</table>
**TCMTR, TCM Type Register**

The TCMTR characteristics are:

**Purpose**

Provides information about the implementation of the TCM.

**Configuration**

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TCMTR are UNDEFINED.

If EL1 or above can use AArch32 then this register must be implemented.

**Attributes**

TCMTR is a 32-bit register.

**Field descriptions**

The TCMTR bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED | bits [31:0] | IMPLEMENTATION DEFINED | |

**Accessing the TCMTR**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elif PSTATE.EL == EL1 then
  if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp; HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp; HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
elif EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp; HCR_EL2.TID1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
elif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp; HCR.TID1 == '1' then
    AArch32.TakeHypTrapException(0x03);
else
  return TCMTR;
elif PSTATE.EL == EL2 then
  return TCMTR;
elif PSTATE.EL == EL3 then
  return TCMTR;
TLBIALL, TLB Invalidate All

The TLBIALL characteristics are:

**Purpose**

Invalidates all cached copies of translation table entries from TLBs that are from any level of the translation table walk. The entries that are invalidated are as follows:

- If executed at EL1, all entries that:
  - Would be required for the EL1&0 translation regime.
  - Match the current VMID, if EL2 is implemented and enabled in the current Security state.
- If executed in Secure state when EL3 is using AArch32, all entries that would be required for the Secure PL1&0 translation regime.
- If executed at EL2, and if EL2 is enabled in the current Security state, the stage 1 or stage 2 translation table entries that would be required for the PL1&0 translation regime and matches the current VMID.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIALL are **UNDEFINED**.

**Attributes**

TLBIALL is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLBIALL instruction**

Accesses to this instruction use the following encodings:

\[ \text{MCR}\{<c>\}{<q>} \ <\text{coproc}>, \{#<opc1>\}, \ <\text{Rt}>, \ <\text{CRn}>, \ <\text{CRm}\{, \{#<opc2>\}\} \]

<table>
<thead>
<tr>
<th>proc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FB == '1' then
    TLBIALLIS();
  else
    TLBIALL();
elsif PSTATE.EL == EL2 then
  TLBIALL();
elseif PSTATE.EL == EL3 then
  TLBIALL();
The TLBIALLH characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for the Non-secure EL2 translation regime.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIALLH are UNDEFINED.

**Attributes**

TLBIALLH is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLBIALLH instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \ <\text{coproc}>\,\{\#<opc1>\},\ <Rt>,\ <CRn>,\ <CRm>\{\,\{\#<opc2>\}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elseif PSTATE.EL == EL2 then
    TLBIALLH();
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    else
        TLBIALLH();
    end

TLBIALLH, TLB Invalidate All, Hyp mode
The TLBIALLHIS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for the Non-secure EL2 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIALLHIS are UNDEFINED.

**Attributes**

TLBIALLHIS is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLBIALLHIS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \; \text{coproc}, \; \{#\}\text{opc1}, \; <Rt>, \; <CRn>, \; <CRm}\{, \; \{#\}\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBIALLHIS();
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    UNDEFINED;
  else
    TLBIALLHIS();
  endif
endif
The TLBIALLIS characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk. The entries that are invalidated are as follows:

- If executed at EL1, all entries that:
  - Would be required for the EL1&0 translation regime.
  - Match the current VMID, if EL2 is implemented and enabled in the current Security state.
- If executed in Secure state when EL3 is using AArch32, all entries that would be required for the Secure PL1&0 translation regime.
- If executed at EL2 and if EL2 is enabled in the current Security state, the stage 1 or stage 2 translation table entries that would be required for the PL1&0 translation regime and matches the current VMID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIALLIS are *UNDEFINED*.

**Attributes**

TLBIALLIS is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLBIALLIS instruction**

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \text{ <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>\}}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLBIS == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TTLBIS == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        TLBIALLIS();
    end if;
elsif PSTATE.EL == EL2 then
    TLBIALLIS();
elif PSTATE.EL == EL3 then
    TLBIALLIS();
TLB Invalid All, Non-Secure Non-Hyp

The TLB Invalid All, Non-Secure Non-Hyp characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for stage 1 or stage 2 of the Non-secure PL1&0 translation regime, regardless of the associated VMID.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLB Invalid All, Non-Secure Non-Hyp are UNDEFINED.

**Attributes**

TLB Invalid All, Non-Secure Non-Hyp is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLB Invalid All, Non-Secure Non-Hyp instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBIALLNSNH();
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    else
        TLBIALLNSNH();

TLBIALLNSNHIS, TLB Invalidate All, Non-Secure Non-Hyp, Inner Shareable

The TLBIALLNSNHIS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for stage 1 or stage 2 of the Non-secure PL1&0 translation regime, regardless of the associated VMID.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIALLNSNHIS are UNDEFINED.

**Attributes**

TLBIALLNSNHIS is a 32-bit System instruction.

**Field descriptions**

This instruction has no applicable fields.

The value in the register specified by <Rt> is ignored.

**Executing the TLBIALLNSNHIS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end if;
elsif PSTATE.EL == EL2 then
    TLBIALLNSNHIS();
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    else
        TLBIALLNSNHIS();
    end if;
TLBIASID, TLB Invalidate by ASID match

The TLBIASID characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIASID are UNDEFINED.

**Attributes**

TLBIASID is a 32-bit System instruction.

**Field descriptions**

The TLBIASID input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ASID |

**Bits [31:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries for non-global pages that match the ASID values will be affected by this System instruction.

**Executing the TLBIASID instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FB == '1' then
        TLBIASID(R[t]);
    else
        TLBIASID(R[t]);
    end
elsif PSTATE.EL == EL2 then
    TLBIASID(R[t]);
elsif PSTATE.EL == EL3 then
    TLBIASID(R[t]);
The TLBIASIDIS characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used for the specified ASID, and either:
  - Is from a level of lookup above the final level.
  - Is a non-global entry from the final level of lookup.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIASIDIS are **UNDEFINED**.

**Attributes**

TLBIASIDIS is a 32-bit System instruction.

**Field descriptions**

The TLBIASIDIS input value bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |   0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**RES0**

Reserved, **RES0**.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries for non-global pages that match the ASID values will be affected by this System instruction.

**Executing the TLBIASIDIS instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLBIS == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TTLBIS == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        TLBIASIDIS(R[t]);
    elsif PSTATE.EL == EL2 then
        TLBIASIDIS(R[t]);
    elsif PSTATE.EL == EL3 then
        TLBIASIDIS(R[t]);
The TLBIPAS2 characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- SCR.NS is 1.
- The entry would be used for the specified IPA.
- The entry would be used with the current VMID.
- The entry would be required for the PL1&0 translation regime.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIPAS2 are UNDEFINED.

---

**Note**

This System instruction is not implemented in architecture versions before Armv8.

---

**Attributes**

TLBIPAS2 is a 32-bit System instruction.

**Field descriptions**

The TLBIPAS2 input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
| IPA[39:12] |

**Bits [31:28]**

Reserved, RES0.

**IPA[39:12], bits [27:0]**

Bits[39:12] of the intermediate physical address to match.

**Executing the TLBIPAS2 instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:

- The instruction is **UNDEFINED**.
The instruction is treated as a NOP.
The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}<q>\{<\text{coproc}>\}, \{#\}<\text{opc1}>\{, \{#\}<\text{opc2}>\{, <Rt>, <CRn>, <CRm>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  TLBIIPAS2(R[t]);
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    UNDEFINED;
  elsif SCR.NS == '0' then
    //no operation
  else
    TLBIIPAS2(R[t]);
  endif
endif
TLBIIPAS2IS, TLB Invalidate by Intermediate Physical Address, Stage 2, Inner Shareable

The TLBIIPAS2IS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 2 only translation table entry, from any level of the translation table walk.
- **SCR**.NS is 1.
- The entry would be used for the specified IPA.
- The entry would be used with the current VMID.
- The entry would be required for the PL1&0 translation regime.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIIPAS2IS are **UNDEFINED**.

---

**Note**

This System instruction is not implemented in architecture versions before Armv8.

---

**Attributes**

TLBIIPAS2IS is a 32-bit System instruction.

**Field descriptions**

The TLBIIPAS2IS input value bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | IPA[39:12] |

**Bits [31:28]**

Reserved, RES0.

**IPA[39:12], bits [27:0]**

Bits[39:12] of the intermediate physical address to match.

**Executing the TLBIIPAS2IS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:
• The instruction is **UNDEFINED**.
• The instruction is treated as a **NOP**.
• The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{c\}\{q\}\ <\text{coproc}, \{#\}<\text{opc1}, \ <\text{Rt}, \ <\text{CRn}, \ <\text{CRm}\{, \{#\}<\text{opc2}\}}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    endif;
elsif PSTATE.EL == EL2 then
    TLBIIPAS2IS(R[t]);
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    elsif SCR.NS == '0' then
        //no operation
    else
        TLBIIPAS2IS(R[t]);
    endif;
endif;
```

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The TLBIPAS2L characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- \(SCR\).NS is 1.
- The entry would be used for the specified IPA.
- The entry would be used with the current VMID.
- The entry would be required for the PL1&0 translation regime.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIPAS2L are **UNDEFINED**.

**Note**

This System instruction is not implemented in architecture versions before Armv8.

**Attributes**

TLBIPAS2L is a 32-bit System instruction.

**Field descriptions**

The TLBIPAS2L input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>IPA[39:12]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**IPA[39:12], bits [27:0]**

Bits[39:12] of the intermediate physical address to match.

**Executing the TLBIPAS2L instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:

- The instruction is **UNDEFINED**.
• The instruction is treated as a NOP.
• The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>}\{<coproc>, \{#\}<opc1>, <Rt>, <CRn>, <CRm}\{, \{#\}<opc2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0100</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBIIPAS2L(R[t]);
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    UNDEFINED;
  elsif SCR.NS == '0' then
    //no operation
  else
    TLBIIPAS2L(R[t]);
The TLBIIPAS2LIS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 2 only translation table entry, from the final level of the translation table walk.
- SCR.NS is 1.
- The entry would be used for the specified IPA.
- The entry would be used with the current VMID.
- The entry would be required for the PL1&0 translation regime.

The invalidation is not required to apply to caching structures that combine stage 1 and stage 2 translation table entries.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIIPAS2LIS are **UNDEFINED**.

---

**Note**

This System instruction is not implemented in architecture versions before Armv8.

---

**Attributes**

TLBIIPAS2LIS is a 32-bit System instruction.

**Field descriptions**

The TLBIIPAS2LIS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>IPA[39:12]</td>
</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**IPA[39:12], bits [27:0]**

Bits[39:12] of the intermediate physical address to match.

**Executing the TLBIIPAS2LIS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:
• The instruction is UNDEFINED.
• The instruction is treated as a NOP.
• The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} \times \text{coproc}, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() \&\& !ELUsingAArch32(EL2) \&\& HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() \&\& ELUsingAArch32(EL2) \&\& HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
  endif
elsif PSTATE.EL == EL2 then
  TLBIIPAS2LIS(R[t]);
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    UNDEFINED;
  elsif SCR.NS == '0' then
    //no operation
  else
    TLBIIPAS2LIS(R[t]);
  endif
endif
The TLBIMVA characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVA are UNDEFINED.

**Attributes**

TLBIMVA is a 32-bit System instruction.

**Field descriptions**

The TLBIMVA input value bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | VA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   | RES0 |   |   |   |   |   |   |   | ASID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| VA |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
Executing the TLBIMVA instruction

Accesses to this instruction use the following encodings:

$$\text{MCR}\{<c>\}\{<q>\}\ <\text{coproc}, \ {#}<\text{opc1}}, \ <\text{Rt}, \ <\text{CRn}, \ <\text{CRm}\{, \ {#}<\text{opc2}\}}$$

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} == \text{EL0}\) then
  UNDEFINED;
elsif \(\text{PSTATE.EL} == \text{EL1}\) then
  if \(\text{EL2Enabled()} \&\& \neg\text{ELUsingAArch32(EL2)} \&\& \text{HSTR_EL2.T8} == '1'\) then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HSTR.T8} == '1'\) then
    AArch32.TakeHypTrapException(0x03);
  elsif \(\text{EL2Enabled()} \&\& \neg\text{ELUsingAArch32(EL2)} \&\& \text{HCR_EL2.TTLB} == '1'\) then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HCR.TTLB} == '1'\) then
    AArch32.TakeHypTrapException(0x03);
  elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HCR.FB} == '1'\) then
    TLBIMVAIS(R[t]);
  else
    TLBIMVA(R[t]);
  endif;
elsif \(\text{PSTATE.EL} == \text{EL2}\) then
  TLBIMVA(R[t]);
elsif \(\text{PSTATE.EL} == \text{EL3}\) then
  TLBIMVA(R[t]);
The TLBIMVAA characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified address.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAA are **UNDEFINED**.

**Attributes**

TLBIMVAA is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAA input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any unlocked TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVAA instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b0111</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FB == '1' then
        TLBIMVAIS(R[t]);
    else
        TLBIMVAA(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    TLBIMVAA(R[t]);
elsif PSTATE.EL == EL3 then
    TLBIMVAA(R[t]);
TLBIMVAAIS, TLB Invalidate by VA, All ASID, Inner Shareable

The TLBIMVAAIS characteristics are:

**Purpose**

invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry, from any level of the translation table walk.
- The entry would be used to translate the specified address.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAAIS are UNDEFINED.

**Attributes**

TLBIMVAAIS is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAAIS input value bit assignments are:

```
 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
   VA RES0
```

**VA, bits [31:12]**

Virtual address to match. Any unlocked TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVAAIS instruction**

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

| coproc | opc1 | CRn | CRm | opc2 |
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLBIS == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TTLBIS == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        TLBIMVAIS(R[t]);
    end if;
elsif PSTATE.EL == EL2 then
    TLBIMVAIS(R[t]);
elsif PSTATE.EL == EL3 then
    TLBIMVAIS(R[t]);
The TLBIMVAAL characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified address.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAAL are **UNDEFINED**.

**Note**

This System instruction is not implemented in architecture versions before Armv8.

**Attributes**

TLBIMVAAL is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAAL input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**VA**, bits [31:12]

Virtual address to match. Any unlocked TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVAAL instruction**

Accesses to this instruction use the following encodings:
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.FB == '1' then
    TLBIMVAALIS(R[t]);
else
  TLBIMVAAL(R[t]);
elsif PSTATE.EL == EL2 then
  TLBIMVAAL(R[t]);
elsif PSTATE.EL == EL3 then
  TLBIMVAAL(R[t]);
TLBIMVAALIS, TLB Invalidate by VA, All ASID, Last level, Inner Shareable

The TLBIMVAALIS characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry, from the final level of the translation table walk.
- The entry would be used to translate the specified address.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAALIS are **UNDEFINED**.

---

**Note**

This System instruction is not implemented in architecture versions before Armv8.

---

**Attributes**

TLBIMVAALIS is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAALIS input value bit assignments are:

```
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| VA  | RES0|
```

**VA, bits [31:12]**

Virtual address to match. Any unlocked TLB entries that match the VA will be affected by this System instruction, regardless of the ASID.

**Bits [11:0]**

Reserved, RES0.
Executing the TLBIMVAALIS instruction

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\}{, \{#\}<\text{opc2}>}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b111</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TTLBIS == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        TLBIMVAALIS(R[t]);
    endif
elsif PSTATE.EL == EL2 then
    TLBIMVAALIS(R[t]);
elsif PSTATE.EL == EL3 then
    TLBIMVAALIS(R[t]);
TLBIMVAH, TLB Invalidate by VA, Hyp mode

The TLBIMVAH characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for the Non-secure EL2 translation regime and used to translate the specified address.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAH are UNDEFINED.

**Attributes**

TLBIMVAH is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAH input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VA</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVAH instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is CONSTRAINED UNPREDICTABLE, and one of the following behaviors must occur:

- The instruction is UNDEFINED.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBIMVAH(R[t]);
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    else
        TLBIMVAH(R[t]);
TLBIMVAHIS, TLB Invalidate by VA, Hyp mode, Inner Shareable

The TLBIMVAHIS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from any level of the translation table walk that would be required for the Non-secure EL2 translation regime and used to translate the specified address.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAHIS are **UNDEFINED**.

**Attributes**

TLBIMVAHIS is a 32-bit System instruction.

**Field descriptions**

The TLBIMVAHIS input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VA | RES0 |

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVAHIS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:

- The instruction is **UNDEFINED**.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  TLBIMVAHIS(R[t]);
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    UNDEFINED;
  else
    TLBIMVAHIS(R[t]);
TLBIMVAIS, TLB Invalidate by VA, Inner Shareable

The TLBIMVAIS characteristics are:

Purpose

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is from a level of lookup above the final level and matches the specified ASID.
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

Configuration

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAIS are undefined.

Attributes

TLBIMVAIS is a 32-bit System instruction.

Field descriptions

The TLBIMVAIS input value bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| VA | RES0 | ASID |

VA, bits [31:12]

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Bits [11:8]

Reserved, RES0.

ASID, bits [7:0]

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
Executing the TLBIMVAIS instruction

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if \(\text{PSTATE.EL} == \text{EL0}\) then
  UNDEFINED;
elsif \(\text{PSTATE.EL} == \text{EL1}\) then
  if \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HSTR_EL2.T8} == '1'\) then
    \(\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)}\);
  elsif \(\text{EL2Enabled()} \&\& \text{ELUsingAArch32(EL2)} \&\& \text{HSTR.T8} == '1'\) then
    \(\text{AArch32.TakeHypTrapException(0x03)}\);
  elsif \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HCR_EL2.TTLB} == '1'\) then
    \(\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)}\);
  elsif \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HCR_EL2.TTLBIS} == '1'\) then
    \(\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)}\);
  elsif \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HCR.TTLB} == '1'\) then
    \(\text{AArch64.AArch32SystemAccessTrap(EL2, 0x03)}\);
  elsif \(\text{EL2Enabled()} \&\& \text{!ELUsingAArch32(EL2)} \&\& \text{HCR2.TTLBIS} == '1'\) then
    \(\text{AArch32.TakeHypTrapException(0x03)}\);
  else
    TLBIMVAIS(R[t]);
  endif
else
  TLBIMVAIS(R[t]);
endif

if \(\text{PSTATE.EL} == \text{EL2}\) then
  TLBIMVAIS(R[t]);
else
  TLBIMVAIS(R[t]);
endif

if \(\text{PSTATE.EL} == \text{EL3}\) then
  TLBIMVAIS(R[t]);
The TLBIMVAL characteristics are:

### Purpose

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation only applies to the PE that executes this System instruction.

### Configuration

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVAL are UNDEFINED.

This System instruction is not implemented in architecture versions before Armv8.

### Attributes

TLBIMVAL is a 32-bit System instruction.

### Field descriptions

The TLBIMVAL input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>RES0</td>
<td>ASID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.
Executing the TLBIMVAL instruction

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}\}\{, \{#\}<\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if \text{PSTATE.EL} == \text{EL0} then
    \text{UNDEFINED};
elsif \text{PSTATE.EL} == \text{EL1} then
    if \text{EL2Enabled()} && \neg \text{ELUsingAArch32(EL2)} && \text{HSTR\_EL2.T8} == '1' then
        \text{AArch64.\text{AArch32SystemAccessTrap}(EL2, 0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HSTR.T8} == '1' then
        \text{AArch32.\text{TakeHypTrapException}(0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HCR\_EL2.TTLB} == '1' then
        \text{AArch64.\text{AArch32SystemAccessTrap}(EL2, 0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HCR.TTLB} == '1' then
        \text{AArch32.\text{TakeHypTrapException}(0x03)};
    elsif \text{EL2Enabled()} && \text{ELUsingAArch32(EL2)} && \text{HCR.FB} == '1' then
        \text{TLBIMVALIS(R[t])};
    else
        \text{TLBIMVAL(R[t])};
    end if;
elsif \text{PSTATE.EL} == \text{EL2} then
    \text{TLBIMVAL(R[t])};
elsif \text{PSTATE.EL} == \text{EL3} then
    \text{TLBIMVAL(R[t])};
else
    \text{TLBIMVAL(R[t])};
end if;
TLBIMVALH, TLB Invalidate by VA, Last level, Hyp mode

The TLBIMVALH characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from the final level of the translation table walk that would be required for the Non-secure EL2 translation regime and used to translate the specified address.

The invalidation only applies to the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVALH are **UNDEFINED**.

This System instruction is not implemented in architecture versions before Armv8.

**Attributes**

TLBIMVALH is a 32-bit System instruction.

**Field descriptions**

The TLBIMVALH input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VA</td>
<td>VA, bits [31:12]</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
<td></td>
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<tr>
<td>27</td>
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<td>26</td>
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<td>25</td>
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<td>23</td>
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<td>20</td>
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<td>18</td>
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<td>4</td>
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<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>RES0</td>
<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVALH instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:

- The instruction is **UNDEFINED**.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1000</td>
<td>0b0111</td>
<td>0b101</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
else
    elsif PSTATE.EL == EL2 then
        TLBIMVALH(R[t]);
else
    elsif PSTATE.EL == EL3 then
        if !HaveEL(EL2) then
            UNDEFINED;
        else
            TLBIMVALH(R[t]);
The TLBIMVALHIS characteristics are:

**Purpose**

If EL2 is implemented, invalidate all cached copies of translation table entries from TLBs that are from the final level of the translation table walk that would be required for the Non-secure EL2 translation regime and used to translate the specified address.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVALHIS are **UNDEFINED**.

This System instruction is not implemented in architecture versions before Armv8.

**Attributes**

TLBIMVALHIS is a 32-bit System instruction.

**Field descriptions**

The TLBIMVALHIS input value bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>VA</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:0]**

Reserved, RES0.

**Executing the TLBIMVALHIS instruction**

If this instruction is executed in a Secure privileged mode other than Monitor mode, then the behavior is **CONSTRAINED UNPREDICTABLE**, and one of the following behaviors must occur:

- The instruction is **UNDEFINED**.
- The instruction is treated as a NOP.
- The instruction executes as if it had been executed in Monitor mode.

Accesses to this instruction use the following encodings:

\[
\text{MCR}\{<c>\}\{<q>\} \text{<coproc>}, \{#\}<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>\}
\]
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    TLBIMVALHIS(R[t]);
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        UNDEFINED;
    else
        TLBIMVALHIS(R[t]);

The TLBIMVALIS characteristics are:

**Purpose**

Invalidate all cached copies of translation table entries from TLBs that meet the following requirements:

- The entry is a stage 1 translation table entry.
- The entry would be used to translate the specified address, and one of the following applies:
  - The entry is a global entry from the final level of lookup.
  - The entry is a non-global entry from the final level of lookup that matches the specified ASID.
- If EL2 is implemented and enabled in the current Security state, the entry would be used with the current VMID.

From the entries that match these requirements, the entries that are invalidated are required for the following translation regime:

- If executed at Secure EL1 when EL3 is using AArch64, the Secure EL1&0 translation regime.
- If executed in Secure state when EL3 is using AArch32, the Secure PL1&0 translation regime.
- If executed in Non-secure state, the Non-secure PL1&0 translation regime.

The invalidation applies to all PEs in the same Inner Shareable shareability domain as the PE that executes this System instruction.

**Configuration**

This instruction is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBIMVALIS are **UNDEFINED**.

This System instruction is not implemented in architecture versions before Armv8.

**Attributes**

TLBIMVALIS is a 32-bit System instruction.

**Field descriptions**

The TLBIMVALIS input value bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>VA</td>
</tr>
<tr>
<td>30</td>
<td>29</td>
</tr>
<tr>
<td></td>
<td>ASID</td>
</tr>
</tbody>
</table>

**VA, bits [31:12]**

Virtual address to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.

**Bits [11:8]**

Reserved, RES0.

**ASID, bits [7:0]**

ASID value to match. Any TLB entries that match the ASID value and VA value will be affected by this System instruction.
Global TLB entries that match the VA value will be affected by this System instruction, regardless of the value of the ASID field.

### Executing the TLBIMVALID instruction

Accesses to this instruction use the following encodings:

```
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1000</td>
<td>0b0011</td>
<td>0b101</td>
</tr>
</tbody>
</table>

```c
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T8 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T8 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLB == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TTLBIS == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TTLB == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR2.TTLBIS == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        TLBIMVAL(R[t]);
    endif
else
    TLBIMVAL(R[t]);
endif
```

30/09/2020 15:07; ccead0cb9f089f9c3ee50268e829ee71047211

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TLBTR, TLB Type Register

The TLBTR characteristics are:

### Purpose

Provides information about the TLB implementation. The register must define whether the implementation provides separate instruction and data TLBs, or a unified TLB. Normally, the IMPLEMENTATION DEFINED information in this register includes the number of lockable entries in the TLB.

### Configuration

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TLBTR are UNDEFINED.

### Attributes

TLBTR is a 32-bit register.

### Field descriptions

The TLBTR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-1</td>
<td>IMPLEMENTATION DEFINED</td>
<td>nU</td>
</tr>
<tr>
<td>30-1</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>nU</td>
<td>Not Unified TLB. Indicates whether the implementation has a unified TLB:</td>
</tr>
<tr>
<td></td>
<td>0b0</td>
<td>Unified TLB.</td>
</tr>
<tr>
<td></td>
<td>0b1</td>
<td>Separate Instruction and Data TLBs.</td>
</tr>
</tbody>
</table>

### Accessing the TLBTR

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{,#}<opc2>
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TID1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TID1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    return TLBTR;
elsif PSTATE.EL == EL2 then
  return TLBTR;
elsif PSTATE.EL == EL3 then
  return TLBTR;
TPIDRPRW, PL1 Software Thread ID Register

The TPIDRPRW characteristics are:

**Purpose**

Provides a location where software executing at EL1 or higher can store thread identifying information that is not visible to software executing at EL0, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch32 System register TPIDRPRW bits [31:0] are architecturally mapped to AArch64 System register TPIDR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TPIDRPRW are UNDEFINED.

**Note**

The PE never updates this register.

**Attributes**

TPIDRPRW is a 32-bit register.

**Field descriptions**

The TPIDRPRW bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| Thread ID |

**Bits [31:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TPIDRPRW**

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\}, \{#\}<\text{opc1}\}, <\text{Rt}\}, <\text{CRn}\}, <\text{CRm}\}, \{#\}<\text{opc2}\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return TPIDRPRW_NS;
  else
    return TPIDRPRW;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return TPIDRPRW_NS;
  else
    return TPIDRPRW;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return TPIDRPRW_S;
  else
    return TPIDRPRW_NS;
else
  return TPIDRPRW;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b100</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    TPDPRW_NS = R[t];
  else
    TPDPRW = R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    TPDPRW_NS = R[t];
  else
    TPDPRW = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    TPDPRW_S = R[t];
  else
    TPDPRW_NS = R[t];
TPIDRURO, PL0 Read-Only Software Thread ID Register

The TPIDRURO characteristics are:

**Purpose**

Provides a location where software executing at EL1 or higher can store thread identifying information that is visible to software executing at EL0, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch32 System register TPIDRURO bits [31:0] are architecturally mapped to AArch64 System register TPIDRRO_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TPIDRURO are **UNDEFINED**.

**Note**

The PE never updates this register.

**Attributes**

TPIDRURO is a 32-bit register.

**Field descriptions**

The TPIDRURO bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| Thread ID |

**Bits [31:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the TPIDRURO**

Accesses to this register use the following encodings:

```
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL1) && HCR_EL2.<E2H,TGE> != '11' && (!HaveEL(EL3) ||
    SCR_EL3.FGTEn == '1') && HFGRTR_EL2.TPIDRURO_EL0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  else
    return TPIDRURO;
  end if
else
  if PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
      AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
      return TPIDRURO_NS;
    else
      return TPIDRURO;
    end if
  elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      return TPIDRURO_NS;
    else
      return TPIDRURO;
    end if
  elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
      return TPIDRURO_S;
    else
      return TPIDRURO_NS;
    end if
  end if
end if

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T13 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T13 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    TPIDRURO_NS = R[t];
  else
    TPIDRURO = R[t];
  end if
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    TPIDRURO_NS = R[t];
  else
    TPIDRURO = R[t];
  end if
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    TPIDRURO_S = R[t];
  else
    TPIDRURO_NS = R[t];
  end if
end if
TPIDRURW, PL0 Read/Write Software Thread ID Register

The TPIDRURW characteristics are:

**Purpose**

Provides a location where software executing at EL0 can store thread identifying information, for OS management purposes.

The PE makes no use of this register.

**Configuration**

AArch32 System register TPIDRURW bits [31:0] are architecturally mapped to AArch64 System register TPIDR_EL0[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TPIDRURW are UNDEFINED.

**Note**

The PE never updates this register.

**Attributes**

TPIDRURW is a 32-bit register.

**Field descriptions**

The TPIDRURW bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Thread ID</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Thread ID. Thread identifying information stored by software running at this Exception level.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the TPIDRURW**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.<E2H,TGE> != '1' &amp;&amp; HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp;&amp; HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() &amp; !ELUsingAArch32(EL1) &amp;&amp; HCR_EL2.<E2H,TGE> != '11' &amp;&amp; (!HaveEL(EL3) ||
        SCR_EL3.FGTEn == '1') &amp;&amp; HFGWTR_EL2.TPIDR_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        return TPIDURW;
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp;&amp; HSTR_EL2.T13 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp;&amp; HSTR.T13 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elseif HaveEL(EL3) &amp;&amp; ELUsingAArch32(EL3) then
            return TPIDURW_NS;
        else
            return TPIDURW;
        endif
    elseif PSTATE.EL == EL2 then
        if HaveEL(EL3) &amp;&amp; ELUsingAArch32(EL3) then
            return TPIDURW_NS;
        else
            return TPIDURW;
        endif
    elseif PSTATE.EL == EL3 then
        if SCR.NS == '0' then
            return TPIDURW_S;
        else
            return TPIDURW_NS;
        endif
    endif
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1101</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp;&amp; HCR_EL2.<E2H,TGE> != '1' &amp;&amp; HSTR_EL2.T13 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp;&amp; HSTR.T13 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() &amp; !ELUsingAArch32(EL1) &amp;&amp; HCR_EL2.<E2H,TGE> != '11' &amp;&amp; (!HaveEL(EL3) ||
        SCR_EL3.FGTEn == '1') &amp;&amp; HFGWTR_EL2.TPIDR_EL0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    else
        TPIDURW = R[t];
    endif
else
    if PSTATE.EL == EL1 then
        if EL2Enabled() &amp; !ELUsingAArch32(EL2) &amp;&amp; HSTR_EL2.T13 == '1' then
            AArch64.AArch32SystemAccessTrap(EL2, 0x03);
        elseif EL2Enabled() &amp; ELUsingAArch32(EL2) &amp;&amp; HSTR.T13 == '1' then
            AArch32.TakeHypTrapException(0x03);
        elseif HaveEL(EL3) &amp;&amp; ELUsingAArch32(EL3) then
            TPIDURW_NS = R[t];
        else
            TPIDURW = R[t];
        endif
    elseif PSTATE.EL == EL2 then
        if HaveEL(EL3) &amp;&amp; ELUsingAArch32(EL3) then
            TPIDURW_NS = R[t];
        else
            TPIDURW = R[t];
        endif
    elseif PSTATE.EL == EL3 then
        if SCR.NS == '0' then
            TPIDURW_S = R[t];
        else
            TPIDURW_NS = R[t];
        endif
The TRFCR characteristics are:

**Purpose**

Provides EL1 controls for Trace.

**Configuration**

AArch32 System register TRFCR bits [31:0] are architecturally mapped to AArch64 System register TRFCR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level and FEAT_TRF is implemented. Otherwise, direct accesses to TRFCR are UNDEFINED.

**Attributes**

TRFCR is a 32-bit register.

**Field descriptions**

The TRFCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit position</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-7</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>6-5</td>
<td>TS</td>
<td></td>
</tr>
<tr>
<td>4-3</td>
<td>E0TRE</td>
<td></td>
</tr>
<tr>
<td>2-0</td>
<td>E1TREOTRE</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:7]**

Reserved, RES0.

**TS, bits [6:5]**

Timestamp Control. Controls which timebase is used for trace timestamps.

<table>
<thead>
<tr>
<th>TS</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>Virtual timestamp. The traced timestamp is the physical counter value minus the value of CNTVOFF.</td>
<td>When FEAT_ECV is implemented</td>
</tr>
</tbody>
</table>
| 0b10| Guest physical timestamp. The traced timestamp is the physical counter value minus a physical offset. If any of the following are true, the physical offset is zero, otherwise the physical offset is the value of CNTPOFF_EL2.  
  - EL3 is implemented and using AArch32.  
  - EL3 is implemented, using AArch64, and SCR_EL3.ECVEn == 0b0.  
  - EL2 is using AArch32.  
  - EL2 is using AArch64 and CNTCTL_EL2.ECV == 0b0. | |
| 0b11| Physical timestamp. The traced timestamp is the physical counter value. |             |

All other values are reserved.

This field is ignored by the PE when any of the following are true:

- EL2 is implemented and HTRFCR.TS != 0b0.
• SelfHostedTraceEnabled() == FALSE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [4:2]**

Reserved, RES0.

**E1TRE, bit [1]**

EL1 Trace Enable.

<table>
<thead>
<tr>
<th>E1TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tracing is prohibited in PL1 modes.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tracing is allowed in PL1 modes.</td>
</tr>
</tbody>
</table>

This field is ignored if SelfHostedTraceEnabled() == FALSE.

On a Warm reset, this field resets to 0.

**E0TRE, bit [0]**

EL0 Trace Enable.

<table>
<thead>
<tr>
<th>E0TRE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Tracing is prohibited at EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Tracing is allowed at EL0.</td>
</tr>
</tbody>
</table>

This field is ignored if any of the following are true:

• SelfHostedTraceEnabled() == FALSE.
• EL2 is implemented and enabled in the current security state and HCR.TGE == 1.

On a Warm reset, this field resets to 0.

**Accessing the TRFCR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
    UNDEFINED;
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && MDCR_EL2.TTRF == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TTRF == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    return TRFCR;
  endif
elsif PSTATE.EL == EL2 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
    UNDEFINED;
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    endif
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch32.TakeMonitorTrapException();
    endif
  else
    return TRFCR;
  endif
elsif PSTATE.EL == EL3 then
  if PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
    AArch32.TakeMonitorTrapException();
  else
    return TRFCR;
  endif

MCR{coproc}{opc1}{CRn}{CRm}{opc2}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0001</td>
<td>0b0010</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    UNDEFINED;
  elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
    UNDEFINED;
  elif EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T1 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T1 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && MDCR_EL2.TTRF == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HDCR.TTRF == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
    if Halted() && EDSCR.SDD == '1' then
      UNDEFINED;
    else
      AArch64.AArch32SystemAccessTrap(EL3, 0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) && PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
      if Halted() && EDSCR.SDD == '1' then
        UNDEFINED;
      else
        AArch32.TakeMonitorTrapException();
      else
        TRFCR = R[t];
    elsif PSTATE.EL == EL2 then
      if Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
        UNDEFINED;
      elsif Halted() && HaveEL(EL3) && EDSCR.SDD == '1' && boolean IMPLEMENTATION_DEFINED "EL3 trap priority when SDD == '1'" && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
        UNDEFINED;
      elsif HaveEL(EL3) && !ELUsingAArch32(EL3) && MDCR_EL3.TTRF == '1' then
        if Halted() && EDSCR.SDD == '1' then
          UNDEFINED;
        else
          AArch64.AArch32SystemAccessTrap(EL3, 0x03);
        elsif HaveEL(EL3) && ELUsingAArch32(EL3) && SDCR.TTRF == '1' then
          if Halted() && EDSCR.SDD == '1' then
            UNDEFINED;
          else
            AArch32.TakeMonitorTrapException();
          else
            TRFCR = R[t];
      elsif PSTATE.EL == EL3 then
        if PSTATE.M != M32_Monitor && SDCR.TTRF == '1' then
          AArch32.TakeMonitorTrapException();
        else
          TRFCR = R[t];

TTBCR, Translation Table Base Control Register

The TTBCR characteristics are:

**Purpose**

The control register for stage 1 of the PL1&0 translation regime. Its controls include:

- Where the VA range is split between addresses translated using TTBR0 and addresses translated using TTBR1.
- The translation table format used by this stage of translation.

From Armv8.2, when the value of TTBCR.{EAE, T2E} is {1, 1}, TTBCR is used with TTBCR2.

**Configuration**

AArch32 System register TTBCR bits [31:0] are architecturally mapped to AArch64 System register TCR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TTBCR are UNDEFINED.

The current translation table format determines which format of the register is used.

Some RW fields of this register have defined reset values. These apply only if the PE resets into an Exception level that is using AArch32. If the PE resets into EL3 using AArch32 then:

- The EAE bit resets to 0 in both the Secure and the Non-secure instances of the register.
- Other reset values apply only to the Secure instance of the register.

**Attributes**

TTBCR is a 32-bit register.

**Field descriptions**

The TTBCR bit assignments are:

**When TTBCR.EAE == 0:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EAE | RES0 | PD1 | PD0 | RES0 | N |

**EAE, bit [31]**

Extended Address Enable.

<table>
<thead>
<tr>
<th>EAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Use the VMSAv8-32 translation system with the Short-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Bits [30:6]**

Reserved, RES0.
**PD1, bit [5]**

Translation table walk disable for translations using TTBR1. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR1.

<table>
<thead>
<tr>
<th>PD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBR1.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBR1 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**PD0, bit [4]**

Translation table walk disable for translations using TTBR0. This bit controls whether a translation table walk is performed on a TLB miss for an address that is translated using TTBR0.

<table>
<thead>
<tr>
<th>PD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBR0.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBR0 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Bit [3]**

Reserved, RES0.

**N, bits [2:0]**

Indicate the width of the base address held in TTBR0. In TTBR0, the base address field is bits[31:14-N]. The value of N also determines:

- Whether TTBR0 or TTBR1 is used as the base address for translation table walks.
- The size of the translation table pointed to by TTBR0.

N can take any value from 0 to 7, that is, from 0b000 to 0b111.

When N has its reset value of 0, the translation table base is compatible with Armv5 and Armv6.

On a Warm reset, this field resets to 0.

**When TTBCR.EAE == 1:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| EAE | IMPLEMENTATION DEFINED | SH1 | ORGN1 | RGN1 | EPD1 | A1 | RES0 | T1S | RES0 | SH0 | ORGN0 | RGN0 | EPD0 | T2E | RES0 | T0SZ |

**EAE, bit [31]**

Extended Address Enable.

<table>
<thead>
<tr>
<th>EAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Use the VMSAv8-32 translation system with the Long-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**IMPLEMENTATION DEFINED, bit [30]**

IMPLEMENTATION DEFINED.
On a Warm reset, this field resets to 0.

**SH1, bits [29:28]**

Shareability attribute for memory associated with translation table walks using TTBR1.

<table>
<thead>
<tr>
<th>SH1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to 0.

**ORGN1, bits [27:26]**

Outer cacheability attribute for memory associated with translation table walks using TTBR1.

<table>
<thead>
<tr>
<th>ORGN1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**IRGN1, bits [25:24]**

Inner cacheability attribute for memory associated with translation table walks using TTBR1.

<table>
<thead>
<tr>
<th>IRGN1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**EPD1, bit [23]**

Translation table walk disable for translations using TTBR1. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR1.

<table>
<thead>
<tr>
<th>EPD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBR1.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBR1 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**A1, bit [22]**

Selects whether TTBR0 or TTBR1 defines the ASID.
Meaning

| A1 | TTBR0.ASID defines the ASID. |
| A0 | TTBR1.ASID defines the ASID. |

On a Warm reset, this field resets to 0.

### Bits [21:19]

Reserved, RES0.

### T1SZ, bits [18:16]

See 'Selecting between TTBR0 and TTBR1, VMSAv8-32 Long-descriptor translation table format' for how TTBCR.{T1SZ, T0SZ} determine the input address ranges and memory region sizes translated using TTBR0 and TTBR1.

On a Warm reset, this field resets to 0.

### Bits [15:14]

Reserved, RES0.

### SH0, bits [13:12]

Shareability attribute for memory associated with translation table walks using TTBR0.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Non-shareable</td>
</tr>
<tr>
<td>01</td>
<td>Outer Shareable</td>
</tr>
<tr>
<td>11</td>
<td>Inner Shareable</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to 0.

### ORGN0, bits [11:10]

Outer cacheability attribute for memory associated with translation table walks using TTBR0.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

### IRGN0, bits [9:8]

Inner cacheability attribute for memory associated with translation table walks using TTBR0.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to 0.

**EPD0, bit [7]**

Translation table walk disable for translations using TTBR0. This bit controls whether a translation table walk is performed on a TLB miss, for an address that is translated using TTBR0.

<table>
<thead>
<tr>
<th>EPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Perform translation table walks using TTBR0.</td>
</tr>
<tr>
<td>0b1</td>
<td>A TLB miss on an address that is translated using TTBR0 generates a Translation fault. No translation table walk is performed.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**T2E, bit [6]**

When FEAT_AA32HPD is implemented:

TTBCR2 Enable.

<table>
<thead>
<tr>
<th>T2E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>TTBCR2 is disabled. The contents of TTBCR2 are treated as 0 for all purposes other than reading or writing the register.</td>
</tr>
<tr>
<td>0b1</td>
<td>TTBCR2 is enabled.</td>
</tr>
</tbody>
</table>

If TTBCR.EAE==0, then the behavior is as if the bit is 0.

Otherwise:

Reserved, RES0.

**Bits [5:3]**

Reserved, RES0.

**T0SZ, bits [2:0]**

See 'Selecting between TTBR0 and TTBR1, VMSAv8-32 Long-descriptor translation table format' for how TTBCR.{T1SZ, T0SZ} determine the input address ranges and memory region sizes translated using TTBR0 and TTBR1.

On a Warm reset, this field resets to 0.

**Accessing the TTBCR**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
      return TTBCR_NS;
   else
      return TTBCR;
   end
elsif PSTATE.EL == EL2 then
   if EL2Enabled() && ELUsingAArch32(EL3) then
      return TTBCR_NS;
   else
      return TTBCR;
   end
elsif PSTATE.EL == EL3 then
   if SCR.NS == '0' then
      return TTBCR_S;
   else
      return TTBCR_NS;
end

MCR{<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
   UNDEFINED;
elsif PSTATE.EL == EL1 then
   if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
      AArch64.AArch32SystemAccessTrap(EL2, 0x03);
   elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
      AArch32.TakeHypTrapException(0x03);
   elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
      TTBCR_NS = R[t];
   else
      TTBCR = R[t];
   end
elsif PSTATE.EL == EL2 then
   if EL2Enabled() && ELUsingAArch32(EL3) then
      TTBCR_NS = R[t];
   else
      TTBCR = R[t];
   end
elsif PSTATE.EL == EL3 then
   if SCR.NS == '0' && CP15SDISABLE == HIGH then
      UNDEFINED;
   elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
      UNDEFINED;
   else
      if SCR.NS == '0' then
         TTBCR_S = R[t];
      else
         TTBCR_NS = R[t];
      end
   end
end
TTBCR2, Translation Table Base Control Register 2

The TTBCR2 characteristics are:

**Purpose**

The second control register for stage 1 of the PL1&0 translation regime.

If FEAT_AA32HPD is not implemented then this register is not implemented and its encoding is **UNDEFINED**. Otherwise:

- When the value of TTBCR.EAE, T2E is not \{1, 1\} the contents of TTBCR2 are treated as zero for all purposes other than reading or writing the register.
- When the value of TTBCR.EAE, T2E is \{1, 1\} TTBCR2 is used with TTBCR.

**Configuration**

AArch32 System register TTBCR2 bits \[31:0\] are architecturally mapped to AArch64 System register TCR_EL1[63:32].

This register is present only when AArch32 is supported at any Exception level and FEAT_AA32HPD is implemented. Otherwise, direct accesses to TTBCR2 are **UNDEFINED**.

**Attributes**

TTBCR2 is a 32-bit register.

**Field descriptions**

The TTBCR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | HWU162 | HWU161 | HWU160 | HWU159 | HWU062 | HWU061 | HWU060 | HWU059 | HPD1 | HPD0 | RES0 |

**Bits [31:19]**

Reserved, RES0.

**HWU162, bit [18]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using TTBR1.

<table>
<thead>
<tr>
<th>HWU162</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD1 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.
Otherwise:

Reserved, RES0.

**HWU161, bit [17]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using TTBR1.

<table>
<thead>
<tr>
<th>HWU161</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1, bit[61] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1, bit[61] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD1 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU160, bit [16]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using TTBR1.

<table>
<thead>
<tr>
<th>HWU160</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD1 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**HWU159, bit [15]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using TTBR1.
The Effective value of this field is 0 if the value of TTBCR2.HPD1 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU062, bit [14]

When FEAT_HPD52 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 1 translation table Block or Page entry for translations using TTBR0.

<table>
<thead>
<tr>
<th>HWU062</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR1, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR1, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD1 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD1 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU061, bit [13]

When FEAT_HPD52 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 1 translation table Block or Page entry for translations using TTBR0.

<table>
<thead>
<tr>
<th>HWU061</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0, bit[62] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0, bit[62] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD0 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.
HWU060, bit [12]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 1 translation table Block or Page entry for translations using TTBR0.

<table>
<thead>
<tr>
<th>HWU060</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0, bit[60] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0, bit[60] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD0 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HWU059, bit [11]

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 1 translation table Block or Page entry for translations using TTBR0.

<table>
<thead>
<tr>
<th>HWU059</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>For translations using TTBR0, bit[59] of each stage 1 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>For translations using TTBR0, bit[59] of each stage 1 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose if the value of TTBCR2.HPD0 is 1.</td>
</tr>
</tbody>
</table>

The Effective value of this field is 0 if the value of TTBCR2.HPD0 is 0 or the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HPD1, bit [10]

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, XNTable, and PXNTable, in the translation tables pointed to by TTBR1.

<table>
<thead>
<tr>
<th>HPD1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled if TTBCR.T2E == 1.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are 0.

The Effective value of this field is 0 if the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**HPD0, bit [9]**

Hierarchical Permission Disables. This affects the hierarchical control bits, APTable, XNTable, and PXNTable, in the translation tables pointed to by TTBR0.

<table>
<thead>
<tr>
<th>HPD0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Hierarchical permissions are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Hierarchical permissions are disabled if TTBCR.T2E == 1.</td>
</tr>
</tbody>
</table>

When disabled, the permissions are treated as if the bits are 0.

The Effective value of this field is 0 if the value of TTBCR.T2E is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [8:0]**

Reserved, RES0.

**Accessing the TTBCR2**

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TRVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TRVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBCR2_NS;
else
    return TTBCR2;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBCR2_NS;
else
    return TTBCR2;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return TTBCR2_S;
else
    return TTBCR2_NS;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
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<tbody>
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<td>0b0010</td>
<td>0b0000</td>
<td>0b011</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        TTBCR2_NS = R[t];
    else
        TTBCR2 = R[t];
    elsif PSTATE.EL == EL2 then
        if HaveEL(EL3) && ELUsingAArch32(EL3) then
            TTBCR2_NS = R[t];
        else
            TTBCR2 = R[t];
    elsif PSTATE.EL == EL3 then
        if SCR.NS == '0' && CP15DISABLE == HIGH then
            UNDEFINED;
        elsif SCR.NS == '0' && CP15DISABLE2 == HIGH then
            UNDEFINED;
        else
            if SCR.NS == '0' then
                TTBCR2.S = R[t];
            else
                TTBCR2_NS = R[t];
            end if
        end if
    end if
else
    TTBCR2 = R[t];
end if
TTBR0, Translation Table Base Register 0

The TTBR0 characteristics are:

Purpose

Holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the lower VA range in the PL1&0 translation regime, and other information for this translation regime.

Configuration

AArch32 System register TTBR0 bits [63:0] are architecturally mapped to AArch64 System register TTBR0_EL1[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TTBR0 are UNDEFINED.

TTBR0 is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, accesses read and write bits [31:0] and do not modify bits [63:32].

TTBCR.EAE determines which TTBR0 format is used:

- TTBCR.EAE == 0b0: 32-bit format is used. TTBR0[63:32] are ignored.
- TTBCR.EAE == 0b1: 64-bit format is used.

When EL3 is using AArch32, write access to TTBR0(S) is disabled when the CP15SDISABLE signal is asserted HIGH.

Used in conjunction with the TTBCR. When the 64-bit TTBR0 format is used, cacheability and shareability information is held in the TTBCR, not in TTBR0.

Attributes

TTBR0 is a 64-bit register.

Field descriptions

The TTBR0 bit assignments are:

When TTBCR.EAE == 0:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TTB0 | [RGN[0]] | NOS | [RGN] | IMP | S | [RGN[1]] |

Bits [63:32]

Reserved, RES0.

TTB0, bits [31:7]

Translation table base address, bits[31:x], where x is 14-(TTBCR.N). Register bits [x-1:7] are RES0, with the additional requirement that if these bits are not all zero, this is a misaligned translation table base address, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Register bits [x-1:7] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IRGN, bits [0, 6]**

Inner region bits. Bits [0,6] of this register together indicate the Inner Cacheability attributes for the memory associated with the translation table walks. The possible values of IRGN[1:0] are:

<table>
<thead>
<tr>
<th>IRGN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back no Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

**Note**

The encoding of the IRGN bits is counter-intuitive, with register bit[6] being IRGN[0] and register bit[0] being IRGN[1]. This encoding is chosen to give a consistent encoding of memory region types and to ensure that software written for ARMv7 without the Multiprocessing Extensions can run unmodified on an implementation that includes the functionality introduced by the ARMv7 Multiprocessing Extensions.

The IRGN field is split as follows:

- IRGN[0] is TTBR0[6].
- IRGN[1] is TTBR0[0].

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NOS, bit [5]**

Not Outer Shareable. When the value of TTBR0.S is 1, indicates whether the memory associated with a translation table walk is Inner Shareable or Outer Shareable:

<table>
<thead>
<tr>
<th>NOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Memory is Outer Shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory is Inner Shareable.</td>
</tr>
</tbody>
</table>

This bit is ignored when the value of TTBR0.S is 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**RGN, bits [4:3]**

Region bits. Indicates the Outer cacheability attributes for the memory associated with the translation table walks:

<table>
<thead>
<tr>
<th>RGN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back no Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**IMP, bit [2]**

The effect of this bit is **IMPLEMENTATION DEFINED**. If the translation table implementation does not include any **IMPLEMENTATION DEFINED** features this bit is **RES0**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**S, bit [1]**

Shareable. Indicates whether the memory associated with the translation table walks is Non-shareable:
Meaning
---
0b0  Memory is Non-shareable.
0b1  Memory is shareable. The TTBR0.NOS field indicates whether the memory is Inner Shareable or Outer Shareable.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

**When TTBCR.EAE == 1:**

<table>
<thead>
<tr>
<th>Bits [63:56]</th>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0.</td>
<td></td>
</tr>
</tbody>
</table>

**ASID, bits [55:48]**

An ASID for the translation table base address. The TTBCR.A1 field selects either TTBR0.ASID or TTBR1.ASID.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

**BADDR, bits [47:1]**

Translation table base address, bits[47:x], Bits [x-1:1] are RES0, with the additional requirement that if bits[x-1:3] are not all zero, this is a misaligned translation table base address, with effects that are `CONSTRAINED UNPREDICTABLE`, and must be one of the following:

- Register bits [x-1:3] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

x is determined from the value of TTBCR.T0SZ as follows:

- If TTBCR.T0SZ is 0 or 1, x = 5 - TTBCR.T0SZ.
- If TTBCR.T0SZ is greater than 1, x = 14 - TTBCR.T0SZ.

If bits[47:40] of the translation table base address are not zero, an Address size fault is generated.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

**CnP, bit [0]**

**When FEAT_TTCNP is implemented:**

Common not Private. When TTBCR.EAE == 1, this bit indicates whether each entry that is pointed to by TTBR0 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR0.CnP is 1.
The translation table entries pointed to by this instance of TTBR0, for the current ASID, are permitted to differ from corresponding entries for this instance of TTBR0 for other PEs in the Inner Shareable domain. This is not affected by:

- The value of TTBR0.CnP on those other PEs.
- The value of TTBCR.EAE on those other PEs.
- The value of the current ASID or, for the Non-secure instance of TTBR0, the value of the current VMID.

The translation table entries pointed to by this instance of TTBR0 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR0.CnP is 1 for this instance of TTBR0 and all of the following apply:

- The translation table entries are pointed to by this instance of TTBR0.
- The value of the applicable TTBCR.EAE field is 1.
- The ASID is the same as the current ASID.
- For the Non-secure instance of TTBR0, the VMID is the same as the current VMID.

When a TLB combines entries from stage 1 translation and stage 2 translation into a single entry, that entry can only be shared between different PEs if the value of the CnP bit is 1 for both stage 1 and stage 2.

Note

If the value of the TTBR0.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR0s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are **CONstrained UNPREDICTable**, see 'CONstrained UNPREDICTable behaviors due to caching of control or data values'.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

### Accessing the TTBR0

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}{<q>} <\text{coproc}>, \{#<\text{opc1}>\}, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#<\text{opc2}>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBR0_NS<31:0>;
    else
        return TTBR0<31:0>;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBR0_NS<31:0>;
    else
        return TTBR0<31:0>;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return TTBR0_S<31:0>;
    else
        return TTBR0_NS<31:0>;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        TTBR0_NS = ZeroExtend(R[t]);
    else
        TTBR0 = ZeroExtend(R[t]);
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        TTBR0_NS = ZeroExtend(R[t]);
    else
        TTBR0 = ZeroExtend(R[t]);
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            TTBR0_S = ZeroExtend(R[t]);
        else
            TTBR0_NS = ZeroExtend(R[t]);

MRRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b0010</td>
<td>0b0000</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return TTBR0_NS;
  else
    return TTBR0;
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    return TTBR0_NS;
  else
    return TTBR0;
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    return TTBR0_S;
  else
    return TTBR0_NS;

MCRR{<c>}{<q>} coproc, {#}<opc1>, <Rt>, <Rt2>, <CRm>

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
<tr>
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</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    TTBR0_NS = R[t2]:R[t];
  else
    TTBR0 = R[t2]:R[t];
elsif PSTATE.EL == EL2 then
  if HaveEL(EL3) && ELUsingAArch32(EL3) then
    TTBR0_NS = R[t2]:R[t];
  else
    TTBR0 = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' && CP15SDISABLE == HIGH then
    UNDEFINED;
  else
    if SCR.NS == '0' then
      TTBR0_S = R[t2]:R[t];
    else
      TTBR0_NS = R[t2]:R[t];
TTBR1, Translation Table Base Register 1

The TTBR1 characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 1 of the translation of an address from the higher VA range in the PL1&0 translation regime, and other information for this translation regime.

**Configuration**

AArch32 System register TTBR1 bits [63:0] are architecturally mapped to AArch64 System register TTBR1_EL1[63:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to TTBR1 are UNDEFINED.

TTBR1 is a 64-bit register that can also be accessed as a 32-bit value. If it is accessed as a 32-bit register, accesses read and write bits [31:0] and do not modify bits [63:32].

**TTBCR** EAE determines which TTBR1 format is used:

- **TTBCR** EAE == 0b0: 32-bit format is used. TTBR1[63:32] are ignored.
- **TTBCR** EAE == 0b1: 64-bit format is used.

Used in conjunction with the **TTBCR**. When the 64-bit TTBR1 format is used, cacheability and shareability information is held in the TTBCR, not in TTBR1.

**Attributes**

TTBR1 is a 64-bit register.

**Field descriptions**

The TTBR1 bit assignments are:

**When TTBCR.EAE == 0:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
</tr>
<tr>
<td>62</td>
<td></td>
</tr>
<tr>
<td>61</td>
<td>TTB1</td>
</tr>
<tr>
<td>60</td>
<td></td>
</tr>
<tr>
<td>59</td>
<td></td>
</tr>
<tr>
<td>58</td>
<td></td>
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<td>57</td>
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<td>56</td>
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<td>55</td>
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<td>54</td>
<td></td>
</tr>
<tr>
<td>53</td>
<td></td>
</tr>
<tr>
<td>52</td>
<td></td>
</tr>
<tr>
<td>51</td>
<td>TGN[1]</td>
</tr>
<tr>
<td>50</td>
<td>NOS</td>
</tr>
<tr>
<td>49</td>
<td>RGN</td>
</tr>
<tr>
<td>48</td>
<td>IMP</td>
</tr>
<tr>
<td>47</td>
<td>S</td>
</tr>
<tr>
<td>46</td>
<td>IRGN[0]</td>
</tr>
<tr>
<td>45</td>
<td></td>
</tr>
<tr>
<td>44</td>
<td></td>
</tr>
<tr>
<td>43</td>
<td></td>
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<tr>
<td>42</td>
<td></td>
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<td>35</td>
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<tr>
<td>34</td>
<td></td>
</tr>
<tr>
<td>33</td>
<td></td>
</tr>
<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**TTB1, bits [31:7]**

Translation table base address, bits[31:14]. Register bits [13:7] are RES0, with the additional requirement that if these bits are not all zero, this is a misaligned translation table base address, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Register bits [13:7] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
IRGN, bits [6, 0]

Inner region bits. IRGN[1:0] indicate the Inner Cacheability attributes for the memory associated with the translation table walks. The possible values of IRGN[1:0] are:

<table>
<thead>
<tr>
<th>IRGN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>01</td>
<td>Normal memory, Inner Write-Back Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>10</td>
<td>Normal memory, Inner Write-Through Cacheable.</td>
</tr>
<tr>
<td>11</td>
<td>Normal memory, Inner Write-Back no Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

Note

The encoding of the IRGN bits is counter-intuitive, with register bit[6] being IRGN[0] and register bit[0] being IRGN[1]. This encoding is chosen to give a consistent encoding of memory region types and to ensure that software written for Armv7 without the Multiprocessing Extensions can run unmodified on an implementation that includes the functionality introduced by the ARMv7 Multiprocessing Extensions.

The IRGN field is split as follows:

- IRGN[1] is TTBR1[6].
- IRGN[0] is TTBR1[0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

NOS, bit [5]

Not Outer Shareable. When the value of TTBR1.S is 1, indicates whether the memory associated with a translation table walk is Inner Shareable or Outer Shareable:

<table>
<thead>
<tr>
<th>NOS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Memory is Outer Shareable.</td>
</tr>
<tr>
<td>01</td>
<td>Memory is Inner Shareable.</td>
</tr>
</tbody>
</table>

This bit is ignored when the value of TTBR1.S is 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RGN, bits [4:3]

Region bits. Indicates the Outer cacheability attributes for the memory associated with the translation table walks:

<table>
<thead>
<tr>
<th>RGN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>01</td>
<td>Normal memory, Outer Write-Back Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>10</td>
<td>Normal memory, Outer Write-Through Cacheable.</td>
</tr>
<tr>
<td>11</td>
<td>Normal memory, Outer Write-Back no Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IMP, bit [2]

The effect of this bit is IMPLEMENTATION DEFINED. If the translation table implementation does not include any IMPLEMENTATION DEFINED features this bit is RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

S, bit [1]

Shareable. Indicates whether the memory associated with the translation table walks is Non-shareable:
Meaning

<table>
<thead>
<tr>
<th>S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Memory is Non-shareable.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory is shareable. The TTBR1.NOS field indicates whether the memory is Inner Shareable or Outer Shareable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### When TTBCR.EAE == 1:

<table>
<thead>
<tr>
<th>Bits</th>
<th>63:56</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>55:48</td>
<td>ASID, bits</td>
</tr>
<tr>
<td></td>
<td>47:1</td>
<td>BADDR, bits</td>
</tr>
<tr>
<td></td>
<td></td>
<td>CnP</td>
</tr>
</tbody>
</table>

#### Bits [63:56]

Reserved, RES0.

#### ASID, bits [55:48]

An ASID for the translation table base address. The TTBCR.A1 field selects either TTBR0.ASID or TTBR1.ASID.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

#### BADDR, bits [47:1]

Translation table base address, bits[47:x], Bits [x-1:1] are RES0, with the additional requirement that if bits[x-1:3] are not all zero, this is a misaligned translation table base address, with effects that are **CONSTRAINED UNPREDICTABLE**, and must be one of the following:

- Register bits [x-1:3] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

x is determined from the value of TTBCR.T1SZ as follows:

- If TTBCR.T1SZ is 0 or 1, x = 5 - TTBCR.T1SZ.
- If TTBCR.T1SZ is greater than 1, x = 14 - TTBCR.T1SZ.

If bits[47:40] of the translation table base address are not zero, an Address size fault is generated.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

#### CnP, bit [0]

**When FEAT_TTCNP is implemented:**

Common not Private. When TTBCR.EAE == 1, this bit indicates whether each entry that is pointed to by TTBR1 is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of TTBR1.CnP is 1.
### CnP

<table>
<thead>
<tr>
<th>Meaning</th>
<th>CnP</th>
</tr>
</thead>
<tbody>
<tr>
<td>The translation table entries pointed to by this instance of TTBR1, for the current ASID, are permitted to differ from corresponding entries for this instance of TTBR1 for other PEs in the Inner Shareable domain. This is not affected by:</td>
<td></td>
</tr>
<tr>
<td>• The value of TTBR1.CnP on those other PEs.</td>
<td></td>
</tr>
<tr>
<td>• The value of TTBCR.EAE on those other PEs.</td>
<td></td>
</tr>
<tr>
<td>• The value of the current ASID or, for the Non-secure instance of TTBR1, the value of the current VMID.</td>
<td></td>
</tr>
<tr>
<td>The translation table entries pointed to by this instance of TTBR1 are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of TTBR1.CnP is 1 for this instance of TTBR1 and all of the following apply:</td>
<td></td>
</tr>
<tr>
<td>• The translation table entries are pointed to by this instance of TTBR1.</td>
<td></td>
</tr>
<tr>
<td>• The value of the applicable TTBCR.EAE field is 1.</td>
<td></td>
</tr>
<tr>
<td>• The ASID is the same as the current ASID.</td>
<td></td>
</tr>
<tr>
<td>• For the Non-secure instance of TTBR1, the VMID is the same as the current VMID.</td>
<td></td>
</tr>
</tbody>
</table>

When a TLB combines entries from stage 1 translation and stage 2 translation into a single entry, that entry can only be shared between different PEs if the value of the CnP bit is 1 for both stage 1 and stage 2.

### Note

If the value of the TTBR1.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those TTBR1s do not point to the same translation table entries when the other conditions specified for the case when the value of CnP is 1 apply, then the results of translations are CONSTRAINED UNPREDICTABLE, see ‘CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values’.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Otherwise:

Reserved, RES0.

### Accessing the TTBR1

Accesses to this register use the following encodings:

```
MRC{<c>{<q>}} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}
```

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b000</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBR1_NS<<31:0>;
    else
        return TTBR1<31:0>;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return TTBR1_NS<<31:0>;
    else
        return TTBR1<31:0>;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return TTBR1_S<<31:0>;
    else
        return TTBR1_NS<<31:0>;
else
    return TTBR1<31:0>;

MCR{<c>{<q}> <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0010</td>
<td>0b0000</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        TTBR1_NS = ZeroExtend(R[t]);
    else
        TTBR1 = ZeroExtend(R[t]);
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        TTBR1_NS = ZeroExtend(R[t]);
    else
        TTBR1 = ZeroExtend(R[t]);
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDLISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDLISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            TTBR1_S = ZeroExtend(R[t]);
        else
            TTBR1_NS = ZeroExtend(R[t]);
if PSTATE_EL == EL0 then
  UNDEFINED;
elsif PSTATE_EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    return TTBR1_NS;
  else
    return TTBR1;
  elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      return TTBR1_NS;
    else
      TTBR1 = R[t2]:R[t];
    fi
  elsif PSTATE_EL == EL3 then
    if SCR.NS == '0' then
      UNDEFINED;
    else
      if SCR.NS == '0' then
        TTBR1_S = R[t2]:R[t];
      else
        TTBR1_NS = R[t2]:R[t];
      fi
    fi
  fi

if PSTATE_EL == EL0 then
  UNDEFINED;
elsif PSTATE_EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.TVM == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x04);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.TVM == '1' then
    AArch32.TakeHypTrapException(0x04);
  elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
    TTBR1_NS = R[t2]:R[t];
  else
    TTBR1 = R[t2]:R[t];
  elsif PSTATE_EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
      TTBR1_NS = R[t2]:R[t];
    else
      TTBR1 = R[t2]:R[t];
  elsif PSTATE_EL == EL3 then
    if SCR.NS == '0' & CP15SDISABLE == HIGH then
      UNDEFINED;
    else
      if SCR.NS == '0' then
        TTBR1_S = R[t2]:R[t];
      else
        TTBR1_NS = R[t2]:R[t];
      fi
    fi
VBAR, Vector Base Address Register

The VBAR characteristics are:

**Purpose**

When high exception vectors are not selected, holds the vector base address for exceptions that are not taken to Monitor mode or to Hyp mode.

Software must program VBAR(NS) with the required initial value as part of the PE boot sequence.

**Configuration**

AArch32 System register VBAR bits [31:0] are architecturally mapped to AArch64 System register VBAR_EL1[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to VBAR are UNDEFINED.

**Attributes**

VBAR is a 32-bit register.

**Field descriptions**

The VBAR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:5]**

Vector Base Address. Bits[31:5] of the base address of the exception vectors for exceptions taken to this Exception level. Bits[4:0] of an exception vector are the exception offset.

On a Warm reset, this field resets to an IMPLEMENTATION DEFINED value.

**Bits [4:0]**

Reserved, RES0.

**Accessing the VBAR**

Accesses to this register use the following encodings:

\[\text{MRC\{<c>\}{<q>} <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>{, \{#<opc2>}}\}\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

Page 3125
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        return VBAR_NS;
    else
        return VBAR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return VBAR_NS;
    else
        return VBAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        return VBAR_S;
    else
        return VBAR_NS;
else
    return VBAR;
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        return VBAR_NS;
    else
        return VBAR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            VBAR_S = R[t];
        else
            VBAR_NS = R[t];
else
    VBAR = R[t];

MCR{<c>}{<q>}<coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0000</td>
<td>0b000</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif HaveEL(EL3) && ELUsingAArch32(EL3) then
        VBAR_NS = R[t];
    else
        VBAR = R[t];
elsif PSTATE.EL == EL2 then
    if HaveEL(EL3) && ELUsingAArch32(EL3) then
        VBAR_NS = R[t];
    else
        VBAR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' && CP15SDISABLE == HIGH then
        UNDEFINED;
    elsif SCR.NS == '0' && CP15SDISABLE2 == HIGH then
        UNDEFINED;
    else
        if SCR.NS == '0' then
            VBAR_S = R[t];
        else
            VBAR_NS = R[t];
VDFSR, Virtual SError Exception Syndrome Register

The VDFSR characteristics are:

**Purpose**

Provides the syndrome value reported to software on taking a virtual SError interrupt exception to EL1, or on executing an ESB instruction at EL1.

When a virtual SError interrupt is taken, the syndrome value is reported in DFRS (AET, ExT) and the remainder of the DFRS is set as defined by VMSAv8-32. For more information, see 'The AArch32 Virtual Memory System Architecture'.

If the virtual SError interrupt is deferred by an ESB instruction, then the syndrome value is written to VDISR.

**Configuration**

AArch32 System register VDFSR bits [31:0] are architecturally mapped to AArch64 System register VSESR_EL2[31:0] when the highest implemented Exception level is using AArch64.

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to VDFSR are UNDEFINED.

If EL2 is not implemented, then VDFSR is res0 from Monitor mode when SCR.NS == 1.

**Attributes**

VDFSR is a 32-bit register.

**Field descriptions**

The VDFSR bit assignments are:

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0  AET  RES0ExT  RES0</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**AET, bits [15:14]**

When a virtual SError interrupt is taken to EL1 using AArch32, DFRS[15:4] is set to VDFSR.AET.
When a virtual SError interrupt is deferred by an ESB instruction, VDISR[15:4] is set to VDFSR.AET.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [13]**

Reserved, RES0.

**ExT, bit [12]**

When a virtual SError interrupt is taken to EL1 using AArch32, DFRS[12] is set to VDFSR.ExT.
When a virtual SError interrupt is deferred by an ESB instruction, VDISR[12] is set to VDFSR.ExT.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [11:0]  
Reserved, RES0.

**Accessing the VDFSR**

Direct reads and writes of VDFSR are **UNDEFINED** if EL3 is implemented and using AArch32 in all Secure privileged modes other than Monitor mode.

If EL2 is not implemented, then VDFSR is **RES0** from Monitor mode when SCR.NS == 1.

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return VDFSR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return VDFSR;

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0101</td>
<td>0b0010</td>
<td>0b011</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T5 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T5 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    VDFSR = R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        VDFSR = R[t];
**VDISR, Virtual Deferred Interrupt Status Register**

The VDISR characteristics are:

**Purpose**

Records that an SError interrupt has been consumed by an ESB instruction.

**Configuration**

AArch32 System register VDISR bits [31:0] are architecturally mapped to AArch64 System register VDISR_EL2[31:0].

This register is present only when FEAT_RAS is implemented. Otherwise, direct accesses to VDISR are UNDEFINED.

If EL2 is not implemented, then VDISR is RES0 from Monitor mode when SCR.NS == 1.

**Attributes**

VDISR is a 32-bit register.

**Field descriptions**

The VDISR bit assignments are:

**When TTBCR.EAE == 0:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>A</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>AET</td>
</tr>
<tr>
<td>28</td>
<td>RES0</td>
</tr>
<tr>
<td>27</td>
<td>ExT</td>
</tr>
<tr>
<td>26</td>
<td>RES0</td>
</tr>
<tr>
<td>25</td>
<td>FS[4]</td>
</tr>
<tr>
<td>24</td>
<td>LPAE</td>
</tr>
<tr>
<td>23</td>
<td>RES0</td>
</tr>
<tr>
<td>22</td>
<td>FS[3:0]</td>
</tr>
</tbody>
</table>

A, bit [31]

Set to 1 when an ESB instruction defers a virtual SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [30:16]

Reserved, RES0.

AET, bits [15:14]

The value copied from VDFSR.AET.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [13]

Reserved, RES0.

ExT, bit [12]

The value copied from VDFSR.ExT.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [11]

Reserved, RES0.

FS, bits [10, 3:0]

Fault status code. Set to 0b10110 when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>FS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b10110</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The FS field is split as follows:

- FS[4] is VDISR[10].
- FS[3:0] is VDISR[3:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

LPAE, bit [9]

Format.

Set to TTBCR.EAE when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Using the Short-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [8:4]

Reserved, RES0.

When TTBCR.EAE == 1:

| 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0 |
|---------------------------------------------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|--|-----------------|--|
| A                                          | RES0 | AET | RES0 | ExT| RES0 | LPAE | RES0 | STATUS |

A, bit [31]

Set to 1 when an ESB instruction defers a virtual SError interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [30:16]

Reserved, RES0.

AET, bits [15:14]

The value copied from VDFSRAET.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [13]

Reserved, RES0.
ExT, bit [12]

The value copied from VDFSR.ExT.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [11:10]

Reserved, RES0.

LPAE, bit [9]

Format.
Set to TTBCR.EAE when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>LPAE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1</td>
<td>Using the Long-descriptor translation table format.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [8:6]

Reserved, RES0.

STATUS, bits [5:0]

Fault status code. Set to 0b010001 when an ESB instruction defers a virtual SError interrupt.

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b010001</td>
<td>Asynchronous SError interrupt.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the VDISR

Direct reads and writes of VDFSR are UNDEFINED if EL3 is implemented and using AArch32 in all Secure privileged modes other than Monitor mode.

An indirect write to VDISR made by an ESB instruction does not require an explicit synchronization operation for the value that is written to be observed by a direct read of DISR occurring in program order after the ESB instruction.

If EL2 is not implemented, then VDISR is RES0 from Monitor mode when SCR.NS == 1.

Accesses to this register use the following encodings:

\[
\text{MRC}\{<c>\}\{<q>\} <\text{coproc}>, \{#\}<\text{opc1}>, <\text{Rt}>, <\text{CRn}>, <\text{CRm}>, \{#\}<\text{opc2}>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    return VDISR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return VDISR;
    endif
endif

MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td></td>
<td></td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() & !ELUsingAArch32(EL2) & HSTR_EL2.T12 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() & ELUsingAArch32(EL2) & HSTR.T12 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    endif
elsif PSTATE.EL == EL2 then
    return DISR;
elsif PSTATE.EL == EL3 then
    return DISR;
endif

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td></td>
<td></td>
<td>0b001</td>
</tr>
</tbody>
</table>
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b1100</td>
<td>0b0001</td>
<td>0b001</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T12 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T12 == '1' then
    AArch32.TakeHypTrapException(0x03);
  elsif EL2Enabled() && !ELUsingAArch32(EL2) && HCR_EL2.AMO == '1' then
    VDISR_EL2 = R[t];
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HCR.AMO == '1' then
    VDISR = R[t];
  else
    DISR = R[t];
elsif PSTATE.EL == EL2 then
  DISR = R[t];
else if PSTATE.EL == EL3 then
  DISR = R[t];
**VMPIDR, Virtualization Multiprocessor ID Register**

The VMPIDR characteristics are:

**Purpose**

Holds the value of the Virtualization Multiprocessor ID. This is the value returned by Non-secure EL1 reads of MPIDR.

**Configuration**

AArch32 System register VMPIDR bits [31:0] are architecturally mapped to AArch64 System register VMPIDR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to VMPIDR are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, this register takes the value of the MPIDR.

**Attributes**

VMPIDR is a 32-bit register.

**Field descriptions**

The VMPIDR bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>M</th>
<th>U</th>
<th>RES0</th>
<th>MT</th>
<th>Aff2</th>
<th>Aff1</th>
<th>Aff0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td></td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
</tr>
<tr>
<td>19</td>
<td></td>
<td></td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>13</td>
<td></td>
<td></td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**M, bit [31]**

Indicates whether this implementation includes the functionality introduced by the ARMv7 Multiprocessing Extensions. The possible values of this bit are:

<table>
<thead>
<tr>
<th>M</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This implementation does not include the ARMv7 Multiprocessing Extensions functionality.</td>
</tr>
<tr>
<td>0b1</td>
<td>This implementation includes the ARMv7 Multiprocessing Extensions functionality.</td>
</tr>
</tbody>
</table>

From Armv8 this bit is RES1.

**U, bit [30]**

Indicates a Uniprocessor system, as distinct from PE 0 in a multiprocessor system. The possible values of this bit are:

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Processor is part of a multiprocessor system.</td>
</tr>
<tr>
<td>0b1</td>
<td>Processor is part of a uniprocessor system.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MPIDR.U.

**Bits [29:25]**

Reserved, RES0.
MT, bit [24]

Indicates whether the lowest level of affinity consists of logical PEs that are implemented using a multithreading type approach. See the description of Aff0 for more information about affinity levels. The possible values of this bit are:

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Performance of PEs at the lowest affinity level is largely independent.</td>
</tr>
<tr>
<td>0b1</td>
<td>Performance of PEs at the lowest affinity level is very interdependent.</td>
</tr>
</tbody>
</table>

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MPIDR.MT.

Aff2, bits [23:16]

Affinity level 2. See the description of Aff0 for more information.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MPIDR.Aff2.

Aff1, bits [15:8]

Affinity level 1. See the description of Aff0 for more information.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MPIDR.Aff1.

Aff0, bits [7:0]

Affinity level 0. This is the affinity level that is most significant for determining PE behavior. Higher affinity levels are increasingly less significant in determining PE behavior. The assigned value of the MPIDR.{Aff2, Aff1, Aff0} or MPIDR_EL1.{Aff3, Aff2, Aff1, Aff0} set of fields of each PE must be unique within the system as a whole.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MPIDR.Aff0.

Accessing the VMPIDR

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q>} <coproc>, \\{#\}<opc1>, <Rt>, <CRn>, <CRm>\{, \\{#\}<opc2>\}
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

\[
\text{if PSTATE.EL == EL0 then UNDEFINED;}
\text{elsif PSTATE.EL == EL1 then}
\text{\quad if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then}
\text{\quad \quad AArch64.AArch32SystemAccessTrap(EL2, 0x03);}
\text{\quad elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then}
\text{\quad \quad AArch32.TakeHypTrapException(0x03);}
\text{\quad else UNDEFINED;}
\text{\quad elsif PSTATE.EL == EL2 then}
\text{\quad \quad return VMPIDR;}
\text{\quad elsif PSTATE.EL == EL3 then}
\text{\quad \quad if !HaveEL(EL2) then}
\text{\quad \quad \quad return MPIDR;}
\text{\quad \quad elsif SCR.NS == '0' then}
\text{\quad \quad \quad \quad UNDEFINED;}
\text{\quad \quad else}
\text{\quad \quad \quad \quad return VMPIDR;}
\text{\quad else UNDEFINED;}
\text{\quad elsif PSTATE.EL == EL3 then}
\text{\quad \quad if !HaveEL(EL2) then}
\text{\quad \quad \quad return MPIDR;}
\text{\quad \quad elsif SCR.NS == '0' then}
\text{\quad \quad \quad \quad UNDEFINED;}
\text{\quad \quad else}
\text{\quad \quad \quad \quad return VMPIDR;}
\text{\quad else UNDEFINED;}
\text{\quad \quad \quad \quad return VMPIDR;}
\text{else UNDEFINED;}
\]

VMPIDR, Virtualization Multiprocessor ID Register
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm},{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
ellif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end
    elseif PSTATE.EL == EL2 then
        VMPIDR = R[t];
    elseif PSTATE.EL == EL3 then
        if !HaveEL(EL2) then
            //no operation
        elseif SCR.NS == '0' then
            UNDEFINED;
        else
            VMPIDR = R[t];
        end
    end
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b000</td>
<td>0b0000</td>
<td>0b0000</td>
<td>0b101</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
ellif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elseif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elseif EL2Enabled() && !ELUsingAArch32(EL2) then
        return VMPIDR_EL2<31:0>;
    elseif EL2Enabled() && ELUsingAArch32(EL2) then
        return VMPIDR;
    else
        return MPIDR;
    end
    elseif PSTATE.EL == EL2 then
        return MPIDR;
    elseif PSTATE.EL == EL3 then
        return MPIDR;
VPI DR, Virtualization Processor ID Register

The VPI DR characteristics are:

Purpose

Holds the value of the Virtualization Processor ID. This is the value returned by Non-secure EL1 reads of MIDR.

Configuration

AArch32 System register VPI DR bits [31:0] are architecturally mapped to AArch64 System register VPI DR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to VPI DR are UNDEFINED.

If EL2 is not implemented but EL3 is implemented, this register takes the value of the MIDR.

Attributes

VPI DR is a 32-bit register.

Field descriptions

The VPI DR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Implementer | Variant | Architecture | PartNum | Revision |

Implementer, bits [31:24]

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>ASCII representation</th>
<th>Implementer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x41</td>
<td>A</td>
<td>Arm Limited</td>
</tr>
<tr>
<td>0x42</td>
<td>B</td>
<td>Broadcom Corporation</td>
</tr>
<tr>
<td>0x43</td>
<td>C</td>
<td>Cavium Inc.</td>
</tr>
<tr>
<td>0x44</td>
<td>D</td>
<td>Digital Equipment Corporation</td>
</tr>
<tr>
<td>0x49</td>
<td>I</td>
<td>Infineon Technologies AG</td>
</tr>
<tr>
<td>0x40</td>
<td>M</td>
<td>Motorola or Freescale Semiconductor Inc.</td>
</tr>
<tr>
<td>0x4E</td>
<td>N</td>
<td>NVIDIA Corporation</td>
</tr>
<tr>
<td>0x50</td>
<td>P</td>
<td>Applied Micro Circuits Corporation</td>
</tr>
<tr>
<td>0x51</td>
<td>Q</td>
<td>Qualcomm Inc.</td>
</tr>
<tr>
<td>0x56</td>
<td>V</td>
<td>Marvell International Ltd.</td>
</tr>
<tr>
<td>0x69</td>
<td>i</td>
<td>Intel Corporation</td>
</tr>
</tbody>
</table>

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MIDR. Implementer.

Variant, bits [23:20]

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product.
On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MIDR.Variant.

**Architecture, bits [19:16]**

Architecture version. Defined values are:

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv4.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv4T.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv5 (obsolete).</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv5T.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv5TE.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv5TEJ.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv6.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Architectural features are individually identified in the ID.* registers, see ‘ID registers’.</td>
</tr>
</tbody>
</table>

All other values are reserved.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MIDRArchitecture.

**PartNum, bits [15:4]**

An IMPLEMENTATION DEFINED primary part number for the device.

On processors implemented by Arm, if the top four bits of the primary part number are 0x0 or 0x7, the variant and architecture are encoded differently.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MIDR.PartNum.

**Revision, bits [3:0]**

An IMPLEMENTATION DEFINED revision number for the device.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to the value in MIDR.Revision.

**Accessing the VPIDR**

Accesses to this register use the following encodings:

\[
\text{MRC\{<c>\}{<q}> <coproc>, \{#<opc1>, <Rt>, <CRn>, <CRm>\}, \{#<opc2>\}}
\]

\[
\begin{array}{|c|c|c|c|c|}
\hline
\text{coproc} & \text{opc1} & \text{CRn} & \text{CRm} & \text{opc2} \\
\hline
0b1111 & 0b100 & 0b0000 & 0b0000 & 0b000 \\
\hline
\end{array}
\]

if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  return VPIDR;
elsif PSTATE.EL == EL3 then
  if !HaveEL(EL2) then
    return MIDR;
  elsif SCR.NS == '0' then
    UNDEFINED;
  else
    return VPIDR;

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end
elsif PSTATE.EL == EL2 then
    VPIDR = R[t];
elsif PSTATE.EL == EL3 then
    if !HaveEL(EL2) then
        //no operation
    elsif SCR.NS == '0' then
        UNDEFINED;
    else
        VPIDR = R[t];
    end
MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T0 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T0 == '1' then
        AArch32.TakeHypTrapException(0x03);
    elsif EL2Enabled() && !ELUsingAArch32(EL2) then
        return VPIDR_EL2<31:0>;
    elsif EL2Enabled() && ELUsingAArch32(EL2) then
        return VPIDR;
    else
        return MIDR;
    end
elsif PSTATE.EL == EL2 then
    return MIDR;
elsif PSTATE.EL == EL3 then
    return MIDR;

30/09/2020 15:07; ccead0cbf089f9ceec50268e82aec9e71047211
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VTCR, Virtualization Translation Control Register

The VTCR characteristics are:

**Purpose**

The control register for stage 2 of the Non-secure PL1&0 translation regime.

**Note**

This stage of translation always uses the Long-descriptor translation table format.

**Configuration**

AArch32 System register VTCR bits [31:0] are architecturally mapped to AArch64 System register VTCR_EL2[31:0].

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to VTCR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

VTCR is a 32-bit register.

**Field descriptions**

The VTCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES1 | RES0 | HWU62 | HWU61 | HWU60 | HWU59 | RES0 | SH0 | ORGN0 | RGNO | SL0 | RES0 | S | T0SZ |

**Bit [31]**

Reserved, RES1.

**Bits [30:29]**

Reserved, RES0.

**HWU62, bit [28]**

When FEAT_HPDS2 is implemented:

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[62] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU62</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[62] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[62] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:
Reserved, RES0.

**HWU61, bit [27]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[61] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU61</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[61] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[61] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

**HWU60, bit [26]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[60] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU60</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[60] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[60] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

**HWU59, bit [25]**

*When FEAT_HPDS2 is implemented:*

Hardware Use. Indicates IMPLEMENTATION DEFINED hardware use of bit[59] of the stage 2 translation table Block or Page entry.

<table>
<thead>
<tr>
<th>HWU59</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bit[59] of each stage 2 translation table Block or Page entry cannot be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bit[59] of each stage 2 translation table Block or Page entry can be used by hardware for an IMPLEMENTATION DEFINED purpose.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Otherwise:

Reserved, RES0.

Bits [24:14]

Reserved, RES0.

SH0, bits [13:12]

Shareability attribute for memory associated with translation table walks using VTTBR.

<table>
<thead>
<tr>
<th>SH0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

Other values are reserved. The effect of programming this field to a Reserved value is that behavior is CONSTRAINED UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

ORGN0, bits [11:10]

Outer cacheability attribute for memory associated with translation table walks using VTTBR.

<table>
<thead>
<tr>
<th>ORGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Outer Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Outer Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Outer Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

IRGN0, bits [9:8]

Inner cacheability attribute for memory associated with translation table walks using VTTBR.

<table>
<thead>
<tr>
<th>IRGN0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Normal memory, Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal memory, Inner Write-Back Read-Allocate Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal memory, Inner Write-Through Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal memory, Inner Write-Back Read-Allocate No Write-Allocate Cacheable.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

SL0, bits [7:6]

Starting level for translation table walks using VTTBR.

<table>
<thead>
<tr>
<th>SL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Start at level 2</td>
</tr>
<tr>
<td>0b01</td>
<td>Start at level 1</td>
</tr>
</tbody>
</table>

All other values are reserved. If this field is programmed to a reserved value, or to a value that is not consistent with the programming of T0SZ, then a stage 2 level 1 Translation fault is generated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bit [5]
Reserved, RES0.

S, bit [4]
Sign extension bit. This bit must be programmed to the value of T0SZ[3]. If it is not, then the behavior is CONSTRAINED UNPREDICTABLE and the stage 2 T0SZ value is treated as an UNKNOWN value, see 'Misprogramming VTCR.S'.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

T0SZ, bits [3:0]
The size offset of the memory region addressed by VTTBR. The region size is $2^{(32-T0SZ)}$ bytes.

This field holds a four-bit signed integer value, meaning it supports values from -8 to 7.

Note
This is different from the other translation control registers, where TnSZ holds a three-bit unsigned integer, supporting values from 0 to 7.

If this field is programmed to a value that is not consistent with the programming of SL0 then a stage 2 level 1 Translation fault is generated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the VTCR

Accesses to this register use the following encodings:

MRC{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>

if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x03);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x03);
    else
        UNDEFINED;
    end iff
elsif PSTATE.EL == EL2 then
    return VTCR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return VTCR;
    end if
MCR{<c>}{<q>} <coproc>, {#}<opc1>, <Rt>, <CRn>, <CRm>{, {#}<opc2>}

<table>
<thead>
<tr>
<th>coproc</th>
<th>opc1</th>
<th>CRn</th>
<th>CRm</th>
<th>opc2</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>0b100</td>
<td>0b0010</td>
<td>0b0001</td>
<td>0b010</td>
</tr>
</tbody>
</table>
if PSTATE.EL == EL0 then
  UNDEFINED;
elsif PSTATE.EL == EL1 then
  if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
    AArch64.AArch32SystemAccessTrap(EL2, 0x03);
  elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
    AArch32.TakeHypTrapException(0x03);
  else
    UNDEFINED;
elsif PSTATE.EL == EL2 then
  VTCR = R[t];
elsif PSTATE.EL == EL3 then
  if SCR.NS == '0' then
    UNDEFINED;
  else
    VTCR = R[t];
VTTBR, Virtualization Translation Table Base Register

The VTTBR characteristics are:

**Purpose**

Holds the base address of the translation table for the initial lookup for stage 2 of an address translation in the Non-secure PL1&0 translation regime, and other information for this translation regime.

**Configuration**

AArch32 System register VTTBR bits [63:0] are architecturally mapped to AArch64 System register \texttt{VTTBR_EL2[63:0]}.

This register is present only when AArch32 is supported at any Exception level. Otherwise, direct accesses to VTTBR are UNDEFINED.

If EL2 is not implemented, this register is RES0 from EL3.

**Attributes**

VTTBR is a 64-bit register.

**Field descriptions**

The VTTBR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | VMID | BADDR | CnP |

Bits [63:56]

Reserved, RES0.

VMID, bits [55:48]

The VMID for the translation table.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to 0.

BADDR, bits [47:1]

Translation table base address, bits[47:x], Bits [x-1:1] are RES0, with the additional requirement that if bits[x-1:3] are not all zero, this is a misaligned translation table base address, with effects that are CONSTRAINED UNPREDICTABLE, and must be one of the following:

- Register bits [x-1:3] are treated as if all the bits are zero. The value read back from these bits is either the value written or zero.
- The result of the calculation of an address for a translation table walk using this register can be corrupted in those bits that are nonzero.

x is determined from the value of \texttt{VTCR.SL0} and \texttt{VTCR.T0SZ} as follows:

- If \texttt{VTCR.SL0} is 0b00, meaning that lookup starts at level 2, then x is 14 - \texttt{VTCR.T0SZ}.
- If \texttt{VTCR.SL0} is 0b01, meaning that lookup starts at level 1, then x is 5 - \texttt{VTCR.T0SZ}.
- If \texttt{VTCR.SL0} is either 0b10 or 0b11 then a stage 2 level 1 Translation fault is generated.
If bits[47:40] of the translation table base address are not zero, an Address size fault is generated.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally UNKNOWN value.

**CnP, bit [0]**

**When FEAT_TTCNP is implemented:**

Common not Private. This bit indicates whether each entry that is pointed to by VTTBR is a member of a common set that can be used by every PE in the Inner Shareable domain for which the value of VTTBR.CnP is 1.

<table>
<thead>
<tr>
<th>CnP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The translation table entries pointed to by VTTBR are permitted to differ from the entries for VTTBR for other PEs in the Inner Shareable domain. This is not affected by the value of the current VMID.</td>
</tr>
<tr>
<td>0b1</td>
<td>The translation table entries pointed to by VTTBR are the same as the translation table entries for every other PE in the Inner Shareable domain for which the value of VTTBR.CnP is 1 and the VMID is the same as the current VMID.</td>
</tr>
</tbody>
</table>

When a TLB combines entries from stage 1 translation and stage 2 translation into a single entry, that entry can only be shared between different PEs if the value of the CnP bit is 1 for both stage 1 and stage 2.

**Note**

If the value of the VTTBR.CnP bit is 1 on multiple PEs in the same Inner Shareable domain and those VTTBRs do not point to the same translation table entries when the VMID value is the same as the current VMID, then the results of translations are CONSTRAINED UNPREDICTABLE, see 'CONSTRAINED UNPREDICTABLE behaviors due to caching of control or data values'.

On a Warm reset, in a system where the PE resets into EL2 or EL3, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Accessing the VTTBR**

Accesses to this register use the following encodings:

\[
\text{MRRC}\{<c>\}\{<q>\} \ <\text{coproc}\>, \{#\}<\text{opc1}\>, \ <\text{Rt}\>, \ <\text{Rt2}\>, \ <\text{CRm}\>
\]

<table>
<thead>
<tr>
<th>coproc</th>
<th>CRm</th>
<th>opc1</th>
</tr>
</thead>
<tbody>
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if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x04);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    return VTTBR;
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        return VTTBR;

MCRR{coproc},{Rt},{Rt2},{CRm}

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if PSTATE.EL == EL0 then
    UNDEFINED;
elsif PSTATE.EL == EL1 then
    if EL2Enabled() && !ELUsingAArch32(EL2) && HSTR_EL2.T2 == '1' then
        AArch64.AArch32SystemAccessTrap(EL2, 0x04);
    elsif EL2Enabled() && ELUsingAArch32(EL2) && HSTR.T2 == '1' then
        AArch32.TakeHypTrapException(0x04);
    else
        UNDEFINED;
elsif PSTATE.EL == EL2 then
    VTTBR = R[t2]:R[t];
elsif PSTATE.EL == EL3 then
    if SCR.NS == '0' then
        UNDEFINED;
    else
        VTTBR = R[t2]:R[t];
# System Register index by instruction and encoding

Below are indexes for registers and operations accessed in the following ways:

For AArch32

- MCR/MRC
- MCRR/MRRC
- MRS/MSR
- VMRS/VMSR

For AArch64

- AT
- CFP
- CPP
- DC
- DVP
- IC
- MRS/MSR
- TLBI

## Registers and operations in AArch32

### Accessed using MCR/MRC:

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System Register index by instruction and encoding

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**Registers and operations in AArch64**

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# System Register index by functional group

Below are indexes for registers with the following main functional groups:

- **ID**
- **Memory**
- **Other**
- **Exception**
- **PSTATE**
- **Cache**
- **Address**
- **TLB**
- **PMU**
- **Reset**
- **Thread**
- **IMP DEF**
- **Timer**
- **Debug**
- **CTI**
- **Virt**
- **Secure**
- **Float**
- **Legacy**
- **GIC**
- **GICD**
- **GICC**
- **GICR**
- **GICH**
- **GICV**
- **GITS**
- **RAS**
- **MPAM**
- **Pointer authentication**
- **AMU**
- **GIC ITS registers**

## In the ID functional group:

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<tr>
<th>Exec State</th>
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<td>Current Cache Size ID Register</td>
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<td>CCSIDR2</td>
<td>Current Cache Size ID Register 2</td>
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<td>CLIDR</td>
<td>Cache Level ID Register</td>
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<td>CSSEL0</td>
<td>Cache Size Selection Register</td>
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<td>Cache Type Register</td>
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<td>Auxiliary Feature Register 0</td>
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<td>ID_PFR2</td>
<td>Processor Feature Register 2</td>
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### System Register index by functional group

#### Exec state | Name | Description
--- | --- | ---
AArch32 | MIDR | Main ID Register
AArch32 | MPIDR | Multiprocessor Affinity Register
AArch32 | REVIDR | Revision ID Register
AArch32 | TCMTR | TCM Type Register
AArch32 | TLBTR | TLB Type Register
AArch64 | CCSIDR2_EL1 | Current Cache Size ID Register 2
AArch64 | CCSIDR_EL1 | Current Cache Size ID Register
AArch64 | CLIDR_EL1 | Cache Level ID Register
AArch64 | CSSEL_EL1 | Cache Size Selection Register
AArch64 | CTR_EL0 | Cache Type Register
AArch64 | DCZID_EL0 | Data Cache Zero ID register
AArch64 | GMID_EL1 | Multiple tag transfer ID register
AArch64 | ID AA64AFR0_EL1 | AArch64 Auxiliary Feature Register 0
AArch64 | ID AA64AFR1_EL1 | AArch64 Auxiliary Feature Register 1
AArch64 | ID AA64DFR0_EL1 | AArch64 Debug Feature Register 0
AArch64 | ID AA64DFR1_EL1 | AArch64 Debug Feature Register 1
AArch64 | ID AA64ISAR0_EL1 | AArch64 Instruction Set Attribute Register 0
AArch64 | ID AA64ISAR1_EL1 | AArch64 Instruction Set Attribute Register 1
AArch64 | ID AA64ISAR2_EL1 | AArch64 Instruction Set Attribute Register 2
AArch64 | ID AA64MMFR0_EL1 | AArch64 Memory Model Feature Register 0
AArch64 | ID AA64MMFR1_EL1 | AArch64 Memory Model Feature Register 1
AArch64 | ID AA64MMFR2_EL1 | AArch64 Memory Model Feature Register 2
AArch64 | ID AA64PFRO_EL1 | AArch64 Processor Feature Register 0
AArch64 | ID AA64PFR1_EL1 | AArch64 Processor Feature Register 1
AArch64 | ID AA64ZFR0_EL1 | SVE Feature ID register 0
AArch64 | ID AFRO_EL1 | AArch32 Auxiliary Feature Register 0
AArch64 | ID DFR0_EL1 | AArch32 Debug Feature Register 0
AArch64 | ID DFR1_EL1 | Debug Feature Register 1
AArch64 | ID ISAR0_EL1 | AArch32 Instruction Set Attribute Register 0
AArch64 | ID ISAR1_EL1 | AArch32 Instruction Set Attribute Register 1
AArch64 | ID ISAR2_EL1 | AArch32 Instruction Set Attribute Register 2
AArch64 | ID ISAR3_EL1 | AArch32 Instruction Set Attribute Register 3
AArch64 | ID ISAR4_EL1 | AArch32 Instruction Set Attribute Register 4
AArch64 | ID ISAR5_EL1 | AArch32 Instruction Set Attribute Register 5
AArch64 | ID ISAR6_EL1 | AArch32 Instruction Set Attribute Register 6
AArch64 | ID MMFR0_EL1 | AArch32 Memory Model Feature Register 0
AArch64 | ID MMFR1_EL1 | AArch32 Memory Model Feature Register 1
AArch64 | ID MMFR2_EL1 | AArch32 Memory Model Feature Register 2
AArch64 | ID MMFR3_EL1 | AArch32 Memory Model Feature Register 3
AArch64 | ID MMFR4_EL1 | AArch32 Memory Model Feature Register 4
AArch64 | ID MMFR5_EL1 | AArch32 Memory Model Feature Register 5
AArch64 | ID PFR0_EL1 | AArch32 Processor Feature Register 0
AArch64 | ID PFR1_EL1 | AArch32 Processor Feature Register 1
AArch64 | ID PFR2_EL1 | AArch32 Processor Feature Register 2
AArch64 | MIDR_EL1 | Main ID Register
AArch64 | MPAMIDR_EL1 | MPAM ID Register (EL1)
AArch64 | MPIDR_EL1 | Multiprocessor Affinity Register
AArch64 | REVIDR_EL1 | Revision ID Register
External | EDA32PF | External Debug Auxiliary Processor Feature Register
External | EDDR | External Debug Feature Register
External | EDPR | External Debug Processor Feature Register
External | MIDR_EL1 | Main ID Register

#### In the Memory functional group:

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<td>Context ID Register</td>
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<td>Domain Access Control Register</td>
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<td>Hyp Auxiliary Memory Attribute Indirection Register 0</td>
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## System Register index by functional group

### In the Other functional group:

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<td>ADFSR</td>
<td>Auxiliary Data Fault Status Register</td>
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<td>AIFS</td>
<td>Auxiliary Instruction Fault Status Register</td>
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<td>DFAR</td>
<td>Data Fault Address Register</td>
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### System Register index by functional group

#### In the Special functional group:

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<td>SPSR_svc</td>
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<td>CurrentEL</td>
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<td>Branch Predictor Invalidate All</td>
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<td>Branch Predictor Invalidate All, Inner Shareable</td>
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<td>BPMV</td>
<td>Branch Predictor Invalidate by VA</td>
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<td>DCCIMVAC</td>
<td>Data Cache line Clean and Invalidate by VA to PoC</td>
</tr>
<tr>
<td>AArch32</td>
<td>DCCISW</td>
<td>Data Cache line Clean and Invalidate by Set/Way</td>
</tr>
<tr>
<td>AArch32</td>
<td>DCCMVAU</td>
<td>Data Cache line Clean by VA to PoU</td>
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<td>DCCSW</td>
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<td>DCIMVAC</td>
<td>Data Cache line Invalidate by VA to PoC</td>
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<td>ICIALLU</td>
<td>Instruction Cache Invalidate All to PoU</td>
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<td>ICIALLUIS</td>
<td>Instruction Cache Invalidate All to PoU, Inner Shareable</td>
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<td>ICIMVAU</td>
<td>Instruction line Invalidate by VA to PoU</td>
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<td>Clean of Data and Allocation Tags by Set/Way</td>
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<tr>
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<td>DC CGDVAC</td>
<td>Clean of Data and Allocation Tags by VA to PoC</td>
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<td>DC CGDVADP</td>
<td>Clean of Data and Allocation Tags by VA to PoDP</td>
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<td>DC CGDVAP</td>
<td>Clean of Data and Allocation Tags by VA to PoP</td>
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<td>DC CGSW</td>
<td>Clean of Allocation Tags by Set/Way</td>
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<td>DC GZVA</td>
<td>Data Cache set Allocation Tags and Zero by VA</td>
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<td>DC IGDWS</td>
<td>Invalidate of Data and Allocation Tags by Set/Way</td>
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<td>DC IGDVAC</td>
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<td>DC IVAC</td>
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<td>IC IALLUIS</td>
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### In the Address functional group:

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<td>Address Translate Stages 1 and 2 Non-secure Only PL1 Read</td>
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<td>ATS12NSOPW</td>
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<td>AArch32</td>
<td>ATS12NSOUR</td>
<td>Address Translate Stages 1 and 2 Non-secure Only Unprivileged Read</td>
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## Exec state

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<td>ATS1CFPR</td>
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<td>ATS1CPRP</td>
<td>Address Translate Stage 1 Current state PL1 Read PAN</td>
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<td>ATS1CUR</td>
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<td>Cache Prefetch Prediction Restriction by Context</td>
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<td>Data TLB Invalidate by ASID match</td>
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<td>DVPRCTX</td>
<td>Data Value Prediction Restriction by Context</td>
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<td>Description</td>
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In the PMU functional group:

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<td>PMCCNTR</td>
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<td>AArch32</td>
<td>PMCEID0</td>
<td>Performance Monitors Common Event Identification register 0</td>
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<tr>
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<td>Performance Monitors Common Event Identification register 1</td>
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<tr>
<td>AArch32</td>
<td>PMCEID2</td>
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<tr>
<td>AArch32</td>
<td>PMCEID3</td>
<td>Performance Monitors Common Event Identification register 3</td>
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<tr>
<td>AArch32</td>
<td>PMCTENCLR</td>
<td>Performance Monitors Count Enable Clear register</td>
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<tr>
<td>AArch32</td>
<td>PMCTENSET</td>
<td>Performance Monitors Count Enable Set register</td>
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<td>AArch32</td>
<td>PMCR</td>
<td>Performance Monitors Control Register</td>
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<tr>
<td>AArch32</td>
<td>PMEVTYPE&lt;n&gt;</td>
<td>Performance Monitors Event Type Registers</td>
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<tr>
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<td>Performance Monitors Interrupt Enable Clear register</td>
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<td>PMMIR</td>
<td>Performance Monitors Machine Identification Register</td>
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<td>PMOVSR</td>
<td>Performance Monitors Overflow Flag Status Register</td>
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<td>PMSWINC</td>
<td>Performance Monitors Software Increment register</td>
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<td>PMUSERENR</td>
<td>Performance Monitors User Enable Register</td>
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<td>AArch32</td>
<td>PMXEVCTR&lt;n&gt;</td>
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<td>AArch32</td>
<td>RMR</td>
<td>Reset Management Register</td>
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<td>AArch32</td>
<td>RVBAR</td>
<td>Reset Vector Base Address Register</td>
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<td>RMR_EL1</td>
<td>Reset Management Register (EL1)</td>
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<td>RMR_EL2</td>
<td>Reset Management Register (EL2)</td>
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<td>RMR_EL3</td>
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<td>RVBAR_EL1</td>
<td>Reset Vector Base Address Register (if EL2 and EL3 not implemented)</td>
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<td>AArch64</td>
<td>RVBAR_EL2</td>
<td>Reset Vector Base Address Register (if EL3 not implemented)</td>
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<td>RVBAR_EL3</td>
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<td>TPIDRPRW</td>
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<td>Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.</td>
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**In the GICR functional group:**

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**In the GICC functional group:**

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<td>GICC_AHPPIR</td>
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<tr>
<td>Exec state</td>
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**In the GITS functional group:**

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<td>External</td>
<td>AMDEVAFF0</td>
<td>Activity Monitors Device Affinity Register 0</td>
</tr>
<tr>
<td>External</td>
<td>AMDEVAFF1</td>
<td>Activity Monitors Device Affinity Register 1</td>
</tr>
<tr>
<td>External</td>
<td>AMDEVAARCH</td>
<td>Activity Monitors Device Architecture Register</td>
</tr>
<tr>
<td>External</td>
<td>AMCR</td>
<td>Activity Monitors Control Register</td>
</tr>
<tr>
<td>External</td>
<td>AMDEVTYPER0&lt;n&gt;</td>
<td>Activity Monitors Event Type Registers 0</td>
</tr>
<tr>
<td>External</td>
<td>AMDEVTYPER1&lt;n&gt;</td>
<td>Activity Monitors Event Type Registers 1</td>
</tr>
<tr>
<td>External</td>
<td>AMIIDR</td>
<td>Activity Monitors Implementation Identification Register</td>
</tr>
<tr>
<td>External</td>
<td>AMPIDR0</td>
<td>Activity Monitors Peripheral Identification Register 0</td>
</tr>
<tr>
<td>External</td>
<td>AMPIDR1</td>
<td>Activity Monitors Peripheral Identification Register 1</td>
</tr>
<tr>
<td>External</td>
<td>AMPIDR2</td>
<td>Activity Monitors Peripheral Identification Register 2</td>
</tr>
<tr>
<td>External</td>
<td>AMPIDR3</td>
<td>Activity Monitors Peripheral Identification Register 3</td>
</tr>
<tr>
<td>External</td>
<td>AMPIDR4</td>
<td>Activity Monitors Peripheral Identification Register 4</td>
</tr>
</tbody>
</table>

In the GIC ITS registers functional group:

<table>
<thead>
<tr>
<th>Exec state</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>External</td>
<td>GITS_BASER&lt;n&gt;</td>
<td>ITS Translation Table Descriptors</td>
</tr>
<tr>
<td>External</td>
<td>GITS_CBASER</td>
<td>ITS Command Queue Descriptor</td>
</tr>
<tr>
<td>External</td>
<td>GITS_CREADR</td>
<td>ITS Read Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_CTLR</td>
<td>ITS Control Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_CWRITER</td>
<td>ITS Write Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_IIDR</td>
<td>ITS Identification Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_MPAMIDR</td>
<td>Report maximum PARTID and PMG Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_MPIDR</td>
<td>Report ITS’s affinity.</td>
</tr>
<tr>
<td>External</td>
<td>GITS_PARTIDR</td>
<td>Set PARTID and PMG Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_SGIR</td>
<td>ITS SGI Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_STATUSDR</td>
<td>ITS Error Reporting Status Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_TRANSLATER</td>
<td>ITS Translation Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_TYPER</td>
<td>ITS Type Register</td>
</tr>
<tr>
<td>External</td>
<td>GITS_UMSIR</td>
<td>ITS Unmapped MSI register</td>
</tr>
</tbody>
</table>

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External registers

AMCFGR: Activity Monitors Configuration Register

AMCGCR: Activity Monitors Counter Group Configuration Register

AMCIDR0: Activity Monitors Component Identification Register 0

AMCIDR1: Activity Monitors Component Identification Register 1

AMCIDR2: Activity Monitors Component Identification Register 2

AMCIDR3: Activity Monitors Component Identification Register 3

AMCNTENCLR0: Activity Monitors Count Enable Clear Register 0

AMCNTENCLR1: Activity Monitors Count Enable Clear Register 1

AMCNSENSET0: Activity Monitors Count Enable Set Register 0

AMCNSENSET1: Activity Monitors Count Enable Set Register 1

AMCR: Activity Monitors Control Register

AMDEVAFF0: Activity Monitors Device Affinity Register 0

AMDEVAFF1: Activity Monitors Device Affinity Register 1

AMDEVARC: Activity Monitors Device Architecture Register

AMDEVTYPE: Activity Monitors Device Type Register

AMEVCNTR0<n>: Activity Monitors Event Counter Registers 0

AMEVCNTR1<n>: Activity Monitors Event Counter Registers 1

AMEVTYPER0<n>: Activity Monitors Event Type Registers 0

AMEVTYPER1<n>: Activity Monitors Event Type Registers 1

AMIIDR: Activity Monitors Implementation Identification Register

AMPIDR0: Activity Monitors Peripheral Identification Register 0

AMPIDR1: Activity Monitors Peripheral Identification Register 1

AMPIDR2: Activity Monitors Peripheral Identification Register 2

AMPIDR3: Activity Monitors Peripheral Identification Register 3

AMPIDR4: Activity Monitors Peripheral Identification Register 4

ASICCTL: CTI External Multiplexer Control register

CNTACR<n>: Counter-timer Access Control Registers

CNTCR: Counter Control Register

CNTCV: Counter Count Value register

CNTEL0ACR: Counter-timer EL0 Access Control Register

CNTFID0: Counter Frequency ID

CNTFID<n>: Counter Frequency IDs, n > 0

CNTFRQ: Counter-timer Frequency

CNTID: Counter Identification Register
CNTNSAR: Counter-timer Non-secure Access Register
CNTPCT: Counter-timer Physical Count
CNT_P_CTL: Counter-timer Physical Timer Control
CNTP_CVAL: Counter-timer Physical Timer CompareValue
CNTP_TVAL: Counter-timer Physical Timer TimerValue
CNTSCR: Counter Scale Register
CNTSR: Counter Status Register
CNTTIDR: Counter-timer Timer ID Register
CNTVCT: Counter-timer Virtual Count
CNTVOFF: Counter-timer Virtual Offset
CNTVOFF<n>: Counter-timer Virtual Offsets
CNTV_CTL: Counter-timer Virtual Timer Control
CNTV_CVAL: Counter-timer Virtual Timer CompareValue
CNTV_TVAL: Counter-timer Virtual Timer TimerValue
CounterID<n>: Counter ID registers
CTIAPPCLEAR: CTI Application Trigger Clear register
CTIAPPUPDATE: CTI Application Pulse register
CTIAPPSET: CTI Application Trigger Set register
CTIAUTHSTATUS: CTI Authentication Status register
CTICHINSTATUS: CTI Channel In Status register
CTICHOUTSTATUS: CTI Channel Out Status register
CTICIDR0: CTI Component Identification Register 0
CTICIDR1: CTI Component Identification Register 1
CTICIDR2: CTI Component Identification Register 2
CTICIDR3: CTI Component Identification Register 3
CTICLAIMCLR: CTI CLAIM Tag Clear register
CTICLAIMSET: CTI CLAIM Tag Set register
CTICONTROL: CTI Control register
CTIDEVAFF0: CTI Device Affinity register 0
CTIDEVAFF1: CTI Device Affinity register 1
CTIDEVARCH: CTI Device Architecture register
CTIDEVCTL: CTI Device Control register
CTIDEVID: CTI Device ID register 0
CTIDEVID1: CTI Device ID register 1
CTIDEVID2: CTI Device ID register 2
CTIDEVTYPE: CTI Device Type register
CTIGATE: CTI Channel Gate Enable register
CTIINEN<n>: CTI Input Trigger to Output Channel Enable registers
CTIINTACK: CTI Output Trigger Acknowledge register
CTITHCTRL: CTI Integration mode Control register
CTILAR: CTI Lock Access Register
CTILSR: CTI Lock Status Register
CTIOUTEN<n>: CTI Input Channel to Output Trigger Enable registers
CTIPIDR0: CTI Peripheral Identification Register 0
CTIPIDR1: CTI Peripheral Identification Register 1
CTIPIDR2: CTI Peripheral Identification Register 2
CTIPIDR3: CTI Peripheral Identification Register 3
CTIPIDR4: CTI Peripheral Identification Register 4
CTITRIGINSTATUS: CTI Trigger In Status register
CTITRIGOUTSTATUS: CTI Trigger Out Status register
DBGAUTHSTATUS_EL1: Debug Authentication Status register
DBGBCR<n>_EL1: Debug Breakpoint Control Registers
DBGBVR<n>_EL1: Debug Breakpoint Value Registers
DBGCLAIMCLR_EL1: Debug CLAIM Tag Clear register
DBGCLAIMSET_EL1: Debug CLAIM Tag Set register
DBGDTRRX_EL0: Debug Data Transfer Register, Receive
DBGDTRTX_EL0: Debug Data Transfer Register, Transmit
DBGWCR<n>_EL1: Debug Watchpoint Control Registers
DBGWVR<n>_EL1: Debug Watchpoint Value Registers
EDAA32PFR: External Debug Auxiliary Processor Feature Register
EDACR: External Debug Auxiliary Control Register
EDCIDR0: External Debug Component Identification Register 0
EDCIDR1: External Debug Component Identification Register 1
EDCIDR2: External Debug Component Identification Register 2
EDCIDR3: External Debug Component Identification Register 3
EDCIDSr: External Debug Context ID Sample Register
EDDEVAFF0: External Debug Device Affinity register 0
EDDEVAFF1: External Debug Device Affinity register 1
EDDEVARCH: External Debug Device Architecture register
EDDEVID: External Debug Device ID register 0
EDDEVID1: External Debug Device ID register 1
EDDEVID2: External Debug Device ID register 2
### External registers

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>EDEVTYPE</td>
<td>External Debug Device Type register</td>
</tr>
<tr>
<td>EDDFR</td>
<td>External Debug Feature Register</td>
</tr>
<tr>
<td>EDEVCCR</td>
<td>External Debug Exception Catch Control Register</td>
</tr>
<tr>
<td>EDECR</td>
<td>External Debug Execution Control Register</td>
</tr>
<tr>
<td>EDESRS</td>
<td>External Debug Event Status Register</td>
</tr>
<tr>
<td>EDTOCTRL</td>
<td>External Debug Integration mode Control register</td>
</tr>
<tr>
<td>EDITTR</td>
<td>External Debug Instruction Transfer Register</td>
</tr>
<tr>
<td>EDLAR</td>
<td>External Debug Lock Access Register</td>
</tr>
<tr>
<td>EDSLRS</td>
<td>External Debug Lock Status Register</td>
</tr>
<tr>
<td>EDPCSR</td>
<td>External Debug Program Counter Sample Register</td>
</tr>
<tr>
<td>EDPRFR</td>
<td>External Debug Processor Feature Register</td>
</tr>
<tr>
<td>EDPIDR0</td>
<td>External Debug Peripheral Identification Register 0</td>
</tr>
<tr>
<td>EDPIDR1</td>
<td>External Debug Peripheral Identification Register 1</td>
</tr>
<tr>
<td>EDPIDR2</td>
<td>External Debug Peripheral Identification Register 2</td>
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<tr>
<td>EDPIDR3</td>
<td>External Debug Peripheral Identification Register 3</td>
</tr>
<tr>
<td>EDPIDR4</td>
<td>External Debug Peripheral Identification Register 4</td>
</tr>
<tr>
<td>EDPRCR</td>
<td>External Debug Power/Reset Control Register</td>
</tr>
<tr>
<td>EDPSRS</td>
<td>External Debug Processor Status Register</td>
</tr>
<tr>
<td>EDRCR</td>
<td>External Debug Reserve Control Register</td>
</tr>
<tr>
<td>EDSCR</td>
<td>External Debug Status and Control Register</td>
</tr>
<tr>
<td>EDVIDSR</td>
<td>External Debug Virtual Context Sample Register</td>
</tr>
<tr>
<td>EDWAR</td>
<td>External Debug Watchpoint Address Register</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;ADDR</td>
<td>Error Record Address Register</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;CTLR</td>
<td>Error Record Control Register</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;FR</td>
<td>Error Record Feature Register</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;MISC0</td>
<td>Error Record Miscellaneous Register 0</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;MISC1</td>
<td>Error Record Miscellaneous Register 1</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;MISC2</td>
<td>Error Record Miscellaneous Register 2</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;MISC3</td>
<td>Error Record Miscellaneous Register 3</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;PFGCDN</td>
<td>Pseudo-fault Generation Countdown Register</td>
</tr>
<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;PFGCTL</td>
<td>Pseudo-fault Generation Control Register</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;PFGF</td>
<td>Pseudo-fault Generation Feature Register</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;STATUS</td>
<td>Error Record Primary Status Register</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;CIDR0</td>
<td>Component Identification Register 0</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;CIDR1</td>
<td>Component Identification Register 1</td>
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<tr>
<td>E&lt;sub&gt;n&lt;/sub&gt;CIDR2</td>
<td>Component Identification Register 2</td>
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</table>
ERRCIDR3: Component Identification Register 3
ERRCRICR0: Critical Error Interrupt Configuration Register 0
ERRCRICR1: Critical Error Interrupt Configuration Register 1
ERRCRICR2: Critical Error Interrupt Configuration Register 2
ERRDEVAFF: Device Affinity Register
ERRDEVARCH: Device Architecture Register
ERRDEVID: Device Configuration Register
ERRERICR0: Error Recovery Interrupt Configuration Register 0
ERRERICR1: Error Recovery Interrupt Configuration Register 1
ERRERICR2: Error Recovery Interrupt Configuration Register 2
ERRFHIRICR0: Fault Handling Interrupt Configuration Register 0
ERRFHIRICR1: Fault Handling Interrupt Configuration Register 1
ERRFHIRICR2: Fault Handling Interrupt Configuration Register 2
ERRGSR: Error Group Status Register
ERRIIDR: Implementation Identification Register
ERRIMPDEF<n>: IMPLEMENTATION DEFINED Register <n>
ERRIRQCR<n>: Generic Error Interrupt Configuration Register
ERRIRQSR: Error Interrupt Status Register
ERRPIDR0: Peripheral Identification Register 0
ERRPIDR1: Peripheral Identification Register 1
ERRPIDR2: Peripheral Identification Register 2
ERRPIDR3: Peripheral Identification Register 3
ERRPIDR4: Peripheral Identification Register 4
GICC_ABPR: CPU Interface Aliased Binary Point Register
GICC_AEOIR: CPU Interface Aliased End Of Interrupt Register
GICC_AHPPIR: CPU Interface Aliased Highest Priority Pending Interrupt Register
GICC_AIAR: CPU Interface Aliased Interrupt Acknowledge Register
GICC_APR<n>: CPU Interface Active Priorities Registers
GICC_BPR: CPU Interface Binary Point Register
GICC_CTLR: CPU Interface Control Register
GICC_DIR: CPU Interface Deactivate Interrupt Register
GICC_EOIR: CPU Interface End Of Interrupt Register
GICC_HPPIR: CPU Interface Highest Priority Pending Interrupt Register
GICC_JAR: CPU Interface Interrupt Acknowledge Register
GICC_IIDR: CPU Interface Identification Register
GICC_NSAPR<n>: CPU Interface Non-secure Active Priorities Registers
GICC_PMR: CPU Interface Priority Mask Register
GICC_RPR: CPU Interface Running Priority Register
GICC_STATUSR: CPU Interface Status Register
GICD_CLR_SPI_NSR: Clear Non-secure SPI Pending Register
GICD_CLR_SPI_SR: Clear Secure SPI Pending Register
GICD_CPENDSGIR<n>: SGI Clear-Pending Registers
GICD_CCTRL: Distributor Control Register
GICD_ICACTIVER<n>: Interrupt Clear-Active Registers
GICD_ICACTIVER<n>E: Interrupt Clear-Active Registers (extended SPI range)
GICD_ICENABLER<n>: Interrupt Clear-Enable Registers
GICD_ICENABLER<n>E: Interrupt Clear-Enable Registers
GICD_ICFGR<n>: Interrupt Configuration Registers
GICD_ICFGR<n>E: Interrupt Configuration Registers (Extended SPI Range)
GICD_ICPENDR<n>: Interrupt Clear-Pending Registers
GICD_ICPENDR<n>E: Interrupt Clear-Pending Registers (extended SPI range)
GICD_IGROUPR<n>: Interrupt Group Registers
GICD_IGROUPR<n>E: Interrupt Group Registers (extended SPI range)
GICD_IGRPMODR<n>: Interrupt Group Modifier Registers
GICD_IGRPMODR<n>E: Interrupt Group Modifier Registers (extended SPI range)
GICD_IIDR: Distributor Implementer Identification Register
GICD_IPRIORITYR<n>: Interrupt Priority Registers
GICD_IPRIORITYR<n>E: Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.
GICD_IROUTER<n>: Interrupt Routing Registers
GICD_IROUTER<n>E: Interrupt Routing Registers (Extended SPI Range)
GICD_ISACTIVER<n>: Interrupt Set-Active Registers
GICD_ISACTIVER<n>E: Interrupt Set-Active Registers (extended SPI range)
GICD_ISENABLER<n>: Interrupt Set-Enable Registers
GICD_ISENABLER<n>E: Interrupt Set-Enable Registers
GICD_ISPENDR<n>: Interrupt Set-Pending Registers
GICD_ISPENDR<n>E: Interrupt Set-Pending Registers (extended SPI range)
GICD_ITARGETSR<n>: Interrupt Processor Targets Registers
GICD_NSACR<n>: Non-secure Access Control Registers
GICD_NSACR<n>E: Non-secure Access Control Registers
GICD_SETSPI_NSR: Set Non-secure SPI Pending Register
GICD_SETSPI_SR: Set Secure SPI Pending Register
GICD_SGIR: Software Generated Interrupt Register

External registers
GICD\_SPENDSGIR\(<n>\): SGI Set-Pending Registers
GICD\_STATUSR: Error Reporting Status Register
GICD\_TYPER: Interrupt Controller Type Register
GICD\_TYPER2: Interrupt Controller Type Register 2
GICD\_APR\(<n>\): Active Priorities Registers
GICD\_EISR: End Interrupt Status Register
GICD\_ELRSR: Empty List Register Status Register
GICD\_HCR: Hypervisor Control Register
GICD\_LR\(<n>\): List Registers
GICD\_MISR: Maintenance Interrupt Status Register
GICD\_VMCR: Virtual Machine Control Register
GICD\_VTR: Virtual Type Register
GICD\_CLRLPIR: Clear LPI Pending Register
GICD\_CTRLR: Redistributor Control Register
GICD\_ICACTIVER0: Interrupt Clear-Active Register 0
GICD\_ICACTIVER\(<n>E>\): Interrupt Clear-Active Registers
GICD\_ICENABLER0: Interrupt Clear-Enable Register 0
GICD\_ICENABLER\(<n>E>\): Interrupt Clear-Enable Registers
GICD\_ICFGR0: Interrupt Configuration Register 0
GICD\_ICFGR1: Interrupt Configuration Register 1
GICD\_ICFGR\(<n>E>\): Interrupt configuration registers
GICD\_ICPENDR0: Interrupt Clear-Pending Register 0
GICD\_ICPENDR\(<n>E>\): Interrupt Clear-Pending Registers
GICD\_IGROUPR0: Interrupt Group Register 0
GICD\_IGROUPR\(<n>E>\): Interrupt Group Registers
GICD\_IGRPMODR0: Interrupt Group Modifier Register 0
GICD\_IGRPMODR\(<n>E>\): Interrupt Group Modifier Registers
GICD\_IIDR: Redistributor Implementer Identification Register
GICD\_INVALLR: Redistributor Invalidate All Register
GICD\_INVLPIR: Redistributor Invalidate LPI Register
GICD\_IPRIORITYR\(<n>\): Interrupt Priority Registers
GICD\_IPRIORITYR\(<n>E>\): Interrupt Priority Registers (extended PPI range)
GICD\_ISACTIVER0: Interrupt Set-Active Register 0
GICD\_ISACTIVER\(<n>E>\): Interrupt Set-Active Registers
GICD\_ISENABLER0: Interrupt Set-Enable Register 0
GICD\_ISENABLER\(<n>E>\): Interrupt Set-Enable Registers
GICR_ISPENDR0: Interrupt Set-Pending Register 0
GICR_ISPENDR<n>E: Interrupt Set-Pending Registers
GICR_MPAMIDR: Report maximum PARTID and PMG Register
GICR_NSACR: Non-secure Access Control Register
GICR_PARTIDR: Set PARTID and PMG Register
GICR_PENDBASER: Redistributor LPI Pending Table Base Address Register
GICR_PROPBASER: Redistributor Properties Base Address Register
GICR_SETLPIR: Set LPI Pending Register
GICR_STATUSR: Error Reporting Status Register
GICR_SYNCR: Redistributor Synchronize Register
GICR_TYPER: Redistributor Type Register
GICR_VPENDBASER: Virtual Redistributor LPI Pending Table Base Address Register
GICR_VPROPBASER: Virtual Redistributor Properties Base Address Register
GICR_VSGIPENDR: Redistributor virtual SGI pending state register
GICR_VSGIR: Redistributor virtual SGI pending state request register
GICR_WAKER: Redistributor Wake Register
GICV_ABPR: Virtual Machine Aliased Binary Point Register
GICV_AEOIR: Virtual Machine Aliased End Of Interrupt Register
GICV_AHPPIR: Virtual Machine Aliased Highest Priority Pending Interrupt Register
GICV_AIAR: Virtual Machine Aliased Interrupt Acknowledge Register
GICV APR<n>: Virtual Machine Active Priorities Registers
GICV_BPR: Virtual Machine Binary Point Register
GICV_CTLR: Virtual Machine Control Register
GICV_DIR: Virtual Machine Deactivate Interrupt Register
GICV_EOIR: Virtual Machine End Of Interrupt Register
GICV_HPPIR: Virtual Machine Highest Priority Pending Interrupt Register
GICV_IAR: Virtual Machine Interrupt Acknowledge Register
GICV_IIDR: Virtual Machine CPU Interface Identification Register
GICV_PMR: Virtual Machine Priority Mask Register
GICV_RPR: Virtual Machine Running Priority Register
GICV_STATUSR: Virtual Machine Error Reporting Status Register
GITS_BASER<n>: ITS Translation Table Descriptors
GITS_CBASER: ITS Command Queue Descriptor
GITS_CREADR: ITS Read Register
GITS_CTLR: ITS Control Register
GITS_CWRITER: ITS Write Register
External registers

**GITS_IIDR**: ITS Identification Register

**GITS_MPAMIDR**: Report maximum PARTID and PMG Register

**GITS_MPIR**: Report ITS's affinity.

**GITS_PARTIDR**: Set PARTID and PMG Register

**GITS_SGIR**: ITS SGI Register

**GITS_STATUSR**: ITS Error Reporting Status Register

**GITS_TRANSLATER**: ITS Translation Register

**GITS_TYPER**: ITS Type Register

**GITS_UMSIR**: ITS Unmapped MSI register

**MIDR_EL1**: Main ID Register

**MPAMCFG_CMAX**: MPAM Cache Maximum Capacity Partition Configuration Register

**MPAMCFG_CPBM<n>**: MPAM Cache Portion Bitmap Partition Configuration Register

**MPAMCFG_INTPARTID**: MPAM Internal PARTID Narrowing Configuration Register

**MPAMCFG_MBW_MAX**: MPAM Memory Bandwidth Maximum Partition Configuration Register

**MPAMCFG_MBW_MIN**: MPAM Memory Bandwidth Minimum Partition Configuration Register

**MPAMCFG_MBW_PBM<n>**: MPAM Bandwidth Portion Bitmap Partition Configuration Register

**MPAMCFG_MBW_PROP**: MPAM Memory Bandwidth Proportional Stride Partition Configuration Register

**MPAMCFG_MBW_WINWD**: MPAM Memory Bandwidth Partitioning Window Width Configuration Register

**MPAMCFG_PART_SEL**: MPAM Partition Configuration Selection Register

**MPAMCFG_PRI**: MPAM Priority Partition Configuration Register

**MPAMF_AIDR**: MPAM Architecture Identification Register

**MPAMF_CCAP_IDR**: MPAM Features Cache Capacity Partitioning ID register

**MPAMF_CPOR_IDR**: MPAM Features Cache Portion Partitioning ID register

**MPAMF_CSUMON_IDR**: MPAM Features Cache Storage Usage Monitoring ID register

**MPAMF_ECR**: MPAM Error Control Register

**MPAMF_ESR**: MPAM Error Status Register

**MPAMF_IDR**: MPAM Features Identification Register

**MPAMF_IIDR**: MPAM Implementation Identification Register

**MPAMF_IMPL_IDR**: MPAM Implementation-Specific Partitioning Feature Identification Register

**MPAMF_MBWUMON_IDR**: MPAM Features Memory Bandwidth Usage Monitoring ID register

**MPAMF_MSMON_IDR**: MPAM Resource Monitoring Identification Register

**MPAMF_PARTID_NRW_IDR**: MPAM PARTID Narrowing ID register

**MPAMF_PRI_IDR**: MPAM Priority Partitioning Identification Register

**MPAMF_SIDR**: MPAM Features Secure Identification Register

**MSMON_CAPT_EVNT**: MPAM Capture Event Generation Register
External registers

- **MSMON_CFG_CSU_CTL**: MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register
- **MSMON_CFG_CSU_FLT**: MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register
- **MSMON_CFG_MBWU_CTL**: MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register
- **MSMON_CFG_MBWU_FLT**: MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register
- **MSMON_CFG_MON_SEL**: MPAM Monitor Instance Selection Register
- **MSMON_CSU**: MPAM Cache Storage Usage Monitor Register
- **MSMON_CSU_CAPTURE**: MPAM Cache Storage Usage Monitor Capture Register
- **MSMON_MBWU**: MPAM Memory Bandwidth Usage Monitor Register
- **MSMON_MBWU_CAPTURE**: MPAM Memory Bandwidth Usage Monitor Capture Register
- **MSMON_MBWU_L**: MPAM Long Memory Bandwidth Usage Monitor Register
- **MSMON_MBWU_L_CAPTURE**: MPAM Long Memory Bandwidth Usage Monitor Capture Register
- **OSLAR_EL1**: OS Lock Access Register
- **PMAUTHSTATUS**: Performance Monitors Authentication Status register
- **PMCCFILTR_EL0**: Performance Monitors Cycle Counter Filter Register
- **PMCCNTR_EL0**: Performance Monitors Cycle Counter
- **PMCEID0**: Performance Monitors Common Event Identification register 0
- **PMCEID1**: Performance Monitors Common Event Identification register 1
- **PMCEID2**: Performance Monitors Common Event Identification register 2
- **PMCEID3**: Performance Monitors Common Event Identification register 3
- **PMCFGR**: Performance Monitors Configuration Register
- **PMCID1SR**: CONTEXTIDR_EL1 Sample Register
- **PMCID2SR**: CONTEXTIDR_EL2 Sample Register
- **PMCIDR0**: Performance Monitors Component Identification Register 0
- **PMCIDR1**: Performance Monitors Component Identification Register 1
- **PMCIDR2**: Performance Monitors Component Identification Register 2
- **PMCIDR3**: Performance Monitors Component Identification Register 3
- **PMCNTENCLR_EL0**: Performance Monitors Count Enable Clear register
- **PMCNTENSET_EL0**: Performance Monitors Count Enable Set register
- **PMCR_EL0**: Performance Monitors Control Register
- **PMDEVAFF0**: Performance Monitors Device Affinity register 0
- **PMDEVAFF1**: Performance Monitors Device Affinity register 1
- **PMDEVARCH**: Performance Monitors Device Architecture register
- **PMDEVID**: Performance Monitors Device ID register
- **PMDEVTYPE**: Performance Monitors Device Type register
- **PMEVCNTR<n>_EL0**: Performance Monitors Event Count Registers
PMEVTYPER<n>_EL0: Performance Monitors Event Type Registers
PMINTENCLR_EL1: Performance Monitors Interrupt Enable Clear register
PMINTENSET_EL1: Performance Monitors Interrupt Enable Set register
PMITCTRL: Performance Monitors Integration mode Control register
PMLAR: Performance Monitors Lock Access Register
PMLSRS: Performance Monitors Lock Status Register
PMMIR: Performance Monitors Machine Identification Register
PMOVSCCLR_EL0: Performance Monitors Overflow Flag Status Clear register
PMOVSET_EL0: Performance Monitors Overflow Flag Status Set register
PMPCSR: Program Counter Sample Register
PMPI DRO: Performance Monitors Peripheral Identification Register 0
PMPI DR1: Performance Monitors Peripheral Identification Register 1
PMPI DR2: Performance Monitors Peripheral Identification Register 2
PMPI DR3: Performance Monitors Peripheral Identification Register 3
PMPI DR4: Performance Monitors Peripheral Identification Register 4
PMSWINC_EL0: Performance Monitors Software Increment register
PMVIDSR: VMID Sample Register
External register index by offset

Below are indexes for external registers in the following blocks:

- Debug
- PMU
- Timer
- GIC Distributor
- GIC Redistributor
- GIC Virtual CPU interface
- CTI
- GIC CPU interface
- GIC ITS control
- GIC Virtual interface control
- GIC ITS translation
- RAS
- AMU
- MPAM

In the **Debug** block:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x020</td>
<td>EDESR</td>
<td>External Debug Event Status Register</td>
</tr>
<tr>
<td>0x024</td>
<td>EDECR</td>
<td>External Debug Execution Control Register</td>
</tr>
<tr>
<td>0x030</td>
<td>EDWAR[31:0]</td>
<td>External Debug Watchpoint Address Register</td>
</tr>
<tr>
<td>0x034</td>
<td>EDWAR[63:32]</td>
<td>External Debug Watchpoint Address Register</td>
</tr>
<tr>
<td>0x080</td>
<td>DBGDTRRX_EL0</td>
<td>Debug Data Transfer Register, Receive</td>
</tr>
<tr>
<td>0x084</td>
<td>EDITR</td>
<td>External Debug Instruction Transfer Register</td>
</tr>
<tr>
<td>0x088</td>
<td>EDSCR</td>
<td>External Debug Status and Control Register</td>
</tr>
<tr>
<td>0x08C</td>
<td>DBGDTRTX_EL0</td>
<td>Debug Data Transfer Register, Transmit</td>
</tr>
<tr>
<td>0x090</td>
<td>EDRCR</td>
<td>External Debug Reserve Control Register</td>
</tr>
<tr>
<td>0x094</td>
<td>EDACR</td>
<td>External Debug Auxiliary Control Register</td>
</tr>
<tr>
<td>0x098</td>
<td>EDECCR</td>
<td>External Debug Exception Catch Control Register</td>
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<tr>
<td>0x0A0</td>
<td>EDPCSR[31:0]</td>
<td>External Debug Program Counter Sample Register</td>
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<tr>
<td>0x0A4</td>
<td>EDCISR</td>
<td>External Debug Context ID Sample Register</td>
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<td>0x0A8</td>
<td>EDVIDSR</td>
<td>External Debug Virtual Context Sample Register</td>
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<td>EDPCSR[63:32]</td>
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<tr>
<td>0x300</td>
<td>OSLAR_EL1</td>
<td>OS Lock Access Register</td>
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<tr>
<td>0x310</td>
<td>EDPBCR</td>
<td>External Debug Power/Reset Control Register</td>
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<tr>
<td>0x314</td>
<td>EDPRSR</td>
<td>External Debug Processor Status Register</td>
</tr>
<tr>
<td>0x400 + (16 * n)</td>
<td>DBGBVn&gt; EL1[63:0]</td>
<td>Debug Breakpoint Value Registers</td>
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<tr>
<td>0x408 + (16 * n)</td>
<td>DBGBCn&gt; EL1</td>
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<tr>
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<td>EDPFR[31:0]</td>
<td>External Debug Processor Feature Register</td>
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<td>EDDFR[63:32]</td>
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<td>External Debug Auxiliary Processor Feature Register</td>
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<td>External Debug Integration mode Control register</td>
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<td>DBGCLAIMSET_EL1</td>
<td>Debug CLAIM Tag Set register</td>
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<tr>
<td>0x0FA4</td>
<td>DBGCLAIMCLR_EL1</td>
<td>Debug CLAIM Tag Clear register</td>
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### External register index by offset

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<td>EDDEVAFF1</td>
<td>External Debug Device Affinity register 1</td>
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<td>EDLAR</td>
<td>External Debug Lock Access Register</td>
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<td>EDLSR</td>
<td>External Debug Lock Status Register</td>
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<td>Debug Authentication Status register</td>
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<tr>
<td>0xFBC</td>
<td>EDDEVARCH</td>
<td>External Debug Device Architecture register</td>
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<td>External Debug Device ID register 0</td>
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### In the PMU block:

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<td>Performance Monitors Event Count Registers</td>
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<td>PMCCNTR_EL0[31:0]</td>
<td>Performance Monitors Cycle Counter</td>
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<td>0x0FC</td>
<td>PMCCNTR_EL0[63:32]</td>
<td>Performance Monitors Cycle Counter</td>
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<td>PMPCSR[63:32]</td>
<td>Program Counter Sample Register</td>
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<td>PMCID1SR</td>
<td>CONTEXTIDR_EL1 Sample Register</td>
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<td>PMVIDSR</td>
<td>VMID Sample Register</td>
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<tr>
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<td>PMCNTENCLR_EL0</td>
<td>Performance Monitors Count Enable Clear register</td>
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<td>PMSWINC_EL0</td>
<td>Performance Monitors Software Increment register</td>
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<td>PMOVSSSET_EL0</td>
<td>Performance Monitors Overflow Flag Status Set register</td>
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<td>PMCFGFR</td>
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<td>PMCR_EL0</td>
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<td>Performance Monitors Common Event Identification register 0</td>
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<td>Performance Monitors Common Event Identification register 1</td>
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<tr>
<td>Offset</td>
<td>Name</td>
<td>Description</td>
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<td>PMLSRS</td>
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<td>PMDEVAUNCH</td>
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<td>PMCIDR0</td>
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<td>PMCIDR3</td>
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In the Timer block:

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<th>Description</th>
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<td>CNTBaseN</td>
<td>0x000</td>
<td>CNTPCT[31:0]</td>
<td>Counter-timer Physical Count</td>
</tr>
<tr>
<td>CNTBaseN</td>
<td>0x004</td>
<td>CNTPCT[63:32]</td>
<td>Counter-timer Physical Count</td>
</tr>
<tr>
<td>CNTBaseN</td>
<td>0x008</td>
<td>CNTVCT[31:0]</td>
<td>Counter-timer Virtual Count</td>
</tr>
<tr>
<td>CNTBaseN</td>
<td>0x00C</td>
<td>CNTVCT[63:32]</td>
<td>Counter-timer Virtual Count</td>
</tr>
<tr>
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<td>CNTFRQ</td>
<td>Counter-timer Frequency</td>
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<td>CNTBaseN</td>
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<td>CNTEL0ACR</td>
<td>Counter-timer EL0 Access Control Register</td>
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<td>Counter-timer Virtual Offset</td>
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<td>CNTVOFF[63:32]</td>
<td>Counter-timer Virtual Offset</td>
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<td>CNTP_CVAL[31:0]</td>
<td>Counter-timer Physical Timer CompareValue</td>
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<td>CNTP_CVAL[63:32]</td>
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<td>CNTV_CTL</td>
<td>Counter-timer Virtual Timer Control</td>
</tr>
<tr>
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<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
<td>Counter ID registers</td>
</tr>
<tr>
<td>CNTCTLBase</td>
<td>0x000</td>
<td>CNTFRQ</td>
<td>Counter-timer Frequency</td>
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</table>
### External register index by offset

<table>
<thead>
<tr>
<th>Frame</th>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTCTLBase</td>
<td>0x004</td>
<td>CNTNSAR</td>
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<td>Counter ID registers</td>
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<td>CNTP_CVAL[63:32]</td>
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<td>Counter-timer Frequency</td>
</tr>
<tr>
<td>CNTControlBase</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
<td>Counter ID registers</td>
</tr>
<tr>
<td>CNTReadBase</td>
<td>0x000</td>
<td>CNTCV[63:0]</td>
<td>Counter Count Value register</td>
</tr>
<tr>
<td>CNTReadBase</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
<td>Counter ID registers</td>
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### In the GIC Distributor block:

<table>
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<tr>
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<th>Description</th>
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<tbody>
<tr>
<td>0x0000</td>
<td>GICD_CTRL</td>
<td>Distributor Control Register</td>
</tr>
<tr>
<td>0x0004</td>
<td>GICD_TYPER</td>
<td>Interrupt Controller Type Register</td>
</tr>
<tr>
<td>0x0008</td>
<td>GICD_IIDR</td>
<td>Distributor Implementer Identification Register</td>
</tr>
<tr>
<td>0x000C</td>
<td>GICD_TYPER2</td>
<td>Interrupt Controller Type Register 2</td>
</tr>
<tr>
<td>0x0010</td>
<td>GICD_STATUSR</td>
<td>Error Reporting Status Register</td>
</tr>
<tr>
<td>0x0010</td>
<td>GICD_STATUSR</td>
<td>Error Reporting Status Register</td>
</tr>
<tr>
<td>0x0040</td>
<td>GICD_SETSPI_NS</td>
<td>Set Non-secure SPI Pending Register</td>
</tr>
<tr>
<td>0x0048</td>
<td>GICD_CLRSPI_NS</td>
<td>Clear Non-secure SPI Pending Register</td>
</tr>
<tr>
<td>0x0050</td>
<td>GICD_SETSPI_SR</td>
<td>Set Secure SPI Pending Register</td>
</tr>
<tr>
<td>0x0058</td>
<td>GICD_CLRSPI_SR</td>
<td>Clear Secure SPI Pending Register</td>
</tr>
</tbody>
</table>

| 0x0080 + (4 * n) | GICD_IGROUPR<n> | Interrupt Group Registers |

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<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0100 + (4 * n)</td>
<td>GICD_ISENABLER&lt;n&gt;</td>
<td>Interrupt Set-Enable Registers</td>
</tr>
<tr>
<td>0x0180 + (4 * n)</td>
<td>GICD_ICENABLEL&lt;n&gt;</td>
<td>Interrupt Clear-Enable Registers</td>
</tr>
<tr>
<td>0x0200 + (4 * n)</td>
<td>GICD_ICPENDR&lt;n&gt;</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>0x0280 + (4 * n)</td>
<td>GICD_ISACTIVER&lt;n&gt;</td>
<td>Interrupt Set-Active Registers</td>
</tr>
<tr>
<td>0x0300 + (4 * n)</td>
<td>GICD_ICPENDR&lt;n&gt;</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>0x0380 + (4 * n)</td>
<td>GICD_ICACTIVER&lt;n&gt;</td>
<td>Interrupt Clear-Active Registers</td>
</tr>
<tr>
<td>0x0400 + (4 * n)</td>
<td>GICD_IPRIORITYR&lt;n&gt;</td>
<td>Interrupt Priority Registers</td>
</tr>
<tr>
<td>0x0800 + (4 * n)</td>
<td>GICD_ITARGETSR&lt;n&gt;</td>
<td>Interrupt Processor Targets Registers</td>
</tr>
<tr>
<td>0x0C00 + (4 * n)</td>
<td>GICD_ICFGR&lt;n&gt;</td>
<td>Interrupt Configuration Registers</td>
</tr>
<tr>
<td>0x0D00 + (4 * n)</td>
<td>GICD_IGRPMODR&lt;n&gt;</td>
<td>Interrupt Group Modifier Registers</td>
</tr>
<tr>
<td>0x0E00 + (4 * n)</td>
<td>GICD_NSACR&lt;n&gt;</td>
<td>Non-secure Access Control Registers</td>
</tr>
<tr>
<td>0x0F00</td>
<td>GICD_SGIR</td>
<td>Software Generated Interrupt Register</td>
</tr>
<tr>
<td>0x0F10 + (4 * n)</td>
<td>GICD_CPENDSGIR&lt;n&gt;</td>
<td>SGI Clear-Pending Registers</td>
</tr>
<tr>
<td>0x0F20 + (4 * n)</td>
<td>GICD_SPENDSGIR&lt;n&gt;</td>
<td>SGI Set-Pending Registers</td>
</tr>
<tr>
<td>0x1000 + (4 * n)</td>
<td>GICD_ICGROUPR&lt;n&gt;E</td>
<td>Interrupt Group Registers (extended SPI range)</td>
</tr>
<tr>
<td>0x1200 + (4 * n)</td>
<td>GICD_ISENABLER&lt;n&gt;E</td>
<td>Interrupt Set-Enable Registers</td>
</tr>
<tr>
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<td>GICD_ICENABLEL&lt;n&gt;E</td>
<td>Interrupt Clear-Enable Registers</td>
</tr>
<tr>
<td>0x1600 + (4 * n)</td>
<td>GICD_ICPENDR&lt;n&gt;E</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>0x1800 + (4 * n)</td>
<td>GICD_ICPENRD&lt;n&gt;E</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>0x1A00 + (4 * n)</td>
<td>GICD_ISACTIVER&lt;n&gt;E</td>
<td>Interrupt Set-Active Registers</td>
</tr>
<tr>
<td>0x1C00 + (4 * n)</td>
<td>GICD_ICACTIVER&lt;n&gt;E</td>
<td>Interrupt Clear-Active Registers</td>
</tr>
<tr>
<td>0x2000 + (4 * n)</td>
<td>GICD_IPRIORITYR&lt;n&gt;E</td>
<td>Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.</td>
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<tr>
<td>0x3000 + (4 * n)</td>
<td>GICD_ICFGR&lt;n&gt;E</td>
<td>Interrupt Configuration Registers (Extended SPI Range)</td>
</tr>
<tr>
<td>0x3400 + (4 * n)</td>
<td>GICD_IGRPMODR&lt;n&gt;E</td>
<td>Interrupt Group Modifier Registers (extended SPI range)</td>
</tr>
<tr>
<td>0x3600 + (4 * n)</td>
<td>GICD_NSACR&lt;n&gt;E</td>
<td>Non-secure Access Control Registers</td>
</tr>
<tr>
<td>0x6000 + (8 * n)</td>
<td>GICD_IROUTER&lt;n&gt;</td>
<td>Interrupt Routing Registers</td>
</tr>
<tr>
<td>0x8000 + (8 * n)</td>
<td>GICD_IROUTER&lt;n&gt;E</td>
<td>Interrupt Routing Registers (Extended SPI Range)</td>
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In the GIC Redistributor block:

<table>
<thead>
<tr>
<th>Frame</th>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
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</thead>
<tbody>
<tr>
<td>RD base</td>
<td>0x0000</td>
<td>GICR_CTLR</td>
<td>Redistributor Control Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0004</td>
<td>GICR_IIDR</td>
<td>Redistributor Implementer Identification Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0008</td>
<td>GICR_TYPER</td>
<td>Redistributor Type Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0010</td>
<td>GICR_STATUSR</td>
<td>Error Reporting Status Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0010</td>
<td>GICR_STATUSR</td>
<td>Error Reporting Status Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0014</td>
<td>GICR_WAKER</td>
<td>Redistributor Wake Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0018</td>
<td>GICR_MPAMIDR</td>
<td>Report maximum PARTID and PMG Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x001C</td>
<td>GICR_PARTIDR</td>
<td>Set PARTID and PMG Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0040</td>
<td>GICR_SETLPIR</td>
<td>Set LPI Pending Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0048</td>
<td>GICR_CLRLPIR</td>
<td>Clear LPI Pending Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0070</td>
<td>GICR_PROPBASER</td>
<td>Redistributor Properties Base Address Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x0078</td>
<td>GICR_PENDBASER</td>
<td>Redistributor LPI Pending Table Base Address Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x00A0</td>
<td>GICR_INVLPIR</td>
<td>Redistributor Invalidate LPI Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x00B0</td>
<td>GICR_INVALLR</td>
<td>Redistributor Invalidate All Register</td>
</tr>
<tr>
<td>RD base</td>
<td>0x00C0</td>
<td>GICR_SYNCR</td>
<td>Redistributor Synchronize Register</td>
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</table>
## GIC Base Registers

<table>
<thead>
<tr>
<th>Frame</th>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SGI_base</td>
<td>0x0080</td>
<td>GICR_GROUPR0</td>
<td>Interrupt Group Register 0</td>
</tr>
<tr>
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<td>0x0080 + (4 * n)</td>
<td>GICR_GROUPR&lt;n&gt;E</td>
<td>Interrupt Group Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0100</td>
<td>GICR_ISENABLER0</td>
<td>Interrupt Set-Enable Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0100 + (4 * n)</td>
<td>GICR_ISENABLER&lt;n&gt;E</td>
<td>Interrupt Set-Enable Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0180</td>
<td>GICR_ICENABLER0</td>
<td>Interrupt Clear-Enable Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0180 + (4 * n)</td>
<td>GICR_ICENABLER&lt;n&gt;E</td>
<td>Interrupt Clear-Enable Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0200</td>
<td>GICR_ISPENDR0</td>
<td>Interrupt Set-Pending Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0200 + (4 * n)</td>
<td>GICR_ISPENDR&lt;n&gt;E</td>
<td>Interrupt Set-Pending Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0280</td>
<td>GICR_ICPENDR0</td>
<td>Interrupt Clear-Pending Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0280 + (4 * n)</td>
<td>GICR_ICPENDR&lt;n&gt;E</td>
<td>Interrupt Clear-Pending Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0300</td>
<td>GICR_ISACTIVER0</td>
<td>Interrupt Set-Active Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0300 + (4 * n)</td>
<td>GICR_ISACTIVER&lt;n&gt;E</td>
<td>Interrupt Set-Active Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0380</td>
<td>GICR_ICACTIVER0</td>
<td>Interrupt Clear-Active Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0380 + (4 * n)</td>
<td>GICR_ICACTIVER&lt;n&gt;E</td>
<td>Interrupt Clear-Active Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0400 + (4 * n)</td>
<td>GICR_IPRIORITYR&lt;n&gt;E</td>
<td>Interrupt Priority Registers (extended PPI range)</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x0400 + (4 * n)</td>
<td>GICR_IPRIORITYR&lt;n&gt;</td>
<td>Interrupt Priority Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00C0</td>
<td>GICR_ICFRG0</td>
<td>Interrupt Configuration Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00C0 + (4 * n)</td>
<td>GICR_ICFRG&lt;n&gt;E</td>
<td>Interrupt configuration registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00C4</td>
<td>GICR_ICFRG1</td>
<td>Interrupt Configuration Register 1</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00D0</td>
<td>GICR_IGRPMODR0</td>
<td>Interrupt Group Modifier Register 0</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00D0 + (4 * n)</td>
<td>GICR_IGRPMODR&lt;n&gt;E</td>
<td>Interrupt Group Modifier Registers</td>
</tr>
<tr>
<td>SGI_base</td>
<td>0x00E0</td>
<td>GICR_NSACR</td>
<td>Non-secure Access Control Register</td>
</tr>
<tr>
<td>VLPI_base</td>
<td>0x0070</td>
<td>GICR_VPROPBASER</td>
<td>Virtual Redistributor Properties Base Address Register</td>
</tr>
<tr>
<td>VLPI_base</td>
<td>0x0078</td>
<td>GICR_VPENDBASE</td>
<td>Virtual Redistributor LPI Pending Table Base Address Register</td>
</tr>
<tr>
<td>VLPI_base</td>
<td>0x0080</td>
<td>GICR_VSGIR</td>
<td>Redistributor virtual SGI pending state request register</td>
</tr>
<tr>
<td>VLPI_base</td>
<td>0x0088</td>
<td>GICR_VSGIPENDR</td>
<td>Redistributor virtual SGI pending state register</td>
</tr>
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</table>

### In the GIC Virtual CPU interface block:

<table>
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<tr>
<th>Offset</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>GICV_CTLR</td>
<td>Virtual Machine Control Register</td>
</tr>
<tr>
<td>0x0004</td>
<td>GICV_PMR</td>
<td>Virtual Machine Priority Mask Register</td>
</tr>
<tr>
<td>0x0008</td>
<td>GICV_BPR</td>
<td>Virtual Machine Binary Point Register</td>
</tr>
<tr>
<td>0x00C0</td>
<td>GICV_IAR</td>
<td>Virtual Machine Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>0x0010</td>
<td>GICV_EOIR</td>
<td>Virtual Machine End Of Interrupt Register</td>
</tr>
<tr>
<td>0x0014</td>
<td>GICV_RPR</td>
<td>Virtual Machine Running Priority Register</td>
</tr>
<tr>
<td>0x0018</td>
<td>GICV_HPPIR</td>
<td>Virtual Machine Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>0x001C</td>
<td>GICV_ABPR</td>
<td>Virtual Machine Aliased Binary Point Register</td>
</tr>
<tr>
<td>0x0020</td>
<td>GICV_AIAR</td>
<td>Virtual Machine Aliased Interrupt Acknowledge Register</td>
</tr>
<tr>
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<td>GICV_AEOIR</td>
<td>Virtual Machine Aliased End Of Interrupt Register</td>
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<tr>
<td>0x0028</td>
<td>GICV_AHPPR</td>
<td>Virtual Machine Aliased Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>0x002C</td>
<td>GICV_STATUSR</td>
<td>Virtual Machine Error Reporting Status Register</td>
</tr>
<tr>
<td>0x00D0 + (4 * n)</td>
<td>GICV_APR&lt;n&gt;</td>
<td>Virtual Machine Active Priorities Registers</td>
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<tr>
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<td>GICV_IHDR</td>
<td>Virtual Machine CPU Interface Identification Register</td>
</tr>
<tr>
<td>0x1000</td>
<td>GICV_DIR</td>
<td>Virtual Machine Deactivate Interrupt Register</td>
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### In the CTI block:

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<th>Name</th>
<th>Description</th>
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<tbody>
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<td>CTICONTROL</td>
<td>CTI Control register</td>
</tr>
<tr>
<td>0x010</td>
<td>CTIINTACK</td>
<td>CTI Output Trigger Acknowledge register</td>
</tr>
<tr>
<td>0x014</td>
<td>CTIAPPSET</td>
<td>CTI Application Trigger Set register</td>
</tr>
<tr>
<td>0x018</td>
<td>CTIAPPCLEAR</td>
<td>CTI Application Trigger Clear register</td>
</tr>
<tr>
<td>0x01C</td>
<td>CTIAPPPULSE</td>
<td>CTI Application Pulse register</td>
</tr>
<tr>
<td>0x020 + (4 * n)</td>
<td>CTIINEN&lt;n&gt;</td>
<td>CTI Input Trigger to Output Channel Enable registers</td>
</tr>
<tr>
<td>0x0A0 + (4 * n)</td>
<td>CTIOUTEN&lt;n&gt;</td>
<td>CTI Input Channel to Output Trigger Enable registers</td>
</tr>
<tr>
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<td>CTI Trigger In Status register</td>
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<tr>
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<td>CTITRIGOUTSTATUS</td>
<td>CTI Trigger Out Status register</td>
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<tr>
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<td>CTICHINSTATUS</td>
<td>CTI Channel In Status register</td>
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<td>CTICHOUTSTATUS</td>
<td>CTI Channel Out Status register</td>
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<td>CTIGATE</td>
<td>CTI Channel Gate Enable register</td>
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<td>ASICCTL</td>
<td>CTI External Multiplexer Control register</td>
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<tr>
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<td>CTIDEVCTRL</td>
<td>CTI Device Control register</td>
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<tr>
<td>0x154</td>
<td>CTITCTRL</td>
<td>CTI Integration mode Control register</td>
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<td>CTICLAIMSET</td>
<td>CTI CLAIM Tag Set register</td>
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<td>CTICLAIMCLR</td>
<td>CTI CLAIM Tag Clear register</td>
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<td>CTIDEVAFF0</td>
<td>CTI Device Affinity register 0</td>
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<td>CTIDEVAFF1</td>
<td>CTI Device Affinity register 1</td>
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<td>CTI Lock Access Register</td>
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<td>CTILSR</td>
<td>CTI Lock Status Register</td>
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<td>CTI Authentication Status register</td>
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<td>CTI Device ID register 0</td>
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<td>CTIDEVTYPE</td>
<td>CTI Device Type register</td>
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<td>CTI Peripheral Identification Register 1</td>
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<td>CTI Peripheral Identification Register 3</td>
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<td>CTI Component Identification Register 1</td>
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<td>CTICIDR2</td>
<td>CTI Component Identification Register 2</td>
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<tr>
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<td>CTICIDR3</td>
<td>CTI Component Identification Register 3</td>
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### In the GIC CPU interface block:

<table>
<thead>
<tr>
<th>Offset</th>
<th>Name</th>
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<tbody>
<tr>
<td>0x0000</td>
<td>GICC_CTRL</td>
<td>CPU Interface Control Register</td>
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<tr>
<td>0x0004</td>
<td>GICC_PMR</td>
<td>CPU Interface Priority Mask Register</td>
</tr>
<tr>
<td>0x0008</td>
<td>GICC_BPR</td>
<td>CPU Interface Binary Point Register</td>
</tr>
<tr>
<td>0x000C</td>
<td>GICC_IAR</td>
<td>CPU Interface Interrupt Acknowledge Register</td>
</tr>
<tr>
<td>0x0010</td>
<td>GICC_EOIR</td>
<td>CPU Interface End Of Interrupt Register</td>
</tr>
<tr>
<td>0x0014</td>
<td>GICC_RPR</td>
<td>CPU Interface Running Priority Register</td>
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<tr>
<td>0x0018</td>
<td>GICC_HPPIR</td>
<td>CPU Interface Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>Offset</td>
<td>Name</td>
<td>Description</td>
</tr>
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<tr>
<td>0x001C</td>
<td>GICC_ABPR</td>
<td>CPU Interface Aliased Binary Point Register</td>
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<tr>
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<td>GICC_AIAR</td>
<td>CPU Interface Aliased Interrupt Acknowledge Register</td>
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<td>GICC_AEOIR</td>
<td>CPU Interface Aliased End Of Interrupt Register</td>
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<td>0x0028</td>
<td>GICC_AHPPIR</td>
<td>CPU Interface Aliased Highest Priority Pending Interrupt Register</td>
</tr>
<tr>
<td>0x002C</td>
<td>GICC_STATUSR</td>
<td>CPU Interface Status Register</td>
</tr>
<tr>
<td>0x002C</td>
<td>GICC_STATUSR</td>
<td>CPU Interface Status Register</td>
</tr>
<tr>
<td>0x00D0 + (4 * n)</td>
<td>GICC_APR&lt;n&gt;</td>
<td>CPU Interface Active Priorities Registers</td>
</tr>
<tr>
<td>0x00E0 + (4 * n)</td>
<td>GICC_NSAPR&lt;n&gt;</td>
<td>CPU Interface Non-secure Active Priorities Registers</td>
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<tr>
<td>0x00FC</td>
<td>GICC_DIR</td>
<td>CPU Interface Deactivate Interrupt Register</td>
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In the GIC ITS control block:

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<tr>
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<td>GITS_CTLR</td>
<td>ITS Control Register</td>
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<tr>
<td>0x0004</td>
<td>GITS_IIDR</td>
<td>ITS Identification Register</td>
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<tr>
<td>0x0008</td>
<td>GITS_TYPER</td>
<td>ITS Type Register</td>
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<tr>
<td>0x0010</td>
<td>GITS_MPAIDR</td>
<td>Report maximum PARTID and PMG Register</td>
</tr>
<tr>
<td>0x0014</td>
<td>GITS_PARTIDR</td>
<td>Set PARTID and PMG Register</td>
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<tr>
<td>0x0018</td>
<td>GITS_MPIDR</td>
<td>Report ITS’s affinity.</td>
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<tr>
<td>0x0020</td>
<td>GITS_STATUSR</td>
<td>ITS Error Reporting Status Register</td>
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<tr>
<td>0x0028</td>
<td>GITS_UMSIR</td>
<td>ITS Unmapped MSI register</td>
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<tr>
<td>0x0080</td>
<td>GITS_CBASER</td>
<td>ITS Command Queue Descriptor</td>
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<tr>
<td>0x0088</td>
<td>GITS_CWRITER</td>
<td>ITS Write Register</td>
</tr>
<tr>
<td>0x0090</td>
<td>GITS_CREADR</td>
<td>ITS Read Register</td>
</tr>
<tr>
<td>0x0100 + (8 * n)</td>
<td>GITS_BASER&lt;n&gt;</td>
<td>ITS Translation Table Descriptors</td>
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<td>GITS_SGIR</td>
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In the GIC Virtual interface control block:

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<td>GICH_HCR</td>
<td>Hypervisor Control Register</td>
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<tr>
<td>0x0004</td>
<td>GICH_VTR</td>
<td>Virtual Type Register</td>
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<td>0x0008</td>
<td>GICH_VMCR</td>
<td>Virtual Machine Control Register</td>
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<td>GICH_MISR</td>
<td>Maintenance Interrupt Status Register</td>
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<td>GICH_EISR</td>
<td>End Interrupt Status Register</td>
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<td>GICH_ELRSR</td>
<td>Empty List Register Status Register</td>
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<td>GICH_APR&lt;n&gt;</td>
<td>Active Priorities Registers</td>
</tr>
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<td>0x0100 + (4 * n)</td>
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In the GIC ITS translation block:

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<td>GITS_TRANSLATER</td>
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In the RAS block:

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<td>0x0000 + (64 * n)</td>
<td>ERR&lt;n&gt;FR</td>
<td>Error Record Feature Register</td>
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</table>
### External register index by offset

<table>
<thead>
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<th>Name</th>
<th>Description</th>
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<tr>
<td>0x008 + (64 * n)</td>
<td>ERR&lt;n&gt;CTRL</td>
<td>Error Record Control Register</td>
</tr>
<tr>
<td>0x010 + (64 * n)</td>
<td>ERR&lt;n&gt;STATUS</td>
<td>Error Record Primary Status Register</td>
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<tr>
<td>0x018 + (64 * n)</td>
<td>ERR&lt;n&gt;ADDR</td>
<td>Error Record Address Register</td>
</tr>
<tr>
<td>0x020 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC0</td>
<td>Error Record Miscellaneous Register 0</td>
</tr>
<tr>
<td>0x028 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC1</td>
<td>Error Record Miscellaneous Register 1</td>
</tr>
<tr>
<td>0x030 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC2</td>
<td>Error Record Miscellaneous Register 2</td>
</tr>
<tr>
<td>0x038 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC3</td>
<td>Error Record Miscellaneous Register 3</td>
</tr>
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<td>0x800 + (64 * n)</td>
<td>ERR&lt;n&gt;PFGF</td>
<td>Pseudo-fault Generation Feature Register</td>
</tr>
<tr>
<td>0x800 + (8 * n)</td>
<td>ERRIMPDEF&lt;n&gt;</td>
<td>IMPLEMENTATION DEFINED Register &lt;n&gt;</td>
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<tr>
<td>0x808 + (64 * n)</td>
<td>ERR&lt;n&gt;PFGCTL</td>
<td>Pseudo-fault Generation Control Register</td>
</tr>
<tr>
<td>0x810 + (64 * n)</td>
<td>ERR&lt;n&gt;PFGCDN</td>
<td>Pseudo-fault Generation Countdown Register</td>
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<tr>
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<td>ERRGSR</td>
<td>Error Group Status Register</td>
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<td>0xE10</td>
<td>ERRIIDR</td>
<td>Implementation Identification Register</td>
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<tr>
<td>0xE80</td>
<td>ERRFHIICR0</td>
<td>Fault Handling Interrupt Configuration Register 0</td>
</tr>
<tr>
<td>0xE80 + (8 * n)</td>
<td>ERRIROCR&lt;n&gt;</td>
<td>Generic Error Interrupt Configuration Register</td>
</tr>
<tr>
<td>0xE88</td>
<td>ERRFHIICR1</td>
<td>Fault Handling Interrupt Configuration Register 1</td>
</tr>
<tr>
<td>0xE8C</td>
<td>ERRFHIICR2</td>
<td>Fault Handling Interrupt Configuration Register 2</td>
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<td>ERRERICR0</td>
<td>Error Recovery Interrupt Configuration Register 0</td>
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<tr>
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<td>ERRERICR1</td>
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<td>ERRERICR2</td>
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<td>ERRCRCR0</td>
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<tr>
<td>0xEA8</td>
<td>ERRCRCR1</td>
<td>Critical Error Interrupt Configuration Register 1</td>
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<tr>
<td>0xEAC</td>
<td>ERRCRCR2</td>
<td>Critical Error Interrupt Configuration Register 2</td>
</tr>
<tr>
<td>0xEF8</td>
<td>ERRIRQSR</td>
<td>Error Interrupt Status Register</td>
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<tr>
<td>0xFA8</td>
<td>ERREDEVAFR</td>
<td>Device Affinity Register</td>
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<tr>
<td>0xFBC</td>
<td>ERREDEVARCH</td>
<td>Device Architecture Register</td>
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<tr>
<td>0xFC8</td>
<td>ERRDEVID</td>
<td>Device Configuration Register</td>
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<td>0xFD0</td>
<td>ERPPIDR4</td>
<td>Peripheral Identification Register 4</td>
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<td>0xFE0</td>
<td>ERPPIDR0</td>
<td>Peripheral Identification Register 0</td>
</tr>
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<td>0xFE4</td>
<td>ERPPIDR1</td>
<td>Peripheral Identification Register 1</td>
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<td>0xFE8</td>
<td>ERPPIDR2</td>
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<td>ERPPIDR3</td>
<td>Peripheral Identification Register 3</td>
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<td>0xFF0</td>
<td>ERRCIDR0</td>
<td>Component Identification Register 0</td>
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<tr>
<td>0xFF4</td>
<td>ERRCIDR1</td>
<td>Component Identification Register 1</td>
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<td>ERRCIDR2</td>
<td>Component Identification Register 2</td>
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<tr>
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<td>ERRCIDR3</td>
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### In the AMU block:

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<tr>
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<th>Name</th>
<th>Description</th>
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<tbody>
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<td>0x000 + (8 * n)</td>
<td>AMEVCNTR0&lt;n&gt;[31:0]</td>
<td>Activity Monitors Event Counter Registers 0</td>
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<td>AMEVCNTR0&lt;n&gt;[63:32]</td>
<td>Activity Monitors Event Counter Registers 0</td>
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<td>Activity Monitors Event Counter Registers 1</td>
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<td>Activity Monitors Event Type Registers 0</td>
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<td>AMCNTENSET1</td>
<td>Activity Monitors Count Enable Set Register 1</td>
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<tr>
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<td>AMCNTENCLR0</td>
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### In the MPAM block:

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<th>Offset</th>
<th>Name</th>
<th>Description</th>
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<tbody>
<tr>
<td>MPAMF_BASE_ns</td>
<td>0x0000</td>
<td>MPAMF_IDR</td>
<td>MPAM Features Identification Register</td>
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<tr>
<td>MPAMF_BASE_ns</td>
<td>0x0018</td>
<td>MPAMF_IIDR</td>
<td>MPAM Implementation Identification Register</td>
</tr>
<tr>
<td>MPAMF_BASE_ns</td>
<td>0x0020</td>
<td>MPAMF_AIDR</td>
<td>MPAM Architecture Identification Register</td>
</tr>
<tr>
<td>MPAMF_BASE_ns</td>
<td>0x0028</td>
<td>MPAMF_IMPL_IDR</td>
<td>MPAM Implementation-Specific Partitioning Feature Identification Register</td>
</tr>
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<td>MPAMF_CPOR_IDR</td>
<td>MPAM Features Cache Portion Partitioning ID register</td>
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<td>MPAMF_CCAP_IDR</td>
<td>MPAM Features Cache Capacity Partitioning ID register</td>
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<tr>
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<td>MPAMF_MBW_IDR</td>
<td>MPAM Memory Bandwidth Partitioning Identification Register</td>
</tr>
<tr>
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<td>MPAMF_PRI_IDR</td>
<td>MPAM Priority Partitioning Identification Register</td>
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<td>MPAM PARTID Narrowing ID register</td>
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<td>MPAM Resource Monitoring Identification Register</td>
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<td>MPAMF_CSUMON_IDR</td>
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<td>Offset</td>
<td>Name</td>
<td>Description</td>
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<td>MPAM Cache Portion Bitmap Partition Configuration Register</td>
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<tr>
<td>Frame</td>
<td>Offset</td>
<td>Name</td>
<td>Description</td>
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</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0030</td>
<td>MPAMF_CPOR_IDR</td>
<td>MPAM Features Cache Portion Partitioning ID register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0038</td>
<td>MPAMF_CCAP_IDR</td>
<td>MPAM Features Cache Capacity Partitioning ID register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0040</td>
<td>MPAMF_MBW_IDR</td>
<td>MPAM Memory Bandwidth Partitioning Identification Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0048</td>
<td>MPAMF_PRI_IDR</td>
<td>MPAM Priority Partitioning Identification Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0050</td>
<td>MPAMF_PARTID_NRW_IDR</td>
<td>MPAM PARTID Narrowing ID register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0080</td>
<td>MPAMF_MSMON_IDR</td>
<td>MPAM Resource Monitoring Identification Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0088</td>
<td>MPAMF_CSUMON_IDR</td>
<td>MPAM Features Cache Storage Usage Monitoring ID register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0090</td>
<td>MPAMF_MBWUMON_IDR</td>
<td>MPAM Features Memory Bandwidth Usage Monitoring ID register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x00F0</td>
<td>MPAMF_ECR</td>
<td>MPAM Error Control Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x00F8</td>
<td>MPAMF_ESR</td>
<td>MPAM Error Status Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0100</td>
<td>MPAMCFG_PART_SEL</td>
<td>MPAM Partition Configuration Selection Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0108</td>
<td>MPAMCFG_CMAX</td>
<td>MPAM Cache Maximum Capacity Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0200</td>
<td>MPAMCFG_MBW_MIN</td>
<td>MPAM Memory Bandwidth Minimum Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0208</td>
<td>MPAMCFG_MBW_MAX</td>
<td>MPAM Memory Bandwidth Maximum Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0220</td>
<td>MPAMCFG_MBW_WINWD</td>
<td>MPAM Memory Bandwidth Partitioning Window Width Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0400</td>
<td>MPAMCFG_PRI</td>
<td>MPAM Priority Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0500</td>
<td>MPAMCFG_MBW_PROP</td>
<td>MPAM Memory Bandwidth Proportional Stride Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0600</td>
<td>MPAMCFG_INTPARTID</td>
<td>MPAM Internal PARTID Narrowing Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0800</td>
<td>MSMON_CFG_MON_SEL</td>
<td>MPAM Monitor Instance Selection Register</td>
</tr>
<tr>
<td>Frame</td>
<td>Offset</td>
<td>Name</td>
<td>Description</td>
</tr>
<tr>
<td>------------------</td>
<td>-------------------</td>
<td>-----------------------------</td>
<td>---------------------------------------------------------------</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0808</td>
<td>MS.MON.CapT.EvNT</td>
<td>MPAM Capture Event Generation Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0810</td>
<td>MS.MON_CFG_CSU_FLT</td>
<td>MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0818</td>
<td>MS.MON_CFG_CSU_CTL</td>
<td>MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0820</td>
<td>MS.MON_CFG_MBWU_FLT</td>
<td>MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0828</td>
<td>MS.MON_CFG_MBWU_CTL</td>
<td>MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Control Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0840</td>
<td>MS.MON_CSU</td>
<td>MPAM Cache Storage Usage Monitor Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0848</td>
<td>MS.MON_CSU_CAPTURE</td>
<td>MPAM Cache Storage Usage Monitor Capture Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0860</td>
<td>MS.MON_MBWU</td>
<td>MPAM Memory Bandwidth Usage Monitor Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0868</td>
<td>MS.MON_MBWU_CAPTURE</td>
<td>MPAM Memory Bandwidth Usage Monitor Capture Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0880</td>
<td>MS.MON_MBWU_L</td>
<td>MPAM Long Memory Bandwidth Usage Monitor Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x0890</td>
<td>MS.MON_MBWU_L_CAPTURE</td>
<td>MPAM Long Memory Bandwidth Usage Monitor Capture Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x1000 + (4 * n)</td>
<td>MPAMCFG_CPB.M&lt;n&gt;</td>
<td>MPAM Cache Portion Bitmap Partition Configuration Register</td>
</tr>
<tr>
<td>MPAMF_BASE_s</td>
<td>0x2000 + (4 * n)</td>
<td>MPAMCFG_MBW_PBM&lt;n&gt;</td>
<td>MPAM Bandwidth Portion Bitmap Partition Configuration Register</td>
</tr>
</tbody>
</table>
AMCFGR, Activity Monitors Configuration Register

The AMCFGR characteristics are:

**Purpose**

Global configuration register for the activity monitors.

Provides information on supported features, the number of counter groups implemented, the total number of activity monitor event counters implemented, and the size of the counters. AMCFGR is applicable to both the architected and the auxiliary counter groups.

**Configuration**

External register AMCFGR bits [31:0] are architecturally mapped to AArch64 System register AMCFGR_EL0[31:0].

External register AMCFGR bits [31:0] are architecturally mapped to AArch32 System register AMCFGR[31:0].

The power domain of AMCFGR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCFGR are RES0.

**Attributes**

AMCFGR is a 32-bit register.

**Field descriptions**

The AMCFGR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-28</td>
<td>NCG</td>
<td>Defines the number of counter groups. The number of implemented counter groups is defined as [AMCFGR,NCG + 1]. If the number of implemented auxiliary activity monitor event counters is zero, this field has a value of 0b0000. Otherwise, this field has a value of 0b0001.</td>
</tr>
<tr>
<td>27-25</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>24</td>
<td>HDBG</td>
<td>Halt-on-debug supported. From Armv8, this feature must be supported, and so this bit is 0b1.</td>
</tr>
<tr>
<td>23-20</td>
<td>RAZ</td>
<td>Reservation.</td>
</tr>
<tr>
<td>19-16</td>
<td>SIZE</td>
<td>Size.</td>
</tr>
<tr>
<td>15-10</td>
<td></td>
<td></td>
</tr>
<tr>
<td>9-5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4-0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NCG, bits [31:28]**

Defines the number of counter groups.

The number of implemented counter groups is defined as [AMCFGR,NCG + 1].

If the number of implemented auxiliary activity monitor event counters is zero, this field has a value of 0b0000. Otherwise, this field has a value of 0b0001.

**Bits [27:25]**

Reserved, RES0.

**HDBG, bit [24]**

Halt-on-debug supported.

From Armv8, this feature must be supported, and so this bit is 0b1.

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>AMCR,HDBG is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>AMCR,HDBG is read/write.</td>
</tr>
</tbody>
</table>
Bits [23:14]

Reserved, RAZ.

SIZE, bits [13:8]

Defines the size of activity monitor event counters.

The size of the activity monitor event counters implemented by the Activity Monitors Extension is defined as [AMCFGR.SIZE + 1].

From Armv8, the counters are 64-bit, and so this field is 0b111111.

---

**Note**

Software also uses this field to determine the spacing of counters in the memory-map. From Armv8, the counters are at doubleword-aligned addresses.

---

N, bits [7:0]

Defines the number of activity monitor event counters.

The total number of counters implemented in all groups by the Activity Monitors Extension is defined as [AMCFGR.N + 1].

### Accessing the AMCFGR

**AMCFGR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xE00</td>
<td>AMCFGR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The AMCGCR characteristics are:

**Purpose**

Provides information on the number of activity monitor event counters implemented within each counter group.

**Configuration**

External register AMCGCR bits [31:0] are architecturally mapped to AArch64 System register `AMCGCR_EL0[31:0]`. External register AMCGCR bits [31:0] are architecturally mapped to AArch32 System register `AMCGCR[31:0]`. The power domain of AMCGCR is IMPLEMENTATION DEFINED. This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCGCR are RES0.

**Attributes**

AMCGCR is a 32-bit register.

**Field descriptions**

The AMCGCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Reserved</td>
<td>RES0</td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
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<tr>
<td>4</td>
<td></td>
<td></td>
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<tr>
<td>5</td>
<td></td>
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<tr>
<td>6</td>
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<tr>
<td>7</td>
<td></td>
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<tr>
<td>8</td>
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<td>9</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
<td></td>
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<tr>
<td>11</td>
<td></td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
<td></td>
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<tr>
<td>13</td>
<td></td>
<td></td>
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<tr>
<td>14</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
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<tr>
<td>18</td>
<td></td>
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<tr>
<td>19</td>
<td></td>
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<tr>
<td>20</td>
<td></td>
<td></td>
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<tr>
<td>21</td>
<td></td>
<td></td>
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<tr>
<td>22</td>
<td></td>
<td></td>
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<tr>
<td>23</td>
<td></td>
<td></td>
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<tr>
<td>24</td>
<td></td>
<td></td>
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<tr>
<td>25</td>
<td></td>
<td></td>
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<tr>
<td>26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
<td></td>
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<tr>
<td>28</td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**CG1NC, bits [15:8]**

Counter Group 1 Number of Counters. The number of counters in the auxiliary counter group.

In an implementation that includes FEAT_AMUv1, the permitted range of values is 0 to 16.

**CG0NC, bits [7:0]**

Counter Group 0 Number of Counters. The number of counters in the architected counter group.

In an implementation that includes FEAT_AMUv1, the value of this field is 4.

**Accessing the AMCGCR**

AMCGCR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xCE0</td>
<td>AMCGCR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCIDR0, Activity Monitors Component Identification Register 0

The AMCIDR0 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

**Configuration**

The power domain of AMCIDR0 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMCIDR0 is a 32-bit register.

**Field descriptions**

The AMCIDR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | PRMBL_0 |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_0, bits [7:0]**

Preamble.

Reads as 0x0D.

**Accessing the AMCIDR0**

AMCIDR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFF0</td>
<td>AMCIDR0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCIDR1, Activity Monitors Component Identification Register 1

The AMCIDR1 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

**Configuration**

The power domain of AMCIDR1 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMCIDR1 is a 32-bit register.

**Field descriptions**

The AMCIDR1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | CLASS | PRMBL_1 |

**Bits [31:8]**

Reserved, RES0.

**CLASS, bits [7:4]**

Component class.

<table>
<thead>
<tr>
<th>CLASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1001</td>
<td>CoreSight component.</td>
</tr>
</tbody>
</table>

Other values are defined by the CoreSight Architecture.

This field reads as 0x9.

**PRMBL_1, bits [3:0]**

Preamble.

Reads as 0b0000.
Accessing the AMCIDR1

AMCIDR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFF4</td>
<td>AMCIDR1</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCIDR2, Activity Monitors Component Identification Register 2

The AMCIDR2 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

**Configuration**

The power domain of AMCIDR2 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMCIDR2 is a 32-bit register.

**Field descriptions**

The AMCIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30-8</td>
<td>PRMBL_2</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PRMBL_2, bits [7:0]**

Preamble.

Reads as 0x05.

**Accessing the AMCIDR2**

**AMCIDR2 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFF8</td>
<td>AMCIDR2</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCIDR3, Activity Monitors Component Identification Register 3

The AMCIDR3 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Component identification scheme'.

**Configuration**

The power domain of AMCIDR3 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMCIDR3 is a 32-bit register.

**Field descriptions**

The AMCIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
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<tr>
<td>26</td>
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<td>25</td>
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<tr>
<td>24</td>
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<tr>
<td>23</td>
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<td>22</td>
<td></td>
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<tr>
<td>21</td>
<td></td>
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<tr>
<td>20</td>
<td></td>
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<tr>
<td>19</td>
<td></td>
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<tr>
<td>18</td>
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<tr>
<td>17</td>
<td></td>
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<td>16</td>
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<td>15</td>
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<td>14</td>
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<td>11</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
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<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>PRMBL_3</td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PRMBL_3, bits [7:0]**

Preamble.

Reads as 0xB1.

**Accessing the AMCIDR3**

**AMCIDR3 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFFC</td>
<td>AMCIDR3</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCNTENCLR0, Activity Monitors Count Enable Clear Register 0

The AMCNTENCLR0 characteristics are:

Purpose

Disable control bits for the architected s event counters, AMEVCTR0<n>.

Configuration

External register AMCNTENCLR0 bits [31:0] are architecturally mapped to AArch64 System register
AMCNTENCLR0_EL0[31:0].

External register AMCNTENCLR0 bits [31:0] are architecturally mapped to AArch32 System register
AMCNTENCLR0[31:0].

The power domain of AMCNTENCLR0 is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR0 are
RES0.

Attributes

AMCNTENCLR0 is a 32-bit register.

Field descriptions

The AMCNTENCLR0 bit assignments are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>bit [n], for n = 31 to 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Activity monitor event counter disable bit for AMEVCTR0&lt;n&gt;.</td>
</tr>
<tr>
<td></td>
<td>Bits [31:N] are RAZ/WI. N is the value in AMCGCR.CG0NC.</td>
</tr>
<tr>
<td></td>
<td>Possible values of each bit are:</td>
</tr>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCTR0&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCTR0&lt;n&gt; is enabled. When written, disables AMEVCTR0&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

Accessing the AMCNTENCLR0

AMCNTENCLR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xC20</td>
<td>AMCNTENCLR0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCNTENCLR1, Activity Monitors Count Enable Clear Register 1

The AMCNTENCLR1 characteristics are:

Purpose

Disable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>.

Configuration

External register AMCNTENCLR1 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENCLR1_EL0[31:0].

External register AMCNTENCLR1 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENCLR1[31:0].

The power domain of AMCNTENCLR1 is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENCLR1 are RES0.

Attributes

AMCNTENCLR1 is a 32-bit register.

Field descriptions

The AMCNTENCLR1 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |ayy

P<n>, bit [n], for n = 31 to 0

Activity monitor event counter disable bit for AMEVCNTR1<n>.

Bits [31:N] are RAZ/WI. N is the value in AMCGCR.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is enabled. When written, disables AMEVCNTR1&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

Accessing the AMCNTENCLR1

If the number of auxiliary activity monitor event counters implemented is zero, reads of AMCNTENCLR1 are RAZ/WI. Software must treat reserved accesses as RES0. See 'Access requirements for reserved and unallocated registers'.

Note
The number of auxiliary activity monitor event counters implemented is zero exactly when AMCFGR.NCG == 0b0000.

**AMCNTENCLR1 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xC24</td>
<td>AMCNTENCLR1</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
AMCNTENSET0, Activity Monitors Count Enable Set Register 0

The AMCNTENSET0 characteristics are:

**Purpose**

Enable control bits for the architected activity monitors event counters, AMEVCNTR0\(n\).

**Configuration**

External register AMCNTENSET0 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENSET0_EL0[31:0].

External register AMCNTENSET0 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENSET0[31:0].

The power domain of AMCNTENSET0 is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET0 are RES0.

**Attributes**

AMCNTENSET0 is a 32-bit register.

**Field descriptions**

The AMCNTENSET0 bit assignments are:

\[
\begin{array}{ccccccccccccccccccc}
\end{array}
\]

\(P<n>, \text{ bit } [n], \text{ for } n = 31 \text{ to } 0\)

Activity monitor event counter enable bit for AMEVCNTR0\(n\).

Bits [31:N] are RAZ/WI. N is the value in AMCGCR.CG0NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>(P&lt;n&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR0(n) is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR0(n) is enabled. When written, enables AMEVCNTR0(n).</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENSET0**

AMCNTENSET0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xC00</td>
<td>AMCNTENSET0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCNTENSET1, Activity Monitors Count Enable Set Register 1

The AMCNTENSET1 characteristics are:

**Purpose**

Enable control bits for the auxiliary activity monitors event counters, AMEVCNTR1<n>.

**Configuration**

External register AMCNTENSET1 bits [31:0] are architecturally mapped to AArch64 System register AMCNTENSET1_EL0[31:0].

External register AMCNTENSET1 bits [31:0] are architecturally mapped to AArch32 System register AMCNTENSET1[31:0].

The power domain of AMCNTENSET1 is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCNTENSET1 are RES0.

**Attributes**

AMCNTENSET1 is a 32-bit register.

**Field descriptions**

The AMCNTENSET1 bit assignments are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;, bit [n], for n = 31 to 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
</tr>
<tr>
<td>----</td>
</tr>
</tbody>
</table>

Activity monitor event counter enable bit for AMEVCNTR1<n>.

Bits [31:N] are RAZ/WI. N is the value in AMCGCR.CG1NC.

Possible values of each bit are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that AMEVCNTR1&lt;n&gt; is enabled. When written, enables AMEVCNTR1&lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**Accessing the AMCNTENSET1**

If the number of auxiliary activity monitor event counters implemented is zero, reads of AMCNTENSET1 are RAZ/WI. Software must treat reserved accesses as RES0. See 'Access requirements for reserved and unallocated registers'.

**Note**
The number of auxiliary activity monitor counters implemented is zero exactly when \texttt{AMCFG.NCG} \texttt{== 0b0000}.

\textbf{AMCNTENSET1 can be accessed through the memory-mapped interfaces:}

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xC04</td>
<td>AMCNTENSET1</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMCR, Activity Monitors Control Register

The AMCR characteristics are:

**Purpose**

Global control register for the activity monitors implementation. AMCR is applicable to both the architected and the auxiliary counter groups.

**Configuration**

External register AMCR bits [31:0] are architecturally mapped to AArch64 System register AMCR_EL0[31:0].

External register AMCR bits [31:0] are architecturally mapped to AArch32 System register AMCR[31:0].

The power domain of AMCR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMCR are RES0.

**Attributes**

AMCR is a 32-bit register.

**Field descriptions**

The AMCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>HDBG</td>
</tr>
<tr>
<td>29</td>
<td>RAZ/WI</td>
</tr>
</tbody>
</table>

**Bits [31:11]**

Reserved, RES0.

**HDBG, bit [10]**

This bit controls whether activity monitor counting is halted when the PE is halted in Debug state.

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Activity monitors do not halt counting when the PE is halted in Debug state.</td>
</tr>
<tr>
<td>1</td>
<td>Activity monitors halt counting when the PE is halted in Debug state.</td>
</tr>
</tbody>
</table>

**Bits [9:0]**

Reserved, RAZ/WI.

**Accessing the AMCR**

AMCR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xE04</td>
<td>AMCR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMDEVAFF0, Activity Monitors Device Affinity Register

The AMDEVAFF0 characteristics are:

**Purpose**

Copy of the low half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the AMU component relates to.

**Configuration**

The power domain of AMDEVAFF0 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMDEVAFF0 is a 32-bit register.

**Field descriptions**

The AMDEVAFF0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>MPIDR_EL1lo</td>
</tr>
</tbody>
</table>

**MPIDR_EL1lo, bits [31:0]**

MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the AMDEVAFF0**

AMDEVAFF0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFA8</td>
<td>AMDEVAFF0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMDEVAFF1, Activity Monitors Device Affinity Register

The AMDEVAFF1 characteristics are:

**Purpose**

Copy of the high half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the AMU component relates to.

**Configuration**

The power domain of AMDEVAFF1 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMDEVAFF1 is a 32-bit register.

**Field descriptions**

The AMDEVAFF1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

MPIDR_EL1hi, bits [31:0]

MPIDR_EL1 hi half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the AMDEVAFF1**

AMDEVAFF1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFAC</td>
<td>AMDEVAFF1</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMDEVARCH, Activity Monitors Device Architecture Register

The AMDEVARCH characteristics are:

Purpose

Identifies the programmers' model architecture of the AMU component.

Configuration

The power domain of AMDEVARCH is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

Attributes

AMDEVARCH is a 32-bit register.

Field descriptions

The AMDEVARCH bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ARCHITECT | PRESENT | REVISION | ARCHID |

ARCHITECT, bits [31:21]

Defines the architecture of the component. For AMU, this is Arm Limited.

Bits [31:28] are the JEP106 continuation code, 0x4.

Bits [27:21] are the JEP106 ID code, 0x3B.

PRESENT, bit [20]

When set to 1, indicates that the DEVARCH is present.

This field is 1 in Armv8.

REVISION, bits [19:16]

Defines the architecture revision. For architectures defined by Arm this is the minor revision.

<table>
<thead>
<tr>
<th>REVISION</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Architecture revision is AMUv1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

ARCHID, bits [15:0]

Defines this part to be an AMU component. For architectures defined by Arm this is further subdivided.

For AMU:
• Bits [15:12] are the architecture version, 0x0.
• Bits [11:0] are the architecture part number, 0xA66.

This corresponds to AMU architecture version AMUv1.

**Accessing the AMDEVARCH**

**AMDEVARCH can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFBC</td>
<td>AMDEVARCH</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
AMDEVTYPE, Activity Monitors Device Type Register

The AMDEVTYPE characteristics are:

**Purpose**

Indicates to a debugger that this component is part of a PE's performance monitor interface.

**Configuration**

The power domain of AMDEVTYPE is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMDEVTYPE is a 32-bit register.

**Field descriptions**

The AMDEVTYPE bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Bits [31:8]</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>SUB</td>
<td>Bits [7:4]</td>
<td>Subtype. Reads as 0x1, to indicate this is a component within a PE.</td>
</tr>
<tr>
<td>MAJOR</td>
<td>Bits [3:0]</td>
<td>Major type. Reads as 0x6, to indicate this is a performance monitor component.</td>
</tr>
</tbody>
</table>

**Accessing the AMDEVTYPE**

AMDEVTYPE can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFCC</td>
<td>AMDEVTYPE</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMEVCNTR0\(<n>\), Activity Monitors Event Counter Registers 0, n = 0 - 15

The AMEVCNTR0\(<n>\) characteristics are:

**Purpose**

Provides access to the architected activity monitor event counters.

**Configuration**

External register AMEVCNTR0\(<n>\) bits [63:0] are architecturally mapped to AArch64 System register AMEVCNTR0\(<n>_EL0[63:0]\).

External register AMEVCNTR0\(<n>\) bits [63:0] are architecturally mapped to AArch32 System register AMEVCNTR0\(<n>[63:0]\).

The power domain of AMEVCNTR0\(<n>\) is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR0\(<n>\) are RES0.

**Attributes**

AMEVCNTR0\(<n>\) is a 64-bit register.

**Field descriptions**

The AMEVCNTR0\(<n>\) bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**ACNT, bits [63:0]**

Architected activity monitor event counter n.

Value of architected activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

**Accessing the AMEVCNTR0\(<n>\)**

If \(<n>\) is greater than or equal to the number of architected activity monitor event counters, reads of AMEVCNTR0\(<n>\) are RAZ/WI. Software must treat reserved accesses as RES0. See 'Access requirements for reserved and unallocated registers'.
AMEVCNTR0\(<n>\) can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0x000 + (8 * n)</td>
<td>AMEVCNTR0(&lt;n&gt;)</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0x004 + (8 * n)</td>
<td>AMEVCNTR0(&lt;n&gt;)</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMEVCNTR1<n>, Activity Monitors Event Counter Registers 1, n = 0 - 15

The AMEVCNTR1<n> characteristics are:

**Purpose**

Provides access to the auxiliary activity monitor event counters.

**Configuration**

External register AMEVCNTR1<n> bits [63:0] are architecturally mapped to AArch64 System register AMEVCNTR1<n>_EL0[63:0].

External register AMEVCNTR1<n> bits [63:0] are architecturally mapped to AArch32 System register AMEVCNTR1<n>[63:0].

The power domain of AMEVCNTR1<n> is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVCNTR1<n> are RES0.

**Attributes**

AMEVCNTR1<n> is a 64-bit register.

**Field descriptions**

The AMEVCNTR1<n> bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| ACNT | ACNT |

**ACNT, bits [63:0]**

Auxiliary activity monitor event counter n.

Value of auxiliary activity monitor event counter n, where n is the number of this register and is a number from 0 to 15.

If the counter is enabled, writes to this register have UNPREDICTABLE results.

On a Cold reset, this field resets to 0.

**Accessing the AMEVCNTR1<n>**

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads of AMEVCNTR1<n> are RAZ/WI. Software must treat reserved accesses as RES0. See ‘Access requirements for reserved and unallocated registers’.

**Note**

AMECGCR.CG1NC identifies the number of auxiliary activity monitor event counters.
AMEVCNTR1<\(n\)> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>(0x100 + (8 \times n))</td>
<td>AMEVCNTR1&lt;(n)&gt;</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are \textbf{RO}.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>(0x104 + (8 \times n))</td>
<td>AMEVCNTR1&lt;(n)&gt;</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are \textbf{RO}.
AMEVTYPER0\(<n>\), Activity Monitors Event Type Registers 0, n = 0 - 15

The AMEVTYPER0\(<n>\) characteristics are:

**Purpose**

Provides information on the events that an architected activity monitor event counter AMEVCNTR0\(<n>\) counts.

**Configuration**

External register AMEVTYPER0\(<n>\) bits [31:0] are architecturally mapped to AArch64 System register AMEVTYPER0\(<n>_EL0[31:0]\).

External register AMEVTYPER0\(<n>\) bits [31:0] are architecturally mapped to AArch32 System register AMEVTYPER0\(<n>[31:0]\).

The power domain of AMEVTYPER0\(<n>\) is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER0\(<n>\) are RES0.

**Attributes**

AMEVTYPER0\(<n>\) is a 32-bit register.

**Field descriptions**

The AMEVTYPER0\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 - 25</td>
<td>Reserved, RAZ.</td>
</tr>
<tr>
<td>24 - 16</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15 - 0</td>
<td>Event to count. The event number of the event that is counted by the architected activity monitor event counter AMEVCNTR0(&lt;n&gt;). The value of this field is architecturally mandated for each architected counter.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>evtCount</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0011</td>
<td>Processor frequency cycles</td>
<td>When n == 0</td>
</tr>
<tr>
<td>0x4004</td>
<td>Constant frequency cycles</td>
<td>When n == 1</td>
</tr>
<tr>
<td>0x0008</td>
<td>Instructions retired</td>
<td>When n == 2</td>
</tr>
<tr>
<td>0x4005</td>
<td>Memory stall cycles</td>
<td>When n == 3</td>
</tr>
</tbody>
</table>
Accessing the AMEVTYPE0<n>

If <n> is greater than or equal to the number of architected activity monitor event counters, reads of AMEVTYPE0<n> are RAZ/WI. Software must treat reserved accesses as RES0. See 'Access requirements for reserved and unallocated registers'.

---

**Note**

AMCGCR.CG0NC identifies the number of architected activity monitor event counters.

---

**AMEVTYPE0<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0x400 + (4 * n)</td>
<td>AMEVTYPE0&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The AMEVTYPER1\(<n>\) characteristics are:

**Purpose**

Provides information on the events that an auxiliary activity monitor event counter AMEVCNTR1\(<n>\) counts.

**Configuration**

External register AMEVTYPER1\(<n>\) bits [31:0] are architecturally mapped to AArch64 System register AMEVTYPER1\(<n>_EL0[31:0]\).

External register AMEVTYPER1\(<n>\) bits [31:0] are architecturally mapped to AArch32 System register AMEVTYPER1\(<n>_E[31:0]\).

The power domain of AMEVTYPER1\(<n>\) is implementation defined.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMEVTYPER1\(<n>\) are RES0.

**Attributes**

AMEVTYPER1\(<n>\) is a 32-bit register.

**Field descriptions**

The AMEVTYPER1\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RAZ</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>evtCount</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RAZ</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Bits [31:25]**

Reserved, RAZ.

**Bits [24:16]**

Reserved, RES0.

**evtCount, bits [15:0]**

Event to count. The event number of the event that is counted by the auxiliary activity monitor event counter AMEVCNTR1\(<n>\).

It is implementation defined what values are supported by each counter.

If software writes a value to this field which is not supported by the corresponding counter AMEVCNTR1\(<n>\), then:

- It is unpredictable which event will be counted.
- The value read back is unknown.

**Note**

The event counted by AMEVCNTR1\(<n>\) might be fixed at implementation. In this case, the field is read-only and writes are undefined.
If the corresponding counter AMEVCNTR1<n> is enabled, writes to this register have **UNPREDICTABLE** results.

**Accessing the AMEVTYPER1<n>**

If <n> is greater than or equal to the number of auxiliary activity monitor event counters, reads of AMEVTYPER1<n> are RAZ/WI. Software must treat reserved accesses as RES0. See 'Access requirements for reserved and unallocated registers'.

---

**Note**

AMEGCR.CG1NC identifies the number of auxiliary activity monitor event counters.

---

AMEVTYPER1<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0x480 + (4 * n)</td>
<td>AMEVTYPER1&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
AMIIDR, Activity Monitors Implementation Identification Register

The AMIIDR characteristics are:

**Purpose**

Defines the implementer and revisions of the AMU.

**Configuration**

The power domain of AMIIDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_AMUv1 is implemented. Otherwise, direct accesses to AMIIDR are RES0.

**Attributes**

AMIIDR is a 32-bit register.

**Field descriptions**

The AMIIDR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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</tr>
</tbody>
</table>

**ProductID, bits [31:20]**

This field is an AMU part identifier.

The value of this field is IMPLEMENTATION DEFINED.

If **AMPIDR0** is implemented, **AMPIDR0**.PART_0 matches bits [27:20] of this field.

If **AMPIDR1** is implemented, **AMPIDR1**.PART_1 matches bits [31:28] of this field.

**Variant, bits [19:16]**

This field distinguishes product variants or major revisions of the product.

The value of this field is IMPLEMENTATION DEFINED.

If **AMPIDR2** is implemented, **AMPIDR2**.REVISION matches AMIIDR.Variant.

**Revision, bits [15:12]**

This field distinguishes minor revisions of the product.

The value of this field is IMPLEMENTATION DEFINED.

If **AMPIDR3** is implemented, **AMPIDR3**.REVAND matches AMIIDR.Revision.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the AMU.

For an Arm implementation, this field reads as 0x43B.
Bits [11:8] contain the JEP106 continuation code of the implementer.

Bit 7 is RES0

Bits [6:0] contain the JEP106 identity code of the implementer.

If AMPIDR4 is implemented, AMPIDR4.DES_2 matches bits [11:8] of this field.
If AMPIDR2 is implemented, AMPIDR2.DES_1 matches bits [6:4] of this field.
If AMPIDR1 is implemented, AMPIDR1.DES_0 matches bits [3:0] of this field.

**Accessing the AMIIDR**

AMIIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xE08</td>
<td>AMIIDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The AMPIDR0 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

The power domain of AMPIDR0 is **IMPLEMENTATION DEFINED**.

Implementation of this register is **OPTIONAL**.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMPIDR0 is a 32-bit register.

**Field descriptions**

The AMPIDR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | PART_0 |

**Bits [31:8]**

Reserved, RES0.

**PART_0, bits [7:0]**

Part number, least significant byte.

The value of this field is **IMPLEMENTATION DEFINED**.

**Accessing the AMPIDR0**

AMPIDR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFE0</td>
<td>AMPIDR0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
**AMPIDR1, Activity Monitors Peripheral Identification Register 1**

The AMPIDR1 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

The power domain of AMPIDR1 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMPIDR1 is a 32-bit register.

**Field descriptions**

The AMPIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:2</td>
<td>Reserved, RES0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>7:4</td>
<td>Designer, least significant</td>
<td>0b1011 for Arm Limited</td>
</tr>
<tr>
<td></td>
<td>nibble of JEP106 ID code</td>
<td></td>
</tr>
<tr>
<td>3:0</td>
<td>Part number, most significant</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**Accessing the AMPIDR1**

**AMPIDR1 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFE4</td>
<td>AMPIDR1</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The AMPIDR2 characteristics are:

Purpose

Provides information to identify an activity monitors component.
For more information, see 'About the Peripheral identification scheme'.

Configuration

The power domain of AMPIDR2 is IMPLEMENTATION DEFINED.
Implementation of this register is OPTIONAL.
This register is present only when FEAT_AMUv1 is implemented.

Attributes

AMPIDR2 is a 32-bit register.

Field descriptions

The AMPIDR2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | REVISION | JEDEC | DES_1 |

Bits [31:8]

Reserved, RES0.

REVISION, bits [7:4]

Part major revision. Parts can also use this field to extend Part number to 16-bits.
The value of this field is IMPLEMENTATION DEFINED.

JEDEC, bit [3]

RAO. Indicates a JEP106 identity code is used.

DES_1, bits [2:0]

Designer, most significant bits of JEP106 ID code.
The value of this field is IMPLEMENTATION DEFINED. For Arm Limited, this field is 0b011.
Accessing the AMPIDR2

AMPIDR2 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFE8</td>
<td>AMPIDR2</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMPIDR3, Activity Monitors Peripheral Identification Register 3

The AMPIDR3 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

The power domain of AMPIDR3 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMPIDR3 is a 32-bit register.

**Field descriptions**

The AMPIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>REVAND</td>
<td>CMOD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**REVAND, bits [7:4]**

Part minor revision. Parts using AMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.

The value of this field is IMPLEMENTATION DEFINED.

**CMOD, bits [3:0]**

Customer modified. Indicates someone other than the Designer has modified the component.

The value of this field is IMPLEMENTATION DEFINED.

**Accessing the AMPIDR3**

AMPIDR3 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFEC</td>
<td>AMPIDR3</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
AMPIDR4, Activity Monitors Peripheral Identification Register 4

The AMPIDR4 characteristics are:

**Purpose**

Provides information to identify an activity monitors component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

The power domain of AMPIDR4 is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

This register is present only when FEAT_AMUv1 is implemented.

**Attributes**

AMPIDR4 is a 32-bit register.

**Field descriptions**

The AMPIDR4 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | SIZE | DES_2 |

**Bits [31:8]**

Reserved, RES0.

**SIZE, bits [7:4]**

Size of the component. \( \log_2 \) of the number of 4KB pages from the start of the component to the end of the component ID registers.

This field reads as \( 0b0000 \).

**DES_2, bits [3:0]**

Designer. JEP106 continuation code, least significant nibble.

The value of this field is IMPLEMENTATION DEFINED. For Arm Limited, this field is \( 0b0100 \).

**Accessing the AMPIDR4**

AMPIDR4 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMU</td>
<td>0xFD0</td>
<td>AMPIDR4</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ASICCTL, CTI External Multiplexer Control register

The ASICCTL characteristics are:

**Purpose**

Can be used to provide IMPLEMENTATION DEFINED controls for the CTI. For example, the register might be used to control multiplexors for additional IMPLEMENTATION DEFINED triggers. The IMPLEMENTATION DEFINED controls provided by this register might modify the architecturally defined behavior of the CTI.

**Note**

The architecturally-defined triggers must not be multiplexed.

**Configuration**

It is IMPLEMENTATION DEFINED whether ASICCTL is implemented in the Core power domain or in the Debug power domain.

If it is implemented in the Core power domain then it is IMPLEMENTATION DEFINED whether it is in the Cold reset domain or the Warm reset domain.

This register must reset to a value that supports the architecturally-defined behavior of the CTI. Changing the value of the register from its reset value causes IMPLEMENTATION DEFINED behavior that might differ from the architecturally-defined behavior of the CTI.

Other than the requirements listed in this register description, all aspects of the reset behavior of the ASICCTL are IMPLEMENTATION DEFINED.

**Attributes**

ASICCTL is a 32-bit register.

**Field descriptions**

The ASICCTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**Accessing the ASICCTL**

ASICCTL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x144</td>
<td>ASICCTL</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and SoftwareLockStatus() accesses to this register are RO.
- Otherwise accesses to this register are IMPDEF.
The CNTACR\<n> characteristics are:

**Purpose**

Provides top-level access controls for the elements of a timer frame. CNTACR\<n> provides the controls for frame CNTBaseN.

In addition to the CNTACR\<n> control:

- CNTNSAR controls whether CNTACR\<n> is accessible by Non-secure accesses.
- If frame CNTEL0BaseN is implemented, the CNTEL0ACR in frame CNTBaseN provides additional control of accesses to frame CNTEL0BaseN.

**Configuration**

The power domain of CNTACR\<n> is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

Implemented only if the value of CNTTIDR.Frame\<n> is 1.

An implementation of the counters might not provide configurable access to some or all of the features. In this case, the associated field in the CNTACR\<n> register is:

- RAZ/WI if access is always denied.
- RAO/WI if access is always permitted.

**Attributes**

CNTACR\<n> is a 32-bit register.

**Field descriptions**

The CNTACR\<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RWPT | RWVT | RVOFF | RFRQ | RVCTR | RPCT |

**Bits [31:6]**

Reserved, RES0.

**RWPT, bit [5]**

Read/write access to the EL1 Physical Timer registers CNTP_CVAL, CNTP_TVAL, and CNTP_CTL in frame \<n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RWPT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to the EL1 Physical Timer registers in frame &lt;n&gt;. The registers are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read/write access to the EL1 Physical Timer registers in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
RWVT, bit [4]

Read/write access to the Virtual Timer register CNTV_CVAL, CNTV_TVAL, and CNTV_CTL, in frame <n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RWVT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to the Virtual Timer registers in frame &lt;n&gt;. The registers are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read/write access to the Virtual Timer registers in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RVOFF, bit [3]

Read-only access to CNTVOFF, in frame <n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RVOFF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to CNTVOFF in frame &lt;n&gt;. The register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read-only access to CNTVOFF in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RFRQ, bit [2]

Read-only access to CNTFRQ, in frame <n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RFRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to CNTFRQ in frame &lt;n&gt;. The register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read-only access to CNTFRQ in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RVCT, bit [1]

Read-only access to CNTVCT, in frame <n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RVCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to CNTVCT in frame &lt;n&gt;. The register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read-only access to CNTVCT in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

RPCT, bit [0]

Read-only access to CNTPCT, in frame <n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th>RPCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access to CNTPCT in frame &lt;n&gt;. The register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read-only access to CNTPCT in frame &lt;n&gt;.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the CNTACR<n>

In a system that recognizes two Security states:

- CNTACR<n> is always accessible by Secure accesses.
- CNTNSAR.NS<n> determines whether CNTACR<n> is accessible by Non-secure accesses.

CNTACR<n> can be accessed through the memory-mapped interfaces:
<table>
<thead>
<tr>
<th>Timer</th>
<th>CNTCTLBase $\times 0x40 + (4 \times n)$</th>
<th>CNTACR(\langle n\rangle)</th>
</tr>
</thead>
</table>

Accesses on this interface are **RW**.
CNTCR, Counter Control Register

The CNTCR characteristics are:

Purpose

Enables the counter, controls the counter frequency setting, and controls counter behavior during debug.

Configuration

The power domain of CNTCR is IMPLEMENTATION DEFINED.

For more information, see ‘Power and reset domains for the system level implementation of the Generic Timer’.

Attributes

CNTCR is a 32-bit register.

Field descriptions

The CNTCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | FCREQ | RES0 | SCEN | HDBG | EN |

Bits [31:18]

Reserved, RES0.

FCREQ, bits [17:8]

Frequency change request. Indicates the number of the entry in the Frequency modes table to select.

Selecting an unimplemented entry, or an entry that contains 0, has no effect on the counter.

The maximum number of entries in the Frequency modes table is IMPLEMENTATION DEFINED up to a maximum of 1004 entries, see ‘The Frequency modes table’. An implementation is only required to implement an FCREQ field that can hold values from 0 to the highest supported Frequency modes table entry. Any unrequired most-significant bits of FCREQ can be implemented as RES0.

On a Warm reset, this field resets to 0.

Bits [7:3]

Reserved, RES0.

SCEN, bit [2]

When FEAT_CNTSC is implemented:

Scale Enable.

<table>
<thead>
<tr>
<th>SCEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Scaling is not enabled. The counter value is incremented by 0x1.0000000 for each counter tick.</td>
</tr>
<tr>
<td>0b1</td>
<td>Scaling is enabled. The counter is incremented by CNTSCR.ScaleVal for each counter tick.</td>
</tr>
</tbody>
</table>
The SCEN bit can only be changed when the counter is disabled, when CNTCR.EN == 0.

If the value of CNTCR.SCEN changes when CNTCR.EN == 1 then:

- The counter value becomes UNKNOWN.
- The counter value remains UNKNOWN on future ticks of the clock.

When the CNTCV register in the CNTControlBase frame of the memory mapped counter module is written to, the accumulated fraction information is reset to zero.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

HDBG, bit [1]

Halt-on-debug. Controls whether a Halt-on-debug signal halts the system counter:

<table>
<thead>
<tr>
<th>HDBG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>System counter ignores Halt-on-debug.</td>
</tr>
<tr>
<td>0b1</td>
<td>Asserted Halt-on-debug signal halts system counter update.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EN, bit [0]

Enables the counter:

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>System counter disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>System counter enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the CNTCR**

In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, that includes this register, is implemented only in the Secure memory map.

**CNTCR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x000</td>
<td>CNTCR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
CNTCV, Counter Count Value register

The CNTCV characteristics are:

**Purpose**

Indicates the current count value.

**Configuration**

The power domain of CNTCV is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTCV is a 64-bit register.

**Field descriptions**

The CNTCV bit assignments are:

```
| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    | CountValue |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    | CountValue |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
```

**CountValue, bits [63:0]**

Indicates the counter value.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTCV**

<table>
<thead>
<tr>
<th>Frame</th>
<th>Accessibility</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTControlBase</td>
<td>RW</td>
</tr>
<tr>
<td>CNTReadBase</td>
<td>RO</td>
</tr>
</tbody>
</table>

A write to CNTCV must be visible in the CNTPCT register of each running processor in a finite time.

For the instance of the register in the CNTControlBase frame:

- In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, and therefore this register instance, is implemented only in the Secure memory map.
- If the counter is enabled, the effect of writing to the register is UNKNOWN.

In an implementation that supports 64-bit atomic memory accesses, this register must be accessible using a 64-bit atomic access.

CNTCV can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x008</td>
<td>CNTCV</td>
<td>63:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTReadBase</td>
<td>0x000</td>
<td>CNTCV</td>
<td>63:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The CNTEL0ACR characteristics are:

**Purpose**

An implementation of CNTEL0ACR in the frame at CNTBaseN controls whether the **CNTPCT**, **CNTVCT**, **CNTFRO**, EL1 Physical Timer, and Virtual Timer registers are visible in the frame at CNTEL0BaseN.

**Configuration**

The power domain of CNTEL0ACR is **IMPLEMENTATION DEFINED**.

Implementation of this register is **OPTIONAL**.

For more information, see ‘Power and reset domains for the system level implementation of the Generic Timer’.

**Attributes**

CNTEL0ACR is a 32-bit register.

**Field descriptions**

The CNTEL0ACR bit assignments are:

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
<th>RES0</th>
<th>ELOPTEN</th>
<th>ELOVTEN</th>
<th>RES0</th>
<th>ELOVCTEN</th>
<th>ELOPCTEN</th>
</tr>
</thead>
</table>

**Bits [31:10]**

Reserved, RES0.

**ELOPTEN, bit [9]**

Second view read/write access control for the EL1 Physical Timer registers. This bit controls whether the **CNTP_CVAL**, **CNTP_TVAL**, and **CNTP_CTL** registers in the current CNTBaseN frame are also accessible in the corresponding CNTEL0BaseN frame. The possible values of this bit are:

<table>
<thead>
<tr>
<th>ELOPTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access. Registers are RES0 in the second view.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access permitted. If the registers are accessible in the current frame then they are accessible in the second view.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**ELOVTEN, bit [8]**

Second view read/write access control for the Virtual Timer registers. This bit controls whether the **CNTV_CVAL**, **CNTV_TVAL**, and **CNTV_CTL** registers in the current CNTBaseN frame are also accessible in the corresponding CNTEL0BaseN frame. The possible values of this bit are:

<table>
<thead>
<tr>
<th>ELOVTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No access. Registers are RES0 in the second view.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access permitted. If the registers are accessible in the current frame then they are accessible in the second view.</td>
</tr>
</tbody>
</table>
The definition of this bit means that, if the Virtual Timer registers are not implemented in the current CNTBaseN frame, then the Virtual Timer register addresses are RES0 in the corresponding CNTEL0BaseN frame, regardless of the value of this bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [7:2]**

Reserved, RES0.

**ELOVCTEN, bit [1]**

Second view read access control for CNTVCT and CNTFRQ. The possible values of this bit are:

<table>
<thead>
<tr>
<th>ELOVCTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CNTVCT is not visible in the second view. If EL0PCTEN is set to 0, CNTFRQ is not visible in the second view.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access permitted. If CNTVCT and CNTFRQ are visible in the current frame then they are visible in the second view.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**ELOPCTEN, bit [0]**

Second view read access control for CNTPCT and CNTFRQ. The possible values of this bit are:

<table>
<thead>
<tr>
<th>ELOPCTEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CNTPCT is not visible in the second view. If EL0VCTEN is set to 0, CNTFRQ is not visible in the second view.</td>
</tr>
<tr>
<td>0b1</td>
<td>Access permitted. If CNTPCT and CNTFRQ are visible in the current frame then they are visible in the second view.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTEL0ACR**

CNTEL0ACR can be implemented in any implemented CNTBaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

If CNTEL0ACR is not implemented in an implemented CNTBaseN frame:

- The register location in that frame is RAZ/WI.
- If the corresponding CNTEL0BaseN frame is implemented, the registers CNTFRQ, CNTP_CTL, CNTP_CVAL, CNTP_TVAL, CNTPCT, CNTV_CTL, CNTV_CVAL, CNTV_TVAL, and CNTVCT are not visible in that frame.

**CNTEL0ACR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x014</td>
<td>CNTEL0ACR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
CNTFID0, Counter Frequency ID

The CNTFID0 characteristics are:

Purpose

Indicates the base frequency of the system counter.

Configuration

The power domain of CNTFID0 is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

The possible frequencies for the system counter are stored in the Frequency modes table as 32-bit words starting with the base frequency, CNTFID0. For more information, see 'The Frequency modes table'.

The final entry in the Frequency modes table must be followed by a 32-bit word of zero value, to mark the end of the table.

Typically, the Frequency modes table will be in read-only memory. However, a system implementation might use read/write memory for the table, and initialize the table entries as part of its start-up sequence.

If the Frequency modes table is in read/write memory, Arm strongly recommends that the table is not updated once the system is running.

Attributes

CNTFID0 is a 32-bit register.

Field descriptions

The CNTFID0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Frequency</td>
</tr>
</tbody>
</table>

Frequency, bits [31:0]

The base frequency of the system counter, in Hz.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the CNTFID0

It is IMPLEMENTATION DEFINED whether this register is RO or RW

In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, that includes this register, is implemented only in the Secure memory map.

CNTFID0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x020</td>
<td>CNTFID0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO or RW.
The CNTFID<n> characteristics are:

**Purpose**

Indicates alternative system counter update frequencies.

**Configuration**

The power domain of CNTFID<n> is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

The possible frequencies for the system counter are stored in the Frequency modes table as 32-bit words starting with the base frequency, CNTFID0, see 'The Frequency modes table'.

The number of CNTFID<n> registers is IMPLEMENTATION DEFINED, and the only required CNTFID<n> register is CNTFID0.

The final entry in the Frequency modes table must be followed by a 32-bit word of zero value, to mark the end of the table.

The architecture can support up to 1004 entries in the Frequency modes table, including the zero-word end marker, and the number of entries is IMPLEMENTATION DEFINED up to this limit. For an implementation that includes registers in the IMPLEMENTATION DEFINED register space 0x0C0-0x0FC, the maximum number of entries in the Frequency modes table is 40, including the zero-word end marker.

Typically, the Frequency modes table will be in read-only memory. However, a system implementation might use read/write memory for the table, and initialize the table entries as part of its start-up sequence.

If the Frequency modes table is in read/write memory, Arm strongly recommends that the table is not updated once the system is running.

**Attributes**

CNTFID<n> is a 32-bit register.

**Field descriptions**

The CNTFID<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Frequency

**Frequency, bits [31:0]**

A system counter update frequency, in Hz. Must be an exact divisor of the base frequency. Arm strongly recommends that all frequency values in the Frequency modes table are integer power-of-two divisors of the base frequency.

When the system timer is operating at a lower frequency than the base frequency, the increment applied at each counter update is given by:

increment = (base frequency) / (selected frequency)

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**Accessing the CNTFID<\(n\)>**

It is **IMPLEMENTATION DEFINED** whether this register is **RO or RW**

In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, that includes these registers, is implemented only in the Secure memory map.

**CNTFID<\(n\)> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x020 + (4 * (n))</td>
<td>CNTFID&lt;(n)&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO or RW**.
CNTFRQ, Counter-timer Frequency

The CNTFRQ characteristics are:

**Purpose**

This register is provided so that software can discover the frequency of the system counter. The instance of the register in the CNTCTLBase frame must be programmed with this value as part of system initialization. The value of the register is not interpreted by hardware.

**Configuration**

The power domain of CNTFRQ is IMPLEMENTATION DEFINED.

For more information see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTFRQ is a 32-bit register.

**Field descriptions**

The CNTFRQ bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Clock frequency</td>
</tr>
</tbody>
</table>

Bits [31:0]

Clock frequency. Indicates the system counter clock frequency, in Hz.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTFRQ**

CNTFRQ must be implemented as an RW register in the CNTCTLBase frame.

In a system that recognizes two Security states, the instance of the register in the CNTCTLBase frame is only accessible by Secure accesses.

CNTFRQ can be implemented as a RO register in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTFRQ is accessible in that frame, as a RO register, if the value of CNTACR<n>.RFRQ is 1.
- Otherwise, the CNTFRQ address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTFRQ is accessible as a RO register in that frame if both:
  - CNTFRQ is accessible in the corresponding CNTBaseN frame.
Either the value of CNTEL0ACR.EL0VCTEN is 1 or the value of CNTEL0ACR.EL0PCTEN is 1.

- Otherwise, the CNTFRQ address in that frame is RAZ/WI.

**CNTFRQ can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x010</td>
<td>CNTFRQ</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x010</td>
<td>CNTFRQ</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>0x000</td>
<td>CNTFRQ</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CNTID, Counter Identification Register

The CNTID characteristics are:

Purpose

Indicates whether counter scaling is implemented.

Configuration

The power domain of CNTID is IMPLEMENTATION DEFINED.

This register is present only when FEAT_CNTSC is implemented. Otherwise, direct accesses to CNTID are RES0.

Attributes

CNTID is a 32-bit register.

Field descriptions

The CNTID bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
</tr>
<tr>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>CNTSC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [31:4]

Reserved, RES0.

CNTSC, bits [3:0]

Indicates whether Counter Scaling is implemented

<table>
<thead>
<tr>
<th>CNTSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Counter scaling is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Counter scaling is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Accessing the CNTID

In a system that supports Secure and Non-secure memory maps, the CNTControlBase frame, that includes this register, is implemented only in the Secure memory map.

CNTID can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x1C</td>
<td>CNTID</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CNTNSAR, Counter-timer Non-secure Access Register

The CNTNSAR characteristics are:

**Purpose**

Provides the highest-level control of whether frames CNTBaseN and CNTEL0BaseN are accessible by Non-secure accesses.

**Configuration**

The power domain of CNTNSAR is **IMPLEMENTATION DEFINED**.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTNSAR is a 32-bit register.

**Field descriptions**

The CNTNSAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Reserved</td>
<td>NS&lt;n&gt; for n = 7 to 0</td>
</tr>
<tr>
<td>NS0 to NS7</td>
<td>Non-secure access to frame n. The possible values of this bit are:</td>
<td></td>
</tr>
</tbody>
</table>

### Bits [31:8]

**Reserved, RES0.**

**NS<n>, bit [n], for n = 7 to 0**

Non-secure access to frame n. The possible values of this bit are:

<table>
<thead>
<tr>
<th>NS&lt;n&gt;</th>
<th>Meaning</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure access only. Behaves as RES0 to Non-secure accesses.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>Secure and Non-secure accesses permitted.</td>
<td></td>
</tr>
</tbody>
</table>

This bit also determines whether, in the CNTCTLLBase frame, CNTACR<n> and CNTVOFF<n> are accessible to Non-secure accesses.

If frame CNTBase<n>:

- Is not implemented, then NS<n> is RES0.
- Is not Configurable access, and is accessible only by Secure accesses, then NS<n> is RES0.
- Is not Configurable access, and is accessible by both Secure and Non-secure accesses, then NS<n> is RES1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTNSAR**

In a system that recognizes two Security states, this register is only accessible by Secure accesses.

**CNTNSAR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CNTNSAR, Counter-timer Non-secure Access Register</td>
<td>Page 3308</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>0x004</td>
<td>CNTNSAR</td>
</tr>
<tr>
<td>-------</td>
<td>------------</td>
<td>-------</td>
<td>---------</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
The CNTP_CTL characteristics are:

**Purpose**

Control register for the EL1 physical timer.

**Configuration**

The power domain of CNTP_CTL is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTP_CTL is a 32-bit register.

**Field descriptions**

The CNTP_CTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Status of the timer, this bit indicates</td>
</tr>
<tr>
<td></td>
<td>whether the timer condition is met.</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt mask bit, permitted values are</td>
</tr>
<tr>
<td></td>
<td>Timer interrupt is not masked by the</td>
</tr>
<tr>
<td></td>
<td>IMASK bit.</td>
</tr>
<tr>
<td>0</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

Bits [31:3]

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTatus indicates whether the timer condition is met. ISTatus takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
ENABLE, bit [0]

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from `CNTP_TVAL` continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the CNTP_CTL

`CNTP_CTL` can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- `CNTP_CTL` is accessible in that frame if the value of `CNTACR<n>.RWPT` is 1.
- Otherwise, the `CNTP_CTL` address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- `CNTP_CTL` is accessible in that frame if both:
  - `CNTP_CTL` is accessible in the corresponding CNTBaseN frame:
  - The value of `CNTEL0ACR.EL0PTEN` is 1.
- Otherwise, the `CNTP_CTL` address in that frame is RAZ/WI.

**CNTP_CTL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x02C</td>
<td>CNTP_CTL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x02C</td>
<td>CNTP_CTL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
CNTP_CVAL, Counter-timer Physical Timer CompareValue

The CNTP_CVAL characteristics are:

**Purpose**

Holds the 64-bit compare value for the EL1 physical timer.

**Configuration**

The power domain of CNTP_CVAL is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTP_CVAL is a 64-bit register.

**Field descriptions**

The CNTP_CVAL bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**CompareValue, bits [63:0]**

Holds the EL1 physical timer CompareValue.

When CNTP_CTL.ENABLE is 1, the timer condition is met when (CNTPCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTP_CTL.ISTATUS is set to 1.
- An interrupt is generated if CNTP_CTL.IMASK is 0.

When CNTP_CTL.ENABLE is 0, the timer condition is not met, but CNTPCT continues to count.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTP_CVAL**

CNTP_CVAL can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTP_CVAL is accessible in that frame if the value of CNTACR<n>.RWPT is 1.
• Otherwise, the CNTP_CVAL address in that frame is RAZ/WI.

For an implemented CNTELOBaseN frame:

• CNTP_CVAL is accessible in that frame if both:
  ◦ CNTP_CVAL is accessible in the corresponding CNTBaseN frame:
  ◦ The value of CNTELOACR_EL0PTEN is 1.
• Otherwise, the CNTP_CVAL address in that frame is RAZ/WI.

If the implementation supports 64-bit atomic accesses, then the CNTP_CVAL register must be accessible as an atomic 64-bit value.

**CNTP_CVAL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x020</td>
<td>CNTP_CVAL</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x024</td>
<td>CNTP_CVAL</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x020</td>
<td>CNTP_CVAL</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x024</td>
<td>CNTP_CVAL</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

30/09/2020 15:07; ccead0cb9f089f9ceec50268e82aec9e71047211

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CNTP_TVAL, Counter-timer Physical Timer TimerValue

The CNTP_TVAL characteristics are:

**Purpose**

Holds the timer value for the EL1 physical timer.

**Configuration**

The power domain of CNTP_TVAL is **IMPLEMENTATION DEFINED**.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTP_TVAL is a 32-bit register.

**Field descriptions**

The CNTP_TVAL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**TimerValue, bits [31:0]**

The TimerValue view of the EL1 physical timer.

On a read of this register:

- If CNTP_CTL.ENABLE is 0, the value returned is **UNKNOWN**.
- If CNTP_CTL.ENABLE is 1, the value returned is (CompareValue - CNTPCT).

On a write of this register, CompareValue is set to (CNTPCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTP_CTL.ENABLE is 1, the timer condition is met when (CNTPCT - CompareValue) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTP_CTL.ISTATUS is set to 1.
- If CNTP_CTL.IMASK is 0, an interrupt is generated.

When CNTP_CTL.ENABLE is 0, the timer condition is not met, but CNTPCT continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the CNTP_TVAL**

CNTP_TVAL can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.
For an implemented CNTBaseN frame:

- CNTP_TVAL is accessible in that frame if the value of CNTACR<n> RWPT is 1.
- Otherwise, the CNTP_TVAL address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTP_TVAL is accessible in that frame if both:
  - CNTP_TVAL is accessible in the corresponding CNTBaseN frame:
  - The value of CNTEL0ACR EL0PTEN is 1.
- Otherwise, the CNTP_TVAL address in that frame is RAZ/WI.

**CNTP_TVAL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x028</td>
<td>CNTP_TVAL</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x028</td>
<td>CNTP_TVAL</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
CNTPCT, Counter-timer Physical Count

The CNTPCT characteristics are:

**Purpose**

Holds the 64-bit physical count value.

**Configuration**

The power domain of CNTPCT is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTPCT is a 64-bit register.

**Field descriptions**

The CNTPCT bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Physical count value</td>
</tr>
<tr>
<td>62</td>
<td>Physical count value</td>
</tr>
<tr>
<td>31</td>
<td>Physical count value</td>
</tr>
<tr>
<td>30</td>
<td>Physical count value</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Physical count value.

**Accessing the CNTPCT**

CNTPCT can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame, as a RO register.

'CNTCTRL base status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTPCT is accessible in that frame, as a RO register, if the value of CNTACR<RPCT> is 1.
- Otherwise, the CNTPCT address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTPCT is accessible in that frame if both:
  - CNTPCT is accessible in the corresponding CNTBaseN frame.
  - The value of CNTEL0ACR EL0PCTEN is 1.
- Otherwise, the CNTPCT address in that frame is RAZ/WI.

If the implementation supports 64-bit atomic accesses, then the CNTPCT register must be accessible as an atomic 64-bit value.
### CNTPCT can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x000</td>
<td>CNTPCT</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x004</td>
<td>CNTPCT</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x000</td>
<td>CNTPCT</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x004</td>
<td>CNTPCT</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The CNTSCR characteristics are:

**Purpose**

Enables the counter, controls the counter frequency setting, and controls counter behavior during debug.

**Configuration**

The power domain of CNTSCR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_CNTSC is implemented. Otherwise, direct accesses to CNTSCR are RES0.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTSCR is a 32-bit register.

**Field descriptions**

The CNTSCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ScaleVal

**ScaleVal, bits [31:0]**

Scale Value

When counter scaling is enabled, ScaleVal is the amount added to the counter value for every counter tick.

Counter tick is defined as one period of the current operating frequency of the Generic counter.

ScaleVal is expressed as an unsigned fixed point number with an 8-bit integer value and a 24-bit fractional value.

CNTSCR.ScaleVal can only be changed when CNTCR.EN == 0. If the value of this field is changed when CNTCR.EN == 1:

- The counter value becomes UNKNOWN.
- The counter value remains UNKNOWN on future ticks of the clock.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTSCR**

In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, that includes this register, is implemented only in the Secure memory map.

**CNTSCR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x10</td>
<td>CNTSCR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
CNTSR, Counter Status Register

The CNTSR characteristics are:

**Purpose**

Provides counter frequency status information.

**Configuration**

The power domain of CNTSR is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTSR is a 32-bit register.

**Field descriptions**

The CNTSR bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| FCACK |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| RES0 |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| DBGH |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |

**FCACK, bits [31:8]**

Frequency change acknowledge. Indicates the currently selected entry in the Frequency modes table, see 'The Frequency modes table'.

On a Warm reset, this field resets to 0.

**Bits [7:2]**

Reserved, RES0.

**DBGH, bit [1]**

Indicates whether the counter is halted because the Halt-on-debug signal is asserted:

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Counter is not halted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Counter is halted.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bit [0]**

Reserved, RES0.

**Accessing the CNTSR**

In a system that supports Secure and Non-secure memory maps the CNTControlBase frame, that includes this register, is implemented only in the Secure memory map.
CNTSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0x004</td>
<td>CNTSR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CNTTIDR, Counter-timer Timer ID Register

The CNTTIDR characteristics are:

**Purpose**

Indicates the implemented timers in the memory map, and their features. For each value of N from 0 to 7 it indicates whether:

- Frame CNTBaseN is a view of an implemented timer.
- Frame CNTBaseN has a second view, CNTEL0BaseN.
- Frame CNTBaseN has a virtual timer capability.

**Configuration**

The power domain of CNTTIDR is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTTIDR is a 32-bit register.

**Field descriptions**

The CNTTIDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Frame7 | Frame6 | Frame5 | Frame4 | Frame3 | Frame2 | Frame1 | Frame0 |

**Frame<n>, bits [4n+3:4n], for n = 7 to 0**

A 4-bit field indicating the features of frame CNTBase<n>.

Bit[3] of the field is RES0.

Bit[2], the FEL0 subfield, indicates whether frame CNTBase<n> has a second view, CNTEL0Base<n>. The possible values of this bit are:

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Frame&lt;n&gt; does not have a second view. The CNTEL0ACR register in the first view of the frame is RES0</td>
</tr>
<tr>
<td>0b1</td>
<td>Frame&lt;n&gt; has a second view, CNTEL0Base&lt;n&gt;</td>
</tr>
</tbody>
</table>

If bit[0] is 0, bit[2] is RES0.

Bit[1], the FVI subfield, indicates whether both:

- Frame CNTBase<n> implements the virtual timer registers CNTV_CVAL, CNTV_TVAL, and CNTV_CTL.
- This CNTCTLBase frame implements the virtual timer offset register CNTVOFF<n>.

The possible values of bit[1] are:

<table>
<thead>
<tr>
<th>Bit[1]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Frame&lt;n&gt; does not have virtual capability. The virtual time and offset registers are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Frame&lt;n&gt; has virtual capability. The virtual time and offset registers are implemented</td>
</tr>
</tbody>
</table>

If bit[0] is 0, bit[1] is RES0.
Bit[0], the FI subfield, indicates whether frame CNTBase<n> is implemented. The possible values of this bit are:

<table>
<thead>
<tr>
<th>Bit[0]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Frame&lt;n&gt; is not implemented. All registers associated with the frame are RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Frame&lt;n&gt; is implemented</td>
</tr>
</tbody>
</table>

### Accessing the CNTTIDR

In a system that recognizes two Security states this register is accessible by both Secure and Non-secure accesses.

**CNTTIDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>0x008</td>
<td>CNTTIDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CNTV_CTL, Counter-timer Virtual Timer Control

The CNTV_CTL characteristics are:

**Purpose**

Control register for the virtual timer.

**Configuration**

The power domain of CNTV_CTL is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTV_CTL is a 32-bit register.

**Field descriptions**

The CNTV_CTL bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>ISTATUS</td>
<td>IMASK</td>
<td>ENABLE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**ISTATUS, bit [2]**

The status of the timer. This bit indicates whether the timer condition is met:

<table>
<thead>
<tr>
<th>ISTATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer condition is not met.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer condition is met.</td>
</tr>
</tbody>
</table>

When the value of the ENABLE bit is 1, ISTATUS indicates whether the timer condition is met. ISTATUS takes no account of the value of the IMASK bit. If the value of ISTATUS is 1 and the value of IMASK is 0 then the timer interrupt is asserted.

When the value of the ENABLE bit is 0, the ISTATUS field is UNKNOWN.

This bit is read-only.

**IMASK, bit [1]**

Timer interrupt mask bit. Permitted values are:

<table>
<thead>
<tr>
<th>IMASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer interrupt is not masked by the IMASK bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer interrupt is masked by the IMASK bit.</td>
</tr>
</tbody>
</table>

For more information, see the description of the ISTATUS bit.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
ENABLE, bit [0]

Enables the timer. Permitted values are:

<table>
<thead>
<tr>
<th>ENABLE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Timer disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Timer enabled.</td>
</tr>
</tbody>
</table>

Setting this bit to 0 disables the timer output signal, but the timer value accessible from CNTV_TVAL continues to count down.

**Note**

Disabling the output signal might be a power-saving option.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Accessing the CNTV_CTL

CNTV_CTL can be implemented in any implemented CNTBaseN frame that has virtual timer capability, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame that has virtual timer capability:

- CNTV_CTL is accessible in that frame if the value of CNTACR<n>.RWVT is 1.
- Otherwise, the CNTV_CTL address in that frame is RAZ/NI.

For an implemented CNTEL0BaseN frame:

- CNTV_CTL is accessible in that frame if both:
  - CNTV_CTL is accessible in the corresponding CNTBaseN frame:
  - The value of CNTEL0ACR.EL0VTEN is 1.
- Otherwise, the CNTV_CTL address in that frame is RAZ/NI.

### CNTV_CTL can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x03C</td>
<td>CNTV_CTL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x03C</td>
<td>CNTV_CTL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
The CNTV_CVAL characteristics are:

**Purpose**

Holds the 64-bit compare value for the virtual timer.

**Configuration**

The power domain of CNTV_CVAL is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTV_CVAL is a 64-bit register.

**Field descriptions**

The CNTV_CVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CompareValue</td>
</tr>
<tr>
<td>62</td>
<td>CompareValue</td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CompareValue</td>
</tr>
</tbody>
</table>

**CompareValue, bits [63:0]**

Holds the virtual timer CompareValue.

When CNTV_CTL.ENABLE is 1, the timer condition is met when (CNTVCT - CompareValue) is greater than or equal to zero. This means that CompareValue acts like a 64-bit upcounter timer. When the timer condition is met:

- CNTV_CTL.ISTATUS is set to 1.
- An interrupt is generated if CNTV_CTL.IMASK is 0.

When CNTV_CTL.ENABLE is 0, the timer condition is not met, but CNTVCT continues to count.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTV_CVAL**

CNTV_CVAL can be implemented in any implemented CNTBaseN frame that has virtual timer capability, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBases status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame that has virtual timer capability:

- CNTV_CVAL is accessible in that frame if the value of CNTACR<n>.RWVT is 1.
• Otherwise, the CNTV_CVAL address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

• CNTV_CVAL is accessible in that frame if both:
  ◦ CNTV_CVAL is accessible in the corresponding CNTBaseN frame:
  ◦ The value of CNTEL0ACR_EL0VTEN is 1.
  • Otherwise, the CNTV_CVAL address in that frame is RAZ/WI.

If the implementation supports 64-bit atomic accesses, then the CNTV_CVAL register must be accessible as an atomic 64-bit value.

CNTV_CVAL can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x030</td>
<td>CNTV_CVAL</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x034</td>
<td>CNTV_CVAL</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x030</td>
<td>CNTV_CVAL</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x034</td>
<td>CNTV_CVAL</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
CNTV_TVAL, Counter-timer Virtual Timer TimerValue

The CNTV_TVAL characteristics are:

**Purpose**

Holds the timer value for the virtual timer.

**Configuration**

The power domain of CNTV_TVAL is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTV_TVAL is a 32-bit register.

**Field descriptions**

The CNTV_TVAL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>TimerValue</td>
</tr>
</tbody>
</table>

**TimerValue, bits [31:0]**

The TimerValue view of the virtual timer.

On a read of this register:

- If CNTV_CTL.ENABLE is 0, the value returned is UNKNOWN.
- If CNTV_CTL.ENABLE is 1, the value returned is (CompareValue - CNTVCT).

On a write of this register, CompareValue is set to (CNTVCT + TimerValue), where TimerValue is treated as a signed 32-bit integer.

When CNTV_CTL.ENABLE is 1, the timer condition is met when (CNTVCT - CompareValue) is greater than or equal to zero. This means that TimerValue acts like a 32-bit downcounter timer. When the timer condition is met:

- CNTV_CTL.ISTATUS is set to 1.
- If CNTV_CTL.IMASK is 0, an interrupt is generated.

When CNTV_CTL.ENABLE is 0, the timer condition is not met, but CNTVCT continues to count, so the TimerValue view appears to continue to count down.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTV_TVAL**

CNTV_TVAL can be implemented in any implemented CNTBaseN frame that has virtual timer capability, and in the corresponding CNTEL0BaseN frame.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.
For an implemented CNTBaseN frame that has virtual timer capability:

- CNTV_TVAL is accessible in that frame if the value of CNTACR<n>.RWVT is 1.
- Otherwise, the CNTV_TVAL address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTV_TVAL is accessible in that frame if both:
  - CNTV_TVAL is accessible in the corresponding CNTBaseN frame:
  - The value of CNTEL0ACR.EL0VTEN is 1.
- Otherwise, the CNTV_TVAL address in that frame is RAZ/WI.

**CNTV_TVAL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x038</td>
<td>CNTV_TVAL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x038</td>
<td>CNTV_TVAL</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

30/09/2020 15:06; ccead0cb9f089f9ceec50268e82aec9e71047211

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CNTVCT, Counter-timer Virtual Count

The CNTVCT characteristics are:

Purpose

Holds the 64-bit virtual count value.

Configuration

The power domain of CNTVCT is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

Attributes

CNTVCT is a 64-bit register.

Field descriptions

The CNTVCT bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

Virtual count value

Virtual count value

Bits [63:0]

Virtual count value.

Accessing the CNTVCT

CNTVCT can be implemented in any implemented CNTBaseN frame, and in the corresponding CNTEL0BaseN frame, as a RO register.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame:

- CNTVCT is accessible in that frame, as a RO register, if the value of CNTACR<n>.RVCT is 1.
- Otherwise, the CNTVCT address in that frame is RAZ/WI.

For an implemented CNTEL0BaseN frame:

- CNTVCT is accessible in that frame if both:
  - CNTVCT is accessible in the corresponding CNTBaseN frame.
  - The value of CNTEL0ACR.EL0VCTEN is 1.
- Otherwise, the CNTVCT address in that frame is RAZ/WI.

If the implementation supports 64-bit atomic accesses, then the CNTVCT register must be accessible as an atomic 64-bit value.
CNTVCT can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x008</td>
<td>CNTVCT</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x00C</td>
<td>CNTVCT</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x008</td>
<td>CNTVCT</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0x00C</td>
<td>CNTVCT</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CNTVOFF, Counter-timer Virtual Offset

The CNTVOFF characteristics are:

Purpose

Holds the 64-bit virtual offset for a CNTBaseN frame that has virtual timer capability. This is the offset between real time and virtual time.

Configuration

The power domain of CNTVOFF is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

Attributes

CNTVOFF is a 64-bit register.

Field descriptions

The CNTVOFF bit assignments are:

| Bit 63 | Bit 62 | Bit 61 | Bit 60 | Bit 59 | Bit 58 | Bit 57 | Bit 56 | Bit 55 | Bit 54 | Bit 53 | Bit 52 | Bit 51 | Bit 50 | Bit 49 | Bit 48 | Bit 47 | Bit 46 | Bit 45 | Bit 44 | Bit 43 | Bit 42 | Bit 41 | Bit 40 | Bit 39 | Bit 38 | Bit 37 | Bit 36 | Bit 35 | Bit 34 | Bit 33 | Bit 32 |
|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
|        |       | Virtual offset |       |       | Virtual offset |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |       |

Bits [63:0]

Virtual offset.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the CNTVOFF

CNTVOFF is implemented, as a RO register, in any implemented CNTBaseN frame that has virtual timer capability.

'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a CNTBaseN frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.

For an implemented CNTBaseN frame that has virtual timer capability:

- CNTVOFF is accessible in that frame, as a RO register, if the value of CNTACR<n>.RVOFF is 1.
- Otherwise, the CNTVOFF address in that frame is RAZ/WI.

Note

CNTVOFF is never visible in any CNTEL0BaseN frame. This means that the CNTVOFF address in any implemented CNTEL0BaseN frame is RAZ/WI.

In an implementation that supports 64-bit atomic accesses, a CNTVOFF{<n>} register must be accessible as an atomic 64-bit value.
CNTVOFF can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x018</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0x01C</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The CNTVOFF<n> characteristics are:

**Purpose**

Holds the 64-bit virtual offset for frame CNTBase<n>. This is the offset between real time and virtual time.

**Configuration**

The power domain of CNTVOFF<n> is IMPLEMENTATION DEFINED.

Implementation of this register is OPTIONAL.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

**Attributes**

CNTVOFF<n> is a 64-bit register.

**Field descriptions**

The CNTVOFF<n> bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Virtual offset</td>
<td></td>
<td></td>
<td>Virtual offset</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Virtual offset.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CNTVOFF<n>**

In the CNTCTLBase frame a CNTVOFF<n> register must be implemented, as a RW register, for each CNTBaseN frame that has virtual timer capability. For more information, see ‘CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames’.

---

**Note**

The value of <n> in an instance of CNTVOFF<n> specifies the value of N for the associated CNTBaseN frame.

---

In a system that recognizes two Security states, for any CNTVOFF<n> register in the CNTCTLBase frame:

- CNTVOFF<n> is always accessible by Secure accesses.
- CNTNSAR.NS<n> determines whether CNTVOFF<n> is accessible by Non-secure accesses.

The register location of any unimplemented CNTVOFF<n> register in the CNTCTLBase frame is RAZ/WI.

The CNTVOFF<n> register is accessible in the CNTBaseN frame using CNTVOFF.

In an implementation that supports 64-bit atomic accesses, then the CNTVOFF<n> registers must be accessible as atomic 64-bit values.
CNTVOFF\(<n>\), Counter-timer Virtual Offsets, \(n = 0 - 7\)

CNTVOFF\(<n>\) can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>(0x080 + (8 \times n))</td>
<td>31:0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>(0x084 + (8 \times n))</td>
<td>63:32</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
CounterID\(<n>\), Counter ID registers, \(n = 0 - 11\)

The CounterID\(<n>\) characteristics are:

**Purpose**

IMPLEMENTATION DEFINED identification registers 0 to 11 for the memory-mapped Generic Timer.

**Configuration**

The power domain of CounterID\(<n>\) is IMPLEMENTATION DEFINED.

For more information, see 'Power and reset domains for the system level implementation of the Generic Timer'.

These registers are implemented independently in each of the implemented Generic Timer memory-mapped frames.

If the implementation of the Counter ID registers requires an architecture version, the value for this version of the Arm Generic Timer is version 0.

The Counter ID registers can be implemented as a set of CoreSight ID registers, comprising Peripheral ID Registers and Component ID Registers. An implementation of these registers for the Generic Timer must use a Component class value of 0xF.

**Attributes**

CounterID\(<n>\) is a 32-bit register.

**Field descriptions**

The CounterID\(<n>\) bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

**Accessing the CounterID\(<n>\)**

These registers must be implemented, as RO registers, in every implemented Generic Timer memory-mapped frame.

For the CNTCTLBase frame, in a system that recognizes two Security states these registers are accessible by both Secure and Non-secure accesses.

For the CNTControlBase frame, in a system that supports Secure and Non-secure memory maps the frame is implemented only in the Secure memory map, meaning these registers are implemented only in the Secure memory map.

For the CNTBaseN frames, 'CNTCTLBase status and control fields for the CNTBaseN and CNTEL0BaseN frames' describes the status fields that identify whether a frame is implemented, and for an implemented frame:

- Whether the CNTBaseN frame has virtual timer capability.
- Whether the corresponding CNTEL0BaseN frame is implemented.
- For an implementation that recognizes two Security states, whether the CNTBaseN frame, and any corresponding CNTEL0BaseN frame, is accessible by Non-secure accesses.
CounterID<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTControlBase</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTReadBase</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTBaseN</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTEL0BaseN</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer</td>
<td>CNTCTLBase</td>
<td>0xFD0 + (4 * n)</td>
<td>CounterID&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIAPPCLEAR, CTI Application Trigger Clear register

The CTIAPPCLEAR characteristics are:

**Purpose**

Clears bits of the Application Trigger register.

**Configuration**

CTIAPPCLEAR is in the Debug power domain.

**Attributes**

CTIAPPCLEAR is a 32-bit register.

**Field descriptions**

The CTIAPPCLEAR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>APPCLEAR31</td>
<td>APPCLEAR30</td>
<td>APPCLEAR29</td>
<td>APPCLEAR28</td>
<td>APPCLEAR27</td>
<td>APPCLEAR26</td>
<td>APPCLEAR25</td>
<td>APPCLEAR24</td>
<td>APPCLEAR23</td>
<td>APPCLEAR22</td>
<td>APPCLEAR21</td>
<td>APPCLEAR20</td>
<td>APPCLEAR19</td>
<td>APPCLEAR18</td>
<td>APPCLEAR17</td>
<td>APPCLEAR16</td>
<td>APPCLEAR15</td>
<td>APPCLEAR14</td>
<td>APPCLEAR13</td>
<td>APPCLEAR12</td>
<td>APPCLEAR11</td>
<td>APPCLEAR10</td>
<td>APPCLEAR9</td>
<td>APPCLEAR8</td>
<td>APPCLEAR7</td>
<td>APPCLEAR6</td>
<td>APPCLEAR5</td>
<td>APPCLEAR4</td>
<td>APPCLEAR3</td>
<td>APPCLEAR2</td>
<td>APPCLEAR1</td>
<td>APPCLEAR0</td>
</tr>
</tbody>
</table>

APPCLEAR<x>, bit [x], for x = 31 to 0

Application trigger <x> disable.

Bits [31:N] are RAZ/WI. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

Writing to this bit has the following effect:

<table>
<thead>
<tr>
<th>APBOX=0x0</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>No effect.</td>
<td>Clear corresponding bit in CTIAPPTRIG to 0 and clear the corresponding channel event.</td>
<td></td>
</tr>
</tbody>
</table>

If the ECT does not support multicycle channel events, use of CTIAPPCLEAR is deprecated and the debugger must only use CTIAPPULSE.

**Accessing the CTIAPPCLEAR**

CTIAPPCLEAR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x018</td>
<td>CTIAPPCLEAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are WI.
- When !SoftwareLockStatus() accesses to this register are WO.
CTIAPPPULSE, CTI Application Pulse register

The CTIAPPPULSE characteristics are:

**Purpose**

Causes event pulses to be generated on ECT channels.

**Configuration**

CTIAPPPULSE is in the Debug power domain.

**Attributes**

CTIAPPPULSE is a 32-bit register.

**Field descriptions**

The CTIAPPPULSE bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| APPPULSE31 | APPPULSE30 | APPPULSE29 | APPPULSE28 | APPPULSE27 | APPPULSE26 | APPPULSE25 | APPPULSE24 | APPPULSE23 | APPPULSE22 | APPPULSE21 | APPPULSE20 | APPPULSE19 | APPPULSE18 | APPPULSE17 | APPPULSE16 | APPPULSE15 | APPPULSE14 | APPPULSE13 | APPPULSE12 | APPPULSE11 | APPPULSE10 | APPPULSE9 | APPPULSE8 | APPPULSE7 | APPPULSE6 | APPPULSE5 | APPPULSE4 | APPPULSE3 | APPPULSE2 | APPPULSE1 | APPPULSE0 |

APPPULSE<x>, bit [x], for x = 31 to 0

Generate event pulse on ECT channel <x>.

Bits [31:N] are RAZ/WI. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

Writing to this bit has the following effect:

<table>
<thead>
<tr>
<th>APPPULSE&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>Channel &lt;x&gt; event pulse generated.</td>
</tr>
</tbody>
</table>

**Note**

- The CTIAPPPULSE operation does not affect the state of the Application Trigger register, CTIAPPTRIG. If the channel is active, either because of an earlier event or from the application trigger, then the value written to CTIAPPPULSE might have no effect.
- Multiple pulse events that occur close together might be merged into a single pulse event.

**Accessing the CTIAPPPULSE**

It is constrained unpredictable whether a write to CTIAPPPULSE generates an event on a channel if CTICONTROL.GLBEN is 0.

CTIAPPPULSE can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x01C</td>
<td>CTIAPPPULSE</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are WI.
- When !SoftwareLockStatus() accesses to this register are WO.
CTIAPPSET, CTI Application Trigger Set register

The CTIAPPSET characteristics are:

**Purpose**

Sets bits of the Application Trigger register.

**Configuration**

CTIAPPSET is in the Debug power domain.

**Attributes**

CTIAPPSET is a 32-bit register.

**Field descriptions**

The CTIAPPSET bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>APPSET31</td>
</tr>
<tr>
<td>30</td>
<td>APPSET30</td>
</tr>
<tr>
<td>29</td>
<td>APPSET29</td>
</tr>
<tr>
<td>28</td>
<td>APPSET28</td>
</tr>
<tr>
<td>27</td>
<td>APPSET27</td>
</tr>
<tr>
<td>26</td>
<td>APPSET26</td>
</tr>
<tr>
<td>25</td>
<td>APPSET25</td>
</tr>
<tr>
<td>24</td>
<td>APPSET24</td>
</tr>
<tr>
<td>23</td>
<td>APPSET23</td>
</tr>
<tr>
<td>22</td>
<td>APPSET22</td>
</tr>
<tr>
<td>21</td>
<td>APPSET21</td>
</tr>
<tr>
<td>20</td>
<td>APPSET20</td>
</tr>
<tr>
<td>19</td>
<td>APPSET19</td>
</tr>
<tr>
<td>18</td>
<td>APPSET18</td>
</tr>
<tr>
<td>17</td>
<td>APPSET17</td>
</tr>
<tr>
<td>16</td>
<td>APPSET16</td>
</tr>
<tr>
<td>15</td>
<td>APPSET15</td>
</tr>
<tr>
<td>14</td>
<td>APPSET14</td>
</tr>
<tr>
<td>13</td>
<td>APPSET13</td>
</tr>
<tr>
<td>12</td>
<td>APPSET12</td>
</tr>
<tr>
<td>11</td>
<td>APPSET11</td>
</tr>
<tr>
<td>10</td>
<td>APPSET10</td>
</tr>
<tr>
<td>9</td>
<td>APPSET9</td>
</tr>
<tr>
<td>8</td>
<td>APPSET8</td>
</tr>
<tr>
<td>7</td>
<td>APPSET7</td>
</tr>
<tr>
<td>6</td>
<td>APPSET6</td>
</tr>
<tr>
<td>5</td>
<td>APPSET5</td>
</tr>
<tr>
<td>4</td>
<td>APPSET4</td>
</tr>
<tr>
<td>3</td>
<td>APPSET3</td>
</tr>
<tr>
<td>2</td>
<td>APPSET2</td>
</tr>
<tr>
<td>1</td>
<td>APPSET1</td>
</tr>
<tr>
<td>0</td>
<td>APPSET0</td>
</tr>
</tbody>
</table>

APPSET<x>, bit [x], for x = 31 to 0

Application trigger <x> enable.

Bits [31:N] are RAZ/WI. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

<table>
<thead>
<tr>
<th>APPSET&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reading this means the application trigger is inactive. Writing this has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reading this means the application trigger is active. Writing this sets the corresponding bit in CTIAPPTRIG to 1 and generates a channel event.</td>
</tr>
</tbody>
</table>

If the ECT does not support multicycle channel events, use of CTIAPPSET is deprecated and the debugger must only use CTIAPPULSE.

On an External debug reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CTIAPPSET**

CTIAPPSET can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x014</td>
<td>CTIAPPSET</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are RO.
- When !SoftwareLockStatus() accesses to this register are RW.
The CTIAUTHSTATUS characteristics are:

**Purpose**

Provides information about the state of the IMPLEMENTATION DEFINED authentication interface for CTI.

**Configuration**

CTIAUTHSTATUS is in the Debug power domain.

This register is **OPTIONAL**, and is required for CoreSight compliance.

**Attributes**

CTIAUTHSTATUS is a 32-bit register.

**Field descriptions**

The CTIAUTHSTATUS bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>RAZ</td>
</tr>
<tr>
<td>29</td>
<td>NSNID</td>
</tr>
<tr>
<td>28</td>
<td>NSID</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**Bits [7:4]**

Reserved, RAZ.

**NSNID, bits [3:2]**

If EL3 is implemented, this field holds the same value as DBGAUTHSTATUS_EL1.NSNID.

If EL3 is not implemented and the implemented Security state is Secure state, this field holds the same value as DBGAUTHSTATUS_EL1.SNID.

**NSID, bits [1:0]**

If EL3 is implemented, this field holds the same value as DBGAUTHSTATUS_EL1.NSID.

If EL3 is not implemented and the implemented Security state is Secure state, this field holds the same value as DBGAUTHSTATUS_EL1.SID.

**Accessing the CTIAUTHSTATUS**

CTIAUTHSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFB8</td>
<td>CTIAUTHSTATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTICHINSTATUS, CTI Channel In Status register

The CTICHINSTATUS characteristics are:

**Purpose**

Provides the raw status of the ECT channel inputs to the CTI.

**Configuration**

CTICHINSTATUS is in the Debug power domain.

**Attributes**

CTICHINSTATUS is a 32-bit register.

**Field descriptions**

The CTICHINSTATUS bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
</tr>
</thead>
<tbody>
<tr>
<td>CHIN31</td>
<td>CHIN30</td>
<td>CHIN29</td>
<td>CHIN28</td>
<td>CHIN27</td>
<td>CHIN26</td>
<td>CHIN25</td>
<td>CHIN24</td>
<td>CHIN23</td>
<td>CHIN22</td>
<td>CHIN21</td>
<td>CHIN20</td>
<td>CHIN19</td>
<td>CHIN18</td>
<td>CHIN17</td>
</tr>
</tbody>
</table>

CHIN<n>, bit [n], for n = 31 to 0

Input channel <n> status.

Bits [31:N] are RAZ. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

<table>
<thead>
<tr>
<th>CHIN&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input channel &lt;n&gt; is inactive.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input channel &lt;n&gt; is active.</td>
</tr>
</tbody>
</table>

If the ECT channels do not support multicycle events then it is IMPLEMENTATION DEFINED whether an input channel can be observed as active.

**Accessing the CTICHINSTATUS**

CTICHINSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x138</td>
<td>CTICHINSTATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The CTICHOUTSTATUS characteristics are:

**Purpose**

Provides the status of the ECT channel outputs from the CTI.

**Configuration**

CTICHOUTSTATUS is in the Debug power domain.

**Attributes**

CTICHOUTSTATUS is a 32-bit register.

**Field descriptions**

The CTICHOUTSTATUS bit assignments are:

| Bit | CHOUT31 | CHOUT30 | CHOUT29 | CHOUT28 | CHOUT27 | CHOUT26 | CHOUT25 | CHOUT24 | CHOUT23 | CHOUT22 | CHOUT21 | CHOUT20 | CHOUT19 | CHOUT18 | CHOUT17 | CHOUT16 | CHOUT15 | CHOUT14 | CHOUT13 | CHOUT12 | CHOUT11 | CHOUT10 | CHOUT9 | CHOUT8 | CHOUT7 | CHOUT6 | CHOUT5 | CHOUT4 | CHOUT3 | CHOUT2 | CHOUT1 | CHOUT0 |
|-----|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|---------|

CHOUT<n>, bit [n], for n = 31 to 0

Output channel <n> status.

Bits [31:N] are RAZ. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

Possible values of this bit are:

<table>
<thead>
<tr>
<th>CHOUT&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Output channel &lt;n&gt; is inactive.</td>
</tr>
<tr>
<td>0b1</td>
<td>Output channel &lt;n&gt; is active.</td>
</tr>
</tbody>
</table>

If the ECT channels do not support multicycle events then it is IMPLEMENTATION DEFINED whether an output channel can be observed as active.

**Note**

The value in CTICHOUTSTATUS is after gating by the channel gate. For more information, see CTIGATE.

**Accessing the CTICHOUTSTATUS**

CTICHOUTSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x13C</td>
<td>CTICHOUTSTATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTICIDR0, CTI Component Identification Register 0

The CTICIDR0 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

CTICIDR0 is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

This register is required for CoreSight compliance.

**Attributes**

CTICIDR0 is a 32-bit register.

**Field descriptions**

The CTICIDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>7-0</td>
<td>Preamble, PRMBL_0</td>
<td>0x0D</td>
</tr>
</tbody>
</table>

**Accessing the CTICIDR0**

CTICIDR0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFF0</td>
<td>CTICIDR0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTICIDR1, CTI Component Identification Register 1

The CTICIDR1 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

CTICIDR1 is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

This register is required for CoreSight compliance.

**Attributes**

CTICIDR1 is a 32-bit register.

**Field descriptions**

The CTICIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td><strong>RES0</strong></td>
</tr>
<tr>
<td>30</td>
<td><strong>CLASS</strong></td>
</tr>
<tr>
<td>29</td>
<td><strong>PRMBL_1</strong></td>
</tr>
<tr>
<td>28</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>27</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>26</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>25</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>24</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>23</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>22</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>21</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>20</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>19</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>18</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>17</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>16</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>15</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>14</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>13</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>12</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>11</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>10</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>9</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>8</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>7</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>6</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>5</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>4</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>3</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>2</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>1</td>
<td><strong>Reserved</strong></td>
</tr>
<tr>
<td>0</td>
<td><strong>Reserved</strong></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, **RES0**.

**CLASS, bits [7:4]**

Component class.

<table>
<thead>
<tr>
<th>CLASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1001</td>
<td>CoreSight component.</td>
</tr>
</tbody>
</table>

Other values are defined by the CoreSight Architecture.

This field reads as **0x9**.

**PRMBL_1, bits [3:0]**

Preamble. RAZ.

Reads as **0b0000**.

**Accessing the CTICIDR1**

CTICIDR1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFF4</td>
<td>CTICIDR1</td>
</tr>
</tbody>
</table>
Accesses on this interface are **RO**.
CTICIDR2, CTI Component Identification Register 2

The CTICIDR2 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

CTICIDR2 is in the Debug power domain.

Implementation of this register is OPTIONAL.

This register is required for CoreSight compliance.

**Attributes**

CTICIDR2 is a 32-bit register.

**Field descriptions**

The CTICIDR2 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_2, bits [7:0]**

Preamble.

Reads as 0x05.

**Accessing the CTICIDR2**

CTICIDR2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFF8</td>
<td>CTICIDR2</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTICDR3, CTI Component Identification Register 3

The CTICDR3 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

CTICDR3 is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

This register is required for CoreSight compliance.

**Attributes**

CTICDR3 is a 32-bit register.

**Field descriptions**

The CTICDR3 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | PRMBL_3 |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_3, bits [7:0]**

Preamble.

Reads as 0xB1.

**Accessing the CTICDR3**

**CTICDR3 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFFC</td>
<td>CTICDR3</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTICLAIMCLR, CTI CLAIM Tag Clear register

The CTICLAIMCLR characteristics are:

Purpose

Used by software to read the values of the CLAIM bits, and to clear CLAIM tag bits to 0.

Configuration

CTICLAIMCLR is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

Attributes

CTICLAIMCLR is a 32-bit register.

Field descriptions

The CTICLAIMCLR bit assignments are:

CLAIM31 CLAIM30 CLAIM29 CLAIM28 CLAIM27 CLAIM26 CLAIM25 CLAIM24 CLAIM23 CLAIM22 CLAIM21 CLAIM20 CLAIM19 CLAIM18 CLAIM17 CLAIM16 CLAIM15 CLAIM14 CLAIM13 CLAIM12 CLAIM11 CLAIM10 CLAIM9 CLAIM8 CLAIM7 CLAIM6 CLAIM5 CLAIM4 CLAIM3 CLAIM2 CLAIM1 CLAIM0

CLAIM<x>, bit [x], for x = 31 to 0

CLAIM tag clear bit.

For values of x greater than or equal to the IMPLEMENTATION DEFINED number of CLAIM tags, this bit is RAZ/SBZ. Software can rely on these bits reading as zero, and must use a Should-Be-Zero policy on writes. Implementations must ignore writes.

For other values of x, reads return the value of CLAIM[x] and the behavior on writes is:

<table>
<thead>
<tr>
<th>CLAIM&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Indirectly clear CLAIM[x] to 0.</td>
</tr>
</tbody>
</table>

A single write to CTICLAIMCLR can clear multiple tags to 0.

An External Debug reset clears the CLAIM tag bits to 0.

Accessing the CTICLAIMCLR

CTICLAIMCLR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFA4</td>
<td>CTICLAIMCLR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are **RO**.
- When !SoftwareLockStatus() accesses to this register are **RW**.
The CTICLAIMSET characteristics are:

**Purpose**

Used by software to set CLAIM bits to 1.

**Configuration**

CTICLAIMSET is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

**Attributes**

CTICLAIMSET is a 32-bit register.

**Field descriptions**

The CTICLAIMSET bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLAIM31</td>
<td>CLAIM30</td>
<td>CLAIM29</td>
<td>CLAIM28</td>
<td>CLAIM27</td>
<td>CLAIM26</td>
<td>CLAIM25</td>
<td>CLAIM24</td>
<td>CLAIM23</td>
<td>CLAIM22</td>
<td>CLAIM21</td>
<td>CLAIM20</td>
<td>CLAIM19</td>
</tr>
</tbody>
</table>

CLAIM<x>, bit [x], for x = 31 to 0

CLAIM tag set bit.

For values of x greater than or equal to the IMPLEMENTATION DEFINED number of CLAIM tags, this bit is RAZ/SBZ. Software can rely on these bits reading as zero, and must use a Should-Be-Zero policy on writes. Implementations must ignore writes.

For other values of x, the bit is RAO and the behavior on writes is:

<table>
<thead>
<tr>
<th>CLAIM&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Indirectly set CLAIM[x] tag to 1.</td>
</tr>
</tbody>
</table>

A single write to CTICLAIMSET can set multiple tags to 1.

An External Debug reset clears the CLAIM tag bits to 0.

**Accessing the CTICLAIMSET**

CTICLAIMSET can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFA0</td>
<td>CTICLAIMSET</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are **RO**.
- When !SoftwareLockStatus() accesses to this register are **RW**.
CTICONTROL, CTI Control register

The CTICONTROL characteristics are:

**Purpose**

Controls whether the CTI is enabled.

**Configuration**

CTICONTROL is in the Debug power domain.

**Attributes**

CTICONTROL is a 32-bit register.

**Field descriptions**

The CTICONTROL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | GLBEN |

**Bits [31:1]**

Reserved, RES0.

**GLBEN, bit [0]**

Enables or disables the CTI mapping functions. Possible values of this field are:

<table>
<thead>
<tr>
<th>GLBEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>CTI mapping functions and application trigger disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>CTI mapping functions and application trigger enabled.</td>
</tr>
</tbody>
</table>

When GLBEN is 0, the input channel to output trigger, input trigger to output channel, and application trigger functions are disabled and do not signal new events on either output triggers or output channels. If a previously asserted output trigger has not been acknowledged, it remains asserted after the mapping functions are disabled. All output triggers are disabled by CTI reset.

If the ECT supports multicycle channel events any existing output channel events will be terminated.

On an External debug reset, this field resets to 0.

**Accessing the CTICONTROL**

CTICONTROL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x000</td>
<td>CTICONTROL</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are **RO**.
- When !SoftwareLockStatus() accesses to this register are **RW**.
The CTIDEVAFF0 characteristics are:

**Purpose**

Copy of the low half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the CTI component relates to.

**Configuration**

CTIDEVAFF0 is in the Debug power domain.

If the CTI is CTIv1, this register is *OPTIONAL*. If the CTI is CTIv2, this register is mandatory.

Arm recommends that the CTI is CTIv2.

In an Armv8.5 compliant implementation, the CTI must be CTIv2.

If this register is implemented, then CTIDEVAFF1 must also be implemented. If the CTI of a PE does not implement the CTI Device Affinity registers, the CTI block of the external debug memory map must be located 64KB above the debug registers in the external debug interface.

**Attributes**

CTIDEVAFF0 is a 32-bit register.

**Field descriptions**

The CTIDEVAFF0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>MPIDR_EL1lo, bits [31:0]</td>
</tr>
</tbody>
</table>

MPIDR_EL1lo, bits [31:0]

MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the CTIDEVAFF0**

CTIDEVAFF0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFA8</td>
<td>CTIDEVAFF0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The CTIDEVAFF1 characteristics are:

**Purpose**

Copy of the high half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the CTI component relates to.

**Configuration**

CTIDEVAFF1 is in the Debug power domain.

If the CTI is CTIv1, this register is **OPTIONAL**. If the CTI is CTIv2, this register is mandatory.

Arm recommends that the CTI is CTIv2.

In an Armv8.5 compliant implementation, the CTI must be CTIv2.

If this register is implemented, then CTIDEVAFF0 must also be implemented. If the CTI of a PE does not implement the CTI Device Affinity registers, the CTI block of the external debug memory map must be located 64KB above the debug registers in the external debug interface.

**Attributes**

CTIDEVAFF1 is a 32-bit register.

**Field descriptions**

The CTIDEVAFF1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

MPIDR_EL1hi, bits [31:0]

MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the CTIDEVAFF1**

CTIDEVAFF1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFAC</td>
<td>CTIDEVAFF1</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIDEVARCH, CTI Device Architecture register

The CTIDEVARCH characteristics are:

**Purpose**

Identifies the programmers' model architecture of the CTI component.

**Configuration**

CTIDEVARCH is in the Debug power domain.

If the CTI is CTIv1, this register is **OPTIONAL**. If the CTI is CTIv2, this register is mandatory.

Arm recommends that the CTI is CTIv2.

In an Armv8.5 compliant implementation, the CTI must be CTIv2.

If this register is not implemented, CTIDEVAFF0 and CTIDEVAFF1 are also not implemented.

**Attributes**

CTIDEVARCH is a 32-bit register.

**Field descriptions**

The CTIDEVARCH bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    | ARCHITECT | PRESENT | REVISION | ARCHID |    |

**ARCHITECT, bits [31:21]**

Defines the architecture of the component. For CTI, this is Arm Limited.

Bits [31:28] are the JEP106 continuation code, 0x4.

Bits [27:21] are the JEP106 ID code, 0x3B.

**PRESENT, bit [20]**

When set to 1, indicates that the DEVARCH is present.

This field is 1 in Armv8.

**REVISION, bits [19:16]**

Revision.

Defines the architecture revision of the component.

<table>
<thead>
<tr>
<th>REVISION</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>First revision.</td>
<td></td>
</tr>
<tr>
<td>0b0001</td>
<td>As 0b0000, and also adds support for CTIDEVCCTL.</td>
<td>When FEAT_DoPD is implemented</td>
</tr>
</tbody>
</table>

All other values are reserved.
ARCHID, bits [15:0]

Defines this part to be an Armv8 debug component. For architectures defined by Arm this is further subdivided.

For CTI:

- Bits [15:12] are the architecture version, 0x1.
- Bits [11:0] are the architecture part number, 0xA14.

This corresponds to CTI architecture version CTIv2.

**Accessing the CTIDEVARCH**

CTIDEVARCH can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFBC</td>
<td>CTIDEVARCH</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTIDEVCTL, CTI Device Control register

The CTIDEVCTL characteristics are:

**Purpose**

Provides target-specific device controls

**Configuration**

CTIDEVCTL is in the Debug power domain.

This register is present only when FEAT_DoPD is implemented. Otherwise, direct accesses to CTIDEVCTL are RES0.

**Attributes**

CTIDEVCTL is a 32-bit register.

**Field descriptions**

The CTIDEVCTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>RCE</td>
</tr>
<tr>
<td>29</td>
<td>OSUCE</td>
</tr>
</tbody>
</table>

**Bits [31:2]**

Reserved, RES0.

**RCE, bit [1]**

Reset Catch Enable.

<table>
<thead>
<tr>
<th>RCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reset Catch debug event disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset Catch debug event enabled.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 0.

**OSUCE, bit [0]**

OS Unlock Catch Enable

<table>
<thead>
<tr>
<th>OSUCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Unlock Catch debug event disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Unlock Catch debug event enabled.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 0.

**Accessing the CTIDEVCTL**

CTIDEVCTL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x150</td>
<td>CTIDEVCTL</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When `SoftwareLockStatus()` accesses to this register are **RO**.
- When `!SoftwareLockStatus()` accesses to this register are **RW**.
The CTIDEVID characteristics are:

**Purpose**

Describes the CTI component to the debugger.

**Configuration**

CTIDEVID is in the Debug power domain.

**Attributes**

CTIDEVID is a 32-bit register.

**Field descriptions**

The CTIDEVID bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:26] RES0</td>
<td>Reserved, 0</td>
</tr>
<tr>
<td>[25:24] INOUT</td>
<td>Input/output options. Indicates presence of the input gate. If the CTM is not implemented or CTIv2 is not implemented, this field is RAZ.</td>
</tr>
<tr>
<td>[23:22] NUMCHAN</td>
<td>Number of ECT channels implemented. IMPLEMENTATION DEFINED. For Armv8, valid values are:</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>NUMCHAN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>3 channels (0..2) implemented.</td>
</tr>
<tr>
<td>0b00100</td>
<td>4 channels (0..3) implemented.</td>
</tr>
<tr>
<td>0b00101</td>
<td>5 channels (0..4) implemented.</td>
</tr>
<tr>
<td>0b00110</td>
<td>6 channels (0..5) implemented.</td>
</tr>
<tr>
<td></td>
<td>and so on up to 0b100000, 32 channels (0..31) implemented.</td>
</tr>
<tr>
<td></td>
<td>All other values are reserved.</td>
</tr>
</tbody>
</table>
Bits [15:14]

Reserved, RES0.

NUMTRIG, bits [13:8]

Number of triggers implemented. IMPLEMENTATION DEFINED. This is one more than the index of the largest trigger, rather than the actual number of triggers.

For Armv8, valid values are:

<table>
<thead>
<tr>
<th>NUMTRIG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000011</td>
<td>Up to 3 triggers (0..2) implemented.</td>
</tr>
<tr>
<td>0b001000</td>
<td>Up to 8 triggers (0..7) implemented.</td>
</tr>
<tr>
<td>0b001001</td>
<td>Up to 9 triggers (0..8) implemented.</td>
</tr>
<tr>
<td>0b001010</td>
<td>Up to 10 triggers (0..9) implemented.</td>
</tr>
</tbody>
</table>

...and so on up to 0b100000, 32 triggers (0..31) implemented.

All other values are reserved. If the PE contains a Trace extension, this field must be at least 0b001000. There is no guarantee that any of the implemented triggers, including the highest numbered, are connected to any components.

Bits [7:5]

Reserved, RES0.

EXTMUXNUM, bits [4:0]

Number of multiplexors available on triggers. This value is used in conjunction with External Control register, ASICCTL.

Accessing the CTIDEVID

CTIDEVID can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFC8</td>
<td>CTIDEVID</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTIDEVID1, CTI Device ID register 1

The CTIDEVID1 characteristics are:

**Purpose**

Reserved for future information about the CTI component to the debugger.

**Configuration**

CTIDEVID1 is in the Debug power domain.

**Attributes**

CTIDEVID1 is a 32-bit register.

**Field descriptions**

The CTIDEVID1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

Accessing the CTIDEVID1

CTIDEVID1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFC4</td>
<td>CTIDEVID1</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIDEVID2, CTI Device ID register 2

The CTIDEVID2 characteristics are:

**Purpose**

Reserved for future information about the CTI component to the debugger.

**Configuration**

CTIDEVID2 is in the Debug power domain.

**Attributes**

CTIDEVID2 is a 32-bit register.

**Field descriptions**

The CTIDEVID2 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |

**Bits [31:0]**

Reserved, RES0.

**Accessing the CTIDEVID2**

**CTIDEVID2 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFC0</td>
<td>CTIDEVID2</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIDEVTYPE, CTI Device Type register

The CTIDEVTYPE characteristics are:

**Purpose**

Indicates to a debugger that this component is part of a PEs cross-trigger interface.

**Configuration**

CTIDEVTYPE is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

**Attributes**

CTIDEVTYPE is a 32-bit register.

**Field descriptions**

The CTIDEVTYPE bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>SUB</td>
<td>MAJOR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SUB, bits [7:4]**

Subtype. Must read as 0x1 to indicate this is a component within a PE.

**MAJOR, bits [3:0]**

Major type. Must read as 0x4 to indicate this is a cross-trigger component.

**Accessing the CTIDEVTYPE**

CTIDEVTYPE can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFCC</td>
<td>CTIDEVTYPE</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIGATE, CTI Channel Gate Enable register

The CTIGATE characteristics are:

**Purpose**

Determines whether events on channels propagate through the CTM to other ECT components, or from the CTM into the CTI.

**Configuration**

CTIGATE is in the Debug power domain.

**Attributes**

CTIGATE is a 32-bit register.

**Field descriptions**

The CTIGATE bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>GATE31</td>
</tr>
<tr>
<td>30</td>
<td>GATE30</td>
</tr>
<tr>
<td>29</td>
<td>GATE29</td>
</tr>
<tr>
<td>28</td>
<td>GATE28</td>
</tr>
<tr>
<td>27</td>
<td>GATE27</td>
</tr>
<tr>
<td>26</td>
<td>GATE26</td>
</tr>
<tr>
<td>25</td>
<td>GATE25</td>
</tr>
<tr>
<td>24</td>
<td>GATE24</td>
</tr>
<tr>
<td>23</td>
<td>GATE23</td>
</tr>
<tr>
<td>22</td>
<td>GATE22</td>
</tr>
<tr>
<td>21</td>
<td>GATE21</td>
</tr>
<tr>
<td>20</td>
<td>GATE20</td>
</tr>
<tr>
<td>19</td>
<td>GATE19</td>
</tr>
<tr>
<td>18</td>
<td>GATE18</td>
</tr>
<tr>
<td>17</td>
<td>GATE17</td>
</tr>
<tr>
<td>16</td>
<td>GATE16</td>
</tr>
<tr>
<td>15</td>
<td>GATE15</td>
</tr>
<tr>
<td>14</td>
<td>GATE14</td>
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<tr>
<td>13</td>
<td>GATE13</td>
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<tr>
<td>12</td>
<td>GATE12</td>
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<tr>
<td>11</td>
<td>GATE11</td>
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<tr>
<td>10</td>
<td>GATE10</td>
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<tr>
<td>9</td>
<td>GATE9</td>
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<tr>
<td>8</td>
<td>GATE8</td>
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<tr>
<td>7</td>
<td>GATE7</td>
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<tr>
<td>6</td>
<td>GATE6</td>
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<tr>
<td>5</td>
<td>GATE5</td>
</tr>
<tr>
<td>4</td>
<td>GATE4</td>
</tr>
<tr>
<td>3</td>
<td>GATE3</td>
</tr>
<tr>
<td>2</td>
<td>GATE2</td>
</tr>
<tr>
<td>1</td>
<td>GATE1</td>
</tr>
<tr>
<td>0</td>
<td>GATE0</td>
</tr>
</tbody>
</table>

GATE<x>, bit [x], for x = 31 to 0

Channel <x> gate enable.

Bits [31:N] are RAZ/WI. N is the number of ECT channels implemented as defined by the CTIDEVID.NUMCHAN field.

<table>
<thead>
<tr>
<th>GATE&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disable output and, if CTIDEVID.INOUT == 0b01, input channel &lt;x&gt; propagation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enable output and, if CTIDEVID.INOUT == 0b01, input channel &lt;x&gt; propagation.</td>
</tr>
</tbody>
</table>

If GATE[x] is set to 0, no new events will be propagated to the ECT, and if the ECT supports multicycle channel events any existing output channel events will be terminated.

On an External debug reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CTIGATE**

CTIGATE can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x140</td>
<td>CTIGATE</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are **RO**.
- When !SoftwareLockStatus() accesses to this register are **RW**.
CTIINEN\(<n>\), CTI Input Trigger to Output Channel Enable registers, \(n = 0 - 31\)

The CTIINEN\(<n>\) characteristics are:

**Purpose**

Enables the signaling of an event on output channels when input trigger event \(n\) is received by the CTI.

**Configuration**

CTIINEN\(<n>\) is in the Debug power domain.

If input trigger \(n\) is not connected, the behavior of CTIINEN\(<n>\) is IMPLEMENTATION DEFINED.

**Attributes**

CTIINEN\(<n>\) is a 32-bit register.

**Field descriptions**

The CTIINEN\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>INEN&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input trigger (&lt;n&gt;) will not generate an event on output channel (&lt;x&gt;).</td>
</tr>
<tr>
<td>0b1</td>
<td>Input trigger (&lt;n&gt;) will generate an event on output channel (&lt;x&gt;).</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CTIINEN\(<n>\)**

CTIINEN\(<n>\) can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x020 + (4 * (n))</td>
<td>CTIINEN(&lt;n&gt;)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are RO.
- When !SoftwareLockStatus() accesses to this register are RW.
CTIINTACK, CTI Output Trigger Acknowledge register

The CTIINTACK characteristics are:

**Purpose**

Can be used to deactivate the output triggers.

**Configuration**

CTIINTACK is in the Debug power domain.

**Attributes**

CTIINTACK is a 32-bit register.

**Field descriptions**

The CTIINTACK bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ACK31</td>
</tr>
<tr>
<td>30</td>
<td>ACK30</td>
</tr>
<tr>
<td>29</td>
<td>ACK29</td>
</tr>
<tr>
<td>28</td>
<td>ACK28</td>
</tr>
<tr>
<td>27</td>
<td>ACK27</td>
</tr>
<tr>
<td>26</td>
<td>ACK26</td>
</tr>
<tr>
<td>25</td>
<td>ACK25</td>
</tr>
<tr>
<td>24</td>
<td>ACK24</td>
</tr>
<tr>
<td>23</td>
<td>ACK23</td>
</tr>
<tr>
<td>22</td>
<td>ACK22</td>
</tr>
<tr>
<td>21</td>
<td>ACK21</td>
</tr>
<tr>
<td>20</td>
<td>ACK20</td>
</tr>
<tr>
<td>19</td>
<td>ACK19</td>
</tr>
<tr>
<td>18</td>
<td>ACK18</td>
</tr>
<tr>
<td>17</td>
<td>ACK17</td>
</tr>
<tr>
<td>16</td>
<td>ACK16</td>
</tr>
<tr>
<td>15</td>
<td>ACK15</td>
</tr>
<tr>
<td>14</td>
<td>ACK14</td>
</tr>
<tr>
<td>13</td>
<td>ACK13</td>
</tr>
<tr>
<td>12</td>
<td>ACK12</td>
</tr>
<tr>
<td>11</td>
<td>ACK11</td>
</tr>
<tr>
<td>10</td>
<td>ACK10</td>
</tr>
<tr>
<td>9</td>
<td>ACK9</td>
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<tr>
<td>8</td>
<td>ACK8</td>
</tr>
<tr>
<td>7</td>
<td>ACK7</td>
</tr>
<tr>
<td>6</td>
<td>ACK6</td>
</tr>
<tr>
<td>5</td>
<td>ACK5</td>
</tr>
<tr>
<td>4</td>
<td>ACK4</td>
</tr>
<tr>
<td>3</td>
<td>ACK3</td>
</tr>
<tr>
<td>2</td>
<td>ACK2</td>
</tr>
<tr>
<td>1</td>
<td>ACK1</td>
</tr>
<tr>
<td>0</td>
<td>ACK0</td>
</tr>
</tbody>
</table>

**ACK<n>, bit [n], for n = 31 to 0**

Acknowledge for output trigger <n>.

Bits [31:N] are RAZ/WI. N is the number of CTI triggers implemented as defined by the CTIDEVID[NUMTRIG] field.

If any of the following is true, writes to ACK<n> are ignored:

- n >= CTIDEVID[NUMTRIG], the number of implemented triggers.
- Output trigger n is not active.
- The channel mapping function output, as controlled by CTIOUTEN<n>, is still active.

Otherwise, if any of the following are true, it is IMPLEMENTATION DEFINED whether writes to ACK<n> are ignored:

- Output trigger n is not implemented.
- Output trigger n is not connected.
- Output trigger n is self-acknowledging and does not require software acknowledge.

Otherwise, the behavior on writes to ACK<n> is as follows:

<table>
<thead>
<tr>
<th>ACK&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No effect</td>
</tr>
<tr>
<td>0b1</td>
<td>Deactivate the trigger.</td>
</tr>
</tbody>
</table>

**Accessing the CTIINTACK**

A debugger must read CTITRIGOUTSTATUS to confirm that the output trigger has been acknowledged before generating any event that must be ordered after the write to CTIINTACK, such as a write to CTIAPPWUE to activate another trigger.

**CTIINTACK can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x010</td>
<td>CTIINTACK</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When `SoftwareLockStatus()` accesses to this register are `WI`.
- When `!SoftwareLockStatus()` accesses to this register are `WO`.
CTIITCTRL, CTI Integration mode Control register

The CTIITCTRL characteristics are:

**Purpose**

Enables the CTI to switch from its default mode into integration mode, where test software can control directly the inputs and outputs of the PE, for integration testing or topology detection.

**Configuration**

It is IMPLEMENTATION DEFINED whether CTIITCTRL is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is OPTIONAL.

**Attributes**

CTIITCTRL is a 32-bit register.

**Field descriptions**

The CTIITCTRL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RES0 | IME |

**Bits [31:1]**

Reserved, RES0.

**IME, bit [0]**

Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED.

<table>
<thead>
<tr>
<th>IME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Integration mode enabled.</td>
</tr>
</tbody>
</table>

The following resets apply:

- If the register is implemented in the Core power domain:
  - On a Cold reset, this field resets to 0.
  - On an External debug reset, the value of this field is unchanged.
  - On a Warm reset, the value of this field is unchanged.

- If the register is implemented in the External debug power domain:
  - On a Cold reset, the value of this field is unchanged.
  - On an External debug reset, this field resets to 0.
  - On a Warm reset, the value of this field is unchanged.
Accessing the CTIITCTRL

CTIITCTRL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xF00</td>
<td>CTIITCTRL</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register are IMPDEF.
CTILAR, CTI Lock Access Register

The CTILAR characteristics are:

**Purpose**

Allows or disallows access to the CTI registers through a memory-mapped interface.

The optional Software Lock provides a lock to prevent memory-mapped writes to the Cross-Trigger Interface registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the Cross-Trigger Interface registers. It does not, and cannot, prevent all accidental or malicious damage.

**Configuration**

CTILAR is in the Debug power domain.

If FEAT_Debugv8p4 is implemented, the Software Lock is not implemented.

Software uses CTILAR to set or clear the lock, and CTILSR to check the current status of the lock.

**Attributes**

CTILAR is a 32-bit register.

**Field descriptions**

The CTILAR bit assignments are:

---

**When the Software Lock is implemented:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
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<th>14</th>
<th>13</th>
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<th>11</th>
<th>10</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>KEY</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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</tr>
</tbody>
</table>

**KEY, bits [31:0]**

Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component’s registers through a memory-mapped interface.

Writing any other value to this register locks the lock, disabling write accesses to this component’s registers through a memory-mapped interface.

---

**Otherwise:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Otherwise

**Bits [31:0]**

Reserved, RES0.
Accessing the CTILAR

CTILAR can be accessed through a memory-mapped access to the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFB0</td>
<td>CTILAR</td>
</tr>
</tbody>
</table>

Accesses on this interface are WO.
CTILSR, CTI Lock Status Register

The CTILSR characteristics are:

**Purpose**

Indicates the current status of the Software Lock for CTI registers.

The optional Software Lock provides a lock to prevent memory-mapped writes to the Cross-Trigger Interface registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the Cross-Trigger Interface registers. It does not, and cannot, prevent all accidental or malicious damage.

**Configuration**

CTILSR is in the Debug power domain.

If FEAT_Debugv8p4 is implemented, the Software Lock is not implemented.

Software uses CTILAR to set or clear the lock, and CTILSR to check the current status of the lock.

**Attributes**

CTILSR is a 32-bit register.

**Field descriptions**

The CTILSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>nTT</td>
</tr>
<tr>
<td>29</td>
<td>SLK</td>
</tr>
<tr>
<td>28</td>
<td>SLI</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**nTT, bit [2]**

Not thirty-two bit access required. RAZ.

**SLK, bit [1]**

*When the Software Lock is implemented:*

Software Lock status for this component. For an access to LSR that is not a memory-mapped access, or when the Software Lock is not implemented, this field is RES0.

For memory-mapped accesses when the Software Lock is implemented, possible values of this field are:

<table>
<thead>
<tr>
<th>SLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Lock clear. Writes are permitted to this component’s registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Lock set. Writes to this component's registers are ignored, and reads have no side effects.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 1.
Otherwise:
Reserved, RAZ.

SLI, bit [0]

Software Lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are:

<table>
<thead>
<tr>
<th>SLI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Software Lock not implemented or not memory-mapped access.</td>
</tr>
<tr>
<td>0b1</td>
<td>Software Lock implemented and memory-mapped access.</td>
</tr>
</tbody>
</table>

Accessing the CTILSR

CTILSR can be accessed through a memory-mapped access to the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFB4</td>
<td>CTILSR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTIOUTEN<\n>, CTI Input Channel to Output Trigger Enable registers, n = 0 - 31

The CTIOUTEN<\n> characteristics are:

**Purpose**

Defines which input channels generate output trigger n.

**Configuration**

CTIOUTEN<\n> is in the Debug power domain.

If output trigger n is not connected, the behavior of CTIOUTEN<\n> is IMPLEMENTATION DEFINED.

**Attributes**

CTIOUTEN<\n> is a 32-bit register.

**Field descriptions**

The CTIOUTEN<\n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| OUTEN31 | OUTEN30 | OUTEN29 | OUTEN28 | OUTEN27 | OUTEN26 | OUTEN25 | OUTEN24 | OUTEN23 | OUTEN22 | OUTEN21 | OUTEN20 | OUTEN19 | OUTEN18 | OUTEN17 | OUTEN16 | OUTEN15 | OUTEN14 | OUTEN13 | OUTEN12 | OUTEN11 | OUTEN10 | OUTEN9 | OUTEN8 | OUTEN7 | OUTEN6 | OUTEN5 | OUTEN4 | OUTEN3 | OUTEN2 | OUTEN1 | OUTEN0 |

OUTEN<\x>, bit \([x]\), for \(x = 31\) to \(0\)

Input channel <\x\> to output trigger <\n\> enable.

Bits [31:N] are RAZ/WI. N is the number of ECT channels implemented as defined by the CTIDEVID_NUMCHAN field.

Possible values of this bit are:

<table>
<thead>
<tr>
<th>OUTEN&lt;\x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>An event on input channel &lt;\x&gt; will not cause output trigger &lt;\n&gt; to be asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>An event on input channel &lt;\x&gt; will cause output trigger &lt;\n&gt; to be asserted.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to an architecturally UNKNOWN value.

**Accessing the CTIOUTEN<\n>**

CTIOUTEN<\n> can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x0A0 + (4 * (n))</td>
<td>CTIOUTEN&lt;\n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When SoftwareLockStatus() accesses to this register are RO.
- When !SoftwareLockStatus() accesses to this register are RW.
CTIOUTEN<n>, CTI Input Channel to Output Trigger Enable registers, n = 0 · 31

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CTIPIDR0, CTI Peripheral Identification Register 0

The CTIPIDR0 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

CTIPIDR0 is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

This register is required for CoreSight compliance.

**Attributes**

CTIPIDR0 is a 32-bit register.

**Field descriptions**

The CTIPIDR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **RES0** |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PART_0 |

**Bits [31:8]**

Reserved, RES0.

**PART_0, bits [7:0]**

Part number, least significant byte.

**Accessing the CTIPIDR0**

CTIPIDR0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFE0</td>
<td>CTIPIDR0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIPIDR1, CTI Peripheral Identification Register 1

The CTIPIDR1 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

CTIPIDR1 is in the Debug power domain.

Implementation of this register is **OPTIONAL**.

This register is required for CoreSight compliance.

**Attributes**

CTIPIDR1 is a 32-bit register.

**Field descriptions**

The CTIPIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>Designer, least significant nibble of JEP106 ID code. For Arm Limited, this field is (0b1011).</td>
</tr>
<tr>
<td>29</td>
<td>Part number, most significant nibble.</td>
</tr>
</tbody>
</table>

**Accessing the CTIPIDR1**

CTIPIDR1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFE4</td>
<td>CTIPIDR1</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The CTIPIDR2 characteristics are:

**Purpose**

Provides information to identify a CTI component.
For more information, see 'About the Peripheral identification scheme'.

**Configuration**

CTIPIDR2 is in the Debug power domain.
Implementation of this register is **OPTIONAL**.
This register is required for CoreSight compliance.

**Attributes**

CTIPIDR2 is a 32-bit register.

**Field descriptions**

The CTIPIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>REVISION</td>
</tr>
<tr>
<td>29</td>
<td>JEDEC</td>
</tr>
<tr>
<td>28</td>
<td>DES_1</td>
</tr>
<tr>
<td>27</td>
<td>Bit 0</td>
</tr>
<tr>
<td>26</td>
<td>Bit 1</td>
</tr>
<tr>
<td>25</td>
<td>Bit 2</td>
</tr>
<tr>
<td>24</td>
<td>Bit 3</td>
</tr>
<tr>
<td>23</td>
<td>Bit 4</td>
</tr>
<tr>
<td>22</td>
<td>Bit 5</td>
</tr>
<tr>
<td>21</td>
<td>Bit 6</td>
</tr>
<tr>
<td>20</td>
<td>Bit 7</td>
</tr>
<tr>
<td>19</td>
<td>Bit 8</td>
</tr>
<tr>
<td>18</td>
<td>Bit 9</td>
</tr>
<tr>
<td>17</td>
<td>Bit 10</td>
</tr>
<tr>
<td>16</td>
<td>Bit 11</td>
</tr>
<tr>
<td>15</td>
<td>Bit 12</td>
</tr>
<tr>
<td>14</td>
<td>Bit 13</td>
</tr>
<tr>
<td>13</td>
<td>Bit 14</td>
</tr>
<tr>
<td>12</td>
<td>Bit 15</td>
</tr>
<tr>
<td>11</td>
<td>Bit 16</td>
</tr>
<tr>
<td>10</td>
<td>Bit 17</td>
</tr>
<tr>
<td>9</td>
<td>Bit 18</td>
</tr>
<tr>
<td>8</td>
<td>Bit 19</td>
</tr>
<tr>
<td>7</td>
<td>Bit 20</td>
</tr>
<tr>
<td>6</td>
<td>Bit 21</td>
</tr>
<tr>
<td>5</td>
<td>Bit 22</td>
</tr>
<tr>
<td>4</td>
<td>Bit 23</td>
</tr>
<tr>
<td>3</td>
<td>Bit 24</td>
</tr>
<tr>
<td>2</td>
<td>Bit 25</td>
</tr>
<tr>
<td>1</td>
<td>Bit 26</td>
</tr>
<tr>
<td>0</td>
<td>Bit 27</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**REVISION, bits [7:4]**

Part major revision. Parts can also use this field to extend Part number to 16-bits.

**JEDEC, bit [3]**

RAO. Indicates a JEP106 identity code is used.

**DES_1, bits [2:0]**

Designer, most significant bits of JEP106 ID code. For Arm Limited, this field is 0b011.

**Accessing the CTIPIDR2**

CTIPIDR2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFE8</td>
<td>CTIPIDR2</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
CTIPIDR3, CTI Peripheral Identification Register 3

The CTIPIDR3 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

CTIPIDR3 is in the Debug power domain.

Implementation of this register is OPTIONAL.

This register is required for CoreSight compliance.

**Attributes**

CTIPIDR3 is a 32-bit register.

**Field descriptions**

The CTIPIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>7:4</td>
<td>REVAND, Part minor revision</td>
</tr>
<tr>
<td>3:0</td>
<td>CMOD, Customer modified</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**REVAND, bits [7:4]**

Part minor revision. Parts using CTIPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.

**CMOD, bits [3:0]**

Customer modified. Indicates someone other than the Designer has modified the component.

**Accessing the CTIPIDR3**

CTIPIDR3 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFEC</td>
<td>CTIPIDR3</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTIPIDR4, CTI Peripheral Identification Register 4

The CTIPIDR4 characteristics are:

**Purpose**

Provides information to identify a CTI component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

CTIPIDR4 is in the Debug power domain.

Implementation of this register is OPTIONAL.

This register is required for CoreSight compliance.

**Attributes**

CTIPIDR4 is a 32-bit register.

**Field descriptions**

The CTIPIDR4 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RES0 | SIZE | DES_2 |

**Bits [31:8]**

Reserved, RES0.

**SIZE, bits [7:4]**

Size of the component. RAZ. \( \log_2 \) of the number of 4KB pages from the start of the component to the end of the component ID registers.

**DES_2, bits [3:0]**

Designer, JEP106 continuation code, least significant nibble. For Arm Limited, this field is 0b0100.

**Accessing the CTIPIDR4**

CTIPIDR4 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0xFD0</td>
<td>CTIPIDR4</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The CTITRIGINSTATUS characteristics are:

**Purpose**

Provides the status of the trigger inputs.

**Configuration**

CTITRIGINSTATUS is in the Debug power domain.

**Attributes**

CTITRIGINSTATUS is a 32-bit register.

**Field descriptions**

The CTITRIGINSTATUS bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TRIN31 | TRIN30 | TRIN29 | TRIN28 | TRIN27 | TRIN26 | TRIN25 | TRIN24 | TRIN23 | TRIN22 | TRIN21 | TRIN20 | TRIN19 | TRIN18 | TRIN17 | TRIN16 | TRIN15 | TRIN14 | TRIN13 | TRIN12 | TRIN11 | TRIN10 | TRIN9 | TRIN8 | TRIN7 | TRIN6 | TRIN5 | TRIN4 | TRIN3 | TRIN2 | TRIN1 | TRIN0 |

TRIN<n>, bit [n], for n = 31 to 0

Trigger input <n> status.

Bits [31:N] are RAZ. N is the number of CTI triggers implemented as defined by the CTIDEVID.NUMTRIG field.

<table>
<thead>
<tr>
<th>TRIN&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Input trigger n is inactive.</td>
</tr>
<tr>
<td>0b1</td>
<td>Input trigger n is active.</td>
</tr>
</tbody>
</table>

Not implemented and not-connected input triggers are always inactive.

It is IMPLEMENTATION DEFINED whether an input trigger that does not support multicycle events can be observed as active.

**Accessing the CTITRIGINSTATUS**

CTITRIGINSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x130</td>
<td>CTITRIGINSTATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
CTITRIGOUTSTATUS, CTI Trigger Out Status register

The CTITRIGOUTSTATUS characteristics are:

**Purpose**

Provides the raw status of the trigger outputs, after processing by any IMPLEMENTATION DEFINED trigger interface logic. For output triggers that are self-acknowledging, this is only meaningful if the CTI implements multicycle channel events.

**Configuration**

CTITRIGOUTSTATUS is in the Debug power domain.

**Attributes**

CTITRIGOUTSTATUS is a 32-bit register.

**Field descriptions**

The CTITRIGOUTSTATUS bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TROUT31</td>
<td>TROUT30</td>
<td>TROUT29</td>
<td>TROUT28</td>
<td>TROUT27</td>
<td>TROUT26</td>
<td>TROUT25</td>
<td>TROUT24</td>
<td>TROUT23</td>
<td>TROUT22</td>
<td>TROUT21</td>
<td>TROUT20</td>
<td>TROUT19</td>
<td>TROUT18</td>
<td>TROUT17</td>
<td>TROUT16</td>
<td>TROUT15</td>
<td>TROUT14</td>
<td>TROUT13</td>
<td>TROUT12</td>
<td>TROUT11</td>
<td>TROUT10</td>
<td>TROUT9</td>
<td>TROUT8</td>
<td>TROUT7</td>
<td>TROUT6</td>
<td>TROUT5</td>
<td>TROUT4</td>
<td>TROUT3</td>
<td>TROUT2</td>
<td>TROUT1</td>
<td>TROUT0</td>
</tr>
</tbody>
</table>

TROUT<><n>, bit [n], for n = 31 to 0

Trigger output <n> status.

Bits [31:N] are RAZ. N is the value in CTIDEVID.NUMTRIG.

If n < N, and output trigger <n> is implemented and connected, and either the trigger is not self-acknowledging or the CTI implements multicycle channel events, then permitted values for TROUT<n> are:

<table>
<thead>
<tr>
<th>TROUT&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Output trigger n is inactive.</td>
</tr>
<tr>
<td>0b1</td>
<td>Output trigger n is active.</td>
</tr>
</tbody>
</table>

Otherwise when n < N it is IMPLEMENTATION DEFINED whether TROUT<n> behaves as described here or is RAZ.

**Accessing the CTITRIGOUTSTATUS**

CTITRIGOUTSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTI</td>
<td>0x134</td>
<td>CTITRIGOUTSTATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
DBGAUTHSTATUS_EL1, Debug Authentication Status register

The DBGAUTHSTATUS_EL1 characteristics are:

**Purpose**

Provides information about the state of the IMPLEMENTATION DEFINED authentication interface for debug.

**Configuration**

External register DBGAUTHSTATUS_EL1 bits [31:0] are architecturally mapped to AArch64 System register DBGAUTHSTATUS_EL1[31:0].

External register DBGAUTHSTATUS_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGAUTHSTATUS[31:0].

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

DBGAUTHSTATUS_EL1 is a 32-bit register.

**Field descriptions**

The DBGAUTHSTATUS_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**SNID, bits [7:6]**

When FEAT_Debugv8p4 is implemented:

Secure non-invasive debug.

This field has the same value as DBGAUTHSTATUS_EL1.SID.

Otherwise:

Secure non-invasive debug.

<table>
<thead>
<tr>
<th>SNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.
**SID, bits [5:4]**

Secure invasive debug.

<table>
<thead>
<tr>
<th>SID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalSecureInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalSecureInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSNID, bits [3:2]**

When FEAT_Debugv8p4 is implemented:

Non-secure non-invasive debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

If the Effective value of SCR_EL3.NS is 1, or if EL3 is implemented and EL2 is not implemented, this field reads as 0b11.

All other values are reserved.

Otherwise:

Non-secure non-invasive debug.

<table>
<thead>
<tr>
<th>NSNID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalNoninvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalNoninvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSID, bits [1:0]**

Non-secure invasive debug.

<table>
<thead>
<tr>
<th>NSID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented. EL3 is not implemented and the Effective value of SCR_EL3.NS is 0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Implemented and disabled. ExternalInvasiveDebugEnabled() == FALSE.</td>
</tr>
<tr>
<td>0b11</td>
<td>Implemented and enabled. ExternalInvasiveDebugEnabled() == TRUE.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Accessing the DBGAUTHSTATUS_EL1**

DBGAUTHSTATUS_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>
This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
The DBGCR<n>_EL1 characteristics are:

**Purpose**

Holds control information for a breakpoint. Forms breakpoint n together with value register DBGVR<n>_EL1.

**Configuration**

External register DBGCR<n>_EL1 bits [31:0] are architecturally mapped to AArch64 System register DBGCR<n>_EL1[31:0].

External register DBGCR<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGCR<n>[31:0].

DBGCR<n>_EL1 is in the Core power domain.

If breakpoint n is not implemented then accesses to this register are:

- RES0 when IsCorePowered() && !DoubleLockStatus() && !OSLockStatus() && AllowExternalDebugAccess().
- A CONSTRAINED UNPREDICTABLE choice of RES0 or ERROR otherwise.

**Attributes**

DBGCR<n>_EL1 is a 32-bit register.

**Field descriptions**

The DBGCR<n>_EL1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | BT | LBN | SSC | HMC | RES0 | BAS | RES0 | PMC | E |

When the E field is zero, all the other fields in the register are ignored.

**Bits [31:24]**

Reserved, RES0.

**BT, bits [23:20]**

Breakpoint Type. Possible values are:
### DBGBCR<n>_EL1, Debug Breakpoint Control Registers, n = 0 - 15

<table>
<thead>
<tr>
<th>BT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Unlinked instruction address match. DBGVR&lt;n&gt;_EL1 is the address of an instruction.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As 0b0000 but linked to a Context matching breakpoint.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Unlinked Context ID match. When FEAT_VHE is implemented, EL2 is using AArch64, and the Effective value of HCR_EL2.E2H is 1, if either the PE is executing at EL0 with HCR_EL2.TGE set to 1 or the PE is executing at EL2, then DBGVR&lt;n&gt;_EL1.ContextID must match the CONTEXTIDR_EL2 value. Otherwise, DBGVR&lt;n&gt;_EL1.ContextID must match the CONTEXTIDR_EL1 value.</td>
</tr>
<tr>
<td>0b0011</td>
<td>As 0b0010, with linking enabled.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Unlinked instruction address mismatch. DBGBVR&lt;n&gt;_EL1 is the address of an instruction to be stepped.</td>
</tr>
<tr>
<td>0b0101</td>
<td>As 0b0100, with linking enabled.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Unlinked CONTEXTIDR_EL1 match. DBGVR&lt;n&gt;_EL1.ContextID is a Context ID compared against CONTEXTIDR_EL1.</td>
</tr>
<tr>
<td>0b0111</td>
<td>As 0b0110, with linking enabled.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Unlinked VMID match. DBGVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b1001</td>
<td>As 0b1000, with linking enabled.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Unlinked VMID and Context ID match. DBGVR&lt;n&gt;_EL1.ContextID is a Context ID compared against CONTEXTIDR_EL1, and DBGVR&lt;n&gt;_EL1.VMID is a VMID compared against VTTBR_EL2.VMID.</td>
</tr>
<tr>
<td>0b1011</td>
<td>As 0b1010, with linking enabled.</td>
</tr>
<tr>
<td>0b1100</td>
<td>Unlinked CONTEXTIDR_EL2 match. DBGVR&lt;n&gt;_EL1.ContextID2 is a Context ID compared against CONTEXTIDR_EL2.</td>
</tr>
<tr>
<td>0b1101</td>
<td>As 0b1100, with linking enabled.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Unlinked Full Context ID match. DBGVR&lt;n&gt;_EL1.ContextID is compared against CONTEXTIDR_EL1, and DBGVR&lt;n&gt;_EL1.ContextID2 is compared against CONTEXTIDR_EL2.</td>
</tr>
<tr>
<td>0b1111</td>
<td>As 0b1110, with linking enabled.</td>
</tr>
</tbody>
</table>

Constraints on breakpoint programming mean some values are reserved under certain conditions.

For more information on the operation of the SSC, HMC, and PMC fields, and on the effect of programming this field to a reserved value, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions' and 'Reserved DBGBCR<n>_EL1.BT values'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

#### LBN, bits [19:16]

Linked breakpoint number. For Linked address matching breakpoints, this specifies the index of the Context-matching breakpoint linked to.

For all other breakpoint types this field is ignored and reads of the register return an **UNKNOWN** value.

This field is ignored when the value of DBGBCR<n>_EL1.E is 0.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

#### SSC, bits [15:14]

Security state control. Determines the Security states under which a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the HMC and PMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields. For more information, including the effect of programming the fields to a reserved set of values, see 'Reserved DBGBCR<n>_EL1.{SSC, HMC, PMC} values'.

For more information on the operation of the SSC, HMC, and PMC fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.
HMC, bit [13]

Higher mode control. Determines the debug perspective for deciding when a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and PMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields. For more information see DBGBCR<n>_EL1, SSC description.

For more information on the operation of the SSC, HMC, and PMC fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [12:9]

Reserved, RES0.

BAS, bits [8:5]

When AArch32 is supported at any Exception level:

Byte address select. Defines which half-words an address-matching breakpoint matches, regardless of the instruction set and Execution state.

The permitted values depend on the breakpoint type.

For Address match breakpoints in either AArch32 or AArch64 state, the permitted values are:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Match instruction at</th>
<th>Constraint for debuggers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0011</td>
<td>DBGVR&lt;n&gt;_EL1</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1100</td>
<td>DBGVR&lt;n&gt;_EL1 + 2</td>
<td>Use for T32 instructions</td>
</tr>
<tr>
<td>0b1111</td>
<td>DBGVR&lt;n&gt;_EL1</td>
<td>Use for A64 and A32 instructions</td>
</tr>
</tbody>
</table>

All other values are reserved.

For more information, see 'Using the BAS field in Address Match breakpoints'.

For Address mismatch breakpoints in an AArch32 stage 1 translation regime, the permitted values are:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Match instruction at</th>
<th>Constraint for debuggers</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>-</td>
<td>Use for a match anywhere breakpoint</td>
</tr>
<tr>
<td>0b0011</td>
<td>DBGVR&lt;n&gt;_EL1</td>
<td>Use for stepping T32 instructions</td>
</tr>
<tr>
<td>0b1100</td>
<td>DBGVR&lt;n&gt;_EL1 + 2</td>
<td>Use for stepping T32 instructions</td>
</tr>
<tr>
<td>0b1111</td>
<td>DBGVR&lt;n&gt;_EL1</td>
<td>Use for stepping A64 and A32 instructions</td>
</tr>
</tbody>
</table>

For more information, see 'Using the BAS field in Address Match breakpoints'.

For Context matching breakpoints, this field is RES1 and ignored.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES1.

Bits [4:3]

Reserved, RES0.

PMC, bits [2:1]

Privilege mode control. Determines the Exception level or levels at which a Breakpoint debug event for breakpoint n is generated. This field must be interpreted along with the SSC and HMC fields, and there are constraints on the permitted values of the {HMC, SSC, PMC} fields. For more information see the DBGBCR<n>_EL1, SSC description.
For more information on the operation of the SSC, HMC, and PMC fields, see 'Execution conditions for which a breakpoint generates Breakpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**E**, bit [0]

Enable breakpoint **DBGBVR<n>_EL1**. Possible values are:

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Breakpoint disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Breakpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the DBGBCR<n> _EL1**

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalDebugAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

**DBGBCR<n>_EL1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x408 + (16 * n)</td>
<td>DBGBCR&lt;n&gt; _EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
The DBGBVR\textsubscript{n} EL1 characteristics are:

**Purpose**

Holds a virtual address, or a VMID and/or a context ID, for use in breakpoint matching. Forms breakpoint \textit{n} together with control register DBGBCR\textsubscript{n} EL1.

**Configuration**

External register DBGBVR\textsubscript{n} EL1 bits [63:0] are architecturally mapped to AArch64 System register DBGBVR\textsubscript{n} EL1[63:0].

External register DBGBVR\textsubscript{n} EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGBVR\textsubscript{n} [31:0].

External register DBGBVR\textsubscript{n} EL1 bits [63:32] are architecturally mapped to AArch32 System register DBGXVR\textsubscript{n} [31:0].

DBGBVR\textsubscript{n} EL1 is in the Core power domain.

How this register is interpreted depends on the value of DBGBCR\textsubscript{n} EL1 BT.

- When DBGBCR\textsubscript{n} EL1 BT is 0b000x, this register holds a virtual address.
- When DBGBCR\textsubscript{n} EL1 BT is 0b001x, 0b011x, or 0b110x, this register holds a Context ID.
- When DBGBCR\textsubscript{n} EL1 BT is 0b100x, this register holds a VMID.
- When DBGBCR\textsubscript{n} EL1 BT is 0b101x, this register holds a VMID and a Context ID.
- When DBGBCR\textsubscript{n} EL1 BT is 0b111x, this register holds two Context ID values.

For other values of DBGBCR\textsubscript{n} EL1 BT, this register is RES0.

If breakpoint \textit{n} is not implemented then accesses to this register are:

- RES0 when IsCorePowered() && !DoubleLockStatus() && !OSLockStatus() && AllowExternalDebugAccess().
- A CONSTRAINED UNPREDICTABLE choice of RES0 or ERROR otherwise.

**Attributes**

DBGBVR\textsubscript{n} EL1 is a 64-bit register.

**Field descriptions**

The DBGBVR\textsubscript{n} EL1 bit assignments are:

**When DBGBCR\textsubscript{n} EL1.BT == 0b000x:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-62</td>
<td>RES[14:4]</td>
</tr>
<tr>
<td>58-57</td>
<td>Bits[52:49]</td>
</tr>
<tr>
<td>48-47</td>
<td>VA[48:2]</td>
</tr>
<tr>
<td>31-0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**RESS[14:4], bits [63:53]:**

Reserved, Sign extended. Software must treat this field as RES0 if the most significant bit of VA is 0 or RES0, and as RES1 if the most significant bit of VA is 1.

Hardware always ignores the value of these bits and it is IMPLEMENTATION DEFINED whether:
• The bits are hardwired to a copy of the most significant bit of VA, meaning writes to these bits are ignored, and reads to the bits always return the hardwired value.
• The value in those bits can be written, and reads will return the last value written. The value held in those bits is ignored by hardware.

VA[52:49], bits [52:49]

When FEAT_LVA is implemented:


On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:


VA[48:2], bits [48:2]

If the address is being matched in an AArch64 stage 1 translation regime:

- This field contains bits[48:2] of the address for comparison.
- When FEAT_LVA is implemented, VA[52:49] forms the upper part of the address value. Otherwise, VA[52:49] are RESS.

If the address is being matched in an AArch32 stage 1 translation regime, the first 20 bits of this field are RES0, and the rest of the field contains bits[31:2] of the address for comparison.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [1:0]

Reserved, RES0.

When DBGBCR<n>_EL1.BT == 0b001x:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ContextID |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

Bits [63:32]

Reserved, RES0.

ContextID, bits [31:0]

Context ID value for comparison.

The value is compared against CONTEXTIDR_EL2 when (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented), EL2 is using AArch64, HCR_EL2.E2H is 1, and either:

- The PE is executing at EL2.
- HCR_EL2.TGE is 1, the PE is executing at EL0, and EL2 is enabled in the current Security state.

Otherwise, the value is compared against the following:

- CONTEXTIDR when the PE is executing at AArch32.
- CONTEXTIDR_EL1 when the PE is executing at AArch64.

On a Cold reset, this field resets to an architecturally UNKNOWN value.
When DBGBCR\(_{n}\)\_EL1.BT == 0b011x, EL2 is implemented and (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented):

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>RESERVED, RES0</th>
</tr>
</thead>
</table>

**ContextID, bits [31:0]**

Context ID value for comparison against CONTEXTIDR_EL1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR\(_{n}\)\_EL1.BT == 0b100x and EL2 is implemented:

<table>
<thead>
<tr>
<th>Bits [63:48]</th>
<th>RESERVED, RES0</th>
</tr>
</thead>
</table>

**VMID[15:8], bits [47:40]**

When FEAT_VHE is implemented and VTCR_EL2.VS == 1:

Extension to VMID[7:0]. See DBGBVR\(_{n}\)\_EL1.VMID[7:0] for more details.

If EL2 is using AArch32, this field is RES0.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**VMID[7:0], bits [39:32]**

VMID value for comparison.

The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [31:0]**

Reserved, RES0.
When DBGBCR<n>_EL1.BT == 0b101x and EL2 is implemented:

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
</tr>
<tr>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
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<td>43</td>
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<td>41</td>
<td>40</td>
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<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
</tr>
<tr>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
</tr>
<tr>
<td>RES0</td>
<td>VMID[15:8]</td>
<td>VMID[7:0]</td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

VMID[15:8], bits [47:40]

When FEAT_VMID16 is implemented and VTCR_EL2.VS == 1:

Extension to VMID[7:0]. See DBGVR<n>_EL1.VMID[7:0] for more details.

If EL2 is using AArch32, or if the implementation has an 8-bit VMID, this field is RES0.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

VMID[7:0], bits [39:32]

VMID value for comparison.

The VMID is 8 bits when any of the following are true:

- EL2 is using AArch32.
- VTCR_EL2.VS is 0.
- FEAT_VMID16 is not implemented.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

ContextID, bits [31:0]

Context ID value for comparison.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When DBGBCR<n>_EL1.BT == 0b110x, EL2 is implemented and (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented):

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
</tr>
<tr>
<td>59</td>
<td>58</td>
<td>57</td>
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<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
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<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
</tr>
<tr>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
</tr>
<tr>
<td>ContextID2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

ContextID2, bits [63:32]

Context ID value for comparison.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [31:0]

Reserved, RES0.
When DBGBCR<n>_EL1.BT == 0b111x, EL2 is implemented and (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented):

<table>
<thead>
<tr>
<th>ContextID2</th>
<th>ContextID</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td></td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
<td></td>
</tr>
</tbody>
</table>

ContextID2, bits [63:32]

Context ID value for comparison against CONTEXTIDR_EL2.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

ContextID, bits [31:0]

Context ID value for comparison against CONTEXTIDR_EL1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Accessing the DBGBVR<n>_EL1

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalDebugAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

DBGBVR<n>_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x400 + (16 * n)</td>
<td>DBGBVR&lt;n&gt;_EL1</td>
<td>63:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
The DBGCLAIMCLR_EL1 characteristics are:

**Purpose**

Used by software to read the values of the CLAIM tag bits, and to clear CLAIM tag bits to 0.

The architecture does not define any functionality for the CLAIM tag bits.

**Note**

CLAIM tags are typically used for communication between the debugger and target software.

Used in conjunction with the DBGCLAIMSET_EL1 register.

**Configuration**

External register DBGCLAIMCLR_EL1 bits [31:0] are architecturally mapped to AArch64 System register DBGCLAIMCLR_EL1[31:0].

External register DBGCLAIMCLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGCLAIMCLR[31:0].

DBGCLAIMCLR_EL1 is in the Core power domain.

An implementation must include eight CLAIM tag bits.

**Attributes**

DBGCLAIMCLR_EL1 is a 32-bit register.

**Field descriptions**

The DBGCLAIMCLR_EL1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| RAZ/SBZ | CLAIM |

**Bits [31:8]**

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.

**CLAIM, bits [7:0]**

Read or clear CLAIM tag bits. Reading this field returns the current value of the CLAIM tag bits.

Writing a 1 to one of these bits clears the corresponding CLAIM tag bit to 0. This is an indirect write to the CLAIM tag bits. A single write operation can clear multiple CLAIM tag bits to 0.

Writing 0 to one of these bits has no effect.

On a Cold reset, this field resets to 0.
Accessing the DBGCLAIMCLR_EL1

DBGCLAIMCLR_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFA4</td>
<td>DBGCLAIMCLR_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
DBGCLAIMSET_EL1, Debug CLAIM Tag Set register

The DBGCLAIMSET_EL1 characteristics are:

Purpose

Used by software to set the CLAIM tag bits to 1.

The architecture does not define any functionality for the CLAIM tag bits.

Note

CLAIM tags are typically used for communication between the debugger and target software.

Used in conjunction with the DBGCLAIMCLR_EL1 register.

Configuration

External register DBGCLAIMSET_EL1 bits [31:0] are architecturally mapped to AArch64 System register DBGCLAIMSET_EL1[31:0].

External register DBGCLAIMSET_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGCLAIMSET[31:0].

DBGCLAIMSET_EL1 is in the Core power domain.

An implementation must include eight CLAIM tag bits.

Attributes

DBGCLAIMSET_EL1 is a 32-bit register.

Field descriptions

The DBGCLAIMSET_EL1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RAZ/SBZ |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CLAIM |

Bits [31:8]

Reserved, RAZ/SBZ. Software can rely on these bits reading as zero, and must use a should-be-zero policy on writes. Implementations must ignore writes.

CLAIM, bits [7:0]

Set CLAIM tag bits.

This field is RAO.

Writing a 1 to one of these bits sets the corresponding CLAIM tag bit to 1. This is an indirect write to the CLAIM tag bits. A single write operation can set multiple CLAIM tag bits to 1.

Writing 0 to one of these bits has no effect.
Accessing the DBGCLAIMSET_EL1

DBGCLAIMSET_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFA0</td>
<td>DBGCLAIMSET_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
DBGDTRRX_EL0, Debug Data Transfer Register, Receive

The DBGDTRRX_EL0 characteristics are:

**Purpose**

Transfers data from an external debugger to the PE. For example, it is used by a debugger transferring commands and data to a debug target. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communications Channel.

**Configuration**

External register DBGDTRRX_EL0 bits [31:0] are architecturally mapped to AArch64 System register DBGDTRRX_EL0[31:0].

External register DBGDTRRX_EL0 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRRXint[31:0].

DBGDTRRX_EL0 is in the Core power domain.

**Attributes**

DBGDTRRX_EL0 is a 32-bit register.

**Field descriptions**

The DBGDTRRX_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>Update DTRRX</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Update DTRRX.

Writes to this register:

- If RXfull is set to 1, set DTRRX to UNKNOWN.
- If RXfull is set to 0, update the value in DTRRX.

After the write, RXfull is set to 1.

Reads of this register:

- If RXfull is set to 1, return the last value written to DTRRX.
- If RXfull is set to 0, return an UNKNOWN value.

After the read, RXfull remains unchanged.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.
Accessing the DBGDTRRX_EL0

If EDSCR.ITE == 0 when the PE exits Debug state on receiving a Restart request trigger event, the behavior of any operation issued by a DTR access in memory access mode that has not completed execution is CONSTRAINED UNPREDICTABLE, and must do one of the following:

- It must complete execution in Debug state before the PE executes the restart sequence.
- It must complete execution in Non-debug state before the PE executes the restart sequence.
- It must be abandoned. This means that the instruction does not execute. Any registers or memory accessed by the instruction are left in an UNKNOWN state.

DBGDTRRX_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x080</td>
<td>DBGDTRRX_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
DBGDTRTX_EL0, Debug Data Transfer Register, Transmit

The DBGDTRTX_EL0 characteristics are:

**Purpose**

Transfers data from the PE to an external debugger. For example, it is used by a debug target to transfer data to the debugger. See DBGDTR_EL0 for additional architectural mappings. It is a component of the Debug Communication Channel.

**Configuration**

External register DBGDTRTX_EL0 bits [31:0] are architecturally mapped to AArch64 System register DBGDTRTX_EL0[31:0].

External register DBGDTRTX_EL0 bits [31:0] are architecturally mapped to AArch32 System register DBGDTRTXint[31:0].

DBGDTRTX_EL0 is in the Core power domain.

**Attributes**

DBGDTRTX_EL0 is a 32-bit register.

**Field descriptions**

The DBGDTRTX_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Return DTRTX</td>
</tr>
</tbody>
</table>

**Bits [31:0]**

Return DTRTX.

Reads of this register:

- If TXfull is set to 1, return the last value written to DTRTX.
- If TXfull is set to 0, return an UNKNOWN value.

After the read, TXfull is cleared to 0.

Writes to this register:

- If TXfull is set to 1, set DTRTX to UNKNOWN.
- If TXfull is set to 0, update the value in DTRTX.

After the write, TXfull remains unchanged.

For the full behavior of the Debug Communications Channel, see 'The Debug Communication Channel and Instruction Transfer Register'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.
**Accessing the DBGDTRTX_EL0**

If `EDSCR.ITE == 0` when the PE exits Debug state on receiving a Restart request trigger event, the behavior of any operation issued by a DTR access in memory access mode that has not completed execution is **CONSTRAINED UNPREDICTABLE**, and must do one of the following:

- It must complete execution in Debug state before the PE executes the restart sequence.
- It must complete execution in Non-debug state before the PE executes the restart sequence.
- It must be abandoned. This means that the instruction does not execute. Any registers or memory accessed by the instruction are left in an **UNKNOWN** state.

**DBGDTRTX_EL0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x08C</td>
<td>DBGDTRTX_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `IsCorePowered(), !DoubleLockStatus(), !OSLockStatus()` and `SoftwareLockStatus()` accesses to this register are **RO**.
- When `IsCorePowered(), !DoubleLockStatus(), !OSLockStatus()` and `!SoftwareLockStatus()` accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
DBGWCR<n>_EL1, Debug Watchpoint Control Registers, n = 0 - 15

The DBGWCR<n>_EL1 characteristics are:

**Purpose**

Holds control information for a watchpoint. Forms watchpoint n together with value register DBGWVR<n>_EL1.

**Configuration**

External register DBGWCR<n>_EL1 bits [31:0] are architecturally mapped to AArch64 System register DBGWCR<n>_EL1[31:0].

External register DBGWCR<n>_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGWCR<n>[31:0].

DBGWCR<n>_EL1 is in the Core power domain.

If watchpoint n is not implemented then accesses to this register are:

- When IsCorePowered() && !DoubleLockStatus() && !IOSLockStatus() && AllowExternalDebugAccess(), RES0.
- Otherwise, a CONSTRAINED UNPREDICTABLE choice of RES0 or ERROR.

**Attributes**

DBGWCR<n>_EL1 is a 32-bit register.

**Field descriptions**

The DBGWCR<n>_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>MASK</td>
</tr>
<tr>
<td>29</td>
<td>RES0</td>
</tr>
<tr>
<td>28</td>
<td>WT</td>
</tr>
<tr>
<td>27</td>
<td>LBN</td>
</tr>
<tr>
<td>26</td>
<td>SSC</td>
</tr>
<tr>
<td>25</td>
<td>HMC</td>
</tr>
<tr>
<td>24</td>
<td>BAS</td>
</tr>
<tr>
<td>23</td>
<td>LSC</td>
</tr>
<tr>
<td>22</td>
<td>PAC</td>
</tr>
<tr>
<td>21</td>
<td>E</td>
</tr>
</tbody>
</table>

When the E field is zero, all the other fields in the register are ignored.

**Bits [31:29]**

Reserved, RES0.

**MASK, bits [28:24]**

Address mask. Only objects up to 2GB can be watched using a single mask.

<table>
<thead>
<tr>
<th>MASK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000</td>
<td>No mask.</td>
</tr>
<tr>
<td>0b00001</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b00010</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

If programmed with a reserved value, a watchpoint must behave as if either:

- MASK has been programmed with a defined value, which might be 0 (no mask), other than for a direct read of DBGWCR<n>_EL1.
- The watchpoint is disabled.

Software must not rely on this property because the behavior of reserved values might change in a future revision of the architecture.
Other values mask the corresponding number of address bits, from 0b00011 masking 3 address bits (0x00000007 mask for address) to 0b11111 masking 31 address bits (0x7FFFFFFF mask for address).

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [23:21]**

Reserved, RES0.

**WT, bit [20]**

Watchpoint type. Possible values are:

<table>
<thead>
<tr>
<th>WT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Unlinked data address match.</td>
</tr>
<tr>
<td>0b1</td>
<td>Linked data address match.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**LBN, bits [19:16]**

Linked breakpoint number. For Linked data address watchpoints, this specifies the index of the Context-matching breakpoint linked to.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**SSC, bits [15:14]**

Security state control. Determines the Security states under which a Watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the HMC and PAC fields.

For more information on the operation of the SSC, HMC, and PAC fields, see 'Execution conditions for which a watchpoint generates Watchpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**HMC, bit [13]**

Higher mode control. Determines the debug perspective for deciding when a Watchpoint debug event for watchpoint n is generated. This field must be interpreted along with the SSC and PAC fields.

For more information on the operation of the SSC, HMC, and PAC fields, see 'Execution conditions for which a watchpoint generates Watchpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**BAS, bits [12:5]**

Byte address select. Each bit of this field selects whether a byte from within the word or double-word addressed by DBGWVR<n>_EL1 is being watched.

<table>
<thead>
<tr>
<th>BAS</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxxx1xxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1</td>
</tr>
<tr>
<td>xxxxx1x</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 1</td>
</tr>
<tr>
<td>xxxxx1xx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 2</td>
</tr>
<tr>
<td>xxxx1xxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 3</td>
</tr>
</tbody>
</table>

In cases where DBGWVR<n>_EL1 addresses a double-word:

<table>
<thead>
<tr>
<th>BAS</th>
<th>Description, if DBGWVR&lt;n&gt;_EL1[2] == 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>xxx1xxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 4</td>
</tr>
<tr>
<td>xx1xxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 5</td>
</tr>
<tr>
<td>x1xxxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 6</td>
</tr>
<tr>
<td>1xxxxxxxx</td>
<td>Match byte at DBGWVR&lt;n&gt;_EL1 + 7</td>
</tr>
</tbody>
</table>
If \( \text{DBGWVR}_\text{n}_\text{EL1}[2] == 1 \), only BAS\[3:0\] is used. Arm deprecates setting \( \text{DBGWVR}_\text{n}_\text{EL1}[2] == 1 \).

The valid values for BAS are non-zero binary number all of whose set bits are contiguous. All other values are reserved and must not be used by software. See 'Reserved DBGWCR\<\text{n}>.BAS values'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

### LSC, bits [4:3]

Load/store control. This field enables watchpoint matching on the type of access being made. Possible values of this field are:

<table>
<thead>
<tr>
<th>LSC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>001</td>
<td>Match instructions that load from a watchpointed address.</td>
</tr>
<tr>
<td>010</td>
<td>Match instructions that store to a watchpointed address.</td>
</tr>
<tr>
<td>011</td>
<td>Match instructions that load from or store to a watchpointed address.</td>
</tr>
</tbody>
</table>

All other values are reserved, but must behave as if the watchpoint is disabled. Software must not rely on this property as the behavior of reserved values might change in a future revision of the architecture.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

### PAC, bits [2:1]

Privilege of access control. Determines the Exception level or levels at which a Watchpoint debug event for watchpoint \( n \) is generated. This field must be interpreted along with the SSC and HMC fields.

For more information on the operation of the SSC, HMC, and PAC fields, see 'Execution conditions for which a watchpoint generates Watchpoint exceptions'.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

### E, bit [0]

Enable watchpoint \( n \). Possible values are:

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>Watchpoint disabled.</td>
</tr>
<tr>
<td>01</td>
<td>Watchpoint enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

## Accessing the DBGWCR\<n>_EL1

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalDebugAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

### DBGWCR\<n>_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x808 + (16 * ( n ))</td>
<td>DBGWCR&lt;n&gt;_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
**DBGWVR<n>_EL1, Debug Watchpoint Value Registers, n = 0 - 15**

The **DBGWVR<n>_EL1** characteristics are:

**Purpose**

Holds a data address value for use in watchpoint matching. Forms watchpoint n together with control register **DBGWCR<n>_EL1**.

**Configuration**

External register **DBGWVR<n>_EL1** bits [63:0] are architecturally mapped to AArch64 System register **DBGWVR<n>_EL1[63:0]**.

External register **DBGWVR<n>_EL1** bits [31:0] are architecturally mapped to AArch32 System register **DBGWVR<n>[31:0]**.

**DBGWVR<n>_EL1** is in the Core power domain.

If watchpoint n is not implemented then accesses to this register are:

- When IsCorePowered() && !DoubleLockStatus() && !OSLockStatus() && AllowExternalDebugAccess(), RES0.
- Otherwise, a CONSTRAINED UNPREDICTABLE choice of RES0 or ERROR.

**Attributes**

**DBGWVR<n>_EL1** is a 64-bit register.

**Field descriptions**

The **DBGWVR<n>_EL1** bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**RESS[14:4]**, bits [63:53]

Reserved. Sign extended. Hardware and software must treat this field as RES0 if the most significant bit of VA is 0 or RES0, and as RES1 if the most significant bit of VA is 1.

Hardware always ignores the value of these bits and it is IMPLEMENTATION DEFINED whether:

- The bits are hardwired to a copy of the most significant bit of VA, meaning writes to these bits are ignored, and reads to the bits always return the hardwired value.
- The value in those bits can be written, and reads will return the last value written. The value held in those bits is ignored by hardware.

**VA[52:49]**, bits [52:49]

When **FEAT_LVA** is implemented:


On a Cold reset, this field resets to an architecturally UNKNOWN value.
Otherwise:


**VA[48:2], bits [48:2]**

Bits[48:2] of the address value for comparison.

When FEAT_IVA is implemented, VA[52:49] forms the upper part of the address value. Otherwise, VA[52:49] are RESS.


On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [1:0]**

Reserved, RES0.

**Accessing the DBGWVR<n>_EL1**

---

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalDebugAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

---

**DBGWVR<n>_EL1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x800 + (16 * n)</td>
<td>DBGWVR&lt;n&gt;_EL1</td>
<td>63:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalDebugAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
The EDAA32PFR characteristics are:

**Purpose**

Provides information about implemented PE features.

**Note**

The register mnemonic, EDAA32PFR, is derived from previous definitions of this register that defined this register only when AArch64 was not supported at any Exception level.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

It is IMPLEMENTATION DEFINED whether EDAA32PFR is implemented in the Core power domain or in the Debug power domain.

**Attributes**

EDAA32PFR is a 64-bit register.

**Field descriptions**

The EDAA32PFR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | MSA frac | EL3 | EL2 | PMSA | VMSA |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:20]**

Reserved, RES0.

**MSA_frac, bits [19:16]**

When EDAA32PFR.PMSA == 0b0000 and EDAA32PFR.VMSA == 0b1111:

Memory System Architecture fractional field. This holds the information on additional Memory System Architectures supported. Defined values are:

<table>
<thead>
<tr>
<th>MSA_frac</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>PMSAv8-64 supported in all translation regimes. VMSAv8-64 not supported.</td>
</tr>
<tr>
<td>0b0010</td>
<td>PMSAv8-64 supported in all translation regimes. In addition to PMSAv8-64, stage 1 EL1&amp;0 translation regime also supports VMSAv8-64.</td>
</tr>
</tbody>
</table>

All other values are reserved.
Otherwise:

Reserved, RES0.

**EL3, bits [15:12]**

When EDPFR.EL3 == 0b0000:

AArch32 EL3 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL3 is not implemented or can be executed in AArch64 state.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL3 can be executed in AArch32 state only.</td>
</tr>
</tbody>
</table>

All other values are reserved.

*Note*

EDPFR.EL3 indicates whether EL3 can only be executed in AArch32 state.

Otherwise:

Reserved, RAZ.

**EL2, bits [11:8]**

When EDPFR.EL2 == 0b0000:

AArch32 EL2 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL2 is not implemented or can be executed in AArch64 state.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL2 can be executed in AArch32 state only.</td>
</tr>
</tbody>
</table>

All other values are reserved.

*Note*

EDPFR.EL2 indicates whether EL2 can only be executed in AArch32 state.

Otherwise:

Reserved, RAZ.

**PMSA, bits [7:4]**

Indicates support for a 32-bit PMSA. Defined values are:

<table>
<thead>
<tr>
<th>PMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PMSA-32 not supported.</td>
</tr>
<tr>
<td>0b0100</td>
<td>PMSA-32 supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

**VMSA, bits [3:0]**
When $\text{EDAA32PFR.PMSA} \neq 0b0000$:

Indicates support for a VMSA in addition to a 32-bit PMSA Defined values are:

<table>
<thead>
<tr>
<th>VMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>VMSA not supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

When $\text{EDAA32PFR.PMSA} == 0b0000$:

Defined values are:

<table>
<thead>
<tr>
<th>VMSA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>VMSAv8-64 supported.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Memory system architecture described by</td>
</tr>
<tr>
<td></td>
<td>$\text{EDAA32PFR.MSA}_{frac}$.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In Armv8-A, the only permitted value is 0b0000.

Otherwise:

Reserved, RAZ.

**Accessing the EDAA32PFR**

**EDAA32PFR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD60</td>
<td>EDAA32PFR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When $\text{IsCorePowered()}$ and $\text{!DoubleLockStatus()}$ accesses to this register are **RO**.
- Otherwise accesses to this register are **IMPDEF**.
EDACR, External Debug Auxiliary Control Register

The EDACR characteristics are:

**Purpose**

Allows implementations to support **IMPLEMENTATION DEFINED** controls.

**Configuration**

It is **IMPLEMENTATION DEFINED** whether EDACR is implemented in the Core power domain or in the Debug power domain.

If FEAT_DoPD is implemented, this register is implemented in the Core power domain.

If FEAT_DoPD is not implemented, the power domain that this register is implemented in is **IMPLEMENTATION DEFINED**.

Changing this register from its reset value causes **IMPLEMENTATION DEFINED** behavior, including possible deviation from the architecturally-defined behavior.

If the EDACR contains any control bits that must be preserved over power down, then these bits must be accessible by the external debug interface when the OS Lock is locked, **OSLSR_EL1** OSLK == 1, and when the Core is powered off.

**Attributes**

EDACR is a 32-bit register.

**Field descriptions**

The EDACR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**IMPLEMENTATION DEFINED**

**IMPLEMENTATION DEFINED**, bits [31:0]

**IMPLEMENTATION DEFINED**.

The following resets apply:

- If the register is implemented in the Core power domain:
  - On a Cold reset, this field resets to an architecturally **UNKNOWN** value.
  - On an External debug reset, the value of this field is unchanged.
  - On a Warm reset, the value of this field is unchanged.

- If the register is implemented in the External debug power domain:
  - On a Cold reset, the value of this field is unchanged.
  - On an External debug reset, this field resets to an architecturally **UNKNOWN** value.
  - On a Warm reset, the value of this field is unchanged.
Accessing the EDACR

EDACR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x094</td>
<td>EDACR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register are IMPDEF.
EDCIDR0, External Debug Component Identification Register 0

The EDCIDR0 characteristics are:

Purpose

Provides information to identify an external debug component.

For more information, see 'About the Component Identification scheme'.

Configuration

Implementation of this register is OPTIONAL.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

Attributes

EDCIDR0 is a 32-bit register.

Field descriptions

The EDCIDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>7-0</td>
<td>PRMBL_0, Preamble</td>
</tr>
</tbody>
</table>

Accessing the EDCIDR0

EDCIDR0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFF0</td>
<td>EDCIDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
The EDCIDR1 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDCIDR1 is a 32-bit register.

**Field descriptions**

The EDCIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>CLASS</td>
<td>PRMBL_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**CLASS, bits [7:4]**

Component class.

<table>
<thead>
<tr>
<th>CLASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1001</td>
<td>CoreSight component.</td>
</tr>
</tbody>
</table>

Other values are defined by the CoreSight Architecture.

This field reads as 0x9.

**PRMBL_1, bits [3:0]**

Preamble.

Reads as 0b0000.
Accessing the EDCIDR1

EDCIDR1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFF4</td>
<td>EDCIDR1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDCIDR2, External Debug Component Identification Register 2

The EDCIDR2 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDCIDR2 is a 32-bit register.

**Field descriptions**

The EDCIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PRMBL_2</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PRMBL_2, bits [7:0]**

Preamble.

Reads as 0x05.

**Accessing the EDCIDR2**

**EDCIDR2 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFF8</td>
<td>EDCIDR2</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDCIDR3, External Debug Component Identification Register 3

The EDCIDR3 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDCIDR3 is a 32-bit register.

**Field descriptions**

The EDCIDR3 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_3, bits [7:0]**

Preamble.

Reads as 0xB1.

**Accessing the EDCIDR3**

EDCIDR3 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFFC</td>
<td>EDCIDR3</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDCDSR, External Debug Context ID Sample Register

The EDCDSR characteristics are:

**Purpose**

Contains the sampled value of the Context ID, captured on reading EDCSR[31:0].

**Configuration**

EDCDSR is in the Core power domain.

This register is present only when FEAT_PCSRv8 is implemented and FEAT_PCSRv8p2 is not implemented. Otherwise, direct accesses to EDCDSR are RES0.

Implemented only if the OPTIONAL PC Sample-based Profiling Extension is implemented in the external debug registers space.

**Note**

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors registers space.

**Attributes**

EDCDSR is a 32-bit register.

**Field descriptions**

The EDCDSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**CONTEXTIDR, bits [31:0]**

Context ID. The value of CONTEXTIDR that is associated with the most recent EDCSR sample. When the most recent EDCSR sample was generated:

- If EL1 is using AArch64, then the Context ID is sampled from CONTEXTIDR_EL1.
- If EL1 is using AArch32, then the Context ID is sampled from CONTEXTIDR.
- If EL3 is implemented and is using AArch32, then CONTEXTIDR is a banked register, and EDCDSR samples the current banked copy of CONTEXTIDR for the Security state that is associated with the most recent EDCSR sample.

Because the value written to EDCDSR is an indirect read of CONTEXTIDR, it is CONstrained UNPredictable whether EDCDSR is set to the original or new value if EDCSR samples:

- An instruction that writes to CONTEXTIDR.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the EDCDSR**

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

EDCDSR, External Debug Context ID Sample Register
EDCIDSR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xA4</td>
<td>EDCIDSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDDEVAFF0, External Debug Device Affinity register 0

The EDDEVAFF0 characteristics are:

**Purpose**

Copy of the low half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the external debug component relates to.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVAFF0 is a 32-bit register.

**Field descriptions**

The EDDEVAFF0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>MPIDR_EL1lo</td>
<td>MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented Exception level.</td>
</tr>
</tbody>
</table>

**Accessing the EDDEVAFF0**

**EDDEVAFF0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFA8</td>
<td>EDDEVAFF0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVAFF1, External Debug Device Affinity register 1

The EDDEVAFF1 characteristics are:

**Purpose**

Copy of the high half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the external debug component relates to.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVAFF1 is a 32-bit register.

**Field descriptions**

The EDDEVAFF1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
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<td></td>
</tr>
</tbody>
</table>

**MPIDR_EL1hi, bits [31:0]**

MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the EDDEVAFF1**

**EDDEVAFF1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFAC</td>
<td>EDDEVAFF1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVARCH, External Debug Device Architecture register

The EDDEVARCH characteristics are:

**Purpose**

Identifies the programmers' model architecture of the external debug component.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVARCH is a 32-bit register.

**Field descriptions**

The EDDEVARCH bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ARCHITECT | PRESENT | REVISION | ARCHVER | ARCHPART |

**ARCHITECT, bits [31:21]**

Defines the architecture of the component. For debug, this is Arm Limited.

Bits [31:28] are the JEP106 continuation code, 0x4.

Bits [27:21] are the JEP106 ID code, 0x3B.

**PRESENT, bit [20]**

When set to 1, indicates that the DEVARCH is present.

This field is 1 in Armv8.

**REVISION, bits [19:16]**

Defines the architecture revision. For architectures defined by Arm this is the minor revision.

For debug, the revision defined by Armv8-A is 0x0.

All other values are reserved.

**ARCHVER, bits [15:12]**

Defines the architecture version of the component. This is the same value as ID_AA64FR0_EL1, DebugVer and DBGDIDR, Version. The defined values of this field are:
<table>
<thead>
<tr>
<th>ARCHVER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0110</td>
<td>Armv8.0 Debug architecture.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv8.0 Debug architecture with Virtualization Host Extensions.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Armv8.2 Debug architecture.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Armv8.4 Debug architecture.</td>
</tr>
</tbody>
</table>

FEAT_Debugv8p4 adds the functionality indicated by the value 0b1001. FEAT_Debugv8p2 adds the functionality indicated by the value 0b1000. If FEAT_VHE is not implemented, the only permitted value is 0b0110.

The fields ARCHVER and ARCHPART together form the field ARCHID, so that ARCHVER is ARCHID[15:12].

**ARCHPART, bits [11:0]**

<table>
<thead>
<tr>
<th>ARCHPART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA15</td>
<td>The part number of the Armv8-A debug component.</td>
</tr>
</tbody>
</table>

The fields ARCHVER and ARCHPART together form the field ARCHID, so that ARCHPART is ARCHID[11:0].

**Accessing the EDDEVARCH**

EDDEVARCH can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFBC</td>
<td>EDDEVARCH</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVID, External Debug Device ID register 0

The EDDEVID characteristics are:

**Purpose**

Provides extra information for external debuggers about features of the debug implementation.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVID is a 32-bit register.

**Field descriptions**

The EDDEVID bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:28</td>
<td>AuxRegs</td>
</tr>
<tr>
<td>27:24</td>
<td>DebugPower</td>
</tr>
<tr>
<td>23:8</td>
<td>PCSample</td>
</tr>
<tr>
<td>19:16</td>
<td>RES0</td>
</tr>
<tr>
<td>15:12</td>
<td>RES0</td>
</tr>
<tr>
<td>11:8</td>
<td>AuxRegs</td>
</tr>
<tr>
<td>7:4</td>
<td>DebugPower</td>
</tr>
<tr>
<td>3:0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**Bits [31:28]**

Reserved, RES0.

**AuxRegs, bits [27:24]**

Indicates support for Auxiliary registers. Defined values are:

<table>
<thead>
<tr>
<th>AuxRegs</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>None supported.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Support for External Debug Auxiliary Control Register, EDACR.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Bits [23:8]**

Reserved, RES0.

**DebugPower, bits [7:4]**

Indicates support for the FEAT_DoPD feature. Defined values are:

<table>
<thead>
<tr>
<th>DebugPower</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>FEAT_DoPD not implemented. Registers in the external debug interface register map are implemented in a mix of the Debug and Core power domains.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_DoPD implemented. All registers in the external debug interface register map are implemented in the Core power domain.</td>
</tr>
</tbody>
</table>

FEAT_DoPD implements the functionality added by the value 0b0001.
All other values are reserved.

**PCSample, bits [3:0]**

Indicates the level of PC Sample-based Profiling support using external debug registers. Defined values are:

<table>
<thead>
<tr>
<th>PCSample</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PC Sample-based Profiling Extension is not implemented in the external debug registers space.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Only EDPCSR and EDCIDSR are implemented. This option is only permitted if EL3 and EL2 are not implemented.</td>
</tr>
<tr>
<td>0b0011</td>
<td>EDPCSR, EDCIDSR, and EDVIDSR are implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

When FEAT_PCSRv8p2 is implemented, the only permitted value is 0b0000.

**Note**

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors register space, as indicated by the value of PMDEVID.PCSample.

**Accessing the EDDEVID**

**EDDEVID can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFC8</td>
<td>EDDEVID</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVID1, External Debug Device ID register 1

The EDDEVID1 characteristics are:

**Purpose**

Provides extra information for external debuggers about features of the debug implementation.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVID1 is a 32-bit register.

**Field descriptions**

The EDDEVID1 bit assignments are:

|   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |   |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
| RES0 | PCSROffset |

**Bits [31:4]**

Reserved, RES0.

**PCSROffset, bits [3:0]**

This field indicates the offset applied to PC samples returned by reads of EDPCSR. Permitted values of this field in Armv8 are:

<table>
<thead>
<tr>
<th>PCSROffset</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EDPCSR not implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EDPCSR implemented, and samples have no offset applied and do not sample the instruction set state in AArch32 state.</td>
</tr>
</tbody>
</table>

When FEAT_PCSRv8p2 is implemented, the only permitted value is 0b0000.

**Note**

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors register space, as indicated by the value of PMDEVID.PCSample.

**Accessing the EDDEVID1**

**EDDEVID1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFC4</td>
<td>EDDEVID1</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVID2, External Debug Device ID register 2

The EDDEVID2 characteristics are:

**Purpose**

Reserved for future descriptions of features of the debug implementation.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVID2 is a 32-bit register.

**Field descriptions**

The EDDEVID2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Accessing the EDDEVID2**

**EDDEVID2 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFC0</td>
<td>EDDEVID2</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDDEVTYPE, External Debug Device Type register

The EDDEVTYPE characteristics are:

**Purpose**

Indicates to a debugger that this component is part of a PE’s debug logic.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDDEVTYPE is a 32-bit register.

**Field descriptions**

The EDDEVTYPE bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>SUB</td>
<td>0x1</td>
</tr>
<tr>
<td>28</td>
<td>MAJOR</td>
<td>0x5</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SUB, bits [7:4]**

Subtype. Must read as 0x1 to indicate this is a component within a PE.

**MAJOR, bits [3:0]**

Major type. Must read as 0x5 to indicate this is a debug logic component.

**Accessing the EDDEVTYPE**

EDDEVTYPE can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFCC</td>
<td>EDDEVTYPE</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDDFR, External Debug Feature Register

The EDDFR characteristics are:

**Purpose**

Provides top level information about the debug system.

**Note**

Debuggers must use EDDEVARCH to determine the Debug architecture version.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

It is IMPLEMENTATION DEFINED whether EDDFR is implemented in the Core power domain or in the Debug power domain.

**Attributes**

EDDFR is a 64-bit register.

**Field descriptions**

The EDDFR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>43-40</td>
<td>TraceFilt</td>
<td>Armv8.4 Self-hosted Trace Extension version. Defined values are:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0000: Armv8.4 Self-hosted Trace Extension is not implemented.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0b0001: Armv8.4 Self-hosted Trace Extension is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_TRF implements the functionality added by 0b0001.

From Armv8.4, the permitted values are 0b0000 and 0b0001.

**Bits [39:32]**

Reserved, UNKNOWN.
CTX_CMPs, bits [31:28]

Number of breakpoints that are context-aware, minus 1. These are the highest numbered breakpoints.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64DFR0_EL1.CTX_CMPs.

Bits [27:24]

Reserved, RES0.

WRPs, bits [23:20]

Number of watchpoints, minus 1. The value of 0b0000 is reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64DFR0_EL1.WRPs.

Bits [19:16]

Reserved, RES0.

BRPs, bits [15:12]

Number of breakpoints, minus 1. The value of 0b0000 is reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64DFR0_EL1.BRPs.

PMUVer, bits [11:8]

Performance Monitors Extension version.

This field does not follow the standard ID scheme, but uses the alternative ID scheme described in 'Alternative ID scheme used for the Performance Monitors Extension version'

Defined values are:

<table>
<thead>
<tr>
<th>PMUVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Performance Monitors Extension not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Performance Monitors Extension, PMUv3 implemented.</td>
</tr>
<tr>
<td>0b0100</td>
<td>PMUv3 for Armv8.1. As 0b0001, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• Extended 16-bit PMEVTYPER&lt;n&gt;_EL0(evtCount field.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the MDCR_EL2.HPMD control bit.</td>
</tr>
<tr>
<td>0b0101</td>
<td>PMUv3 for Armv8.4. As 0b0100, and also includes support for the PMMIR_EL1 register.</td>
</tr>
<tr>
<td>0b0110</td>
<td>PMUv3 for Armv8.5. As 0b0101, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• 64-bit event counters.</td>
</tr>
<tr>
<td></td>
<td>• If EL2 is implemented, the MDCR_EL2.HCCD control bit.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.SCCD control bit.</td>
</tr>
<tr>
<td>0b0111</td>
<td>PMUv3 for Armv8.7. As 0b0110, and also includes support for:</td>
</tr>
<tr>
<td></td>
<td>• The PMCR_EL0.FZO and, if EL2 is implemented, MDCR_EL2.HPMFZO control bits.</td>
</tr>
<tr>
<td></td>
<td>• If EL3 is implemented, the MDCR_EL3.{MPMX,MCCD} control bits.</td>
</tr>
<tr>
<td>0b1111</td>
<td>IMPLEMENTATION DEFINED form of performance monitors supported, PMUv3 not supported. Arm does not recommend this value for new implementations.</td>
</tr>
</tbody>
</table>

All other values are reserved.
FEAT_PMUv3 implements the functionality identified by the value 0b0001.

FEAT_PMUv3p1 implements the functionality identified by the value 0b0100.

FEAT_PMUv3p4 implements the functionality identified by the value 0b0101.

FEAT_PMUv3p5 implements the functionality identified by the value 0b0110.

FEAT_PMUv3p7 implements the functionality identified by the value 0b0111.

From Armv8.1, if FEAT_PMUv3 is implemented, the value 0b0001 is not permitted.

From Armv8.4, if FEAT_PMUv3 is implemented, the value 0b0100 is not permitted.

From Armv8.5, if FEAT_PMUv3 is implemented, the value 0b0101 is not permitted.

From Armv8.7, if FEAT_PMUv3 is implemented, the value 0b0110 is not permitted.

**TraceVer, bits [7:4]**

Trace support. Indicates whether System register interface to a PE trace unit is implemented. Defined values are:

<table>
<thead>
<tr>
<th>TraceVer</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PE trace unit System registers not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PE trace unit System registers implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

A value of 0b0000 only indicates that no System register interface to a PE trace unit is implemented. A PE trace unit might nevertheless be implemented without a System register interface.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64DFR0_EL1.TraceVer.

**Bits [3:0]**

Reserved, UNKNOWN.

**Accessing the EDDFR**

**EDDFR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD28</td>
<td>EDDFR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus() accesses to this register are RO.
- Otherwise accesses to this register are IMPDEF.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD2C</td>
<td>EDDFR</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus() accesses to this register are RO.
- Otherwise accesses to this register are IMPDEF.
EDECCR, External Debug Exception Catch Control Register

The EDECCR characteristics are:

**Purpose**

Controls Exception Catch debug events.

**Configuration**

External register EDECCR bits [31:0] are architecturally mapped to AArch64 System register OSECCR_EL1[31:0].

External register EDECCR bits [31:0] are architecturally mapped to AArch32 System register DBGOSECCR[31:0].

EDECCR is in the Core power domain.

**Attributes**

EDECCR is a 32-bit register.

**Field descriptions**

The EDECCR bit assignments are:

When FEAT_Debugv8p2 is implemented:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | NSR3 | NSR2 | NSR1 | NSR0 | SR3 | SR2 | SR1 | SR0 | NSE3 | NSE2 | NSE1 | NSE0 | SE3 | SE2 | SE1 | SE0 |

Bits [31:16]

- Reserved, RES0.

**NSR<n>, bit [n+12], for n = 3 to 0**

Controls Non-secure exception catch on exception return to EL<n> in conjunction with NSE<n>. For information, see 'Summary of Exception Catch debug event control'.

<table>
<thead>
<tr>
<th>NSR&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the corresponding NSE&lt;n&gt; bit is 0, then Exception Catch debug events are disabled for Non-secure Exception level &lt;n&gt;. If the corresponding NSE&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception entry, reset entry and exception return to Non-secure Exception level &lt;n&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the corresponding NSE&lt;n&gt; bit is 0, then Exception Catch debug events are enabled for exception returns to Non-secure Exception level &lt;n&gt;. If the corresponding NSE&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception entry and reset entry to Non-secure Exception level &lt;n&gt;.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the PE behaves as if SCR_EL3.NS is set to 0, this field is reserved, RES0.

**Note**
It is IMPLEMENTATION DEFINED whether a reset entry to an Exception level is permitted to generate an Exception Catch debug event.

A value of the NSR field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the NSR field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for NSR by a read of EDECCR is UNKNOWN.

On a Cold reset, this field resets to 0.

**SR<n>, bit [n+8], for n = 3 to 0**

Controls Secure exception catch on exception return to EL<n> in conjunction with SE<n>. For information, see ‘Summary of Exception Catch debug event control’.

<table>
<thead>
<tr>
<th>SR&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the corresponding SE&lt;n&gt; bit is 0, then Exception Catch debug events are disabled for Secure Exception level &lt;n&gt;. If the corresponding SE&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception entry, reset entry and exception return to Secure Exception level &lt;n&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the corresponding SE&lt;n&gt; bit is 0, then Exception Catch debug events are enabled for exception returns to Secure Exception level &lt;n&gt;. If the corresponding SE&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception entry and reset entry to Secure Exception level &lt;n&gt;.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the PE behaves as if SCR_EL3.NS is set to 1, this field is reserved, RES0.

**Note**

It is IMPLEMENTATION DEFINED whether a reset entry to an Exception level is permitted to generate an Exception Catch debug event.

A value of the SR field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the SR field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for SR by a read of EDECCR is UNKNOWN.

On a Cold reset, this field resets to 0.

**NSE<n>, bit [n+4], for n = 3 to 0**

Coarse-grained Non-secure exception catch for EL<n>. This controls whether Exception Catch debug events are enabled for Non-secure EL<n>. This also controls:

- The behavior of exception catch on exception entry to EL<n>.
- The behavior of exception catch on exception return to EL<n> in conjunction with NSR<n>.

<table>
<thead>
<tr>
<th>NSE&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the corresponding NSR&lt;n&gt; bit is 0, then Exception Catch debug events are disabled for Non-secure Exception level &lt;n&gt;. If the corresponding NSR&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception returns to Non-secure Exception level &lt;n&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the corresponding NSR&lt;n&gt; bit is 0, then Exception Catch debug events are enabled for exception entry, reset entry and exception return to Non-secure Exception level &lt;n&gt;. If the corresponding NSR&lt;n&gt; bit is 1, then Exception Catch debug events are enabled for exception entry and reset entry to Non-secure Exception level &lt;n&gt;.</td>
</tr>
</tbody>
</table>
If EL3 is not implemented and the PE behaves as if \texttt{SCR\_EL3\_NS} is set to 0, this field is reserved, \texttt{RES0}.

A value of the NSE field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the NSE field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for NSE by a read of EDECCR is \texttt{UNKNOWN}.

On a Cold reset, this field resets to 0.

**SE\textsubscript{\textit{n}}, bit \textit{[n]}, for n = 3 to 0**

Coarse-grained Secure exception catch for EL\textsubscript{\textit{n}}. This field controls whether Exception Catch debug events are enabled for Secure EL\textsubscript{\textit{n}}.

- The behavior of exception catch on exception entry to EL\textsubscript{\textit{n}}.
- The behavior of exception catch on exception return to EL\textsubscript{\textit{n}} in conjunction with SR\textsubscript{\textit{n}}.

<table>
<thead>
<tr>
<th>SE\textsubscript{\textit{n}}</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0}</td>
<td>If the corresponding SR\textsubscript{\textit{n}} bit is 0, then Exception Catch debug events are disabled for Secure Exception level \textsubscript{\textit{n}}. If the corresponding SR\textsubscript{\textit{n}} bit is 1, then Exception Catch debug events are enabled for exception returns to Secure Exception level \textsubscript{\textit{n}}.</td>
</tr>
<tr>
<td>\texttt{0b1}</td>
<td>If the corresponding SR\textsubscript{\textit{n}} bit is 0, then Exception Catch debug events are enabled for exception entry, reset entry and exception return to Secure Exception level \textsubscript{\textit{n}}. If the corresponding SR\textsubscript{\textit{n}} bit is 1, then Exception Catch debug events are enabled for exception entry and reset entry to Secure Exception level \textsubscript{\textit{n}}.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the PE behaves as if \texttt{SCR\_EL3\_NS} is set to 1, this field is reserved, \texttt{RES0}.

A value of the SE field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the SE field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for SE by a read of EDECCR is \texttt{UNKNOWN}.

On a Cold reset, this field resets to 0.

**Otherwise:**

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0 NSE3 NSE2 NSE1 NSE0 SE3 SE2 SE1 SE0</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, \texttt{RES0}.

**NSE\textsubscript{\textit{n}}, bit \textit{[n+4]}, for n = 3 to 0**

Coarse-grained Non-secure exception catch. If EL3 and EL2 are not implemented and the PE behaves as if \texttt{SCR\_EL3\_NS} is set to 0, this field is reserved, \texttt{RES0}. Otherwise, possible values for this field are:

<table>
<thead>
<tr>
<th>NSE\textsubscript{\textit{n}}</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>\texttt{0b0}</td>
<td>Exception Catch debug events are disabled for Non-secure Exception level \textsubscript{\textit{n}}.</td>
</tr>
<tr>
<td>\texttt{0b1}</td>
<td>Exception Catch debug events are enabled for Non-secure Exception level \textsubscript{\textit{n}}.</td>
</tr>
</tbody>
</table>

A value of the NSE field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the NSE field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for NSE by a read of EDECCR is \texttt{UNKNOWN}. 
On a Cold reset, this field resets to 0.

**SE<n>, bit [n], for n = 3 to 0**

Coarse-grained Secure exception catch.

<table>
<thead>
<tr>
<th>SE&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Exception Catch debug events are disabled for Secure Exception level &lt;n&gt;.</td>
</tr>
<tr>
<td>0b1</td>
<td>Exception Catch debug events are enabled for Secure Exception level &lt;n&gt;.</td>
</tr>
</tbody>
</table>

If EL3 is not implemented and the PE behaves as if SCR_EL3_NS is set to 1, this field is reserved, RES0.

A value of the SE field that enables an Exception Catch debug event for an Exception level that is not implemented is reserved. If the SE field is programmed with a reserved value then:

- The PE behaves as if it is programmed with a defined value, other than for a read of EDECCR.
- The value returned for SE by a read of EDECCR is UNKNOWN.

On a Cold reset, this field resets to 0.

**Accessing the EDECCR**

EDECCR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x098</td>
<td>EDECCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
The EDECR characteristics are:

**Purpose**

Controls Halting debug events.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

EDECR is a 32-bit register.

**Field descriptions**

The EDECR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
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<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>SS</td>
<td>RCE</td>
<td>OSUCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**SS, bit [2]**

Halting step enable. Possible values of this field are:

<table>
<thead>
<tr>
<th>SS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Halting step debug event disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Halting step debug event enabled.</td>
</tr>
</tbody>
</table>

If the value of EDECR.SS is changed when the PE is in Non-debug state, behavior is **CONSTRAINED UNPREDICTABLE** as described in 'Changing the value of EDECR.SS when not in Debug state'.

On a Cold reset, when FEAT_DoPD is implemented, this field resets to 0.

On an External debug reset, when FEAT_DoPD is not implemented, this field resets to 0.

**RCE, bit [1]**

**When FEAT_DoPD is not implemented:**

Reset Catch Enable.

<table>
<thead>
<tr>
<th>RCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reset Catch debug event disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset Catch debug event enabled.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 0.
Otherwise:

Reserved, RES0.

**OSUCE, bit [0]**

When FEAT_DoPD is not implemented:

OS Unlock Catch Enable.

<table>
<thead>
<tr>
<th>OSUCE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>OS Unlock Catch debug event disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>OS Unlock Catch debug event enabled.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 0.

Otherwise:

Reserved, RES0.

**Accessing the EDECR**

**EDECR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x024</td>
<td>EDECR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When (FEAT_DoPD is not implemented or IsCorePowered()) and SoftwareLockStatus() accesses to this register are **RO**.
- When (FEAT_DoPD is not implemented or IsCorePowered()) and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
EDESR, External Debug Event Status Register

The EDESR characteristics are:

**Purpose**

Indicates the status of internally pending Halting debug events.

**Configuration**

EDESR is in the Core power domain.

**Attributes**

EDESR is a 32-bit register.

**Field descriptions**

The EDESR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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<th>15</th>
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<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**SS, bit [2]**

*When FEAT_DoPD is implemented:*

Halting step debug event pending. Possible values of this field are:

<table>
<thead>
<tr>
<th>SS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reading this means that a Halting step debug event is not pending.</td>
</tr>
<tr>
<td></td>
<td>Writing this means no action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reading this means that a Halting step debug event is pending.</td>
</tr>
<tr>
<td></td>
<td>Writing this clears the pending Halting step debug event.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

*Otherwise:*

Halting step debug event pending. Possible values of this field are:

<table>
<thead>
<tr>
<th>SS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reading this means that a Halting step debug event is not pending.</td>
</tr>
<tr>
<td></td>
<td>Writing this means no action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reading this means that a Halting step debug event is pending.</td>
</tr>
<tr>
<td></td>
<td>Writing this clears the pending Halting step debug event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to the value in EDECR.SS.

**RC, bit [1]**

Reset Catch debug event pending. Possible values of this field are:
**RC, bit [0]**

Reset Catch debug event pending. Possible values of this field are:

<table>
<thead>
<tr>
<th>RC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reading this means that a Reset Catch debug event is not pending. Writing this means no action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reading this means that a Reset Catch debug event is pending. Writing this clears the pending Reset Catch debug event.</td>
</tr>
</tbody>
</table>

On a Warm reset, when FEAT_DoPD is implemented, this field resets to the value in `CTIDEVCTL.RCE`. On a Warm reset, when FEAT_DoPD is not implemented, this field resets to the value in `EDECR.RCE`.

**OSUC, bit [0]**

OS Unlock Catch debug event pending. Possible values of this field are:

<table>
<thead>
<tr>
<th>OSUC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Reading this means that an OS Unlock Catch debug event is not pending. Writing this means no action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reading this means that an OS Unlock Catch debug event is pending. Writing this clears the pending OS Unlock Catch debug event.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the EESR**

If a request to clear a pending Halting debug event is received at or about the time when halting becomes allowed, it is **CONSTRAINED UNPREDICTABLE** whether the event is taken.

If Core power is removed while a Halting debug event is pending, it is lost. However, it might become pending again when the Core is powered back on and Cold reset.

**EESR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x020</td>
<td>EESR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
**EDITCTRL, External Debug Integration mode Control register**

The EDITCTRL characteristics are:

**Purpose**

Enables the external debug to switch from its default mode into integration mode, where test software can control directly the inputs and outputs of the PE, for integration testing or topology detection.

**Configuration**

It is IMPLEMENTATION DEFINED whether EDITCTRL is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is OPTIONAL.

**Attributes**

EDITCTRL is a 32-bit register.

**Field descriptions**

The EDITCTRL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-1</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Integration mode enable (IME).</td>
</tr>
</tbody>
</table>

**IME, bit [0]**

Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED.

<table>
<thead>
<tr>
<th>IME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Integration mode enabled.</td>
</tr>
</tbody>
</table>

The following resets apply:

- Whichever power domain the register is implemented in, this field resets to 0.
- Otherwise, the value of this field is unchanged.

**Accessing the EDITCTRL**

EDITCTRL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xF00</td>
<td>EDITCTRL</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:
EDITCTRL, External Debug Integration mode Control register

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register are **IMPDEF**.
EDITR, External Debug Instruction Transfer Register

The EDITR characteristics are:

**Purpose**

Used in Debug state for passing instructions to the PE for execution.

**Configuration**

EDITR is in the Core power domain.

**Attributes**

EDITR is a 32-bit register.

**Field descriptions**

The EDITR bit assignments are:

**When AArch32 is supported at any Exception level and in AArch32 state:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    | T32Second |    | T32First |

T32Second, bits [31:16]

Second halfword of the T32 instruction to be executed on the PE. When EDITR contains a 16-bit T32 instruction, this field is ignored. For more information, see 'Behavior in Debug state'.

T32First, bits [15:0]

First halfword of the T32 instruction to be executed on the PE.

**When AArch64 is supported at any Exception level and in AArch64 state:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    | A64 instruction to be executed on the PE |

Bits [31:0]

A64 instruction to be executed on the PE.

**Accessing the EDITR**

If EDSQRITE == 0 when the PE exits Debug state on receiving a Restart request trigger event, the behavior of any instruction issued through the ITR in Normal access mode that has not completed execution is CONSTRAINED UNPREDICTABLE, and must do one of the following:

- It must complete execution in Debug state before the PE executes the restart sequence.
- It must complete execution in Non-debug state before the PE executes the restart sequence.
- It must be abandoned. This means that the instruction does not execute. Any registers or memory accessed by the instruction are left in an UNKNOWN state.

EDITR ignores writes if the PE is in Non-debug state.
EDITR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x084</td>
<td>EDITR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are **WI**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are **WO**.
- Otherwise accesses to this register generate an error response.
EDLAR, External Debug Lock Access Register

The EDLAR characteristics are:

**Purpose**

Allows or disallows access to the external debug registers through a memory-mapped interface.

The optional Software Lock provides a lock to prevent memory-mapped writes to the debug registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the debug registers. It does not, and cannot, prevent all accidental or malicious damage.

**Configuration**

If FEAT_DoPD is implemented, Software Lock is not implemented by the architecturally-defined debug components of the PE in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

Software uses EDLAR to set or clear the lock, and EDLSR to check the current status of the lock.

**Attributes**

EDLAR is a 32-bit register.

**Field descriptions**

The EDLAR bit assignments are:

**When Software Lock is implemented:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **KEY** |

**KEY, bits [31:0]**

Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.

Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory-mapped interface.

**Otherwise:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| **RES0** |

Otherwise

**Bits [31:0]**

Reserved, RES0.
Accessing the EDLAR

EDLAR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFB0</td>
<td>EDLAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are WO.
- Otherwise accesses to this register generate an error response.
EDLSR, External Debug Lock Status Register

The EDLSR characteristics are:

**Purpose**

Indicates the current status of the software lock for external debug registers.

The optional Software Lock provides a lock to prevent memory-mapped writes to the debug registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the debug registers. It does not, and cannot, prevent all accidental or malicious damage.

**Configuration**

If FEAT_DoPD is implemented, Software Lock is not implemented by the architecturally-defined debug components of the PE in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

Software uses EDLAR to set or clear the lock, and EDLSR to check the current status of the lock.

**Attributes**

EDLSR is a 32-bit register.

**Field descriptions**

The EDLSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>nTT</td>
</tr>
<tr>
<td>29</td>
<td>SLK</td>
</tr>
<tr>
<td>28</td>
<td>SLI</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**nTT, bit [2]**

Not thirty-two bit access required. RAZ.

**SLK, bit [1]**

**When Software Lock is implemented:**

Software Lock status for this component. For an access to LSR that is not a memory-mapped access, or when Software Lock is not implemented, this field is RES0.

For memory-mapped accesses when Software Lock is implemented, possible values of this field are:

<table>
<thead>
<tr>
<th>SLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Lock clear. Writes are permitted to this component's registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Lock set. Writes to this component's registers are ignored, and reads have no side effects.</td>
</tr>
</tbody>
</table>

On a Cold reset, when FEAT_DoPD is implemented, this field resets to 1.

On an External debug reset, when FEAT_DoPD is not implemented, this field resets to 1.
Otherwise:

Reserved, RAZ.

**SLI, bit [0]**

Software Lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are:

<table>
<thead>
<tr>
<th>SLI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Software Lock not implemented or not memory-mapped access.</td>
</tr>
<tr>
<td>0b1</td>
<td>Software Lock implemented and memory-mapped access.</td>
</tr>
</tbody>
</table>

**Accessing the EDLSR**

**EDLSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFB4</td>
<td>EDLSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
The EDPCSR characteristics are:

**Purpose**

Holds a sampled instruction address value.

**Configuration**

EDPCSR is in the Core power domain.

This register is present only when FEAT_PCSRv8 is implemented and FEAT_PCSRv8p2 is not implemented. Otherwise, direct accesses to EDPCSR are \texttt{RES0}.

EDPCSR is a pair of 32-bit registers.

If FEAT_VHE is implemented, the format of this register differs depending on the value of EDSCR.SC2.

Implemented only if the \texttt{OPTIONAL} PC Sample-based Profiling Extension is implemented in the external debug registers space.

**Note**

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors registers space.

**Attributes**

EDPCSR is a 64-bit register.

**Field descriptions**

The EDPCSR bit assignments are:

**When FEAT_VHE is not implemented or EDSCR.SC2 == 0:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
<th>Bit</th>
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</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
<td>53</td>
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<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
</tr>
<tr>
<td>PC Sample high word, EDPCSRhi</td>
<td>PC Sample low word</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [63:32]**

PC Sample high word, EDPCSRhi. If \texttt{EDVIDSR.HV} == 0 then this field is RAZ, otherwise bits [63:32] of the sampled instruction address value. The translation regime that EDPCSR samples can be determined from \texttt{EDVIDSR.\{NS,E2,E3\}}.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Bits [31:0]**

PC Sample low word. EDPCSRlo, bits[31:0] of the sampled instruction address value.

EDPCSRlo reads as \texttt{0xFFFFFFFF} when any of the following are true:
The PE is in Debug state.
PC Sample-based profiling is prohibited.

If an instruction has retired since the PE left Reset state, then the first read of EDPCSR[31:0] is permitted but not required to return 0xFFFFFFFF.

EDPCSRlo reads as an UNKNOWN value when any of the following are true:

- The PE is in Reset state.
- No instruction has retired since the PE left Reset state, Debug state, or a state where PC Sample-based Profiling is prohibited.
- No instruction has retired since the last read of EDPCSR[31:0].

For the cases where a read of EDPCSR[31:0] returns 0xFFFFFFFF or an UNKNOWN value, the read has the side-effect of setting EDPCSRhi, EDCIDSR, and EDVIDSR to UNKNOWN values.

Otherwise, a read of EDPCSR[31:0] returns bits [31:0] of the sampled instruction address value and has the side-effect of indirectly writing to EDPCSRhi, EDCIDSR, and EDVIDSR. The translation regime that EDPCSR samples can be determined from EDVIDSR.\{NS,E2,E3\}.

For a read of EDPCSR[31:0] from the memory-mapped interface, if EDLSR.SLK == 1, meaning the OPTIONAL Software Lock is locked, then the side-effect of the access does not occur and EDPCSRhi, EDCIDSR, and EDVIDSR are unchanged.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When FEAT_VHE is implemented and EDSRCR.SC2 == 1:

<table>
<thead>
<tr>
<th>NS</th>
<th>EL</th>
<th>RES0</th>
<th>PC Sample high word, EDPCSRhi</th>
<th>PC Sample low word</th>
<th>EDPCSR, External Debug Program Counter Sample Register</th>
</tr>
</thead>
</table>

**NS, bit [63]**
Non-secure state sample. Indicates the Security state that is associated with the most recent EDPCSR sample or, when it is read as a single atomic 64-bit read, the current EDPCSR sample. The translation regime that EDPCSR samples can be determined from EDPCSR.\{NS,EL\}.

If EL3 is not implemented, this bit indicates the Effective value of SCR.NS.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sample is from Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sample is from Non-secure state.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**EL, bits [62:61]**
Exception level status sample. Indicates the Exception level that is associated with the most recent EDPCSR sample or, when it is read as a single atomic 64-bit read, the current EDPCSR sample. The translation regime that EDPCSR samples can be determined from EDPCSR.\{NS,EL\}.

<table>
<thead>
<tr>
<th>EL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Sample is from EL0.</td>
</tr>
<tr>
<td>0b01</td>
<td>Sample is from EL1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Sample is from EL2.</td>
</tr>
<tr>
<td>0b11</td>
<td>Sample is from EL3.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Bits [60:56]**
Reserved, RES0.
Bits [55:32]

PC Sample high word, EDPCSRhi. Bits [55:32] of the sampled instruction address value. The translation regime that EDPCSR samples can be determined from EDPCSR.{NS,EL}.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [31:0]

PC Sample low word. EDPCSRlo, bits[31:0] of the sampled instruction address value.

EDPCSRlo reads as 0xFFFFFFFF when any of the following are true:

- The PE is in Debug state.
- PC Sample-based profiling is prohibited.

If an instruction has retired since the PE left Reset state, then the first read of EDPCSR[31:0] is permitted but not required to return 0xFFFFFFFF.

EDPCSRlo reads as an UNKNOWN value when any of the following are true:

- The PE is in Reset state.
- No instruction has retired since the PE left Reset state, Debug state, or a state where PC Sample-based Profiling is prohibited.
- No instruction has retired since the last read of EDPCSR[31:0].

For the cases where a read of EDPCSR[31:0] returns 0xFFFFFFFF or an UNKNOWN value, the read has the side-effect of setting EDPCSRhi, EDCIDSR, and EDVIDSR to UNKNOWN values.

Otherwise, a read of EDPCSR[31:0] returns bits [31:0] of the sampled instruction address value and has the side-effect of indirectly writing to EDPCSRhi, EDCIDSR, and EDVIDSR. The translation regime that EDPCSR samples can be determined from EDPCSR.{NS,EL}.

For a read of EDPCSR[31:0] from the memory-mapped interface, if EDLSR.SLK == 1, meaning the OPTIONAL Software Lock is locked, then the side-effect of the access does not occur and EDPCSRhi, EDCIDSR, and EDVIDSR are unchanged.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Accessing the EDPCSR

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'

EDPCSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x0A0</td>
<td>EDPCSR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x0AC</td>
<td>EDPCSR</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDPFR, External Debug Processor Feature Register

The EDPFR characteristics are:

**Purpose**

Provides information about implemented PE features.

For general information about the interpretation of the ID registers, see 'Principles of the ID scheme for fields in ID registers'.

**Configuration**

It is IMPLEMENTATION DEFINED whether EDPFR is implemented in the Core power domain or in the Debug power domain.

**Attributes**

EDPFR is a 64-bit register.

**Field descriptions**

The EDPFR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| UNKNOWN | UNKNOWN | RES0 | UNKNOWN | AMU | UNKNOWN | SEL2 | SVE |
| UNKNOWN | GIC | AdvSIMD | FP | EL3 | EL2 | EL1 | EL0 |

**Bits [63:60]**

From Armv8.5:

Reserved, UNKNOWN.

Otherwise:

Reserved, RES0.

**Bits [59:56]**

From Armv8.5:

Reserved, UNKNOWN.

Otherwise:

Reserved, RES0.

**Bits [55:52]**

Reserved, RES0.
Bits [51:48]
From Armv8.4:
Reserved, UNKNOWN.

Otherwise:
Reserved, RES0.

AMU, bits [47:44]
Indicates support for Activity Monitors Extension. Defined values are:

<table>
<thead>
<tr>
<th>AMU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Activity Monitors Extension is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>FEAT_AMUv1 is implemented.</td>
</tr>
<tr>
<td>0b0010</td>
<td>FEAT_AMUv1p1 is implemented. As 0b0001 and adds support for virtualization of the activity monitor event counters.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_AMUv1 implements the functionality identified by the value 0b0001.

FEAT_AMUv1p1 implements the functionality identified by the value 0b0010.

In Armv8.0, the only permitted value is 0b0000.

In Armv8.4, the permitted values are 0b0000 and 0b0010.

From Armv8.6, the permitted values are 0b0000, 0b0001, and 0b0010.

Bits [43:40]
From Armv8.2:
Reserved, UNKNOWN.

Otherwise:
Reserved, RES0.

SEL2, bits [39:36]
Secure EL2. Defined values are:

<table>
<thead>
<tr>
<th>SEL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Secure EL2 is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Secure EL2 is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

SVE, bits [35:32]
Scalable Vector Extension. Defined values are:

<table>
<thead>
<tr>
<th>SVE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>SVE is not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>SVE is implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Bits [31:28]
From Armv8.2:

Reserved, UNKNOWN.

Otherwise:

Reserved, RES0.

**GIC, bits [27:24]**

System register GIC interface support. Defined values are:

<table>
<thead>
<tr>
<th>GIC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>GIC CPU interface system registers not implemented.</td>
</tr>
<tr>
<td>0b0001</td>
<td>System register interface to versions 3.0 and 4.0 of the GIC CPU interface is supported.</td>
</tr>
<tr>
<td>0b0011</td>
<td>System register interface to version 4.1 of the GIC CPU interface is supported.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of `ID_AA64PFR0_EL1.GIC`.

**AdvSIMD, bits [23:20]**

Advanced SIMD. Defined values are:

<table>
<thead>
<tr>
<th>AdvSIMD</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0000 | Advanced SIMD is implemented, including support for the following SISD and SIMD operations:  
• Integer byte, halfword, word and doubleword element operations.  
• Single-precision and double-precision floating-point arithmetic.  
• Conversions between single-precision and half-precision data types, and double-precision and half-precision data types. |
| 0b0001 | As for 0b0000, and also includes support for half-precision floating-point arithmetic. |
| 0b1111 | Advanced SIMD is not implemented.                                      |

All other values are reserved.

This field must have the same value as the FP field.

The permitted values are:

• 0b0000 in an implementation with Advanced SIMD support, that does not include the FEAT_FP16 extension.  
• 0b0001 in an implementation with Advanced SIMD support, that includes the FEAT_FP16 extension.  
• 0b1111 in an implementation without Advanced SIMD support.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of `ID_AA64PFR0_EL1.AdvSIMD`.

**FP, bits [19:16]**

Floating-point. Defined values are:
Meaning

<table>
<thead>
<tr>
<th>FP</th>
<th>Floating-point is implemented, and includes support for:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>• Single-precision and double-precision floating-point types.</td>
</tr>
<tr>
<td></td>
<td>• Conversions between single-precision and half-precision data types, and double-precision and half-precision data types.</td>
</tr>
<tr>
<td>0b0001</td>
<td>As for 0b0000, and also includes support for half-precision floating-point arithmetic.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Floating-point is not implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field must have the same value as the AdvSIMD field.

The permitted values are:

- 0b0000 in an implementation with floating-point support, that does not include the FEAT_FP16 extension.
- 0b0001 in an implementation with floating-point support, that includes the FEAT_FP16 extension.
- 0b1111 in an implementation without floating-point support.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64PFR0_EL1.FP.

### EL3, bits [15:12]

AArch64 EL3 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL3 is not implemented or cannot be executed in AArch64 state.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL3 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL3 can be executed in both Execution states.</td>
</tr>
</tbody>
</table>

When the value of EDAA32PFR.EL3 is non-zero, this field must be 0b0000.

All other values are reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64PFR0_EL1.EL3.

### EL2, bits [11:8]

AArch64 EL2 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL2 is not implemented or cannot be executed in AArch64 state.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL2 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL2 can be executed in both Execution states.</td>
</tr>
</tbody>
</table>

When the value of EDAA32PFR.EL2 is non-zero, this field must be 0b0000.

All other values are reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64PFR0_EL1.EL2.

### EL1, bits [7:4]

AArch64 EL1 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL1 cannot be executed in AArch64 state.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL1 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL1 can be executed in both Execution states.</td>
</tr>
</tbody>
</table>
All other values are reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64PFR0_EL1.EL0.

### EL0, bits [3:0]

AArch64 EL0 Exception level handling. Defined values are:

<table>
<thead>
<tr>
<th>EL0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>EL0 cannot be executed in AArch64 state.</td>
</tr>
<tr>
<td></td>
<td>EL0 can be executed in AArch32 state only.</td>
</tr>
<tr>
<td>0b0001</td>
<td>EL0 can be executed in AArch64 state only.</td>
</tr>
<tr>
<td>0b0010</td>
<td>EL0 can be executed in both Execution states.</td>
</tr>
</tbody>
</table>

All other values are reserved.

In an Armv8-A implementation that supports AArch64 state in at least one Exception level, this field returns the value of ID_AA64PFR0_EL1.EL0.

### Accessing the EDPFR

**EDPFR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD20</td>
<td>EDPFR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register are **IMPDEF**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD24</td>
<td>EDPFR</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register are **IMPDEF**.
The EDPIDR0 characteristics are:

**Purpose**

Provides information to identify an external debug component.
For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is OPTIONAL.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDPIDR0 is a 32-bit register.

**Field descriptions**

The EDPIDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>PART_0</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PART_0, bits [7:0]**

Part number, least significant byte.

**Accessing the EDPIDR0**

EDPIDR0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFE0</td>
<td>EDPIDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
**EDPIDR1, External Debug Peripheral Identification Register 1**

The EDPIDR1 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDPIDR1 is a 32-bit register.

**Field descriptions**

The EDPIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>DES_0</td>
<td>Designer, least significant nibble of JEP106 ID code. For Arm Limited, this field is 0b1011.</td>
</tr>
<tr>
<td>29</td>
<td>PART_1</td>
<td>Part number, most significant nibble.</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**DES_0, bits [7:4]**

Designer, least significant nibble of JEP106 ID code. For Arm Limited, this field is 0b1011.

**PART_1, bits [3:0]**

Part number, most significant nibble.

**Accessing the EDPIDR1**

**EDPIDR1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFE4</td>
<td>EDPIDR1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDPIDR2, External Debug Peripheral Identification Register 2

The EDPIDR2 characteristics are:

Purpose

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

Implementation of this register is \textit{OPTIONAL}.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

Attributes

EDPIDR2 is a 32-bit register.

Field descriptions

The EDPIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit positions</th>
<th>Bit name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[31:8]</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>[7:4]</td>
<td>REVISION</td>
<td>Part major revision. Parts can also use this field to extend Part number to 16-bits.</td>
</tr>
<tr>
<td>[3]</td>
<td>JEDEC</td>
<td>RAO. Indicates a JEP106 identity code is used.</td>
</tr>
<tr>
<td>[2:0]</td>
<td>DES_1</td>
<td>Designer, most significant bits of JEP106 ID code. For Arm Limited, this field is 0b011.</td>
</tr>
</tbody>
</table>

Accessing the EDPIDR2

EDPIDR2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFE8</td>
<td>EDPIDR2</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDPIDR3, External Debug Peripheral Identification Register 3

The EDPIDR3 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is *OPTIONAL*.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDPIDR3 is a 32-bit register.

**Field descriptions**

The EDPIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>0</td>
</tr>
<tr>
<td>30</td>
<td>REVAND</td>
<td>0</td>
</tr>
<tr>
<td>29</td>
<td>CMOD</td>
<td>0</td>
</tr>
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<td>4</td>
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<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**REVAND, bits [7:4]**

Part minor revision. Parts using EDPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.

**CMOD, bits [3:0]**

Customer modified. Indicates someone other than the Designer has modified the component.

**Accessing the EDPIDR3**

EDPIDR3 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFEC</td>
<td>EDPIDR3</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDPIDR4, External Debug Peripheral Identification Register 4

The EDPIDR4 characteristics are:

**Purpose**

Provides information to identify an external debug component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

EDPIDR4 is a 32-bit register.

**Field descriptions**

The EDPIDR4 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>SIZE</td>
</tr>
<tr>
<td>29</td>
<td>DES_2</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SIZE, bits [7:4]**

Size of the component. RAZ. Log2 of the number of 4KB pages from the start of the component to the end of the component ID registers.

**DES_2, bits [3:0]**

Designer, JEP106 continuation code, least significant nibble. For Arm Limited, this field is 0b0100.

**Accessing the EDPIDR4**

**EDPIDR4 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xFD0</td>
<td>EDPIDR4</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
EDPRCR, External Debug Power/Reset Control Register

The EDPRCR characteristics are:

**Purpose**

Controls the PE functionality related to powerup, reset, and powerdown.

**Configuration**

EDPRCR contains fields that are in the Core power domain and fields that are in the Debug power domain.

If FEAT_DoPD is implemented then all fields in this register are in the Core power domain.

CORENPDRQ is the only field that is mapped between the EDPRCR and DBGPRCR and DBGPRCR_EL1.

**Attributes**

EDPRCR is a 32-bit register.

**Field descriptions**

The EDPRCR bit assignments are:

**When FEAT_DoPD is implemented:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | CWRR | CORENPDRQ |

**Bits [31:2]**

Reserved, RES0.

**CWRR, bit [1]**

Warm reset request.

The extent of the reset is IMPLEMENTATION DEFINED, but must be one of:

- The request is ignored.
- Only this PE is Warm reset.
- This PE and other components of the system, possibly including other PEs, are Warm reset.

Arm deprecates use of this bit, and recommends that implementations ignore the request.

<table>
<thead>
<tr>
<th>CWRR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Request Warm reset.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain

The PE ignores writes to this bit if any of the following are true:

- ExternalInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Non-secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Secure state.
• ExternalSecureInvasiveDebugEnabled() == FALSE and EL3 is implemented.

In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.

On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

• When OSLockStatus() or SoftwareLockStatus(), access to this field is RAZ/WI.
• Otherwise, access to this field is WO/RAZ.

CORENPDRQ, bit [0]

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

When this bit reads as UNKNOWN, the PE ignores writes to this bit.

This field is in the Core power domain, and permitted accesses to this field map to the DBGPRCR CORENPDRQ and DBGPRCR_EL1 CORENPDRQ fields.

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to the Cold reset value on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states, see 'Core power domain power states'.

Note

Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, if the powerup request is implemented and the powerup request has been asserted, this field is an IMPLEMENTATION DEFINED choice of 0 or 1. If the powerup request is not asserted, this field is set to 0.

Accessing this field has the following behavior:

• When OSLockStatus(), access to this field is UNKNOWN/WI.
• When SoftwareLockStatus(), access to this field is RO.
• Otherwise, access to this field is RW.

Otherwise:

<table>
<thead>
<tr>
<th>Bits [31:4]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

COREPURQ, bit [3]

Core powerup request. Allows a debugger to request that the power controller power up the core, enabling access to the debug register in the Core power domain, and that the power controller emulates powerdown.
This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>COREPURQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not request power up of the Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>Request power up of the Core power domain, and emulation of powerdown.</td>
</tr>
</tbody>
</table>

In an implementation that includes the recommended external debug interface, this bit drives the DBGPWRUPREQ signal.

This field is in the Debug power domain and can be read and written when the Core power domain is powered off.

**Note**

 Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On an External debug reset, this field resets to 0.

Accessing this field has the following behavior:

- When SoftwareLockStatus(), access to this field is RO.
- Otherwise, access to this field is RW.

**Bit [2]**

Reserved, RES0.

**CWRR, bit [1]**

Warm reset request.

The extent of the reset is IMPLEMENTATION DEFINED, but must be one of:

- The request is ignored.
- Only this PE is Warm reset.
- This PE and other components of the system, possibly including other PEs, are Warm reset.

Arm deprecates use of this bit, and recommends that implementations ignore the request.

<table>
<thead>
<tr>
<th>CWRR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Request Warm reset.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain

The PE ignores writes to this bit if any of the following are true:

- ExternalInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Non-secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE, EL3 is not implemented, and the implemented Security state is Secure state.
- ExternalSecureInvasiveDebugEnabled() == FALSE and EL3 is implemented.

In an implementation that includes the recommended external debug interface, this bit drives the DBGRSTREQ signal.

On a Warm reset, this field resets to 0.

Accessing this field has the following behavior:

- When !IsCorePowered(), or DoubleLockStatus(), or OSLockStatus() or SoftwareLockStatus(), access to this field is RAZ/WI.
- Otherwise, access to this field is WO/RAZ.
CORENPDRQ, bit [0]

Core no powerdown request. Requests emulation of powerdown.

This request is typically passed to an external power controller. This means that whether a request causes power up is dependent on the IMPLEMENTATION DEFINED nature of the system. The power controller must not allow the Core power domain to switch off while this bit is 1.

<table>
<thead>
<tr>
<th>CORENPDRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the system responds to a powerdown request, it powers down Core power domain.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the system responds to a powerdown request, it does not powerdown the Core power domain, but instead emulates a powerdown of that domain.</td>
</tr>
</tbody>
</table>

When this bit reads as UNKNOWN, the PE ignores writes to this bit.

This field is in the Core power domain, and permitted accesses to this field map to the DBGPRCR, CORENPDRQ and DBGPRCR_EL1, CORENPDRQ fields.

In an implementation that includes the recommended external debug interface, this bit drives the DBGNOPWRDWN signal.

It is IMPLEMENTATION DEFINED whether this bit is reset to the value of EDPRCR, COREPURQ on exit from an IMPLEMENTATION DEFINED software-visible retention state. For more information about retention states, see 'Core power domain power states'.

Note

 Writes to this bit are not prohibited by the IMPLEMENTATION DEFINED authentication interface. This means that a debugger can request emulation of powerdown regardless of whether invasive debug is permitted.

On a Cold reset, this field resets to the value in EDPRCR, COREPURQ.

Accessing this field has the following behavior:

- When !IsCorePowered(), or DoubleLockStatus() or OSLockStatus(), access to this field is UNKNOWN/WI.
- When SoftwareLockStatus(), access to this field is RO.
- Otherwise, access to this field is RW.

Accessing the EDPRCR

On permitted accesses to the register, other access controls affect the behavior of some fields. See the field descriptions for more information.

EDPRCR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x310</td>
<td>EDPRCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When (FEAT_DoPD is not implemented or IsCorePowered()) and SoftwareLockStatus() accesses to this register are RO.
- When (FEAT_DoPD is not implemented or IsCorePowered()) and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
EDPRSR, External Debug Processor Status Register

The EDPRSR characteristics are:

**Purpose**

Holds information about the reset and powerdown state of the PE.

**Configuration**

EDPRSR contains fields that are in the Core power domain and fields that are in the Debug power domain.

If FEAT_DoPD is implemented then all fields in this register are in the Core power domain.

**Attributes**

EDPRSR is a 32-bit register.

**Field descriptions**

The EDPRSR bit assignments are:

\[
\begin{array}{ccccccccccccc}
\hline
\text{RES0} & \text{SDR} & \text{SPMAD} & \text{EPMAD} & \text{SDAD} & \text{EDAD} & \text{DLK} & \text{OSLK} & \text{HALTED} & \text{SR} & \text{R} & \text{SPD} & \text{PU} \\
\end{array}
\]

**Bits [31:12]**

Reserved, RES0.

**SDR, bit [11]**

Sticky Debug Restart. Set to 1 when the PE exits Debug state.

Permitted values are:

<table>
<thead>
<tr>
<th>SDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The PE has not restarted since EDPRSR was last read.</td>
</tr>
<tr>
<td>0b1</td>
<td>The PE has restarted since EDPRSR was last read.</td>
</tr>
</tbody>
</table>

**Note**

If a reset occurs when the PE is in Debug state, the PE exits Debug state. SDR is \textit{UNKNOWN} on Warm reset, meaning a debugger must also use the SR bit to determine whether the PE has left Debug state.

If The Core power domain is powered up, then following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE this bit clears to 0.
- If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, it is \textit{CONSTRAINED UNPREDICTABLE} whether this bit clears to 0 or is unchanged.

This field is in the Core power domain.

On a Warm reset, this field resets to an architecturally \textit{UNKNOWN} value.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is \textit{UNKNOWN/WI}. 

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When SoftwareLockStatus(), access to this field is RO.

Otherwise, access to this field is RC/WI.

**SPMAD, bit [10]**

When FEAT_Debugv8p4 is implemented:

Sticky EPMAD error. Set to 1 if an external debug interface access to a Performance Monitors register returns an error because AllowExternalPMUAccess() == FALSE.

Permitted values are:

<table>
<thead>
<tr>
<th>SPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Non-secure external debug interface accesses to the external Performance Monitors registers have failed because AllowExternalPMUAccess() == FALSE for the access since EDPRSR was last read.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one Non-secure external debug interface access to the external Performance Monitors register has failed and returned an error because AllowExternalPMUAccess() == FALSE for the access since EDPRSR was last read.</td>
</tr>
</tbody>
</table>

If the Core power domain is powered up, then, following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE, this bit clears to 0.
- If FEAT_DoubleLock is implemented, and DoubleLockStatus() == TRUE, it is CONSTRAINED UNPREDICTABLE whether this bit clears to 0 or is unchanged.

This field is in the Core power domain.

On a Cold reset, this field resets to 0.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is UNKNOWN/WI.
- When SoftwareLockStatus(), access to this field is RO.
- Otherwise, access to this field is RC/WI.

**Otherwise:**

Sticky EPMAD error.

<table>
<thead>
<tr>
<th>SPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No external debug interface accesses to the Performance Monitors registers have failed because AllowExternalPMUAccess() == FALSE since EDPRSR was last read.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one external debug interface access to the Performance Monitors registers has failed and returned an error because AllowExternalPMUAccess() == FALSE since EDPRSR was last read.</td>
</tr>
</tbody>
</table>

If the Core power domain is powered up, then, following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE, this bit clears to 0.
- If FEAT_DoubleLock is implemented, and DoubleLockStatus() == TRUE, it is CONSTRAINED UNPREDICTABLE whether this bit clears to 0 or is unchanged.

This field is in the Core power domain.

On a Cold reset, this field resets to 0.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or OSIStatus(), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is UNKNOWN/WI.
- When SoftwareLockStatus(), access to this field is RO.
• Otherwise, access to this field is RC/WI.

**EPMAD, bit [9]**

*When FEAT_Debugv8p4 is implemented:*

External Performance Monitors Access Disable status.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Non-secure Performance Monitors access enabled. AllowExternalPMUAccess() == TRUE for a Non-secure access.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Non-secure Performance Monitors access disabled. AllowExternalPMUAccess() == FALSE for a Non-secure access.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

**Otherwise:**

External Performance Monitors access disable status.

<table>
<thead>
<tr>
<th>EPMAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Performance Monitors access enabled. AllowExternalPMUAccess() == TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Performance Monitors access disabled. AllowExternalPMUAccess() == FALSE.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or OSLockStatus(), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

**SDAD, bit [8]**

*When FEAT_Debugv8p4 is implemented:*

Sticky EDAD error. Set to 1 if an external debug interface access to a debug register returns an error because AllowExternalDebugAccess() == FALSE.

<table>
<thead>
<tr>
<th>SDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Non-secure external debug interface accesses to the debug registers have failed because AllowExternalDebugAccess() == FALSE for the access since EDPRSR was last read.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one Non-secure external debug interface access to the debug registers has failed and returned an error because AllowExternalDebugAccess() == FALSE for the access since EDPRSR was last read.</td>
</tr>
</tbody>
</table>

If the Core power domain is powered up, then, following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE this bit clears to 0.
- If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, it is CONSTRAINED UNPREDICTABLE whether this bit clears to 0 or is unchanged.

This field is in the Core power domain.

On a Cold reset, this field resets to 0.
EDPRSR, External Debug Processor Status Register

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is **UNKNOWN/WI**.
- Otherwise, access to this field is **RO**.

**Otherwise:**

Sticky EDAD error. Set to 1 if an external debug interface access to a debug register returns an error because AllowExternalDebugAccess() == FALSE.

<table>
<thead>
<tr>
<th>SDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No external debug interface accesses to the debug registers have failed because AllowExternalDebugAccess() == FALSE since EDPRSR was last read.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one external debug interface access to the debug registers has failed and returned an error because AllowExternalDebugAccess() == FALSE since EDPRSR was last read.</td>
</tr>
</tbody>
</table>

If the Core power domain is powered up, then, following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE this bit clears to 0.
- If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, it is **CONSTRAINED UNPREDICTABLE** whether this bit clears to 0 or is unchanged.

This bit is **UNKNOWN** on reads if OSLockStatus() == TRUE and external debug writes to OSLAR_EL1 do not return an error when AllowExternalDebugAccess() == FALSE.

This field is in the Core power domain.

On a Cold reset, this field resets to 0.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is **UNKNOWN/WI**.
- Otherwise, access to this field is **RO**.

**EDAD, bit [7]**

**When FEAT_Debugv8p4 is implemented:**

External Debug Access Disable status.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Non-secure access to breakpoint registers, watchpoint registers, and OSLAR_EL1 enabled. AllowExternalDebugAccess() == TRUE for a Non-secure access.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Non-secure access to breakpoint registers, watchpoint registers, and OSLAR_EL1 disabled. AllowExternalDebugAccess() == FALSE for a Non-secure access.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is **UNKNOWN/WI**.
- Otherwise, access to this field is **RO**.

**When FEAT_Debugv8p2 is implemented:**

External Debug Access Disable status.
**EDAD**

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External access to breakpoint registers, watchpoint registers, and OSLAR_EL1 enabled. AllowExternalDebugAccess() == TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>External access to breakpoint registers, watchpoint registers, and OSLAR_EL1 disabled. AllowExternalDebugAccess() == FALSE.</td>
</tr>
</tbody>
</table>

This bit is not valid and reads **UNKNOWN** if OSLockStatus() == TRUE and external debug writes to OSLAR_EL1 do not return an error when AllowExternalDebugAccess() == FALSE.

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is **UNKNOWN/WI**.
- Otherwise, access to this field is **RO**.

### Otherwise:

External Debug Access Disable status.

<table>
<thead>
<tr>
<th>EDAD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External access to breakpoint registers, watchpoint registers, and OSLAR_EL1 enabled. AllowExternalDebugAccess() == TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>External access to breakpoint registers, watchpoint registers disabled. It is <strong>IMPLEMENTATION DEFINED</strong> whether accesses to OSLAR_EL1 are enabled or disabled. AllowExternalDebugAccess() == FALSE.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), or DoubleLockStatus() or EDPRSR.R == 1, access to this field is **UNKNOWN/WI**.
- Otherwise, access to this field is **RO**.

### DLK, bit [6]

#### When FEAT_Debugv8p4 is implemented:

This field is **RES0**.

#### When FEAT_Debugv8p2 is implemented and FEAT_DoubleLock is implemented:

Double Lock.

From Armv8.2, this field is deprecated.

This field is in the Core power domain.

Accessing this field has the following behavior:

- When IsCorePowered() and !DoubleLockStatus(), access to this field is **RAZ/WI**.
- Otherwise, access to this field is **UNKNOWN/WI**.

#### When FEAT_DoubleLock is implemented:

Double Lock.

This field returns the result of the pseudocode function DoubleLockStatus().
If the Core power domain is powered up and DoubleLockStatus() == TRUE, it is IMPLEMENTATION DEFINED whether:

- EDPRSR.PU reads as 1, EDPRSR.DLK reads as 1, and EDPRSR.SPD is UNKNOWN.
- EDPRSR.PU reads as 0, EDPRSR.DLK is UNKNOWN, and EDPRSR.SPD reads as 0.

This field is in the Core power domain.

<table>
<thead>
<tr>
<th>DLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>DoubleLockStatus() returns FALSE.</td>
</tr>
<tr>
<td>0b1</td>
<td>DoubleLockStatus() returns TRUE and the Core power domain is powered up.</td>
</tr>
</tbody>
</table>

Accessing this field has the following behavior:

- When FEAT_DoPD is not implemented and !IsCorePowered(), access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

Otherwise:

Reserved, RES0.

OSLK, bit [5]

OS Lock status bit.

A read of this bit returns the value of OLSR_EL1.OSLK.

This field is in the Core power domain.

Accessing this field has the following behavior:

- When (FEAT_DoPD is not implemented and !IsCorePowered()), DoubleLockStatus() and EDPRSR.R == 1, access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

HALTED, bit [4]

Halted status bit.

<table>
<thead>
<tr>
<th>HALTED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PE is in Non-debug state.</td>
</tr>
<tr>
<td>0b1</td>
<td>PE is in Debug state.</td>
</tr>
</tbody>
</table>

This field is in the Core power domain.

Accessing this field has the following behavior:

- When FEAT_DoPD is not implemented and !IsCorePowered(), access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

SR, bit [3]

Sticky core Reset status bit.

Permitted values are:

<table>
<thead>
<tr>
<th>SR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The non-debug logic of the PE is not in reset state and has not been reset since the last time EDPRSR was read.</td>
</tr>
<tr>
<td>0b1</td>
<td>The non-debug logic of the PE is in reset state or has been reset since the last time EDPRSR was read.</td>
</tr>
</tbody>
</table>

If EDPRSR.PU reads as 1 and EDPRSR.R reads as 0, which means that the Core power domain is in a powerup state and that the non-debug logic of the PE is not in reset state, then following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE this bit clears to 0.
• If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, it is UNPREDICTABLE whether this bit clears to 0 or is unchanged.

This field is in the Core power domain.

On a Warm reset, this field resets to 1.

Accessing this field has the following behavior:
• When (FEAT_DoPD is not implemented and !IsCorePowered()) or DoubleLockStatus(), access to this field is UNKNOWN/WI.
• When SoftwareLockStatus(), access to this field is RO.
• Otherwise, access to this field is RC/WI.

R, bit [2]

PE Reset status bit.
Permitted values are:

<table>
<thead>
<tr>
<th>R</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The non-debug logic of the PE is not in reset state.</td>
</tr>
<tr>
<td>0b1</td>
<td>The non-debug logic of the PE is in reset state.</td>
</tr>
</tbody>
</table>

If FEAT_DoubleLock is implemented, the PE is in reset state, and the PE entered reset state with the OS Double Lock locked this bit has a CONSTRAINED UNPREDICTABLE value. For more information, see 'EDPRSR.{DLK, R} and reset state'.

This field is in the Core power domain.

Accessing this field has the following behavior:
• When (FEAT_DoPD is not implemented and !IsCorePowered()) or DoubleLockStatus(), access to this field is UNKNOWN/WI.
• Otherwise, access to this field is RO.

SPD, bit [1]

Sticky core Powerdown status bit.

If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, then:
• If FEAT_Debugv8p2 is implemented, this bit reads as 0.
• If FEAT_Debugv8p2 is not implemented, this bit might read as 0 or 1.

For more information, see 'EDPRSR.{DLK, SPD, PU} and the Core power domain'.

<table>
<thead>
<tr>
<th>SPD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If EDPRSR.PU is 0, it is not known whether the state of the debug registers in the Core power domain is lost. If EDPRSR.PU is 1, the state of the debug registers in the Core power domain has not been lost.</td>
</tr>
<tr>
<td>0b1</td>
<td>The state of the debug registers in the Core power domain has been lost.</td>
</tr>
</tbody>
</table>

If the Core power domain is powered up, then, following a read of EDPRSR:
• If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE this bit clears to 0.
• If FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, it is CONSTRAINED UNPREDICTABLE whether this bit clears to 0 or is unchanged.

When FEAT_DoPD is not implemented and the Core power domain is in either retention or powerdown state, the value of EDPRSR.SPD is IMPLEMENTATION DEFINED. For more information, see 'EDPRSR.SPD when the Core domain is in either retention or powerdown state'.

EDPRSR.{DLK, SPD, PU} describe whether registers in the Core power domain can be accessed, and whether their state has been lost since the last time the register was read. For more information, see 'EDPRSR.{DLK, SPD, PU} and the Core power domain'.

This field is in the Core power domain.
On a Cold reset, this field resets to 1.

Accessing this field has the following behavior:

- When FEAT_DoPD is not implemented and !IsCorePowered(), access to this field is RAZ/WI.
- When IsCorePowered() and DoubleLockStatus(), access to this field is UNKNOWN/WI.
- Otherwise, access to this field is RO.

**PU, bit [0]**

When FEAT_DoPD is implemented:

Core powerup status bit.

Access to this field is RAO/WI.

When FEAT_Debugv8p2 is implemented:

Core Powerup status bit. Indicates whether the debug registers in the Core power domain can be accessed.

<table>
<thead>
<tr>
<th>PU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Either the Core power domain is in a low-power or powerdown state, or FEAT_DoubleLock is implemented and DoubleLockStatus() == TRUE, meaning the debug registers in the Core power domain cannot be accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Core power domain is in a powerup state, and either FEAT DoubleLock is not implemented or DoubleLockStatus() == FALSE, meaning the debug registers in the Core power domain can be accessed.</td>
</tr>
</tbody>
</table>

If FEAT_DoubleLock is implemented, the PE is in reset state, and the PE entered reset state with the OS Double Lock locked this bit has a CONSTRAINED UNPREDICTABLE value. For more information, see 'EDPRSR.{DLK, R} and reset state'

EDPRSR.{DLK, SPD, PU} describe whether registers in the Core power domain can be accessed, and whether their state has been lost since the last time the register was read. For more information, see 'EDPRSR.{DLK, SPD, PU} and the Core power domain'

Access to this field is RO.

Otherwise:

Core Powerup status bit. Indicates whether the debug registers in the Core power domain can be accessed.

When the Core power domain is powered-up and DoubleLockStatus() == TRUE, then the value of EDPRSR.PU is IMPLEMENTATION DEFINED. See the description of the DLK bit for more information.

Otherwise, permitted values are:

<table>
<thead>
<tr>
<th>PU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Core power domain is in a low-power or powerdown state where the debug registers in the Core power domain cannot be accessed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Core power domain is in a powerup state where the debug registers in the Core power domain can be accessed.</td>
</tr>
</tbody>
</table>

If FEAT_DoubleLock is implemented, the Core power domain is powered up, and DoubleLockStatus() == TRUE, it is IMPLEMENTATION DEFINED whether this bit reads as 0 or 1.

If FEAT_DoubleLock is implemented, the PE is in reset state, and the PE entered reset state with the OS Double Lock locked this bit has a CONSTRAINED UNPREDICTABLE value. For more information see 'EDPRSR.{DLK, R} and reset state'

EDPRSR.{DLK, SPD, PU} describe whether registers in the Core power domain can be accessed, and whether their state has been lost since the last time the register was read. For more information, see 'EDPRSR.{DLK, SPD, PU} and the Core power domain'.

Access to this field is RO.
Accessing the EDPRSR

On permitted accesses to the register, other access controls affect the behavior of some fields. See the field descriptions for more information.

If the Core power domain is powered up (EDPRSR.PU == 1), then following a read of EDPRSR:

- If FEAT_DoubleLock is not implemented or DoubleLockStatus() == FALSE, then:
  - EDPRSR.{SDR, SPMAD, SDAD, SPD} are cleared to 0.
  - EDPRSR.SR is cleared to 0 if the non-debug logic of the PE is not in reset state (EDPRSR.R == 0).
- Otherwise it is CONSTRAINED UNPREDICTABLE whether or not this clearing occurs.

If FEAT_DoPD is not implemented and the Core power domain is powered down (EDPRSR.PU == 0), then:

- EDPRSR.{SDR, SPMAD, SDAD, SR} are all UNKNOWN, and are either reset or restored on being powered up.
- EDPRSR.SPD is not cleared following a read of EDPRSR. See the SPD bit description for more information.

The clearing of bits is an indirect write to EDPRSR.

EDPRSR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x314</td>
<td>EDPRSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
EDCR, External Debug Reserve Control Register

The EDCR characteristics are:

**Purpose**

This register is used to allow imprecise entry to Debug state and clear sticky bits in ESCR.

**Configuration**

EDCR is in the Core power domain.

**Attributes**

EDCR is a 32-bit register.

**Field descriptions**

The EDCR bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit 31</th>
<th>Bit 30</th>
<th>Bit 29</th>
<th>Bit 28</th>
<th>Bit 27</th>
<th>Bit 26</th>
<th>Bit 25</th>
<th>Bit 24</th>
<th>Bit 23</th>
<th>Bit 22</th>
<th>Bit 21</th>
<th>Bit 20</th>
<th>Bit 19</th>
<th>Bit 18</th>
<th>Bit 17</th>
<th>Bit 16</th>
<th>Bit 15</th>
<th>Bit 14</th>
<th>Bit 13</th>
<th>Bit 12</th>
<th>Bit 11</th>
<th>Bit 10</th>
<th>Bit 9</th>
<th>Bit 8</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:5]**

Reserved, RES0.

**CBRRQ, bit [4]**

Allow imprecise entry to Debug state. The actions on writing to this bit are:

<table>
<thead>
<tr>
<th>CBRRQ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Allow imprecise entry to Debug state, for example by canceling pending bus accesses.</td>
</tr>
</tbody>
</table>

Setting this bit to 1 allows a debugger to request imprecise entry to Debug state. An External Debug Request debug event must be pending before the debugger sets this bit to 1.

This feature is optional. If this feature is not implemented, writes to this bit are ignored.

**CSPA, bit [3]**

Clear Sticky Pipeline Advance. This bit is used to clear the ESCR.PipeAdv bit to 0. The actions on writing to this bit are:

<table>
<thead>
<tr>
<th>CSPA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Clear the ESCR.PipeAdv bit to 0.</td>
</tr>
</tbody>
</table>

**CSE, bit [2]**

Clear Sticky Error. Used to clear the ESCR cumulative error bits to 0. The actions on writing to this bit are:
<table>
<thead>
<tr>
<th>CSE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Clear the EDSCR (TXU, RXO, ERR) bits, and, if the PE is in Debug state, the EDSCR.ITO bit, to 0.</td>
</tr>
</tbody>
</table>

**Bits [1:0]**

Reserved, RES0.

**Accessing the EDRCR**

**EDRCR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x090</td>
<td>EDRCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are **WI**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are **WO**.
- Otherwise accesses to this register generate an error response.
EDSCR, External Debug Status and Control Register

The EDSCR characteristics are:

**Purpose**

Main control register for the debug implementation.

**Configuration**

External register EDSCR bits [30:29] are architecturally mapped to AArch64 System register MDCCSR_EL0[30:29].

EDSCR is in the Core power domain.

**Attributes**

EDSCR is a 32-bit register.

**Field descriptions**

The EDSCR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| TFO | RXfull | TXfull | TXU | PipeAdv | ITE | INTdis | TDA | MASC | 2 | NS | RES0 | SDD | RES0 | HDE | RW | EL | ERR | STATUS |

**TFO, bit [31]**

When FEAT_TRF is implemented:

Trace Filter Override. Overrides the Trace Filter controls allowing the external debugger to trace any visible Exception level.

<table>
<thead>
<tr>
<th>TFO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>000</td>
<td>Trace Filter controls are not affected.</td>
</tr>
<tr>
<td>001</td>
<td>Trace Filter controls in TRFCR_EL1, TRFCR_EL2 are ignored. Trace Filter controls TRFCR and HTRFCR are ignored.</td>
</tr>
</tbody>
</table>

When OLSR_EL1.OSLK == 1, this bit can be indirectly read and written through the MDSCR_EL1 and DBGDSCRExt System registers.

This bit is ignored by the PE when ExternalSecureNoninvasiveDebugEnabled() == FALSE and the Effective value of MDCR_EL3.STE == 1.

On a Cold reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**RXfull, bit [30]**

DTRRX full.

On a Cold reset, this field resets to 0.

Access to this field is RO.
**TXfull, bit [29]**

DTRTX full.

On a Cold reset, this field resets to 0.

Access to this field is **RO**.

**ITO, bit [28]**

ITR overrun.

If the PE is in Non-debug state, this bit is **UNKNOWN**. ITO is set to 0 on entry to Debug state.

Access to this field is **RO**.

**RXO, bit [27]**

DTRRX overrun.

On a Cold reset, this field resets to 0.

Access to this field is **RO**.

**TXU, bit [26]**

DTRTX underrun.

On a Cold reset, this field resets to 0.

Access to this field is **RO**.

**PipeAdv, bit [25]**

Pipeline advance. Set to 1 every time the PE pipeline retires one or more instructions. Cleared to 0 by a write to **EDRCR.CSPA**.

The architecture does not define precisely when this bit is set to 1. It requires only that this happen periodically in Non-debug state to indicate that software execution is progressing.

Access to this field is **RO**.

**ITE, bit [24]**

ITR empty.

If the PE is in Non-debug state, this bit is **UNKNOWN**. It is always valid in Debug state.

Access to this field is **RO**.

**INTdis, bits [23:22]**

When **FEAT_Debugv8p4** is implemented:

Interrupt disable. Disables taking interrupts in Non-Debug state.

<table>
<thead>
<tr>
<th><strong>INTdis</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Masking of interrupts is controlled by PSTATE and interrupt routing controls.</td>
</tr>
<tr>
<td>0b01</td>
<td>If <strong>ExternalSecureDebugEnabled() == TRUE</strong>, then all interrupts, including virtual and SError interrupts, are masked. If <strong>ExternalSecureDebugEnabled() == FALSE</strong>, then all interrupts targeting Non-secure state are masked.</td>
</tr>
</tbody>
</table>
When \texttt{OSLSR\_EL1\_OSLK} == 1, this field can be indirectly read and written through the \texttt{MDSCR\_EL1} and \texttt{DBGDSCR\_Ext} System registers.

This field is ignored by the PE and treated as zero when \texttt{ExternalDebugEnabled}() == FALSE.

When \texttt{FEAT\_Debugv8p4} is implemented, bit[23] of the register is \texttt{RES0}.

On a Cold reset, this field resets to 0.

\textbf{Otherwise:}

Interrupt disable.

When \texttt{OSLSR\_EL1\_OSLK} == 1, this field can be indirectly read and written through the \texttt{MDSCR\_EL1} and \texttt{DBGDSCR\_Ext} System registers.

<table>
<thead>
<tr>
<th>INTdis</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Do not disable interrupts.</td>
</tr>
<tr>
<td>0b01</td>
<td>Disable interrupts taken to Non-secure EL1.</td>
</tr>
<tr>
<td>0b10</td>
<td>Disable interrupts taken only to Non-secure EL1 and Non-secure EL2. If \texttt{ExternalSecureInvasiveDebugEnabled}() == TRUE, also disable interrupts taken to Secure EL1.</td>
</tr>
<tr>
<td>0b11</td>
<td>Disable interrupts taken only to Non-secure EL1 and Non-secure EL2. If \texttt{ExternalSecureInvasiveDebugEnabled}() == TRUE, also disable all other interrupts.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

\textbf{TDA, bit [21]}

Traps accesses to the following debug System registers:

- AArch64: \texttt{DBGBCR<n>\_EL1}, \texttt{DBGVR<n>\_EL1}, \texttt{DBGWCR<n>\_EL1}, \texttt{DBGWVR<n>\_EL1}.
- AArch32: \texttt{DBGBCR<n>}, \texttt{DBGVR<n>}, \texttt{DBGXVR<n>}, \texttt{DBGWCR<n>}, \texttt{DBGWVR<n>}.

The possible values of this field are:

<table>
<thead>
<tr>
<th>TDA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Accesses to debug System registers do not generate a Software Access Debug event.</td>
</tr>
<tr>
<td>0b1</td>
<td>Accesses to debug System registers generate a Software Access Debug event, if \texttt{OSLSR_EL1_OSLK} is 0 and if halting is allowed.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

\textbf{MA, bit [20]}

Memory access mode. Controls the use of memory-access mode for accessing ITR and the DCC. This bit is ignored if in Non-debug state and set to zero on entry to Debug state.

Possible values of this field are:

<table>
<thead>
<tr>
<th>MA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal access mode.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory access mode.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

\textbf{SC2, bit [19]}

When \texttt{FEAT\_PCSRv8} is implemented, (\texttt{FEAT\_VHE} is implemented or \texttt{FEAT\_Debugv8p2} is implemented) and \texttt{FEAT\_PCSRv8p2} is not implemented:

Sample \texttt{CONTEXTIDR\_EL2}. Controls whether the PC Sample-based Profiling Extension samples \texttt{CONTEXTIDR\_EL2} or \texttt{VTTBR\_EL2} VMID.
On a Cold reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**NS, bit [18]**

Non-secure status. When in Debug state, gives the current Security state:

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure state, IsSecure() == TRUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure state, IsSecure() == FALSE.</td>
</tr>
</tbody>
</table>

In Non-debug state, this bit is **UNKNOWN**.

Access to this field is **RO**.

**Bit [17]**

Reserved, RES0.

**SDD, bit [16]**

Secure debug disabled.

On entry to Debug state:

- If entering in Secure state, SDD is set to 0.
- If entering in Non-secure state, SDD is set to the inverse of ExternalSecureInvasiveDebugEnabled().

In Debug state, the value of the SDD bit does not change, even if ExternalSecureInvasiveDebugEnabled() changes.

In Non-debug state:

- SDD returns the inverse of ExternalSecureInvasiveDebugEnabled(). If the authentication signals that control ExternalSecureInvasiveDebugEnabled() change, a context synchronization event is required to guarantee their effect.
- This bit is unaffected by the Security state of the PE.

If EL3 is not implemented and the implementation is Non-secure, this bit is **RES1**.

Access to this field is **RO**.

**Bit [15]**

Reserved, RES0.

**HDE, bit [14]**

Halting debug enable. The possible values of this field are:

<table>
<thead>
<tr>
<th>HDE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Halting disabled for Breakpoint, Watchpoint and Halt Instruction debug events.</td>
</tr>
<tr>
<td>0b1</td>
<td>Halting enabled for Breakpoint, Watchpoint and Halt Instruction debug events.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.
**RW, bits [13:10]**

Exception level Execution state status. In Debug state, each bit gives the current Execution state of each Exception level.

<table>
<thead>
<tr>
<th>RW</th>
<th>Meaning</th>
<th>Applies when</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>All Exception levels are using AArch64 or the PE is in Non-debug state.</td>
<td></td>
</tr>
<tr>
<td>0b1110</td>
<td>The PE is in Debug state. EL0 is using AArch32. All other Exception levels are using AArch64. Only permitted if the PE is executing at EL0.</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b110x</td>
<td>The PE is in Debug state. EL0 and EL1 are using AArch32. EL2 and EL3 are using AArch64. Only permitted if EL2 is implemented and enabled in the current Security state.</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b10xx</td>
<td>The PE is in Debug state. EL0, EL1, and, if implemented in the current Security state, EL2 are using AArch32. EL3 is using AArch64.</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
<tr>
<td>0b0xxx</td>
<td>The PE is in Debug state. All Exception levels are using AArch32.</td>
<td>When AArch32 is supported at any Exception level</td>
</tr>
</tbody>
</table>

In Non-debug state, this field is RAO.

Access to this field is RO.

**EL, bits [9:8]**

Exception level. In Debug state, this gives the current Exception level of the PE.

In Non-debug state, this field is RAZ.

Access to this field is RO.

**A, bit [7]**

SErrror interrupt pending. In Debug state, indicates whether an SError interrupt is pending:

- If \( \text{HCR EL2.\{AMO, TGE\}} = \{1, 0\} \), EL2 is enabled in the current Security state, and the PE is executing at EL0 or EL1, a virtual SError interrupt.
- Otherwise, a physical SError interrupt.

<table>
<thead>
<tr>
<th>A</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No SError interrupt pending.</td>
</tr>
<tr>
<td>0b1</td>
<td>SError interrupt pending.</td>
</tr>
</tbody>
</table>

A debugger can read EDSCR to check whether an SError interrupt is pending without having to execute further instructions. A pending SError might indicate data from target memory is corrupted.

UNKNOWN in Non-debug state.

Access to this field is RO.

**ERR, bit [6]**

Cumulative error flag. This bit is set to 1 following exceptions in Debug state and on any signaled overrun or underrun on the DTR or EDITR.

On a Cold reset, this field resets to 0.
Access to this field is RO.

**STATUS, bits [5:0]**

Debug status flags.

<table>
<thead>
<tr>
<th>STATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000001</td>
<td>PE is restarting, exiting Debug state.</td>
</tr>
<tr>
<td>0b000010</td>
<td>PE is in Non-debug state.</td>
</tr>
<tr>
<td>0b000111</td>
<td>Breakpoint.</td>
</tr>
<tr>
<td>0b010011</td>
<td>External debug request.</td>
</tr>
<tr>
<td>0b011011</td>
<td>Halting step, normal.</td>
</tr>
<tr>
<td>0b011111</td>
<td>Halting step, exclusive.</td>
</tr>
<tr>
<td>0b100011</td>
<td>OS Unlock Catch.</td>
</tr>
<tr>
<td>0b100111</td>
<td>Reset Catch.</td>
</tr>
<tr>
<td>0b101011</td>
<td>Watchpoint.</td>
</tr>
<tr>
<td>0b101111</td>
<td>HLT instruction.</td>
</tr>
<tr>
<td>0b110011</td>
<td>Software access to debug register.</td>
</tr>
<tr>
<td>0b110111</td>
<td>Exception Catch.</td>
</tr>
<tr>
<td>0b111011</td>
<td>Halting step, no syndrome.</td>
</tr>
</tbody>
</table>

All other values of STATUS are reserved.

Access to this field is RO.

**Accessing the EDSCR**

EDSCR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x088</td>
<td>EDSCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `IsCorePowered()`, `!DoubleLockStatus()`, `!OSLockStatus()` and `SoftwareLockStatus()` accesses to this register are **RO**.
- When `IsCorePowered()`, `!DoubleLockStatus()`, `!OSLockStatus()` and `!SoftwareLockStatus()` accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
EDVIDSR, External Debug Virtual Context Sample Register

The EDVIDSR characteristics are:

**Purpose**

Contains sampled values captured on reading EDPCSR[31:0].

**Configuration**

EDVIDSR is in the Core power domain.

This register is present only when FEAT_PCSRv8 is implemented and FEAT_PCSRv8p2 is not implemented. Otherwise, direct accesses to EDVIDSR are RES0.

If FEAT_VHE is implemented, the format of this register differs depending on the value of EDSCR.SC2.

Implemented only if the OPTIONAL PC Sample-based Profiling Extension is implemented in the external debug registers space.

When the PC Sample-based Profiling Extension is implemented in the external debug registers space, if EL2 is not implemented and EL3 is not implemented, it is IMPLEMENTATION DEFINED whether EDVIDSR is implemented.

**Note**

FEAT_PCSRv8p2 implements the PC Sample-based Profiling Extension in the Performance Monitors registers space.

**Attributes**

EDVIDSR is a 32-bit register.

**Field descriptions**

The EDVIDSR bit assignments are:

When **FEAT_VHE is not implemented or EDSCR.SC2 == 0:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>NS</td>
</tr>
<tr>
<td>30</td>
<td>E2</td>
</tr>
<tr>
<td>29</td>
<td>E3</td>
</tr>
<tr>
<td>28</td>
<td>HV</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>VMID[15:8]</td>
</tr>
<tr>
<td>25</td>
<td>VMID</td>
</tr>
</tbody>
</table>

This format applies in all Armv8.0 implementations.

**NS, bit [31]**

Non-secure state sample. Indicates the Security state associated with the most recent EDPCSR sample.

If EL3 is not implemented, this bit indicates the Effective value of SCR.NS.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sample is from Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sample is from Non-secure state.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**E2, bit [30]**
When EL2 is implemented:

Exception level 2 status sample. Indicates whether the most recent EDPCSR sample was associated with EL2.

<table>
<thead>
<tr>
<th>E2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sample is not from EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sample is from EL2.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

E3, bit [29]

When EL3 is implemented and the highest implemented Exception level is using AArch64 state:

Exception level 3 status sample. Indicates whether the most recent EDPCSR sample was associated with EL3 using AArch64.

<table>
<thead>
<tr>
<th>E3</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sample is not from EL3 using AArch64.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sample is from EL3 using AArch64.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

HV, bit [28]

EDPCSRhi (EDPCSR[63:32]) valid. Indicates whether bits [63:32] of the most recent EDPCSR sample might be nonzero:

<table>
<thead>
<tr>
<th>HV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Bits[63:32] of the most recent EDPCSR sample are zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Bits[63:32] of the most recent EDPCSR sample might be nonzero.</td>
</tr>
</tbody>
</table>

An EDVIDSR.HV value of 1 does not mean that the value of EDPCSRhi is nonzero. An EDVIDSR.HV value of 0 is a hint that EDPCSRhi (EDPCSR[63:32]) does not need to be read.

On a Cold reset, this field resets to an architecturally unknown value.

Bits [27:16]

Reserved, RES0.

VMID[15:8], bits [15:8]

When FEAT_VMID16 is implemented and EL2 is implemented:

Extension to VMID[7:0]. See VMID[7:0] for more details.

On a Cold reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.
VMID, bits [7:0]
When EL2 is implemented:

VMID sample. The VMID associated with the most recent EDPCSRlo (EDPCSR[31:0]) sample. When the most recent EDPCSR sample was generated:

• This field is RES0 if any of the following apply:
  ◦ The PE is executing in Secure state.
  ◦ The PE is executing at EL2.
• Otherwise:
  ◦ If EL2 is using AArch64 and either FEAT_VMID16 is not implemented or VTCR_EL2.VS is 1, this field is set to VTTBR_EL2.VMID.
  ◦ If EL2 is using AArch64, FEAT_VMID16 is implemented, and VTCR_EL2.VS is 0, PMVIDSR.VMID[7:0] is set to VTTBR_EL2.VMID[7:0] and PMVIDSR.VMID[15:8] is RES0.
  ◦ If EL2 is using AArch32, this field is set to VTTBR.VMID.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

When (FEAT_VHE is implemented or FEAT_Debugv8p2 is implemented) and EDSR.SC2 == 1:

CONTEXTIDR_EL2, bits [31:0]

Context ID. The value of CONTEXTIDR_EL2 that is associated with the most recent EDPCSR sample. When the most recent EDPCSR sample was generated:

• If EL2 was using AArch64 and the PE was executing in Non-secure state, then this field is set to the Context ID sampled from CONTEXTIDR_EL2.
• If EL2 was using AArch32 or the PE was executing in Secure state, then this field is set to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Accessing the EDVIDSR

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

EDVIDSR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x0A8</td>
<td>EDVIDSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
• Otherwise accesses to this register generate an error response.
EDWAR, External Debug Watchpoint Address Register

The EDWAR characteristics are:

**Purpose**

Returns the virtual data address being accessed when a Watchpoint Debug Event was triggered.

**Configuration**

EDWAR is in the Core power domain.

**Attributes**

EDWAR is a 64-bit register.

**Field descriptions**

The EDWAR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Watchpoint address | Watchpoint address |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:0]**

Watchpoint address. The data virtual address being accessed when a Watchpoint Debug Event was triggered and caused entry to Debug state. This address must be within a naturally-aligned block of memory of power-of-two size no larger than the DC ZVA block size.

The value of this register is **UNKNOWN** if the PE is in Non-debug state, or if Debug state was entered other than for a Watchpoint debug event.

The value of EDWAR[63:32] is **UNKNOWN** if Debug state was entered for a Watchpoint debug event taken from AArch32 state.

The EDWAR is subject to the same alignment rules as the reporting of a watchpointed address in the FAR. See 'Determining the memory location that caused a Watchpoint exception'.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the EDWAR**

**EDWAR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x030</td>
<td>EDWAR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x034</td>
<td>EDWAR</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:
• When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
• Otherwise accesses to this register generate an error response.
ERRCIDR0, Component Identification Register 0

The ERRCIDR0 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRCIDR0 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCIDR0 is a 32-bit register.

**Field descriptions**

The ERRCIDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>7-0</td>
<td>PRMBL_0</td>
<td>Component identification preamble, segment 0. Reads as 0x0D.</td>
</tr>
</tbody>
</table>

**Accessing the ERRCIDR0**

**ERRCIDR0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFF0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
**ERRCIDR1, Component Identification Register 1**

The ERRCIDR1 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRCIDR1 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCIDR1 is a 32-bit register.

**Field descriptions**

The ERRCIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>RES0, Bits [31:8]</td>
</tr>
<tr>
<td></td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td></td>
<td>CLASS, Bits [7:4]</td>
</tr>
<tr>
<td></td>
<td>Component class</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>CLASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1111</td>
<td>Generic peripheral with IMPLEMENTATION DEFINED register layout.</td>
</tr>
</tbody>
</table>

Other values are defined by the CoreSight Architecture.

This field reads as 0xF.

**PRMBL_1, Bits [3:0]**

Component identification preamble, segment 1.

Reads as 0b0000.

**Accessing the ERRCIDR1**

ERRCIDR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFF4</td>
</tr>
</tbody>
</table>
Accesses on this interface are **RO**.
The ERRCIDR2 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRCIDR2 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCIDR2 is a 32-bit register.

**Field descriptions**

The ERRCIDR2 bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| PRMBL_2 |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_2, bits [7:0]**

Component identification preamble, segment 2.

Reads as 0x05.

**Accessing the ERRCIDR2**

**ERRCIDR2 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFF8</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The ERRCIDR3 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRCIDR3 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCIDR3 is a 32-bit register.

**Field descriptions**

The ERRCIDR3 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | PRMBL_3 |

**Bits [31:8]**

Reserved, RES0.

**PRMBL_3, bits [7:0]**

Component identification preamble, segment 3.

Reads as 0xB1.

**Accessing the ERRCIDR3**

**ERRCIDR3 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFFC</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
ERRCRICR0, Critical Error Interrupt Configuration Register 0

The ERRCRICR0 characteristics are:

**Purpose**

Critical Error Interrupt configuration register.

**Configuration**

This register is present only when (the Critical Error Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRCRICR0 are RES0.

ERRCRICR0 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCRICR0 is a 64-bit register.

**Field descriptions**

The ERRCRICR0 bit assignments are:

When the Critical Error Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:

<table>
<thead>
<tr>
<th>Bit(s)</th>
<th>Field Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:56]</td>
<td>Bits [63:56]</td>
</tr>
<tr>
<td>[1:0]</td>
<td>Bits [1:0]</td>
</tr>
</tbody>
</table>

**Bits [63:56]**

Reserved, RES0.

**ADDR, bits [55:2]**

Message Signaled Interrupt address. (ERRCRICR0.ADDR << 2) is the address that the component writes to when signaling the Critical Error Interrupt. Bits [1:0] of the address are always zero.

The physical address size supported by the component is IMPLEMENTATION DEFINED. Unimplemented high-order physical address bits are RES0.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

**Bits [1:0]**

Reserved, RES0.
When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

Accessing the ERRCRICR0

ERRCRICR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xEA0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRCRICR1, Critical Error Interrupt Configuration Register 1

The ERRCRICR1 characteristics are:

**Purpose**

Critical Error Interrupt configuration register.

**Configuration**

This register is present only when (the Critical Error Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRCRICR1 are RES0.

ERRCRICR1 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCRICR1 is a 32-bit register.

**Field descriptions**

The ERRCRICR1 bit assignments are:

*When the Critical Error Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:*

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| **DATA** |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**DATA, bits [31:0]**

Payload for the message signaled interrupt.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

*When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:*

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
| **IMPLEMENTATION DEFINED** |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

**Accessing the ERRCRICR1**

ERRCRICR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xEA8</td>
</tr>
</tbody>
</table>
Accesses on this interface are **RW**.
ERRCRICR2, Critical Error Interrupt Configuration Register 2

The ERRCRICR2 characteristics are:

**Purpose**

Critical Error Interrupt control and configuration register.

**Configuration**

This register is present only when (the Critical Error Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRCRICR2 are RES0.

ERRCRICR2 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRCRICR2 is a 32-bit register.

**Field descriptions**

The ERRCRICR2 bit assignments are:

**When the Critical Error Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>30</td>
<td>IRQEN</td>
<td>Message signaled interrupt enable. Enables generation of message signaled interrupts.</td>
</tr>
<tr>
<td>29</td>
<td>NSMSI</td>
<td>Message signaled interrupt enable.</td>
</tr>
<tr>
<td>28</td>
<td>SH</td>
<td>Message signaled interrupts are always enabled.</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**IRQEN, bit [7]**

**When the component supports disabling message signaled interrupts:**

<table>
<thead>
<tr>
<th>IRQEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enabled.</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

Message signaled interrupt enable.

Message signaled interrupts are always enabled.
**NSMSI, bit [6]**

When the component supports configuring the Security attribute for message signaled interrupts and the component does not allow Non-secure writes to ERRCRICR2:

Security attribute. Defines the physical address space for message signaled interrupts.

<table>
<thead>
<tr>
<th>NSMSI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure.</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to an implementation defined value.

When the component allows Non-secure writes to ERRCRICR2:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute used for message signaled interrupts is Non-secure.

Otherwise:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute for message signaled interrupts is implementation defined.

**SH, bits [5:4]**

When the component supports configuring the Shareability domain:

Shareability. Defines the Shareability domain for message signaled interrupts.

<table>
<thead>
<tr>
<th>SH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not shared.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is ignored when ERRCRICR2.MemAttr specifies any of the following memory types:

- Any Device memory type.
- Normal memory, Inner Non-cacheable, Outer Non-cacheable.

All Device and Normal Inner Non-cacheable Outer Non-cacheable memory regions are always treated as Outer Shareable.

On an Error recovery reset, this field resets to an architecturally unknown value.

Otherwise:

Reserved, RES0.

Shareability.

The Shareability domain for message signaled interrupts is implementation defined.
**MemAttr, bits [3:0]**

When the component supports configuring the memory type for message signaled interrupts:

Memory type. Defines the memory type and attributes for message signaled interrupts.

<table>
<thead>
<tr>
<th>MemAttr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Device-nGnRE memory.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Device-nGRE memory.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Device-GRE memory.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Normal memory, Inner Non-cacheable, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Normal memory, Inner Write-Through, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Normal memory, Inner Write-Back, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Normal memory, Inner Write-Through, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Normal memory, Inner Write-Back, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1101</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Normal memory, Inner Write-Through, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Normal memory, Inner Write-Back, Outer Write-Back.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Note**

This is the same format as the VMSAv8-64 stage 2 memory region attributes.

On an Error recovery reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

Memory type.

The memory type used for message signaled interrupts is **IMPLEMENTATION DEFINED**.

**When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:**

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**IMPLEMENTATION DEFINED, bits [31:0]**

**IMPLEMENTATION DEFINED.**

**Accessing the ERRCRICR2**

**ERRCRICR2 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xEAC</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
ERRDEVAFF, Device Affinity Register

The ERRDEVAFF characteristics are:

**Purpose**

For a group of error records that has affinity with a single PE or a group of PEs, ERRDEVAFF is a copy of `MPIDR_EL1` or part of `MPIDR_EL1`:

- If the group of error records has affinity with a single PE, the affinity level is 0, ERRDEVAFF reads the same value as `MPIDR_EL1`, and ERRDEVAFF.F0V reads-as-one to indicate affinity level 0.
- If the group of error records has affinity with a group of PEs, the affinity level is 1, 2, or 3, parts of ERRDEVAFF reads the same value as parts of `MPIDR_EL1`, and the rest of ERRDEVAFF indicates the level.

For example, if the group of PEs is a subset of the PEs at affinity level 1 then all of the following are true:

- All the PEs in the group have the same values in `MPIDR_EL1`.\{Aff3,Aff2\}, and these values are equal to ERRDEVAFF.\{Aff3,Aff2\}.
- ERRDEVAFF.Aff1 is nonzero and not 0x80, and ERRDEVAFF.\{Aff0,F0V\} read-as-zero, to indicate at least affinity level 1. The subset of PEs at level 1 that the group of error records has affinity with is indicated by the least-significant set bit in ERRDEVAFF.Aff1. In this example, if ERRDEVAFF.Aff1[2:0] is 0b100, then the group of error records has affinity with the up-to 8 PEs that have `MPIDR_EL1`.Aff1[7:3] == ERRDEVAFF.Aff1[7:3].

If RAS System Architecture v1.1 is not implemented, ERRDEVAFF can only describe a group of error records that is affine with a single PE or all the PEs at an affinity level.

**Configuration**

This register is present only when the group of error records has affinity with a PE or cluster of PEs. Otherwise, direct accesses to ERRDEVAFF are `RES0`.

ERRDEVAFF is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRDEVAFF is a 64-bit register.

**Field descriptions**

The ERRDEVAFF bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Bit Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-40</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>39-32</td>
<td>PE affinity level 3. The <code>MPIDR_EL1</code>.Aff3 field, viewed from the highest Exception level of the associated PE or PEs.</td>
</tr>
<tr>
<td>31</td>
<td>Indicates that the ERRDEVAFF.Aff0 field is valid.</td>
</tr>
</tbody>
</table>

**Bits [63:40]**

Reserved, RES0.

**Aff3, bits [39:32]**

PE affinity level 3. The `MPIDR_EL1`.Aff3 field, viewed from the highest Exception level of the associated PE or PEs.

**F0V, bit [31]**

 Indicates that the ERRDEVAFF.Aff0 field is valid.
### F0V

<table>
<thead>
<tr>
<th><strong>F0V</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERRDEVAFF.Aff0 is not valid, and the PE affinity is above level 0 or a subset of level 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERRDEVAFF.Aff0 is valid, and the PE affinity is at level 0.</td>
</tr>
</tbody>
</table>

#### U, bit [30]

When ERRDEVAFF.F0V == 1:

Uniprocessor: The MPIDR_EL1.U bit, viewed from the highest Exception level of the associated PE.

Otherwise:

Reserved, UNKNOWN.

#### Bits [29:25]

Reserved, RES0.

#### MT, bit [24]

When ERRDEVAFF.F0V == 1:

Multithreaded. The MPIDR_EL1.MT bit, viewed from the highest Exception level of the associated PE.

Otherwise:

Reserved, UNKNOWN.

#### Aff2, bits [23:16]

When affine with a PE or PEs at affinity level 2 or below:

PE affinity level 2. The MPIDR_EL1.Aff2 field, viewed from the highest Exception level of the associated PE or PEs.

When affine with a sub-set of PEs at affinity level 2:

PE affinity level 2. Defines part of the MPIDR_EL1.Aff2 field, viewed from the highest Exception level of the associated PEs.

<table>
<thead>
<tr>
<th><strong>Aff2</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxxxxxxx1</td>
<td>ERRDEVAFF.Aff2[7:1] is the value of MPIDR_EL1.Aff2[7:1], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxxx10</td>
<td>ERRDEVAFF.Aff2[7:2] is the value of MPIDR_EL1.Aff2[7:2], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxx100</td>
<td>ERRDEVAFF.Aff2[7:3] is the value of MPIDR_EL1.Aff2[7:3], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxx1000</td>
<td>ERRDEVAFF.Aff2[7:4] is the value of MPIDR_EL1.Aff2[7:4], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxx100000</td>
<td>ERRDEVAFF.Aff2[7:5] is the value of MPIDR_EL1.Aff2[7:5], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bx1000000</td>
<td>ERRDEVAFF.Aff2[7] is the value of MPIDR_EL1.Aff2[7], viewed from the highest Exception level of the associated PEs.</td>
</tr>
</tbody>
</table>
Otherwise:

PE affinity level 2. Indicates whether the PE affinity is at level 3.

<table>
<thead>
<tr>
<th>Aff2</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x80</td>
<td>PE affinity is at level 3.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Aff1, bits [15:8]**

When affine with a PE or PEs at affinity level 1 or below:

PE affinity level 1. The \texttt{MPIDR\_EL1.Aff1} field, viewed from the highest Exception level of the associated PE or PEs.

When affine with a sub-set of PEs at affinity level 1:

PE affinity level 1. Defines part of the \texttt{MPIDR\_EL1.Aff1} field, viewed from the highest Exception level of the associated PEs.

<table>
<thead>
<tr>
<th>Aff1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxxxxxxx1</td>
<td>\texttt{ERRDEVAFF.Aff1}[7:1] is the value of \texttt{MPIDR_EL1.Aff1}[7:1], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxxx10</td>
<td>\texttt{ERRDEVAFF.Aff1}[7:2] is the value of \texttt{MPIDR_EL1.Aff1}[7:2], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxx100</td>
<td>\texttt{ERRDEVAFF.Aff1}[7:3] is the value of \texttt{MPIDR_EL1.Aff1}[7:3], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxx10000</td>
<td>\texttt{ERRDEVAFF.Aff1}[7:4] is the value of \texttt{MPIDR_EL1.Aff1}[7:4], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxx1000000</td>
<td>\texttt{ERRDEVAFF.Aff1}[7:5] is the value of \texttt{MPIDR_EL1.Aff1}[7:5], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bx10000000</td>
<td>\texttt{ERRDEVAFF.Aff1}[7] is the value of \texttt{MPIDR_EL1.Aff1}[7], viewed from the highest Exception level of the associated PEs.</td>
</tr>
</tbody>
</table>

Otherwise:

PE affinity level 1. Indicates whether the PE affinity is at level 2.

<table>
<thead>
<tr>
<th>Aff1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>PE affinity is above level 2 or a subset of level 2.</td>
</tr>
<tr>
<td>0x80</td>
<td>PE affinity is at level 2.</td>
</tr>
</tbody>
</table>

**Aff0, bits [7:0]**

When affine with a PE at affinity level 0:

PE affinity level 0. The \texttt{MPIDR\_EL1.Aff0} field, viewed from the highest Exception level of the associated PE.

When affine with a sub-set of PEs at affinity level 0:

PE affinity level 0. Defines part of the \texttt{MPIDR\_EL1.Aff0} field, viewed from the highest Exception level of the associated PEs.
ERRDEVAFF, Device Affinity Register

<table>
<thead>
<tr>
<th>Aff0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxxxxxxx1</td>
<td>ERRDEVAFF.Aff0[7:1] is the value of MPIDR_EL1.Aff0[7:1], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxxx10</td>
<td>ERRDEVAFF.Aff0[7:2] is the value of MPIDR_EL1.Aff0[7:2], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxxx100</td>
<td>ERRDEVAFF.Aff0[7:3] is the value of MPIDR_EL1.Aff0[7:3], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxxxx1000</td>
<td>ERRDEVAFF.Aff0[7:4] is the value of MPIDR_EL1.Aff0[7:4], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bxx10000</td>
<td>ERRDEVAFF.Aff0[7:5] is the value of MPIDR_EL1.Aff0[7:5], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bx100000</td>
<td>ERRDEVAFF.Aff0[7:6] is the value of MPIDR_EL1.Aff0[7:6], viewed from the highest Exception level of the associated PEs.</td>
</tr>
<tr>
<td>0bx100000</td>
<td>ERRDEVAFF.Aff0[7] is the value of MPIDR_EL1.Aff0[7], viewed from the highest Exception level of the associated PEs.</td>
</tr>
</tbody>
</table>

Otherwise:

PE affinity level 0. Indicates whether the PE affinity is at level 1.

<table>
<thead>
<tr>
<th>Aff0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>PE affinity is above level 1 or a subset of level 1.</td>
</tr>
<tr>
<td>0x80</td>
<td>PE affinity is at level 1.</td>
</tr>
</tbody>
</table>

Accessing the ERRDEVAFF

ERRDEVAFF can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFA8</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERRDEVARCH, Device Architecture Register

The ERRDEVARCH characteristics are:

**Purpose**

Provides discovery information for the component.

**Configuration**

ERRDEVARCH is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRDEVARCH is a 32-bit register.

**Field descriptions**

The ERRDEVARCH bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ARCHITECT</td>
<td>PRESENT</td>
<td>REVISION</td>
<td>ARCHVER</td>
<td>ARCHPART</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ARCHITECT, bits [31:21]**

Architect. Defines the architect of the component. Bits [31:28] are the JEP106 continuation code (JEP106 bank ID, minus 1) and bits [27:21] are the JEP106 ID code.

<table>
<thead>
<tr>
<th>ARCHITECT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01000111011</td>
<td>JEP106 continuation code 0x4, ID code 0x3B. Arm Limited.</td>
</tr>
</tbody>
</table>

Other values are defined by the JEDEC JEP106 standard.

This field reads as 0x23B.

**PRESENT, bit [20]**

DEVARCH Present. Defines that the DEVARCH register is present.

<table>
<thead>
<tr>
<th>PRESENT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Device Architecture information not present.</td>
</tr>
<tr>
<td>0b1</td>
<td>Device Architecture information present.</td>
</tr>
</tbody>
</table>

This bit reads as 0b1.

**REVISION, bits [19:16]**

Revision. Defines the architecture revision of the component.
### REVISION

<table>
<thead>
<tr>
<th>Meaning</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS System Architecture v1.0.</td>
<td>0000</td>
</tr>
</tbody>
</table>
| RAS System Architecture v1.1. As 0b0000 and also:  
  - Simplifies ERR<n>STATUS.  
  - Adds support for additional ERR<n>MISC<m> registers.  
  - Adds support for the optional RAS Timestamp Extension.  
  - Adds support for the optional RAS Common Fault Injection Model Extension. | 0001 |

All other values are reserved.

### ARCHVER, bits [15:12]

Architecture Version. Defines the architecture version of the component.

<table>
<thead>
<tr>
<th>ARCHVER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>RAS System Architecture v1.0</td>
</tr>
</tbody>
</table>

All other values are reserved.

ARCHVER and ARCHPART are also defined as a single field, ARCHID, so that ARCHVER is ARCHID[15:12].

This field reads as 0b0000.

### ARCHPART, bits [11:0]

Architecture Part. Defines the architecture of the component.

<table>
<thead>
<tr>
<th>ARCHPART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xA00</td>
<td>RAS System Architecture.</td>
</tr>
</tbody>
</table>

ARCHVER and ARCHPART are also defined as a single field, ARCHID, so that ARCHPART is ARCHID[11:0].

This field reads as 0xA00.

### Accessing the ERRDEVARCH

**ERRDEVARCH, Device Architecture Register**

**ERRDEVARCH can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFBC</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERRDEVID, Device Configuration Register

The ERRDEVID characteristics are:

**Purpose**

Provides discovery information for the component.

**Configuration**

ERRDEVID is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRDEVID is a 32-bit register.

**Field descriptions**

The ERRDEVID bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>16</td>
<td>NUM</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**NUM, bits [15:0]**

Highest numbered index of the error records in this group, plus one. Each implemented record is owned by a node. A node might own multiple records.

This manual describes a group of error records accessed via a standard 4KB memory-mapped peripheral. For a 4KB peripheral, up to 24 error records can be accessed if the Common Fault Injection Model is implemented, and up to 56 otherwise.

This field reads as an IMPLEMENTATION DEFINED value.

**Accessing the ERRDEVID**

ERRDEVID can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFC8</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERRERICR0, Error Recovery Interrupt Configuration Register 0

The ERRERICR0 characteristics are:

**Purpose**

Error Recovery Interrupt configuration register.

**Configuration**

This register is present only when (the Error Recovery Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRERICR0 are RES0.

ERRERICR0 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRERICR0 is a 64-bit register.

**Field descriptions**

The ERRERICR0 bit assignments are:

**When the Error Recovery Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ADDR | ADDR | RES0 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:56]**

Reserved, RES0.

**ADDR, bits [55:2]**

Message Signaled Interrupt address. (ERRERICR0.ADDR << 2) is the address that the component writes to when signaling the Error Recovery Interrupt. Bits [1:0] of the address are always zero.

The physical address size supported by the component is IMPLEMENTATION DEFINED. Unimplemented high-order physical address bits are RES0.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

**Bits [1:0]**

Reserved, RES0.
When the implementation does not use the recommended layout for the ERRIRQCR\(<n>\) registers:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ![IMPLEMENTATION DEFINED](image1)
| ![IMPLEMENTATION DEFINED](image2) |

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED.

**Accessing the ERRERICR0**

ERRERICR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE90</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRERICR1, Error Recovery Interrupt Configuration Register 1

The ERRERICR1 characteristics are:

**Purpose**

Error Recovery Interrupt configuration register.

**Configuration**

This register is present only when (the Error Recovery Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRERICR1 are RES0.

ERRERICR1 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRERICR1 is a 32-bit register.

**Field descriptions**

The ERRERICR1 bit assignments are:

**When the Error Recovery Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| DATA | DATA, bits [31:0] | Payload for the message signaled interrupt. | On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

**When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
| IMPLEMENTATION DEFINED, bits [31:0] | IMPLEMENTATION DEFINED. |

**Accessing the ERRERICR1**

ERRERICR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE98</td>
</tr>
</tbody>
</table>
Accesses on this interface are **RW**.
ERRERICR2, Error Recovery Interrupt Configuration Register 2

The ERRERICR2 characteristics are:

**Purpose**

Error Recovery Interrupt control and configuration register.

**Configuration**

This register is present only when (the Error Recovery Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRERICR2 are RES0.

ERRERICR2 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRERICR2 is a 32-bit register.

**Field descriptions**

The ERRERICR2 bit assignments are:

### When the Error Recovery Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>IRQEN</td>
</tr>
<tr>
<td>29</td>
<td>NSMSI</td>
</tr>
<tr>
<td>28</td>
<td>SH</td>
</tr>
<tr>
<td>27</td>
<td>MemAttr</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**IRQEN, bit [7]**

When the component supports disabling message signaled interrupts:

Message signaled interrupt enable. Enables generation of message signaled interrupts.

<table>
<thead>
<tr>
<th>IRQEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enabled.</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

Message signaled interrupt enable.

Message signaled interrupts are always enabled.
NSMSI, bit [6]

When the component supports configuring the Security attribute for message signaled interrupts and the component does not allow Non-secure writes to ERRERICR2:

Security attribute. Defines the physical address space for message signaled interrupts.

<table>
<thead>
<tr>
<th>NSMSI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to an IMPLEMENTATION DEFINED value.

When the component allows Non-secure writes to ERRERICR2:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute used for message signaled interrupts is Non-secure.

Otherwise:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute for message signaled interrupts is IMPLEMENTATION DEFINED.

SH, bits [5:4]

When the component supports configuring the Shareability domain:

Shareability. Defines the Shareability domain for message signaled interrupts.

<table>
<thead>
<tr>
<th>SH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Not shared</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is ignored when ERRERICR2.MemAttr specifies any of the following memory types:

- Any Device memory type.
- Normal memory, Inner Non-cacheable, Outer Non-cacheable.

All Device and Normal Inner Non-cacheable Outer Non-cacheable memory regions are always treated as Outer Shareable.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Shareability.

The Shareability domain for message signaled interrupts is IMPLEMENTATION DEFINED.
MemAttr, bits [3:0]

When the component supports configuring the memory type for message signaled interrupts:

Memory type. Defines the memory type and attributes for message signaled interrupts.

<table>
<thead>
<tr>
<th>MemAttr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Device-nGnRE memory.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Device-nGRE memory.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Device-GRE memory.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Normal memory, Inner Non-cacheable, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Normal memory, Inner Write-Through, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Normal memory, Inner Write-Back, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Through.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Normal memory, Inner Write-Through, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Normal memory, Inner Write-Back, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Normal memory, Inner Write-Through, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Normal memory, Inner Write-Back, Outer Write-Back.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

This is the same format as the VMSAv8-64 stage 2 memory region attributes.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Memory type.

The memory type used for message signaled interrupts is IMPLEMENTATION DEFINED.

When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:

Accessing the ERRIRCR2

ERRIRCR2 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE9C</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRFHICR0, Fault Handling Interrupt Configuration Register 0

The ERRFHICR0 characteristics are:

**Purpose**

Fault Handling Interrupt configuration register.

**Configuration**

This register is present only when (the Fault Handling Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRFHICR0 are RES0.

ERRFHICR0 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRFHICR0 is a 64-bit register.

**Field descriptions**

The ERRFHICR0 bit assignments are:

When the Fault Handling Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:56</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>55:2</td>
<td>Message Signaled Interrupt address. (ERRFHICR0.ADDR &lt;&lt; 2) is the address that the component writes to when signaling the Fault Handling Interrupt. Bits [1:0] of the address are always zero. The physical address size supported by the component is IMPLEMENTATION DEFINED. Unimplemented high-order physical address bits are RES0. On an Error recovery reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>1:0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>
When the implementation does not use the recommended layout for the \texttt{ERRIRQCR\textless n\textgreater} registers:

\begin{verbatim}
63  62  61  60  59  58  57  56  55  54  53  52  51  50  49  48  47  46  45  44  43  42  41  40  39  38  37  36  35  34  33  32
  IMPLEMENTATION DEFINED
  IMPLEMENTATION DEFINED
  IMPLEMENTATION DEFINED
  IMPLEMENTATION DEFINED, bits [63:0]

  IMPLEMENTATION DEFINED.

Accessing the \texttt{ERRFHICR0}

\texttt{ERRFHICR0} can be accessed through the memory-mapped interfaces:

\begin{verbatim}
<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE80</td>
</tr>
</tbody>
</table>
\end{verbatim}

Accesses on this interface are \texttt{RW}.

ERRFHICR1, Fault Handling Interrupt Configuration Register 1

The ERRFHICR1 characteristics are:

Purpose

Fault Handling Interrupt configuration register.

Configuration

This register is present only when (the Fault Handling Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRFHICR1 are RES0.

ERRFHICR1 is implemented only as part of a memory-mapped group of error records.

Attributes

ERRFHICR1 is a 32-bit register.

Field descriptions

The ERRFHICR1 bit assignments are:

When the Fault Handling Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

DATA, bits [31:0]

Payload for the message signaled interrupt.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED.

Accessing the ERRFHICR1

ERRFHICR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE88</td>
</tr>
</tbody>
</table>
Accesses on this interface are RW.
ERRFHICR2, Fault Handling Interrupt Configuration Register 2

The ERRFHICR2 characteristics are:

**Purpose**

Fault Handling Interrupt control and configuration register.

**Configuration**

This register is present only when (the Fault Handling Interrupt is implemented or the implementation does not use the recommended layout for the ERRIRQCR<n> registers) and interrupt configuration registers are implemented. Otherwise, direct accesses to ERRFHICR2 are RES0.

ERRFHICR2 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRFHICR2 is a 32-bit register.

**Field descriptions**

The ERRFHICR2 bit assignments are:

When the Fault Handling Interrupt is implemented and the implementation uses the recommended layout for the ERRIRQCR<n> registers:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  |  9  |  8  |  7  |  6  |  5  |  4  |  3  |  2  |  1  |  0  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0 | IRQEN | NSMSI | SH | MemAttr |

**Bits [31:8]**

Reserved, RES0.

**IRQEN, bit [7]**

When the component supports disabling message signaled interrupts:

Message signaled interrupt enable. Enables generation of message signaled interrupts.

<table>
<thead>
<tr>
<th>IRQEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Enabled.</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

Message signaled interrupt enable.

Message signaled interrupts are always enabled.
NSMSI, bit [6]

When the component supports configuring the Security attribute for message signaled interrupts and the component does not allow Non-secure writes to ERRFHICR2:

Security attribute. Defines the physical address space for message signaled interrupts.

<table>
<thead>
<tr>
<th>NSMSI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure.</td>
</tr>
</tbody>
</table>

On an Error recovery reset, this field resets to an IMPLEMENTATION DEFINED value.

When the component allows Non-secure writes to ERRFHICR2:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute used for message signaled interrupts is Non-secure.

Otherwise:

Reserved, RES0.

Security attribute. Defines the physical address space for message signaled interrupts.

The Security attribute for message signaled interrupts is IMPLEMENTATION DEFINED.

SH, bits [5:4]

When the component supports configuring the Shareability domain:

Shareability. Defines the Shareability domain for message signaled interrupts.

<table>
<thead>
<tr>
<th>SH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Not shared.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Inner Shareable.</td>
</tr>
</tbody>
</table>

All other values are reserved.

This field is ignored when ERRFHICR2.MemAttr specifies any of the following memory types:

- Any Device memory type.
- Normal memory, Inner Non-cacheable, Outer Non-cacheable.

All Device and Normal Inner Non-cacheable Outer Non-cacheable memory regions are always treated as Outer Shareable.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Shareability.

The Shareability domain for message signaled interrupts is IMPLEMENTATION DEFINED.
MemAttr, bits [3:0]

When the component supports configuring the memory type for message signaled interrupts:

Memory type. Defines the memory type and attributes for message signaled interrupts.

<table>
<thead>
<tr>
<th>MemAttr</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Device-nGnRnE memory.</td>
</tr>
<tr>
<td>0b0001</td>
<td>Device-nGnRE memory.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Device-nGRE memory.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Device-GRE memory.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Normal memory, Inner Non-cacheable, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Normal memory, Inner Write-Through, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Normal memory, Inner Write-Back, Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Normal memory, Inner Write-Through, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Normal memory, Inner Write-Back, Outer Write-Through.</td>
</tr>
<tr>
<td>0b1101</td>
<td>Normal memory, Inner Non-cacheable, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Normal memory, Inner Write-Through, Outer Write-Back.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Normal memory, Inner Write-Back, Outer Write-Back.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

This is the same format as the VMSA v8-64 stage 2 memory region attributes.

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

Memory type.

The memory type used for message signaled interrupts is IMPLEMENTATION DEFINED.

When the implementation does not use the recommended layout for the ERRIRQCR<n> registers:

<table>
<thead>
<tr>
<th>Offset</th>
<th>IMPLEMENTATION DEFINED</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xE8C</td>
<td></td>
</tr>
</tbody>
</table>

Accessing the ERRFHIRCR2

ERRFHIRCR2 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE8C</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The ERRGSR characteristics are:

**Purpose**

Shows the status for the records in the group.

**Configuration**

ERRGSR is implemented only as part of a memory-mapped group of error records.

This manual describes a group of error records accessed via a standard 4KB memory-mapped peripheral. For a 4KB peripheral, up to 24 error records can be accessed if the Common Fault Injection Model is implemented, and up to 56 otherwise.

**Attributes**

ERRGSR is a 64-bit register.

**Field descriptions**

The ERRGSR bit assignments are:

<table>
<thead>
<tr>
<th>Bits [63:56]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>S&lt;m&gt;</strong>, bit [m], for m = 55 to 0</td>
<td>When error record &lt;m&gt; is implemented and error record &lt;m&gt; supports this type of reporting:</td>
</tr>
<tr>
<td>The status for error record &lt;m&gt;. A read-only copy of ERR&lt;m&gt;STATUS.V.</td>
<td></td>
</tr>
<tr>
<td><strong>S&lt;m&gt;</strong></td>
<td>Meaning</td>
</tr>
<tr>
<td>0b0</td>
<td>No error.</td>
</tr>
<tr>
<td>0b1</td>
<td>One or more errors.</td>
</tr>
</tbody>
</table>

If the Common Fault Injection Model is implemented, up-to 24 records can be implemented meaning bits [55:24] are RES0.

**Otherwise:**

Reserved, RES0.

**Accessing the ERRGSR**

ERRGSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Accesses on this interface are RO.
ERRIIDR, Implementation Identification Register

The ERRIIDR characteristics are:

**Purpose**

Defines the implementer of the component.

**Configuration**

Implementation of this register is **OPTIONAL**.

This register is present only when RAS System Architecture v1.1 is implemented.

**Attributes**

ERRIIDR is a 32-bit register.

**Field descriptions**

The ERRIIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ProductID</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
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<tr>
<td>24</td>
<td></td>
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<tr>
<td>23</td>
<td></td>
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<tr>
<td>22</td>
<td></td>
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<tr>
<td>21</td>
<td></td>
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<td>20</td>
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<td>19</td>
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<td>18</td>
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<td>17</td>
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<tr>
<td>16</td>
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<tr>
<td>15</td>
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<tr>
<td>14</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
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<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
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<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
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<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Implementer</td>
</tr>
</tbody>
</table>

**ProductID, bits [31:20]**

Part number, bits [11:0]. The part number is selected by the designer of the component.

If ERRIIDR0 and ERRIIDR1 are implemented, ERRIIDR0.PART_0 matches bits [7:0] of ERRIIDR.ProductID and ERRIIDR1.PART_1 matches bits [11:8] of ERRIIDR.ProductID.

**Variant, bits [19:16]**

Component major revision.

This field distinguishes product variants or major revisions of the product.

If ERRIIDR2 is implemented, ERRIIDR2.REVISION matches ERRIIDR.Variant.

**Revision, bits [15:12]**

Component minor revision.

This field distinguishes minor revisions of the product.

If ERRIIDR3 is implemented, ERRIIDR3.REVAND matches ERRIIDR.Revision.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the RAS component. For an Arm implementation, this field has the value 0x43B.

Bits [11:8] contain the JEP106 continuation code of the implementer, and bits [6:0] contain the JEP106 identity code of the implementer. Bit 7 is RES0.
If \texttt{ERRPIDR4} is implemented, \texttt{ERRPIDR2} is implemented, and \texttt{ERRPIDR1} is implemented, \texttt{ERRPIDR4.DE5_2} matches bits [11:8] of \texttt{ERRIIDR}\texttt{.Implementer}, \texttt{ERRPIDR2.DE5_1} matches bits [6:4] of \texttt{ERRIIDR}\texttt{.Implementer}, and \texttt{ERRPIDR1.DE5_0} matches bits [3:0] of \texttt{ERRIIDR}\texttt{.Implementer}.

### Accessing the ERRIIDR


erriidr can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE10</td>
</tr>
</tbody>
</table>

Accesses on this interface are \texttt{RO}.
ERRIMPDEF<n>, IMPLEMENTATION DEFINED Register <n>, n = 0 - 191

The ERRIMPDEF<n> characteristics are:

**Purpose**

IMPLEMENTATION DEFINED RAS extensions.

**Configuration**

This register is present only when the RAS Common Fault Injection Model Extension is not implemented, ERRDEVID.NUM <= 32 and an implementation implements ERRIMPDEF<n>. Otherwise, direct accesses to ERRIMPDEF<n> are RES0.

**Attributes**

ERRIMPDEF<n> is a 64-bit register.

**Field descriptions**

The ERRIMPDEF<n> bit assignments are:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
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<th>47</th>
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<th>45</th>
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<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td><strong>IMPLEMENTATION DEFINED</strong></td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

**IMPLEMENTATION DEFINED.**

**Accessing the ERRIMPDEF<n>**

ERRIMPDEF<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x800 + (8 * n)</td>
<td>ERRIMPDEF&lt;n&gt;</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRIRQCR\(<n>\), Generic Error Interrupt Configuration Register, n = 0 - 15

The ERRIRQCR\(<n>\) characteristics are:

**Purpose**

The ERRIRQCR\(<n>\) registers are reserved for IMPLEMENTATION DEFINED interrupt configuration registers.

The architecture provides a recommended layout for the ERRIRQCR\(<n>\) registers. These registers are named:

- **ERRFHIRC0**, **ERRFHIRC1**, and **ERRFHIRC2** for the fault handling interrupt controls.
- **ERRERICR0**, **ERRERICR1**, and **ERRERICR2** for the error recovery interrupt controls.
- **ERRCIRC0**, **ERRCIRC1**, and **ERRCIRC2** for the critical error interrupt controls.
- **ERRROS** for the status register.

This section describes the generic, IMPLEMENTATION DEFINED, format.

**Configuration**

This register is present only when the interrupt configuration registers are implemented. Otherwise, direct accesses to ERRIRQCR\(<n>\) are RES0.

ERRIRQCR\(<n>\) is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRIRQCR\(<n>\) is a 64-bit register.

**Field descriptions**

The ERRIRQCR\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

IMPLEMENTATION DEFINED controls. The content of these registers is IMPLEMENTATION DEFINED.

**Accessing the ERRIRQCR\(<n>\)**

ERRIRQCR\(<n>\) can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xE80  + (8 * (&lt;n&gt;))</td>
<td>ERRIRQCR(&lt;n&gt;)</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRIRQSR, Error Interrupt Status Register

The ERRIRQSR characteristics are:

**Purpose**

Interrupt status register.

**Configuration**

This register is present only when interrupt configuration registers are implemented. Otherwise, direct accesses to ERRIRQSR are read-only.

ERRIRQSR is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRIRQSR is a 64-bit register.

**Field descriptions**

The ERRIRQSR bit assignments are:

**When the implementation uses the recommended layout for the ERRIRQCR<n> registers:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | CRIERR | CRIERR | ERIERR | ERIERR |

Bits [63:6]

Reserved, RES0.

**CRIERR, bit [5]**

**When the Critical Error Interrupt is implemented:**

Critical Error Interrupt error.

<table>
<thead>
<tr>
<th>CRIERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Critical Error Interrupt write has not returned an error since this bit was last cleared to zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Critical Error Interrupt write has returned an error since this bit was last cleared to zero.</td>
</tr>
</tbody>
</table>

This bit is read/write-one-to-clear.

On an Error recovery reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**CRI, bit [4]**
When the **Critical Error Interrupt** is implemented:

Critical Error Interrupt write in progress.

<table>
<thead>
<tr>
<th>CRI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Critical Error Interrupt write not in progress.</td>
</tr>
<tr>
<td>0b1</td>
<td>Critical Error Interrupt write in progress.</td>
</tr>
</tbody>
</table>

Software must not disable an interrupt whilst the write is in progress.

**Note**

This bit does not indicate whether an interrupt is active, but rather whether a write triggered by the interrupt is in progress.

To determine whether an interrupt is active, software must examine the individual **ERR<n>STATUS** registers.

Access to this field is RO.

**Otherwise:**

Reserved, RES0.

**ERIERR, bit [3]**

When the **Error Recovery Interrupt** is implemented:

Error Recovery Interrupt error.

<table>
<thead>
<tr>
<th>ERIERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error Recovery Interrupt write has not returned an error since this bit was last cleared to zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error Recovery Interrupt write has returned an error since this bit was last cleared to zero.</td>
</tr>
</tbody>
</table>

This bit is read/write-one-to-clear.

On an Error recovery reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, RES0.

**ERI, bit [2]**

When the **Error Recovery Interrupt** is implemented:

Error Recovery Interrupt write in progress.

<table>
<thead>
<tr>
<th>ERI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error Recovery Interrupt write not in progress.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error Recovery Interrupt write in progress.</td>
</tr>
</tbody>
</table>

Software must not disable an interrupt whilst the write is in progress.

**Note**

This bit does not indicate whether an interrupt is active, but rather whether a write triggered by the interrupt is in progress.
To determine whether an interrupt is active, software must examine the individual `ERR<n>STATUS` registers.

Access to this field is RO.

Otherwise:

Reserved, RES0.

**FHIERR, bit [1]**

When the Fault Handling Interrupt is implemented:

Fault Handling Interrupt error.

<table>
<thead>
<tr>
<th>FHIERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault Handling Interrupt write has not returned an error since this bit was last cleared to zero.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault Handling Interrupt write has returned an error since this bit was last cleared to zero.</td>
</tr>
</tbody>
</table>

This bit is read/write-one-to-clear:

On an Error recovery reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**FHI, bit [0]**

When the Fault Handling Interrupt is implemented:

Fault Handling Interrupt write in progress.

<table>
<thead>
<tr>
<th>FHI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault Handling Interrupt write not in progress.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault Handling Interrupt write in progress.</td>
</tr>
</tbody>
</table>

Software must not disable an interrupt whilst the write is in progress.

**Note**

This bit does not indicate whether an interrupt is active, but rather whether a write triggered by the interrupt is in progress.

To determine whether an interrupt is active, software must examine the individual `ERR<n>STATUS` registers.

Access to this field is RO.

Otherwise:

Reserved, RES0.
When the implementation does not use the recommended layout for the ERRIRQ<Cr> registers:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>61</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>59</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>58</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>57</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>56</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>55</td>
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<td>54</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>IMPLEMENTATION DEFINED</td>
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<td>52</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>51</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>50</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>IMPLEMENTATION DEFINED</td>
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<td>42</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>41</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>IMPLEMENTATION DEFINED</td>
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<td>36</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>35</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>34</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>33</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>32</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>29</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>28</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>27</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>26</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>25</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>24</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>23</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>22</td>
<td>IMPLEMENTATION DEFINED</td>
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<td>21</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>20</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>19</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>18</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>17</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>16</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>15</td>
<td>IMPLEMENTATION DEFINED</td>
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<tr>
<td>14</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>13</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>12</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>11</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>10</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>9</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>8</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>7</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>6</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>5</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>4</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>3</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>2</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>1</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:0]**

**Accessing the ERRIRQSR**

ERRIRQSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xEF8</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
**ERR<n>ADDR, Error Record Address Register, n = 0 - 65534**

The ERR<n>ADDR characteristics are:

**Purpose**

If an address is associated with a detected error, then it is written to ERR<n>ADDR when the error is recorded. It is *IMPLEMENTATION DEFINED* how the recorded address maps to the software-visible physical address. Software might have to reconstruct the actual physical addresses using the identity of the node and knowledge of the system.

**Configuration**

This register is present only when error record <n> is implemented and error record <n> includes an address associated with an error. Otherwise, direct accesses to ERR<n>ADDR are *RES0*.

ERR<q>FR describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record, then q = n.

**Attributes**

ERR<n>ADDR is a 64-bit register.

**Field descriptions**

The ERR<n>ADDR bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>NS</td>
<td>63</td>
<td>Non-secure attribute.</td>
</tr>
<tr>
<td>SI</td>
<td>62</td>
<td>Secure Incorrect.</td>
</tr>
<tr>
<td>AI</td>
<td>61</td>
<td>Actual Incorrect.</td>
</tr>
<tr>
<td>VA</td>
<td>60</td>
<td>Virtual Address.</td>
</tr>
<tr>
<td>RES0</td>
<td>59</td>
<td>Reserved.</td>
</tr>
<tr>
<td>PADDR</td>
<td>58</td>
<td>Physical Address.</td>
</tr>
</tbody>
</table>

**NS, bit [63]**

Non-secure attribute.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;ADDR.PADDR is a Secure address.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;ADDR.PADDR is a Non-secure address.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally *UNKNOWN* value.

**SI, bit [62]**

Secure Incorrect. Indicates whether ERR<n>ADDR.NS is valid.

<table>
<thead>
<tr>
<th>SI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;ADDR.NS is correct. That is, it matches the programmers’ view of the Non-secure attribute for this recorded location.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;ADDR.NS might not be correct, and might not match the programmers’ view of the Non-secure attribute for the recorded location.</td>
</tr>
</tbody>
</table>

It is *IMPLEMENTATION DEFINED* whether this bit is read-only or read/write.

On a Cold reset, this field resets to an architecturally *UNKNOWN* value.
AI, bit [61]

Address Incorrect. Indicates whether ERR<n>ADDR.PADDR is a valid physical address that is known to match the programmers’ view of the physical address for the recorded location.

<table>
<thead>
<tr>
<th>AI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;ADDR.PADDR is a valid physical address. That is, it matches the programmers' view of the physical address for the recorded location.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;ADDR.PADDR might not be a valid physical address, and might not match the programmers' view of the physical address for the recorded location.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this bit is read-only or read/write.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

VA, bit [60]

Virtual Address. Indicates whether ERR<n>ADDR.PADDR field is a virtual address.

<table>
<thead>
<tr>
<th>VA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;ADDR.PADDR is not a virtual address.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;ADDR.PADDR is a virtual address.</td>
</tr>
</tbody>
</table>

No context information is provided for the virtual address. When ERR<n>ADDR.VA == 0b1, ERR<n>ADDR.{NS,SI,VI} read as {0,1,1}.

Support for this bit is optional. If this bit is not implemented and ERR<n>ADDR.PADDR field is a virtual address, then ERR<n>ADDR.{NS,SI,VI} read as {0,1,1}.

It is IMPLEMENTATION DEFINED whether this bit is read-only or read/write.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Bits [59:56]

Reserved, RES0.

PADDR, bits [55:0]

Physical Address. Address of the recorded location. If the physical address size implemented by this component is smaller than the size of this field, then high-order bits are unimplemented and either RES0 or have a fixed read-only IMPLEMENTATION DEFINED value. Low-order address bits might also be unimplemented and RES0, for example, if the physical address is always aligned to the size of a protection granule.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Accessing the ERR<n>ADDR

ERR<n>ADDR ignores writes if all of the following are true:

- Any of the following are true:
  - The RAS Common Fault Injection Model Extension is implemented by the node that owns this error record and ERR<q>PFGF.AV == 0b0.
  - The RAS Common Fault Injection Model Extension is not implemented by the node that owns this error record.
  - ERR<n>STATUS.AV == 0b1.

ERR<n>ADDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x018 + (64 * n)</td>
<td>ERR&lt;n&gt;ADDR</td>
</tr>
</tbody>
</table>
Accesses on this interface are **RW**.
The ERR<n>CTRL characteristics are:

**Purpose**

The error control register contains enable bits for the node that writes to this record:

- Enabling error detection and correction.
- Enabling the critical error, error recovery, and fault handling interrupts.
- Enabling in-band error response for Uncorrected errors.

For each bit, if the node does not support the feature, then the bit is RES0. The definition of each record is IMPLEMENTATION DEFINED.

**Configuration**

This register is present only when error record <n> is implemented and error record <n> is the first error record owned by a node. Otherwise, direct accesses to ERR<n>CTRL are RES0.

ERR<n>FR describes the features implemented by the node.

**Attributes**

ERR<n>CTRL is a 64-bit register.

**Field descriptions**

The ERR<n>CTRL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>RESERVED</td>
</tr>
<tr>
<td>61</td>
<td>CI</td>
</tr>
<tr>
<td>60</td>
<td>RES0</td>
</tr>
<tr>
<td>59</td>
<td>WUI</td>
</tr>
<tr>
<td>58</td>
<td>WUI</td>
</tr>
<tr>
<td>57</td>
<td>WCF</td>
</tr>
<tr>
<td>56</td>
<td>Bit[10]</td>
</tr>
<tr>
<td>55</td>
<td>Bit[9]</td>
</tr>
<tr>
<td>54</td>
<td>Bit[8]</td>
</tr>
<tr>
<td>53</td>
<td>Bit[7]</td>
</tr>
<tr>
<td>52</td>
<td>Bit[6]</td>
</tr>
<tr>
<td>51</td>
<td>Bit[5]</td>
</tr>
<tr>
<td>50</td>
<td>Bit[4]</td>
</tr>
<tr>
<td>49</td>
<td>Bit[3]</td>
</tr>
<tr>
<td>48</td>
<td>Bit[2]</td>
</tr>
<tr>
<td>47</td>
<td>Bit[1]</td>
</tr>
<tr>
<td>46</td>
<td>Bit[0]</td>
</tr>
<tr>
<td>45</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:32]**

Reserved for IMPLEMENTATION DEFINED controls. Must permit SBZP write policy for software.

**Bits [31:14]**

Reserved, RES0.

**CI, bit [13]**

When ERR<n>FR.CI == 0b10:

Critical error interrupt enable. When enabled, the critical error interrupt is generated for a critical error condition.

<table>
<thead>
<tr>
<th>CI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Critical error interrupt not generated for critical errors. Critical errors are treated as Uncontained errors.</td>
</tr>
<tr>
<td>0b1</td>
<td>Critical error interrupt generated for critical errors.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.
Otherwise:
Reserved, RES0.

Bit [12]
Reserved, RES0.

**WDUI, bit [11]**

**When ERR<n>FR.DUI == 0b11:**

Error recovery interrupt for deferred errors on writes enable.

When enabled, the error recovery interrupt is generated for detected Deferred errors on writes.

<table>
<thead>
<tr>
<th><strong>WDUI</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt not generated for deferred errors on writes.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt generated for deferred errors on writes.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:
Reserved, RES0.

**DUI, bit [10]**

**When ERR<n>FR.DUI == 0b10:**

Error recovery interrupt for deferred errors enable.

When ERR<n>FR.DUI == 0b10, this control applies to errors arising from both reads and writes.

When enabled, the error recovery interrupt is generated for all detected Deferred errors.

<table>
<thead>
<tr>
<th><strong>DUI</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt not generated for deferred errors.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt generated for deferred errors.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**When ERR<n>FR.DUI == 0b11:**

Error recovery interrupt for deferred errors on reads enable.

When ERR<n>FR.DUI == 0b11, this bit is named RDUI.

When enabled, the error recovery interrupt is generated for detected Deferred errors on reads.

<table>
<thead>
<tr>
<th><strong>RDUI</strong></th>
<th><strong>Meaning</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt not generated for deferred errors on reads.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt generated for deferred errors on reads.</td>
</tr>
</tbody>
</table>
The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**WCFI, bit [9]**

*When ERR<n>FR.CFI == 0b11:*

Fault handling interrupt for Corrected errors on writes enable.

When enabled:

- If the node implements Corrected error counters for writes, then the fault handling interrupt is generated when a counter overflows and the overflow bit for the counter is set to 0b1. For more information, see ERR<n>MISC0.
- Otherwise, the fault handling interrupt is also generated for detected Corrected errors on writes.

<table>
<thead>
<tr>
<th>WCFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt not generated for Corrected errors on writes.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt generated for Corrected errors on writes.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**CFI, bit [8]**

*When ERR<n>FR.CFI == 0b10:*

Fault handling interrupt for Corrected errors enable.

When ERR<n>FR.CFI == 0b10, this control applies to errors arising from both reads and writes.

When enabled:

- If the node implements Corrected error counters, then the fault handling interrupt is generated when a counter overflows and the overflow bit for the counter is set to 0b1. For more information, see ERR<n>MISC0.
- Otherwise, the fault handling interrupt is also generated for all detected Corrected errors.

<table>
<thead>
<tr>
<th>CFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt not generated for Corrected errors.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt generated for Corrected errors.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

*When ERR<n>FR.CFI == 0b11:*

Fault handling interrupt for Corrected errors on reads enable.

When ERR<n>FR.CFI == 0b11, this bit is named RCFI.
When enabled:

- If the node implements Corrected error counters for reads, then the fault handling interrupt is generated when a counter overflows and the overflow bit for the counter is set to 0b1. For more information, see ERR<n>MISC0.
- Otherwise, the fault handling interrupt is also generated for detected Corrected errors on reads.

<table>
<thead>
<tr>
<th>RCFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt not generated for Corrected errors on reads.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt generated for Corrected errors on reads.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**WUE, bit [7]**

When ERR<n>FR.UE == 0b11:

In-band Uncorrected error reporting on writes enable.

When enabled, responses to writes that detect an Uncorrected error that cannot be deferred are signaled in-band as a detected Uncorrected error (External Abort).

<table>
<thead>
<tr>
<th>WUE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Abort response for Uncorrected errors on writes disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Abort response for Uncorrected errors on writes enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:

Reserved, RES0.

**WFI, bit [6]**

When ERR<n>FR.FI == 0b11:

Fault handling interrupt on writes enable.

When enabled:

- The fault handling interrupt is generated for detected Deferred errors and Uncorrected errors.
- If the corresponding fault handling interrupt for Corrected errors control is not implemented:
  - If the node implements Corrected error counters for writes, then the fault handling interrupt is also generated when a counter overflows and the overflow bit for the counter is set to 0b1.
  - Otherwise, the fault handling interrupt is also generated for detected Corrected errors on writes.

<table>
<thead>
<tr>
<th>WFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt on writes disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt on writes enabled.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.
Otherwise:
Reserved, RES0.

**WUI, bit [5]**

When ERR\(n>FR.UI = 0b11\):

Uncorrected error recovery interrupt on writes enable.

When enabled, the error recovery interrupt is generated for detected Uncorrected errors on writes that are not deferred.

<table>
<thead>
<tr>
<th>WUI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt on writes disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt on writes enabled.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.

**UE, bit [4]**

When ERR\(n>FR.UE = 0b10\):

In-band Uncorrected error reporting enable.

When ERR\(n>FR.UE = 0b10\), this control applies to errors arising from both reads and writes.

When enabled, responses to transactions that detect an Uncorrected error that cannot be deferred are signaled in-band as a detected Uncorrected error (External Abort).

<table>
<thead>
<tr>
<th>UE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Abort response for Uncorrected errors disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Abort response for Uncorrected errors enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

When ERR\(n>FR.UE = 0b11\):

In-band Uncorrected error reporting on reads enable.

When ERR\(n>FR.UE = 0b11\), this bit is named RUE.

When enabled, responses to reads that detect an Uncorrected error that cannot be deferred are signaled in-band as a detected Uncorrected error (External Abort).

<table>
<thead>
<tr>
<th>RUE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>External Abort response for Uncorrected errors on reads disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>External Abort response for Uncorrected errors on reads enabled.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Otherwise:
Reserved, RES0.
**FI, bit [3]**

When \( \text{ERR}_n^{<}\text{FR}.\text{FI} == 0b10 \):

Fault handling interrupt enable.

When \( \text{ERR}_n^{<}\text{FR}.\text{FI} == 0b10 \), this control applies to errors arising from both reads and writes.

When enabled:

- The fault handling interrupt is generated for all detected Deferred errors and Uncorrected errors.
- If the fault handling interrupt for Corrected errors control is not implemented:
  - If the node implements Corrected error counters, then the fault handling interrupt is also generated when a counter overflows and the overflow bit for the counter is set to 0b1.
  - Otherwise, the fault handling interrupt is also generated for all detected Corrected errors.

<table>
<thead>
<tr>
<th>FI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt enabled.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

When \( \text{ERR}_n^{<}\text{FR}.\text{FI} == 0b11 \):

Fault handling interrupt on reads enable.

When \( \text{ERR}_n^{<}\text{FR}.\text{FI} == 0b11 \), this bit is named RFI.

When enabled:

- The fault handling interrupt is generated for detected Deferred errors and Uncorrected errors.
- If the corresponding fault handling interrupt for Corrected errors control is not implemented:
  - If the node implements Corrected error counters for reads, then the fault handling interrupt is also generated when a counter overflows and the overflow bit for the counter is set to 0b1.
  - Otherwise, the fault handling interrupt is also generated for detected Corrected errors on reads.

<table>
<thead>
<tr>
<th>RFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Fault handling interrupt on reads disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Fault handling interrupt on reads enabled.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES0**.

**UI, bit [2]**

When \( \text{ERR}_n^{<}\text{FR}.\text{UI} == 0b10 \):

Uncorrected error recovery interrupt enable.

When \( \text{ERR}_n^{<}\text{FR}.\text{UI} == 0b10 \), this control applies to errors arising from both reads and writes.

When enabled, the error recovery interrupt is generated for all detected Uncorrected errors that are not deferred.

<table>
<thead>
<tr>
<th>UI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt enabled.</td>
</tr>
</tbody>
</table>
The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**When ERR<n>FR.UI == 0b11:**

Uncorrected error recovery interrupt on reads enable.

When ERR<n>FR.UI == 0b11, this bit is named RUI.

When enabled, the error recovery interrupt is generated for detected Uncorrected errors on reads that are not deferred.

<table>
<thead>
<tr>
<th>RUI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error recovery interrupt on reads disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error recovery interrupt on reads enabled.</td>
</tr>
</tbody>
</table>

The interrupt is generated even if the error syndrome is discarded because the error record already records a higher priority error.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES\(0\).

**IMPLEMENTATION DEFINED, bit [1]**

Reserved for IMPLEMENTATION DEFINED controls. Must permit SBZP write policy for software.

**ED, bit [0]**

**When ERR<n>FR.ED == 0b10:**

Error reporting and logging enable. When disabled, the node behaves as if error detection and correction are disabled, and no errors are recorded or signaled by the node. Arm recommends that, when disabled, correct error detection and correction codes are written for writes, unless disabled by an IMPLEMENTATION DEFINED control for error injection.

<table>
<thead>
<tr>
<th>ED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Error reporting disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Error reporting enabled.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether the node fully disables error detection and correction when reporting is disabled. That is, even with error reporting disabled, the node might continue to silently correct errors. Uncorrectable errors might result in corrupt data being silently propagated by the node.

**Note**

If this node requires initialization after Cold reset to prevent signaling false errors, then Arm recommends this bit is set to 0b0 on Cold reset, meaning errors are not reported from Cold reset. This allows boot software to initialize a node without signaling errors. Software can enable error reporting after the node is initialized. Otherwise, the Cold reset value is IMPLEMENTATION DEFINED. If the Cold reset value is 0b1, the reset values of other controls in this register are also IMPLEMENTATION DEFINED and should not be UNKNOWN.

On a Cold reset, this field resets to an IMPLEMENTATION DEFINED value.

**Otherwise:**

Reserved, RES\(0\).
Accessing the ERR\text{n}\text{CTRL}

ERR\text{n}\text{CTRL} can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x008 + (64 * n)</td>
<td>ERR\text{n}\text{CTRL}</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERR<n>FR, Error Record Feature Register, n = 0 - 65534

The ERR<n>FR characteristics are:

**Purpose**

Defines whether <n> is the first record owned by a node:

- If <n> is the first error record owned by a node, then ERR<n>FR.ED != 0b00.
- If <n> is not the first error record owned by a node, then ERR<n>FR.ED == 0b00.

If <n> is the first record owned by the node, defines which of the common architecturally-defined features are implemented by the node and, of the implemented features, which are software programmable.

**Configuration**

This register is present only when error record <n> is implemented. Otherwise, direct accesses to ERR<n>FR are RES0.

**Attributes**

ERR<n>FR is a 64-bit register.

**Field descriptions**

The ERR<n>FR bit assignments are:

When ERR<n>FR.ED != 0b00:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>62</td>
<td>CE</td>
</tr>
<tr>
<td>61</td>
<td>DEEOQERUEUCUUC</td>
</tr>
<tr>
<td>54</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>53</td>
<td>FRX</td>
</tr>
<tr>
<td>52</td>
<td>RES0</td>
</tr>
<tr>
<td>51</td>
<td>TS</td>
</tr>
<tr>
<td>50</td>
<td>CI</td>
</tr>
<tr>
<td>49</td>
<td>INJ</td>
</tr>
<tr>
<td>48</td>
<td>CEO</td>
</tr>
<tr>
<td>47</td>
<td>DUI</td>
</tr>
<tr>
<td>46</td>
<td>RP</td>
</tr>
<tr>
<td>45</td>
<td>CEC</td>
</tr>
<tr>
<td>44</td>
<td>CFI</td>
</tr>
<tr>
<td>43</td>
<td>UE</td>
</tr>
<tr>
<td>42</td>
<td>F1</td>
</tr>
<tr>
<td>41</td>
<td>UI</td>
</tr>
<tr>
<td>35</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>34</td>
<td>33</td>
</tr>
<tr>
<td>32</td>
<td>31</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:55]**

When ERR<n>FR.FRX != 1:

Reserved for identifying IMPLEMENTATION DEFINED controls.

Otherwise:

Reserved, RES0.

**CE, bits [54:53]**

When ERR<n>FR.FRX == 1:

Corrected Error recording. Describes the types of Corrected Error the node can record.
CE

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The node does not record any type of Corrected Error.</td>
</tr>
<tr>
<td>0b01</td>
<td>The node can record transient or persistent Corrected Errors (Corrected Errors that are recorded as ERROR.STATUS.CE == 0b01 and 0b11).</td>
</tr>
<tr>
<td>0b10</td>
<td>The node can record of a non-specific Corrected Error (a Corrected Error that is recorded as ERROR.STATUS.CE == 0b10).</td>
</tr>
<tr>
<td>0b11</td>
<td>The node can record any type of Corrected Error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.

DE, bit [52]

When ERROR.FR.FR.X == 1:

Deferred Error recording. Describes whether the node can record this type of error.

<table>
<thead>
<tr>
<th>DE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not record this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The node can record this type of error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.

UEO, bit [51]

When ERROR.FR.FR.X == 1:

Latent or Restartable Error recording. Describes whether the node can record this type of error.

<table>
<thead>
<tr>
<th>UEO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not record this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The node can record this type of error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.

UER, bit [50]

When ERROR.FR.FR.X == 1:

Signaled or Recoverable Error recording. Describes whether the node can record this type of error.

<table>
<thead>
<tr>
<th>UER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not record this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The node can record this type of error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.
UEU, bit [49]

When ERR<n>FR.FR ± 1:

Unrecoverable Error recording. Describes whether the node can record this type of error.

<table>
<thead>
<tr>
<th>UEU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not record this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The node can record this type of error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.

UC, bit [48]

When ERR<n>FR.FR ± 1:

Uncontainable Error recording. Describes whether the node can record this type of error.

<table>
<thead>
<tr>
<th>UC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not record this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The node can record this type of error.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved for identifying IMPLEMENTATION DEFINED controls.

IMPLEMENTATION DEFINED, bits [47:32]

Reserved for identifying IMPLEMENTATION DEFINED controls.

FRX, bit [31]

When RAS System Architecture v1.1 is implemented:

Feature Register extension. Defines whether ERR<n>FR[63:48] are architecturally defined.

<table>
<thead>
<tr>
<th>FRX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;FR[63:48] are IMPLEMENTATION DEFINED.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;FR[63:48] are defined by the architecture.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

Bits [30:26]

Reserved, RES0.

TS, bits [25:24]

Timestamp Extension. Indicates whether, for each error record <m> owned by this node, ERR<m>MISC3 is used as the timestamp register, and, if it is, the timebase used by the timestamp.
The node does not support a timestamp register.

The node implements a timestamp register. The timestamp uses the same timebase as the system Generic Timer.

Note
For an error record which has an affinity to a PE, this is the same timer that is visible through `CNTPCT_EL0` at the highest Exception level on that PE.

The node implements a timestamp register. The timebase for the timestamp is IMPLEMENTATION DEFINED.

All other values are reserved.

**CI, bits [23:22]**

Critical error interrupt. Indicates whether the critical error interrupt and associated controls are implemented.

<table>
<thead>
<tr>
<th>CI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the critical error interrupt. ERR&lt;n&gt;CTLR CI is RES0.</td>
</tr>
<tr>
<td>0b01</td>
<td>Critical error interrupt is supported and always enabled. ERR&lt;n&gt;CTLR CI is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Critical error interrupt is supported and controllable using ERR&lt;n&gt;CTLR CI.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**INJ, bits [21:20]**

Fault Injection Extension. Indicates whether the RAS Common Fault Injection Model Extension is implemented.

<table>
<thead>
<tr>
<th>INJ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>The node does not support the RAS Common Fault Injection Model Extension.</td>
</tr>
<tr>
<td>0b01</td>
<td>The node implements the RAS Common Fault Injection Model Extension. See ERR&lt;n&gt;PFGF for more information.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**CEO, bits [19:18]**

When ERR<n>FR.CEC != 0b000:

Corrected Error overwrite. Indicates the behavior when a second Corrected error is detected after a first Corrected error has been recorded by an error record <m> owned by the node.

<table>
<thead>
<tr>
<th>CEO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Counts Corrected errors if a counter is implemented. Keeps the previous error syndrome. If the counter overflows, or no counter is implemented, then ERR&lt;m&gt;STATUS.OF is set to 0b1.</td>
</tr>
<tr>
<td>0b01</td>
<td>Counts Corrected errors. If ERR&lt;m&gt;STATUS.OF == 0b1 before the Corrected error is counted, then keeps the previous syndrome. Otherwise the previous syndrome is overwritten. If the counter overflows, then ERR&lt;m&gt;STATUS.OF is set to 0b1.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Otherwise:

Reserved, RES0.

**DUI, bits [17:16]**
When \( \text{ERR}<n>\text{FR.UI} \neq \text{0b00} \):

Error recovery interrupt for deferred errors control. Indicates whether the control for enabling error recovery interrupts on deferred errors are implemented.

<table>
<thead>
<tr>
<th>DUI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the control for enabling error recovery interrupts on deferred errors. ( \text{ERR}&lt;n&gt;\text{CTRL}.\text{DUI} ) is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Control for enabling error recovery interrupts on deferred errors is supported and controllable using ( \text{ERR}&lt;n&gt;\text{CTRL}.\text{DUI} ).</td>
</tr>
<tr>
<td>0b11</td>
<td>Control for enabling error recovery interrupts on deferred errors is supported and controllable using ( \text{ERR}&lt;n&gt;\text{CTRL}.\text{WDUI} ) for writes and ( \text{ERR}&lt;n&gt;\text{CTRL}.\text{RDUI} ) for reads.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Otherwise:

Reserved, RES0.

RP, bit [15]

When \( \text{ERR}<n>\text{FR.CEC} \neq \text{0b000} \):

Repeat counter. Indicates whether the node implements the repeat Corrected error counter in \( \text{ERR}<m>\text{MISC}0 \) for each error record \( <m> \) owned by the node that implements the standard Corrected error counter.

<table>
<thead>
<tr>
<th>RP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A single CE counter is implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>A first (repeat) counter and a second (other) counter are implemented. The repeat counter is the same size as the primary error counter.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

CEC, bits [14:12]

Corrected Error Counter. Indicates whether the node implements the standard Corrected error counter (CE counter) mechanisms in \( \text{ERR}<m>\text{MISC}0 \) for each error record \( <m> \) owned by the node that can record countable errors.

<table>
<thead>
<tr>
<th>CEC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Does not implement the standard Corrected error counter model.</td>
</tr>
<tr>
<td>0b010</td>
<td>Implements an 8-bit Corrected error counter in ( \text{ERR}&lt;m&gt;\text{MISC}0[39:32] ).</td>
</tr>
<tr>
<td>0b100</td>
<td>Implements a 16-bit Corrected error counter in ( \text{ERR}&lt;m&gt;\text{MISC}0[47:32] ).</td>
</tr>
</tbody>
</table>

All other values are reserved.

Note

Implementations might include other error counter models, or might include the standard model and not indicate this in \( \text{ERR}<n>\text{FR} \).
CFI, bits [11:10]

When ERR<n>FR.FI != 0b00:

Fault handling interrupt for corrected errors. Indicates whether the control for enabling fault handling interrupts on corrected errors are implemented.

<table>
<thead>
<tr>
<th>CFI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the control for enabling fault handling interrupts on corrected errors. ERR&lt;n&gt;CTRL.CFI is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Control for enabling fault handling interrupts on corrected errors is supported and controllable using ERR&lt;n&gt;CTRL.CFI.</td>
</tr>
<tr>
<td>0b11</td>
<td>Control for enabling fault handling interrupts on corrected errors is supported and controllable using ERR&lt;n&gt;CTRL.WCFI for writes and ERR&lt;n&gt;CTRL.RCFI for reads.</td>
</tr>
</tbody>
</table>

All other values are reserved.

Otherwise:

Reserved, RES0.

UE, bits [9:8]

In-band uncorrected error reporting. Indicates whether the in-band uncorrected error reporting (External Aborts) and associated controls are implemented.

<table>
<thead>
<tr>
<th>UE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the in-band uncorrected error reporting (External Aborts). ERR&lt;n&gt;CTRL.UE is RES0.</td>
</tr>
<tr>
<td>0b01</td>
<td>In-band uncorrected error reporting (External Aborts) is supported and always enabled. ERR&lt;n&gt;CTRL.UE is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>In-band uncorrected error reporting (External Aborts) is supported and controllable using ERR&lt;n&gt;CTRL.UE.</td>
</tr>
<tr>
<td>0b11</td>
<td>In-band uncorrected error reporting (External Aborts) is supported and controllable using ERR&lt;n&gt;CTRL.WUE for writes and ERR&lt;n&gt;CTRL.RUE for reads.</td>
</tr>
</tbody>
</table>

FI, bits [7:6]

Fault handling interrupt. Indicates whether the fault handling interrupt and associated controls are implemented.

<table>
<thead>
<tr>
<th>FI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the fault handling interrupt. ERR&lt;n&gt;CTRL.FI is RES0.</td>
</tr>
<tr>
<td>0b01</td>
<td>Fault handling interrupt is supported and always enabled. ERR&lt;n&gt;CTRL.FI is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Fault handling interrupt is supported and controllable using ERR&lt;n&gt;CTRL.FI.</td>
</tr>
<tr>
<td>0b11</td>
<td>Fault handling interrupt is supported and controllable using ERR&lt;n&gt;CTRL.WFI for writes and ERR&lt;n&gt;CTRL.RFI for reads.</td>
</tr>
</tbody>
</table>

Ui, bits [5:4]

Error recovery interrupt for uncorrected errors. Indicates whether the error handling interrupt and associated controls are implemented.
<table>
<thead>
<tr>
<th>UI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Does not support the error handling interrupt. ERR&lt;n&gt;CTLR.UI is RES0.</td>
</tr>
<tr>
<td>0b01</td>
<td>Error handling interrupt is supported and always enabled. ERR&lt;n&gt;CTLR.UI is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Error handling interrupt is supported and controllable using ERR&lt;n&gt;CTLR.UI.</td>
</tr>
<tr>
<td>0b11</td>
<td>Error handling interrupt is supported and controllable using ERR&lt;n&gt;CTLR.WUI for writes and ERR&lt;n&gt;CTLR.RUI for reads.</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [3:2]**

IMPLEMENTATION DEFINED.

**ED, bits [1:0]**

Error reporting and logging. Indicates whether error record <n> is the first record owned the node, and, if so, whether it implements the controls for enabling and disabling error reporting and logging.

<table>
<thead>
<tr>
<th>ED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b01</td>
<td>Error reporting and logging always enabled. ERR&lt;n&gt;CTLR.ED is RES0.</td>
</tr>
<tr>
<td>0b10</td>
<td>Error reporting and logging is controllable using ERR&lt;n&gt;CTLR.ED.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**When ERR<n>FR.ED == 0b00:**

<table>
<thead>
<tr>
<th>Bits [63:2]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
</table>

**ED, bits [1:0]**

Error reporting and logging. Indicates error record <n> is not the first record owned by the node.

<table>
<thead>
<tr>
<th>ED</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Error record &lt;n&gt; is not the first record owned by the node.</td>
</tr>
</tbody>
</table>

This field reads as 0b00.

**Accessing the ERR<n>FR**

ERR<n>FR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x000 + (64 * n)</td>
<td>ERR&lt;n&gt;FR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The ERR<n>MISC0 characteristics are:

**Purpose**

*IMPLEMENTATION DEFINED* error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

If the node that owns error record <n> implements architecturally-defined error counters (*ERR<q>FR.CEC != 0b000*), and error record <n> can record countable errors, then ERR<n>MISC0 implements the architecturally-defined error counter or counters.

**Configuration**

This register is present only when error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC0 are RES0.

*ERR<q>FR* describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record, then q = n.

For *IMPLEMENTATION DEFINED* fields in ERR<n>MISC0, writing zero returns the error record to an initial quiescent state.

In particular, if any *IMPLEMENTATION DEFINED* syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, non-zero, and ignore writes are compliant with this requirement.

**Note**

Arm recommends that any *IMPLEMENTATION DEFINED* syndrome field that can generate a Fault Handling, Error Recovery, Critical, or *IMPLEMENTATION DEFINED* interrupt request is disabled at Cold reset and is enabled by software writing an *IMPLEMENTATION DEFINED* nonzero value to an *IMPLEMENTATION DEFINED* field in *ERR<q>CTRL*.

**Attributes**

ERR<n>MISC0 is a 64-bit register.

**Field descriptions**

The ERR<n>MISC0 bit assignments are:

**When ERR<q>FR.CEC == 0b000:**

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-0</td>
<td><em>IMPLEMENTATION DEFINED</em></td>
</tr>
<tr>
<td>31-1</td>
<td><em>IMPLEMENTATION DEFINED</em></td>
</tr>
</tbody>
</table>
IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED syndrome.

**When ERR<q>FR.CEC == 0b100 and ERR<q>FR.RP == 0:**

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
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<td>IMPLEMENTATION DEFINED</td>
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</tbody>
</table>

IMPLEMENTATION DEFINED, bits [63:48]

IMPLEMENTATION DEFINED syndrome.

**OF, bit [47]**

Sticky overflow bit. Set to 1 when ERR<n>MISC0.CEC is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CEC, bits [46:32]**

Corrected error count. Incremented for each Corrected error. It is IMPLEMENTATION DEFINED and might be UNPREDICTABLE whether Deferred and Uncorrected errors are counted.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

IMPLEMENTATION DEFINED, bits [31:0]

IMPLEMENTATION DEFINED syndrome.

**When ERR<q>FR.CEC == 0b010 and ERR<q>FR.RP == 0:**

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----| IMPLEMENTATION DEFINED |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [63:40]

IMPLEMENTATION DEFINED syndrome.

**OF, bit [39]**

Sticky overflow bit. Set to 1 when ERR<n>MISC0.CEC is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.
On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CEC, bits [38:32]**

Corrected error count. Incremented for each Corrected error. It is IMPLEMENTATION DEFINED and might be UNPREDICTABLE whether Deferred and Uncorrected errors are counted.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED syndrome.

**When ERR<q>FR.CEC == 0b100 and ERR<q>FR.RP == 1:**

| 63  | 62  | 61  | 60  | 59  | 58  | 57  | 56  | 55  | 54  | 53  | 52  | 51  | 50  | 49  | 48  | 47  | 46  | 45  | 44  | 43  | 42  | 41  | 40  | 39  | 38  | 37  | 36  | 35  | 34  | 33  | 32  |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| OFO | CECO | OFR | CECR |
| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |

**OFO, bit [63]**

Sticky overflow bit, other. Set to 1 when ERR<n>MISC0.CECO is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OFO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Other counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Other counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CECO, bits [62:48]**

Corrected error count, other. Incremented for each countable error that is not accounted for by incrementing ERR<n>MISC0.CECR.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**OFR, bit [47]**

Sticky overflow bit, repeat. Set to 1 when ERR<n>MISC0.CECR is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OFR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Repeat counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Repeat counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CECR, bits [46:32]**

Corrected error count, repeat. Incremented for the first countable error, which also records other syndrome for the error, and subsequently for each countable error that matches the recorded other syndrome. Corrected errors are countable errors. It is IMPLEMENTATION DEFINED and might be UNPREDICTABLE whether Deferred and Uncorrected errors are countable errors.

**Note**
For example, the other syndrome might include the set and way information for an error detected in a cache. This might be recorded in the IMPLEMENTATION DEFINED ERR<n>MISC<m> fields on a first Corrected error. ERR<n>MISC0.CECR is then incremented for each subsequent Corrected Error in the same set and way.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**IMPLEMENTATION DEFINED, bits [31:0]**

**When ERR<q>FR.CEC == 0b010 and ERR<q>FR.RP == 1:**

<table>
<thead>
<tr>
<th></th>
<th>IMPLEMENTATION DEFINED</th>
<th>OFO</th>
<th>CECO</th>
<th>OFR</th>
<th>CECR</th>
</tr>
</thead>
<tbody>
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</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [63:48]**

**OFO, bit [47]**

Sticky overflow bit, other. Set to 1 when ERR<n>MISC0.CECO is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OFO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Other counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Other counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CECO, bits [46:40]**

Corrected error count, other. Incremented for each countable error that is not accounted for by incrementing ERR<n>MISC0.CECR.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**OFR, bit [39]**

Sticky overflow bit, repeat. Set to 1 when ERR<n>MISC0.CECR is incremented and wraps through zero.

<table>
<thead>
<tr>
<th>OFR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Repeat counter has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Repeat counter has overflowed.</td>
</tr>
</tbody>
</table>

A direct write that modifies this bit might indirectly set ERR<n>STATUS.OF to an UNKNOWN value and a direct write to ERR<n>STATUS.OF that clears it to zero might indirectly set this bit to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**CECR, bits [38:32]**

Corrected error count, repeat. Incorporated for the first countable error, which also records other syndrome for the error, and subsequently for each countable error that matches the recorded other syndrome. Corrected errors are
countable errors. It is IMPLEMENTATION DEFINED and might be UNPREDICTABLE whether Deferred and Uncorrected errors are countable errors.

---

**Note**

For example, the other syndrome might include the set and way information for an error detected in a cache. This might be recorded in the IMPLEMENTATION DEFINED ERR<n>MISC<m> fields on a first Corrected error. ERR<n>MISC0.CECR is then incremented for each subsequent Corrected Error in the same set and way.

---

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**IMPLEMENTATION DEFINED, bits [31:0]**

**IMPLEMENTATION DEFINED** syndrome.

### Accessing the ERR<n>MISC0

Reads from ERR<n>MISC0 return an IMPLEMENTATION DEFINED value and writes have IMPLEMENTATION DEFINED behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and ERR<n>PFGF.MV is 0b1, then some parts of this register are read/write when ERR<n>STATUS.MV == 0b1. See ERR<n>PFGF.MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When ERR<n>STATUS.MV == 0b1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

---

**Note**

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

### ERR<n>MISC0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x820 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERR<n>MISC1, Error Record Miscellaneous Register 1, n = 0 - 65534

The ERR<n>MISC1 characteristics are:

**Purpose**

IMPLEMENTATION DEFINED error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

**Configuration**

This register is present only when error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC1 are RES0.

ERR<q>FR describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record, then q = n.

For IMPLEMENTATION DEFINED fields in ERR<n>MISC1, writing zero returns the error record to an initial quiescent state.

In particular, if any IMPLEMENTATION DEFINED syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, non-zero, and ignore writes are compliant with this requirement.

**Note**

Arm recommends that any IMPLEMENTATION DEFINED syndrome field that can generate a Fault Handling, Error Recovery, Critical, or IMPLEMENTATION DEFINED, interrupt request is disabled at Cold reset and is enabled by software writing an IMPLEMENTATION DEFINED nonzero value to an IMPLEMENTATION DEFINED field in ERR<q>CTLR.

**Attributes**

ERR<n>MISC1 is a 64-bit register.

**Field descriptions**

The ERR<n>MISC1 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| **IMPLEMENTATION DEFINED** | **IMPLEMENTATION DEFINED** |

**IMPLEMENTATION DEFINED, bits [63:0]**

IMPLEMENTATION DEFINED syndrome.
Accessing the ERR<n>MISC1

Reads from ERR<n>MISC1 return an IMPLEMENTATION DEFINED value and writes have IMPLEMENTATION DEFINED behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and ERR<n>PFGF.MV is 0b1, then some parts of this register are read/write when ERR<n>STATUS.MV == 0b1. See ERR<n>PFGF.MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When ERR<n>STATUS.MV == 0b1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

**Note**

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

**ERR<n>MISC1 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x028 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC1</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERR<n>MISC2, Error Record Miscellaneous Register 2, n = 0 - 65534

The ERR<n>MISC2 characteristics are:

**Purpose**

IMPLEMENTATION DEFINED error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

**Configuration**

This register is present only when (an implementation implements ERR<n>MISC2 or RAS System Architecture v1.1 is implemented) and error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC2 are RES0.

ERR<q>FR describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record, then q = n.

For IMPLEMENTATION DEFINED fields in ERR<n>MISC2, writing zero returns the error record to an initial quiescent state.

In particular, if any IMPLEMENTATION DEFINED syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, non-zero, and ignore writes are compliant with this requirement.

If RAS System Architecture v1.1 is not implemented, Arm recommendes that ERR<n>MISC2 does not require zeroing to return the record to a quiescent state.

**Note**

Arm recommends that any IMPLEMENTATION DEFINED syndrome field that can generate a Fault Handling, Error Recovery, Critical, or IMPLEMENTATION DEFINED, interrupt request is disabled at Cold reset and is enabled by software writing an IMPLEMENTATION DEFINED nonzero value to an IMPLEMENTATION DEFINED field in ERR<q>CTRL.

**Attributes**

ERR<n>MISC2 is a 64-bit register.

**Field descriptions**

The ERR<n>MISC2 bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| IMPLEMENTATION DEFINED | IMPLEMENTATION DEFINED |

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED syndrome.
Accessing the ERR<n>MISC2

Reads from ERR<n>MISC2 return an IMPLEMENTATION DEFINED value and writes have IMPLEMENTATION DEFINED behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and ERR<n>PFGF.MV is 0b1, then some parts of this register are read/write when ERR<n>STATUS.MV == 0b1. See ERR<n>PFGF.MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When ERR<n>STATUS.MV == 0b1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

Note

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

ERR<n>MISC2 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x030 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC2</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERR<n>MISC3, Error Record Miscellaneous Register 3, n = 0 - 65534

The ERR<n>MISC3 characteristics are:

**Purpose**

IMPLEMENTATION DEFINED error syndrome register. The miscellaneous syndrome registers might contain:

- Information to locate where the error was detected.
- If the error was detected within a FRU, the identity of the FRU.
- A Corrected error counter or counters.
- Other state information not present in the corresponding status and address registers.

If the node that owns error record n supports the RAS Timestamp Extension (ERR<q>FR.TS != 0b00), then ERR<n>MISC3 contains the timestamp value for error record n when the error was detected. Otherwise the contents of ERR<n>MISC3 are IMPLEMENTATION DEFINED.

**Configuration**

This register is present only when (an implementation implements ERR<n>MISC3 or RAS System Architecture v1.1 is implemented) and error record <n> is implemented. Otherwise, direct accesses to ERR<n>MISC3 are RES0.

ERR<q>FR describes the features implemented by the node that owns error record <n>. <q> is the index of the first error record owned by the same node as error record <n>. If the node owns a single record, then q = n.

For IMPLEMENTATION DEFINED fields in ERR<n>MISC3, writing zero returns the error record to an initial quiescent state.

In particular, if any IMPLEMENTATION DEFINED syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, non-zero, and ignore writes are compliant with this requirement.

If RAS System Architecture v1.1 is not implemented, Arm recommended that ERR<n>MISC3 does not require zeroing to return the record to a quiescent state.

**Note**

Arm recommends that any IMPLEMENTATION DEFINED syndrome field that can generate a Fault Handling, Error Recovery, Critical, or IMPLEMENTATION DEFINED, interrupt request is disabled at Cold reset and is enabled by software writing an IMPLEMENTATION DEFINED nonzero value to an IMPLEMENTATION DEFINED field in ERR<q>CTRL.

**Attributes**

ERR<n>MISC3 is a 64-bit register.

**Field descriptions**

The ERR<n>MISC3 bit assignments are:
When ERR<q>FR.TS != 0b00:

TS, bits [63:0]

Timestamp. Timestamp value recorded when the error was detected. Valid only if ERR<n>STATUS.V == 0b1.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

Access to this field is RO or RW.

When ERR<q>FR.TS == 0b00:

IMPLEMENTATION DEFINED, bits [63:0]

IMPLEMENTATION DEFINED syndrome.

Accessing the ERR<n>MISC3

Reads from ERR<n>MISC3 return an IMPLEMENTATION DEFINED value and writes have IMPLEMENTATION DEFINED behavior.

If the Common Fault Injection Mechanism is implemented by the node that owns this error record, and ERR<q>PFGF.MV is 0b1, then some parts of this register are read/write when ERR<n>STATUS.MV == 0b1. See ERR<n>PFGF.MV for more information.

For other parts of this register, or if the Common Fault Injection Mechanism is not implemented, then Arm recommends that:

- Miscellaneous syndrome for multiple errors, such as a corrected error counter, is read/write.
- When ERR<n>STATUS.MV == 0b1, the miscellaneous syndrome specific to the most recently recorded error ignores writes.

Note

These recommendations allow a counter to be reset in the presence of a persistent error, while preventing specific information, such as that identifying a FRU, from being lost if an error is detected while the previous error is being logged.

ERR<n>MISC3 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x638 + (64 * n)</td>
<td>ERR&lt;n&gt;MISC3</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The ERR<n>PFGCDN characteristics are:

**Purpose**

Generates one of the errors enabled in the corresponding ERR<n>PFGCTL register.

**Configuration**

This register is present only when error record <n> is implemented, the node implements the RAS Common Fault Injection Model Extension (ERR<n>FR.INJ != 0b00) and error record <n> is the first error record owned by a node. Otherwise, direct accesses to ERR<n>PFGCDN are reserved.

ERR<n>FR describes the features implemented by the node.

**Attributes**

ERR<n>PFGCDN is a 64-bit register.

**Field descriptions**

The ERR<n>PFGCDN bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CDN |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**Bits [63:32]**

Reserved, RES0.

**CDN, bits [31:0]**

Countdown value.

This field is copied to Error Generation Counter when either:

- Software writes ERR<n>PFGCTL.CDNEN with 1.
- The Error Generation Counter decrements to zero and ERR<n>PFGCTL.R == 0b1.

While ERR<n>PFGCTL.CDNEN == 0b1 and the Error Generation Counter is nonzero, the counter decrements by 1 for each cycle at an IMPLEMENTATION DEFINED clock rate. When the counter reaches 0, one of the errors enabled in the ERR<n>PFGCTL register is generated.

**Note**

The current Error Generation Counter value is not visible to software.

On a Cold reset, this field resets to an architecturally UNKNOWN value.
Accessing the ERR\textless n\textgreater PFGCDN

ERR\textless n\textgreater PFGCDN can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x810 + (64 * n)</td>
<td>ERR\textless n\textgreater PFGCDN</td>
</tr>
</tbody>
</table>

Accesses on this interface are \textbf{RW}.
**ERR<n>PFGCTL, Pseudo-fault Generation Control Register, n = 0 - 65534**

The ERR<n>PFGCTL characteristics are:

**Purpose**

Enables controlled fault generation.

**Configuration**

This register is present only when error record <n> is implemented, the node implements the RAS Common Fault Injection Model Extension (ERR<n>FR.INJ != 0b00) and error record <n> is the first error record owned by a node. Otherwise, direct accesses to ERR<n>PFGCTL are RES0.

ERR<n>FR describes the features implemented by the node.

**Attributes**

ERR<n>PFGCTL is a 64-bit register.

**Field descriptions**

The ERR<n>PFGCTL bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| CDNEN | R | RES0 | MV | AV | VN | ER | CI | CE | DE | UE | O | UE0 | UE1 | UEU | UC | OF |

**Bits [63:32]**

Reserved, RES0.

**CDNEN, bit [31]**

Countdown Enable. Controls transfers from the value that is held in the ERR<n>PFGCDN into the Error Generation Counter and enables this counter.

<table>
<thead>
<tr>
<th>CDNEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Error Generation Counter is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Error Generation Counter is enabled. On a write of 0b1 to this bit, the Error Generation Counter is set to ERR&lt;n&gt;PFGCDN.CDN.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to 0.

**R, bit [30]**

Restart. Controls whether, upon reaching zero, the Error Generation Counter restarts from the ERR<n>PFGCDN value or stops.

<table>
<thead>
<tr>
<th>R</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>On reaching 0, the Error Generation Counter will stop.</td>
</tr>
<tr>
<td>0b1</td>
<td>On reaching 0, the Error Generation Counter is set to ERR&lt;n&gt;PFGCDN.CDN.</td>
</tr>
</tbody>
</table>
This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**Bits [29:13]**

Reserved, \texttt{RES0}.

**MV, bit [12]**

Miscellaneous syndrome. The value that is written to \texttt{ERR<n>STATUS.MV} when an injected error is recorded.

<table>
<thead>
<tr>
<th>MV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>\texttt{ERR&lt;n&gt;STATUS.MV} is set to 0b0 when an injected error is recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>\texttt{ERR&lt;n&gt;STATUS.MV} is set to 0b1 when an injected error is recorded.</td>
</tr>
</tbody>
</table>

This bit reads-as-one if the node always records some syndrome in \texttt{ERR<n>MISC<m>}, setting \texttt{ERR<n>STATUS.MV} to 1, when an injected error is recorded. This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**AV, bit [11]**

Address syndrome. The value that is written to \texttt{ERR<n>STATUS.AV} when an injected error is recorded.

<table>
<thead>
<tr>
<th>AV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>\texttt{ERR&lt;n&gt;STATUS.AV} is set to 0b0 when an injected error is recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>\texttt{ERR&lt;n&gt;STATUS.AV} is set to 0b1 when an injected error is recorded.</td>
</tr>
</tbody>
</table>

This bit reads-as-one if the node always sets \texttt{ERR<n>STATUS.AV} to 0b1 when an injected error is recorded. This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**PN, bit [10]**

Poison flag. The value that is written to \texttt{ERR<n>STATUS.PN} when an injected error is recorded.

<table>
<thead>
<tr>
<th>PN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>\texttt{ERR&lt;n&gt;STATUS.PN} is set to 0b0 when an injected error is recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>\texttt{ERR&lt;n&gt;STATUS.PN} is set to 0b1 when an injected error is recorded.</td>
</tr>
</tbody>
</table>

This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

**ER, bit [9]**

Error Reported flag. The value that is written to \texttt{ERR<n>STATUS.ER} when an injected error is recorded.

<table>
<thead>
<tr>
<th>ER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>\texttt{ERR&lt;n&gt;STATUS.ER} is set to 0b0 when an injected error is recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>\texttt{ERR&lt;n&gt;STATUS.ER} is set to 0b1 when an injected error is recorded.</td>
</tr>
</tbody>
</table>

This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.
CI, bit [8]

Critical Error flag. The value that is written to \texttt{ERR<n>STATUS.CI} when an injected error is recorded.

\begin{table}[ht]
\centering
\begin{tabular}{|c|p{14em}|}
\hline
CI & Meaning \\
\hline
0b0 & \texttt{ERR<n>STATUS.CI} is set to 0b0 when an injected error is recorded. \\
0b1 & \texttt{ERR<n>STATUS.CI} is set to 0b1 when an injected error is recorded. \\
\hline
\end{tabular}
\end{table}

This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

CE, bits [7:6]

Corrected Error generation enable. Controls the type of Corrected Error condition that might be generated.

\begin{table}[ht]
\centering
\begin{tabular}{|c|p{14em}|}
\hline
CE & Meaning \\
\hline
0b00 & No error of this type will be generated. \\
0b01 & A non-specific Corrected Error, that is, a Corrected Error that is recorded as \texttt{ERR<n>STATUS.CE} == 0b10, might be generated when the Error Generation Counter decrements to zero. \\
0b10 & A transient Corrected Error; that is, a Corrected Error that is recorded as \texttt{ERR<n>STATUS.CE} == 0b01, might be generated when the Error Generation Counter decrements to zero. \\
0b11 & A persistent Corrected Error; that is, a Corrected Error that is recorded as \texttt{ERR<n>STATUS.CE} == 0b11, might be generated when the Error Generation Counter decrements to zero. \\
\hline
\end{tabular}
\end{table}

The set of permitted values for this field is defined by \texttt{ERR<n>PFGF.CE}. This field is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

DE, bit [5]

Deferred Error generation enable. Controls whether this type of error condition might be generated. It is IMPLEMENTATION DEFINED whether the error is generated if the data is not consumed.

\begin{table}[ht]
\centering
\begin{tabular}{|c|p{14em}|}
\hline
DE & Meaning \\
\hline
0b0 & No error of this type will be generated. \\
0b1 & An error of this type might be generated when the Error Generation Counter decrements to zero. \\
\hline
\end{tabular}
\end{table}

This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.

UEO, bit [4]

Latent or Restartable Error generation enable. Controls whether this type of error condition might be generated. It is IMPLEMENTATION DEFINED whether the error is generated if the data is not consumed.

\begin{table}[ht]
\centering
\begin{tabular}{|c|p{14em}|}
\hline
UEO & Meaning \\
\hline
0b0 & No error of this type will be generated. \\
0b1 & An error of this type might be generated when the Error Generation Counter decrements to zero. \\
\hline
\end{tabular}
\end{table}

This bit is \texttt{RES0} if the node does not support this control.

On a Cold reset, this field resets to an architecturally \texttt{UNKNOWN} value.
UER, bit [3]

Signaled or Recoverable Error generation enable. Controls whether this type of error condition might be generated. It is IMPLEMENTATION DEFINED whether the error is generated if the data is not consumed.

<table>
<thead>
<tr>
<th>UER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No error of this type will be generated.</td>
</tr>
<tr>
<td>0b1</td>
<td>An error of this type might be generated when the Error Generation Counter decrements to zero.</td>
</tr>
</tbody>
</table>

This bit is RES0 if the node does not support this control.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

UEU, bit [2]

Unrecoverable Error generation enable. Controls whether this type of error condition might be generated. It is IMPLEMENTATION DEFINED whether the error is generated if the data is not consumed.

<table>
<thead>
<tr>
<th>UEU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No error of this type will be generated.</td>
</tr>
<tr>
<td>0b1</td>
<td>An error of this type might be generated when the Error Generation Counter decrements to zero.</td>
</tr>
</tbody>
</table>

This bit is RES0 if the node does not support this control.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

UC, bit [1]

Uncontainable Error generation enable. Controls whether this type of error condition might be generated. It is IMPLEMENTATION DEFINED whether the error is generated if the data is not consumed.

<table>
<thead>
<tr>
<th>UC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No error of this type will be generated.</td>
</tr>
<tr>
<td>0b1</td>
<td>An error of this type might be generated when the Error Generation Counter decrements to zero.</td>
</tr>
</tbody>
</table>

This bit is RES0 if the node does not support this control.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

OF, bit [0]

Overflow flag. The value that is written to `ERR<n>STATUS.OF` when an injected error is recorded.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>ERR&lt;n&gt;STATUS.OF</code> is set to 0b0 when an injected error is recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>ERR&lt;n&gt;STATUS.OF</code> is set to 0b1 when an injected error is recorded.</td>
</tr>
</tbody>
</table>

This bit is RES0 if the node does not support this control.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ERR<n>PFGCTL**

`ERR<n>PFGCTL` can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x808</td>
<td>ERR&lt;n&gt;PFGCTL</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERR<n>PFGCTL, Pseudo-fault Generation Control Register, n = 0 - 65534
ERR<n>PFGF, Pseudo-fault Generation Feature Register, n = 0 - 65534

The ERR<n>PFGF characteristics are:

**Purpose**

Defines which common architecturally-defined fault generation features are implemented.

**Configuration**

This register is present only when error record <n> is implemented, the node implements the RAS Common Fault Injection Model Extension (ERR<n>FR.INJ != 0b00) and error record <n> is the first error record owned by a node. Otherwise, direct accesses to ERR<n>PFGF are RES0.

ERR<n>FR describes the features implemented by the node.

**Attributes**

ERR<n>PFGF is a 64-bit register.

**Field descriptions**

The ERR<n>PFGF bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | R | SYN | RES0 | MV | AV | PN | ER | CI | CE | DE | UE | QU | UE | UJ | UE | UC | OF |

**Bits [63:31]**

Reserved, RES0.

**R, bit [30]**

Restartable. Support for Error Generation Counter restart mode.

<table>
<thead>
<tr>
<th>R</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The node does not support this feature.</td>
</tr>
<tr>
<td>0b1</td>
<td>Feature controllable.</td>
</tr>
</tbody>
</table>

**SYN, bit [29]**

Syndrome. Fault syndrome injection.

<table>
<thead>
<tr>
<th>SYN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When an injected error is recorded, the node sets ERR&lt;n&gt;STATUS. {IERR, SERR} to IMPLEMENTATION DEFINED values. ERR&lt;n&gt;STATUS. {IERR, SERR} are UNKNOWN when ERR&lt;n&gt;STATUS.V == 0b0.</td>
</tr>
<tr>
<td>0b1</td>
<td>When an injected error is recorded, the node does not update the ERR&lt;n&gt;STATUS. {IERR, SERR} fields. ERR&lt;n&gt;STATUS. {IERR, SERR} are writable when ERR&lt;n&gt;STATUS.V == 0b0.</td>
</tr>
</tbody>
</table>

**Note**
If ERR\textsubscript{n}>PFGF.SYN == 0b1, software can write specific values into the \texttt{ERR\textsubscript{n}>STATUS}.\{IERR, SERR\} fields when setting up a fault injection event. The sets of values that can be written to these fields is \texttt{IMPLEMENTATION DEFINED}.

**Bits [28:13]**

Reserved, RES0.

**MV, bit [12]**

Miscellaneous syndrome.

Additional syndrome injection. Defines whether software can control all or part of the syndrome recorded in the ERR\textsubscript{n}>MISC\textsubscript<m> registers when an injected error is recorded.

It is \texttt{IMPLEMENTATION DEFINED} which syndrome fields in ERR\textsubscript{n}>MISC\textsubscript<m> this refers to, as some fields might always be recorded by an error. For example, a Corrected Error counter.

<table>
<thead>
<tr>
<th>MV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When an injected error is recorded, the node might record \texttt{IMPLEMENTATION DEFINED} additional syndrome in ERR\textsubscript{n}&gt;MISC\textsubscript&lt;m&gt;. If any syndrome is recorded in ERR\textsubscript{n}&gt;MISC\textsubscript&lt;m&gt;, then ERR\textsubscript{n}&gt;STATUS.MV is set to 0b1.</td>
</tr>
</tbody>
</table>
| 0b1 | When an injected error is recorded, the node does not update all the syndrome fields in the ERR\textsubscript{n}>MISC\textsubscript<m> and does one of:  
• The node does not update any fields in ERR\textsubscript{n}>MISC\textsubscript<m> and sets ERR\textsubscript{n}>STATUS.MV to ERR\textsubscript{n}>PFGCTL.MV.  
• The node records some syndrome in ERR\textsubscript{n}>MISC\textsubscript<m> and sets ERR\textsubscript{n}>STATUS.MV to 0b1. ERR\textsubscript{n}>PFGCTL.MV is \texttt{RAO}.  
The syndrome fields that the node does not update are unchanged and are writable when ERR\textsubscript{n}>STATUS.MV == 0b0. |

**Note**

If ERR\textsubscript{n}>PFGF.MV == 0b1, software can write specific values into the ERR\textsubscript{n}>MISC\textsubscript<m> registers when setting up a fault injection event. The values that can be written to these registers are \texttt{IMPLEMENTATION DEFINED}.

**AV, bit [11]**

Address syndrome. Address syndrome injection.

<table>
<thead>
<tr>
<th>AV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When an injected error is recorded, the node either sets ERR\textsubscript{n}&gt;ADDR and ERR\textsubscript{n}&gt;STATUS.AV for the access, or leaves these unchanged.</td>
</tr>
</tbody>
</table>
| 0b1 | When an injected error is recorded, the node does not update ERR\textsubscript{n}>ADDR and does one of:  
• Sets ERR\textsubscript{n}>STATUS.AV to ERR\textsubscript{n}>PFGCTL.AV.  
• Sets ERR\textsubscript{n}>STATUS.AV to 0b1. ERR\textsubscript{n}>PFGCTL.AV is \texttt{RAO}.  
ERR\textsubscript{n}>ADDR is writable when ERR\textsubscript{n}>STATUS.AV == 0b0. |

**Note**

If ERR\textsubscript{n}>PFGF.AV == 0b1, software can write a specific value into ERR\textsubscript{n}>ADDR when setting up a fault injection event.

**PN, bit [10]**

Poison flag. Describes how the fault generation feature of the node sets the ERR\textsubscript{n}>STATUS.PN status flag.
### PN

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>When an injected error is recorded, it is IMPLEMENTATION DEFINED</td>
<td>When an injected error is recorded, ERR&lt;n&gt;STATUS.PN to 0b1.</td>
<td>When an injected error is recorded, ERR&lt;n&gt;STATUS.PN is set to</td>
</tr>
<tr>
<td>whether the node sets ERR&lt;n&gt;STATUS.PN to 0b1.</td>
<td></td>
<td>ERR&lt;n&gt;PFGCTL.PN.</td>
</tr>
</tbody>
</table>

This behavior replaces the architecture-defined rules for setting the PN bit.

This bit reads-as-zero if the node does not support this flag.

### ER, bit [9]

Error Reported flag. Describes how the fault generation feature of the node sets the ERR<n>STATUS.ER status flag.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>When an injected error is recorded, the node sets ERR&lt;n&gt;STATUS.ER</td>
<td>When an injected error is recorded, ERR&lt;n&gt;STATUS.ER is set to</td>
<td></td>
</tr>
<tr>
<td>according to the architecture-defined rules for setting the ER bit.</td>
<td>ERR&lt;n&gt;PFGCTL.ER.</td>
<td></td>
</tr>
</tbody>
</table>

This bit reads-as-zero if the node does not support this flag.

### CI, bit [8]

Critical Error flag. Describes how the fault generation feature of the node sets the ERR<n>STATUS.CI status flag.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>0b1</th>
</tr>
</thead>
<tbody>
<tr>
<td>When an injected error is recorded, it is IMPLEMENTATION DEFINED</td>
<td>When an injected error is recorded, ERR&lt;n&gt;STATUS.CI to 0b1.</td>
<td>When an injected error is recorded, ERR&lt;n&gt;STATUS.CI is set to</td>
</tr>
<tr>
<td>whether the node sets ERR&lt;n&gt;STATUS.CI to 0b1.</td>
<td></td>
<td>ERR&lt;n&gt;PFGCTL.CI.</td>
</tr>
</tbody>
</table>

This behavior replaces the architecture-defined rules for setting the CI bit.

This bit reads-as-zero if the node does not support this flag.

### CE, bits [7:6]

Corrected Error generation. Describes the types of Corrected Error that the fault generation feature of the node can generate.

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b00</th>
<th>0b01</th>
<th>0b11</th>
</tr>
</thead>
<tbody>
<tr>
<td>The fault generation feature of the node cannot generate this type of</td>
<td>The fault generation feature of the node allows generation of a</td>
<td>The fault generation feature of the node allows generation of</td>
<td></td>
</tr>
<tr>
<td>error.</td>
<td>non-specific Corrected Error, that is, a Corrected Error that is</td>
<td>transient or persistent Corrected Errors, that is, Corrected</td>
<td></td>
</tr>
<tr>
<td></td>
<td>recorded as ERR&lt;n&gt;STATUS.CE == 0b10.</td>
<td>Errors that are recorded as ERR&lt;n&gt;STATUS.CE == 0b01 and 0b11.</td>
<td></td>
</tr>
</tbody>
</table>

All other values are reserved.

If ERR<n>FR.FRX is 0b1 then ERR<n>FR.CE indicates whether the node supports this type of error.

This field reads-as-zeros if the node does not support this type of error.

### DE, bit [5]

Deferred Error generation. Describes whether the fault generation feature of the node can generate this type of error.
If $\text{ERR}_n\text{FR}.\text{FRX}$ is 0b1 then $\text{ERR}_n\text{FR}.\text{DE}$ indicates whether the node supports this type of error.

This bit reads-as-zero if the node does not support this type of error.

### UEO, bit [4]

Latent or Restartable Error generation. Describes whether the fault generation feature of the node can generate this type of error.

<table>
<thead>
<tr>
<th>UEO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault generation feature of the node cannot generate this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault generation feature of the node allows generation of this type of error.</td>
</tr>
</tbody>
</table>

If $\text{ERR}_n\text{FR}.\text{FRX}$ is 0b1 then $\text{ERR}_n\text{FR}.\text{UEO}$ indicates whether the node supports this type of error.

This bit reads-as-zero if the node does not support this type of error.

### UER, bit [3]

Signaled or Recoverable Error generation. Describes whether the fault generation feature of the node can generate this type of error.

<table>
<thead>
<tr>
<th>UER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault generation feature of the node cannot generate this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault generation feature of the node allows generation of this type of error.</td>
</tr>
</tbody>
</table>

If $\text{ERR}_n\text{FR}.\text{FRX}$ is 0b1 then $\text{ERR}_n\text{FR}.\text{UER}$ indicates whether the node supports this type of error.

This bit reads-as-zero if the node does not support this type of error.

### UEU, bit [2]

Unrecoverable Error generation. Describes whether the fault generation feature of the node can generate this type of error.

<table>
<thead>
<tr>
<th>UEU</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault generation feature of the node cannot generate this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault generation feature of the node allows generation of this type of error.</td>
</tr>
</tbody>
</table>

If $\text{ERR}_n\text{FR}.\text{FRX}$ is 0b1 then $\text{ERR}_n\text{FR}.\text{UEU}$ indicates whether the node supports this type of error.

This bit reads-as-zero if the node does not support this type of error.

### UC, bit [1]

Uncontainable Error generation. Describes whether the fault generation feature of the node can generate this type of error.

<table>
<thead>
<tr>
<th>UC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The fault generation feature of the node cannot generate this type of error.</td>
</tr>
<tr>
<td>0b1</td>
<td>The fault generation feature of the node allows generation of this type of error.</td>
</tr>
</tbody>
</table>
If `ERR<n>FR.FR` is 0b1 then `ERR<n>FR.UC` indicates whether the node supports this type of error.

This bit reads-as-zero if the node does not support this type of error.

**OF, bit [0]**

Overflow flag. Describes how the fault generation feature of the node sets the `ERR<n>STATUS.OF` status flag.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When an injected error is recorded, the node sets <code>ERR&lt;n&gt;STATUS.OF</code> according to the architecture-defined rules for setting the OF bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>When an injected error is recorded, <code>ERR&lt;n&gt;STATUS.OF</code> is set to <code>ERR&lt;n&gt;PFGCTL.OF</code>. This behavior replaces the architecture-defined rules for setting the OF bit.</td>
</tr>
</tbody>
</table>

This bit reads-as-zero if the node does not support this flag.

**Accessing the `ERR<n>PFGF`**

`ERR<n>PFGF` can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x800 + (64 * n)</td>
<td><code>ERR&lt;n&gt;PFGF</code></td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERR\(n\)STATUS, Error Record Primary Status Register, \(n = 0 - 65534\)

The ERR\(n\)STATUS characteristics are:

**Purpose**

Contains status information for error record \(\textless n\rangle\), including:

- Whether any error has been detected (valid).
- Whether any detected error was not corrected, and returned to a Requester.
- Whether any detected error was not corrected and deferred.
- Whether an error record has been discarded because additional errors have been detected before the first error was handled by software (overflow).
- Whether any error has been reported.
- Whether the other error record registers contain valid information.
- Whether the error was reported because poison data was detected or because a corrupt value was detected by an error detection code.
- A primary error code.
- An IMPLEMENTATION DEFINED extended error code.

Within this register:

- The \{AV, V, MV\} bits are valid bits that define whether error record \(\textless n\rangle\) registers are valid.
- The \{UE, OF, CE, DE, UET\} bits encode the types of error or errors recorded.
- The \{CI, ER, PN, IERR, SERR\} fields are syndrome fields.

**Configuration**

This register is present only when error record \(\textless n\rangle\) is implemented. Otherwise, direct accesses to ERR\(n\)STATUS are \texttt{RES0}.

ERR\(q\)FR describes the features implemented by the node that owns error record \(\textless n\rangle\). \(q\) is the index of the first error record owned by the same node as error record \(\textless n\rangle\). If the node owns a single record, then \(q = n\).

For IMPLEMENTATION DEFINED fields in ERR\(n\)STATUS, writing zero returns the error record to an initial quiescent state.

In particular, if any IMPLEMENTATION DEFINED syndrome fields might generate a Fault Handling or Error Recovery Interrupt request, writing zero is sufficient to deactivate the Interrupt request.

Fields that are read-only, non-zero, and ignore writes are compliant with this requirement.

**Note**

Arm recommends that any IMPLEMENTATION DEFINED syndrome field that can generate a Fault Handling, Error Recovery, Critical, or IMPLEMENTATION DEFINED, interrupt request is disabled at Cold reset and is enabled by software writing an IMPLEMENTATION DEFINED nonzero value to an IMPLEMENTATION DEFINED field in ERR\(q\)CTRL.

**Attributes**

ERR\(n\)STATUS is a 64-bit register.

**Field descriptions**

The ERR\(n\)STATUS bit assignments are:
When RAS System Architecture v1.1 is implemented:

<table>
<thead>
<tr>
<th>Bits [63:32]</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
</table>
| AV, bit [31] | \(0b0\) \(ERR<n>ADDR\) not valid.  
\(0b1\) \(ERR<n>ADDR\) contains an address associated with the highest priority error recorded by this record. |

This bit is read/write-one-to-clear.  
On a Cold reset, this field resets to 0.

<table>
<thead>
<tr>
<th>Otherwise:</th>
<th>Reserved, RES0.</th>
</tr>
</thead>
</table>
| V, bit [30] | \(0b0\) \(ERR<n>STATUS\) not valid.  
\(0b1\) \(ERR<n>STATUS\) valid. At least one error has been recorded. |

This bit is read/write-one-to-clear.  
On a Cold reset, this field resets to 0.

<table>
<thead>
<tr>
<th>UE, bit [29]</th>
<th>Uncorrected Error.</th>
</tr>
</thead>
<tbody>
<tr>
<td>(0b0)</td>
<td>No errors have been detected, or all detected errors have been either corrected or deferred.</td>
</tr>
<tr>
<td>(0b1)</td>
<td>At least one detected error was not corrected and not deferred.</td>
</tr>
</tbody>
</table>

When clearing \(ERR<n>STATUS. V\) to \(0b0\), if this bit is nonzero, then Arm recommends that software write \(0b1\) to this bit to clear this bit to zero.  
This bit is not valid and reads \textit{UNKNOWN} if \(ERR<n>STATUS. V == 0b0\).  
This bit is read/write-one-to-clear.  
On a Cold reset, this field resets to an architecturally \textit{UNKNOWN} value.

<p>| ER, bit [28] | Error Reported. |</p>
<table>
<thead>
<tr>
<th>ER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No in-band error (External Abort) reported.</td>
</tr>
</tbody>
</table>
| 0b1 | An External Abort was signaled by the component to the Requester making the access or other transaction. This can be because any of the following are true:  
  * The applicable one of the `ERR<q>CTRL`.{WUE,RUE,UE} bits is implemented and was set to 0b1 when an Uncorrected error was detected.  
  * The applicable one of the `ERR<q>CTRL`.{WUE,RUE,UE} bits is not implemented and the component always reports errors. |

It is IMPLEMENTATION DEFINED whether this bit can be set to 0b1 by a Deferred error.

When clearing `ERR<n>STATUS.V` to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads UNKNOWN if any of the following are true:

- `ERR<n>STATUS.V == 0b0`.  
- `ERR<n>STATUS.UE == 0b0` and this bit is never set to 0b1 by a Deferred error.  
- `ERR<n>STATUS.{UE,DE} == {0,0}` and this bit can be set to 0b1 by a Deferred error.

This bit is read/write-one-to-clear.

**Note**

An External Abort signaled by the component might be masked and not generate any exception.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**OF, bit [27]**

Overflow.

Indicates that multiple errors have been detected. This bit is set to 0b1 when one of the following occurs:

- A Corrected error counter is implemented, an error is counted, and the counter overflows.  
- `ERR<n>STATUS.V` was previously set to 0b1, a Corrected error counter is not implemented, and a Corrected error is recorded.  
- `ERR<n>STATUS.V` was previously set to 0b1, and a type of error other than a Corrected error is recorded.

Otherwise, this bit is unchanged when an error is recorded.

If a Corrected error counter is implemented:

- A direct write that modifies the counter overflow flag indirectly might set this bit to an UNKNOWN value.  
- A direct write to this bit that clears this bit to zero might indirectly set the counter overflow flag to an UNKNOWN value.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Since this bit was last cleared to zero, no error syndrome has been discarded and, if a Corrected error counter is implemented, it has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Since this bit was last cleared to zero, at least one error syndrome has been discarded or, if a Corrected error counter is implemented, it might have overflowed.</td>
</tr>
</tbody>
</table>

When clearing `ERR<n>STATUS.V` to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads UNKNOWN if `ERR<n>STATUS.V == 0b0`.  

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**MV, bit [26]**
When error record \( n \) includes an additional information for an error:

Miscellaneous Registers Valid.

<table>
<thead>
<tr>
<th>MV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR( n )MISC(&lt;m&gt; ) not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The IMPLEMENTATION DEFINED contents of the ERR( n )MISC(&lt;m&gt; ) registers contains additional information for an error recorded by this record.</td>
</tr>
</tbody>
</table>

This bit is read/write-one-to-clear.

Note

If the ERR\( n \)MISC\(<m> \) registers can contain additional information for a previously recorded error, then the contents must be self-describing to software or a user. For example, certain fields might relate only to Corrected errors, and other fields only to the most recent error that was not discarded.

On a Cold reset, this field resets to 0.

Otherwise:

Reserved, RES\( 0 \).

CE, bits [25:24]

Corrected Error.

<table>
<thead>
<tr>
<th>CE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No errors were corrected.</td>
</tr>
<tr>
<td>0b01</td>
<td>At least one transient error was corrected.</td>
</tr>
<tr>
<td>0b10</td>
<td>At least one error was corrected.</td>
</tr>
<tr>
<td>0b11</td>
<td>At least one persistent error was corrected.</td>
</tr>
</tbody>
</table>

The mechanism by which a component or node detects whether a correctable error is transient or persistent is IMPLEMENTATION DEFINED. If no such mechanism is implemented, then the node sets this field to 0b10 when a corrected error is recorded.

When clearing ERR\( n \)STATUS.V to 0b0, if this field is nonzero, then Arm recommends that software write ones to this field to clear this field to zero.

This field is not valid and reads UNKNOWN if ERR\( n \)STATUS.V == 0b0.

This field is read/write-ones-to-clear. Writing a value other than all-zeros or all-ones sets this field to an UNKNOWN value.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

DE, bit [23]

Deferred Error.

<table>
<thead>
<tr>
<th>DE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No errors were deferred.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one error was not corrected and deferred.</td>
</tr>
</tbody>
</table>

Support for deferring errors is IMPLEMENTATION DEFINED.

When clearing ERR\( n \)STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads UNKNOWN if ERR\( n \)STATUS.V == 0b0.
This bit is read/write-one-to-clear:
On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**PN, bit [22]**

Poison.

<table>
<thead>
<tr>
<th>PN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Uncorrected error or Deferred error recorded because a corrupt value was detected, for example, by an error detection code (EDC), or Corrected error recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>Uncorrected error or Deferred error recorded because a poison value was detected.</td>
</tr>
</tbody>
</table>

When clearing ERR<\n>STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads **UNKNOWN** if any of the following are true:

- ERR<\n>STATUS.V == 0b0.
- ERR<\n>STATUS.{DE,UE} == {0,0}.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**UET, bits [21:20]**

Uncorrected Error Type. Describes the state of the component after detecting or consuming an Uncorrected error.

<table>
<thead>
<tr>
<th>UET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Uncorrected error; Uncontainable error (UC).</td>
</tr>
<tr>
<td>0b01</td>
<td>Uncorrected error; Unrecoverable error (UE).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncorrected error; Latent or Restartable error (UEO).</td>
</tr>
<tr>
<td>0b11</td>
<td>Uncorrected error; Signaled or Recoverable error (UER).</td>
</tr>
</tbody>
</table>

When clearing ERR<\n>STATUS.V to 0b0, if this field is nonzero, then Arm recommends that software write ones to this field to clear this field to zero.

This field is not valid and reads **UNKNOWN** if any of the following are true:

- ERR<\n>STATUS.V == 0b0.
- ERR<\n>STATUS.UE == 0b0.

This field is read/write-ones-to-clear. Writing a value other than all-zeros or all-ones sets this field to an **UNKNOWN** value.

**Note**

Software might use the information in the error record registers to determine what recovery is necessary.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**CI, bit [19]**

Critical Error. Indicates whether a critical error condition has been recorded.

<table>
<thead>
<tr>
<th>CI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No critical error condition.</td>
</tr>
<tr>
<td>0b1</td>
<td>Critical error condition.</td>
</tr>
</tbody>
</table>

When clearing ERR<\n>STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.
This bit is not valid and reads **UNKNOWN** if ERR<\(n\)>STATUS.V == 0b0.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [18:16]**

Reserved, **RES0**.

**IERR, bits [15:8]**

**IMPLEMENTATION DEFINED** error code. Used with any primary error code ERR<\(n\)>STATUS.SERR value. Further **IMPLEMENTATION DEFINED** information can be placed in the ERR<\(n\)>MISC<\(m\)> registers.

The implemented set of valid values that this field can take is **IMPLEMENTATION DEFINED**. If any value not in this set is written to this register, then the value read back from this field is **UNKNOWN**.

---

**Note**

This means that one or more bits of this field might be implemented as fixed read-as-zero or read-as-one values.

---

This field is not valid and reads **UNKNOWN** if all of the following are true:

- Any of the following are true:
  - The RAS Common Fault Injection Model Extension is implemented by the node that owns this error record and ERR<\(q\)>PFGE.SYN == 0b0.
  - The RAS Common Fault Injection Model Extension is not implemented by the node that owns this error record.
- ERR<\(n\)>STATUS.V == 0b0.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**SERR, bits [7:0]**

Architecturally-defined primary error code. The primary error code might be used by a fault handling agent to triage an error without requiring device-specific code. For example, to count and threshold corrected errors in software, or generate a short log entry.
<table>
<thead>
<tr>
<th>SERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>No error.</td>
</tr>
<tr>
<td>0x01</td>
<td>IMPLEMENTATION DEFINED error.</td>
</tr>
<tr>
<td>0x02</td>
<td>Data value from (non-associative) internal memory. For example, ECC from on-chip SRAM or buffer.</td>
</tr>
<tr>
<td>0x03</td>
<td>IMPLEMENTATION DEFINED pin. For example, nSEI pin.</td>
</tr>
<tr>
<td>0x04</td>
<td>Assertion failure. For example, consistency failure.</td>
</tr>
<tr>
<td>0x05</td>
<td>Error detected on internal data path. For example, parity on ALU result.</td>
</tr>
<tr>
<td>0x06</td>
<td>Data value from associative memory. For example, ECC error on cache data.</td>
</tr>
<tr>
<td>0x07</td>
<td>Address/control value from associative memory. For example, ECC error on cache tag.</td>
</tr>
<tr>
<td>0x08</td>
<td>Data value from a TLB. For example, ECC error on TLB data.</td>
</tr>
<tr>
<td>0x09</td>
<td>Address/control value from a TLB. For example, ECC error on TLB tag.</td>
</tr>
<tr>
<td>0x0A</td>
<td>Data value from producer. For example, parity error on write data bus.</td>
</tr>
<tr>
<td>0x0B</td>
<td>Address/control value from producer. For example, parity error on address bus.</td>
</tr>
<tr>
<td>0x0C</td>
<td>Data value from (non-associative) external memory. For example, ECC error in SDRAM.</td>
</tr>
<tr>
<td>0x0D</td>
<td>Illegal address (software fault). For example, access to unpopulated memory.</td>
</tr>
<tr>
<td>0x0E</td>
<td>Illegal access (software fault). For example, byte write to word register.</td>
</tr>
<tr>
<td>0x0F</td>
<td>Illegal state (software fault). For example, device not ready.</td>
</tr>
<tr>
<td>0x10</td>
<td>Internal data register. For example, parity on a SIMD&amp;FP register. For a PE, all general-purpose, stack pointer, SIMD&amp;FP, and SVE registers are data registers.</td>
</tr>
<tr>
<td>0x11</td>
<td>Internal control register. For example, Parity on a System register. For a PE, all registers other than general-purpose, stack pointer, SIMD&amp;FP, and SVE registers are control registers.</td>
</tr>
<tr>
<td>0x12</td>
<td>Error response from Completer of access. For example, error response from cache write-back.</td>
</tr>
<tr>
<td>0x13</td>
<td>External timeout. For example, timeout on interaction with another component.</td>
</tr>
<tr>
<td>0x14</td>
<td>Internal timeout. For example, timeout on interface within the component.</td>
</tr>
<tr>
<td>0x15</td>
<td>Deferred error from Completer not supported at Requester. For example, poisoned data received from the Completer of an access by a Requester that cannot defer the error further.</td>
</tr>
<tr>
<td>0x16</td>
<td>Deferred error from Requester not supported at Completer. For example, poisoned data received from the Requester of an access by a Completer that cannot defer the error further.</td>
</tr>
<tr>
<td>0x17</td>
<td>Deferred error from Completer passed through. For example, poisoned data received from the Completer of an access and returned to the Requester.</td>
</tr>
<tr>
<td>0x18</td>
<td>Deferred error from Requester passed through. For example, poisoned data received from the Requester of an access and deferred to the Completer.</td>
</tr>
<tr>
<td>0x19</td>
<td>Error recorded by PCIe error logs. Indicates that the component has recorded an error in a PCIe error log. This might be the PCIe device status register, AER, DVSEC, or other mechanisms defined by PCIe.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The implemented set of valid values that this field can take is IMPLEMENTATION DEFINED. If any value not in this set is written to this register, then the value read back from this field is UNKNOWN.

**Note**

This means that one or more bits of this field might be implemented as fixed read-as-zero or read-as-one values.

This field is not valid and reads UNKNOWN if all of the following are true:
Any of the following are true:

- The RAS Common Fault Injection Model Extension is implemented by the node that owns this error record and ERR<n>PFGF.SYN == 0b0.
- The RAS Common Fault Injection Model Extension is not implemented by the node that owns this error record.

ERR<n>STATUS.V == 0b0.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

### When RAS System Architecture v1.0 is implemented:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>AV bit [31]</td>
<td><strong>AV, bit [31]</strong></td>
</tr>
</tbody>
</table>

**When error record <n> includes an address associated with an error:**

- **Address Valid.**

<table>
<thead>
<tr>
<th>AV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;ADDR not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;ADDR contains an address associated with the highest priority error recorded by this record.</td>
</tr>
</tbody>
</table>

This bit ignores writes if ERR<n>STATUS.{CE,DE,UE} != {0b00,0,0}, and the highest priority of these is not being cleared to zero in the same write.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

- **V bit [30]**

**Status Register Valid.**

<table>
<thead>
<tr>
<th>V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;STATUS not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>ERR&lt;n&gt;STATUS valid. At least one error has been recorded.</td>
</tr>
</tbody>
</table>

This bit ignores writes if ERR<n>STATUS.{CE,DE,UE} != {0b00,0,0}, and is not being cleared to 0b0 in the same write.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to 0.

**UE bit [29]**

**Uncorrected Error.**
**ERR<n>STATUS, Error Record Primary Status Register, n = 0 - 65534**

<table>
<thead>
<tr>
<th>UE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No errors have been detected, or all detected errors have been either corrected or deferred.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one detected error was not corrected and not deferred.</td>
</tr>
</tbody>
</table>

When clearing ERR<n>STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads UNKNOWN if ERR<n>STATUS.V == 0b0. This bit ignores writes if ERR<n>STATUS.OF == 0b1 and is not being cleared to 0b0 in the same write.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**ER, bit [28]**

Error Reported.

<table>
<thead>
<tr>
<th>ER</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No in-band error (External Abort) reported.</td>
</tr>
<tr>
<td>0b1</td>
<td>An External Abort was signaled by the component to the Requester making the access or other transaction. This can be because any of the following are true:</td>
</tr>
</tbody>
</table>
  - The applicable one of the ERR<q>CTLR.{WUE,RUE,UE} bits is implemented and was set to 0b1 when an Uncorrected error was detected. |
  - The applicable one of the ERR<q>CTLR.{WUE,RUE,UE} bits is not implemented and the component always reports errors. |

It is IMPLEMENTATION DEFINED whether this bit can be set to 0b1 by a Deferred error.

If this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero, when any of:

- Clearing ERR<n>STATUS.V to 0b0.
- Clearing ERR<n>STATUS.UE to 0b0, if this bit is never set to 0b1 by a Deferred error.
- Clearing ERR<n>STATUS.{UE,DE} to {0,0}, if this bit can be set to 0b1 by a Deferred error.

This bit is not valid and reads UNKNOWN if any of the following are true:

- ERR<n>STATUS.V == 0b0.
- ERR<n>STATUS.UE == 0b0 and this bit is never set to 0b1 by a Deferred error.
- ERR<n>STATUS.{UE,DE} == {0,0} and this bit can be set to 0b1 by a Deferred error.

This bit ignores writes if ERR<n>STATUS.{CE,DE,UE} !={0b00,0,0}, and the highest priority of these is not being cleared to zero in the same write.

This bit is read/write-one-to-clear.

**Note**

An External Abort signaled by the component might be masked and not generate any exception.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**OF, bit [27]**

Overflow.

Indicates that multiple errors have been detected. This bit is set to 0b1 when one of the following occurs:

- An Uncorrected error is detected and ERR<n>STATUS.UE == 0b1.
- A Deferred error is detected, ERR<n>STATUS.UE == 0b0 and ERR<n>STATUS.DE == 0b1.
- A Corrected error is detected, no Corrected error counter is implemented, ERR<n>STATUS.UE == 0b0, ERR<n>STATUS.DE == 0b0, and ERR<n>STATUS.CE != 0b00. ERR<n>STATUS.CE might be updated for the new Corrected error.
A Corrected error counter is implemented, ERR<n>STATUS.UE == 0b0, ERR<n>STATUS.DE == 0b0, and the counter overflows.

It is IMPLEMENTATION DEFINED whether this bit is set to 0b1 when one of the following occurs:

- A Deferred error is detected and ERR<n>STATUS.UE == 0b1.
- A Corrected error is detected, no Corrected error counter is implemented, and either or both the ERR<n>STATUS.UE or ERR<n>STATUS.DE bits are set to 0b1.
- A Corrected error counter is implemented, either or both the ERR<n>STATUS.UE or ERR<n>STATUS.DE bits are set to 0b1, and the counter overflows.

It is IMPLEMENTATION DEFINED whether this bit is cleared to 0b0 when one of the following occurs:

- An Uncorrected error is detected and ERR<n>STATUS.UE == 0b0.
- A Deferred error is detected, ERR<n>STATUS.UE == 0b0 and ERR<n>STATUS.DE == 0b0.
- A Corrected error is detected, ERR<n>STATUS.UE == 0b0, ERR<n>STATUS.DE == 0b0 and ERR<n>STATUS.CE == 0b0.

The IMPLEMENTATION DEFINED clearing of this bit might also depend on the value of the other error status bits.

If a Corrected error counter is implemented:

- A direct write that modifies the counter overflow flag indirectly might set this bit to an UNKNOWN value.
- A direct write to this bit that clears this bit to 0b0 might indirectly set the counter overflow flag to an UNKNOWN value.

<table>
<thead>
<tr>
<th>OF</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0    | If ERR<n>STATUS.UE == 0b1, then no error syndrome for an Uncorrected error has been discarded.  
        |   If ERR<n>STATUS.UE == 0b0 and ERR<n>STATUS.DE == 0b1, then no error syndrome for a Deferred error has been discarded.  
        |   If ERR<n>STATUS.UE == 0b0, ERR<n>STATUS.DE == 0b0, and a Corrected error counter is implemented, then the counter has not overflowed.  
        |   If ERR<n>STATUS.UE == 0b0, ERR<n>STATUS.DE == 0b0, ERR<n>STATUS.CE != 0b00, and no Corrected error counter is implemented, then no error syndrome for a Corrected error has been discarded.  |
| 0b1    | At least one error syndrome has been discarded or, if a Corrected error counter is implemented, it might have overflowed. |

When clearing ERR<n>STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads UNKNOWN if ERR<n>STATUS.V == 0b0.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**MV, bit [26]**

*When error record <n> includes an additional information for an error:*

<table>
<thead>
<tr>
<th>MV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ERR&lt;n&gt;MISC&lt;m&gt; not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The IMPLEMENTATION DEFINED contents of the ERR&lt;n&gt;MISC&lt;m&gt; registers contains additional information for an error recorded by this record.</td>
</tr>
</tbody>
</table>

This bit ignores writes if ERR<n>STATUS.{CE,DE,UE} != \{0b00,0,0\}, and the highest priority of these is not being cleared to zero in the same write.
This bit is read/write-one-to-clear:

**Note**

If the ERR<n>MISC<m> registers can contain additional information for a previously recorded error, then the contents must be self-describing to software or a user. For example, certain fields might relate only to Corrected errors, and other fields only to the most recent error that was not discarded.

On a Cold reset, this field resets to 0.

**Otherwise:**

Reserved, RES0.

**CE, bits [25:24]**

Corrected Error.

<table>
<thead>
<tr>
<th>CE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No errors were corrected.</td>
</tr>
<tr>
<td>0b01</td>
<td>At least one transient error was corrected.</td>
</tr>
<tr>
<td>0b10</td>
<td>At least one error was corrected.</td>
</tr>
<tr>
<td>0b11</td>
<td>At least one persistent error was corrected.</td>
</tr>
</tbody>
</table>

The mechanism by which a component or node detects whether a correctable error is transient or persistent is **IMPLEMENTATION DEFINED**. If no such mechanism is implemented, then the node sets this field to 0b10 when a corrected error is recorded.

When clearing ERR<n>STATUS.V to 0b0, if this field is nonzero, then Arm recommends that software write ones to this field to clear this field to zero.

This field is not valid and reads **UNKNOWN** if ERR<n>STATUS.V == 0b0. This field ignores writes if ERR<n>STATUS.OF == 0b1 and is not being cleared to 0b0 in the same write.

This field is read/write-ones-to-clear. Writing a value other than all-zeros or all-ones sets this field to an **UNKNOWN** value.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**DE, bit [23]**

Deferred Error.

<table>
<thead>
<tr>
<th>DE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No errors were deferred.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one error was not corrected and deferred.</td>
</tr>
</tbody>
</table>

Support for deferring errors is **IMPLEMENTATION DEFINED**.

When clearing ERR<n>STATUS.V to 0b0, if this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero.

This bit is not valid and reads **UNKNOWN** if ERR<n>STATUS.V == 0b0. This bit ignores writes if ERR<n>STATUS.OF == 0b1 and is not being cleared to 0b0 in the same write.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**PN, bit [22]**

Poison.
### PN Meaning

<table>
<thead>
<tr>
<th>PN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Uncorrected error or Deferred error recorded because a corrupt value was detected, for example, by an error detection code (EDC), or Corrected error recorded.</td>
</tr>
<tr>
<td>0b1</td>
<td>Uncorrected error or Deferred error recorded because a poison value was detected.</td>
</tr>
</tbody>
</table>

If this bit is nonzero, then Arm recommends that software write 0b1 to this bit to clear this bit to zero, when any of:

- Clearing ERR<\text{n}>STATUS.V to 0b0.
- Clearing both ERR<\text{n}>STATUS.{DE, UE} to 0b0.

This bit is not valid and reads *UNKNOWN* if any of the following are true:

- ERR<\text{n}>STATUS.V == 0b0.
- ERR<\text{n}>STATUS.{DE,UE} == \{0,0\}.

This bit ignores writes if ERR<\text{n}>STATUS.{CE,DE,UE} != \{0b00,0,0\}, and the highest priority of these is not being cleared to zero in the same write.

This bit is read/write-one-to-clear.

On a Cold reset, this field resets to an architecturally *UNKNOWN* value.

### UET, bits [21:20]

Uncorrected Error Type. Describes the state of the component after detecting or consuming an Uncorrected error.

<table>
<thead>
<tr>
<th>UET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Uncorrected error, Uncontainable error (UC).</td>
</tr>
<tr>
<td>0b01</td>
<td>Uncorrected error, Unrecoverable error (UEU).</td>
</tr>
<tr>
<td>0b10</td>
<td>Uncorrected error, Latent or Restartable error (UEO).</td>
</tr>
<tr>
<td>0b11</td>
<td>Uncorrected error, Signaled or Recoverable error (UER).</td>
</tr>
</tbody>
</table>

If this field is nonzero, then Arm recommends that software write ones to this field to clear this field to zero, when any of:

- Clearing ERR<\text{n}>STATUS.V to 0b0.
- Clearing ERR<\text{n}>STATUS.UE to 0b0.

This field is not valid and reads *UNKNOWN* if any of the following are true:

- ERR<\text{n}>STATUS.V == 0b0.
- ERR<\text{n}>STATUS.UE == 0b0.

This field ignores writes if ERR<\text{n}>STATUS.{CE,DE,UE} != \{0b00,0,0\}, and the highest priority of these is not being cleared to zero in the same write.

This field is read/write-ones-to-clear. Writing a value other than all-zeros or all-ones sets this field to an *UNKNOWN* value.

**Note**

Software might use the information in the error record registers to determine what recovery is necessary.

On a Cold reset, this field resets to an architecturally *UNKNOWN* value.

### Bits [19:16]

Reserved, RES0.

### IERR, bits [15:8]

IMPLEMENTATION DEFINED error code. Used with any primary error code ERR<\text{n}>STATUS.SERR value. Further IMPLEMENTATION DEFINED information can be placed in the ERR<\text{n}>MISC<m> registers.
The implemented set of valid values that this field can take is IMPLEMENTATION DEFINED. If any value not in this set is written to this register, then the value read back from this field is UNKNOWN.

**Note**

This means that one or more bits of this field might be implemented as fixed read-as-zero or read-as-one values.

This field is not valid and reads UNKNOWN if all of the following are true:

- Any of the following are true:
  - The RAS Common Fault Injection Model Extension is implemented by the node that owns this error record and \( \text{ERR<q>PFGF.SYN} == \text{0b0} \).
  - The RAS Common Fault Injection Model Extension is not implemented by the node that owns this error record.
  - \( \text{ERR<n>STATUS.V} == \text{0b0} \).

This field ignores writes if \( \text{ERR<n>STATUS.{CE,DE,UE}} != \{0b00,0,0\} \), and the highest priority of these is not being cleared to zero in the same write.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**SERR, bits [7:0]**

Architecturally-defined primary error code. The primary error code might be used by a fault handling agent to triage an error without requiring device-specific code. For example, to count and threshold corrected errors in software, or generate a short log entry.
<table>
<thead>
<tr>
<th>SERR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>No error.</td>
</tr>
<tr>
<td>0x01</td>
<td>IMPLEMENTATION DEFINED error.</td>
</tr>
<tr>
<td>0x02</td>
<td>Data value from (non-associative) internal memory. For example, ECC from on-chip SRAM or buffer.</td>
</tr>
<tr>
<td>0x03</td>
<td>IMPLEMENTATION DEFINED pin. For example, nSEI pin.</td>
</tr>
<tr>
<td>0x04</td>
<td>Assertion failure. For example, consistency failure.</td>
</tr>
<tr>
<td>0x05</td>
<td>Error detected on internal data path. For example, parity on ALU result.</td>
</tr>
<tr>
<td>0x06</td>
<td>Data value from associative memory. For example, ECC error on cache data.</td>
</tr>
<tr>
<td>0x07</td>
<td>Address/control value from associative memory. For example, ECC error on cache tag.</td>
</tr>
<tr>
<td>0x08</td>
<td>Data value from a TLB. For example, ECC error on TLB data.</td>
</tr>
<tr>
<td>0x09</td>
<td>Address/control value from a TLB. For example, ECC error on TLB tag.</td>
</tr>
<tr>
<td>0x0A</td>
<td>Data value from producer. For example, parity error on write data bus.</td>
</tr>
<tr>
<td>0x0B</td>
<td>Address/control value from producer. For example, parity error on address bus.</td>
</tr>
<tr>
<td>0x0C</td>
<td>Data value from (non-associative) external memory. For example, ECC error in SDRAM.</td>
</tr>
<tr>
<td>0x0D</td>
<td>Illegal address (software fault). For example, access to unpopulated memory.</td>
</tr>
<tr>
<td>0x0E</td>
<td>Illegal access (software fault). For example, byte write to word register.</td>
</tr>
<tr>
<td>0x0F</td>
<td>Illegal state (software fault). For example, device not ready.</td>
</tr>
<tr>
<td>0x10</td>
<td>Internal data register. For example, parity on a SIMD&amp;FP register. For a PE, all general-purpose, stack pointer, SIMD&amp;FP, and SVE registers are data registers.</td>
</tr>
<tr>
<td>0x11</td>
<td>Internal control register. For example, Parity on a System register. For a PE, all registers other than general-purpose, stack pointer, SIMD&amp;FP, and SVE registers are control registers.</td>
</tr>
<tr>
<td>0x12</td>
<td>Error response from Completer of access. For example, error response from cache write-back.</td>
</tr>
<tr>
<td>0x13</td>
<td>External timeout. For example, timeout on interaction with another component.</td>
</tr>
<tr>
<td>0x14</td>
<td>Internal timeout. For example, timeout on interface within the component.</td>
</tr>
<tr>
<td>0x15</td>
<td>Deferred error from Completer not supported at Requester. For example, poisoned data received from the Completer of an access by a Requester that cannot defer the error further.</td>
</tr>
<tr>
<td>0x16</td>
<td>Deferred error from Requester not supported at Completer. For example, poisoned data received from the Requester of an access by a Completer that cannot defer the error further.</td>
</tr>
<tr>
<td>0x17</td>
<td>Deferred error from Completer passed through. For example, poisoned data received from the Completer of an access and returned to the Requester.</td>
</tr>
<tr>
<td>0x18</td>
<td>Deferred error from Requester passed through. For example, poisoned data received from the Requester of an access and deferred to the Completer.</td>
</tr>
<tr>
<td>0x19</td>
<td>Error recorded by PCIe error logs. Indicates that the component has recorded an error in a PCIe error log. This might be the PCIe device status register, AER, DVSEC, or other mechanisms defined by PCIe.</td>
</tr>
</tbody>
</table>

All other values are reserved.

The implemented set of valid values that this field can take is IMPLEMENTATION DEFINED. If any value not in this set is written to this register, then the value read back from this field is UNKNOWN.

**Note**

This means that one or more bits of this field might be implemented as fixed read-as-zero or read-as-one values.

This field is not valid and reads UNKNOWN if all of the following are true:
• Any of the following are true:
  ○ The RAS Common Fault Injection Model Extension is implemented by the node that owns this error record and \( \text{ERR}<q>\text{PFGF}.\text{SYN} == 0b0 \).
  ○ The RAS Common Fault Injection Model Extension is not implemented by the node that owns this error record.
• \( \text{ERR}<n>\text{STATUS}.V == 0b0 \).

This field ignores writes if \( \text{ERR}<n>\text{STATUS.} \{\text{CE,DE,UE}\} != \{0b00,0,0\} \), and the highest priority of these is not being cleared to zero in the same write.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the ERR<sub>n</sub>STATUS**

The \{AV, V, UE, ER, OF, MV, CE, DE, PN, UET, CI\} fields are write-one-to-clear, meaning writes of zero are ignored, and a write of one or all-ones to the field clears the field to zero. The \{IERR, SERR\} fields are read/write fields, although the set of implemented valid values is IMPLEMENTATION DEFINED. See also \( \text{ERR}<n>\text{PFGF}.\text{SYN} \).

After reading \( \text{ERR}<n>\text{STATUS} \), software must clear the valid bits in the register to allow new errors to be recorded. However, between reading the register and clearing the valid bits, a new error might have overwritten the register. To prevent this error being lost by software, the register prevents updates to fields that might have been updated by a new error.

When RAS System Architecture v1.0 is implemented:

• Writes to the \{UE, DE, CE\} fields are ignored if the OF bit is set and is not being cleared.
• Writes to the V bit are ignored if any of the \{UE, DE, CE\} fields are nonzero and are not being cleared.
• Writes to the \{AV, MV\} bits and \{ER, PN, UET, IERR, SERR\} syndrome fields are ignored if the highest priority error status field is nonzero and not being cleared. The error status fields in priority order from highest to lowest, are UE, DE, and CE.

When RAS System Architecture v1.1 is implemented, a write to the register is ignored if all of:

• Any of \{V, UE, OF, CE, DE\} fields are nonzero before the write.
• The write does not clear the nonzero \{V, UE, OF, CE, DE\} fields to zero by writing ones to the applicable field or fields.

Some of the fields in \( \text{ERR}<n>\text{STATUS} \) are also defined as UNKNOWN where certain combinations of the \{V, DE, UE\} status fields are zero. The rules for writes to \( \text{ERR}<n>\text{STATUS} \) allow a node to implement such a field as a fixed read-only value.

For example, when RAS System Architecture v1.1 is implemented, a write to \( \text{ERR}<n>\text{STATUS} \) when \( \text{ERR}<n>\text{STATUS.V} \) is 1 results in either \( \text{ERR}<n>\text{STATUS.V} \) field being cleared to zero, or \( \text{ERR}<n>\text{STATUS.V} \) not changing. Since all fields in \( \text{ERR}<n>\text{STATUS} \), other than \{AV, V, MV\}, usually read as UNKNOWN values when \( \text{ERR}<n>\text{STATUS.V} \) is zero, this means those fields can be implemented as read-only if applicable.

To ensure correct and portable operation, when software is clearing the valid bits in the register to allow new errors to be recorded, Arm recommends that software:

• Determine which fields to clear to zero by reading \( \text{ERR}<n>\text{STATUS} \).
• Write ones to all the write-one-to-clear fields that are nonzero.
• Write zero to all the read/write fields.
• Write zero to all the write-one-to-clear fields that are zero.

Otherwise, these fields might not have the correct value when a new fault is recorded.

An exception is when the node supports writing to these fields as part of fault injection. See also \( \text{ERR}<n>\text{PFGF}.\text{SYN} \).

\( \text{ERR}<n>\text{STATUS} \) can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0x010  + (64 * n)</td>
<td>ERR&lt;n&gt;STATUS</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
ERRPIDR0, Peripheral Identification Register 0

The ERRPIDR0 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRPIDR0 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRPIDR0 is a 32-bit register.

**Field descriptions**

The ERRPIDR0 bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
|        |        |        |        |        |        |        | RES0   |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |
|        |        |        |        |        |        |        | PART_0 |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

**Bits [31:8]**

Reserved, RES0.

**PART_0, bits [7:0]**

Part number, bits [7:0].

The part number is selected by the designer of the component. The designer chooses whether to use a 12-bit or a 16-bit part number:

- If a 12-bit part number is used, it is stored in ERRPIDR1.PART_1 and ERRPIDR0.PART_0. There are 8 bits, ERRPIDR2.REVISION and ERRPIDR3.REVAND, available to define the revision of the component.
- If a 16-bit part number is used, it is stored in ERRPIDR2.PART_2, ERRPIDR1.PART_1 and ERRPIDR0.PART_0. There are 4 bits, ERRPIDR3.REVISION, available to define the revision of the component.

This field reads as an **IMPLEMENTATION DEFINED** value.

**Accessing the ERRPIDR0**

**ERRPIDR0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFE0</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The ERRPIDR1 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is *optional*.

ERRPIDR1 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRPIDR1 is a 32-bit register.

**Field descriptions**

The ERRPIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>Designer, JEP106 identification code, bits [3:0]. ERRPIDR1.DES_0 and ERRPIDR2.DES_1 together form the JEDEC-assigned JEP106 identification code for the designer of the component. The parity bit in the JEP106 identification code is not included. The code identifies the designer of the component, which might not be not the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC <a href="http://www.jedec.org">http://www.jedec.org</a>. This field reads as an IMPLEMENTATION DEFINED value.</td>
</tr>
<tr>
<td>29</td>
<td>Part number, bits [11:8]. The part number is selected by the designer of the component. The designer chooses whether to use a 12-bit or a 16-bit part number:</td>
</tr>
<tr>
<td>28</td>
<td>• If a 12-bit part number is used, it is stored in ERRPIDR1.PART_1 and ERRPIDR0.PART_0. There are 8 bits, ERRPIDR2.REVISION and ERRPIDR3.REVAND, available to define the revision of the component.</td>
</tr>
<tr>
<td>27</td>
<td>• If a 16-bit part number is used, it is stored in ERRPIDR2.PART_2, ERRPIDR1.PART_1 and ERRPIDR0.PART_0. There are 4 bits, ERRPIDR3.REVISION, available to define the revision of the component.</td>
</tr>
</tbody>
</table>

**Note**

For a component designed by Arm Limited, the JEP106 identification code is 0x3B.
This field reads as an IMPLEMENTATION DEFINED value.

**Accessing the ERRPIDR1**

ERRPIDR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFE4</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
**ERRPIDR2, Peripheral Identification Register 2**

The ERRPIDR2 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRPIDR2 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRPIDR2 is a 32-bit register.

**Field descriptions**

The ERRPIDR2 bit assignments are:

**When the component uses a 12-bit part number:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>...</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>REVISION</td>
</tr>
<tr>
<td>6</td>
<td>JEDEC</td>
</tr>
<tr>
<td>5</td>
<td>DES_1</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**REVISION, bits [7:4]**

Component major revision. ERRPIDR2.REVISION and ERRPIDR3.REVAND together form the revision number of the component, with ERRPIDR2.REVISION being the most significant part and ERRPIDR3.REVAND the least significant part. When a component is changed, ERRPIDR2.REVISION or ERRPIDR3.REVAND are increased to ensure that software can differentiate the different revisions of the component. If ERRPIDR2.REVISION is increased then ERRPIDR3.REVAND should be set to 0b0000.

This field reads as an **IMPLEMENTATION DEFINED** value.

**JEDEC, bit [3]**

JEDEC-assigned JEP106 implementer code is used.

Reads as 0b1.

**DES_1, bits [2:0]**

Designer, JEP106 identification code, bits [6:4]. ERRPIDR1.DES_0 and ERRPIDR2.DES_1 together form the JEDEC-assigned JEP106 identification code for the designer of the component. The parity bit in the JEP106 identification code is not included. The code identifies the designer of the component, which might not be not the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC http://www.jedec.org.
This field reads as an IMPLEMENTATION DEFINED value.

**Note**

For a component designed by Arm Limited, the JEP106 identification code is 0x3B.

**When the component uses a 16-bit part number:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>PART_2</td>
<td>JEDEC</td>
<td>DES_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PART_2, bits [7:4]**

Part number, bits [15:12].

The part number is selected by the designer of the component. The designer chooses whether to use a 12-bit or a 16-bit part number:

- If a 12-bit part number is used, it is stored in `ERRPIDR1.PART_1` and `ERRPIDR0.PART_0`. There are 8 bits, `ERRPIDR2.REVISION` and `ERRPIDR3.REVAND`, available to define the revision of the component.
- If a 16-bit part number is used, it is stored in `ERRPIDR2.PART_2`, `ERRPIDR1.PART_1` and `ERRPIDR0.PART_0`. There are 4 bits, `ERRPIDR3.REVISION`, available to define the revision of the component.

This field reads as an IMPLEMENTATION DEFINED value.

**JEDEC, bit [3]**

JEDEC-assigned JEP106 implementer code is used.

Reads as 0b1.

**DES_1, bits [2:0]**

Designer JEP106 identification code, bits [6:4]. `ERRPIDR1.DES_0` and `ERRPIDR2.DES_1` together form the JEDEC-assigned JEP106 identification code for the designer of the component. The parity bit in the JEP106 identification code is not included. The code identifies the designer of the component, which might not be the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC http://www.jedec.org.

This field reads as an IMPLEMENTATION DEFINED value.

**Note**

For a component designed by Arm Limited, the JEP106 identification code is 0x3B.

**Accessing the ERRPIDR2**

ERRPIDR2 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFE8</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERRPIDR3, Peripheral Identification Register 3

The ERRPIDR3 characteristics are:

**Purpose**

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

ERRPIDR3 is implemented only as part of a memory-mapped group of error records.

**Attributes**

ERRPIDR3 is a 32-bit register.

**Field descriptions**

The ERRPIDR3 bit assignments are:

**When the component uses a 12-bit part number:**

|   | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 |  9 |  8 |  7 |  6 |  5 |  4 |  3 |  2 |  1 |  0 |
|---|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|   | RES0 | REVAND | CMOD |

**Bits [31:8]**

Reserved, RES0.

**REVAND, bits [7:4]**

Component minor revision. ERRPIDR2.REVISION and ERRPIDR3.REVAND together form the revision number of the component, with ERRPIDR2.REVISION being the most significant part and ERRPIDR3.REVAND the least significant part. When a component is changed, ERRPIDR2.REVISION or ERRPIDR3.REVAND are increased to ensure that software can differentiate the different revisions of the component. If ERRPIDR2.REVISION is increased then ERRPIDR3.REVAND should be set to 0b0000.

This field reads as an **IMPLEMENTATION DEFINED** value.

**CMOD, bits [3:0]**

Customer Modified.

Indicates the component has been modified.

A value of 0b0000 means the component is not modified from the original design.

Any other value means the component has been modified in an **IMPLEMENTATION DEFINED** way.

For any two components with the same Unique Component Identifier:

- If the value of the CMOD fields of both components equals zero, the components are identical.
- If the CMOD fields of both components have the same non-zero value, it does not necessarily mean that they have the same modifications.
If the value of the CMOD field of either of the two components is non-zero, they might not be identical, even though they have the same Unique Component Identifier. This field reads as an IMPLEMENTATION DEFINED value.

**When the component uses a 16-bit part number:**

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | CMOD |

**Bits [31:8]**

Reserved, RES0.

**REVISION, bits [7:4]**

Component revision. When a component is changed, ERRPIDR3.REVISION is increased to ensure that software can differentiate the different revisions of the component. This field reads as an IMPLEMENTATION DEFINED value.

**CMOD, bits [3:0]**

Customer Modified.

Indicates the component has been modified.

A value of 0b0000 means the component is not modified from the original design.

Any other value means the component has been modified in an IMPLEMENTATION DEFINED way.

For any two components with the same Unique Component Identifier:

- If the value of the CMOD fields of both components equals zero, the components are identical.
- If the CMOD fields of both components have the same non-zero value, it does not necessarily mean that they have the same modifications.
- If the value of the CMOD field of either of the two components is non-zero, they might not be identical, even though they have the same Unique Component Identifier.

This field reads as an IMPLEMENTATION DEFINED value.

**Accessing the ERRPIDR3**

**ERRPIDR3 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFEC</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
ERRPIDR4, Peripheral Identification Register 4

The ERRPIDR4 characteristics are:

Purpose

Provides discovery information about the component.

For more information, see 'About the Peripheral identification scheme'.

Configuration

Implementation of this register is OPTIONAL.

ERRPIDR4 is implemented only as part of a memory-mapped group of error records.

Attributes

ERRPIDR4 is a 32-bit register.

Field descriptions

The ERRPIDR4 bit assignments are:

<table>
<thead>
<tr>
<th>Bit positions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>RES0, SIZE, DES_2</td>
</tr>
</tbody>
</table>

Bits [31:8]

Reserved, RES0.

SIZE, bits [7:4]

Size of the component.

The distance from the start of the address space used by this component to the end of the component identification registers.

A value of 0b0000 means one of the following is true:

- The component uses a single 4KB block.
- The component uses an IMPLEMENTATION DEFINED number of 4KB blocks.

Any other value means the component occupies $2^\text{ERRPIDR4.SIZE}$ 4KB blocks.

Using this field to indicate the size of the component is deprecated. This field might not correctly indicate the size of the component. Arm recommends that software determine the size of the component from the Unique Component Identifier fields, and other IMPLEMENTATION DEFINED registers in the component.

This field reads as an IMPLEMENTATION DEFINED value.

DES_2, bits [3:0]

Designer, JEP106 continuation code. This is the JEDEC-assigned JEP106 bank identifier for the designer of the component, minus 1. The code identifies the designer of the component, which might not be not the same as the implementer of the device containing the component. To obtain a number, or to see the assignment of these codes, contact JEDEC http://www.jedec.org.

This field reads as an IMPLEMENTATION DEFINED value.
Note

For a component designed by Arm Limited, the JEP106 bank is 5, meaning this field has the value 0x4.

Accessing the ERRPIDR4

ERRPIDR4 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAS</td>
<td>0xFD0</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
GICC_ABPR, CPU Interface Aliased Binary Point Register

The GICC_ABPR characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption.

**Configuration**

The reset value of this register is defined as \( \text{minimum GICC_BPR.Binary_Point + 1} \), resulting in a permitted range of \( 0x1-0x4 \).

In systems that support two Security states:

- This register is an alias of the Non-secure copy of GICC_BPR.
- Non-secure accesses to this register return a shifted value of the binary point.
- If ICC_CTLR_EL3.CBPR_EL1NS == 1, Secure accesses to this register access ICC_BPR0_EL1.

**Attributes**

GICC_ABPR is a 32-bit register.

**Field descriptions**

The GICC_ABPR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2-0</td>
<td>Binary_Point</td>
</tr>
</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**Binary_Point, bits [2:0]**

Controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. The following list describes how this field determines the interrupt priority bits assigned to the group priority field:

- Secure ICC_BPR1_EL1 Binary Point when CBPR == 0' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069), for the processing of Group 1 interrupts in a GIC implementation that supports interrupt grouping, when GICC_CTLR.CBPR == 0.
- Non-secure ICC_BPR1_EL1 Binary Point when CBPR == 0' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069), for all other cases.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICC_ABPR**

This register is used only when System register access is not enabled. When System register access is enabled, the System registers ICC_BPR0_EL1 and ICC_BPR1_EL1 provide equivalent functionality.
GICC_ABPR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x001C</td>
<td>GICC_ABPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICC_AEOIR characteristics are:

**Purpose**

A write to this register performs priority drop for the specified Group 1 interrupt and, if the appropriate `GICC_CTLR.EOImodeS` or `GICC_CTLR.EOImodeNS` field == 0, also deactivates the interrupt.

**Configuration**

When `GICD_CTLR.DS==0`, this register is an alias of the Non-secure view of `GICC_EOIR`. A Secure access to this register is identical to a Non-secure access to `GICC_EOIR`.

**Attributes**

GICC_AEOIR is a 32-bit register.

**Field descriptions**

The GICC_AEOIR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>INTID</td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

**Accessing the GICC_AEOIR**

A write to this register must correspond to the most recently acknowledged Group 1 interrupt. If a value other than the last value read from `GICC_AIAR` is written to this register, the effect is UNPREDICTABLE.

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICC_EOIR1` provides equivalent functionality.
- For AArch64 implementations, `ICC_EOIR1_EL1` provides equivalent functionality.
When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_AEOIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0024</td>
<td>GICC_AEOIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRL.RS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
The GICC_AHPPIR characteristics are:

### Purpose

If the highest priority pending interrupt is in Group 1, this register provides the INTID of the highest priority pending interrupt on the CPU interface.

### Configuration

If `GICD_CTLR.DS==0`, this register is an alias of the Non-secure view of `GICC_HPPIR`. A Secure access to this register is identical to a Non-secure access to `GICC_HPPIR`.

### Attributes

GICC_AHPPIR is a 32-bit register.

### Field descriptions

The GICC_AHPPIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RE0 | INTID |

**Bits [31:24]**

Reserved, RE0.

**INTID, bits [23:0]**

The INTID of the signalled interrupt.

#### Note

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RE0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RE0.

### Accessing the GICC_AHPPIR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICC_HPPIR1` provides equivalent functionality.
- For AArch64 implementations, `ICC_HPPIR1_EL1` provides equivalent functionality.

If the highest priority pending interrupt is in Group 0, a read of this register returns the special INTID 1023.

Interrupt identifiers corresponding to an interrupt group that is not enabled are ignored.
If the highest priority pending interrupt is a direct interrupt that is both individually enabled in the Distributor and part of an interrupt group that is enabled in the Distributor, and the interrupt group is disabled in the CPU interface for this PE, this register returns the special INTID 1023.

For more information about pending interrupts that are not considered when determining the highest priority pending interrupt, see 'Preemption' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_AHPPIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0028</td>
<td>GICC_AHPPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GICC_AIAR, CPU Interface Aliased Interrupt Acknowledge Register

The GICC_AIAR characteristics are:

**Purpose**

Provides the INTID of the signaled Group 1 interrupt. A read of this register by the PE acts as an acknowledge for the interrupt.

**Configuration**

When **GICD_CTLR.DS==0**, this register is an alias of the Non-secure view of **GICC_IAR**. A Secure access to this register is identical to a Non-secure access to **GICC_IAR**.

**Attributes**

GICC_AIAR is a 32-bit register.

**Field descriptions**

The GICC_AIAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>RES0</td>
</tr>
<tr>
<td>28</td>
<td>RES0</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>RES0</td>
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<tr>
<td>25</td>
<td>RES0</td>
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<tr>
<td>24</td>
<td>RES0</td>
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<td>23</td>
<td>RES0</td>
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<td>22</td>
<td>RES0</td>
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<td>21</td>
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<td>20</td>
<td>RES0</td>
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<td>18</td>
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<td>14</td>
<td>RES0</td>
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<td>13</td>
<td>RES0</td>
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<td>12</td>
<td>RES0</td>
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<tr>
<td>11</td>
<td>RES0</td>
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<tr>
<td>10</td>
<td>RES0</td>
</tr>
<tr>
<td>9</td>
<td>INTID</td>
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<tr>
<td>8</td>
<td>INTID</td>
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<tr>
<td>7</td>
<td>INTID</td>
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<td>6</td>
<td>INTID</td>
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<td>5</td>
<td>INTID</td>
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<tr>
<td>4</td>
<td>INTID</td>
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<tr>
<td>3</td>
<td>INTID</td>
</tr>
<tr>
<td>2</td>
<td>INTID</td>
</tr>
<tr>
<td>1</td>
<td>INTID</td>
</tr>
<tr>
<td>0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

**Accessing the GICC_AIAR**

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_AIAR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

Page 3621
This interface is accessible as follows:

- When GICD CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GICC_APR<n>, CPU Interface Active Priorities Registers, n = 0 - 3

The GICC_APR<n> characteristics are:

**Purpose**

Provides information about interrupt active priorities.

**Configuration**

The contents of these registers are **IMPLEMENTATION DEFINED** with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

When GICD_CTLR_DS == 0, these registers are Banked, and Non-secure accesses do not affect Secure operation. The Secure copies of these registers hold active priorities for Group 0 interrupts, and the Non-secure copies provide a Non-secure view of the active priorities for Group 1 interrupts.

GICC_APR1 is only implemented in implementations that support 6 or more bits of priority. GICC_APR2 and GICC_APR3 are only implemented in implementations that support 7 bits of priority.

When GICD_CTLR_DS==1, these registers hold the active priorities for Group 0 interrupts, and the active priorities for Group 1 interrupts are held by the GICC_NSAPR<n> registers.

**Attributes**

GICC_APR<n> is a 32-bit register.

**Field descriptions**

The GICC_APR<n> bit assignments are:

|   31  |  30  |  29  |  28  |  27  |  26  |  25  |  24  |  23  |  22  |  21  |  20  |  19  |  18  |  17  |  16  |  15  |  14  |  13  |  12  |  11  |  10  |  9   |  8   |  7   |  6   |  5   |  4   |  3   |  2   |  1   |  0   |
|-------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|------|
|       |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |      |

**IMPLEMENTATION DEFINED,** bits [31:0]

**IMPLEMENTATION DEFINED.**

On a Warm reset, this field resets to 0.

**Accessing the GICC_APR<n>**

These registers are used only when System register access is not enabled. When System register access is enabled the following registers provide equivalent functionality:

- In AArch64:
  - For Group 0, ICC_AP0R<n>_EL1.
  - For Group 1, ICC_AP1R<n>_EL1.
- In AArch32:
  - For Group 0, ICC_AP0R<n>.
  - For Group 1, ICC_AP1R<n>.

GICC_APR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

Page 3623
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are \textbf{RW}.
- When an access is Secure accesses to this register are \textbf{RW}.
- When an access is Non-secure accesses to this register are \textbf{RW}.
**GICC_BPR, CPU Interface Binary Point Register**

The GICC_BPR characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field.

**Configuration**

In systems that support two Security states:

- This register is Banked.
- The Secure instance of this register determines Group 0 interrupt preemption.
- The Non-secure instance of this register determines Group 1 interrupt preemption.

In systems that support only one Security state, when `GICC_CTLR.CBPR == 0`, this register determines only Group 0 interrupt preemption.

When `GICC_CTLR.CBPR == 1`, this register determines interrupt preemption for both Group 0 and Group 1 interrupts.

**Attributes**

GICC_BPR is a 32-bit register.

**Field descriptions**

The GICC_BPR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
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<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Binary_Point</td>
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</tbody>
</table>

**Bits [31:3]**

Reserved, RES0.

**Binary_Point, bits [2:0]**

Controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field. The following list describes how this field determines the interrupt priority bits assigned to the group priority field:

- 'Secure ICC_BPR1_EL1 Binary Point when CBPR == 0' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069), for the processing of Group 1 interrupts in a GIC implementation that supports interrupt grouping, when `GICC_CTLR.CBPR == 0`.
- 'Non-secure ICC_BPR1_EL1 Binary Point when CBPR == 0' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069), for all other cases.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Note**

Aliasing the Non-secure GICC_BPR as `GICC_ABPR` in a multiprocessor system permits a PE that can make only Secure accesses to configure the preemption setting for Group 1 interrupts by accessing `GICC_ABPR`. 
Accessing the GICC_BPR

This register is used only when System register access is not enabled. When System register access is enabled this register is RAZ/WI, and the System registers ICC_BPR0_EL1 and ICC_BPR1_EL1 provide equivalent functionality.

GICC_BPR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0008</td>
<td>GICC_BPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICC_CTLR, CPU Interface Control Register

The GICC_CTLR characteristics are:

**Purpose**

Controls the CPU interface, including enabling of interrupt groups, interrupt signal bypass, binary point registers used, and separation of priority drop and interrupt deactivation.

---

**Note**

If the GIC implementation supports two Security states, independent EOI controls are provided for accesses from each Security state. Secure accesses handle both Group 0 and Group 1 interrupts, and Non-secure accesses handle Group 1 interrupts only.

---

**Configuration**

In a GIC implementation that supports two Security states:

- This register is Banked.
- The register bit assignments are different in the Secure and Non-secure copies.

**Attributes**

GICC_CTLR is a 32-bit register.

**Field descriptions**

The GICC_CTLR bit assignments are:

When GICD_CTLR.DS==0, Non-secure access:

<table>
<thead>
<tr>
<th>Bits</th>
<th>RES0</th>
<th>EOImodeNS</th>
<th>RES0</th>
<th>IRQBypDisGrp1</th>
<th>FIQBypDisGrp1</th>
<th>RES0</th>
<th>EnableGrp1</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
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<td>30</td>
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<td>EOImodeNS</td>
<td>RES0</td>
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<td>RES0</td>
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<tr>
<td>29</td>
<td></td>
<td>RES0</td>
<td>RQBypDisGrp1</td>
<td></td>
<td></td>
<td>RES0</td>
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<td>28</td>
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<td>FIQBypDisGrp1</td>
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<td>RES0</td>
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<td>RES0</td>
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<tr>
<td>0</td>
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</tr>
</tbody>
</table>

**Bits [31:10]**

Reserved, RES0.

**EOImodeNS, bit [9]**

Controls the behavior of Non-secure accesses to `GICC_EOIR`, `GICC_AEOIR`, and `GICC_DIR`.

<table>
<thead>
<tr>
<th>EOImodeNS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>GICC_EOIR</code> and <code>GICC_AEOIR</code> provide both priority drop and interrupt deactivation functionality. Accesses to <code>GICC_DIR</code> are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>GICC_EOIR</code> and <code>GICC_AEOIR</code> provide priority drop functionality only. <code>GICC_DIR</code> provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

---

**Note**

An implementation is permitted to make this bit RAO/WI.
On a Warm reset, this field resets to 0.

**Bits [8:7]**

Reserved, RES0.

**IRQBypDisGrp1, bit [6]**

When the signaling of IRQs by the CPU interface is disabled, this field partly controls whether the bypass IRQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>IRQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass IRQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass IRQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DIB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see 'Interrupt bypass support' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

**FIQBypDisGrp1, bit [5]**

When the signaling of FIQs by the CPU interface is disabled, this field partly controls whether the bypass FIQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>FIQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass FIQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass FIQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DFB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see 'Interrupt bypass support' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

**Bits [4:1]**

Reserved, RES0.

**EnableGrp1, bit [0]**

This Non-secure field enables the signaling of Group 1 interrupts by the CPU interface to a target PE:

<table>
<thead>
<tr>
<th>EnableGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupt signaling is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupt signaling is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**When GICD_CTLR.DS==0, Secure access:**

<table>
<thead>
<tr>
<th>Address</th>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>310292827262524232221201918171615143121</td>
<td>31-0</td>
<td>RES0&gt;E0ImodeNS&gt;E0ImodeS&gt;IRQBypDisGrp1&gt;FIQBypDisGrp1&gt;IRQBypDisGrp0&gt;FIQBypDisGrp0</td>
</tr>
</tbody>
</table>

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Bits [31:11]

Reserved, RES0.

EOImodeNS, bit [10]

Controls the behavior of Non-secure accesses to GICC_EOIR, GICC_AEOIR, and GICC_DIR.

<table>
<thead>
<tr>
<th>EOImodeNS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICC_EOIR and GICC_AEOIR provide both priority drop and interrupt deactivation functionality. Accesses to GICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICC_EOIR and GICC_AEOIR provide priority drop functionality only. GICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

Note

An implementation is permitted to make this bit RAO/WI.

On a Warm reset, this field resets to 0.

EOImodeS, bit [9]

Controls the behavior of Secure accesses to GICC_EOIR, GICC_AEOIR, and GICC_DIR.

<table>
<thead>
<tr>
<th>EOImodeS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICC_EOIR and GICC_AEOIR provide both priority drop and interrupt deactivation functionality. Accesses to GICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICC_EOIR and GICC_AEOIR provide priority drop functionality only. GICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

Note

An implementation is permitted to make this bit RAO/WI.

This field shares state with GICC_CTLR.EOImode.

On a Warm reset, this field resets to 0.

IRQBypDisGrp1, bit [8]

When the signaling of IRQs by the CPU interface is disabled, this field partly controls whether the bypass IRQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>IRQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass IRQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass IRQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DIB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see 'Interrupt bypass support' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.
FIQBypDisGrp1, bit [7]

When the signaling of FIQs by the CPU interface is disabled, this field partly controls whether the bypass FIQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>FIQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass FIQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass FIQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and `ICC_SRE_EL3.DFB` == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see ‘Interrupt bypass support’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

IRQBypDisGrp0, bit [6]

When the signaling of IRQs by the CPU interface is disabled, this field partly controls whether the bypass IRQ signal is signaled to the PE for Group 0:

<table>
<thead>
<tr>
<th>IRQBypDisGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass IRQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass IRQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and `ICC_SRE_EL3.DIB` == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see ‘Interrupt bypass support’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

FIQBypDisGrp0, bit [5]

When the signaling of FIQs by the CPU interface is disabled, this field partly controls whether the bypass FIQ signal is signaled to the PE for Group 0:

<table>
<thead>
<tr>
<th>FIQBypDisGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass FIQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass FIQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and `ICC_SRE_EL3.DIB` == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see ‘Interrupt bypass support’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

CBPR, bit [4]

Controls whether `GICC_BPR` provides common control of preemption to Group 0 and Group 1 interrupts:
CBPR | Meaning
---|---
0b0 | GICC_BPR determines preemption for Group 0 interrupts only.
0b1 | GICC_BPR determines preemption for both Group 0 and Group 1 interrupts.

This field is an alias of ICC_CTRLR_EL3.CBPR_EL1NS.

In a GIC that supports two Security states, when CBPR == 1:

- A Non-secure read of GICC_BPR returns the value of Secure GICC_BPR.Binary_Point, incremented by 1, and saturated to 0b111.
- Non-secure writes of GICC_BPR are ignored.

On a Warm reset, this field resets to 0.

**FIQEn, bit [3]**

Controls whether the CPU interface signals Group 0 interrupts to a target PE using the FIQ or IRQ signal:

<table>
<thead>
<tr>
<th>FIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupts are signaled using the IRQ signal.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupts are signaled using the FIQ signal.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Bit [2]**

Reserved, RES0.

**EnableGrp1, bit [1]**

This Non-secure field enables the signaling of Group 1 interrupts by the CPU interface to a target PE:

<table>
<thead>
<tr>
<th>EnableGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupt signaling is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupt signaling is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**EnableGrp0, bit [0]**

Enables the signaling of Group 0 interrupts by the CPU interface to a target PE:

<table>
<thead>
<tr>
<th>EnableGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupt signaling is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupt signaling is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**When GICD_CTRLR.DS == 1:**

<table>
<thead>
<tr>
<th>RES0</th>
<th>EOLmode</th>
<th>RQByDisGrp1</th>
<th>FIQByDisGrp1</th>
<th>RQByDisGrp0</th>
<th>FIQByDisGrp0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31302928272625242322212019181716151413121110</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:10]**

Reserved, RES0.
EOImode, bit [9]

Controls the behavior of accesses to GICC_EOIR, GICC_AEOIR, and GICC_DIR.

<table>
<thead>
<tr>
<th>EOImode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICC_EOIR and GICC_AEOIR provide both priority drop and interrupt deactivation functionality. Accesses to GICC_DIR are UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICC_EOIR and GICC_AEOIR provide priority drop functionality only. GICC_DIR provides interrupt deactivation functionality.</td>
</tr>
</tbody>
</table>

Note

An implementation is permitted to make this bit RAO/WI.

This field shares state with GICC_CTLR EOimodeS.

On a Warm reset, this field resets to 0.

IRQBypDisGrp1, bit [8]

When the signaling of IRQs by the CPU interface is disabled, this field partly controls whether the bypass IRQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>IRQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass IRQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass IRQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DIB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see ‘Interrupt bypass support’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

FIQBypDisGrp1, bit [7]

When the signaling of FIQs by the CPU interface is disabled, this field partly controls whether the bypass FIQ signal is signaled to the PE for Group 1:

<table>
<thead>
<tr>
<th>FIQBypDisGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass FIQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass FIQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DFB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see ‘Interrupt bypass support’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

IRQBypDisGrp0, bit [6]

When the signaling of IRQs by the CPU interface is disabled, this field partly controls whether the bypass IRQ signal is signaled to the PE for Group 0:
###IRQBypDisGrp0, bit [0]

<table>
<thead>
<tr>
<th>IRQBypDisGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass IRQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass IRQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DIB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see 'Interrupt bypass support' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

###FIQBypDisGrp0, bit [5]

When the signaling of FIQs by the CPU interface is disabled, this field partly controls whether the bypass FIQ signal is signaled to the PE for Group 0:

<table>
<thead>
<tr>
<th>FIQBypDisGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bypass FIQ signal is signaled to the PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bypass FIQ signal is not signaled to the PE.</td>
</tr>
</tbody>
</table>

If System register access is enabled for EL3 and ICC_SRE_EL3.DIB == 1, this field is RAO/WI.

If System register access is enabled for EL1, this field is ignored.

If an implementation does not support legacy interrupts, this bit is permitted to be RAO/WI.

For more information, see 'Interrupt bypass support' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

###CBPR, bit [4]

Controls whether GICC_BPR provides common control of preemption to Group 0 and Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICC_BPR determines preemption for Group 0 interrupts only.</td>
</tr>
<tr>
<td></td>
<td>GICC_ABPR determines preemption for Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICC_BPR determines preemption for both Group 0 and Group 1 interrupts.</td>
</tr>
</tbody>
</table>

This field is an alias of ICC_CTLR_EL3.CBPR_EL1NS.

In a GIC that supports two Security states, when CBPR == 1:

- A Non-secure read of GICC_BPR returns the value of Secure GICC_BPR.Binary_Point, incremented by 1, and saturated to 0b111.
- Non-secure writes of GICC_BPR are ignored.

On a Warm reset, this field resets to 0.

###FIQEn, bit [3]

Controls whether the CPU interface signals Group 0 interrupts to a target PE using the FIQ or IRQ signal:

<table>
<thead>
<tr>
<th>FIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupts are signaled using the IRQ signal.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupts are signaled using the FIQ signal.</td>
</tr>
</tbody>
</table>

Group 1 interrupts are signaled using the IRQ signal only.

If an implementation supports two Security states, this bit is permitted to be RAO/WI.

On a Warm reset, this field resets to 0.
Bit [2]

Reserved, RES0.

EnableGrp1, bit [1]

This Non-secure field enables the signaling of Group 1 interrupts by the CPU interface to a target PE:

<table>
<thead>
<tr>
<th>EnableGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupt signaling is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupt signaling is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

EnableGrp0, bit [0]

Enables the signaling of Group 0 interrupts by the CPU interface to a target PE:

<table>
<thead>
<tr>
<th>EnableGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupt signaling is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupt signaling is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Accessing the GICC_CTLR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_CTLR and ICC_MCTLR provide equivalent functionality.
- For AArch64 implementations, ICC_CTLR_EL1 and ICC_CTLR_EL3 provide equivalent functionality.

GICC_CTLR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0000</td>
<td>GICC_CTLR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICC_DIR, CPU Interface Deactivate Interrupt Register

The GICC_DIR characteristics are:

Purpose

When interrupt priority drop is separated from interrupt deactivation, a write to this register deactivates the specified interrupt.

Configuration

Attributes

GICC_DIR is a 32-bit register.

Field descriptions

The GICC_DIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

Bits [31:24]

Reserved, RES0.

INTID, bits [23:0]

The INTID of the signaled interrupt.

Note

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

Accessing the GICC_DIR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_DIR provides equivalent functionality.
- For AArch64 implementations, ICC_DIR_EL1 provides equivalent functionality.

Writes to this register have an effect only in the following cases:

- When GICD_CTLR.DS == 1, if GICC_CTLR.EOImode == 1.
- In GIC implementations that support two Security states:
  - If the access is Secure and GICC_CTLR.EOImodeS == 1.
  - If the access is Non-secure and GICC_CTLR.EOImodeNS == 1.

The following writes must be ignored:
• Writes to this register when the corresponding EOImode field in GICC_CTLR == 0. In systems that support system error generation, an implementation might generate a system error.
• Writes to this register when the corresponding EOImode field in GICC_CTLR == 0 and the corresponding interrupt is not active. In systems that support system error generation, an implementation might generate a system error. In implementations using the GIC Stream Protocol Interface, these writes correspond to a Deactivate packet for an interrupt that is not active. For more information, see 'Deactivate (ICC)' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

If the corresponding EOImode field in GICC_CTLR is 1 and this register is written to without a corresponding write to GICC_EOIR or GICC_AEOIR, the interrupt is deactivated but the bit corresponding to it in the active priorities registers remains set.

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_DIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x1000</td>
<td>GICC_DIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When GICD_CTLR.DS == 0 accesses to this register are **WO**.
• When an access is Secure accesses to this register are **WO**.
• When an access is Non-secure accesses to this register are **WO**.
GICC_EOIR, CPU Interface End Of Interrupt Register

The GICC_EOIR characteristics are:

Purpose

A write to this register performs priority drop for the specified interrupt and, if the appropriate GICC_CTLR.EOiModeS or GICC_CTLR.EOiModeNS field == 0, also deactivates the interrupt.

Configuration

If GICD_CTLR.DS==0:

- This register is Common.
- GICC_AEOIR is an alias of the Non-secure view of this register.

For Secure writes when GICD_CTLR.DS==0, or for Secure and Non-secure writes when GICD_CTLR.DS==1, the register provides functionality for Group 0 interrupts.

For Non-secure writes when GICD_CTLR.DS==1, the register provides functionality for Group 1 interrupts.

Attributes

GICC_EOIR is a 32-bit register.

Field descriptions

The GICC_EOIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

Bits [31:24]

Reserved, RES0.

INTID, bits [23:0]

The INTID of the signaled interrupt.

Note

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

For every read of a valid INTID from GICC_IAR, the connected PE must perform a matching write to GICC_EOIR. The value written to GICC_EOIR must be the INTID from GICC_IAR. Reads of INTIDs 1020-1023 do not require matching writes.

Note
Arm recommends that software preserves the entire register value read from GICC_IAR, and writes that value back to GICC_EOIR on completion of interrupt processing.

For nested interrupts, the order of writes to this register must be the reverse of the order of interrupt acknowledgement. Behavior is UNPREDICTABLE if:

- This ordering constraint is not maintained.
- The value written to this register does not match an active interrupt, or the ID of a spurious interrupt.
- The value written to this register does not match the last valid interrupt value read from GICC_IAR.

For general information about the effect of writes to end of interrupt registers, and about the possible separation of the priority drop and interrupt deactivate operations, see 'Interrupt lifecycle' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

If GICC_CTLR.EOImodeS == 0:

- GICC_CTLR.EOImodeS controls the behavior of Secure accesses to GICC_EOIR and GICC_AEOIR.
- GICC_CTLR.EOImodeNS controls the behavior of Non-secure accesses to GICC_EOIR and GICC_AEOIR.

Accessing the GICC_EOIR

The following writes must be ignored:

- Writes of INTIDs 1020-1023.
- Secure writes corresponding to Group 1 interrupts. In systems that support system error generation, an implementation might generate a system error. In this case, GIC behavior is predictable, and the highest Secure active priority (in the Secure copy of GICC_APR<n>) will be reset if the highest active priority is Secure. System behavior is UNPREDICTABLE.
- Non-secure writes corresponding to Group 0 interrupts when GICC_CTLR.EOImodeS == 1. In systems that support system error generation, an implementation might generate a system error. In this case, GIC behavior is predictable, and the highest Non-secure active priority (in the Non-secure copy of GICC_APR<n>) will be reset if the highest active priority is Non-secure. System behavior is UNPREDICTABLE.

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_EOIR0 and ICC_EOIR1 provide equivalent functionality.
- For AArch64 implementations, ICC_EOIR0_EL1 and ICC_EOIR1_EL1 provide equivalent functionality.

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_EOIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0010</td>
<td>GICC_EOIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRLR.DS == 0 accesses to this register are WO.
- When an access is Secure accesses to this register are WO.
- When an access is Non-secure accesses to this register are WO.
GICC_HPPIR, CPU Interface Highest Priority Pending Interrupt Register

The GICC_HPPIR characteristics are:

**Purpose**

Provides the INTID of the highest priority pending interrupt on the CPU interface.

**Configuration**

If \texttt{GICD_CTLR.DS==0}:

- This register is Common.
- \texttt{GICC_AHPPIR} is an alias of the Non-secure view of this register.

**Attributes**

GICC_HPPIR is a 32-bit register.

**Field descriptions**

The GICC_HPPIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
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<tr>
<td>27</td>
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<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

**Accessing the GICC_HPPIR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, \texttt{ICC_HPPIR0} and \texttt{ICC_HPPIR1} provide equivalent functionality.
- For AArch64 implementations, \texttt{ICC_HPPIR0_EL1} and \texttt{ICC_HPPIR1_EL1} provide equivalent functionality.

If the highest priority pending interrupt is in Group 0, a Non-secure read of this register returns the special INTID 1023.
For Secure reads when `GICD_CTLR.DS==0`, or for Secure and Non-secure reads when `GICD_CTLR.DS==1`, returns the special INTID 1022 if the highest priority pending interrupt is in Group 1.

If no interrupts are in the pending state, a read of this register returns the special INTID 1023.

Interrupt identifiers corresponding to an interrupt group that is not enabled are ignored.

If the highest priority pending interrupt is a direct interrupt that is both individually enabled in the Distributor and part of an interrupt group that is enabled in the Distributor, and the interrupt group is disabled in the CPU interface for this PE, this register returns the special INTID 1023.

For more information about pending interrupts that are not considered when determining the highest priority pending interrupt, see 'Preemption' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_HPPIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0018</td>
<td>GICC_HPPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `GICD_CTLR.DS == 0` accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
The GICC_IAR characteristics are:

**Purpose**

Provides the INTID of the signaled interrupt. A read of this register by the PE acts as an acknowledge for the interrupt.

**Configuration**

This register is available in all configurations of the GIC. If GICD_CTLR.DS==0:

- This register is Common.
- GICC_AIAR is an alias of the Non-secure view of this register.

The format of the INTID is governed by whether affinity routing is enabled for a Security state.

**Attributes**

GICC_IAR is a 32-bit register.

**Field descriptions**

The GICC_IAR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

**Bits [31:24]**

Reserved, RES0.

**INTID, bits [23:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGI, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

A read of this register returns the INTID of the highest priority pending interrupt for the CPU interface. The read returns a spurious INTID of 1023 if any of the following apply:

- Forwarding of interrupts by the Distributor to the CPU interface is disabled.
- Signaling of interrupts by the CPU interface to the connected PE is disabled.
- There are no pending interrupts on the CPU interface with sufficient priority for the interface to signal it to the PE.
When the GIC returns a valid INTID to a read of this register it treats the read as an acknowledge of that interrupt. In addition, it changes the interrupt status from pending to active, or to active and pending if the pending state of the interrupt persists. Normally, the pending state of an interrupt persists only if the interrupt is level-sensitive and remains asserted.

For every read of a valid INTID from GICC_IAR, the connected PE must perform a matching write to **GICC_EOIR**.

---

**Note**

- Arm recommends that software preserves the entire register value read from this register, and writes that value back to **GICC_EOIR** on completion of interrupt processing.
- For SPIs, although multiple target PEs might attempt to read this register at any time, only one PE can obtain a valid INTID. For more information, see 'Activation' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

### Accessing the GICC_IAR

When **GICD_CTLR**.DS==1, if the highest priority pending interrupt is in Group 1, the special INTID 1022 is returned. In GIC implementations that support two Security states, if the highest priority pending interrupt is in Group 0, Non-secure reads return the special INTID 1023.

In GIC implementations that support two Security states, if the highest priority pending interrupt is in Group 1, Secure reads return the special INTID 1022.

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, **ICC_IAR0** and **ICC_IAR1** provide equivalent functionality.
- For AArch64 implementations, **ICC_IAR0_EL1** and **ICC_IAR1_EL1** provide equivalent functionality.

When affinity routing is enabled for a Security state, it is a programming error to use memory-mapped registers to access the GIC.

**GICC_IAR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x000C</td>
<td>GICC_IAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
The GICC_IIDR characteristics are:

**Purpose**

Provides information about the implementer and revision of the CPU interface.

**Configuration**

**Attributes**

GICC_IIDR is a 32-bit register.

**Field descriptions**

The GICC_IIDR bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>PRODUCTID DEFINED</td>
<td>IMPLEMENTATION DEFINED</td>
<td>IMPLEMENTATION DEFINED</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
<tr>
<td>30</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ProductID, bits [31:20]**

An implementation defined product identifier.

**Architecture_version, bits [19:16]**

The version of the GIC architecture that is implemented.

<table>
<thead>
<tr>
<th>Architecture_version</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>GICv1.</td>
</tr>
<tr>
<td>0b0010</td>
<td>GICv2.</td>
</tr>
<tr>
<td>0b0011</td>
<td>FEAT_GICv3 memory-mapped interface supported. Support for the System register interface is discoverable from PE registers ID_PFR1 and ID_A64PFR0_EL1.</td>
</tr>
<tr>
<td>0b0100</td>
<td>FEAT_GICv4 memory-mapped interface supported. Support for the System register interface is discoverable from PE registers ID_PFR1 and ID_A64PFR0_EL1.</td>
</tr>
</tbody>
</table>

Other values are reserved.

**Revision, bits [15:12]**

An implementation defined revision number for the CPU interface.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the CPU interface.

- Bits [11:8] are the JEP106 continuation code of the implementer. For an Arm implementation, this field is 0x4.
- Bit [7] is always 0.
- Bits [6:0] are the JEP106 identity code of the implementer. For an Arm implementation, bits [7:0] are therefore 0x3B.
Accessing the GICC_IIDR

GICC_IIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU</td>
<td>0x00FC</td>
<td>GICC_IIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRL.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
The GICC_NSAPR<n> characteristics are:

**Purpose**

Provides information about Group 1 interrupt active priorities.

**Configuration**

The contents of these registers are IMPLEMENTATION DEFINED with the one architectural requirement that the value 0x00000000 is consistent with no interrupts being active.

When GICD_CTLR.DS==0, these registers are RAZ/WI to Non-secure accesses.

GICC_NSAPR1 is only implemented in implementations that support 6 or more bits of priority. GICC_NSAPR2 and GICC_NSAPR3 are only implemented in implementations that support 7 bits of priority.

**Attributes**

GICC_NSAPR<n> is a 32-bit register.

**Field descriptions**

The GICC_NSAPR<n> bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>IMPLEMENTATION DEFINED</td>
</tr>
</tbody>
</table>

**IMPLEMENTATION DEFINED, bits [31:0]**

IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

**Accessing the GICC_NSAPR<n>**

GICC_NSAPR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x00E0 + (4 * n)</td>
<td>GICC_NSAPR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICC_PMR, CPU Interface Priority Mask Register

The GICC_PMR characteristics are:

**Purpose**

This register provides an interrupt priority filter. Only interrupts with a higher priority than the value in this register are signaled to the PE.

**Note**

Higher interrupt priority corresponds to a lower value of the Priority field.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states this register is Common.

**Attributes**

GICC_PMR is a 32-bit register.

**Field descriptions**

The GICC_PMR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The priority mask level for the CPU interface. If the priority of the interrupt is higher than the value indicated by this field, the interface signals the interrupt to the PE.

If the GIC implementation supports fewer than 256 priority levels some bits might be RAZ/WI, as follows:

- For 128 supported levels, bit [0] = 0b0.
- For 64 supported levels, bits [1:0] = 0b00.
- For 32 supported levels, bits [2:0] = 0b000.
- For 16 supported levels, bits [3:0] = 0b0000.

For more information, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICC_PMR**

If the GIC implementation supports two Security states:

- Non-secure accesses to this register can only read or write values corresponding to the lower half of the priority range.
• If a Secure write has programmed the register with a value that corresponds to a value in the upper half of the priority range then:
  ◦ Any Non-secure read of the register returns 0x00, regardless of the value held in the register.
  ◦ Non-secure writes are ignored.

For more information, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**GICC_PMR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0004</td>
<td>GICC_PMR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When GICD_CTLR.DS == 0 accesses to this register are **RW**.
• When an access is Secure accesses to this register are **RW**.
• When an access is Non-secure accesses to this register are **RW**.

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GICC_RPR, CPU Interface Running Priority Register

The GICC_RPR characteristics are:

**Purpose**

This register indicates the running priority of the CPU interface.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states this register is Common.

**Attributes**

GICC_RPR is a 32-bit register.

**Field descriptions**

The GICC_RPR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The current running priority on the CPU interface. This is the group priority of the current active interrupt.

If there are no active interrupts on the CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

The priority returned is the group priority as if the BPR was set to the minimum value.

**Accessing the GICC_RPR**

If there is no active interrupt on the CPU interface, the idle priority value is returned.

If the GIC implementation supports two Security states, a Non-secure read of the Priority field returns:

- 0x00 if the field value is less than 0x80.
- The Non-secure view of the Priority value if the field value is 0x80 or more.

For more information, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**

Software cannot determine the number of implemented priority bits from this register.
**GICC_RPR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x0014</td>
<td>GICC_RPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
GICC_STATUSR, CPU Interface Status Register

The GICC_STATUSR characteristics are:

**Purpose**

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

**Configuration**

If the GIC implementation supports two Security states this register is Banked to provide Secure and Non-secure copies.

This register is used only when System register access is not enabled. If System register access is enabled, this register is not updated. Equivalent functionality might be provided by appropriate traps and exceptions.

**Attributes**

GICC_STATUSR is a 32-bit register.

**Field descriptions**

The GICC_STATUSR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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<th>7</th>
<th>6</th>
<th>5</th>
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<th>1</th>
<th>0</th>
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</thead>
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<td></td>
</tr>
<tr>
<td>RES0</td>
<td>ASV</td>
<td>WROD</td>
<td>RWOD</td>
<td>WRD</td>
<td>RRD</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**Bits [31:5]**

Reserved, RES0.

**ASV, bit [4]**

Attempted security violation.

<table>
<thead>
<tr>
<th>ASV</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Non-secure access to a Secure register has been detected.</td>
</tr>
</tbody>
</table>

**Note**

This bit is not set to 1 for registers where any of the fields are Non-secure.

**WROD, bit [3]**

Write to an RO location.

<table>
<thead>
<tr>
<th>WROD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to an RO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.
**RWOD, bit [2]**

Read of a WO location.

<table>
<thead>
<tr>
<th>RWOD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a WO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**WRD, bit [1]**

Write to a reserved location.

<table>
<thead>
<tr>
<th>WRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**RRD, bit [0]**

Read of a reserved location.

<table>
<thead>
<tr>
<th>RRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**Accessing the GICC_STATUSR**

This is an optional register. If the register is not implemented, the location is RAZ/WI.

If this register is implemented, **GICV_STATUSR** must also be implemented.

**GICC_STATUSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x002C</td>
<td>GICC_STATUSR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(S)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC CPU interface</td>
<td>0x002C</td>
<td>GICC_STATUSR</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(NS)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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The GICD_CLRSPIN_SR characteristics are:

**Purpose**

Removes the pending state from a valid SPI if permitted by the Security state of the access and the GICD_NSACR<n> value for that SPI.

A write to this register changes the state of a pending SPI to inactive, and the state of an active and pending SPI to active.

**Configuration**

If GICD_TYPER.MBIS == 0, this register is reserved.

When GICD_CTLR.DS==1, this register provides functionality for all SPIs.

**Attributes**

GICD_CLRSPIN_SR is a 32-bit register.

**Field descriptions**

The GICD_CLRSPIN_SR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>INTID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:13]**

Reserved, RES0.

**INTID, bits [12:0]**

The INTID of the SPI.

The function of this register depends on whether the targeted SPI is configured to be an edge-triggered or level-sensitive interrupt:

- For an edge-triggered interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will stop being pending on activation, or if the pending state is removed by a write to GICD_CLRSPIN_SR, GICD_CLRSPIN_SR, or GICD_ICPENDR<n>.
- For a level-sensitive interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will remain pending until it is deasserted by a write to GICD_CLRSPIN_SR or GICD_CLRSPIN_SR. If the interrupt is activated between having the pending state added and being deactivated, then the interrupt will be active and pending.

**Accessing the GICD_CLRSPIN_SR**

Writes to this register have no effect if:

- The value written specifies a Secure SPI, the value is written by a Non-secure access, and the value of the corresponding GICD_NSACR<n> register is less than 0b10.
- The value written specifies an invalid SPI.
- The SPI is not pending.
16-bit accesses to bits [15:0] of this register must be supported.

**Note**

A Secure access to this register can clear the pending state of any valid SPI.

---

**GICD_CLRSPI_NSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0048</td>
<td>GICD_CLRSPI_NSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **W0**.
- When an access is Secure accesses to this register are **W0**.
- When an access is Non-secure accesses to this register are **W0**.
GICD_CLRSPISR, Clear Secure SPI Pending Register

The GICD_CLRSPISR characteristics are:

**Purpose**

Removes the pending state from a valid SPI.

A write to this register changes the state of a pending SPI to inactive, and the state of an active and pending SPI to active.

**Configuration**

If GICD_TYPER.MBIS == 0, this register is reserved.

When GICD_CTLR.DS==1, this register is WI.

**Attributes**

GICD_CLRSPISR is a 32-bit register.

**Field descriptions**

The GICD_CLRSPISR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>RES0</td>
</tr>
<tr>
<td>28</td>
<td>RES0</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>RES0</td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td>RES0</td>
</tr>
<tr>
<td>23</td>
<td>RES0</td>
</tr>
<tr>
<td>22</td>
<td>RES0</td>
</tr>
<tr>
<td>21</td>
<td>RES0</td>
</tr>
<tr>
<td>20</td>
<td>RES0</td>
</tr>
<tr>
<td>19</td>
<td>RES0</td>
</tr>
<tr>
<td>18</td>
<td>RES0</td>
</tr>
<tr>
<td>17</td>
<td>RES0</td>
</tr>
<tr>
<td>16</td>
<td>RES0</td>
</tr>
<tr>
<td>15</td>
<td>RES0</td>
</tr>
<tr>
<td>14</td>
<td>RES0</td>
</tr>
<tr>
<td>13</td>
<td>RES0</td>
</tr>
<tr>
<td>12</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>11</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>10</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>9</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>8</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>7</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>6</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>5</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>4</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>3</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>2</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>1</td>
<td>INTID, bits [12:0]</td>
</tr>
<tr>
<td>0</td>
<td>INTID, bits [12:0]</td>
</tr>
</tbody>
</table>

**Bits [31:13]**

Reserved, RES0.

**INTID, bits [12:0]**

The INTID of the SPI.

The function of this register depends on whether the targeted SPI is configured to be an edge-triggered or level-sensitive interrupt:

- For an edge-triggered interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will stop being pending on activation, or if the pending state is removed by a write to GICD_CLRSPISR, GICD_CLRSPISR, or GICD_ICPENDR.<n>.
- For a level-sensitive interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will remain pending until it is deasserted by a write to GICD_CLRSPISR or GICD_CLRSPISR. If the interrupt is activated between having the pending state added and being deactivated, then the interrupt will be active and pending.

**Accessing the GICD_CLRSPISR**

Writes to this register have no effect if:

- The value is written by a Non-secure access.
- The value written specifies an invalid SPI.
- The SPI is not pending.

16-bit accesses to bits [15:0] of this register must be supported.
GICD_CLR_SPI_SR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0058</td>
<td>GICD_CLR_SPI_SR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRL.DS == 0 accesses to this register are **WI**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WI**.
GICD_CPENDSGIR<n>, SGI Clear-Pending Registers, n = 0 - 3

The GICD_CPENDSGIR<n> characteristics are:

**Purpose**

Removes the pending state from an SGI.

A write to this register changes the state of a pending SGI to inactive, and the state of an active and pending SGI to active.

**Configuration**

Four SGI clear-pending registers are implemented. Each register contains eight clear-pending bits for each of four SGIs, for a total of 16 possible SGIs.

In multiprocessor implementations, each PE has a copy of these registers.

**Attributes**

GICD_CPENDSGIR<n> is a 32-bit register.

**Field descriptions**

The GICD_CPENDSGIR<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| SGI_clear_pending_bits3 | SGI_clear_pending_bits2 | SGI_clear_pending_bits1 | SGI_clear_pending_bits0 |

SGI_clear_pending_bits<x>, bits [8x+7:8x], for x = 3 to 0

Removes the pending state from SGI number 4n + x for the PE corresponding to the bit number written to.

Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>SGI_clear_pending_bits&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>If read, indicates that the SGI from the corresponding PE is not pending and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0x01</td>
<td>If read, indicates that the SGI from the corresponding PE is pending or is active and pending. If written, removes the pending state from the SGI for the corresponding PE.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For SGI ID m, generated by processing element C writing to the corresponding GICD_SGIR field, where DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_CPENDSGIR<n> number is given by n = m DIV 4.
- The offset of the required register is (0xF10 + (4n)).
- The offset of the required field within the register GICD_CPENDSGIR<n> is given by m MOD 4.
- The required bit in the 8-bit SGI clear-pending field m is bit C.
Accessing the GICD_CPENDSGIR<n>

These registers are used only when affinity routing is not enabled. When affinity routing is enabled, this register is RES0. An implementation is permitted to make the register RAZ/WI in this case.

A register bit that corresponds to an unimplemented SGI is RAZ/WI.

These registers are byte-accessible.

If the GIC implementation supports two Security states:

- A register bit that corresponds to a Group 0 interrupt is RAZ/WI to Non-secure accesses.
- Register bits corresponding to unimplemented PEs are RAZ/WI.

GICD_CPENDSGIR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>0x0F10 + (4 * n)</td>
<td>GICD_CPENDSGIR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICD_CTLR, Distributor Control Register

The GICD_CTLR characteristics are:

**Purpose**

Enables interrupts and affinity routing.

**Configuration**

The format of this register depends on the Security state of the access and the number of Security states supported, which is specified by GICD_CTLR.DS.

**Attributes**

GICD_CTLR is a 32-bit register.

**Field descriptions**

The GICD_CTLR bit assignments are:

**When access is Secure, in a system that supports two Security states:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RWP</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>E1NWF</td>
</tr>
<tr>
<td>28</td>
<td>DS</td>
</tr>
<tr>
<td>27</td>
<td>ARE_NS</td>
</tr>
<tr>
<td>26</td>
<td>ARE_S</td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td>EnableGrp1S</td>
</tr>
<tr>
<td>23</td>
<td>EnableGrp1NS</td>
</tr>
<tr>
<td>22</td>
<td>EnableGrp0</td>
</tr>
</tbody>
</table>

**RWP, bit [31]**

Register Write Pending. Read only. Indicates whether a register write is in progress or not:

<table>
<thead>
<tr>
<th>RWP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No register write in progress. The effects of previous register writes to the affected register fields are visible to all logical components of the GIC architecture, including the CPU interfaces.</td>
</tr>
<tr>
<td>0b1</td>
<td>Register write in progress. The effects of previous register writes to the affected register fields are not guaranteed to be visible to all logical components of the GIC architecture, including the CPU interfaces, as the effects of the changes are still being propagated.</td>
</tr>
</tbody>
</table>

This field tracks writes to:

- GICD_CTLR[2:0], the Group Enables, for transitions from 1 to 0 only.
- GICD_CTLR[7:4], the ARE bits, E1NWF bit and DS bit.
- GICD_ICENABLER<n>.

Updates to other register fields are not tracked by this field.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [30:8]**

Reserved, RES0.
E1NWF, bit [7]

Enable 1 of N Wakeup Functionality.

It is IMPLEMENTATION DEFINED whether this bit is programmable, or RAZ/WI.

If it is implemented, then it has the following behavior:

<table>
<thead>
<tr>
<th>E1NWF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A PE that is asleep cannot be picked for 1 of N interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>A PE that is asleep can be picked for 1 of N interrupts as determined by IMPLEMENTATION DEFINED controls.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DS, bit [6]

Disable Security.

<table>
<thead>
<tr>
<th>DS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure accesses are not permitted to access and modify registers that control Group 0 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure accesses are permitted to access and modify registers that control Group 0 interrupts.</td>
</tr>
</tbody>
</table>

If DS is written from 0 to 1 when GICD_CTLR.ARE_S == 1, then GICD_CTLR.ARE for the single Security state is RAO/WI.

If the Distributor only supports a single Security state, this bit is RAO/WI.

If the Distributor supports two Security states, it IMPLEMENTATION DEFINED whether this bit is programmable or implemented as RAZ/WI.

When this field is set to 1, all accesses to GICD_CTLR access the single Security state view, and all bits are accessible.

When set to 1, this field can only be cleared by a hardware reset.

Writing this bit from 0 to 1 is UNPREDICTABLE if any of the following is true:

- GICD_CTLR.EnableGrp0==1.
- GICD_CTLR.EnableGrp1S==1.
- GICD_CTLR.EnableGrp1NS==1.
- One or more INTID is in the Active or Active and Pending state.

On a Warm reset, this field resets to 0.

ARE_NS, bit [5]

Affinity Routing Enable, Non-secure state.

<table>
<thead>
<tr>
<th>ARE_NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Affinity routing disabled for Non-secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Affinity routing enabled for Non-secure state.</td>
</tr>
</tbody>
</table>

When affinity routing is enabled for the Secure state, this field is RAO/WI.

Changing the ARE_NS settings from 0 to 1 is UNPREDICTABLE except when GICD_CTLR.EnableGrp1 Non-secure == 0.

Changing the ARE_NS settings from 1 to 0 is UNPREDICTABLE.

If GICv2 backwards compatibility for Non-secure state is not implemented, this field is RAO/WI.

On a Warm reset, this field resets to 0.

ARE_S, bit [4]

Affinity Routing Enable, Secure state.
ARE_S | Meaning
---|---
0b0 | Affinity routing disabled for Secure state.
0b1 | Affinity routing enabled for Secure state.

Changing the ARE_S setting from 0 to 1 is **UNPREDICTABLE** except when all of the following apply:

- GICD_CTLR.EnableGrp0==0.
- GICD_CTLR.EnableGrp1S==0.
- GICD_CTLR.EnableGrp1NS==0.

Changing the ARE_S settings from 1 to 0 is **UNPREDICTABLE**.

If GICv2 backwards compatibility for Secure state is not implemented, this field is RAO/WI.

On a Warm reset, this field resets to 0.

**Bit [3]**

Reserved, RES0.

**EnableGrp1S, bit [2]**

Enable Secure Group 1 interrupts.

<table>
<thead>
<tr>
<th>EnableGrp1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

If GICD_CTLR.ARE_S == 0, this field is RES0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EnableGrp1NS, bit [1]**

Enable Non-secure Group 1 interrupts.

<table>
<thead>
<tr>
<th>EnableGrp1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Non-secure Group 1 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Non-secure Group 1 interrupts are enabled.</td>
</tr>
</tbody>
</table>

**Note**

This field also controls whether LPIs are forwarded to the PE.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**EnableGrp0, bit [0]**

Enable Group 0 interrupts.

<table>
<thead>
<tr>
<th>EnableGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**When access is Non-secure, in a system that supports two Security states:**

- **RWP**
- **RES0**
- **ARE_NS**
- **RES0**
- **EnableGrp1A**
- **EnableGrp1**
RWP, bit [31]

This bit is a read-only alias of the Secure GICD_CTLR.RWP bit.

Bits [30:5]

Reserved, RES0.

ARE_NS, bit [4]

This bit is a read-write alias of the Secure GICD_CTLR.ARE_NS bit.

If GICv2 backwards compatibility for Non-secure state is not implemented, this field is RAO/WI.

Bits [3:2]

Reserved, RES0.

EnableGrp1A, bit [1]

If ARE_NS == 1, then this bit is a read-write alias of the Secure GICD_CTLR.EnableGrp1NS bit.

If ARE_NS == 0, then this bit is RES0.

EnableGrp1, bit [0]

If ARE_NS == 0, then this bit is a read-write alias of the Secure GICD_CTLR.EnableGrp1NS bit.

If ARE_NS == 1, then this bit is RES0.

When in a system that supports only a single Security state:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No register write in progress. The effects of previous register writes to the affected register fields are visible to all logical components of the GIC architecture, including the CPU interfaces.</td>
</tr>
<tr>
<td>0b1</td>
<td>Register write in progress. The effects of previous register writes to the affected register fields are not guaranteed to be visible to all logical components of the GIC architecture, including the CPU interfaces, as the effects of the changes are still being propagated.</td>
</tr>
</tbody>
</table>

This field tracks updates to:

- GICD_CTLR[2:0], the Group Enables, for transitions from 1 to 0 only.
- GICD_CTLR[7:4], the ARE bits, E1NWF bit and DS bit.
- GICD_ICENABLER<n>, the bits that allow disabling of SPIs.

Updates to other register fields are not tracked by this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [30:9]

Reserved, RES0.

nASSGIreq, bit [8]

When FEAT_GICv4p1 is implemented:

Controls whether SGIs have an active state.

This bit is RES0 if GICD_TYPER2.GICD_TYPER2.nASSGIcap is 0.

This bit is WI when any of GICD_CTLR.{EnableGrp0,EnableGrp1} is 1.

<table>
<thead>
<tr>
<th>nASSGIreq</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SGIs have an active state and must be deactivated.</td>
</tr>
<tr>
<td>0b1</td>
<td>SGIs do not have an active state and do not require deactivation.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Otherwise:

Reserved, RES0.

E1NWF, bit [7]

Enable 1 of N Wakeup Functionality.

It is IMPLEMENTATION DEFINED whether this bit is programmable, or RAZ/WI.

If it is implemented, then it has the following behavior:

<table>
<thead>
<tr>
<th>E1NWF</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A PE that is asleep cannot be picked for 1 of N interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td>A PE that is asleep can be picked for 1 of N interrupts as determined by IMPLEMENTATION DEFINED controls.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

DS, bit [6]

Disable Security. This field is RAO/WI.

Bit [5]

Reserved, RES0.

ARE, bit [4]

Affinity Routing Enable.

<table>
<thead>
<tr>
<th>ARE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Affinity routing disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Affinity routing enabled.</td>
</tr>
</tbody>
</table>

Changing the ARE settings from 0 to 1 is UNPREDICTABLE except when all of the following apply:

- GICD_CTLR.EnableGrp1==0.
- GICD_CTLR.EnableGrp0==0.

Changing ARE from 1 to 0 is UNPREDICTABLE.

If GICv2 backwards compatibility is not implemented, this field is RAO/WI.
On a Warm reset, this field resets to 0.

**Bits [3:2]**

Reserved, RES0.

**EnableGrp1, bit [1]**

Enable Group 1 interrupts.

<table>
<thead>
<tr>
<th>EnableGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 interrupts disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 interrupts enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**EnableGrp0, bit [0]**

Enable Group 0 interrupts.

<table>
<thead>
<tr>
<th>EnableGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 interrupts are enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the GICD_CTLR

If an interrupt is pending within a CPU interface when the corresponding GICD_CTLR.EnableGrpX bit is written from 1 to 0 the interrupt must be retrieved from the CPU interface.

**Note**

This might have no effect on the forwarded interrupt if it has already been activated. When a write changes the value of ARE for a Security state or the value of the DS bit, the format used for interpreting the remaining bits provided in the write data is the format that applied before the write takes effect.

**GICD_CTLR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0000</td>
<td>GICD_CTLR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_ICACTIVER<n>, Interrupt Clear-Active Registers, n = 0 - 31

The GICD_ICACTIVER<n> characteristics are:

Purpose

Deactivates the corresponding interrupt. These registers are used when saving and restoring GIC state.

Configuration

These registers are available in all GIC configurations. If GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_ICACTIVER<n> registers is \((GICD_TYPER.ITLinesNumber+1)\). Registers are numbered from 0.

GICD_ICACTIVER0 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_ICACTIVER0 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

Attributes

GICD_ICACTIVER<n> is a 32-bit register.

Field descriptions

The GICD_ICACTIVER<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear_active_bit31</td>
<td>Clear_active_bit30</td>
<td>Clear_active_bit29</td>
<td>Clear_active_bit28</td>
<td>Clear_active_bit27</td>
<td>Clear_active_bit26</td>
</tr>
</tbody>
</table>

Clear_active_bit<x>, bit [x], for x = 31 to 0

Removes the active state from interrupt number \(32n + x\). Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or is active and pending. If written, deactivates the corresponding interrupt, if the interrupt is active. If the interrupt is already deactivated, the write has no effect.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ICACTIVER<n> number, n, is given by \(n = m \text{ DIV 32}\).
- The offset of the required GICD_ICACTIVER is (0x380 + (4*n)).
- The bit number of the required group modifier bit in this register is \(m \text{ MOD 32}\).
Accessing the GICD_ICACTIVER<n>

When affinity routing is enabled for the Security state of an interrupt, the bits corresponding to SGIs and PPIs in that Security state are RAZ/WI, and equivalent functionality for SGIs and PPIs is provided by GICR_ICACTIVER0.

Bits corresponding to unimplemented interrupts are RAZ/WI.

If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

GICD_ICACTIVER<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0380 + (4 * n)</td>
<td>GICD_ICACTIVER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
**GICD_ICACTIVER<n>E, Interrupt Clear-Active Registers (extended SPI range), n = 0 - 31**

The GICD_ICACTIVER<n>E characteristics are:

**Purpose**

Removes the active state from the corresponding SPI in the extended SPI range.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ICACTIVER<n>E are `RES0`.

When GICD_TYPER.ESPI==0, these registers are `RES0`.

When GICD_TYPER.ESPI==1, the number of implemented GICD_ICACTIVER<n>E registers is (GICD_TYPER.ESPI_range+1). Registers are numbered from 0.

**Attributes**

GICD_ICACTIVER<n>E is a 32-bit register.

**Field descriptions**

The GICD_ICACTIVER<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clear_active_bit31</td>
<td>Clear_active_bit30</td>
<td>Clear_active_bit29</td>
<td>Clear_active_bit28</td>
<td>Clear_active_bit27</td>
<td>Clear_active_bit26</td>
</tr>
</tbody>
</table>

**Clear_active_bit<x>, bit [x], for x = 31 to 0**

For the extended SPIs, removes the active state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or is active and pending. If written, deactivates the corresponding interrupt, if the interrupt is active. If the interrupt is already deactivated, the write has no effect.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ICACTIVER<n>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_ICACTIVER<n>E is (0x1C00 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-4096) MOD 32.

**Accessing the GICD_ICACTIVER<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICD_ICACTIVER<n>E, the corresponding bit is `RES0`. 

---

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When \texttt{GICD\_CTRL.DS==0}, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

\textbf{GICD\_ICACTIVER\(<n>E\) can be accessed through the memory-mapped interfaces:}

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1C00 + (4 * n)</td>
<td>GICD_ICACTIVER(&lt;n&gt;E)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GICD\_CTRL.DS == 0} accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICD_ICENABLER<n> characteristics are:

**Purpose**

Disables forwarding of the corresponding interrupt to the CPU interfaces.

**Configuration**

These registers are available in all GIC configurations. If \( GICD\_\text{CTLR}.\text{DS} == 0 \), these registers are Common.

The number of implemented \( \text{GICD\_ICENABLER}\_n \) registers is \( (\text{GICD\_TYPER}.\text{ITLinesNumber}+1) \). Registers are numbered from 0.

\( \text{GICD\_ICENABLER}0 \) is Banked for each connected PE with \( \text{GICR\_TYPER}.\text{Processor\_Number} < 8 \).

Accessing \( \text{GICD\_ICENABLER}0 \) from a PE with \( \text{GICR\_TYPER}.\text{Processor\_Number} > 7 \) is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

\( \text{GICD\_ICENABLER}\_n \) is a 32-bit register.

**Field descriptions**

The GICD_ICENABLER<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
</table>

Clear_enable_bit<x>, bit \([x]\), for \(x = 31\) to \(0\)

For SPIs and PPIs, controls the forwarding of interrupt number \(32n + x\) to the CPU interfaces. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_enable_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, disables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 0.</td>
</tr>
</tbody>
</table>

For SGIs, the behavior of this bit is IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For INTID \(m\), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ICENABLER<n> number, \( n \), is given by \( n = m \div 32 \).
- The offset of the required GICD_ICENABLER is \((8 \times 180 + (4 \times n))\).
- The bit number of the required group modifier bit in this register is \( m \mod 32 \).
Note

Writing a 1 to a GICD_ICENABLER<n> bit only disables the forwarding of the corresponding interrupt from the Distributor to any CPU interface. It does not prevent the interrupt from changing state, for example becoming pending or active and pending if it is already active.

Accessing the GICD_ICENABLER<n>

For SGIs and PPIs:

- When ARE is 1 for the Security state of an interrupt, the field for that interrupt is RES0 and an implementation is permitted to make the field RAZ/WI in this case.
- Equivalent functionality is provided by GICR_ICENABLER0.

Bits corresponding to unimplemented interrupts are RAZ/WI.

When GICD_CTLR.DS==0, bits corresponding to Group 0 and Secure Group 1 interrupts are RAZ/WI to Non-secure accesses.

It is IMPLEMENTATION DEFINED whether implemented SGIs are permanently enabled, or can be enabled and disabled by writes to GICD_ISENABLER<n> and GICD_ICENABLER<n> where n=0.

Completion of a write to this register does not guarantee that the effects of the write are visible throughout the affinity hierarchy. To ensure an enable has been cleared, software must write to the register with bits set to 1 to clear the required enables. Software must then poll GICD_CTLR.RWP until it has the value zero.

GICD_ICENABLER<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0180 + (4 * n)</td>
<td>GICD_ICENABLER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICD_ICENABLER\textsubscript{n}E characteristics are:

**Purpose**

Disables forwarding of the corresponding SPI in the extended SPI range to the CPU interfaces.

**Configuration**

This register is present only when FEAT\_GICv3p1 is implemented. Otherwise, direct accesses to GICD\_ICENABLER\textsubscript{n}E are \texttt{RES0}.

When \texttt{GICD\_TYPER.ESPI==0}, these registers are \texttt{RES0}.

When \texttt{GICD\_TYPER.ESPI==1}, the number of implemented GICD\_ICENABLER\textsubscript{n}E registers is (\texttt{GICD\_TYPER.ESPI\_range+1}). Registers are numbered from 0.

**Attributes**

GICD\_ICENABLER\textsubscript{n}E is a 32-bit register.

**Field descriptions**

The GICD\_ICENABLER\textsubscript{n}E bit assignments are:

|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|

**Clear_enable_bit\textsubscript{x}, bit [x], for x = 31 to 0**

For the extended SPI range, controls the forwarding of interrupt number x to the CPU interface. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_enable_bit\textsubscript{x}</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, enables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD\_ICENABLER\textsubscript{n}E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD\_ICENABLER\textsubscript{n}E is (0x1400 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-4096) MOD 32.
Accessing the \texttt{GICD\_ICENABLER\langle n\rangle\_E}

When affinity routing is not enabled for the Security state of an interrupt in \texttt{GICD\_ICENABLER\langle n\rangle\_E}, the corresponding bit is \texttt{RES}.0.

When \texttt{GICD\_CTLR.DS==0}, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

\textbf{GICD\_ICENABLER\langle n\rangle\_E can be accessed through the memory-mapped interfaces:}

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1400 + (4 * n)</td>
<td>GICD_ICENABLER\langle n\rangle_E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GICD\_CTLR.DS == 0} accesses to this register are \texttt{RW}.
- When an access is Secure accesses to this register are \texttt{RW}.
- When an access is Non-secure accesses to this register are \texttt{RW}.
GICD_ICFGR<n>, Interrupt Configuration Registers, n = 0 - 63

The GICD_ICFGR<n> characteristics are:

**Purpose**

Determines whether the corresponding interrupt is edge-triggered or level-sensitive.

**Configuration**

These registers are available in all GIC configurations. If the GIC implementation supports two Security states, these registers are Common.

GICD_ICFGR1 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_ICFGR1 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

For SGIs and PPIs:

- When ARE is 1 for the Security state of an interrupt, the field for that interrupt is RES0 and an implementation is permitted to make the field RAZ/WI in this case.
- Equivalent functionality is provided by GICR_ICFGR<n>

For each supported PPI, it is IMPLEMENTATION DEFINED whether software can program the corresponding Int_config field.

For SGIs, Int_config fields are RO, meaning that GICD_ICFGR0 is RO.

Changing Int_config when the interrupt is individually enabled is UNPREDICTABLE.

Changing the interrupt configuration between level-sensitive and edge-triggered (in either direction) at a time when there is a pending interrupt will leave the interrupt in an UNKNOWN pending state.

Fields corresponding to unimplemented interrupts are RAZ/WI.

**Attributes**

GICD_ICFGR<n> is a 32-bit register.

**Field descriptions**

The GICD_ICFGR<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int_config15</td>
<td>Int_config14</td>
<td>Int_config13</td>
<td>Int_config12</td>
<td>Int_config11</td>
<td>Int_config10</td>
<td>Int_config9</td>
<td>Int_config8</td>
<td>Int_config7</td>
<td>Int_config6</td>
<td>Int_config5</td>
<td>Int_config4</td>
<td>Int_config3</td>
<td>Int_config2</td>
<td>Int_config1</td>
<td>Int_config0</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Int_config<x>, bits [2x+1:2x], for x = 15 to 0**

Indicates whether the interrupt with ID 16n + x is level-sensitive or edge-triggered.

Int_config[0] (bit [2x]) is RES0.

Possible values of Int_config[1] (bit [2x+1]) are:
For SGIs, Int_config[1] is RAO/WI.

For SPIs and PPIs, Int_config[1] is programmable unless the implementation supports two Security states and the bit corresponds to a Group 0 or Secure Group 1 interrupt, in which case the bit is RAZ/WI to Non-secure accesses.

On a Warm reset, this field resets to an architecturally "UNKNOWN" value.

**Accessing the GICD_ICFGR<n>**

GICD_ICFGR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0C00 + (4 * n)</td>
<td>GICD_ICFGR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_ICFGR<n>E, Interrupt Configuration Registers (Extended SPI Range), n = 0 - 63

The GICD_ICFGR<n>E characteristics are:

**Purpose**

Determines whether the corresponding SPI in the extended SPI range is edge-triggered or level-sensitive.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ICFGR<n>E are RES0.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1, the number of implemented GICD_ICFGR<n>E registers is ((GICD_TYPER.ESPI_range+1)*2). Registers are numbered from 0.

**Attributes**

GICD_ICFGR<n>E is a 32-bit register.

**Field descriptions**

The GICD_ICFGR<n>E bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13 |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Int_config15 | Int_config14 | Int_config13 | Int_config12 | Int_config11 | Int_config10 | Int_config9 | Int_config8 | Int_config7 | Int_config6 | Int_config5 | Int_config4 | Int_config3 | Int_config2 | Int_config1 | Int_config0 |

Int_config<x>, bits [2x+1:2x], for x = 15 to 0

Indicates whether the interrupt with ID 16n + x is level-sensitive or edge-triggered.

Int_config[0] (bit[2x]) is RES0.

Possible values of Int_config[1] (bit[2x+1]) are:

<table>
<thead>
<tr>
<th>Int_config&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Corresponding interrupt is level-sensitive.</td>
</tr>
<tr>
<td>0b01</td>
<td>Corresponding interrupt is edge-triggered.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICD_ICFGR<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICD_ICFGR<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, a register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICD_ICFGR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>
This interface is accessible as follows:

- When `GICD_CTR.DS` == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_ICPENDR<n>, Interrupt Clear-Pending Registers, n = 0 - 31

The GICD_ICPENDR<n> characteristics are:

**Purpose**

Removes the pending state from the corresponding interrupt.

**Configuration**

These registers are available in all GIC configurations. If GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_ICPENDR<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_ICPENDR0 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_ICPENDR0 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

GICD_ICPENDR<n> is a 32-bit register.

**Field descriptions**

The GICD_ICPENDR<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
</table>

*Clear_pending_bit<x>*, bit [x], for x = 31 to 0

For SPIs and PPIs, removes the pending state from interrupt number 32n + x. Reads and writes have the following behavior:
### Clear_pending_bit<x>

<table>
<thead>
<tr>
<th>Clear_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending on any PE. If written, has no effect.</td>
</tr>
</tbody>
</table>
| 0b1                  | If read, indicates that the corresponding interrupt is pending, or active and pending:  
  • On this PE if the interrupt is an SGI or PPI.  
  • On at least one PE if the interrupt is an SPI.  
If written, changes the state of the corresponding interrupt from pending to inactive, or from active and pending to active. This has no effect in the following cases:  
  • If the interrupt is an SGI. In this case, the write is ignored. The pending state of an SGI can be cleared using GICD_CPENDSGIR<n>.  
  • If the interrupt is not pending and is not active and pending.  
  • If the interrupt is a level-sensitive interrupt that is pending or active and pending for a reason other than a write to GICD_ISPENDR<n>. In this case, if the interrupt signal continues to be asserted, the interrupt remains pending or active and pending. |

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ICPENDR<n> number, n, is given by n = m DIV 32.
- The offset of the required GICD_ICPENDR is (0x200 + (4*n)).
- The bit number of the required group modifier bit in this register is m MOD 32.

### Accessing the GICD_ICPENDR<n>

Clear-pending bits for SGIs are RO/WI.

When affinity routing is enabled for the Security state of an interrupt:

- Bits corresponding to SGIs and PPIs are RAZ/WI, and equivalent functionality for SGIs and PPIs is provided by GICR_ICPENDR0.
- Bits corresponding to Group 0 and Group 1 Secure interrupts can only be cleared by Secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

**GICD_ICPENDR<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0280 + (4 * n)</td>
<td>GICD_ICPENDR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICD_ICPENDR<n>E characteristics are:

**Purpose**

Removes the pending state to the corresponding SPI in the extended SPI range.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ICPENDR<n>E are RES0.

When \( \text{GICD_TYPER.ESPI} == 0 \), these registers are RES0.

When \( \text{GICD_TYPER.ESPI} == 1 \), the number of implemented GICD_ICPENDR<n>E registers is \( (\text{GICD_TYPER.ESPI_range}+1) \). Registers are numbered from 0.

**Attributes**

GICD_ICPENDR<n>E is a 32-bit register.

**Field descriptions**

The GICD_ICPENDR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Clear_pending_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Clear_pending_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Clear_pending_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Clear_pending_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Clear_pending_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Clear_pending_bit26</td>
</tr>
</tbody>
</table>

**Clear_pending_bit<x>, bit [x], for x = 31 to 0**

For the extended PPIs, removes the pending state to interrupt number \( x \). Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending.</td>
</tr>
<tr>
<td></td>
<td>If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is pending, or active and pending.</td>
</tr>
<tr>
<td></td>
<td>If written, changes the state of the corresponding interrupt from pending to inactive, or from active and pending to active.</td>
</tr>
<tr>
<td></td>
<td>This has no effect in the following cases:</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is not pending and is not active and pending.</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is a level-sensitive interrupt that is pending or active and pending for a reason other than a write to GICD_ISPENDR&lt;n&gt;E. In this case, if the interrupt signal continues to be asserted, the interrupt remains pending or active and pending.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:
• The corresponding GICD_ICPENDR<n>E number, n, is given by \( n = (m-4096) \text{ DIV } 32 \).
• The offset of the required GICD_ICPENDR<n>E is \( (0x1800 + (4*n)) \).
• The bit number of the required group modifier bit in this register is \( (m-4096) \text{ MOD } 32 \).

**Accessing the GICD_ICPENDR<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICD_ICPENDR<n>E, the corresponding bit is \texttt{RES0}.

When \texttt{GICD_CTLR.DS==0}, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICD_ICPENDR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>( 0x1800 + (4*n) )</td>
<td>GICD_ICPENDR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When \texttt{GICD_CTLR.DS == 0} accesses to this register are \texttt{RW}.
• When an access is Secure accesses to this register are \texttt{RW}.
• When an access is Non-secure accesses to this register are \texttt{RW}.

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Copyright © 2010-2020 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.
GICD_IGROUPR<n>, Interrupt Group Registers, n = 0 - 31

The GICD_IGROUPR<n> characteristics are:

**Purpose**

Controls whether the corresponding interrupt is in Group 0 or Group 1.

**Configuration**

These registers are available in all GIC configurations. If GICD_CTLR.DS==0, these registers are Secure.

The number of implemented GICD_IGROUPR<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_IGROUPR0 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_IGROUPR0 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

GICD_IGROUPR<n> is a 32-bit register.

**Field descriptions**

The GICD_IGROUPR<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group_status_bit31</td>
<td>Group_status_bit30</td>
<td>Group_status_bit29</td>
<td>Group_status_bit28</td>
<td>Group_status_bit27</td>
<td>Group_status_bit26</td>
</tr>
</tbody>
</table>

**Group_status_bit<x>, bit [x], for x = 31 to 0**

Group status bit.

<table>
<thead>
<tr>
<th>Group_status_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 0. When GICD_CTLR.DS==0, the corresponding interrupt is Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 1. When GICD_CTLR.DS==0, the corresponding interrupt is Non-secure Group 1.</td>
</tr>
</tbody>
</table>

If affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICD_IGRPMODR<n> to form a 2-bit field that defines an interrupt group. The encoding of this field is described in GICD_IGRPMODR<n>.

If affinity routing is disabled for the Security state of an interrupt, then:

- The corresponding GICD_IGRPMODR<n> bit is RES0.
- For Secure interrupts, the interrupt is Secure Group 0.
- For Non-secure interrupts, the interrupt is Non-secure Group 1.

On a Warm reset, when n == 0, this field resets to an UNKNOWN value.
On a Warm reset, when \( n > 0 \), this field resets to 0.

For INTID \( m \), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD\_IGROUP\(<n>\) number, \( n \), is given by \( n = m \div 32 \).
- The offset of the required GICD\_IGROUP is \( (0\times080 + (4\times n)) \).
- The bit number of the required group modifier bit in this register is \( m \mod 32 \).

### Accessing the GICD\_IGROUP\(<n>\)

For SGI\&s and PPI\&s:

- When ARE is 1 for the Security state of an interrupt, the field for that interrupt is \( \text{RES0} \) and an implementation is permitted to make the field RAZ/WI in this case.
- Equivalent functionality is provided by GICR\_IGROUP\(<0>\).

When \( \text{GICD\_CTRL\_DS} = 0 \), the register is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

---

**Note**

Accesses to GICD\_IGROUP\(<0>\) when affinity routing is not enabled for a Security state access the same state as GICR\_IGROUP\(<0>\), and must update Redistributor state associated with the PE performing the accesses. Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

---

**GICD\_IGROUP\(<n>\) can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>( 0\times080 + (4\times n) )</td>
<td>GICD_IGROUP(&lt;n&gt;)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD\_CTRL\_DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
The GICD_IGROUPR<n>E characteristics are:

**Purpose**

Controls whether the corresponding SPI in the extended SPI range is in Group 0 or Group 1.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_IGROUPR<n>E are RES0.

GICD_IGROUPR<n>E resets to 0x00000000.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1:

- The number of implemented GICD_IGROUPR<n>E registers is (GICD_TYPER.ESPI_range+1). Registers are numbered from 0.
- When GICD_CTLR.DS==0, this register is Secure.

**Attributes**

GICD_IGROUPR<n>E is a 32-bit register.

**Field descriptions**

The GICD_IGROUPR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group_status_bit31</td>
<td>Group_status_bit30</td>
<td>Group_status_bit29</td>
<td>Group_status_bit28</td>
<td>Group_status_bit27</td>
<td>Group_status_bit26</td>
</tr>
</tbody>
</table>

**Group_status_bit<x>, bit [x], for x = 31 to 0**

Group status bit.

<table>
<thead>
<tr>
<th>Group_status_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 0. When GICD_CTLR.DS==0, the corresponding interrupt is Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 1. When GICD_CTLR.DS==0, the corresponding interrupt is Non-secure Group 1.</td>
</tr>
</tbody>
</table>

If affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICD_IGRPMODR<n>E to form a 2-bit field that defines an interrupt group. The encoding of this field is described in GICD_IGRPMODR<n>E.

If affinity routing is disabled for the Security state of an interrupt, the bit is RES0:

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_IGROUPR<n>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_IGROUPR<n>E is (0x1000 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-4096) MOD 32.
Accessing the GICD_IGROUPR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICD_IGROUPR<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

GICD_IGROUPR<n>E can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1000 + (4 * n)</td>
<td>GICD_IGROUPR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICD_IGRPMODR<n>, Interrupt Group Modifier Registers, n = 0 - 31

The GICD_IGRPMODR<n> characteristics are:

**Purpose**

When GICD_CTLR.DS==0, this register together with the GICD_IGROUPR<n> registers, controls whether the corresponding interrupt is in:

- Secure Group 0.
- Non-secure Group 1.
- Secure Group 1.

**Configuration**

When GICD_CTLR.DS==0, these registers are Secure.

The number of implemented GICD_IGROUPR<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

When GICD_CTLR.ARE_S==0 or GICD_CTLR.DS==1, the GICD_IGRPMODR<n> registers are RES0. An implementation can make these registers RAZ/WI in this case.

**Attributes**

GICD_IGRPMODR<n> is a 32-bit register.

**Field descriptions**

The GICD_IGRPMODR<n> bit assignments are:

<table>
<thead>
<tr>
<th>Group modifier bit</th>
<th>Group status bit</th>
<th>Definition</th>
<th>Short name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>Secure Group 0</td>
<td>G0S</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>Non-secure Group 1</td>
<td>G1NS</td>
</tr>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>Secure Group 1</td>
<td>G1S</td>
</tr>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>Reserved, treated as Non-secure Group 1</td>
<td>-</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_IGRPMODR<n> number, n, is given by n = m DIV 32.
- The offset of the required GICD_IGRPMODR is (0x080 + (4*n)).
- The bit number of the required group modifier bit in this register is m MOD 32.

See GICD_IGROUPR<n> for information about the GICD_IGRPMODR0 reset value.
Accessing the GICD_IGRPMODR<n>

When affinity routing is enabled for Secure state, GICD_IGRPMODR0 is RES0 and equivalent functionality is proved by GICR_IGRPMODR0.

When GICD_CTLR.DS==0, the register is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

---

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

---

**GICD_IGRPMODR<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0D00 + (4 * n)</td>
<td>GICD_IGRPMODR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
The GICD_IGRPMODR<n>E characteristics are:

**Purpose**

When GICD_CTLR_DS==0, this register together with the GICD_IGROUPR<n>E registers, controls whether the corresponding interrupt is in:

- Secure Group 0.
- Non-secure Group 1.
- When System register access is enabled, Secure Group 1.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_IGRPMODR<n>E are RES0.

GICD_IGRPMODR<n>E resets to 0x00000000.

When GICD_TYPER_ESPI==0, these registers are RES0.

When GICD_TYPER_ESPI==1:

- The number of implemented GICD_IGRPMODR<n>E registers is (GICD_TYPER_ESPI_range+1). Registers are numbered from 0.
- When GICD_CTLR_DS==0, this register is Secure.

**Attributes**

GICD_IGRPMODR<n>E is a 32-bit register.

**Field descriptions**

The GICD_IGRPMODR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group modifier bit31</td>
<td>Group modifier bit30</td>
<td>Group modifier bit29</td>
<td>Group modifier bit28</td>
<td>Group modifier bit27</td>
</tr>
</tbody>
</table>

**Group modifier bit<x>, bit [x], for x = 31 to 0**

Group modifier bit. In implementations where affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICD_IGROUPR<n>E to form a 2-bit field that defines an interrupt group:

<table>
<thead>
<tr>
<th>Group modifier bit</th>
<th>Group status bit</th>
<th>Definition</th>
<th>Short name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>Secure Group 0</td>
<td>G0S</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>Non-secure Group 1</td>
<td>G1NS</td>
</tr>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>Secure Group 1</td>
<td>G1S</td>
</tr>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>Reserved, treated as Non-secure Group 1</td>
<td>-</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_IGRPMODR<n>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_IGRPMODR<n>E is (0x3400 + (4*n)).
The bit number of the required group modifier bit in this register is \((m-4096) \mod 32\).

### Accessing the GICD\_IGRPMODR\(<n>\)E

When affinity routing is not enabled for the Security state of an interrupt in GICD\_IGRPMODR\(<n>\)E, the corresponding bit is \texttt{RES0}.

When \texttt{GICD\_CTRL.DS==0}, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICD\_IGRPMODR\(<n>\)E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>(0x3400 + (4 * n))</td>
<td>GICD_IGRPMODR(&lt;n&gt;)E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GICD\_CTRL.DS == 0} accesses to this register are \texttt{RW}.
- When an access is Secure accesses to this register are \texttt{RW}.
- When an access is Non-secure accesses to this register are \texttt{RW}.
GICD_IIDR, Distributor Implementer Identification Register

The GICD_IIDR characteristics are:

**Purpose**

Provides information about the implementer and revision of the Distributor.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states, this register is Common.

**Attributes**

GICD_IIDR is a 32-bit register.

**Field descriptions**

The GICD_IIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ProductID</td>
</tr>
<tr>
<td>30</td>
<td>Reserved</td>
</tr>
<tr>
<td>29</td>
<td>Variant</td>
</tr>
<tr>
<td>28</td>
<td>Revision</td>
</tr>
<tr>
<td>27</td>
<td>Implementer</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ProductID, bits [31:24]**

An IMPLEMENTATION DEFINED product identifier.

**Bits [23:20]**

Reserved, RES0.

**Variant, bits [19:16]**

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish product variants, or major revisions of a product.

**Revision, bits [15:12]**

An IMPLEMENTATION DEFINED revision number. Typically, this field is used to distinguish minor revisions of a product.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the Distributor:

- Bits [11:8] are the JEP106 continuation code of the implementer. For an Arm implementation, this field is 0x4.
- Bit [7] is always 0.
- Bits [6:0] are the JEP106 identity code of the implementer. For an Arm implementation, bits [7:0] are therefore 0x3B.
Accessing the GICD_IIDR

GICD_IIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0008</td>
<td>GICD_IIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.

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The GICD_IPRIORITYR<n> characteristics are:

**Purpose**

Holds the priority of the corresponding interrupt.

**Configuration**

These registers are available in all configurations of the GIC. When GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_IPRIORITYR<n> registers is 8*(GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_IPRIORITYR0 to GICD_IPRIORITYR7 are Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_IPRIORITYR0 to GICD_IPRIORITYR7 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

GICD_IPRIORITYR<n> is a 32-bit register.

**Field descriptions**

The GICD_IPRIORITYR<n> bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Priority_offset_3B | Priority_offset_2B | Priority_offset_1B | Priority_offset_0B |

**Priority_offset_3B, bits [31:24]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to 0.

**Priority_offset_2B, bits [23:16]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to 0.

**Priority_offset_1B, bits [15:8]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to 0.
Interrupt priority value from an **IMPLEMENTATION DEFINED** range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to 0.

For interrupt ID \( m \), when \( \text{DIV} \) and \( \text{MOD} \) are the integer division and modulo operations:

- The corresponding GICD_IPRIORITY\( \langle n \rangle \) number, \( n \), is given by \( n = m \text{ DIV} 4 \).
- The offset of the required GICD_IPRIORITY\( \langle n \rangle \) register is \( (0x400 + (4*n)) \).
- The byte offset of the required Priority field in this register is \( m \text{ MOD} 4 \), where:
  - Byte offset 0 refers to register bits [7:0].
  - Byte offset 1 refers to register bits [15:8].
  - Byte offset 2 refers to register bits [23:16].
  - Byte offset 3 refers to register bits [31:24].

### Accessing the GICD_IPRIORITY\( \langle n \rangle \)

These registers are always used when affinity routing is not enabled. When affinity routing is enabled for the Security state of an interrupt:

- GICR_IPRIORITY\( \langle n \rangle \) is used instead of GICD_IPRIORITY\( \langle n \rangle \) where \( n = 0 \) to 7 (that is, for SGIs and PPIs).
- GICD_IPRIORITY\( \langle n \rangle \) is RAZ/WI where \( n = 0 \) to 7.

These registers are byte-accessible.

A register field corresponding to an unimplemented interrupt is RAZ/WI.

A GIC might implement fewer than eight priority bits, but must implement at least bits [7:4] of each field. In each field, unimplemented bits are RAZ/WI, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

When GICD_CTLR.DS==0:

- A register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
- A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in 'Software accesses of interrupt priority' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

It is **IMPLEMENTATION DEFINED** whether changing the value of a priority field changes the priority of an active interrupt.

---

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

---

**GICD_IPRIORITY\( \langle n \rangle \)** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0400 + (4 * n)</td>
<td>GICD_IPRIORITY( \langle n \rangle )</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
**GICD_IPRIORITYR<n>E, Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC., n = 0 - 255**

The GICD_IPRIORITYR<n>E characteristics are:

**Purpose**

Holds the priority of the corresponding interrupt for each extended SPI supported by the GIC.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_IPRIORITYR<n>E are RES0.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1, the number of implemented GICD_IPRIORITYR<n>E registers is ((GICD_TYPER.ESPI_range+1)*8). Registers are numbered from 0.

**Attributes**

GICD_IPRIORITYR<n>E is a 32-bit register.

**Field descriptions**

The GICD_IPRIORITYR<n>E bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**Priority_offset_3B, bits [31:24]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_2B, bits [23:16]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_1B, bits [15:8]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_0B, bits [7:0]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_IPRIORITYR<n> number, n, is given by \( n = (m - 4096) \text{ DIV } 4 \).
- The offset of the required GICD_IPRIORITYR<n>E register is \( (0\times2000 + (4n)) \).
- The byte offset of the required Priority field in this register is \( m \text{ MOD } 4 \), where:
  - Byte offset 0 refers to register bits \([7:0]\).
  - Byte offset 1 refers to register bits \([15:8]\).
  - Byte offset 2 refers to register bits \([23:16]\).
  - Byte offset 3 refers to register bits \([31:24]\).

### Accessing the GICD_IPRIORITYR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICD-ISACTIVER<n>E, the corresponding bit is **RES0**.

When GICD_CTLR.DS==0:

- A field that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
- A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in Software accesses of interrupt priority.

Bits corresponding to unimplemented interrupts are RAZ/WI.

---

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than once. The effect of the change must be visible in finite time.

---

**GICD_IPRIORITYR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>( 0\times2000 + (4\text{ n}) )</td>
<td>GICD_IPRIORITYR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_IROUTER<n>, Interrupt Routing Registers, n = 32 - 1019

The GICD_IROUTER<n> characteristics are:

**Purpose**

When affinity routing is enabled, provides routing information for the SPI with INTID n.

**Configuration**

These registers are available in all configurations of the GIC. If the GIC implementation supports two Security states, these registers are Common.

The maximum value of n is given by \(32 \times (\text{GICD_TYPER.ITLinesNumber}+1) - 1\). GICD_IROUTER<n> registers where n=0 to 31 are reserved.

**Attributes**

GICD_IROUTER<n> is a 64-bit register.

**Field descriptions**

The GICD_IROUTER<n> bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | RES0 | Aff3 | Aff1 | Aff0 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 | Aff1 |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:40]**

Reserved, RES0.

**Aff3, bits [39:32]**

Affinity level 3, the least significant affinity level field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Interrupt_Routing_Mode, bit [31]**

Interrupt Routing Mode. Defines how SPIs are routed in an affinity hierarchy:

<table>
<thead>
<tr>
<th>Interrupt_Routing_Mode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PE specified by a.b.c.d. In this routing, a, b, c, and d are the values of fields Aff3, Aff2, Aff1, and Aff0 respectively.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to any PE defined as a participating node.</td>
</tr>
</tbody>
</table>

If GICD_IROUTER<n>.IRM == 0 and the affinity path does not correspond to an implemented PE, then if the corresponding interrupt becomes pending behavior is CONSTRAINED UNPREDICTABLE:

- The interrupt is not forwarded to any PE, direct reads return the written value.
• The affinity path is treated as an unknown implemented PE, direct reads return the unknown implemented PE

• The affinity path is treated as an unknown implemented PE, direct reads return the written value

In implementations that do not require 1 of N distribution of SPIs, this bit might be RAZ/WI.

When this bit is set to 1, GICD_IROUTER<n>.{Aff3, Aff2, Aff1, Aff0} are unknown.

---

**Note**

An implementation might choose to make the Aff<n> fields RO when this field is 1.

---

On a Warm reset, this field resets to an architecturally unknown value.

**Bits [30:24]**

Reserved, RES0.

**Aff2, bits [23:16]**

Affinity level 2, an intermediate affinity level field.

On a Warm reset, this field resets to an architecturally unknown value.

**Aff1, bits [15:8]**

Affinity level 1, an intermediate affinity level field.

On a Warm reset, this field resets to an architecturally unknown value.

**Aff0, bits [7:0]**

Affinity level 0, the most significant affinity level field.

On a Warm reset, this field resets to an architecturally unknown value.

For an SPI with INTID m:

• The corresponding GICD_IROUTER<n> register number, n, is given by n = m.
• The offset of the GICD_IROUTER<n> register is 0x6000 + 8n.

---

**Accessing the GICD_IROUTER<n>**

These registers are used only when affinity routing is enabled. When affinity routing is not enabled:

• These registers are RES0. An implementation is permitted to make the register RAZ/WI in this case.
• The GICD_ITARGETSR<n> registers provide interrupt routing information.

---

**Note**

When affinity routing becomes enabled for a Security state (for example, following a reset or following a write to GICD_CTLR) the value of all writeable fields in this register is unknown for that Security state. When the group of an interrupt changes so the ARE setting for the interrupt changes to 1, the value of this register is unknown for that interrupt.

---

If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any GICD_IROUTER<n> registers that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.
For each interrupt, a GIC implementation might support fewer than 256 values for an affinity level. In this case, some bits of the corresponding affinity level field might be RO. Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

**GICD_IROUTER<n>** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x6000 + (8 * n)</td>
<td>GICD_IROUTER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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The GICD_IROUTER<n>E characteristics are:

### Purpose

When affinity routing is enabled, provides routing information for the corresponding SPI in the extended SPI range.

### Configuration

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_IROUTER<n>E are \texttt{RES0}.

RW fields in this register reset to architecturally \texttt{UNKNOWN} values.

When \texttt{GICD_TYPER.ESPI==0}, these registers are \texttt{RES0}.

When \texttt{GICD_TYPER.ESPI==1}, the number of implemented GICD_IROUTER<n>E registers is \(((GICD_TYPER.ESPI\_range+1)*32)-1\). Registers are numbered from 0.

### Attributes

GICD_IROUTER<n>E is a 64-bit register.

### Field descriptions

The GICD_IROUTER<n>E bit assignments are:

<table>
<thead>
<tr>
<th>Bit (Hex)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-40</td>
<td>Reserved, \texttt{RES0}.</td>
</tr>
<tr>
<td>31</td>
<td>\texttt{Aff3}</td>
</tr>
<tr>
<td>30-24</td>
<td>\texttt{RES0}</td>
</tr>
<tr>
<td>23-16</td>
<td>\texttt{Aff2}</td>
</tr>
<tr>
<td>15-8</td>
<td>\texttt{Aff1}</td>
</tr>
<tr>
<td>7-0</td>
<td>\texttt{Aff0}</td>
</tr>
</tbody>
</table>

#### Bits [63:40]

Reserved, \texttt{RES0}.

#### Aff3, bits [39:32]

Affinity level 3, the least significant affinity level field.

#### Interrupt_Routing_Mode, bit [31]

Interrupt Routing Mode. Defines how SPIs are routed in an affinity hierarchy:

<table>
<thead>
<tr>
<th>Interrupt_Routing_Mode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Interrupts routed to the PE specified by a.b.c.d. In this routing, a, b, c, and d are the values of fields Aff3, Aff2, Aff1, and Aff0 respectively.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupts routed to any PE defined as a participating node.</td>
</tr>
</tbody>
</table>

If GICD_IROUTER<n>E.IRM == 0 and the affinity path does not correspond to an implemented PE, then if the corresponding interrupt becomes pending behavior is \texttt{CONSTRAINED UNPREDICTABLE}: 
• The interrupt is not forwarded to any PE, direct reads return the written value
• The affinity path is treated as an **UNKNOWN** implemented PE, direct reads return the **UNKNOWN** implemented PE
• The affinity path is treated as an **UNKNOWN** implemented PE, direct reads return the written value

In implementations that do not require 1 of N distribution of SPIs, this bit might be RAZ/WI.

When this bit is set to 1, GICD_IROUTER<n>E.{Aff3, Aff2, Aff1, Aff0} are **UNKNOWN**.

---

**Note**

An implementation might choose to make the Aff<n> fields RO when this field is 1.

---

**Bits [30:24]**

Reserved, RES0.

**Aff2, bits [23:16]**

Affinity level 2, an intermediate affinity level field.

**Aff1, bits [15:8]**

Affinity level 1, an intermediate affinity level field.

**Aff0, bits [7:0]**

Affinity level 0, the most significant affinity level field.

For an SPI with INTID m:

• The corresponding GICD_IROUTER<n>E register number, n, is given by n = m.
• The offset of the GICD_IROUTER<n>E register is 0x6000 + 8n.

---

**Accessing the GICD_IROUTER<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICD_IROUTER<n>E, the register is RES0.

When GICD_CTLR.DS==0, a register that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICD_IROUTER<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x6000 + (8 * n)</td>
<td>GICD_IROUTER&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When GICD_CTLR.DS == 0 accesses to this register are **RW**.
• When an access is Secure accesses to this register are **RW**.
• When an access is Non-secure accesses to this register are **RW**.
The GICD_ISACTIVER\(<n>\) characteristics are:

### Purpose

Activates the corresponding interrupt. These registers are used when saving and restoring GIC state.

### Configuration

These registers are available in all GIC configurations. If \(\text{GICD_CTLR.DS} = 0\), these registers are Common.

The number of implemented GICD_ISACTIVER\(<n>\) registers is \((\text{GICD_TYPER.ITLinesNumber} + 1)\). Registers are numbered from 0.

GICD_ISACTIVER0 is Banked for each connected PE with \(\text{GICR_TYPER.Processor_Number} < 8\).

Accessing GICD_ISACTIVER0 from a PE with \(\text{GICR_TYPER.Processor_Number} > 7\) is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

### Attributes

GICD_ISACTIVER\(<n>\) is a 32-bit register.

### Field descriptions

The GICD_ISACTIVER\(<n>\) bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_active_bit31</td>
<td>Set_active_bit30</td>
<td>Set_active_bit29</td>
<td>Set_active_bit28</td>
<td>Set_active_bit27</td>
<td>Set_active_bit26</td>
<td>Set_active_bit25</td>
</tr>
</tbody>
</table>

\[\text{Set_active_bit\(<x>\), bit } [x], \text{ for } x = 31 \text{ to } 0\]

Adds the active state to interrupt number \(32n + x\). Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_active_bit(&lt;x&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or is active and pending. If written, activates the corresponding interrupt, if the interrupt is not already active. If the interrupt is already active, the write has no effect. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID \(m\), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ISACTIVER\(<n>\) number, \(n\), is given by \(n = m \text{ DIV } 32\).
- The offset of the required GICD_ISACTIVER is \((0x300 + (4*n))\).
- The bit number of the required group modifier bit in this register is \(m \text{ MOD } 32\).
Accessing the GICD_ISACTIVER<n>

When affinity routing is enabled for the Security state of an interrupt, bits corresponding to SGIs and PPIs are RAZ/WI, and equivalent functionality for SGIs and PPIs is provided by GICR_ISACTIVER0.

Bits corresponding to unimplemented interrupts are RAZ/WI.

If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

The bit reads as one if the status of the interrupt is active or active and pending. GICD_ISPENDR<n> and GICD_ICPENDR<n> provide the pending status of the interrupt.

GICD_ISACTIVER<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0300 + (4 * n)</td>
<td>GICD_ISACTIVER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICD_ISACTIVER<n>E, Interrupt Set-Active Registers (extended SPI range), n = 0 - 31

The GICD_ISACTIVER<n>E characteristics are:

**Purpose**

Adds the active state to the corresponding SPI in the extended SPI range.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ISACTIVER<n>E are RES0.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1, the number of implemented GICD_ISACTIVER<n>E registers is (GICD_TYPER.ESPI_range+1). Registers are numbered from 0.

**Attributes**

GICD_ISACTIVER<n>E is a 32-bit register.

**Field descriptions**

The GICD_ISACTIVER<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_active_bit31</td>
<td>Set_active_bit30</td>
<td>Set_active_bit29</td>
<td>Set_active_bit28</td>
<td>Set_active_bit27</td>
<td>Set_active_bit26</td>
<td>Set_active_bit25</td>
</tr>
</tbody>
</table>

**Set_active_bit<x>, bit [x], for x = 31 to 0**

For the extended SPIs, adds the active state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or active and pending on this PE. If written, activates the corresponding interrupt, if the interrupt is not already active. If the interrupt is already active, the write has no effect. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ISACTIVER<n>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_ISACTIVER<n>E is (0x1A00 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-4096) MOD 32.

**Accessing the GICD_ISACTIVER<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICD_ISACTIVER<n>E, the corresponding bit is RES0.
When $GICD\_CTLR.DS==0$, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**$GICD\_ISACTIVER<n>E$ can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1A00 + (4 * n)</td>
<td>$GICD_ISACTIVER&lt;n&gt;E$</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When $GICD\_CTLR.DS == 0$ accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_ISENABLER<n>, Interrupt Set-Enable Registers, n = 0 - 31

The GICD_ISENABLER<n> characteristics are:

**Purpose**

Enables forwarding of the corresponding interrupt to the CPU interfaces.

**Configuration**

These registers are available in all GIC configurations. If GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_ISENABLER<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_ISENABLER0 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_ISENABLER0 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

GICD_ISENABLER<n> is a 32-bit register.

**Field descriptions**

The GICD_ISENABLER<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_enable_bit31</td>
<td>Set_enable_bit30</td>
<td>Set_enable_bit29</td>
<td>Set_enable_bit28</td>
<td>Set_enable_bit27</td>
<td>Set_enable_bit26</td>
<td>Set_enable_bit25</td>
</tr>
</tbody>
</table>

**Set_enable_bit<x>, bit [x], for x = 31 to 0**

For SPIs and PPIs, controls the forwarding of interrupt number 32n + x to the CPU interfaces. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_enable_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, enables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

For SGIs, the behavior of this bit is IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ISENABLER<n> number, n, is given by n = m DIV 32.
- The offset of the required GICD_ISENABLER is (0x100 + (4*n)).
- The bit number of the required group modifier bit in this register is m MOD 32.
At start-up, and after a reset, a PE can use this register to discover which peripheral INTIDs the GIC supports. If \texttt{GICD\_CTLR.DS==0} in a system that supports EL3, the PE must do this for the Secure view of the available interrupts, and Non-secure software running on the PE must do this discovery after the Secure software has configured interrupts as Group 0/Secure Group 1 and Non-secure Group 1.

### Accessing the GICD\_ISENABLER\<n>\

For SGIs and PPIs:

- When ARE is 1 for the Security state of an interrupt, the field for that interrupt is \texttt{RES0} and an implementation is permitted to make the field RAZ/WI in this case.
- Equivalent functionality is provided by \texttt{GICR\_ISENABLER0}.

Bits corresponding to unimplemented interrupts are RAZ/WI.

When \texttt{GICD\_CTLR.DS==0}, bits corresponding to Group 0 or Secure Group 1 interrupts are RAZ/WI to Non-secure accesses.

It is \texttt{IMPLEMENTATION DEFINED} whether implemented SGIs are permanently enabled, or can be enabled and disabled by writes to \texttt{GICD\_ISENABLER\<n>} and \texttt{GICD\_ICENABLER\<n>} where \(n=0\).

For SPIs and PPIs, each bit controls the forwarding of the corresponding interrupt from the Distributor to the CPU interfaces.

### GICD\_ISENABLER\<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>0x0100+(4*(n))</td>
<td>GICD_ISENABLER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD\_CTRL.DS == 0 accesses to this register are \texttt{RW}.
- When an access is Secure accesses to this register are \texttt{RW}.
- When an access is Non-secure accesses to this register are \texttt{RW}. 

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GICD_ISENABLER<sup>n</sup>E, Interrupt Set-Enable Registers, n = 0 - 31

The GICD_ISENABLER<sup>n</sup>E characteristics are:

**Purpose**

Enables forwarding of the corresponding SPI in the extended SPI range to the CPU interfaces.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ISENABLER<sup>n</sup>E are RES0.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1, the number of implemented GICD_ISENABLER<sup>n</sup>E registers is (GICD_TYPER.ESPI_range+1). Registers are numbered from 0.

**Attributes**

GICD_ISENABLER<sup>n</sup>E is a 32-bit register.

**Field descriptions**

The GICD_ISENABLER<sup>n</sup>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_enable_bit31</td>
<td>Set_enable_bit30</td>
<td>Set_enable_bit29</td>
<td>Set_enable_bit28</td>
<td>Set_enable_bit27</td>
<td>Set_enable_bit26</td>
<td>Set_enable_bit25</td>
</tr>
</tbody>
</table>

**Set_enable_bit<sup>x</sup>, bit [x], for x = 31 to 0**

For the extended SPI range, controls the forwarding of interrupt number x to the CPU interface. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_enable_bit&lt;sup&gt;x&lt;/sup&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, enables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ISENABLER<sup>n</sup>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_ISENABLER<sup>n</sup>E is (0x1200 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-4096) MOD 32.
Accessing the GICD_ISENABLER<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICD_ISENABLER<n>E, the corresponding bit is RES0.

When GICD_CTRLR.DS == 0, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

GICD_ISENABLER<n>E can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1200 + (4 * n)</td>
<td>GICD_ISENABLER&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICD_ISPENDR<n>, Interrupt Set-Pending Registers, n = 0 - 31

The GICD_ISPENDR<n> characteristics are:

**Purpose**

Adds the pending state to the corresponding interrupt.

**Configuration**

These registers are available in all GIC configurations. If GICD_CTLR.DS==0, these registers are Common.

The number of implemented GICD_ISPENDR<n> registers is (GICD_TYPER.ITLinesNumber+1). Registers are numbered from 0.

GICD_ISPENDR0 is Banked for each connected PE with GICR_TYPER.Processor_Number < 8.

Accessing GICD_ISPENDR0 from a PE with GICR_TYPER.Processor_Number > 7 is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

GICD_ISPENDR<n> is a 32-bit register.

**Field descriptions**

The GICD_ISPENDR<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_pending_bit31</td>
<td>Set_pending_bit30</td>
<td>Set_pending_bit29</td>
<td>Set_pending_bit28</td>
<td>Set_pending_bit27</td>
<td>Set_pending_bit26</td>
</tr>
</tbody>
</table>

**Set_pending_bit<x>, bit [x], for x = 31 to 0**

For SPIs and PPIs, adds the pending state to interrupt number 32n + x. Reads and writes have the following behavior:
<table>
<thead>
<tr>
<th>Set_pending bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending on any PE. If written, has no effect.</td>
</tr>
</tbody>
</table>
| 0b1            | If read, indicates that the corresponding interrupt is pending, or active and pending:  
  • On this PE if the interrupt is an SGI or PPI.  
  • On at least one PE if the interrupt is an SPI.  
If written, changes the state of the corresponding interrupt from inactive to pending, or from active to active and pending. This has no effect in the following cases:  
  • If the interrupt is an SGI. The pending state of an SGI can be set using GICD_SPENDSGIR<n>.  
  • If the interrupt is not inactive and is not active.  
  • If the interrupt is already pending because of a write to GICD_ISPENDR<n>.  
  • If the interrupt is already pending because the corresponding interrupt signal is asserted. In this case, the interrupt remains pending if the interrupt signal is deasserted. |

On a Warm reset, this field resets to 0.

### Accessing the GICD_ISPENDR<n>

Set-pending bits for SGIs are read-only and ignore writes. The Set-pending bits for SGIs are provided as GICD_SPENDSGIR<n>.

When affinity routing is enabled for the Security state of an interrupt:

- Bits corresponding to SGIs and PPIs are RAZ/WI, and equivalent functionality for SGIs and PPIs is provided by GICR_ISPENDR0.
- Bits corresponding to Group 0 and Group 1 Secure interrupts can only be set by Secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

**GICD_ISPENDR<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0200 + (4 * n)</td>
<td>GICD_ISPENDR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
**Purpose**

Adds the pending state to the corresponding SPI in the extended SPI range.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_ISPENDR<n>E are RES0.

When GICD_TYPER_ESPI==0, these registers are RES0.

When GICD_TYPER_ESPI==1, the number of implemented GICD_ISPENDR<n>E registers is (GICD_TYPER_ESPI_range+1). Registers are numbered from 0.

**Attributes**

GICD_ISPENDR<n>E is a 32-bit register.

**Field descriptions**

The GICD_ISPENDR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Assignments</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_pending_bit31</td>
<td>31</td>
<td>If read, indicates that the corresponding interrupt is not pending. If written, has no effect.</td>
</tr>
<tr>
<td>Set_pending_bit30</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>Set_pending_bit29</td>
<td>29</td>
<td></td>
</tr>
<tr>
<td>Set_pending_bit28</td>
<td>28</td>
<td></td>
</tr>
<tr>
<td>Set_pending_bit27</td>
<td>27</td>
<td></td>
</tr>
<tr>
<td>Set_pending_bit26</td>
<td>26</td>
<td></td>
</tr>
</tbody>
</table>

For the extended SPIs, adds the pending state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending. If written, has no effect.</td>
</tr>
</tbody>
</table>
| 0b1               | If read, indicates that the corresponding interrupt is pending, or active and pending. If written, changes the state of the corresponding interrupt from inactive to pending, or from active to active and pending. This has no effect in the following cases:  
  - If the interrupt is already pending because of a write to GICD_ISPENDR<n>E.  
  - If the interrupt is already pending because the corresponding interrupt signal is asserted. In this case, the interrupt remains pending if the interrupt signal is deasserted. |

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ISPENDR<n>E number, n, is given by n = (m-4096) DIV 32.
- The offset of the required GICD_ISPENDR<n>E is (0x1600 + (4*n)).
The bit number of the required group modifier bit in this register is \((m-4096) \mod 32\).

### Accessing the GICD_ISPENDR\(n\)E

When affinity routing is not enabled for the Security state of an interrupt in GICD_ISPENDR\(n\)E, the corresponding bit is RES0.

When \texttt{GICD_CTLR.DS}==0, bits corresponding to Secure SPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICD_ISPENDR\(n\)E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x1600 + (4 * (n))</td>
<td>GICD_ISPENDR(n)E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GICD_CTLR.DS == 0} accesses to this register are \textbf{RW}.
- When an access is Secure accesses to this register are \textbf{RW}.
- When an access is Non-secure accesses to this register are \textbf{RW}.
The GICD_ITARGETSR<\text{n}> characteristics are:

**Purpose**

When affinity routing is not enabled, holds the list of target PEs for the interrupt. That is, it holds the list of CPU interfaces to which the Distributor forwards the interrupt if it is asserted and has sufficient priority.

**Configuration**

These registers are available in all configurations of the GIC. When \text{GICD_CTRLR.DS==0}, these registers are Common.

The number of implemented GICD_ITARGETSR<n> registers is 8*(\text{GICD_TYPER.ITLinesNumber}+1). Registers are numbered from 0.

GICD_ITARGETSR0 to GICD_ITARGETSR7 are Banked for each connected PE with \text{GICR_TYPER.Processor_Number < 8}.

Accessing GICD_ITARGETSR0 to GICD_ITARGETSR7 from a PE with \text{GICR_TYPER.Processor_Number > 7} is CONSTRAINED UNPREDICTABLE:

- Register is RAZ/WI.
- An UNKNOWN banked copy of the register is accessed.

**Attributes**

\text{GICD_ITARGETSR<n>} is a 32-bit register.

**Field descriptions**

The GICD_ITARGETSR<n> bit assignments are:

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU_targets_offset_3B</td>
</tr>
</tbody>
</table>

PEs in the system number from 0, and each bit in a PE targets field refers to the corresponding PE. For example, a value of 0x3 means that the Pending interrupt is sent to PEs 0 and 1. For GICD_ITARGETSR0-GICD_ITARGETSR7, a read of any targets field returns the number of the PE performing the read.

**CPU_targets_offset_3B**, bits [31:24]

PE targets for an interrupt, at byte offset 3.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CPU_targets_offset_2B**, bits [23:16]

PE targets for an interrupt, at byte offset 2.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**CPU_targets_offset_1B**, bits [15:8]

PE targets for an interrupt, at byte offset 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
**CPU_targets_offset_0B, bits [7:0]**

PE targets for an interrupt, at byte offset 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

The bits that are set to 1 in the PE targets field determine which PEs are targeted:

<table>
<thead>
<tr>
<th>Value of PE targets field</th>
<th>Interrupt targets</th>
</tr>
</thead>
<tbody>
<tr>
<td>0bxxxxxxx1</td>
<td>CPU interface 0</td>
</tr>
<tr>
<td>0bxxxxx1xx</td>
<td>CPU interface 1</td>
</tr>
<tr>
<td>0bxxxx1xxxx</td>
<td>CPU interface 2</td>
</tr>
<tr>
<td>0bxxxx1xxxx</td>
<td>CPU interface 3</td>
</tr>
<tr>
<td>0bx1xxxxxx</td>
<td>CPU interface 4</td>
</tr>
<tr>
<td>0bx1xxxxxx</td>
<td>CPU interface 5</td>
</tr>
<tr>
<td>0b1xxxxxxx</td>
<td>CPU interface 6</td>
</tr>
<tr>
<td>0b1xxxxxxx</td>
<td>CPU interface 7</td>
</tr>
</tbody>
</table>

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_ITARGETSR<n> number, n, is given by \( n = m \text{ DIV 4} \).
- The offset of the required GICD_ITARGETSR<n> register is \((0x800 + (4*n))\).
- The byte offset of the required Priority field in this register is m MOD 4, where:
  - Byte offset 0 refers to register bits [7:0].
  - Byte offset 1 refers to register bits [15:8].
  - Byte offset 2 refers to register bits [23:16].
  - Byte offset 3 refers to register bits [31:24].

Software can write to these registers at any time. Any change to a targets field value:

- Has no effect on any active interrupt. This means that removing a CPU interface from a targets list does not cancel an active state for interrupts on that CPU interface. There is no effect on interrupts that are active and pending until the active status is cleared, at which time it is treated as a pending interrupt.
- Has an effect on any pending interrupts. This means:
  - Enables the CPU interface to be chosen as a target for the pending interrupt using an IMPLEMENTATIONDEFINED mechanism.
  - Removing a CPU interface from the target list of a pending interrupt removes the pending state of the interrupt on that CPU interface.

**Accessing the GICD_ITARGETSR<n>**

These registers are used when affinity routing is not enabled. When affinity routing is enabled for the Security state of an interrupt, the target PEs for an interrupt are defined by GICD_IROUTER<n> and the associated byte in GICD_ITARGETSR<n> is RES0. An implementation is permitted to make the byte RAZ/WI in this case.

- These registers are byte-accessible.
- A register field corresponding to an unimplemented interrupt is RAZ/WI.
- A field bit corresponding to an unimplemented CPU interface is RAZ/WI.
- GICD_ITARGETSR0-GICD_ITARGETSR7 are read-only. Each field returns a value that corresponds only to the PE reading the register.
- It is IMPLEMENTATIONDEFINED which, if any, SPIs are statically configured in hardware. The field for such an SPI is read-only, and returns a value that indicates the PE targets for the interrupt.
- If GICD_CTLR.DS==0, unless the GICD_NSACR<n> registers permit Non-secure software to control Group 0 and Secure Group 1 interrupts, any bits that correspond to Group 0 or Secure Group 1 interrupts are accessible only by Secure accesses and are RAZ/WI to Non-secure accesses.

In a single connected PE implementation, all interrupts target one PE, and these registers are RAZ/WI.

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.
GICD_ITARGETSR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0800 + (4 * n)</td>
<td>GICD_ITARGETSR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_NSACR<n>, Non-secure Access Control Registers, n = 0 - 63

The GICD_NSACR<n> characteristics are:

**Purpose**

Enables Secure software to permit Non-secure software on a particular PE to create and control Group 0 interrupts.

**Configuration**

The concept of selective enabling of Non-secure access to Group 0 and Secure Group 1 interrupts applies to SGIs and SPIs.

GICD_NSACR0 is a Banked register used for SGIs. A copy is provided for every PE that has a CPU interface and that supports this feature.

**Attributes**

GICD_NSACR<n> is a 32-bit register.

**Field descriptions**

The GICD_NSACR<n> bit assignments are:

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14
NS_access15 NS_access14 NS_access13 NS_access12 NS_access11 NS_access10 NS_access9 NS_access8 NS_access7
```

**NS_access<x>, bits [2x+1:2x], for x = 15 to 0**

Controls Non-secure access of the interrupt with ID 16n + x.

If the corresponding interrupt does not support configurable Non-secure access, the field is RAZ/WI.

Otherwise, the field is RW and determines the level of Non-secure control permitted if the interrupt is a Secure interrupt. If the interrupt is a Non-secure interrupt, this field is ignored.

The possible values of each 2-bit field are:
NS_access<x> | Meaning
---|---
0b00 | No Non-secure access is permitted to fields associated with the corresponding interrupt.
0b01 | Non-secure read and write access is permitted to setting pending bits in GICD_ISPENDR<n> associated with the corresponding interrupt. A Non-secure write access to GICD_SETSPI_NSR is permitted to set the pending state of the corresponding interrupt. A Non-secure write access to GICD_SGIR is permitted to generate a Secure SGI for the corresponding interrupt. An implementation might also provide read access to clear-pending bits in GICD_ICPENDR<n> associated with the corresponding interrupt.
0b10 | As 0b01, but adds Non-secure read and write access permission to fields associated with the corresponding interrupt in the GICD_ICPENDR<n> registers. A Non-secure write access to GICD_CLRSPI_NSR is permitted to clear the pending state of the corresponding interrupt. Also adds Non-secure read access permission to fields associated with the corresponding interrupt in the GICD_ISACTIVER<n> and GICD_ICACTIVER<n> registers.
0b11 | For GICD_NSACR0 this encoding is reserved and treated as 10. For all other GICD_NSACR<n> registers this encoding is treated as 0b10, but adds Non-secure read and write access permission to GICD_ITARGETSR<n> and GICD_IROUTER<n> fields associated with the corresponding interrupt.

On a Warm reset, this field resets to 0.

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_NSACR<n> number, n, is given by n = m DIV 16.
- The offset of the required GICD_NSACR<n> register is (0xE00 + (4*n)).

**Note**

Because each field in this register comprises two bits, GICD_NSACR0 controls access rights to SGI registers, GICD_NSACR1 controls access to PPI registers (and is always RAZ/WI), and all other GICD_NSACR<n> registers control access to SPI registers.

For compatibility with GICv2, writes to GICD_NSACR0 for a particular PE must be coordinated within the Distributor and must update GICR_NSACR for the Redistributor associated with that PE.

### Accessing the GICD_NSACR<n>

These registers are always used when affinity routing is not enabled. When affinity routing is enabled for the Secure state, GICD_NSACR0 is RES0 and GICR_NSACR provides equivalent functionality for SGIs.

These registers do not support PPIs, therefore GICD_NSACR1 is RAZ/WI.

**GICD_NSACR<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x00E00 + (4 * n)</td>
<td>GICD_NSACR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 1 accesses to this register are RAZ/WI.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RAZ/WI.
The GICD_NSACR<n>E characteristics are:

**Purpose**

Enables Secure software to permit Non-secure software on a particular PE to create and control Group 0 interrupts.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICD_NSACR<n>E are RES0.

When GICD_TYPER.ESPI==0, these registers are RES0.

When GICD_TYPER.ESPI==1, the number of implemented GICD_ICFGR<n>E registers is ((GICD_TYPER.ESPI_range+1)*2). Registers are numbered from 0.

**Attributes**

GICD_NSACR<n>E is a 32-bit register.

**Field descriptions**

The GICD_NSACR<n>E bit assignments are:

```
 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14
NS_access15 NS_access14 NS_access13 NS_access12 NS_access11 NS_access10 NS_access9 NS_access8 NS_access7
```

**NS_access<x>>, bits [2x+1:2x], for x = 15 to 0**

Controls Non-secure access of the interrupt with ID 16n + x.

If the corresponding interrupt does not support configurable Non-secure access, the field is RAZ/WI.

Otherwise, the field is RW and determines the level of Non-secure control permitted if the interrupt is a Secure interrupt. If the interrupt is a Non-secure interrupt, this field is ignored.

The possible values of each 2-bit field are:
<table>
<thead>
<tr>
<th>NS_access&lt;0x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>No Non-secure access is permitted to fields associated with the corresponding interrupt.</td>
</tr>
<tr>
<td>0b01</td>
<td>Non-secure read and write access is permitted to set-pending bits in GICD_ISPENDR&lt;n&gt;E associated with the corresponding interrupt. A Non-secure write access to GICD_SETSPI_NSR is permitted to set the pending state of the corresponding interrupt.</td>
</tr>
<tr>
<td>0b10</td>
<td>As 0b01, but adds Non-secure read and write access permission to fields associated with the corresponding interrupt in the GICD_ICPENDR&lt;n&gt;E registers. A Non-secure write access to GICD_CLRSPN_NSR is permitted to clear the pending state of the corresponding interrupt. Also adds Non-secure read access permission to fields associated with the corresponding interrupt in the GICD_ISACTIVER&lt;n&gt;E and GICD_ICACTIVER&lt;n&gt;E registers.</td>
</tr>
<tr>
<td>0b11</td>
<td>This encoding is treated as 0b10, but adds Non-secure read and write access permission to GICD_IROUTER&lt;n&gt;E fields associated with the corresponding interrupt.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_NSACR<n>E number, n, is given by \( n = (m - 4096) \text{ DIV } 16 \).
- The offset of the required GICD_NSACR<n>E register is \( \text{0x3600 + (4*n)} \).

### Accessing the GICD_NSACR<n>E

GICD_NSACR<n>E can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x3600 + (4*n)</td>
<td>GICD_NSACR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 1 accesses to this register are RAZ/WI.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RAZ/WI.
The GICD_SETSPI_NSR characteristics are:

**Purpose**

Adds the pending state to a valid SPI if permitted by the Security state of the access and the GICD_NSACR<n> value for that SPI.

A write to this register changes the state of an inactive SPI to pending, and the state of an active SPI to active and pending.

**Configuration**

If GICD_TYPER.MBIS == 0, this register is reserved.

When GICD_CTLR.DS==1, this register provides functionality for all SPIs.

**Attributes**

GICD_SETSPI_NSR is a 32-bit register.

**Field descriptions**

The GICD_SETSPI_NSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

**Bits [31:13]**

Reserved, RES0.

**INTID, bits [12:0]**

The INTID of the SPI.

The function of this register depends on whether the targeted SPI is configured to be an edge-triggered or level-sensitive interrupt:

- For an edge-triggered interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will stop being pending on activation, or if the pending state is removed by a write to GICD_CLRSPISR_NSR, GICD_CLRSPISR_SR, or GICD_ICPENDR<n>.
- For a level-sensitive interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will remain pending until it is deasserted by a write to GICD_CLRSPISR_NSR or GICD_CLRSPISR_SR. If the interrupt is activated between having the pending state added and being deactivated, then the interrupt will be active and pending.

**Accessing the GICD_SETSPI_NSR**

Writes to this register have no effect if:

- The value written specifies a Secure SPI, the value is written by a Non-secure access, and the value of the corresponding GICD_NSACR<n> register is 0.
- The value written specifies an invalid SPI.
- The SPI is already pending.
16-bit accesses to bits [15:0] of this register must be supported.

Note

A Secure access to this register can set the pending state of any valid SPI.

**GICD_SETSPI_NS R can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0040</td>
<td>GICD_SETSPI_NS R</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GIC_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
GICD_SETSPI_SR, Set Secure SPI Pending Register

The GICD_SETSPI_SR characteristics are:

Purpose

Adds the pending state to a valid SPI.

A write to this register changes the state of an inactive SPI to pending, and the state of an active SPI to active and pending.

Configuration

If GICD_TYPER.MBIS == 0, this register is reserved.

When GICD_CTLR.DS==1, this register is WI.

Attributes

GICD_SETSPI_SR is a 32-bit register.

Field descriptions

The GICD_SETSPI_SR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

Bits [31:13]

Reserved, RES0.

INTID, bits [12:0]

The INTID of the SPI.

The function of this register depends on whether the targeted SPI is configured to be an edge-triggered or level-sensitive interrupt:

- For an edge-triggered interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will stop being pending on activation, or if the pending state is removed by a write to GICD_CLRSPI_NSR, GICD_CLRSPI_SR, or GICD_ICPNDR<n>.
- For a level-sensitive interrupt, a write to GICD_SETSPI_NSR or GICD_SETSPI_SR adds the pending state to the targeted interrupt. It will remain pending until it is deasserted by a write to GICD_CLRPI_NSR or GICD_CLRPI_SR. If the interrupt is activated between having the pending state added and being deasserted, then the interrupt will be active and pending.

Accessing the GICD_SETSPI_SR

Writes to this register have no effect if:

- The value is written by a Non-secure access.
- The value written specifies an invalid SPI.
- The SPI is already pending.

16-bit accesses to bits [15:0] of this register must be supported.
GICD_SETSPI_SR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0050</td>
<td>GICD_SETSPI_SR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WI**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WI**.
GICD_SGIR, Software Generated Interrupt Register

The GICD_SGIR characteristics are:

**Purpose**

Controls the generation of SGIs.

**Configuration**

This register is available in all configurations of the GIC. If the GIC supports two Security states this register is Common.

**Attributes**

GICD_SGIR is a 32-bit register.

**Field descriptions**

The GICD_SGIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | TargetListFilter | CPUTargetList | NSATT | RES0 | INTID |

**Bits [31:26]**

Reserved, RES0.

**TargetListFilter, bits [25:24]**

Determines how the Distributor processes the requested SGI.

<table>
<thead>
<tr>
<th>TargetListFilter</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Forward the interrupt to the CPU interfaces specified by GICD_SGIR.CPUTargetList.</td>
</tr>
<tr>
<td>0b01</td>
<td>Forward the interrupt to all CPU interfaces except that of the PE that requested the interrupt.</td>
</tr>
<tr>
<td>0b10</td>
<td>Forward the interrupt only to the CPU interface of the PE that requested the interrupt.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

**CPUTargetList, bits [23:16]**

When GICD_SGIR.TargetListFilter is 0b00, this field defines the CPU interfaces to which the Distributor must forward the interrupt.

Each bit of the field refers to the corresponding CPU interface. For example, CPUTargetList[0] corresponds to interface 0. Setting a bit to 1 indicates that the interrupt must be forwarded to the corresponding interface.

If this field is 0b00000000 when GICD_SGIR.TargetListFilter is 0b00, the Distributor does not forward the interrupt to any CPU interface.

**NSATT, bit [15]**

Specifies the required group of the SGI.
### NSATT

<table>
<thead>
<tr>
<th>NSATT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Forward the SGI specified in the INTID field to a specified CPU interface only if the SGI is configured as Group 0 on that interface.</td>
</tr>
<tr>
<td>0b1</td>
<td>Forward the SGI specified in the INTID field to a specified CPU interface only if the SGI is configured as Group 1 on that interface.</td>
</tr>
</tbody>
</table>

This field is writable only by a Secure access. Non-secure accesses can also generate Group 0 interrupts, if allowed to do so by GICD_NSACR0. Otherwise, Non-secure writes to GICD_SGIR generate an SGI only if the specified SGI is programmed as Group 1, regardless of the value of bit [15] of the write.

#### Bits [14:4]

Reserved, RES0.

#### INTID, bits [3:0]

The INTID of the SGI to forward to the specified CPU interfaces.

### Accessing the GICD_SGIR

This register is used only when affinity routing is not enabled. When affinity routing is enabled, this register is RES0.

It is **IMPLEMENTATION DEFINED** whether this register has any effect when the forwarding of interrupts by the Distributor is disabled by GICD_CTLR.

**GICD_SGIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0F00</td>
<td>GICD_SGIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
The GICD_SPENDSGIR\(n\) characteristics are:

### Purpose

Add the pending state to an SGI.

A write to this register changes the state of an inactive SGI to pending, and the state of an active SGI to active and pending.

### Configuration

Four SGI set-pending registers are implemented. Each register contains eight set-pending bits for each of four SGIs, for a total of 16 possible SGIs.

In multiprocessor implementations, each PE has a copy of these registers.

### Attributes

GICD_SPENDSGIR\(n\) is a 32-bit register.

### Field descriptions

The GICD_SPENDSGIR\(n\) bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>SGI_set_pending_bits3</th>
<th>SGI_set_pending_bits2</th>
<th>SGI_set_pending_bits1</th>
<th>SGI_set_pending_bits0</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
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<tr>
<td>30</td>
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<td>1</td>
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<tr>
<td>0</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

SGI_set_pending_bits\(x\), bits \([8x+7:8x]\), for \(x = 3\) to \(0\)

Add the pending state to SGI number \(4n + x\) for the PE corresponding to the bit number written to.

Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>SGI_set_pending_bits(x)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>If read, indicates that the SGI from the corresponding PE is not pending and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0x01</td>
<td>If read, indicates that the SGI from the corresponding PE is pending or is active and pending. If written, adds the pending state to the SGI for the corresponding PE.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For SGI ID \(m\), generated by processing element C writing to the corresponding GICD_SGIR field, where DIV and MOD are the integer division and modulo operations:

- The corresponding GICD_SPENDSGIR\(n\) number is given by \(n = m \text{ DIV} 4\).
- The offset of the required register is \((0xF20 + (4n))\).
- The offset of the required field within the register GICD_SPENDSGIR\(n\) is given by \(m \text{ MOD} 4\).
- The required bit in the 8-bit SGI set-pending field \(m\) is bit C.
Accessing the GICD_SPENDSGIR<n>

These registers are used only when affinity routing is not enabled. When affinity routing is enabled for the Security state of an interrupt then the bit associated with SGI in that Security state is RES0. An implementation is permitted to make the register RAZ/WI in this case.

A register bit that corresponds to an unimplemented SGI is RAZ/WI.

These registers are byte-accessible.

If the GIC implementation supports two Security states:

- A register bit that corresponds to a Group 0 interrupt is RAZ/WI to Non-secure accesses.
- Register bits corresponding to unimplemented PEs are RAZ/WI.

GICD_SPENDSGIR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0F20 + (4 * n)</td>
<td>GICD_SPENDSGIR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICD_STATUSR, Error Reporting Status Register

The GICD_STATUSR characteristics are:

Purpose

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

Configuration

If the GIC implementation supports two Security states this register is Banked to provide Secure and Non-secure copies.

Attributes

GICD_STATUSR is a 32-bit register.

Field descriptions

The GICD_STATUSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved</td>
</tr>
<tr>
<td>30</td>
<td>Reserved</td>
</tr>
<tr>
<td>29</td>
<td>Reserved</td>
</tr>
<tr>
<td>28</td>
<td>Reserved</td>
</tr>
<tr>
<td>27</td>
<td>Reserved</td>
</tr>
<tr>
<td>26</td>
<td>Reserved</td>
</tr>
<tr>
<td>25</td>
<td>Reserved</td>
</tr>
<tr>
<td>24</td>
<td>Reserved</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
</tr>
<tr>
<td>22</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>Reserved</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
</tr>
<tr>
<td>19</td>
<td>Reserved</td>
</tr>
<tr>
<td>18</td>
<td>Reserved</td>
</tr>
<tr>
<td>17</td>
<td>Reserved</td>
</tr>
<tr>
<td>16</td>
<td>Reserved</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
</tr>
<tr>
<td>14</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

Bits [31:4]

Reserved, RES0.

WROD, bit [3]

Write to an RO location.

<table>
<thead>
<tr>
<th>WROD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to an RO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

RWOD, bit [2]

Read of a WO location.

<table>
<thead>
<tr>
<th>RWOD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a WO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

WRD, bit [1]

Write to a reserved location.
When a violation is detected, software must write 1 to this register to reset it.

**RRD, bit [0]**

Read of a reserved location.

<table>
<thead>
<tr>
<th>WRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**Accessing the GICD_STATUSR**

This is an optional register. If the register is not implemented, the location is RAZ/WI.

**GICD_STATUSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0010</td>
<td>GICD_STATUSR (S)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0010</td>
<td>GICD_STATUSR (NS)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICD_TYPER, Interrupt Controller Type Register

The GICD_TYPER characteristics are:

**Purpose**

Provides information about what features the GIC implementation supports. It indicates:

- Whether the GIC implementation supports two Security states.
- The maximum number of INTIDs that the GIC implementation supports.
- The number of PEs that can be used as interrupt targets.

**Configuration**

This register is available in all configurations of the GIC. When $\text{GICD_CTLR.DS}=0$, this register is Common.

**Attributes**

GICD_TYPER is a 32-bit register.

**Field descriptions**

The GICD_TYPER bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>ESPI_range</td>
<td>RSS</td>
<td>No1N</td>
<td>IDbits</td>
<td>DVI</td>
<td>LPIS</td>
<td>MBIS</td>
<td>num_LPIs</td>
<td>SecurityExtn</td>
<td>RES0</td>
<td>ESPe</td>
<td>CPU_number</td>
<td>ITLinesNumber</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**ESPI_range, bits [31:27]**

*When GICD_TYPER.ESPI == 1:*

Indicates the maximum INTID in the Extended SPI range.

Maximum Extended SPI INTID is $(32 \times (\text{ESPI\_range} + 1) + 4095)$

*Otherwise:*

Reserved, RES0.

**RSS, bit [26]**

Range Selector Support.

<table>
<thead>
<tr>
<th>RSS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The IRI supports targeted SGIs with affinity level 0 values of 0 - 15.</td>
</tr>
<tr>
<td>0b1</td>
<td>The IRI supports targeted SGIs with affinity level 0 values of 0 - 255.</td>
</tr>
</tbody>
</table>

**No1N, bit [25]**

Indicates whether 1 of N SPI interrupts are supported.

<table>
<thead>
<tr>
<th>No1N</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>1 of N SPI interrupts are supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>1 of N SPI interrupts are not supported.</td>
</tr>
</tbody>
</table>
A3V, bit [24]

Affinity 3 valid. Indicates whether the Distributor supports nonzero values of Affinity level 3.

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The Distributor only supports zero values of Affinity level 3.</td>
</tr>
<tr>
<td>0b1</td>
<td>The Distributor supports nonzero values of Affinity level 3.</td>
</tr>
</tbody>
</table>

IDbits, bits [23:19]

The number of interrupt identifier bits supported, minus one.

DVIS, bit [18]

When FEAT_GICv4 is implemented:

Indicates whether the implementation supports Direct Virtual LPI injection.

<table>
<thead>
<tr>
<th>DVIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation does not support Direct Virtual LPI injection.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports Direct Virtual LPI injection.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

LPIS, bit [17]

Indicates whether the implementation supports LPIs.

<table>
<thead>
<tr>
<th>LPIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation does not support LPIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports LPIs.</td>
</tr>
</tbody>
</table>

MBIS, bit [16]

Indicates whether the implementation supports message-based interrupts by writing to Distributor registers.

<table>
<thead>
<tr>
<th>MBIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation does not support message-based interrupts by writing to Distributor registers. The GICD_CLRSPI_NSR, GICD_SETSPI_NSR, GICD_CLRSPI_SR, and GICD_SETSPI_SR registers are reserved.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports message-based interrupts by writing to the GICD_CLRSPI_NSR, GICD_SETSPI_NSR, GICD_CLRSPI_SR, or GICD_SETSPI_SR registers.</td>
</tr>
</tbody>
</table>

num_LPIs, bits [15:11]

Number of supported LPIs.

- 0b000000 Number of LPIs as indicated by GICD_TYPER.IDbits.
- All other values Number of LPIs supported is $2^{(\text{num}_\text{LPIs}+1)}$.
  - Available LPI INTIDs are $8192..(8192 + 2^{(\text{num}_\text{LPIs}+1)} - 1)$.
  - This field cannot indicate a maximum LPI INTID greater than that indicated by GICD_TYPER.IDbits.

When the supported INTID width is less than 14 bits, this field is RES0 and no LPIs are supported.
SecurityExtn, bit [10]

Indicates whether the GIC implementation supports two Security states:

When `GICD_CTLR.DS == 1`, this field is RAZ.

<table>
<thead>
<tr>
<th>SecurityExtn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The GIC implementation supports only a single Security state.</td>
</tr>
<tr>
<td>0b1</td>
<td>The GIC implementation supports two Security states.</td>
</tr>
</tbody>
</table>

Bit [9]

Reserved, RES0.

ESPI, bit [8]

Extended SPI

<table>
<thead>
<tr>
<th>ESPI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Extended SPI range not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Extended SPI range implemented.</td>
</tr>
</tbody>
</table>

CPUNumber, bits [7:5]

Reports the number of PEs that can be used when affinity routing is not enabled, minus 1.

These PEs must be numbered contiguously from zero, but the relationship between this number and the affinity hierarchy from MPIDR is IMPLEMENTATION DEFINED. If the implementation does not support ARE being zero, this field is 000.

ITLinesNumber, bits [4:0]

For the INTID range 32 to 1019, indicates the maximum SPI supported.

If the value of this field is N, the maximum SPI INTID is 32(N+1) minus 1. For example, 00011 specifies that the maximum SPI INTID in is 127.

Regardless of the range of INTIDs defined by this field, interrupt IDs 1020-1023 are reserved for special purposes.

A value of 0 indicates no SPIs are support.

The ITLinesNumber field only indicates the maximum number of SPIs that the GIC implementation might support. This value determines the number of instances of the following interrupt registers:

- `GICD_IGROUPR<n>`.
- `GICD_ISENABLER<n>`.
- `GICD_ICENABLER<n>`.
- `GICD_ISPENDR<n>`.
- `GICD_ICPENDR<n>`.
- `GICD_ICACTIVER<n>`.
- `GICD_ICFGR<n>`.
- `GICD_ITARGETSR<n>`.

The GIC architecture does not require a GIC implementation to support a continuous range of SPI interrupt IDs. Software must check which SPI INTIDs are supported, up to the maximum value indicated by `GICD_TYPER.ITLinesNumber`. 
Accessing the GICD_TYPER

GICD_TYPER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x0004</td>
<td>GICD_TYPER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
The GICD_TYPER2 characteristics are:

**Purpose**

Provides information about which features the GIC implementation supports.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICD_TYPER2 are RES0.

When GICD_CTLR.DS == 0, this register is Common.

**Attributes**

GICD_TYPER2 is a 32-bit register.

**Field descriptions**

The GICD_TYPER2 bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>RES0</th>
<th>nASSGICap</th>
<th>VIL</th>
<th>RES0</th>
<th>VID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
</tr>
<tr>
<td></td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:9]**

Reserved, RES0.

**nASSGICap, bit [8]**

Indicates whether SGIs can be configured to not have an active state.

<table>
<thead>
<tr>
<th>nASSGICap</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>SGIs have an active state.</td>
</tr>
<tr>
<td>0b1</td>
<td>SGIs can be globally configured not to have an active state.</td>
</tr>
</tbody>
</table>

This bit is RES0 on implementations that support two Security states.

**VIL, bit [7]**

Indicates whether 16 bits of vPEID are implemented.

<table>
<thead>
<tr>
<th>VIL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GIC supports 16-bit vPEID.</td>
</tr>
<tr>
<td>0b1</td>
<td>GIC supports GICD_TYPER2.VID + 1 bits of vPEID.</td>
</tr>
</tbody>
</table>

**Bits [6:5]**

Reserved, RES0.

**VID, bits [4:0]**

When GICD_TYPER2.VIL == 1, the number of bits is equal to the bits of vPEID minus one.
When GICD_TYPER2.VIL == 0, this field is RES0.

**Accessing the GICD_TYPER2**

**GICD_TYPER2 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Distributor</td>
<td>0x000C</td>
<td>GICD_TYPER2</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
The GICH_APR<n> characteristics are:

**Purpose**

These registers track which preemption levels are active in the virtual CPU interface, and indicate the current active priority. Corresponding bits are set to 1 in this register when an interrupt is acknowledged, based on GICH_LR<n>.Priority, and the least significant bit set is cleared on EOI.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

The number of registers required depends on how many bits are implemented in GICH_LR<n>.Priority:

- When 5 priority bits are implemented, 1 register is required (GICH_APR0).
- When 6 priority bits are implemented, 2 registers are required (GICH_APR0, GICH_APR1).
- When 7 priority bits are implemented, 4 registers are required (GICH_APR0, GICH_APR1, GICH_APR2, GICH_APR3).

Unimplemented registers are RAZ/WI.

**Attributes**

GICH_APR<n> is a 32-bit register.

**Field descriptions**

The GICH_APR<n> bit assignments are:

<table>
<thead>
<tr>
<th>P&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no interrupt active at the priority corresponding to that bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>There is an interrupt active at the priority corresponding to that bit.</td>
</tr>
</tbody>
</table>

The correspondence between priorities and bits depends on the number of bits of priority that are implemented.

If 5 bits of priority are implemented (bits [7:3] of priority), then there are 32 priority groups, and the active state of these priorities are held in GICH_APR0 in the bits corresponding to Priority[7:3].

If 6 bits of priority are implemented (bits [7:2] of priority), then there are 64 priority groups, and:

- The active state of priorities 0 - 124 are held in GICH_APR0 in the bits corresponding to 0:Priority[6:2].
- The active state of priorities 128 - 252 are held in GICH_APR1 in the bits corresponding to 1:Priority[6:2].

If 7 bits of priority are implemented (bits [7:1] of priority), then there are 128 priority groups, and:

- The active state of priorities 0 - 62 are held in GICH_APR0 in the bits corresponding to 00:Priority[5:1].
- The active state of priorities 64 - 126 are held in GICH_APR1 in the bits corresponding to 01:Priority[5:1].
- The active state of priorities 128 - 190 are held in GICH_APR2 in the bits corresponding to 10:Priority[5:1].
- The active state of priorities 192 - 254 are held in GICH_APR3 in the bits corresponding to 11:Priority[5:1].
On a Warm reset, this field resets to 0.

**Accessing the GICH_APR<n>**

These registers are used only when System register access is not enabled. When System register access is enabled the following registers provide equivalent functionality:

- **In AArch64:**
  - For Group 0, **ICH_AP0R<n>_EL2**.
  - For Group 1, **ICH_AP1R<n>_EL2**.

- **In AArch32:**
  - For Group 0, **ICH_AP0R<n>**.
  - For Group 1, **ICH_AP1R<n>**.

**GICH_APR<n>** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x00F0 + (4 * n)</td>
<td>GICH_APR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICH_EISR, End Interrupt Status Register

The GICH_EISR characteristics are:

**Purpose**

Indicates which List registers have outstanding EOI maintenance interrupts.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_EISR is a 32-bit register.

**Field descriptions**

The GICH_EISR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-16</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>15-0</td>
<td>Status&lt;n&gt;, bit [n], for n = 15 to 0</td>
</tr>
</tbody>
</table>

EOI maintenance interrupt status for List register <n>:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICH_LR&lt;n&gt; does not have an EOI maintenance interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICH_LR&lt;n&gt; has an EOI maintenance interrupt that has not been handled.</td>
</tr>
</tbody>
</table>

For any GICH_LR<n> register, the corresponding status bit is set to 1 if all of the following are true:

- GICH_LR<n>.State is 0b00.
- GICH_LR<n>.HW == 0.
- GICH_LR<n>.EOI == 1.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICH_EISR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICH_EISR provides equivalent functionality.
- For AArch64 implementations, ICH_EISR_EL2 provides equivalent functionality.

Bits corresponding to unimplemented List registers are RAZ.

GICH_EISR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0020</td>
<td>GICH_EISR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
The GICH_ELRSR characteristics are:

**Purpose**

Indicates which List registers contain valid interrupts.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_ELRSR is a 32-bit register.

**Field descriptions**

The GICH_ELRSR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Status15 | Status14 | Status13 | Status12 | Status11 | Status10 | Status9 | Status8 | Status7 | Status6 | Status5 | Status4 | Status3 | Status2 | Status1 | Status0 |

**Bits [31:16]**

Reserved, RES0.

**Status<n>, bit [n], for n = 15 to 0**

Status bit for List register <n>:

<table>
<thead>
<tr>
<th>Status&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICH_LR&lt;n&gt;, if implemented, contains a valid interrupt. Using this List register can result in overwriting a valid interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICH_LR&lt;n&gt; does not contain a valid interrupt. The List register is empty and can be used without overwriting a valid interrupt or losing an EOI maintenance interrupt.</td>
</tr>
</tbody>
</table>

For any GICH_LR<n> register, the corresponding status bit is set to 1 if GICH_LR<n>.State is 0b00 and either:

- GICH_LR<n>.HW == 1.
- GICH_LR<n>.EOI == 0.

On a Warm reset, this field resets to 1.

**Accessing the GICH_ELRSR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICH_ELRSR provides equivalent functionality.
- For AArch64 implementations, ICH_ELRSR_EL2 provides equivalent functionality.

Bits corresponding to unimplemented List registers are RES0.
GICH_ELRSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0030</td>
<td>GICH_ELRSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
GICH_HCR, Hypervisor Control Register

The GICH_HCR characteristics are:

**Purpose**

Controls the virtual CPU interface.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_HCR is a 32-bit register.

**Field descriptions**

The GICH_HCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>EOICount</td>
<td>Counts the number of EOIs received that do not have a corresponding entry in the List registers. The virtual CPU interface increments this field automatically when a matching EOI is received. EOIs that do not clear a bit in GICH_APR&lt;n&gt; do not cause an increment. If an EOI occurs when the value of this field is 31, then the field wraps to 0. The maintenance interrupt is asserted whenever this field is nonzero and GICH_HCR.LRENPIE == 1. On a Warm reset, this field resets to an architecturally UNKNOWN value.</td>
</tr>
<tr>
<td>6</td>
<td>VGrp1DIE</td>
<td>VM Group 1 Disabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected virtual machine is disabled:</td>
</tr>
<tr>
<td>5</td>
<td>VGrp1EIE</td>
<td>VM Group 1 Enabled Interrupt Enable. Enables the signaling of a maintenance interrupt while signaling of Group 1 interrupts from the virtual CPU interface to the connected virtual machine is enabled:</td>
</tr>
<tr>
<td>4</td>
<td>VGrp0DIE</td>
<td>VM Group 0 Disabled Interrupt Enable.</td>
</tr>
<tr>
<td>3</td>
<td>VGrp0EIE</td>
<td>VM Group 0 Enabled Interrupt Enable.</td>
</tr>
<tr>
<td>2</td>
<td>NPIE</td>
<td>No Pass Interrupt Enable.</td>
</tr>
<tr>
<td>1</td>
<td>LRENPIE</td>
<td>Local Resources Enabled Pass Interrupt Enable.</td>
</tr>
<tr>
<td>0</td>
<td>En</td>
<td>Enable.</td>
</tr>
</tbody>
</table>

Reserved, RES0.
### VGrp1EIE, bit [0]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Maintenance interrupt signaled when GICV_CTLR.EnableGrp1 == 1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### VGrp0DIE, bit [5]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Maintenance interrupt signaled when GICV_CTLR.EnableGrp0 == 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### VGrp0EIE, bit [4]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Maintenance interrupt signaled when GICV_CTLR.EnableGrp0 == 1.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### NPIE, bit [3]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Maintenance interrupt signaled while the List registers contain no interrupts in the pending state.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### LRENPIE, bit [2]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Maintenance interrupt signaled while GICH_HCR.EOICount is not 0.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### UIE, bit [1]

**Meaning**
- **0b0**: Maintenance interrupt disabled.
- **0b1**: Underflow Interrupt Enable.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**GICH_HCR, Hypervisor Control Register**

[Page 3744]
Enables the signaling of a maintenance interrupt when the List registers are either empty or hold only one valid entry.

<table>
<thead>
<tr>
<th>UIE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Maintenance interrupt disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>A maintenance interrupt is signaled if zero or one of the List register entries are marked as a valid interrupt.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**En, bit [0]**

Enable.

Global enable bit for the virtual CPU interface.

<table>
<thead>
<tr>
<th>En</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Virtual CPU interface operation is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Virtual CPU interface operation is enabled.</td>
</tr>
</tbody>
</table>

When this field is 0:

- The virtual CPU interface does not signal any maintenance interrupts.
- The virtual CPU interface does not signal any virtual interrupts.
- A read of `GICV_IAR` or `GICV_AIAR` returns a spurious interrupt ID.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The VGrp1DIE, VGrp1EIE, VGrp0DIE, and VGrp0EIE fields permit the hypervisor to track the virtual CPU interfaces that are enabled. The hypervisor can then route interrupts that have multiple targets correctly and efficiently, without having to read the virtual CPU interface status.

See 'Maintenance interrupts' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069) and GIC_MISR for more information.

**Accessing the GICH_HCR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICH_HCR` provides equivalent functionality.
- For AArch64 implementations, `ICH_HCR_EL2` provides equivalent functionality.

GICH_HCR.En must be set to 1 for any virtual or maintenance interrupt to be asserted.

**GICH_HCR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0000</td>
<td>GICH_HCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICH_LR<n> characteristics are:

**Purpose**

These registers provide context information for the virtual CPU interface.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

A maximum of 16 List registers can be provided. GICH_VTR.ListRegs defines the number implemented. Unimplemented List registers are RAZ/WI.

**Attributes**

GICH_LR<n> is a 32-bit register.

**Field descriptions**

The GICH_LR<n> bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>HW</th>
<th>State</th>
<th>Priority</th>
<th>RES0</th>
<th>pINTID</th>
<th>vINTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>30 – 29</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>28 – 24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>23 – 16</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 – 11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10 – 0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**HW, bit [31]**

Indicates whether this virtual interrupt is a hardware interrupt, meaning that it corresponds to a physical interrupt. Deactivation of the virtual interrupt also causes the deactivation of the physical interrupt corresponding to the INTID:

<table>
<thead>
<tr>
<th>HW Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This interrupt is triggered entirely in software. No notification is sent to the Distributor when the virtual interrupt is deactivated.</td>
</tr>
<tr>
<td>0b1</td>
<td>A hardware interrupt. A deactivate interrupt request is sent to the Distributor when the virtual interrupt is deactivated, using GICH_LR&lt;n&gt;.pINTID to indicate the physical interrupt identifier. If GICV_CTLR.EOImode == 0, this request corresponds to a write to GICV_EOIR or GICV_AEOIR, otherwise it corresponds to a write to GICV_DIR.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Group, bit [30]**

Indicates whether the interrupt is Group 0 or Group 1:

<table>
<thead>
<tr>
<th>Group Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupt. GICV_CTLR.FIQEn determines whether it is signaled as a virtual IRQ or as a virtual FIQ, and GICV_CTLR.EnableGrp0 enables signaling of this interrupt to the virtual machine.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 virtual interrupt, signaled as a virtual IRQ. GICV_CTLR.EnableGrp1 enables signaling of this interrupt to the virtual machine.</td>
</tr>
</tbody>
</table>

**Note**
GICV_CTLR. CBPR controls whether GICV_BPR or GICV_ABPR determines if a pending Group 1 interrupt has sufficient priority to preempt current execution.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

State, bits [29:28]

The state of the interrupt. This field has one of the following values:

<table>
<thead>
<tr>
<th>State</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Inactive</td>
</tr>
<tr>
<td>0b01</td>
<td>Pending</td>
</tr>
<tr>
<td>0b10</td>
<td>Active</td>
</tr>
<tr>
<td>0b11</td>
<td>Active and pending</td>
</tr>
</tbody>
</table>

The GIC updates these state bits as virtual interrupts proceed through the interrupt life cycle. Entries in the inactive state are ignored, except for the purpose of generating virtual maintenance interrupts.

Note

For hardware interrupts, the active and pending state is held in the Distributor rather than the virtual CPU interface. A hypervisor must only use the active and pending state for software originated interrupts, which are typically associated with virtual devices, or for SGIs.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Priority, bits [27:23]

The priority of this interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [22:20]

Reserved, RES0.

pINTID, bits [19:10]

The function of this field depends on the value of GICH_LR<n>.HW.

When GICH_LR<n>.HW == 0:

- Bit [19] indicates whether the interrupt triggers an EOI maintenance interrupt. If this bit is 1, then when the interrupt identified by vINTID is deactivated, an EOI maintenance interrupt is asserted.
- Bits [18:13] are reserved, SBZ.
- If the vINTID field value corresponds to an SGI (that is, 0-15), bits [12:10] contain the number of the requesting PE. This appears in the corresponding field of GICV_IAR or GICV_AIAR. If the vINTID field value is not 0-15, this field must be cleared to 0.

When GICH_LR<n>.HW == 1:

- This field indicates the pINTID that the hypervisor forwards to the Distributor. This field is only required to implement enough bits to hold a valid value for the ID configuration. Any unused higher order bits are RAZ/WI.
- If the value of pINTID is 0-15 or 1020-1023, behavior is UNPREDICTABLE. If the value of pINTID is 16-31, this field applies to the PPI associated with this same PE as the virtual CPU interface requesting the deactivation.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
\textbf{vINTID, bits [9:0]}

This INTID is returned to the VM when the interrupt is acknowledged through \texttt{GICV_IAR}. Each valid interrupt stored in the List registers must have a unique vINTID for that virtual CPU interface. If the value of vINTID is 1020-1023, behavior is \texttt{UNPREDICTABLE}.

On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

\section*{Accessing the GICH\_LR<\texttt{n}>}

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, \texttt{ICH\_LR<\texttt{n}>} provides equivalent functionality.
- For AArch64 implementations, \texttt{ICH\_LR<\texttt{n>>\_EL2} provides equivalent functionality.

\texttt{GICH\_LR<\texttt{n}> can be accessed through the memory-mapped interfaces:}

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0100 + (4 * \texttt{n})</td>
<td>GICH_LR&lt;\texttt{n}&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD\_CTRL.DS == 0 accesses to this register are \texttt{RW}.
- When an access is Secure accesses to this register are \texttt{RW}.
- When an access is Non-secure accesses to this register are \texttt{RW}.
GICH_MISR, Maintenance Interrupt Status Register

The GICH_MISR characteristics are:

**Purpose**

Indicates which maintenance interrupts are asserted.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_MISR is a 32-bit register.

**Field descriptions**

The GICH_MISR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Description</th>
<th>Byte Location</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-0</td>
<td>Reserved, RES0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>VGrp1D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>VGrp1E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>VGrp0D</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>VGrp0E</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>NP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LREN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>U</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>EOI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**VGrp1D, bit [7]**

vPE Group 1 Disabled.

<table>
<thead>
<tr>
<th>VGrp1D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 1 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 1 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when GICH_HCR.VGrp1DIE == 1 and GICH_VMCR.VENG1 == 0.

On a Warm reset, this field resets to 0.

**VGrp1E, bit [6]**

vPE Group 1 Enabled.

<table>
<thead>
<tr>
<th>VGrp1E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 1 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 1 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when GICH_HCR.VGrp1EIE == 1 and GICH_VMCR.VENG1 == 1.

On a Warm reset, this field resets to 0.

**VGrp0D, bit [5]**

vPE Group 0 Disabled.
VGrp0D

<table>
<thead>
<tr>
<th>VGrp0D</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Disabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Disabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when \texttt{GICH\_HCR.VGrp0DIE} == 1 and \texttt{GICH\_VMCR.VENG0} == 0.

On a Warm reset, this field resets to 0.

**VGrp0E, bit [4]**

vPE Group 0 Enabled.

<table>
<thead>
<tr>
<th>VGrp0E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>vPE Group 0 Enabled maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>vPE Group 0 Enabled maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when \texttt{GICH\_HCR.VGrp0EIE} == 1 and \texttt{GICH\_VMCR.VENG0} == 1.

On a Warm reset, this field resets to 0.

**NP, bit [3]**

No Pending.

<table>
<thead>
<tr>
<th>NP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No Pending maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>No Pending maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when \texttt{GICH\_HCR.NPIE} == 1 and no List register is in the pending state.

On a Warm reset, this field resets to 0.

**LRENP, bit [2]**

List Register Entry Not Present.

<table>
<thead>
<tr>
<th>LRENP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>List Register Entry Not Present maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>List Register Entry Not Present maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when \texttt{GICH\_HCR.LRENPIE} == 1 and \texttt{GICH\_HCR.EOICount} is nonzero.

On a Warm reset, this field resets to 0.

**U, bit [1]**

Underflow.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Underflow maintenance interrupt not asserted.</td>
</tr>
<tr>
<td>0b1</td>
<td>Underflow maintenance interrupt asserted.</td>
</tr>
</tbody>
</table>

This maintenance interrupt is asserted when \texttt{GICH\_HCR.UIE} == 1 and zero or one of the List register entries are marked as a valid interrupt.

On a Warm reset, this field resets to 0.

**EOI, bit [0]**

End Of Interrupt.
This maintenance interrupt is asserted when at least one bit in \texttt{GICH\_EISR} == 1.

On a Warm reset, this field resets to 0.

\textbf{Note}

A List register is in the pending state only if the corresponding \texttt{GICH\_LR<n>} value is \texttt{0b01}, that is, pending. The active and pending state is not included.

**Accessing the GICH\_MISR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, \texttt{ICH\_MISR} provides equivalent functionality.
- For AArch64 implementations, \texttt{ICH\_MISR\_EL2} provides equivalent functionality.

A maintenance interrupt is asserted only if at least one bit is set to 1 in this register and if \texttt{GICH\_HCR.En} == 1.

**GICH\_MISR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual</td>
<td>0x0010</td>
<td>GICH_MISR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GICD\_CTLR.DS} == 0 accesses to this register are \texttt{RO}.
- When an access is Secure accesses to this register are \texttt{RO}.
- When an access is Non-secure accesses to this register are \texttt{RO}.
**GICH_VMCR, Virtual Machine Control Register**

The GICH_VMCR characteristics are:

**Purpose**

Enables the hypervisor to save and restore the virtual machine view of the GIC state. This register is updated when a virtual machine updates the virtual CPU interface registers.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_VMCR is a 32-bit register.

**Field descriptions**

The GICH_VMCR bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|        |
| VPMR   | VBPR0  | VBPR1  | RES0   | VEOIM  | RES0   | VCBPR  | VFIQEn | VAckCtl | VENG1  | VENG0  |        |        |        |        |        |        |        |        |        |        |        |        |        |        |

**VPMR, bits [31:24]**

Virtual priority mask. The priority mask level for the CPU interface. If the priority of an interrupt is higher than the value indicated by this field, the interface signals the interrupt to the PE.

This alias field is updated when a VM updates `GICV_PMR.Priority`.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**VBPR0, bits [23:21]**

Virtual Binary Point Register, Group 0. Defines the point at which the priority value fields split into two parts, the Group priority field and the subpriority field. The Group priority field determines Group 0 interrupt preemption, and also determines Group 1 interrupt preemption if GICH_VMCR.VCBPR == 1.

This alias field is updated when a VM updates `GICV_BPR.Binary_Point`.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**VBPR1, bits [20:18]**

Virtual Binary Point Register, Group 1. Defines the point at which the priority value fields split into two parts, the Group priority field and the subpriority field. The Group priority field determines Group 1 interrupt preemption if GICH_VMCR.VCBPR == 0.

This alias field is updated when a VM updates `GICV_ABPR.Binary_Point`.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [17:10]**

Reserved, RES0.
VEOIM, bit [9]

Virtual EOI mode. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VEOIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A write of an INTID to <code>GICV_EOIR</code> or <code>GICV_AEOIR</code> drops the priority of the interrupt with that INTID, and also deactivates that interrupt.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write of an INTID to <code>GICV_EOIR</code> or <code>GICV_AEOIR</code> only drops the priority of the interrupt with that INTID. Software must write to <code>GICV_DIR</code> to deactivate the interrupt.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR`.EOI mode.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [8:5]

Reserved, RES0.

VCBPR, bit [4]

Virtual Common Binary Point Register. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VCBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>GICV_ABPR</code> determines the preemption group for Group 1 interrupts.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>GICV_BPR</code> determines the preemption group for Group 1 interrupts.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR`.CBPR.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

VFIQEn, bit [3]

Virtual FIQ enable. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VFIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupts are presented as virtual IRQs.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 virtual interrupts are presented as virtual FIQs.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR`.FIQEn.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

VAckCtl, bit [2]

Virtual AckCtl. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VAckCtl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the highest priority pending interrupt is Group 1, a read of <code>GICV_IAR</code> or <code>GICV_HPPIR</code> returns an INTID of 1022.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the highest priority pending interrupt is Group 1, a read of <code>GICV_IAR</code> or <code>GICV_HPPIR</code> returns the INTID of the corresponding interrupt.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR`.AckCtl.

This field is supported for backwards compatibility with GICv2. Arm deprecates the use of this field.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
VENG1, bit [1]

Virtual interrupt enable, Group 1. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 1 virtual interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 1 virtual interrupts are enabled.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR.EnableGrp1`.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

VENG0, bit [0]

Virtual interrupt enable, Group 0. Possible values of this bit are:

<table>
<thead>
<tr>
<th>VENG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupts are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 virtual interrupts are enabled.</td>
</tr>
</tbody>
</table>

This alias field is updated when a VM updates `GICV_CTLR.EnableGrp0`.

On a Warm reset, this field resets to an architecturally `UNKNOWN` value.

**Note**

A List register is in the pending state only if the corresponding `GICH_LR<n>` value is `0b01`, that is, pending. The active and pending state is not included.

**Accessing the GICH_VMCR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICH_VMCR` provides equivalent functionality.
- For AArch64 implementations, `ICH_VMCR_EL2` provides equivalent functionality.

**GICH_VMCR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0008</td>
<td>GICH_VMCR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are `RW`.
- When an access is Secure accesses to this register are `RW`.
- When an access is Non-secure accesses to this register are `RW`.
GICH_VTR, Virtual Type Register

The GICH_VTR characteristics are:

**Purpose**

Indicates the number of implemented virtual priority bits and List registers.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICH_VTR is a 32-bit register.

**Field descriptions**

The GICH_VTR bit assignments are:

<table>
<thead>
<tr>
<th>PRIbits</th>
<th>PREbits</th>
<th>IDbits</th>
<th>SEIS</th>
<th>A3V</th>
<th>RES0</th>
<th>ListRegs</th>
</tr>
</thead>
</table>

**PRIbits, bits [31:29]**

The number of virtual priority bits implemented, minus one.

An implementation must implement at least 32 levels of virtual priority (5 priority bits).

**PREbits, bits [28:26]**

The number of virtual preemption bits implemented, minus one.

An implementation must implement at least 32 levels of virtual preemption priority (5 preemption bits).

The value of this field must be less than or equal to the value of GICH_VTR.PRIbits.

**IDbits, bits [25:23]**

The number of virtual interrupt identifier bits supported:

<table>
<thead>
<tr>
<th>IDbits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>16 bits.</td>
</tr>
<tr>
<td>0b001</td>
<td>24 bits.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**SEIS, bit [22]**

SEI support. Indicates whether the virtual CPU interface supports generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic does not support generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports generation of SEIs.</td>
</tr>
</tbody>
</table>
A3V, bit [21]

Affinity 3 valid. Possible values are:

<table>
<thead>
<tr>
<th>A3V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual CPU interface logic only supports zero values of the Aff3 field in ICC_SGI0R_EL1, ICC_SGI1R_EL1, and ICC_ASGI1R_EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual CPU interface logic supports nonzero values of the Aff3 field in ICC_SGI0R_EL1, ICC_SGI1R_EL1, and ICC_ASGI1R_EL1.</td>
</tr>
</tbody>
</table>

Bits [20:5]

Reserved, RES0.

ListRegs, bits [4:0]

The number of implemented List registers, minus one.

Accessing the GICH_VTR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICH_VTR provides equivalent functionality.
- For AArch64 implementations, ICH_VTR_EL2 provides equivalent functionality.

GICH_VTR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual interface control</td>
<td>0x0004</td>
<td>GICH_VTR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
**GICR_CLRLPIR, Clear LPI Pending Register**

The GICR_CLRLPIR characteristics are:

**Purpose**

Clears the pending state of the specified LPI.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICR_CLRLPIR are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_CLRLPIR is a 64-bit register.

**Field descriptions**

The GICR_CLRLPIR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | RES0 | RES0 | RES0 |

**Bits [63:32]**

Reserved, RES0.

**pINTID, bits [31:0]**

The INTID of the physical LPI.

---

**Note**

The size of this field is IMPLEMENTATION DEFINED, and is specified by the GICD_TYPER.IDbits field. Unimplemented bits are RES0.

---

**Accessing the GICR_CLRLPIR**

When written with a 32-bit write the data is zero-extended to 64 bits.

This register is mandatory in an implementation that supports LPIs and does not include an ITS. The functionality of this register is IMPLEMENTATION DEFINED in an implementation that does include an ITS.

Writes to this register have no effect if any of the following apply:

- **GICR_CTLR.EnableLPIs == 0.**
- The pINTID value specifies an unimplemented LPI.
- The pINTID value specifies an LPI that is not pending.
GICR_CLRLPIR, Clear LPI Pending Register

**GICR_CLRLPIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0048</td>
<td>GICR_CLRLPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
The GICR_CTLR characteristics are:

**Purpose**

Controls the operation of a Redistributor, and enables the signaling of LPIs by the Redistributor to the connected PE.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_CTLR is a 32-bit register.

**Field descriptions**

The GICR_CTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31 30 29 28 27</td>
<td>UWP RES0 DPG1S DPG1NS DPG0</td>
</tr>
<tr>
<td>26 25 24 23 22</td>
<td>RES0</td>
</tr>
<tr>
<td>21 20 19 18 17</td>
<td></td>
</tr>
<tr>
<td>16 15 14 13 12</td>
<td></td>
</tr>
<tr>
<td>11 10 9 8 7 6 5</td>
<td></td>
</tr>
<tr>
<td>4 3 2 1 0</td>
<td>RWP RCE EnableLPIs</td>
</tr>
</tbody>
</table>

**UWP, bit [31]**

Upstream Write Pending. Read-only. Indicates whether all upstream writes have been communicated to the Distributor:

<table>
<thead>
<tr>
<th>UWP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The effects of all upstream writes have been communicated to the Distributor, including any Generate SGI packets. For more information, see ‘Generate SGI (ICC)’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).</td>
</tr>
<tr>
<td>0b1</td>
<td>Not all the effects of upstream writes, including any Generate SGI packets, have been communicated to the Distributor. For more information, see 'Generate SGI (ICC)' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).</td>
</tr>
</tbody>
</table>

**Bits [30:27]**

Reserved, RES0.

**DPG1S, bit [26]**

Disable Processor selection for Group 1 Secure interrupts. When GICR_TYPER.DPGS == 1:

<table>
<thead>
<tr>
<th>DPG1S</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A Group 1 Secure SPI configured to use the 1 of N distribution model can select this PE, if the PE is not asleep and if Secure Group 1 interrupts are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Group 1 Secure SPI configured to use the 1 of N distribution model cannot select this PE.</td>
</tr>
</tbody>
</table>

When GICR_TYPER.DPGS == 0 this bit is RAZ/WI.
When `GICD_CTLR.DS==1`, this field is RAZ/WI. In GIC implementations that support two Security states, this field is only accessible by Secure accesses, and is RAZ/WI to Non-secure accesses.

It is IMPLEMENTATION DEFINED whether these bits affect the selection of PEs for interrupts using the 1 of N distribution model when `GICD_CTLR.ARE_S==0`.

On a Warm reset, this field resets to 0.

**DPG1NS, bit [25]**

Disable Processor selection for Group 1 Non-secure interrupts. When `GICR_TYPER.DPGS == 1`:

<table>
<thead>
<tr>
<th>DPG1NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A Group 1 Non-secure SPI configured to use the 1 of N distribution model can select this PE, if the PE is not asleep and if Non-secure Group 1 interrupts are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Group 1 Non-secure SPI configured to use the 1 of N distribution model cannot select this PE.</td>
</tr>
</tbody>
</table>

When `GICR_TYPER.DPGS == 0` this bit is RAZ/WI.

It is IMPLEMENTATION DEFINED whether these bits affect the selection of PEs for interrupts using the 1 of N distribution model when `GICD_CTLR.ARE_NS==0`.

On a Warm reset, this field resets to 0.

**DPG0, bit [24]**

Disable Processor selection for Group 0 interrupts. When `GICR_TYPER.DPGS == 1`:

<table>
<thead>
<tr>
<th>DPG0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>A Group 0 SPI configured to use the 1 of N distribution model can select this PE, if the PE is not asleep and if Group 0 interrupts are enabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>A Group 0 SPI configured to use the 1 of N distribution model cannot select this PE.</td>
</tr>
</tbody>
</table>

When `GICR_TYPER.DPGS == 0` this bit is RAZ/WI.

When `GICD_CTLR.DS == 1`, this field is always accessible. In GIC implementations that support two Security states, this field is RAZ/WI to Non-secure accesses.

It is IMPLEMENTATION DEFINED whether these bits affect the selection of PEs for interrupts using the 1 of N distribution model when `GICD_CTLR.ARE_S == 0`.

On a Warm reset, this field resets to 0.

**Bits [23:4]**

Reserved, RES0.

**RWP, bit [3]**

Register Write Pending. This bit indicates whether a register write for the current Security state is in progress or not.
Meaning

0b0  The effect of all previous writes to the following registers are visible to all agents in the system:
• GICR_ICENABLER0
• GICR_CTLR DPG1S
• GICR_CTLR DPG1NS
• GICR_CTLR DPG0
• GICR_CTLR, which clears EnableLPIs from 1 to 0.
• In FEAT_GICv4p1, GICR_VPROPBASER, which clears Valid from 1 to 0.

0b1  The effect of all previous writes to the following registers are not guaranteed by the architecture to be visible to all agents in the system while the changes are still being propagated:
• GICR_ICENABLER0
• GICR_CTLR DPG1S
• GICR_CTLR DPG1NS
• GICR_CTLR DPG0
• GICR_CTLR, which clears EnableLPIs from 1 to 0.
• In FEAT_GICv4p1, GICR_VPROPBASER, which clears Valid from 1 to 0.

IR, bit [2]

LPI invalidate registers supported.

This bit is read-only.

Meaning

IR  Meaning

0b0  This bit does not indicate whether the GICR_INVLPIR, GICR_INVALLR and GICR_SYNCR are implemented or not.

0b1  GICR_INVLPIR, GICR_INVALLR and GICR_SYNCR are implemented.

If GICR_TYPER.DirectLPI is 1 or GICR_TYPER.RVPEI is 1, GICR_INVLPIR, GICR_INVALLR, and GICR_SYNCR are always implemented.

Arm recommends that implementations report GICR_CTLR.IR as 1 in these cases.

CES, bit [1]

Clear Enable Supported.

This bit is read-only.

Meaning

CES  Meaning

0b0  The IRI does not indicate whether GICR_CTLR.EnableLPIs is RES1 once set.

0b1  GICR_CTLR.EnableLPIs is not RES1 once set.

Implementing GICR_CTLR.EnableLPIs as programmable and not reporting GICR_CTLR.CES == 1 is deprecated.

Implementing GICR_CTLR.EnableLPIs as RES1 once set is deprecated.

When GICR_CTLR.CES == 0, software cannot assume that GICR_CTLR.EnableLPIs is programmable without observing the bit being cleared.

EnableLPIs, bit [0]

In implementations where affinity routing is enabled for the Security state:

Meaning

EnableLPIs  Meaning

0b0  LPI support is disabled. Any doorbell interrupt generated as a result of a write to a virtual LPI register must be discarded, and any ITS translation requests or commands involving LPIs in this Redistributor are ignored.

0b1  LPI support is enabled.
Note

If $\text{GICR}_\text{TYPER}.\text{PLPIS} == 0$, this field is RES0. If $\text{GICD}_\text{CTLR}.\text{ARE}_\text{NS}$ is written from 1 to 0 when this bit is 1, behavior is an IMPLEMENTATION DEFINED choice between clearing $\text{GICR}_\text{CTLR}.\text{EnableLPIs}$ to 0 or maintaining its current value.

When affinity routing is not enabled for the Non-secure state, this bit is RES0.

When written from 0 to 1, the Redistributor loads the LPI Pending table from memory to check for any pending interrupts.

After it has been written to 1, it is IMPLEMENTATION DEFINED whether the bit becomes RES1 or can be cleared by to 0.

Where the bit remains programmable:

- Software must observe $\text{GICR}_\text{CTLR}.\text{RWP} == 0$ after clearing $\text{GICR}_\text{CTLR}.\text{EnableLPIs}$ from 1 to 0 before writing $\text{GICR}_\text{PENDBASER}$ or $\text{GICR}_\text{PROPBASER}$, otherwise behavior is UNPREDICTABLE.
- Software must observe $\text{GICR}_\text{CTLR}.\text{RWP} == 0$ after clearing $\text{GICR}_\text{CTLR}.\text{EnableLPIs}$ from 1 to 0 before setting $\text{GICR}_\text{CTLR}.\text{EnableLPIs}$ to 1, otherwise behavior is UNPREDICTABLE.

Note

If one or more ITS is implemented, Arm strongly recommends that all LPIs are mapped to another Redistributor before $\text{GICR}_\text{CTLR}.\text{EnableLPIs}$ is cleared to 0.

On a Warm reset, this field resets to 0.

The participation of a PE in the 1 of N distribution model for a given interrupt group is governed by the concatenation of $\text{GICR}_\text{WAKER}_\text{ProcessorSleep}$, the appropriate $\text{GICR}_\text{CTLR}.\text{DPG} \{1, 0\}$ bit, and the PE interrupt group enable. The behavior options are:

<table>
<thead>
<tr>
<th>$\text{PS}$</th>
<th>$\text{DPG} {1S, 1NS, 0}$</th>
<th>Enable</th>
<th>PE Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>0b0</td>
<td>The PE cannot be selected.</td>
</tr>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>0b1</td>
<td>The PE can be selected.</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>*</td>
<td>The PE cannot be selected.</td>
</tr>
<tr>
<td>0b1</td>
<td>*</td>
<td>*</td>
<td>The PE cannot be selected when $\text{GICD}<em>\text{CTLR}.\text{E1NWF} == 0$. When $\text{GICD}</em>\text{CTLR}.\text{E1NWF} == 1$, the mechanism by which PEs are selected is IMPLEMENTATION DEFINED.</td>
</tr>
</tbody>
</table>

If an SPI using the 1 of N distribution model has been forwarded to the PE, and a write to $\text{GICR}_\text{CTLR}$ occurs that changes the DPG bit for the interrupt group of the SPI, the IRI must attempt to select a different target PE for the SPI. This might have no effect on the forwarded SPI if it has already been activated.

### Accessing the GICR_CTLR

$\text{GICR}_\text{CTLR}$ can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>RD_base</td>
<td>0x0000</td>
<td>GICR_CTLR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When $\text{GICD}_\text{CTLR}.\text{DS} == 0$ accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICR_ICACTIVER0, Interrupt Clear-Active Register 0

The GICR_ICACTIVER0 characteristics are:

**Purpose**

Deactivates the corresponding SGI or PPI. These registers are used when saving and restoring GIC state.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICACTIVER0 is a 32-bit register.

**Field descriptions**

The GICR_ICACTIVER0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Clear_active_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Clear_active_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Clear_active_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Clear_active_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Clear_active_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Clear_active_bit26</td>
</tr>
<tr>
<td>25</td>
<td>Clear_active_bit25</td>
</tr>
<tr>
<td>24</td>
<td>Clear_active_bit24</td>
</tr>
<tr>
<td>23</td>
<td>Clear_active_bit23</td>
</tr>
<tr>
<td>22</td>
<td>Clear_active_bit22</td>
</tr>
<tr>
<td>21</td>
<td>Clear_active_bit21</td>
</tr>
<tr>
<td>20</td>
<td>Clear_active_bit20</td>
</tr>
<tr>
<td>19</td>
<td>Clear_active_bit19</td>
</tr>
<tr>
<td>18</td>
<td>Clear_active_bit18</td>
</tr>
<tr>
<td>17</td>
<td>Clear_active_bit17</td>
</tr>
<tr>
<td>16</td>
<td>Clear_active_bit16</td>
</tr>
<tr>
<td>15</td>
<td>Clear_active_bit15</td>
</tr>
<tr>
<td>14</td>
<td>Clear_active_bit14</td>
</tr>
<tr>
<td>13</td>
<td>Clear_active_bit13</td>
</tr>
<tr>
<td>12</td>
<td>Clear_active_bit12</td>
</tr>
<tr>
<td>11</td>
<td>Clear_active_bit11</td>
</tr>
<tr>
<td>10</td>
<td>Clear_active_bit10</td>
</tr>
<tr>
<td>9</td>
<td>Clear_active_bit9</td>
</tr>
<tr>
<td>8</td>
<td>Clear_active_bit8</td>
</tr>
<tr>
<td>7</td>
<td>Clear_active_bit7</td>
</tr>
<tr>
<td>6</td>
<td>Clear_active_bit6</td>
</tr>
<tr>
<td>5</td>
<td>Clear_active_bit5</td>
</tr>
<tr>
<td>4</td>
<td>Clear_active_bit4</td>
</tr>
<tr>
<td>3</td>
<td>Clear_active_bit3</td>
</tr>
<tr>
<td>2</td>
<td>Clear_active_bit2</td>
</tr>
<tr>
<td>1</td>
<td>Clear_active_bit1</td>
</tr>
<tr>
<td>0</td>
<td>Clear_active_bit0</td>
</tr>
</tbody>
</table>

Clear_active_bit<x>, bit [x], for x = 31 to 0

Removes the active state from interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or is active and pending. If written, deactivates the corresponding interrupt, if the interrupt is active. If the interrupt is already deactivated, the write has no effect.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

**Accessing the GICR_ICACTIVER0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICACTIVER0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ICACTIVER<n>, with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ICACTIVER<n>.

When GICD_CTLR.DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.

**GICR_ICACTIVER0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x8380</td>
<td>GICR_ICACTIVER0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_ICACTIVER<n>E characteristics are:

**Purpose**

Removes the active state from the corresponding PPI.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ICACTIVER<n>E are `RES0`.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICACTIVER<n>E is a 32-bit register.

**Field descriptions**

The GICR_ICACTIVER<n>E bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Clear_active_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Clear_active_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Clear_active_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Clear_active_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Clear_active_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Clear_active_bit26</td>
</tr>
<tr>
<td>25</td>
<td>Clear_active_bit25</td>
</tr>
<tr>
<td>24</td>
<td>Clear_active_bit24</td>
</tr>
<tr>
<td>23</td>
<td>Clear_active_bit23</td>
</tr>
<tr>
<td>22</td>
<td>Clear_active_bit22</td>
</tr>
<tr>
<td>21</td>
<td>Clear_active_bit21</td>
</tr>
<tr>
<td>20</td>
<td>Clear_active_bit20</td>
</tr>
<tr>
<td>19</td>
<td>Clear_active_bit19</td>
</tr>
<tr>
<td>18</td>
<td>Clear_active_bit18</td>
</tr>
<tr>
<td>17</td>
<td>Clear_active_bit17</td>
</tr>
<tr>
<td>16</td>
<td>Clear_active_bit16</td>
</tr>
<tr>
<td>15</td>
<td>Clear_active_bit15</td>
</tr>
<tr>
<td>14</td>
<td>Clear_active_bit14</td>
</tr>
<tr>
<td>13</td>
<td>Clear_active_bit13</td>
</tr>
<tr>
<td>12</td>
<td>Clear_active_bit12</td>
</tr>
<tr>
<td>11</td>
<td>Clear_active_bit11</td>
</tr>
<tr>
<td>10</td>
<td>Clear_active_bit10</td>
</tr>
<tr>
<td>9</td>
<td>Clear_active_bit9</td>
</tr>
<tr>
<td>8</td>
<td>Clear_active_bit8</td>
</tr>
<tr>
<td>7</td>
<td>Clear_active_bit7</td>
</tr>
<tr>
<td>6</td>
<td>Clear_active_bit6</td>
</tr>
<tr>
<td>5</td>
<td>Clear_active_bit5</td>
</tr>
<tr>
<td>4</td>
<td>Clear_active_bit4</td>
</tr>
<tr>
<td>3</td>
<td>Clear_active_bit3</td>
</tr>
<tr>
<td>2</td>
<td>Clear_active_bit2</td>
</tr>
<tr>
<td>1</td>
<td>Clear_active_bit1</td>
</tr>
<tr>
<td>0</td>
<td>Clear_active_bit0</td>
</tr>
</tbody>
</table>

For the extended PPIs, removes the active state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
</table>
| 0b0                 | If read, indicates that the corresponding interrupt is not active, and is not active and pending.
|                     | If written, has no effect. |
| 0b1                 | If read, indicates that the corresponding interrupt is active, or is active and pending.
|                     | If written, deactivates the corresponding interrupt, if the interrupt is active. If the interrupt is already deactivated, the write has no effect. |

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ICACTIVER<n>E number, n, is given by n = (m-1024) DIV 32.
- The offset of the required GICR_ICACTIVER<n>E is \((0x200 + (4*n))\).
- The bit number of the required group modifier bit in this register is \((m-1024) \text{ MOD } 32\).

**Accessing the GICR_ICACTIVER<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICACTIVER<n>E, the corresponding bit is `RES0`.

When `GICD_CTRLR.DS==0`, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.
Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR\_ICACTIVER\(<n>E\)** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0380 + (4 * n)</td>
<td>GICR_ICACTIVER(&lt;n&gt;E)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD\_CTRL\_DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_ICENABLER0, Interrupt Clear-Enable Register 0

The GICR_ICENABLER0 characteristics are:

**Purpose**

Disables forwarding of the corresponding SGI or PPI to the CPU interfaces.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICENABLER0 is a 32-bit register.

**Field descriptions**

The GICR_ICENABLER0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, disables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the GICR_ICENABLER0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICENABLER0, the corresponding bit is RAZ/WI and equivalent functionality is provided by **GICD_ICENABLER<n>** with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by **GICD_ICENABLER<n>**.

When **GICD_CTLR.DS == 0**, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.

**GICR_ICENABLER0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>SGI_base</td>
<td>0x0180</td>
<td>GICR_ICENABLER0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR_DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_ICENABLER\(n\)E characteristics are:

**Purpose**

Disables forwarding of the corresponding PPI to the CPU interfaces.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ICENABLER\(n\)E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICENABLER\(n\)E is a 32-bit register.

**Field descriptions**

The GICR_ICENABLER\(n\)E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
</table>

**Clear_enable_bit\(x\), bit \(x\), for \(x = 31\) to \(0\)**

For the extended PPI range, controls the forwarding of interrupt number \(x\) to the CPU interface. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_enable_bit(x)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled.</td>
</tr>
<tr>
<td></td>
<td>If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled.</td>
</tr>
<tr>
<td></td>
<td>If written, disables forwarding of the corresponding interrupt.</td>
</tr>
<tr>
<td></td>
<td>After a write of 1 to this bit, a subsequent read of this bit returns 0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID \(m\), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ICENABLER\(n\)E number, \(n\), is given by \(n = (m-1024) \div 32\).
- The offset of the required GICR_ICENABLER\(n\)E is \((0\times180 + (4 \times n))\).
- The bit number of the required group modifier bit in this register is \((m-1024) \mod 32\).

**Accessing the GICR_ICENABLER\(n\)E**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICENABLER\(n\)E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.
Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_ICENABLER\(<n>E \text{ can be accessed through the memory-mapped interfaces:}**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0180 + (4 * n)</td>
<td>GICR_ICENABLER(&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_ICFGR0 characteristics are:

**Purpose**

Determines whether the corresponding SGI is edge-triggered or level-sensitive.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICFGR0 is a 32-bit register.

**Field descriptions**

The GICR_ICFGR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Int_config15</td>
</tr>
<tr>
<td>30</td>
<td>Int_config14</td>
</tr>
<tr>
<td>29</td>
<td>Int_config13</td>
</tr>
<tr>
<td>28</td>
<td>Int_config12</td>
</tr>
<tr>
<td>27</td>
<td>Int_config11</td>
</tr>
<tr>
<td>26</td>
<td>Int_config10</td>
</tr>
<tr>
<td>25</td>
<td>Int_config9</td>
</tr>
<tr>
<td>24</td>
<td>Int_config8</td>
</tr>
<tr>
<td>23</td>
<td>Int_config7</td>
</tr>
<tr>
<td>22</td>
<td>Int_config6</td>
</tr>
<tr>
<td>21</td>
<td>Int_config5</td>
</tr>
<tr>
<td>20</td>
<td>Int_config4</td>
</tr>
<tr>
<td>19</td>
<td>Int_config3</td>
</tr>
<tr>
<td>18</td>
<td>Int_config2</td>
</tr>
<tr>
<td>17</td>
<td>Int_config1</td>
</tr>
<tr>
<td>16</td>
<td>Int_config0</td>
</tr>
</tbody>
</table>

Int_config<x>, bits [2x+1:2x], for x = 15 to 0

Indicates whether the interrupt with ID 16n + x is level-sensitive or edge-triggered.

Int_config[0] (bit [2x]) is RES0.

Possible values of Int_config[1] (bit [2x+1]) are:

<table>
<thead>
<tr>
<th>Int_config&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Corresponding interrupt is level-sensitive.</td>
</tr>
<tr>
<td>0b01</td>
<td>Corresponding interrupt is edge-triggered.</td>
</tr>
</tbody>
</table>

For SGIs, Int_config[1] is RAO/WI.

A read of this bit always returns the correct value to indicate the interrupt triggering method.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICR_ICFGR0**

This register is used when affinity routing is enabled.

When affinity routing is disabled for the Security state of an interrupt, the field for that interrupt is RES0 and an implementation is permitted to make the field RAZ/WI in this case. Equivalent functionality is provided by GICD_ICFGR<n> with n=0.

When GICD_CTLR.DS==0, a register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.

GICR_ICFGR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>SGI_base</td>
<td>0x0C00</td>
<td>GICR_ICFGR0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICR_ICFGR1,Interrupt Configuration Register 1

The GICR_ICFGR1 characteristics are:

**Purpose**
Determined whether the corresponding PPI is edge-triggered or level-sensitive.

**Configuration**

A copy of this register is provided for each Redistributor.

For each supported PPI, it is IMPLEMENTATION DEFINED whether software can program the corresponding Int_config field.

Changing Int_config when the interrupt is individually enabled is UNPREDICTABLE.

Changing the interrupt configuration between level-sensitive and edge-triggered (in either direction) at a time when there is a pending interrupt will leave the interrupt in an UNKNOWN pending state.

**Attributes**

GICR_ICFGR1 is a 32-bit register.

**Field descriptions**

The GICR_ICFGR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>Int_config15</td>
</tr>
<tr>
<td>29</td>
<td>Int_config14</td>
</tr>
<tr>
<td>28</td>
<td>Int_config13</td>
</tr>
<tr>
<td>27</td>
<td>Int_config12</td>
</tr>
<tr>
<td>26</td>
<td>Int_config11</td>
</tr>
<tr>
<td>25</td>
<td>Int_config10</td>
</tr>
<tr>
<td>24</td>
<td>Int_config9</td>
</tr>
<tr>
<td>23</td>
<td>Int_config8</td>
</tr>
<tr>
<td>22</td>
<td>Int_config7</td>
</tr>
<tr>
<td>21</td>
<td>Int_config6</td>
</tr>
<tr>
<td>20</td>
<td>Int_config5</td>
</tr>
<tr>
<td>19</td>
<td>Int_config4</td>
</tr>
<tr>
<td>18</td>
<td>Int_config3</td>
</tr>
<tr>
<td>17</td>
<td>Int_config2</td>
</tr>
<tr>
<td>16</td>
<td>Int_config1</td>
</tr>
<tr>
<td>15</td>
<td>Int_config0</td>
</tr>
</tbody>
</table>

Int_config<x>, bits [2x+1:2x], for x = 15 to 0
Indicates whether the interrupt with ID 16n + x is level-sensitive or edge-triggered.

Int_config[0] (bit [2x]) is RES0.

Possible values of Int_config[1] (bit [2x+1]) are:

<table>
<thead>
<tr>
<th>Int_config&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Corresponding interrupt is level-sensitive.</td>
</tr>
<tr>
<td>0b01</td>
<td>Corresponding interrupt is edge-triggered.</td>
</tr>
</tbody>
</table>

A read of this bit always returns the correct value to indicate the interrupt triggering method.

For PPIs, Int_config[1] is programmable unless the implementation supports two Security states and the bit corresponds to a Group 0 or Secure Group 1 interrupt, in which case the bit is RAZ/WI to Non-secure accesses.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICR_ICFGR1**

This register is used when affinity routing is enabled.

When affinity routing is disabled for the Security state of an interrupt, the field for that interrupt is RES0 and an implementation is permitted to make the field RAZ/WI in this case. Equivalent functionality is provided by GICD_ICFGR<n> with n=1.
GICR_ICFGR1 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0C04</td>
<td>GICR_ICFGR1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_ICFGR<n>E, Interrupt configuration registers, n = 2 - 5

The GICR_ICFGR<n>E characteristics are:

**Purpose**

Determines whether the corresponding PPI in the extended PPI range is edge-triggered or level-sensitive.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ICFGR<n>E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICFGR<n>E is a 32-bit register.

**Field descriptions**

The GICR_ICFGR<n>E bit assignments are:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
</tr>
</thead>
<tbody>
<tr>
<td>Int_config31</td>
<td>Int_config30</td>
<td>Int_config29</td>
<td>Int_config28</td>
<td>Int_config27</td>
<td>Int_config26</td>
<td>Int_config25</td>
<td>Int_config24</td>
<td>Int_config23</td>
</tr>
</tbody>
</table>
```

**Int_config<x>, bit [x], for x = 31 to 0**

Indicates whether the interrupt with ID 16n + x is level-sensitive or edge-triggered.

Int_config[0] (bit [2x]) is RES0.

Possible values of Int_config[1] (bit [2x+1]) are:

<table>
<thead>
<tr>
<th>Int_config&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The corresponding interrupt is level-sensitive.</td>
</tr>
<tr>
<td>0b1</td>
<td>The corresponding interrupt is edge-triggered.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For each supported extended PPI, it is IMPLEMENTATION DEFINED whether software can program the corresponding Int_config field.

**Accessing the GICR_ICFGR<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICFGR<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, a register bit that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_ICFGR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

---
<table>
<thead>
<tr>
<th>GIC Redistributor</th>
<th>SGI_base</th>
<th>$0x0C00 + (4 * n)$</th>
<th>GICR_ICFGR&lt;n&gt;E</th>
</tr>
</thead>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_ICPENDR0, Interrupt Clear-Pending Register 0

The GICR_ICPENDR0 characteristics are:

**Purpose**

Removes the pending state from the corresponding SGI or PPI.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICPENDR0 is a 32-bit register.

**Field descriptions**

The GICR_ICPENDR0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
</table>

**Clear_pending_bit<x>, bit [x], for x = 31 to 0**

Removes the pending state from interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is pending, or active and pending. If written, changes the state of the corresponding interrupt from pending to inactive, or from active and pending to active. This has no effect in the following cases:</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is not pending and is not active and pending.</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is a level-sensitive interrupt that is pending or active and pending for a reason other than a write to GICD_ISPENDR&lt;n&gt;. In this case, if the interrupt signal continues to be asserted, the interrupt remains pending or active and pending.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally unknown value.

**Accessing the GICR_ICPENDR0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICPENDR0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ICPENDR<n> with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ICENABLER<n>.

When GICD_CTLR_DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.
GICR_ICPENDR0 can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0280</td>
<td>GICR_ICPENDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_ICPENDR<n>E characteristics are:

**Purpose**

Removes the pending state from the corresponding PPI.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ICPENDR<n>E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ICPENDR<n>E is a 32-bit register.

**Field descriptions**

The GICR_ICPENDR<n>E bit assignments are:

|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|---------------------|

For the extended PPIs, removes the pending state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Clear_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending on this PE. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is pending, or active and pending on this PE. If written, changes the state of the corresponding interrupt from pending to inactive, or from active and pending to active. This has no effect in the following cases:</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is not pending and is not active and pending.</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is a level-sensitive interrupt that is pending or active and pending for a reason other than a write to GICR_ISPENDR&lt;n&gt;E. In this case, if the interrupt signal continues to be asserted, the interrupt remains pending or active and pending.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ICPENDR<n>E number, n, is given by \( n = (m-1024) \div 32 \).
- The offset of the required GICR_ICPENDR<n>E is \((0x200 + (4*n))\).
The bit number of the required group modifier bit in this register is \((m-1024) \mod 32\).

**Accessing the GICR_ICPENDR\(n\)E**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ICPENDR\(n\)E, the corresponding bit is RES0.

When \texttt{GICD_CTLR.DS==0}, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_ICPENDR\(n\)E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0280 + (4 * (n))</td>
<td>GICR_ICPENDR(n)E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_IGROUPR0 characteristics are:

**Purpose**

Controls whether the corresponding SGI or PPI is in Group 0 or Group 1.

**Configuration**

This register is available in all GIC configurations. If the GIC implementation supports two Security states, this register is Secure.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_IGROUPR0 is a 32-bit register.

**Field descriptions**

The GICR_IGROUPR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Index</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Redistributor_group_status_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Redistributor_group_status_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Redistributor_group_status_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Redistributor_group_status_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Redistributor_group_status_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Redistributor_group_status_bit26</td>
</tr>
<tr>
<td>25</td>
<td>Redistributor_group_status_bit25</td>
</tr>
<tr>
<td>24</td>
<td>Redistributor_group_status_bit24</td>
</tr>
<tr>
<td>23</td>
<td>Redistributor_group_status_bit23</td>
</tr>
<tr>
<td>22</td>
<td>Redistributor_group_status_bit22</td>
</tr>
<tr>
<td>21</td>
<td>Redistributor_group_status_bit21</td>
</tr>
<tr>
<td>20</td>
<td>Redistributor_group_status_bit20</td>
</tr>
<tr>
<td>19</td>
<td>Redistributor_group_status_bit19</td>
</tr>
<tr>
<td>18</td>
<td>Redistributor_group_status_bit18</td>
</tr>
<tr>
<td>17</td>
<td>Redistributor_group_status_bit17</td>
</tr>
<tr>
<td>16</td>
<td>Redistributor_group_status_bit16</td>
</tr>
<tr>
<td>15</td>
<td>Redistributor_group_status_bit15</td>
</tr>
<tr>
<td>14</td>
<td>Redistributor_group_status_bit14</td>
</tr>
<tr>
<td>13</td>
<td>Redistributor_group_status_bit13</td>
</tr>
<tr>
<td>12</td>
<td>Redistributor_group_status_bit12</td>
</tr>
<tr>
<td>11</td>
<td>Redistributor_group_status_bit11</td>
</tr>
<tr>
<td>10</td>
<td>Redistributor_group_status_bit10</td>
</tr>
<tr>
<td>9</td>
<td>Redistributor_group_status_bit9</td>
</tr>
<tr>
<td>8</td>
<td>Redistributor_group_status_bit8</td>
</tr>
<tr>
<td>7</td>
<td>Redistributor_group_status_bit7</td>
</tr>
<tr>
<td>6</td>
<td>Redistributor_group_status_bit6</td>
</tr>
<tr>
<td>5</td>
<td>Redistributor_group_status_bit5</td>
</tr>
<tr>
<td>4</td>
<td>Redistributor_group_status_bit4</td>
</tr>
<tr>
<td>3</td>
<td>Redistributor_group_status_bit3</td>
</tr>
<tr>
<td>2</td>
<td>Redistributor_group_status_bit2</td>
</tr>
<tr>
<td>1</td>
<td>Redistributor_group_status_bit1</td>
</tr>
<tr>
<td>0</td>
<td>Redistributor_group_status_bit0</td>
</tr>
</tbody>
</table>

**Redistributor_group_status_bit<x>, bit [x], for x = 31 to 0**

Group status bit. In this register:

- Bits [31:16] are group status bits for PPIs.
- Bits [15:0] are group status bits for SGIs.

<table>
<thead>
<tr>
<th>Redistributor_group_status_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 0. When GICD_CTLR.DS==0, the corresponding interrupt is Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 1. When GICD_CTLR.DS==0, the corresponding interrupt is Non-secure Group 1.</td>
</tr>
</tbody>
</table>

When GICD_CTLR.DS == 0, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICR_IGRPMODR0 to form a 2-bit field that defines an interrupt group. The encoding of this field is at GICR_IGRPMODR0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The considerations for the reset value of this register are the same as those for GICD_IGROUPR<n> with n=0.

**Accessing the GICR_IGROUPR0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_IGROUPR0, the corresponding bit is RES0 and equivalent functionality is provided by GICD_IGROUPR<n> with n=0.
When `GICD_CTLR.DS == 0`, the register is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

### Note
Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

**GICR_IGROUPR0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0080</td>
<td>GICR_IGROUPR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `GICD_CTLR.DS == 0` accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_IGROUPR<n>E characteristics are:

**Purpose**

Controls whether the corresponding PPI is in Group 0 or Group 1.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_IGROUPR<n>E are RES0.

When GICD_CTLR.DS==0, this register is Secure.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_IGROUPR<n>E is a 32-bit register.

**Field descriptions**

The GICR_IGROUPR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Group_status_bit31</td>
<td>Group_status_bit30</td>
<td>Group_status_bit29</td>
<td>Group_status_bit28</td>
<td>Group_status_bit27</td>
<td>Group_status_bit26</td>
</tr>
</tbody>
</table>

**Group_status_bit<x>, bit [x], for x = 31 to 0**

Group status bit.

<table>
<thead>
<tr>
<th>Group_status_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 0. When GICD_CTLR.DS==0, the corresponding interrupt is Secure.</td>
</tr>
<tr>
<td>0b1</td>
<td>When GICD_CTLR.DS==1, the corresponding interrupt is Group 1. When GICD_CTLR.DS==0, the corresponding interrupt is Non-secure Group 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

If affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICR_IGRMODR<n>E to form a 2-bit field that defines an interrupt group. The encoding of this field is described in GICR_IGRMODR<n>E.

If affinity routing is disabled for the Security state of an interrupt, the bit is RES0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_IGROUPR<n>E number, n, is given by n = (m-1024) DIV 32.
- The offset of the required GICR_IGROUPR<n>E is (0x80 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-1024) MOD 32.
Accessing the GICR_IGROUPR\(n\)E

When affinity routing is not enabled for the Security state of an interrupt in GICR_IGROUPR\(n\)E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, the register is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

GICR_IGROUPR\(n\)E can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0080 + (4 * (n))</td>
<td>GICR_IGROUPR(n)E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GICR_IGRPMODR0, Interrupt Group Modifier Register 0

The GICR_IGRPMODR0 characteristics are:

**Purpose**

When `GICD_CTLR.DS==0`, this register together with the `GICR_IGROUPR0` register, controls whether the corresponding interrupt is in:

- Secure Group 0.
- Non-secure Group 1.
- When System register access is enabled, Secure Group 1.

**Configuration**

When `GICD_CTLR.DS==0`, this register is Secure.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_IGRPMODR0 is a 32-bit register.

**Field descriptions**

The GICR_IGRPMODR0 bit assignments are:

<table>
<thead>
<tr>
<th>Group modifier bit&lt;31&gt;, bit [x], for x = 31 to 0</th>
</tr>
</thead>
</table>

**Group modifier_bit<x>, bit [x], for x = 31 to 0**

Group modifier bit. In implementations where affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in `GICR_IGROUPR0` to form a 2-bit field that defines an interrupt group:

<table>
<thead>
<tr>
<th>Group modifier bit</th>
<th>Group status bit</th>
<th>Definition</th>
<th>Short name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>Secure Group 0</td>
<td>G0S</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>Non-secure Group 1</td>
<td>G1NS</td>
</tr>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>Secure Group 1</td>
<td>G1S</td>
</tr>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>Reserved, treated as Non-secure Group 1</td>
<td>-</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the GICR_IGRPMODR0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_IGRPMODR0, the corresponding bit is **RES0** and equivalent functionality is provided by `GICD_IGRPMODR<n>` with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by `GICD_IGRPMODR<n>`.

When `GICD_CTLR.ARE_S == 0` or `GICD_CTLR.DS == 1`, GICR_IGRPMODR0 is **RES0**. An implementation can make this register RAZ/WI in this case.

When `GICD_CTLR.DS==0`, the register is RAZ/WI to Non-secure accesses.
Bits corresponding to unimplemented interrupts are RAZ/WI.

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

**GICR_IGRPMODR0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0000</td>
<td>GICR_IGRPMODR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_IGRPMODR\(n\)E, Interrupt Group Modifier Registers, \(n = 1 - 2\)

The GICR_IGRPMODR\(n\)E characteristics are:

**Purpose**

When GIC_D_CTLR.DS\(==0\), this register together with the GICR_IGROUPR\(n\)E registers, controls whether the corresponding interrupt is in:

- Secure Group 0.
- Non-secure Group 1.
- When System register access is enabled, Secure Group 1.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_IGRPMODR\(n\)E are \texttt{RES0}.

When GIC_D_CTLR.DS\(==0\), this register is Secure.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_IGRPMODR\(n\)E is a 32-bit register.

**Field descriptions**

The GICR_IGRPMODR\(n\)E bit assignments are:

<table>
<thead>
<tr>
<th>Group modifier bit</th>
<th>Group status bit</th>
<th>Definition</th>
<th>Short name</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>0b0</td>
<td>Secure Group 0</td>
<td>G0S</td>
</tr>
<tr>
<td>0b0</td>
<td>0b1</td>
<td>Non-secure Group 1</td>
<td>G1NS</td>
</tr>
<tr>
<td>0b1</td>
<td>0b0</td>
<td>Secure Group 1</td>
<td>G1S</td>
</tr>
<tr>
<td>0b1</td>
<td>0b1</td>
<td>Reserved, treated as Non-secure Group 1</td>
<td>-</td>
</tr>
</tbody>
</table>

Group modifier bit. In implementations where affinity routing is enabled for the Security state of an interrupt, the bit that corresponds to the interrupt is concatenated with the equivalent bit in GICR_IGROUPR\(n\)E to form a 2-bit field that defines an interrupt group:

- On a Warm reset, this field resets to an architecturally \texttt{UNKNOWN} value.

For INTID \(m\), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_IGRPMODR\(n\)E number, \(n\), is given by \(n = (m-1024) \text{ DIV} \ 32\).
- The offset of the required GICR_IGRPMODR\(n\)E is \((0x000 + (4*n))\).
- The bit number of the required group modifier bit in this register is \((m-1024) \text{ MOD} \ 32\).
Accessing the GICR_IGRPMODR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICR_IGRPMODR<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, the register is RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_IGRPMODR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0000 + (4 * n)</td>
<td>GICR_IGRPMODR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_IIDR characteristics are:

**Purpose**

Provides information about the implementer and revision of the Redistributor.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states, this register is Common.

**Attributes**

GICR_IIDR is a 32-bit register.

**Field descriptions**

The GICR_IIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Range</th>
<th>Field</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>ProductID</td>
</tr>
<tr>
<td>23-20</td>
<td>RES0</td>
</tr>
<tr>
<td>19-16</td>
<td>Variant</td>
</tr>
<tr>
<td>15-12</td>
<td>Revision</td>
</tr>
<tr>
<td>11-0</td>
<td>Implementer</td>
</tr>
</tbody>
</table>

**ProductID, bits [31:24]**

An IMPLEMENTATION DEFINED product identifier.

**Bits [23:20]**

Reserved, RES0.

**Variant, bits [19:16]**

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish product variants, or major revisions of a product.

**Revision, bits [15:12]**

An IMPLEMENTATION DEFINED revision number. Typically, this field is used to distinguish minor revisions of a product.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the Redistributor:

- Bits [11:8] are the JEP106 continuation code of the implementer. For an Arm implementation, this field is 0x4.
- Bit [7] is always 0.
- Bits [6:0] are the JEP106 identity code of the implementer. For an Arm implementation, bits [7:0] are therefore 0x3B.
Accessing the GICR_IIDR

GICR_IIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC RDistributor</td>
<td>RD_base</td>
<td>0x0004</td>
<td>GICR_IIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
The GIC characteristics are:

**Purpose**

Invalidates any cached configuration data of all physical LPIs, causing the GIC to reload the interrupt configuration from the physical LPI Configuration table at the address specified by GICR_PROPBASER.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_INVALLR is a 64-bit register.

**Field descriptions**

The GICR_INVALLR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| V  | RES0 | vPEID | RES0 | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |

**V, bit [63]**

When FEAT_GICv4p1 is implemented:

Indicates whether the INTID is virtual or physical.

<table>
<thead>
<tr>
<th>V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalidate is for a physical INTID.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalidate is for a virtual INTID.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

**Bits [62:48]**

Reserved, RES0.

**vPEID, bits [47:32]**

When FEAT_GICv4p1 is implemented:

When GICR_INVLPIR.V == 0, this field is RES0

When GICR_INVLPIR.V == 1, this field is the target vPEID of the invalidate.

**Note**
The size of this field is IMPLEMENTATION DEFINED, and is specified by the
GICD_TYPER2.VIL and GICD_TYPER2.VID fields. Unimplemented bits are
RES0.

Otherwise:
Reserved, RES0.

Bits [31:0]
Reserved, RES0.

Note
If any LPI has been forwarded to the PE and a valid write to GICR_INVALLR is
received, the Redistributor must ensure it reloads its properties from memory.
This has no effect on the forwarded LPI if it has already been activated.

Accessing the GICR_INVALLR

This register is mandatory when any of the following are true:

- GICR_TYPER.Direct is 1.
- GICR_CTLR.IR is 1.
- GICv4.1 is implemented.

Otherwise, the functionality is IMPLEMENTATION DEFINED.

Writes to this register have no effect if no physical LPIs are currently stored in the local Redistributor cache.

GICR_INVALLR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC</td>
<td>RD_base</td>
<td>0x0080</td>
<td>GICR_INVALLR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are WO.
- When an access is Secure accesses to this register are WO.
- When an access is Non-secure accesses to this register are WO.
GICR_INVLPiR, Redistributor Invalidate LPI Register

The GICR_INVLPiR characteristics are:

**Purpose**

Invalidates the cached configuration data of a specified LPI, causing the GIC to reload the interrupt configuration from the physical LPI Configuration table at the address specified by GICR_PROPBASER.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_INVLPiR is a 64-bit register.

**Field descriptions**

The GICR_INVLPiR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| V | RES0 | INTID | vPEID |

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

**V, bit [63]**

When FEAT_GICv4p1 is implemented:

Indicates whether the INTID is virtual or physical.

<table>
<thead>
<tr>
<th>V</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Invalidate is for a physical INTID.</td>
</tr>
<tr>
<td>0b1</td>
<td>Invalidate is for a virtual INTID.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

**Bits [62:48]**

Reserved, RES0.

**vPEID, bits [47:32]**

When FEAT_GICv4p1 is implemented:

When GICR_INVLPiR.V == 0, this field is RES0

When GICR_INVLPiR.V == 1, this field is the target vPEID of the invalidate.

**Note**
The size of this field is IMPLEMENTATION DEFINED, and is specified by the
GICD_TYPER2.VIL and GICD_TYPER2.VID fields. Unimplemented bits are
RES0.

Otherwise:

Reserved, RES0.

**INTID, bits [31:0]**

The INTID of the physical LPI to be cleaned.

**Note**

The size of this field is IMPLEMENTATION DEFINED, and is specified by the
GICD_TYPER.IDbits field. Unimplemented bits are RES0.

**Note**

If any LPI has been forwarded to the PE and a valid write to GICR_INVLPIR is
received, the Redistributor must ensure it reloads its properties from memory
and apply any changes by retrieving and reforwarding the LPI as required.
This has no effect on the forwarded LPI if it has already been activated.

**Accessing the GICR_INVLPIR**

When written with a 32-bit write the data is zero-extended to 64 bits.

This register is mandatory when any of the following are true:

- GICR_TYPER.Direct is 1.
- GICR_CTLR.IR is 1.
- GICv4.1 is implemented.

Otherwise, the functionality is IMPLEMENTATION DEFINED.

Writes to this register have no effect if either:

- The specified LPI is not currently stored in the local Redistributor.
- The pINTID field corresponds to an unimplemented LPI.

**GICR_INVLPIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x00A0</td>
<td>GICR_INVLPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are WO.
- When an access is Secure accesses to this register are WO.
- When an access is Non-secure accesses to this register are WO.
GICR_IPRIORITYR\(n\), Interrupt Priority Registers, \(n = 0 - 7\)

The GICR_IPRIORITYR\(n\) characteristics are:

**Purpose**

Holds the priority of the corresponding interrupt for each SGI and PPI supported by the GIC.

**Configuration**

A copy of these registers is provided for each Redistributor.

These registers are configured as follows:

- GICR_IPRIORITYR0-GICR_IPRIORITYR3 store the priority of SGIs.
- GICR_IPRIORITYR4-GICR_IPRIORITYR7 store the priority of PPIs.

**Attributes**

GICR_IPRIORITYR\(n\) is a 32-bit register.

**Field descriptions**

The GICR_IPRIORITYR\(n\) bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
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</tr>
</tbody>
</table>

*Priority_offset_3B*, bits [31:24]

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

*Priority_offset_2B*, bits [23:16]

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

*Priority_offset_1B*, bits [15:8]

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

*Priority_offset_0B*, bits [7:0]

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the GICR_IPRIORITYR<n>

These registers are used when affinity routing is enabled for the Security state of the interrupt. When affinity routing is not enabled the bits corresponding to the interrupt are RAZ/WI and GICD_IPRIORITYR<n> provides equivalent functionality.

These registers are used for SGIs and PPIs only. Equivalent functionality for SPIs is provided by GICD_IPRIORITYR<n>.

These registers are byte-accessible.

When GICD_CTLR.DS == 0:

- A field that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
- A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in 'Software accesses of interrupt priority' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than one time. The effect of the change must be visible in finite time.

**GICR_IPRIORITYR<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0400 + (4 * n)</td>
<td>GICR_IPRIORITYR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_IPRIORITYR<n>E characteristics are:

**Purpose**

Holds the priority of the corresponding interrupt for each extended PPI supported by the GIC.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_IPRIORITYR<n>E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_IPRIORITYR<n>E is a 32-bit register.

**Field descriptions**

The GICR_IPRIORITYR<n>E bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Priority_offset_3B |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Priority_offset_2B |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Priority_offset_1B |
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | Priority_offset_0B |

**Priority_offset_3B, bits [31:24]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 3. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_2B, bits [23:16]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 2. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_1B, bits [15:8]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 1. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Priority_offset_0B, bits [7:0]**

Interrupt priority value from an IMPLEMENTATION DEFINED range, at byte offset 0. Lower priority values correspond to greater priority of the interrupt.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For interrupt ID m, when DIV and MOD are the integer division and modulo operations:
• The corresponding GICR_IPRIORITYR<n> number, n, is given by \( n = (m-1024) \div 4 \).
• The offset of the required GICR_IPRIORITYR<n>E register is \((0x400 + (4*n))\).
• The byte offset of the required Priority field in this register is \( m \mod 4 \), where:
  ◦ Byte offset 0 refers to register bits [7:0].
  ◦ Byte offset 1 refers to register bits [15:8].
  ◦ Byte offset 2 refers to register bits [23:16].
  ◦ Byte offset 3 refers to register bits [31:24].

### Accessing the GICR_IPRIORITYR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISACTIVER<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS == 0:

• A field that corresponds to a Group 0 or Secure Group 1 interrupt is RAZ/WI to Non-secure accesses.
• A Non-secure access to a field that corresponds to a Non-secure Group 1 interrupt behaves as described in Software accesses of interrupt priority.

Bits corresponding to unimplemented interrupts are RAZ/WI.

---

**Note**

Implementations must ensure that an interrupt that is pending at the time of the write uses either the old value or the new value and must ensure that the interrupt is neither lost nor handled more than once. The effect of the change must be visible in finite time.

---

**GICR_IPRIORITYR<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0400 + (4*n)</td>
<td>GICR_IPRIORITYR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When GICD_CTLR.DS == 0 accesses to this register are **RW**.
• When an access is Secure accesses to this register are **RW**.
• When an access is Non-secure accesses to this register are **RW**.
The GICR_ISACTIVER0 characteristics are:

**Purpose**

Activates the corresponding SGI or PPI. These registers are used when saving and restoring GIC state.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISACTIVER0 is a 32-bit register.

**Field descriptions**

The GICR_ISACTIVER0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Set_active_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Set_active_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Set_active_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Set_active_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Set_active_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Set_active_bit26</td>
</tr>
<tr>
<td>25</td>
<td>Set_active_bit25</td>
</tr>
<tr>
<td>24</td>
<td>Set_active_bit24</td>
</tr>
<tr>
<td>23</td>
<td>Set_active_bit23</td>
</tr>
<tr>
<td>22</td>
<td>Set_active_bit22</td>
</tr>
<tr>
<td>21</td>
<td>Set_active_bit21</td>
</tr>
<tr>
<td>20</td>
<td>Set_active_bit20</td>
</tr>
<tr>
<td>19</td>
<td>Set_active_bit19</td>
</tr>
<tr>
<td>18</td>
<td>Set_active_bit18</td>
</tr>
<tr>
<td>17</td>
<td>Set_active_bit17</td>
</tr>
<tr>
<td>16</td>
<td>Set_active_bit16</td>
</tr>
<tr>
<td>15</td>
<td>Set_active_bit15</td>
</tr>
<tr>
<td>14</td>
<td>Set_active_bit14</td>
</tr>
<tr>
<td>13</td>
<td>Set_active_bit13</td>
</tr>
<tr>
<td>12</td>
<td>Set_active_bit12</td>
</tr>
<tr>
<td>11</td>
<td>Set_active_bit11</td>
</tr>
<tr>
<td>10</td>
<td>Set_active_bit10</td>
</tr>
<tr>
<td>9</td>
<td>Set_active_bit9</td>
</tr>
<tr>
<td>8</td>
<td>Set_active_bit8</td>
</tr>
<tr>
<td>7</td>
<td>Set_active_bit7</td>
</tr>
<tr>
<td>6</td>
<td>Set_active_bit6</td>
</tr>
<tr>
<td>5</td>
<td>Set_active_bit5</td>
</tr>
<tr>
<td>4</td>
<td>Set_active_bit4</td>
</tr>
<tr>
<td>3</td>
<td>Set_active_bit3</td>
</tr>
<tr>
<td>2</td>
<td>Set_active_bit2</td>
</tr>
<tr>
<td>1</td>
<td>Set_active_bit1</td>
</tr>
<tr>
<td>0</td>
<td>Set_active_bit0</td>
</tr>
</tbody>
</table>

**Set_active_bit<x>, bit [x], for x = 31 to 0**

Adds the active state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_active_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or is active and pending. If written, activates the corresponding interrupt, if the interrupt is not already active. If the interrupt is already active, the write has no effect. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICR_ISACTIVER0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISACTIVER0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ISACTIVER<n> with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ISACTIVER<n>.

When GICD_CTLR.DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.

**GICR_ISACTIVER0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0300</td>
<td>GICR_ISACTIVER0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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GICR_ISACTIVER\(<n>E\), Interrupt Set-Active Registers, \(n = 1 - 2\)

The GICR_ISACTIVER\(<n>E\) characteristics are:

**Purpose**

Adds the active state to the corresponding PPI.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ISACTIVER\(<n>E\) are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISACTIVER\(<n>E\) is a 32-bit register.

**Field descriptions**

The GICR_ISACTIVER\(<n>E\) bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_active_bit31</td>
<td>Set_active_bit30</td>
<td>Set_active_bit29</td>
<td>Set_active_bit28</td>
<td>Set_active_bit27</td>
<td>Set_active_bit26</td>
<td>Set_active_bit25</td>
</tr>
</tbody>
</table>

**Set_active_bit\(<x>\), bit \([x]\), for \(x = 31\) to \(0\)**

For the extended PPIs, adds the active state to interrupt number \(x\). Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_active_bit(&lt;x&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not active, and is not active and pending. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is active, or active and pending on this PE. If written, activates the corresponding interrupt, if the interrupt is not already active. If the interrupt is already active, the write has no effect. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

For INTID \(m\), when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ISACTIVER\(<n>E\) number, \(n\), is given by \(n = (m-1024) \text{ DIV } 32\).
- The offset of the required GICR_ISACTIVER\(<n>E\) is \((0x200 + (4*n))\).
- The bit number of the required group modifier bit in this register is \((m-1024) \text{ MOD } 32\).

**Accessing the GICR_ISACTIVER\(<n>E\)**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISACTIVER\(<n>E\), the corresponding bit is RES0.

When GICD_CTRLR.DS==0, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.
Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_ISACTIVER<n>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0300 + (4 * (n))</td>
<td>GICR_ISACTIVER&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
**GICR_ISENABLER0, Interrupt Set-Enable Register 0**

The GICR_ISENABLER0 characteristics are:

**Purpose**

Enables forwarding of the corresponding SGI or PPI to the CPU interfaces.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISENABLER0 is a 32-bit register.

**Field descriptions**

The GICR_ISENABLER0 bit assignments are:

<p>| | | | | | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
</tr>
<tr>
<td>Set_enable_bit31</td>
<td>Set_enable_bit30</td>
<td>Set_enable_bit29</td>
<td>Set_enable_bit28</td>
<td>Set_enable_bit27</td>
<td>Set_enable_bit26</td>
<td>Set_enable_bit25</td>
<td>Set_enable_bit24</td>
</tr>
</tbody>
</table>

**Set_enable_bit<x>, bit [x], for x = 31 to 0**

For PPIs and SGIs, controls the forwarding of interrupt number x to the CPU interface. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_enable_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, enables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Accessing the GICR_ISENABLER0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISENABLER0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ISENABLER<n> with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ISENABLER<n>.

When GICD_CTLR.DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.

**GICR_ISENABLER0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0100</td>
<td>GICR_ISENABLER0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_ISENABLER<n>E, Interrupt Set-Enable Registers, n = 1 - 2

The GICR_ISENABLER<n>E characteristics are:

**Purpose**

Enables forwarding of the corresponding PPI to the CPU interfaces.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ISENABLER<n>E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISENABLER<n>E is a 32-bit register.

**Field descriptions**

The GICR_ISENABLER<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_enable_bit31</td>
<td>Set_enable_bit30</td>
<td>Set_enable_bit29</td>
<td>Set_enable_bit28</td>
<td>Set_enable_bit27</td>
<td>Set_enable_bit26</td>
<td>Set_enable_bit25</td>
</tr>
</tbody>
</table>

**Set_enable_bit<x>, bit [x], for x = 31 to 0**

For the extended PPI range, controls the forwarding of interrupt number x to the CPU interface. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_enable_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that forwarding of the corresponding interrupt is disabled. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that forwarding of the corresponding interrupt is enabled. If written, enables forwarding of the corresponding interrupt. After a write of 1 to this bit, a subsequent read of this bit returns 1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ISENABLER<n>E number, n, is given by n = (m-1024) DIV 32.
- The offset of the required GICR_ISENABLER<n>E is (0x100 + (4*n)).
- The bit number of the required group modifier bit in this register is (m-1024) MOD 32.

**Accessing the GICR_ISENABLER<n>E**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISENABLER<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.
Bits corresponding to unimplemented interrupts are RAZ/WI.

**GICR_ISENABLER<\(n\)>E can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0100 + (4 * (n))</td>
<td>GICR_ISENABLER&lt;(n)&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_ISPENDR0 characteristics are:

**Purpose**

Adds the pending state to the corresponding SGI or PPI.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISPENDR0 is a 32-bit register.

**Field descriptions**

The GICR_ISPENDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Set_pending_bit31</td>
</tr>
<tr>
<td>30</td>
<td>Set_pending_bit30</td>
</tr>
<tr>
<td>29</td>
<td>Set_pending_bit29</td>
</tr>
<tr>
<td>28</td>
<td>Set_pending_bit28</td>
</tr>
<tr>
<td>27</td>
<td>Set_pending_bit27</td>
</tr>
<tr>
<td>26</td>
<td>Set_pending_bit26</td>
</tr>
<tr>
<td>25</td>
<td>Set_pending_bit25</td>
</tr>
<tr>
<td>24</td>
<td>Set_pending_bit24</td>
</tr>
<tr>
<td>23</td>
<td>Set_pending_bit23</td>
</tr>
<tr>
<td>22</td>
<td>Set_pending_bit22</td>
</tr>
<tr>
<td>21</td>
<td>Set_pending_bit21</td>
</tr>
<tr>
<td>20</td>
<td>Set_pending_bit20</td>
</tr>
<tr>
<td>19</td>
<td>Set_pending_bit19</td>
</tr>
<tr>
<td>18</td>
<td>Set_pending_bit18</td>
</tr>
<tr>
<td>17</td>
<td>Set_pending_bit17</td>
</tr>
<tr>
<td>16</td>
<td>Set_pending_bit16</td>
</tr>
<tr>
<td>15</td>
<td>Set_pending_bit15</td>
</tr>
<tr>
<td>14</td>
<td>Set_pending_bit14</td>
</tr>
<tr>
<td>13</td>
<td>Set_pending_bit13</td>
</tr>
<tr>
<td>12</td>
<td>Set_pending_bit12</td>
</tr>
<tr>
<td>11</td>
<td>Set_pending_bit11</td>
</tr>
<tr>
<td>10</td>
<td>Set_pending_bit10</td>
</tr>
<tr>
<td>9</td>
<td>Set_pending_bit9</td>
</tr>
<tr>
<td>8</td>
<td>Set_pending_bit8</td>
</tr>
<tr>
<td>7</td>
<td>Set_pending_bit7</td>
</tr>
<tr>
<td>6</td>
<td>Set_pending_bit6</td>
</tr>
<tr>
<td>5</td>
<td>Set_pending_bit5</td>
</tr>
<tr>
<td>4</td>
<td>Set_pending_bit4</td>
</tr>
<tr>
<td>3</td>
<td>Set_pending_bit3</td>
</tr>
<tr>
<td>2</td>
<td>Set_pending_bit2</td>
</tr>
<tr>
<td>1</td>
<td>Set_pending_bit1</td>
</tr>
<tr>
<td>0</td>
<td>Set_pending_bit0</td>
</tr>
</tbody>
</table>

**Set_pending_bit<x>, bit [x], for x = 31 to 0**

For PPIs and SGIs, adds the pending state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending on this PE. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is pending, or active and pending on this PE. If written, changes the state of the corresponding interrupt from inactive to pending, or from active to active and pending. This has no effect in the following cases:</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is already pending because of a write to GICR_ISPENDR0.</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is already pending because the corresponding interrupt signal is asserted. In this case, the interrupt remains pending if the interrupt signal is deasserted.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the GICR_ISPENDR0**

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISPENDR0, the corresponding bit is RAZ/WI and equivalent functionality is provided by GICD_ISPENDR<n> with n=0.

This register only applies to SGIs (bits [15:0]) and PPIs (bits [31:16]). For SPIs, this functionality is provided by GICD_ISPENDR<n>.

When GICD_CTLR_DS == 0, bits corresponding to Secure SGIs and PPIs are RAZ/WI to Non-secure accesses.
**GICR_ISPENDR0 can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0200</td>
<td>GICR_ISPENDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_ISPENDR<n>E, Interrupt Set-Pending Registers, n = 1 - 2

The GICR_ISPENDR<n>E characteristics are:

**Purpose**

Adds the pending state to the corresponding PPI.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_ISPENDR<n>E are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_ISPENDR<n>E is a 32-bit register.

**Field descriptions**

The GICR_ISPENDR<n>E bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Set_pending_bit31</td>
<td>Set_pending_bit30</td>
<td>Set_pending_bit29</td>
<td>Set_pending_bit28</td>
<td>Set_pending_bit27</td>
<td>Set_pending_bit26</td>
</tr>
</tbody>
</table>

**Set_pending_bit<x>, bit [x], for x = 31 to 0**

For the extended PPIs, adds the pending state to interrupt number x. Reads and writes have the following behavior:

<table>
<thead>
<tr>
<th>Set_pending_bit&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If read, indicates that the corresponding interrupt is not pending on this PE. If written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>If read, indicates that the corresponding interrupt is pending, or active and pending on this PE. If written, changes the state of the corresponding interrupt from inactive to pending, or from active to active and pending. This has no effect in the following cases:</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is already pending because of a write to GICR_ISPENDR&lt;n&gt;E.</td>
</tr>
<tr>
<td></td>
<td>• If the interrupt is already pending because the corresponding interrupt signal is asserted. In this case, the interrupt remains pending if the interrupt signal is deasserted.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

For INTID m, when DIV and MOD are the integer division and modulo operations:

- The corresponding GICR_ISPENDR<n>E number, n, is given by \( n = (m-1024) \div 32 \).
- The offset of the required GICR_ISPENDR<n>E is \( 0x200 + (4*n) \).
- The bit number of the required group modifier bit in this register is \( (m-1024) \mod 32 \).
Accessing the GICR_ISPENDR<n>E

When affinity routing is not enabled for the Security state of an interrupt in GICR_ISPENDR<n>E, the corresponding bit is RES0.

When GICD_CTLR.DS==0, bits corresponding to Secure PPIs are RAZ/WI to Non-secure accesses.

Bits corresponding to unimplemented interrupts are RAZ/WI.

GICR_ISPENDR<n>E can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0200 + (4 * n)</td>
<td>GICR_ISPENDR&lt;n&gt;E</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_MPAMIDR characteristics are:

**Purpose**

Reports the maximum support PARTID and PMG values.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_MPAMIDR are RES0.

A copy of this register is provided for each Redistributor.

When GICR_TYPER_MPAM==0, this register is RES0.

**Attributes**

GICR_MPAMIDR is a 32-bit register.

**Field descriptions**

The GICR_MPAMIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PMGmax</td>
</tr>
<tr>
<td>24</td>
<td>PARTIDmax</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**PMGmax, bits [23:16]**

Maximum PMG value supported.

**PARTIDmax, bits [15:0]**

Maximum PARTID value supported.

**Accessing the GICR_MPAMIDR**

GICR_MPAMIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0018</td>
<td>GICR_MPAMIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GICR_NSACR, Non-secure Access Control Register

The GICR_NSACR characteristics are:

**Purpose**

Enables Secure software to permit Non-secure software to create SGIs targeting the PE connected to this Redistributor by writing to ICC_SGI1R_EL1, ICC_ASGI1R_EL1 or ICC_SGI0R_EL1.

For more information, see 'Forwarding an SGI to a target PE' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Configuration**

For a description on when a write to ICC_SGI0R_EL1, ICC_SGI1R_EL1 or ICC_ASGI1R_EL1 is permitted to generate an interrupt, see 'Use of control registers for SGI forwarding' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Attributes**

GICR_NSACR is a 32-bit register.

**Field descriptions**

The GICR_NSACR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NS_access15 | NS_access14 | NS_access13 | NS_access12 | NS_access11 | NS_access10 | NS_access9 | NS_access8 | NS_access7 |

**NS_access<x>, bits [2x+1:2x], for x = 15 to 0**

Configures the level of Non-secure access permitted when the SGI is in Secure Group 0 or Secure Group 1, as defined from GICR_IGROUPR0 and GICR_IGRPMODR0. A field is provided for each SGI. The possible values of each 2-bit field are:

<table>
<thead>
<tr>
<th>NS_access&lt;x&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-secure writes are not permitted to generate Secure Group 0 SGIs or Secure Group 1 SGIs.</td>
</tr>
<tr>
<td>0b01</td>
<td>Non-secure writes are permitted to generate a Secure Group 0 SGI.</td>
</tr>
<tr>
<td>0b10</td>
<td>As 0b01, but additionally Non-secure writes to are permitted to generate a Secure Group 1 SGI.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. If the field is programmed to the reserved value, then the hardware will treat the field as if it has been programmed to an IMPLEMENTATION DEFINED choice of the valid values. However, to maintain the principle that as the value increases additional accesses are permitted Arm strongly recommends that implementations treat this value as 0b10. It is IMPLEMENTATION DEFINED whether the value read back is the value programmed or the valid value chosen.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICR_NSACR**

When GICD_CTRLR.DS == 1, this register is RAZ/WI.
When `GICD_CTLR.DS == 0`, this register is Secure, and is RAZ/WI to Non-secure accesses.

This register is used when affinity routing is enabled. When affinity routing is not enabled for the Security state of the interrupt, `GICD_NSACR<n>` with n=0 provides equivalent functionality.

This register does not support PPIs.

**GICR_NSACR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>SGI_base</td>
<td>0x0E00</td>
<td>GICR_NSACR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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GICR_PARTIDR, Set PARTID and PMG Register

The GICR_PARTIDR characteristics are:

Purpose

Sets the PARTID and PMG values used for memory accesses by the Redistributor.

Configuration

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GICR_PARTIDR are RES0.

A copy of this register is provided for each Redistributor.

When GICR_TYPER.MPAM==0, this register is RES0.

Attributes

GICR_PARTIDR is a 32-bit register.

Field descriptions

The GICR_PARTIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:24</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>23:16</td>
<td>PMG value used when Redistributor accesses memory. It is IMPLEMENTATION DEFINED whether bits not needed to represent PMG values in the range 0 to PMG_MAX are stateful or RES0. On a Warm reset, this field resets to 0.</td>
</tr>
<tr>
<td>15:0</td>
<td>PARTID value used when Redistributor accesses memory. It is IMPLEMENTATION DEFINED whether bits not needed to represent PARTID values in the range 0 to PARTID_MAX are stateful or RES0. On a Warm reset, this field resets to 0.</td>
</tr>
</tbody>
</table>

Accessing the GICR_PARTIDR

GICR_PARTIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

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This interface is accessible as follows:

- When \( \text{GICD_CTLR.DS} == 0 \) accesses to this register are \text{RW}.
- When an access is Secure accesses to this register are \text{RW}.
- When an access is Non-secure accesses to this register are \text{RW}.
The GICR_PENDBASER characteristics are:

**Purpose**

Specifies the base address of the LPI Pending table, and the Shareability and Cacheability of accesses to the LPI Pending table.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_PENDBASER is a 64-bit register.

**Field descriptions**

The GICR_PENDBASER bit assignments are:

<table>
<thead>
<tr>
<th>Bit [63]</th>
<th>Reserved, RE0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>PTZ, bit [62]</td>
<td>Pending Table Zero. Indicates to the Redistributor whether the LPI Pending table is zero when GICR_CTLR.EnableLPi == 1. This field is WO, and reads as 0.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PTZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The LPI Pending table is not zero, and contains live data.</td>
</tr>
<tr>
<td>0b1</td>
<td>The LPI Pending table is zero. Software must ensure the LPI Pending table is zero before this value is written.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bits [61:59]</th>
<th>Reserved, RE0.</th>
</tr>
</thead>
<tbody>
<tr>
<td>OuterCache, bits [58:56]</td>
<td>Indicates the Outer Cacheability attributes of accesses to the LPI Pending table. The possible values of this field are:</td>
</tr>
</tbody>
</table>
OuterCache

| 0b000 | Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability. |
| 0b001 | Normal Outer Non-cacheable. |
| 0b010 | Normal Outer Cacheable Read-allocate, Write-through. |
| 0b011 | Normal Outer Cacheable Read-allocate, Write-back. |
| 0b100 | Normal Outer Cacheable Write-allocate, Write-through. |
| 0b101 | Normal Outer Cacheable Write-allocate, Write-back. |
| 0b110 | Normal Outer Cacheable Read-allocate, Write-allocate, Write-through. |
| 0b111 | Normal Outer Cacheable Read-allocate, Write-allocate, Write-back. |

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [55:52]**

Reserved, RES0.

**Physical Address, bits [51:16]**

Bits [51:16] of the physical address containing the LPI Pending table.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:12]**

Reserved, RES0.

**Shareability, bits [11:10]**

Indicates the Shareability attributes of accesses to the LPI Pending table. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**InnerCache, bits [9:7]**

Indicates the Inner Cacheability attributes of accesses to the LPI Pending table. The possible values of this field are:

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [6:0]**

Reserved, RES0.

**Accessing the GICR_PENDBASER**

Having the GICR_PENDBASER OuterCache, Shareability or InnerCache fields programmed to different values on different Redistributors with **GICR_CTLR**.EnableLPi == 1 in the system is UNPREDICTABLE.

Changing GICR_PENDBASER with **GICR_CTLR**.EnableLPi == 1 is UNPREDICTABLE.

**GICR_PENDBASER** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0078</td>
<td>GICR_PENDBASER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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The GICR_PROPBASER characteristics are:

**Purpose**

Specifies the base address of the LPI Configuration table, and the Shareability and Cacheability of accesses to the LPI Configuration table.

**Configuration**

A copy of this register is provided for each Redistributor.

An implementation might make this register RO, for example to correspond to an LPI Configuration table in read-only memory.

**Attributes**

GICR_PROPBASER is a 64-bit register.

**Field descriptions**

The GICR_PROPBASER bit assignments are:

<table>
<thead>
<tr>
<th>Bit Positions</th>
<th>Bit Assignments</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:59</td>
<td>RES0 OuterCache RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>31:0</td>
<td>Physical Address Shareability InnerCache RES0 IDbits</td>
<td>Physical Address, InnerCache, RES0, IDbits.</td>
</tr>
</tbody>
</table>

**Bits [63:59]**

Reserved, RES0.

**OuterCache, bits [58:56]**

Indicates the Outer Cacheability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [55:52]

Reserved, RES0.

Physical_Address, bits [51:12]

Bits [51:12] of the physical address containing the LPI Configuration table.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Shareability, bits [11:10]

Indicates the Shareability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

InnerCache, bits [9:7]

Indicates the Inner Cacheability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [6:5]

Reserved, RES0.

IDbits, bits [4:0]

The number of bits of LPI INTID supported, minus one, by the LPI Configuration table starting at Physical_Address.

If the value of this field is larger than the value of GICD_TYPER.IDbits, the GICD_TYPER.IDbits value applies.

If the value of this field is less than 0b1101, indicating that the largest INTID is less than 8192 (the smallest LPI interrupt ID), the GIC will behave as if all physical LPis are out of range.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the GICR_PROPBASER

It is IMPLEMENTATION DEFINED whether GICR_PROPBASER can be set to different values on different Redistributors. GICR_TYPER.CommonLPIAff identifies the Redistributors that must have GICR_PROPBASER set to the same values whenever GICR_CTLR.EnableLPIs == 1.

Setting different values in different copies of GICR_PROPBASER on Redistributors that are required to use a common LPI Configuration table when GICR_CTLR.EnableLPIs == 1 leads to UNPREDICTABLE behavior.

Other restrictions apply when a Redistributor caches information from GICR_PROPBASER. For more information, see 'LPI Configuration tables' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

GICR_PROPBASER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0070</td>
<td>GICR_PROPBASER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_SETLPIR characteristics are:

**Purpose**

Generates an LPI by setting the pending state of the specified LPI.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICR_SETLPIR are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_SETLPIR is a 64-bit register.

**Field descriptions**

The GICR_SETLPIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:32</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>31:0</td>
<td>pINTID, bits [31:0]</td>
</tr>
</tbody>
</table>

**Bits [63:32]**

Reserved, RES0.

**pINTID, bits [31:0]**

The INTID of the physical LPI to be generated.

---

**Note**

The size of this field is IMPLEMENTATION DEFINED, and is specified by the GICD_TYPER.IDbits field. Unimplemented bits are RES0.

**Accessing the GICR_SETLPIR**

When written with a 32-bit write the data is zero-extended to 64 bits.

This register is mandatory in an implementation that supports LPIS and does not include an ITS. The functionality is IMPLEMENTATION DEFINED in an implementation that does include an ITS.

Writes to this register have no effect if either:

- The pINTID field corresponds to an LPI that is already pending.
- The pINTID field corresponds to an unimplemented LPI.
- GICR_CTLR_EnableLPIS == 0.
**GICR_SETLPIR** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0040</td>
<td>GICR_SETLPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
GICR_STATUSR, Error Reporting Status Register

The GICR_STATUSR characteristics are:

**Purpose**

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

**Configuration**

A copy of this register is provided for each Redistributor.

If the GIC implementation supports two Security states this register is Banked to provide Secure and Non-secure copies.

**Attributes**

GICR_STATUSR is a 32-bit register.

**Field descriptions**

The GICR_STATUSR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, RES0.

**WROD, bit [3]**

Write to an RO location.

<table>
<thead>
<tr>
<th>WROD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to an RO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**RWOD, bit [2]**

Read of a WO location.

<table>
<thead>
<tr>
<th>RWOD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a WO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**WRD, bit [1]**

Write to a reserved location.
When a violation is detected, software must write 1 to this register to reset it.

**RRD, bit [0]**

Read of a reserved location.

<table>
<thead>
<tr>
<th>RRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**Accessing the GICR_STATUSR**

This is an optional register. If the register is not implemented, the location is RAZ/WI.

**GICR_STATUSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0010</td>
<td>GICR_STATUSR(S)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0010</td>
<td>GICR_STATUSR(NS)</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICR_SYNCR, Redistributor Synchronize Register

The GICR_SYNCR characteristics are:

**Purpose**

Indicates completion of register based invalidate operations.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_SYNCR is a 32-bit register.

**Field descriptions**

The GICR_SYNCR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-1</td>
<td>RES0</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Busy</td>
<td>Indicates completion of invalidation operations</td>
</tr>
</tbody>
</table>

**Busy, bit [0]**

Indicates completion of invalidation operations

<table>
<thead>
<tr>
<th>Busy</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No operations are in progress.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write is in progress to one or more of the following registers:</td>
</tr>
<tr>
<td></td>
<td>• GICR_INVLPIR.</td>
</tr>
<tr>
<td></td>
<td>• GICR_INVALLR.</td>
</tr>
<tr>
<td></td>
<td>• GICv3, GICR_CLRLPIR.</td>
</tr>
</tbody>
</table>

This field tracks operations initiated on the same Redistributor.

**Accessing the GICR_SYNCR**

When this register is accessed, it is optional that an implementation might wait until all operations are complete before returning a value, in which case GICR_SYNCR.Busy is always 0.

This register is mandatory when any of the following are true:

- GICR_TYPER.Direct is 1.
- GICR_CTLR.IR is 1.
- GICv4.1 is implemented.

Otherwise, the functionality is IMPLEMENTATION DEFINED.

**GICR_SYNCR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
The GICR_TYPER characteristics are:

**Purpose**

Provides information about the configuration of this Redistributor.

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_TYPER is a 64-bit register.

**Field descriptions**

The GICR_TYPER bit assignments are:

<table>
<thead>
<tr>
<th>Affinity Value</th>
<th>VLPIS</th>
<th>PLPIS</th>
<th>Last</th>
<th>DirectLP</th>
<th>Dirty</th>
<th>MPAM</th>
<th>DPGS</th>
<th>RVPEID</th>
<th>Processor_Number</th>
<th>CommonLP</th>
<th>VSGI</th>
<th>PPInum</th>
</tr>
</thead>
<tbody>
<tr>
<td>6362616059</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55545352515049484746454443424140</td>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
<td>33</td>
<td>32</td>
</tr>
</tbody>
</table>

**Affinity_Value, bits [63:32]**

The identity of the PE associated with this Redistributor.

Bits [63:56] provide Aff3, the Affinity level 3 value for the Redistributor.

Bits [55:48] provide Aff2, the Affinity level 2 value for the Redistributor.

Bits [47:40] provide Aff1, the Affinity level 1 value for the Redistributor.

Bits [39:32] provide Aff0, the Affinity level 0 value for the Redistributor.

**PPInum, bits [31:27]**

When FEAT_GICv3p1 is implemented:

The value derived from this field specifies the maximum PPI INTID that a GIC implementation can support. An implementation might not implement all PPIs up to this maximum.

<table>
<thead>
<tr>
<th>PPInum</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000</td>
<td>Maximum PPI INTID is 31.</td>
</tr>
<tr>
<td>0b00001</td>
<td>Maximum PPI INTID is 1087.</td>
</tr>
<tr>
<td>0b00010</td>
<td>Maximum PPI INTID is 1119.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**Otherwise:**

Reserved, RES0.
**VSGI, bit [26]**

When **FEAT_GICv4p1** is implemented:

Indicates whether vSGIs are supported.

<table>
<thead>
<tr>
<th>VSGI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Direct injection of SGIs not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Direct injection of SGIs supported.</td>
</tr>
</tbody>
</table>

**Otherwise:**

Reserved, RES0.

**CommonLPIAff, bits [25:24]**

The affinity level at which Redistributors share an LPI Configuration table.

<table>
<thead>
<tr>
<th>CommonLPIAff</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>All Redistributors must share an LPI Configuration table.</td>
</tr>
<tr>
<td>0b01</td>
<td>All Redistributors with the same Aff3 value must share an LPI Configuration table.</td>
</tr>
<tr>
<td>0b10</td>
<td>All Redistributors with the same Aff3.Aff2 value must share an LPI Configuration table.</td>
</tr>
<tr>
<td>0b11</td>
<td>All Redistributors with the same Aff3.Aff2.Aff1 value must share an LPI Configuration table.</td>
</tr>
</tbody>
</table>

**Processor_Number, bits [23:8]**

A unique identifier for the PE. When **GITS_TYPER.PTA == 0**, an ITS uses this field to identify the interrupt target.

When affinity routing is disabled for a Security state, this field indicates which **GICD_ITARGETSR<n>** corresponds to this Redistributor.

**RVPEID, bit [7]**

When **FEAT_GICv4p1** is implemented:

Indicates how the resident vPE is specified.

<table>
<thead>
<tr>
<th>RVPEID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>GICR_VPENDBASER</strong> records the address of the vPE's Virtual Pending Table.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>GICR_VPENDBASER</strong> records vPEID.</td>
</tr>
</tbody>
</table>

**Otherwise:**

Reserved, RES0.

**MPAM, bit [6]**

When **FEAT_GICv3p1** is implemented:

<table>
<thead>
<tr>
<th>MPAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAM not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM supported.</td>
</tr>
</tbody>
</table>
Otherwise:

Reserved, RES0.

**DPGS, bit [5]**

Sets support for GICR_CTLR.DPG* bits.

<table>
<thead>
<tr>
<th>DPGS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICR_CTLR.DPG* bits are not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICR_CTLR.DPG* bits are supported.</td>
</tr>
</tbody>
</table>

**Last, bit [4]**

Indicates whether this Redistributor is the highest-numbered Redistributor in a series of contiguous Redistributor pages.

<table>
<thead>
<tr>
<th>Last</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This Redistributor is not the highest-numbered Redistributor in a series of contiguous Redistributor pages.</td>
</tr>
<tr>
<td>0b1</td>
<td>This Redistributor is the highest-numbered Redistributor in a series of contiguous Redistributor pages.</td>
</tr>
</tbody>
</table>

**DirectLPI, bit [3]**

Indicates whether this Redistributor supports direct injection of LPIs.

<table>
<thead>
<tr>
<th>DirectLPI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This Redistributor does not support direct injection of LPIs. The GICR_SETLPIR, GICR_CLRLPIR, GICR_INVLPIR, GICR_INVALLR, and GICR_SYNCR registers are either not implemented, or have an IMPLEMENTATION DEFINED purpose.</td>
</tr>
<tr>
<td>0b1</td>
<td>This Redistributor supports direct injection of LPIs. The GICR_SETLPIR, GICR_CLRLPIR, GICR_INVLPIR, GICR_INVALLR, and GICR_SYNCR registers are implemented.</td>
</tr>
</tbody>
</table>

**Dirty, bit [2]**

Controls the functionality of GICR_VPENDBASER.Dirty.

<table>
<thead>
<tr>
<th>Dirty</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICR_VPENDBASER.Dirty is UNKNOWN when GICR_VPENDBASER.Valid == 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICR_VPENDBASER.Dirty indicates when the Virtual Pending Table has been parsed when GICR_VPENDBASER.Valid is written from 0 to 1.</td>
</tr>
</tbody>
</table>

When GICR_TYPER.VLPIS == 0, this field is RES0.

**Note**

In GICv4p1 implementations this field is RES1.

**VLPIS, bit [1]**

Indicates whether the GIC implementation supports virtual LPIs and the direct injection of virtual LPIs.
<table>
<thead>
<tr>
<th>VLPIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation does not support virtual LPIs or the direct injection of virtual LPIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports virtual LPIs and the direct injection of virtual LPIs.</td>
</tr>
</tbody>
</table>

**Note**

In GICv3 implementations this field is res0.

---

### PLPIS, bit [0]

Indicates whether the GIC implementation supports physical LPIs.

<table>
<thead>
<tr>
<th>PLPIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The implementation does not support physical LPIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The implementation supports physical LPIs.</td>
</tr>
</tbody>
</table>

---

**Accessing the GICR_TYPER**

**GICR_TYPER can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0008</td>
<td>GICR_TYPER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
GICR_VPENDBASER, Virtual Redistributor LPI Pending Table Base Address Register

The GICR_VPENDBASER characteristics are:

### Purpose

Specifies the base address of the memory that holds the virtual LPI Pending table for the currently scheduled virtual machine.

### Configuration

#### Attributes

GICR_VPENDBASER is a 64-bit register.

#### Field descriptions

The GICR_VPENDBASER bit assignments are:

### When FEAT_GICv4 is implemented:

<table>
<thead>
<tr>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>Valid</td>
<td>bit [63]</td>
</tr>
<tr>
<td>0b0</td>
<td>The virtual LPI Pending table is not valid. No vPE is scheduled.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual LPI Pending table is valid. A vPE is scheduled.</td>
</tr>
</tbody>
</table>

Setting GICR_VPENDBASER.Valid == 1 when the associated CPU interface does not implement FEAT_GICv4 is UNPREDICTABLE.

#### Note

Software can determine whether a PE supports FEAT_GICv3 or FEAT_GICv4 by reading ID_AA64PFR0_EL1.

Writing a new value to any bit of GICR_VPENDBASER, other than GICR_VPENDBASER.Valid, when GICR_VPENDBASER.Valid==1 is UNPREDICTABLE.

On a Warm reset, this field resets to 0.

#### IDAI, bit [62]

Implementation Defined Area Invalid. Indicates whether the IMPLEMENTATION DEFINED area in the virtual LPI Pending table is valid.
For more information, see 'LPI Pending tables' and 'Virtual LPI Configuration tables and virtual LPI Pending tables' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**PendingLast, bit [61]**

Indicates whether there are pending and enabled interrupts for the last scheduled vPE.

This value is set by the implementation when GICR_VPENDBASER.Valid has been written from 1 to 0 and is otherwise **UNKNOWN**.

<table>
<thead>
<tr>
<th>PendingLast</th>
<th>Meaning</th>
<th>IDAI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There are no pending and enabled interrupts for the last scheduled vPE.</td>
<td>The IMPLEMENTATION DEFINED area is valid.</td>
<td></td>
</tr>
<tr>
<td>0b1</td>
<td>There is at least one pending interrupt for the last scheduled vPE. It is IMPLEMENTATION DEFINED whether this bit is set when the only pending interrupts for the last scheduled vPE are not enabled. Arm deprecates setting PendingLast to 1 when the only pending interrupts for the last scheduled virtual machine are not enabled.</td>
<td>The IMPLEMENTATION DEFINED area is invalid and all pending interrupt information is held in the architecturally defined part of the virtual LPI Pending table.</td>
<td></td>
</tr>
</tbody>
</table>

When the GICR_VPENDBASER.Valid bit is written from 0 to 1, this bit is RES1.

On a Warm reset, this field resets to 0.

**Dirty, bit [60]**

- **When GICR_VPENDBASER.Valid == 0:**
  Indicates whether a de-scheduling operation is in progress.
  This field is read-only.

<table>
<thead>
<tr>
<th>Dirty</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No de-scheduling operation in process.</td>
</tr>
<tr>
<td>0b1</td>
<td>De-scheduling operation in process.</td>
</tr>
</tbody>
</table>

Writing 1 to GICR_VPENDBASER.Valid is **UNPREDICTABLE** while GICR_VPENDBASER.Dirty==1.

On a Warm reset, this field resets to 0.

- **When GICR_VPENDBASER.Valid == 1 and GICR_TYPER.Dirty == 1:**
  This field is read-only. Reports whether the Virtual Pending table has been parsed.

<table>
<thead>
<tr>
<th>Dirty</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Parsing of the Virtual Pending Table has completed.</td>
</tr>
<tr>
<td>0b1</td>
<td>Parsing of the Virtual Pending Table has not completed.</td>
</tr>
</tbody>
</table>

Writing 1 to GICR_VPENDBASER.Valid is **UNPREDICTABLE** while GICR_VPENDBASER.Dirty == 1.

On a Warm reset, this field resets to 0.

**Otherwise:**

This field is read-only. This fields is **UNKNOWN**.
On a Warm reset, this field resets to 0.

**Bit [59]**

Reserved, RES0.

**OuterCache, bits [58:56]**

Indicates the Outer Cacheability attributes of accesses to virtual LPI Pending tables of vPEs targeting this Redistributor.

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

The Cacheability, Outer Cacheability and Shareability fields are used for accesses to the virtual LPI Pending table of resident and non-resident vPEs.

If the OuterCacheability attribute of the virtual LPI Pending tables that are associated with vPEs targeting the same Redistributor are different, behavior is UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [55:52]**

Reserved, RES0.

**Physical_Address, bits [51:16]**

Bits [51:16] of the physical address containing the virtual LPI Pending table.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are RES0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [15:12]**

Reserved, RES0.

**Shareability, bits [11:10]**

Indicates the Shareability attributes of accesses to the virtual LPI Pending table.

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.
The Cacheability, Outer Cacheability and Shareability fields are used for accesses to the virtual LPI Pending table of resident and non-resident vPEs.

If the Shareability attribute of the virtual LPI Pending tables that are associated with vPEs targeting the same Redistributor are different, behavior is **UNPREDICTABLE**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### InnerCache, bits [9:7]

Indicates the Inner Cacheability attributes of accesses to the virtual LPI Pending table.

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Write-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Write-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

The Cacheability, Outer Cacheability and Shareability fields are used for accesses to the virtual LPI Pending table of resident and non-resident vPEs.

If the InnerCacheability attribute of the virtual LPI Pending tables that are associated with vPEs targeting the same Redistributor are different, behavior is **UNPREDICTABLE**.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

### Bits [6:0]

Reserved, RES0.

### When FEAT_GICv4p1 is implemented:

<table>
<thead>
<tr>
<th>63</th>
<th>62</th>
<th>61</th>
<th>60</th>
<th>59</th>
<th>58</th>
<th>57</th>
<th>56</th>
<th>55</th>
<th>54</th>
<th>53</th>
<th>52</th>
<th>51</th>
<th>50</th>
<th>49</th>
<th>48</th>
<th>47</th>
<th>46</th>
<th>45</th>
<th>44</th>
<th>43</th>
<th>42</th>
<th>41</th>
<th>40</th>
<th>39</th>
<th>38</th>
<th>37</th>
<th>36</th>
<th>35</th>
<th>34</th>
<th>33</th>
<th>32</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Valid</th>
<th>Doorbell</th>
<th>PendingLast</th>
<th>Dirty</th>
<th>VGrp0En</th>
<th>VGrp1En</th>
<th>RES0</th>
<th>vPEID</th>
</tr>
</thead>
</table>

### Valid, bit [63]

This bit controls whether a vPE is scheduled:

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The virtual LPI Pending table is not valid. No vPE is scheduled.</td>
</tr>
<tr>
<td>0b1</td>
<td>The virtual LPI Pending table is valid. A vPE is scheduled.</td>
</tr>
</tbody>
</table>

Setting GICR_VPENDBASER.Valid == 1 when the associated CPU interface does not implement FEAT_GICv4 is **UNPREDICTABLE**.

### Note

Software can determine whether a PE supports FEAT_GICv3 or FEAT_GICv4 by reading ID_AA64PFR0_EL1.

Writing a new value to any bit of GICR_VPENDBASER, other than GICR_VPENDBASER.Valid, when GICR_VPENDBASER.Valid==1 is **UNPREDICTABLE**.

Setting GICR_VPENDBASER.Valid to 1 is **UNPREDICTABLE** if GICR_VPRPBASER.Valid == 0.

On a Warm reset, this field resets to 0.
Doorbell, bit [62]

When GICR_VPENDBASER.Valid is written from 1 to 0, this bit controls whether a default doorbell interrupt is requested for the descheduled vPE.

<table>
<thead>
<tr>
<th>Doorbell</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No default doorbell requested.</td>
</tr>
<tr>
<td>0b1</td>
<td>Default doorbell requested.</td>
</tr>
</tbody>
</table>

When GICR_VPENDBASER.Valid is written from 1 to 0, if there are outstanding enabled pending interrupts then this bit is treated as 0.

When GICR_VPENDBASER.Valid is written from 1 to 0, if GICR_VPENDBASER.PendingLast is written as 1 then this bit is treated as 0.

When GICR_VPENDBASER.Valid == 1, reads return an **UNKNOWN** value.

On a Warm reset, this field resets to an **UNKNOWN** value.

PendingLast, bit [61]

Indicates whether there are pending and enabled interrupts for the last scheduled vPE.

This value is set by the implementation when GICR_VPENDBASER.Valid is written from 1 to 0 and is otherwise **UNKNOWN**.

<table>
<thead>
<tr>
<th>PendingLast</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There are no pending and enabled interrupts for the last scheduled vPE.</td>
</tr>
<tr>
<td>0b1</td>
<td>There is at least one pending and enabled interrupt for the last scheduled vPE.</td>
</tr>
</tbody>
</table>

When the GICR_VPENDBASER.Valid bit is written from 0 to 1, this bit is **RES1**.

When GICR_VPENDBASER.Valid is written from 1 to 0, if GICR_VPENDBASER.PendingLast is written as 1, then this bit is set to an **UNKNOWN** value.

On a Warm reset, this field resets to an **UNKNOWN** value.

Dirty, bit [60]

**When GICR_VPENDBASER.Valid == 0:**

Read-only. Indicates whether a de-scheduling operation is in progress.

<table>
<thead>
<tr>
<th>Dirty</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No de-scheduling operation in progress.</td>
</tr>
<tr>
<td>0b1</td>
<td>De-scheduling operation in progress.</td>
</tr>
</tbody>
</table>

Writing 1 to GICR_VPENDBASER.Valid is **UNPREDICTABLE** while GICR_VPENDBASER.Dirty == 1.

On a Warm reset, this field resets to 0.

**Otherwise:**

Read-only. Reports whether the Virtual Pending table has been parsed.

<table>
<thead>
<tr>
<th>Dirty</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Parsing of the Virtual Pending Table is complete.</td>
</tr>
<tr>
<td>0b1</td>
<td>Parsing of the Virtual Pending Table has not completed.</td>
</tr>
</tbody>
</table>

Writing 1 to GICR_VPENDBASER.Valid is **UNPREDICTABLE** while GICR_VPENDBASER.Dirty == 1.

On a Warm reset, this field resets to 0.
Enable virtual Group 0 interrupts.

<table>
<thead>
<tr>
<th>VGrp0En</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Forwarding of virtual Group 0 interrupts disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Forwarding of virtual Group 0 interrupts enabled.</td>
</tr>
</tbody>
</table>

Writing a new value to VGrp0En while GICR_VPENDBASER.Valid==1 is CONSTRAINED UNPREDICTABLE:

- The update is ignored.
- The update is ignored for all purposes other than a direct read of the register.
- The virtual group enable is updated.

On a Warm reset, this field resets to an UNKNOWN value.

Enable virtual Group 1 interrupts.

<table>
<thead>
<tr>
<th>VGrp1En</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Forwarding of virtual Group 1 interrupts disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Forwarding of virtual Group 1 interrupts enabled.</td>
</tr>
</tbody>
</table>

Writing a new value to VGrp1En while GICR_VPENDBASER.Valid==1 is CONSTRAINED UNPREDICTABLE:

- The update is ignored.
- The update is ignored for all purposes other than a direct read of the register.
- The virtual group enable is updated.

On a Warm reset, this field resets to an UNKNOWN value.

Reserved, RES0.

When GICR_VPENDBASER.Valid == 1, ID of scheduled vPE.

When GICR_VPENDBASER.Valid == 1, if GICR_VPENDBASER.vPEID is set to a value greater than the configured vPEID width, the behavior of this field is CONSTRAINED UNPREDICTABLE:

- GICR_VPENDBASER.vPEID is treated as having an UNKNOWN valid value for all purposes other than a direct read of the register.
- GICR_VPENDBASER.Valid is treated as being set to 0 for all purposes other than a direct read of the register.

The size of this field is IMPLEMENTATION DEFINED, and is specified by the GICD_TYPER2.VIL and GICD_TYPER2.VID fields, unimplemented bits are RES0.

Accessing the GICR_VPENDBASER

The effect of a write to this register is not guaranteed to be visible throughout the affinity hierarchy, as indicated by GICR_CTLR.RWP == 0.

GICR_VPENDBASER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

Page 3839
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICR_VPROPBASER characteristics are:

**Purpose**

Specifies the base address of the memory that holds the virtual LPI Configuration table for the currently scheduled virtual machine.

**Configuration**

This register is provided in FEAT_GICv4 implementations only.

**Attributes**

GICR_VPROPBASER is a 64-bit register.

**Field descriptions**

The GICR_VPROPBASER bit assignments are:

**When FEAT_GICv4 is implemented:**

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63-59</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**OuterCache, bits [58:56]**

Indicates the Outer Cacheability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0000b</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0001b</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0010b</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0011b</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0100b</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0101b</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0110b</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0111b</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [55:52]
Reserved, RES0.

Physical Address, bits [51:12]
Bits [51:12] of the physical address containing the virtual LPI Configuration table.
In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are RES0.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

Shareability, bits [11:10]
Indicates the Shareability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.
On a Warm reset, this field resets to an architecturally UNKNOWN value.

InnerCache, bits [9:7]
Indicates the Inner Cacheability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [6:5]
Reserved, RES0.

IDbits, bits [4:0]
The number of bits of virtual LPI INTID supported, minus one.
If the value of this field is less than 0b1101, indicating that the largest INTID is less than 8192 (the smallest LPI interrupt ID), the GIC will behave as if all virtual LPIs are out of range.
On a Warm reset, this field resets to an architecturally UNKNOWN value.
When FEAT_GICv4p1 is implemented:

<table>
<thead>
<tr>
<th>Valid</th>
<th>RES0</th>
<th>Entry_Size</th>
<th>OuterCache</th>
<th>Indirect</th>
<th>Page_Size</th>
<th>Z</th>
<th>Physical_Address</th>
<th>Shareability</th>
<th>InnerCache</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
<td>23</td>
<td>22</td>
<td>21</td>
</tr>
<tr>
<td></td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
<td>13</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
</tbody>
</table>

Valid, bit [63]

This bit controls whether the vPE Configuration Table is valid:

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The vPE Configuration table is not valid.</td>
</tr>
<tr>
<td>0b1</td>
<td>The vPE Configuration table is valid.</td>
</tr>
</tbody>
</table>

TBC

On a Warm reset, this field resets to 0.

Bit [62]

Reserved, RES0.

Entry_Size, bits [61:59]

Specifies the number of bytes per table entry, minus one.

This bit is read-only.

OuterCache, bits [58:56]

Indicates the Outer Cacheability attributes of accesses to the table. The possible values of this field are:

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an UNKNOWN value.

Indirect, bit [55]

This field indicates whether GICR_VPROPBASER specifies a single, flat table or a two-level table where the first level contains a list of descriptors.

<table>
<thead>
<tr>
<th>Indirect</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Single Level. The Size field indicates the number of pages used to store data associated with each table entry.</td>
</tr>
<tr>
<td>0b1</td>
<td>Two Level. The Size field indicates the number of pages that contain an array of 64-bit descriptors to pages that are used to store the data associated with each table entry. A little endian memory order model is used.</td>
</tr>
</tbody>
</table>
This field is \texttt{RES0} for GIC implementations that only support flat tables.

On a Warm reset, this field resets to an \texttt{UNKNOWN} value.

**Page_Size, bits [54:53]**

The following values indicate the size of page that the translation table uses:

<table>
<thead>
<tr>
<th>Page Size</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>16KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b10.</td>
</tr>
</tbody>
</table>

\textbf{Note}

If the GIC implementation supports only a single, fixed page size, this field might be RO.

On a Warm reset, this field resets to an \texttt{UNKNOWN} value.

**Z, bit [52]**

When GICR\_VPROPBASER\_Valid is written from 0 to 1, GICR\_VPROPBASER\_Z indicates whether the vPE Configuration table is known to contain all zeros.

<table>
<thead>
<tr>
<th>Z</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The vPE Configuration table is not zero, and contains live data.</td>
</tr>
<tr>
<td>0b1</td>
<td>The vPE Configuration table is zero.</td>
</tr>
</tbody>
</table>

Setting GICR\_VPROPBASER\_Z to 0 causes the IRI to reload configuration from memory.

When GICR\_VPROPBASER\_Valid is written from 0 to 1, if GICR\_VPROPBASER\_Z==1 behavior is \texttt{UNPREDICTABLE} if the allocated memory does not contain all zeros.

This field is WO, and reads as 0.

**Physical_Address, bits [51:12]**

Bits [51:12] of the physical address containing the LPI Configuration table.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are \texttt{RES0}.

On a Warm reset, this field resets to an \texttt{UNKNOWN} value.

**Shareability, bits [11:10]**

Indicates the Shareability attributes of accesses to the LPI Configuration table. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is \texttt{IMPLEMENTATION DEFINED} whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an \texttt{UNKNOWN} value.

**InnerCache, bits [9:7]**

Indicates the Inner Cacheability attributes of accesses to the LPI Configuration table. The possible values of this field are:
### InnerCache

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate,</td>
</tr>
<tr>
<td></td>
<td>Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to a **UNKNOWN** value.

### Size, bits [6:0]

The number of pages of physical memory allocated to the table, minus one.

**GICR_VPROPBASER.** Page Size specifies the size of each page.

On a Warm reset, this field resets to a **UNKNOWN** value.

### Accessing the GICR_VPROPBASER

**GICR_VPROPBASER** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>VLPI_base</td>
<td>0x0070</td>
<td>GICR_VPROPBASER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `GICD_CTLR.DS == 0` accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICR_VSGIPENDR characteristics are:

**Purpose**

Requests the pending state of virtual SGIs for a specified vPE.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICR_VSGIPENDR are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_VSGIPENDR is a 32-bit register.

**Field descriptions**

The GICR_VSGIPENDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Busy</td>
<td>0b0: Query of virtual SGI state not in progress. 0b1: Query of virtual SGI state in progress.</td>
</tr>
<tr>
<td>30:16</td>
<td>Reserved</td>
<td>RES0</td>
</tr>
<tr>
<td>15:0</td>
<td>Pending</td>
<td>0b0: Query of virtual SGI state not in progress. 0b1: Query of virtual SGI state in progress.</td>
</tr>
</tbody>
</table>

**Bits [30:16]**

Reserved, RES0.

**Pending, bits [15:0]**

Pending state of virtual SGIs for requested vPEID.

This field is **UNKNOWN** when GICR_VSGIPENDR.Busy == 1

**Accessing the GICR_VSGIPENDR**

64-bit access only.

**GICR_VSGIPENDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>VLPI_base</td>
<td>0x0088</td>
<td>GICR_VSGIPENDR</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTRLS.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
The GICR_VSGIR characteristics are:

**Purpose**

Requests the pending state of virtual SGIs for a specified vPE.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GICR_VSGIR are RES0.

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_VSGIR is a 32-bit register.

**Field descriptions**

The GICR_VSGIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>vPEID</td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
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<td>23</td>
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<td>22</td>
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<td>19</td>
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<td>17</td>
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<td>16</td>
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<td>11</td>
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<td>10</td>
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<td>9</td>
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<td>8</td>
<td></td>
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<td>7</td>
<td></td>
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<tr>
<td>6</td>
<td></td>
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<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**vPEID, bits [15:0]**

ID of target vPE

Writing this field is **CONSTRAINED UNPREDICTABLE** when GICR_VSGIPENDR.Busy == 1, with either the write ignored or a new query started.

Writing a value greater than the configured vPEID width behaviour is **CONSTRAINED UNPREDICTABLE**:

- GICR_VPENDBASER.vPEID is treated as having an **UNKNOWN** valid value for all purposes other than a direct read of the register.
- GICR_VPENDBASER.Valid is treated as being set to 0 for all purposes other than a direct read of the register.

The size of this field is **IMPLEMENTATION DEFINED**, and is specified by the GICD_TYPER2.VIL and GICD_TYPER2.VID fields. Unimplemented bits are RES0.

**Accessing the GICR_VSGIR**

64-bit access only.

**GICR_VSGIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

Page 3848
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
The GICR_WAKER characteristics are:

**Purpose**

Permits software to control the behavior of the WakeRequest power management signal corresponding to the Redistributor. Power management operations follow the rules in 'Power management' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Configuration**

A copy of this register is provided for each Redistributor.

**Attributes**

GICR_WAKER is a 32-bit register.

**Field descriptions**

The GICR_WAKER bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
<td>Reserved. Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td>ChildrenAsleep</td>
<td>Read-only. Indicates whether the connected PE is quiescent:</td>
</tr>
<tr>
<td>1</td>
<td>ProcessorSleep</td>
<td>Indicates whether the Redistributor can assert the WakeRequest signal:</td>
</tr>
<tr>
<td>0</td>
<td>IMPLEMENTATION DEFINED</td>
<td></td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 1.
<table>
<thead>
<tr>
<th>ProcessorSleep</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This PE is not in, and is not entering, a low power state.</td>
</tr>
</tbody>
</table>
| 0b1           | The PE is either in, or is in the process of entering, a low power state. All interrupts that arrive at the Redistributor:  
  • Assert a **WakeRequest** signal.  
  • Are held in the pending state at the Redistributor, and are not communicated to the CPU interface. |

**Note**
When ProcessorSleep == 1, the Redistributor must ensure that any interrupts that are pending on the CPU interface are released.

For an implementation that is using the GIC Stream Protocol Interface:
• A Quiesce command puts the interface between the Redistributor and the CPU interface in a quiescent state. For more information, see ‘Quiesce (IRI)’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).
• A Release command releases any interrupts that are pending on the CPU interface. For more information, see ‘Release (ICC)’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**Note**
Before powering down a PE, software must set this bit to 1 and wait until ChildrenAsleep == 1. After powering up a PE, or following a failed powerdown, software must set this bit to 0 and wait until ChildrenAsleep == 0.

Changing ProcessorSleep from 1 to 0 when ChildrenAsleep is not 1 results in **UNPREDICTABLE** behavior.

Changing ProcessorSleep from 0 to 1 when the Enable for each interrupt group in the associated CPU interface is not 0 results in **UNPREDICTABLE** behavior.

On a Warm reset, this field resets to 1.

**IMPLEMENTATION DEFINED, bit [0]**

IMPLEMENTATION DEFINED.

**Accessing the GICR_WAKER**

When **GICD_CTLR**.DS==1, this register is always accessible.

When **GICD_CTLR**.DS==0, this is a Secure register. This register is RAZ/WI to Non-secure accesses.

To ensure a Redistributor is quiescent, software must write to GICR_WAKER with ProcessorSleep == 1, then poll the register until ChildrenAsleep == 1.

Resetting the connected PE when GICR_WAKER.ProcessorSleep==0 or GICR_WAKER.ChildrenAsleep==0, can lead to **UNPREDICTABLE** behaviour in the IRI.

Resetting the IRI when GICR_WAKER.ProcessorSleep==0 or GICR_WAKER.ChildrenAsleep==0 can lead to **UNPREDICTABLE** behaviour in the connected PE.
GICR_WAKER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Redistributor</td>
<td>RD_base</td>
<td>0x0014</td>
<td>GICR_WAKER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
GICV_ABPR, Virtual Machine Aliased Binary Point Register

The GICV_ABPR characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 1 interrupt preemption.

This register corresponds to **GICC_ABPR** in the physical CPU interface.

**Note**

**GICH_LR<n>** Group determines whether a virtual interrupt is Group 0 or Group 1.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_ABPR is a 32-bit register.

**Field descriptions**

The GICV_ABPR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|---|
| RES0 | Binary_Point |

**Bits [31:3]**

Reserved, RES0.

**Binary_Point, bits [2:0]**

Controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field.

For information about how this field determines the interrupt priority bits assigned to the group priority field, see 'Priority grouping' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to 0.

The Binary_Point field of this register is aliased to **GICH_VMCR.VBPR1**.

**Accessing the GICV_ABPR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, **ICC_BPR1** provides equivalent functionality.
- For AArch64 implementations, **ICC_BPR1_EL1** provides equivalent functionality.
The value contained in this register is one greater than the actual applied binary point value, as described in 'Priority grouping' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This register is used for Group 1 interrupts when \texttt{GIC\_CTLR.CBPR} == 0. \texttt{GIC\_BPR} provides equivalent functionality for Group 0 interrupts, and for Group 1 interrupts when \texttt{GIC\_CTLR.CBPR} == 1.

\textbf{GICV\_ABPR can be accessed through the memory-mapped interfaces:}

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x001C</td>
<td>GIC_ABPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When \texttt{GIC\_D\_DS} == 0 accesses to this register are \textbf{RW}.
- When an access is Secure accesses to this register are \textbf{RW}.
- When an access is Non-secure accesses to this register are \textbf{RW}.
GICV_AEOIR, Virtual Machine Aliased End Of Interrupt Register

The GICV_AEOIR characteristics are:

**Purpose**

A write to this register performs a priority drop for the specified Group 1 virtual interrupt and, if GICV_CTLR.EOImode == 0, also deactivates the interrupt.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_AEOIR is a 32-bit register.

**Field descriptions**

The GICV_AEOIR bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|--------|
| RES0   | INTID  |

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

---

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

A successful EOI request means that:

- The highest priority bit in GICV_APR<\text{n}> is cleared, causing the running priority to drop.
- If the appropriate GICV_CTLR EOImode bit == 0, the interrupt is deactivated in the corresponding List register. If the INTID corresponds to a hardware interrupt, the interrupt is also deactivated in the Distributor.

---

**Note**

Only Group 1 interrupts can target the hypervisor, and therefore only Group 1 interrupts are deactivated in the Distributor.
A write to this register is **UNPREDICTABLE** if the INTID corresponds to a Group 0 interrupt. In addition, the following GICv2 **UNPREDICTABLE** cases require specific actions:

- If highest active priority is Group 0 and the identified interrupt is in the List Registers and it matches the highest active priority. When EL2 is using System registers and `ICH_VTR_EL2.SEIS` is 1, an **IMPLEMENTATION DEFINED** SEI might be generated, otherwise GICv3 implementations must ignore such writes.
- If the identified interrupt is in the List Registers, and the HW bit is 1, and the interrupt to be deactivated is an SGI (that is, the value of Physical ID is between 0 and 15). GICv3 implementations must perform the deactivate operation. This means that a GICv3 implementation in legacy operation must ensure only a single SGI is active for a PE.
- If the identified interrupt is in the List Registers, and the HW bit is 1, and the corresponding pINTID field value is between 1020 and 1023, indicating a special purpose INTID. GICv3 implementations must not perform a deactivate operation but must still change the state of the List register as appropriate. When EL2 is using System registers and `ICH_VTR_EL2.SEIS` is 1, an implementation might generate a system error.

### Accessing the GICV_AEOIR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICC_EOIR1` provides equivalent functionality.
- For AArch64 implementations, `ICC_EOIR1_EL1` provides equivalent functionality.

This register is used for Group 1 interrupts only. `GICV_EOIR` provides equivalent functionality for Group 0 interrupts.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

### GICV_AEOIR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0024</td>
<td>GICV_AEOIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `GICD_CTLR.DS == 0` accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
The GICV_AHPPIR characteristics are:

**Purpose**

Provides the INTID of the highest priority pending Group 1 virtual interrupt in the List registers.

This register corresponds to the physical CPU interface register GICC_AHPPIR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_AHPPIR is a 32-bit register.

**Field descriptions**

The GICV_AHPPIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |       |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | INTID |

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

A read of this register returns the spurious INTID 1023 if any of the following are true:

- There are no pending interrupts of sufficiently high priority value to be signaled to the PE.
- The highest priority pending interrupt is in Group 0.

**Accessing the GICV_AHPPIR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_HPPIR1 provides equivalent functionality.
- For AArch64 implementations, ICC_HPPIR1_EL1 provides equivalent functionality.
This register is used for Group 1 interrupts only. **GICV_HPPIR** provides equivalent functionality for Group 0 interrupts.

The register does not return the INTID of an interrupt that is active and pending.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

**GICV_AHPPIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0028</td>
<td>GICV_AHPPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
GICV_AIAR, Virtual Machine Aliased Interrupt Acknowledge Register

The GICV_AIAR characteristics are:

**Purpose**

Provides the INTID of the signaled Group 1 virtual interrupt. A read of this register by the PE acts as an acknowledge for the interrupt.

This register corresponds to the physical CPU interface register **GICC_AIAR**.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_AIAR is a 32-bit register.

**Field descriptions**

The GICV_AIAR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>INTID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

The operation of this register is similar to the operation of **GICV_IAR**. When a vPE reads this register, the corresponding **GICH_LR<n>**.Group field is checked to determine whether the interrupt is in Group 0 or Group 1:

- If the interrupt is Group 0, the spurious INTID 1023 is returned and the interrupt is not acknowledged.
- If the interrupt is Group 1, the INTID is returned. The List register entry is updated to active state, and the appropriate bit in **GICH_APR<n>** is set to 1.

A read of this register returns the spurious INTID 1023 if any of the following are true:

- When the virtual CPU interface is enabled and **GICH_HCR.En == 1**:
  - There are no pending interrupts of sufficiently high priority value to be signaled to the PE.
The highest priority pending interrupt is in Group 0.

- Interrupt signaling by the virtual CPU interface is disabled.

**Accessing the GICV_AIAR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_IAR1 provides equivalent functionality.
- For AArch64 implementations, ICC_IAR1_EL1 provides equivalent functionality.

This register is used for Group 1 interrupts only. GICV_IAR provides equivalent functionality for Group 0 interrupts.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

**GICV_AIAR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x0020</td>
<td>GICV_AIAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
GICV_APR<n>, Virtual Machine Active Priorities Registers, n = 0 - 3

The GICV_APR<n> characteristics are:

**Purpose**

Provides information about interrupt active priorities.

These registers correspond to the physical CPU interface registers GICC_APR<n>.

**Configuration**

When System register access is disabled for EL2, these registers access GICH_APR<n>, and all active priorities for virtual machines are held in GICH_APR<n> regardless of interrupt group.

When System register access is enabled for EL2, these registers access ICH_AP1R<n>_EL2, and all active priorities for virtual machines are held in ICH_AP1R<n>_EL2 regardless of interrupt group.

**Attributes**

GICV_APR<n> is a 32-bit register.

**Field descriptions**

The GICV_APR<n> bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P31</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P30</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P29</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P28</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P27</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P26</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P25</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P24</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P23</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P22</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P21</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P20</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P19</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P18</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P17</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P16</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P15</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P14</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P13</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P12</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P11</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P10</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P9</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P8</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P7</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P6</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P5</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P4</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P3</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P2</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P1</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
<tr>
<td>P0</td>
<td>Provide information about active priorities for the virtual machine.</td>
</tr>
</tbody>
</table>

P<x>, bit [x], for x = 31 to 0

Provides information about active priorities for the virtual machine.

See GICH_APR<n> and ICH_AP1R<n>_EL2 for the correspondence between priorities and bits.

**Accessing the GICV_APR<n>**

If System register access is not enabled for EL2, these registers access GICH_APR<n>. If System register access is enabled for EL2, these registers access ICH_AP1R<n>_EL2. All active priority mapped guests are held in the accessed registers, regardless of interrupt group.

GICV_APR<n> can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x00D0 + (4 * n)</td>
<td>GICV_APR&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GICV_BPR characteristics are:

**Purpose**

Defines the point at which the priority value fields split into two parts, the group priority field and the subpriority field. The group priority field determines Group 0 interrupt preemption.

This register corresponds to **GICC_BPR** in the physical CPU interface.

**Note**

**GICH_LR<<n>>** Group determines whether a virtual interrupt is Group 0 or Group 1.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

When **GICV_CTLR**.CBPR == 1, this register determines interrupt preemption for both Group 0 and Group 1 interrupts.

**Attributes**

GICV_BPR is a 32-bit register.

**Field descriptions**

The GICV_BPR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Binary_Point |

**Bits [31:3]**

Reserved, RES0.

**Binary_Point, bits [2:0]**

Controls how the 8-bit interrupt priority field is split into a group priority field, that determines interrupt preemption, and a subpriority field.

For information about how this field determines the interrupt priority bits assigned to the group priority field, see 'ICC_BPR0_EL1 Binary Point for Group 1 interrupts when CBPR == 1, or for Group 0 interrupts' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

The Binary_Point field of this register is aliased to **GICH_VMCR**.VBPR0.

**Accessing the GICV_BPR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, **ICC_BPR0** provides equivalent functionality.
- For AArch64 implementations, **ICC_BPR0_EL1** provides equivalent functionality.
**GICV_BPR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0008</td>
<td>GICV_BPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.

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GICV_CTLR, Virtual Machine Control Register

The GICV_CTLR characteristics are:

**Purpose**

Controls the behavior of virtual interrupts.

This register corresponds to the physical CPU interface register `GICC_CTLR`.

**Configuration**

This register is available when a GIC implementation supports interrupt virtualization.

**Attributes**

GICV_CTLR is a 32-bit register.

**Field descriptions**

The GICV_CTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-10</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>9</td>
<td>EOImode</td>
</tr>
<tr>
<td>8-5</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>4</td>
<td>CBPR</td>
</tr>
<tr>
<td>3</td>
<td>FIQEn</td>
</tr>
<tr>
<td>2</td>
<td>AckCtl</td>
</tr>
<tr>
<td>1</td>
<td>EnableGrp1</td>
</tr>
<tr>
<td>0</td>
<td>EnableGrp0</td>
</tr>
</tbody>
</table>

**Bits [31:10]**

Reserved, RES0.

**EOImode, bit [9]**

Controls the behavior associated with the `GICV_EOIR`, `GICV_AEOIR`, and `GICV_DIR` registers:

<table>
<thead>
<tr>
<th>EOImode</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Writes to <code>GICV_EOIR</code> and <code>GICV_AEOIR</code> perform priority drop and deactivate interrupt operations simultaneously. Behavior on a write to <code>GICV_DIR</code> is unpredictable. When it has completed processing the interrupt, the virtual machine writes to <code>GICV_EOIR</code> or <code>GICV_AEOIR</code> to deactivate the interrupt. The write updates the List registers and causes the virtual CPU interface to signal the interrupt completion to the physical Distributor.</td>
</tr>
<tr>
<td>0b1</td>
<td>Writes to <code>GICV_EOIR</code> and <code>GICV_AEOIR</code> perform priority drop operation only. Writes to <code>GICV_DIR</code> perform deactivate interrupt operation only. When it has completed processing the interrupt, the virtual machine writes to <code>GICV_DIR</code> to deactivate the interrupt. The write updates the List registers and causes the virtual CPU interface to signal the interrupt completion to the Distributor.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [8:5]**

Reserved, RES0.
CBPR, bit [4]

Controls whether GICV_BPR affects both Group 0 and Group 1 interrupts:

<table>
<thead>
<tr>
<th>CBPR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GICV_BPR affects Group 0 virtual interrupts only.</td>
</tr>
<tr>
<td>0b1</td>
<td>GICV_BPR affects both Group 0 and Group 1 virtual interrupts.</td>
</tr>
</tbody>
</table>

For more information, see 'Priority grouping' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

FIQEn, bit [3]

FIQ Enable. Controls whether Group 0 virtual interrupts are presented as virtual FIQs:

<table>
<thead>
<tr>
<th>FIQEn</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Group 0 virtual interrupts are presented as virtual IRQs.</td>
</tr>
<tr>
<td>0b1</td>
<td>Group 0 virtual interrupts are presented as virtual FIQs.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

AckCtl, bit [2]

Arm deprecates use of this bit. Arm strongly recommends that software is written to operate with this bit always cleared to 0.

Acknowledge control. When the highest priority interrupt is Group 1, determines whether GICV_IAR causes the CPU interface to acknowledge the interrupt or returns the spurious identifier 1022, and whether GICV_HPPIR returns the interrupt ID or the special identifier 1022.

<table>
<thead>
<tr>
<th>AckCtl</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns an interrupt ID of 1022.</td>
</tr>
<tr>
<td>0b1</td>
<td>If the highest priority pending interrupt is Group 1, a read of GICV_IAR or GICV_HPPIR returns the interrupt ID of the corresponding interrupt.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EnableGrp1, bit [1]

Enables the signaling of Group 1 virtual interrupts by the virtual CPU interface to the virtual machine:

<table>
<thead>
<tr>
<th>EnableGrp1</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Signaling of Group 1 interrupts is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Signaling of Group 1 interrupts is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

EnableGrp0, bit [0]

Enables the signaling of Group 0 virtual interrupts by the virtual CPU interface to the virtual machine:

<table>
<thead>
<tr>
<th>EnableGrp0</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Signaling of Group 0 interrupts is disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>Signaling of Group 0 interrupts is enabled.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the GICV_CTLR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_CTLR provides equivalent functionality.
- For AArch64 implementations, ICC_CTLR_EL1 provides equivalent functionality.

**GICV_CTLR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0000</td>
<td>GICV_CTLR</td>
</tr>
<tr>
<td>interface</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GICV_DIR characteristics are:

**Purpose**

Deactivates a specified virtual interrupt in the \texttt{GICH\_LR<n>} List registers.

This register corresponds to the physical CPU interface register \texttt{GICC\_DIR}.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_DIR is a 32-bit register.

**Field descriptions**

The GICV_DIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTID |

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

When the virtual machine writes to this register, the specified interrupt in the List registers is changed from active to inactive, or from active and pending to pending. If the specified interrupt is present in the List registers but is not in either the active or active and pending states, the effect is \texttt{UNPREDICTABLE}. If the specified interrupt is not present in the List registers, \texttt{GICH\_HCR} EOICount is incremented, potentially generating a maintenance interrupt.

**Note**

If the specified interrupt is not present in the List registers, the virtual machine cannot recover the INTID. Therefore, the hypervisor must ensure that, when \texttt{GICV\_CTLR} EOImode == 1, no more than one active interrupt is transferred from the List registers into a software list. If more than one active
interrupt that is not stored in the List registers exists, the hypervisor must handle accesses to GICV_DIR in software, typically by trapping these accesses.

If the corresponding GICH_LR<n>.HW == 1, indicating a hardware interrupt, then a deactivate request is sent to the physical Distributor, identifying the physical INTID from the corresponding field in the List register. This effect is identical to a Non-secure write to GICC_DIR from the PE having that physical INTID. This means that if the corresponding physical interrupt is marked as Group 0, the request is ignored.

**Note**

Interrupt deactivation using this register is based on the provided INTID, with no requirement to deactivate interrupts in any particular order. A single register is therefore used to deactivate both Group 0 and Group 1 interrupts.

**Accessing the GICV_DIR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_DIR provides equivalent functionality.
- For AArch64 implementations, ICC_DIR_EL1 provides equivalent functionality.

Writes to this register are valid only when GICV_CTLR.EOImode == 1. Writes to this register are otherwise UNPREDICTABLE.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

**GICV_DIR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x1000</td>
<td>GICV_DIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
GICV_EOIR, Virtual Machine End Of Interrupt Register

The GICV_EOIR characteristics are:

**Purpose**

A write to this register performs a priority drop for the specified Group 0 virtual interrupt and, if GICV_CTLR.EOImode == 0, also deactivates the interrupt.

This register corresponds to the physical CPU interface register GICC_EOIR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_EOIR is a 32-bit register.

**Field descriptions**

The GICV_EOIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>INTID</td>
</tr>
</tbody>
</table>

- **Bits [31:25]**
  - Reserved, RES0.

- **INTID, bits [24:0]**
  - The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

The behavior of this register depends on the setting of GICV_CTLR.EOImode:

<table>
<thead>
<tr>
<th>GICV_CTLR.EOImode</th>
<th>Behavior</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Both the priority drop and the deactivate interrupt effects occur</td>
</tr>
<tr>
<td>0b1</td>
<td>Only the priority drop effect occurs.</td>
</tr>
</tbody>
</table>

A successful EOI request means that:

- The highest priority bit in GICH_APR<n> is cleared, causing the running priority to drop.
- If the appropriate GICV_CTLR.EOImode bit == 0, the interrupt is deactivated in the corresponding List register GICH_LR<n>. If GICH_LR<n>.HW == 1, indicating the INTID corresponds to a hardware interrupt, a deactivate request is also sent to the physical Distributor, identifying the physical INTID from the
corresponding field in the List register. This effect is identical to a Non-secure write to GICC_DIR from the PE having that physical INTID. This means that if the corresponding physical interrupt is marked as Group 0, and GICD_CTLR.DS == 0, the deactivation request is ignored. See GICC_EOIR for more information.

Note

Only Group 1 interrupts can target the hypervisor, and therefore only Group 1 interrupts are deactivated in the Distributor.

Accessing the GICV_EOIR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_EOIR0 provides equivalent functionality.
- For AArch64 implementations, ICC_EOIR0_EL1 provides equivalent functionality.

This register is used for Group 0 interrupts only. GICV_AEOIR provides equivalent functionality for Group 1 interrupts.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

GICV_EOIR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0010</td>
<td>GICV_EOIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are WO.
- When an access is Secure accesses to this register are WO.
- When an access is Non-secure accesses to this register are WO.
GICV_HPPIR, Virtual Machine Highest Priority Pending Interrupt Register

The GICV_HPPIR characteristics are:

**Purpose**

Provides the INTID of the highest priority pending Group 0 virtual interrupt in the List registers.

This register corresponds to the physical CPU interface register GICC_HPPIR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_HPPIR is a 32-bit register.

**Field descriptions**

The GICV_HPPIR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  | INTID |

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

Reads of the GICC_HPPIR that do not return a valid INTID return a spurious INTID, 1022 or 1023. See 'Special INTIDs' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).
<table>
<thead>
<tr>
<th>Highest priority pending interrupt Group</th>
<th>GICV_HPPIR read</th>
<th>GICV_CTLR.AckCtl</th>
<th>Returned INTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Non-secure</td>
<td>x</td>
<td>ID of Group 1 interrupt 1022</td>
</tr>
<tr>
<td>1</td>
<td>Secure</td>
<td>0</td>
<td>ID of Group 1 interrupt 1022</td>
</tr>
<tr>
<td>1</td>
<td>Secure</td>
<td>1</td>
<td>ID of Group 1 interrupt 1022</td>
</tr>
<tr>
<td>0</td>
<td>Non-secure</td>
<td>x</td>
<td>ID of Group 0 interrupt 1023</td>
</tr>
<tr>
<td>0</td>
<td>Secure</td>
<td>x</td>
<td>ID of Group 0 interrupt 1023</td>
</tr>
<tr>
<td>No pending interrupts</td>
<td>x</td>
<td>x</td>
<td>1023</td>
</tr>
</tbody>
</table>

If the CPU interface supports only a single Security state, the entries that apply to Secure reads describe the behavior.

## Accessing the GICV_HPPIR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_HPPIR0 provides equivalent functionality.
- For AArch64 implementations, ICC_HPPIR0_EL1 provides equivalent functionality.

This register is used for Group 0 interrupts only. GICV_AHPPIR provides equivalent functionality for Group 1 interrupts.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

### GICV_HPPIR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x0018</td>
<td>GICV_HPPIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GICV_IAR, Virtual Machine Interrupt Acknowledge Register

The GICV_IAR characteristics are:

**Purpose**

Provides the INTID of the signaled Group 0 virtual interrupt. A read of this register by the PE acts as an acknowledge for the interrupt.

This register corresponds to the physical CPU interface register GICC_IAR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_IAR is a 32-bit register.

**Field descriptions**

The GICV_IAR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-25</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24-0</td>
<td>INTID</td>
</tr>
</tbody>
</table>

**Bits [31:25]**

Reserved, RES0.

**INTID, bits [24:0]**

The INTID of the signaled interrupt.

**Note**

INTIDs 1020-1023 are reserved and convey additional information such as spurious interrupts.

When affinity routing is not enabled:

- Bits [23:13] are RES0.
- For SGIs, bits [12:10] identify the CPU interface corresponding to the source PE. For all other interrupts these bits are RES0.

When the virtual machine writes to this register, the virtual CPU interface acknowledges the highest priority pending virtual interrupt and sets the state in the corresponding List register to active. The appropriate bit in the active priorities register GICH_APR<n> is set to 1.

If GICV_LR<n>.HW == 0, indicating that the interrupt is software-triggered, then bits [12:10] of GICV_LR<n> are returned in bits [12:10] of GICV_IAR. Otherwise bits [12:10] are RES0.

A read of this register returns the spurious INTID 1023 if either of the following is true:

- There are no pending interrupts of sufficiently high priority value to be signaled to the PE with the virtual CPU interface enabled and GICH_HCR.En == 1.
Interrupt signaling by the virtual CPU interface is disabled.

A read of this register returns the spurious INTID 1022 if the highest priority pending interrupt is Group 1 and `GICV_CTLR.AckCtl == 0`.

### Accessing the GICV_IAR

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, `ICC_IAR0` provides equivalent functionality.
- For AArch64 implementations, `ICC_IAR0_EL1` provides equivalent functionality.

This register is used for Group 0 interrupts only. `GICV_AIAR` provides equivalent functionality for Group 1 interrupts.

When affinity routing is enabled, it is a programming error to use memory-mapped registers to access the GIC.

#### GICV_IAR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x000C</td>
<td>GICV_IAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `GICD_CTLR.DS == 0` accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.

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GICV_IIDR, Virtual Machine CPU Interface Identification Register

The GICV_IIDR characteristics are:

**Purpose**

Provides information about the implementer and revision of the virtual CPU interface.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states this register is Common.

**Attributes**

GICV_IIDR is a 32-bit register.

**Field descriptions**

The GICV_IIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit Position</th>
<th>Bit assignments</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-20</td>
<td>ProductID</td>
<td>An IMPLEMENTATION DEFINED product identifier.</td>
</tr>
<tr>
<td>19-16</td>
<td>Architecture_version</td>
<td>The version of the GIC architecture that is implemented.</td>
</tr>
<tr>
<td>15-12</td>
<td>Revision</td>
<td>An IMPLEMENTATION DEFINED revision number for the CPU interface.</td>
</tr>
<tr>
<td>11-0</td>
<td>Implementer</td>
<td>Contains the JEP106 code of the company that implemented the CPU interface.</td>
</tr>
</tbody>
</table>

- **ProductID**, bits [31:20]
  - An IMPLEMENTATION DEFINED product identifier.

- **Architecture_version**, bits [19:16]
  - The version of the GIC architecture that is implemented.
    - **0b0001**: GICv1.
    - **0b0010**: GICv2.
    - **0b0011**: GICv3 memory-mapped interface supported. Support for the System register interface is discoverable from PE registers ID_PFR1 and ID_AA64PFR0_EL1.
    - **0b0100**: GICv4 memory-mapped interface supported. Support for the System register interface is discoverable from PE registers ID_PFR1 and ID_AA64PFR0_EL1.
    - Other values are reserved.

- **Revision**, bits [15:12]
  - An IMPLEMENTATION DEFINED revision number for the CPU interface.

- **Implementer**, bits [11:0]
  - Contains the JEP106 code of the company that implemented the CPU interface.
    - Bits [11:8] are the JEP106 continuation code of the implementer. For an Arm implementation, this field is 0x4.
- Bit [7] is always 0.
- Bits [6:0] are the JEP106 identity code of the implementer. For an Arm implementation, bits [7:0] are therefore 0x3B.

## Accessing the GICV_IIDR

**GICV_IIDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x00FC</td>
<td>GICV_IIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.

---

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GICV_PMR, Virtual Machine Priority Mask Register

The GICV_PMR characteristics are:

**Purpose**

This register provides a virtual interrupt priority filter. Only virtual interrupts with a higher priority than the value in this register are signaled to the PE.

**Note**

Higher interrupt priority corresponds to a lower value of the Priority field.

This register corresponds to the physical CPU interface register GICC_PMR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

The Priority field of this register is aliased to GICH_VMCR.VMPR, to enable state to be switched easily between virtual machines during context-switching.

**Attributes**

GICV_PMR is a 32-bit register.

**Field descriptions**

The GICV_PMR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Priority |

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The priority mask level for the virtual CPU interface. If the priority of the interrupt is higher than the value indicated by this field, the interface signals the interrupt to the PE.

If the GIC implementation supports fewer than 256 priority levels some bits might be RAZ/WI, as follows:

- For 128 supported levels, bit [0] = 0b0.
- For 64 supported levels, bits [1:0] = 0b00.
- For 32 supported levels, bits [2:0] = 0b000.
- For 16 supported levels, bits [3:0] = 0b0000.

For more information, see 'Interrupt prioritization' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the GICV_PMR**

This register is used only when System register access is not enabled. When System register access is enabled:
For AArch32 implementations, ICC_PMR provides equivalent functionality.
For AArch64 implementations, ICC_PMR_EL1 provides equivalent functionality.

**GICV_PMR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x0004</td>
<td>GICV_PMR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GICV_RPR, Virtual Machine Running Priority Register

The GICV_RPR characteristics are:

**Purpose**

This register indicates the running priority of the virtual CPU interface.

This register corresponds to the physical CPU interface register GICC_RPR.

**Configuration**

This register is available when the GIC implementation supports interrupt virtualization.

**Attributes**

GICV_RPR is a 32-bit register.

**Field descriptions**

The GICV_RPR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
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<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
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<tr>
<td>18</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>Priority</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**Priority, bits [7:0]**

The current running priority on the virtual CPU interface. This is the group priority of the current active interrupt.

If there are no active interrupts on the CPU interface, or all active interrupts have undergone a priority drop, the value returned is the Idle priority.

The priority returned is the group priority as if the BPR was set to the minimum value.

**Accessing the GICV_RPR**

This register is used only when System register access is not enabled. When System register access is enabled:

- For AArch32 implementations, ICC_RPR provides equivalent functionality.
- For AArch64 implementations, ICC_RPR_EL1 provides equivalent functionality.

Depending on the implementation, if no bits are set to 1 in GICH_APR<n>, indicating no active virtual interrupts in the virtual CPU interface, the priority reads as 0xFF or 0xF8 to reflect the number of supported interrupt priority bits defined by GICH_VTR_PRIbits.

**GICV_RPR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU</td>
<td>0x0014</td>
<td>GICV_RPR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:
• When GICD_CTLR.DS == 0 accesses to this register are **RO**.
• When an access is Secure accesses to this register are **RO**.
• When an access is Non-secure accesses to this register are **RO**.
GICV_STATUSR, Virtual Machine Error Reporting Status Register

The GICV_STATUSR characteristics are:

**Purpose**

Provides software with a mechanism to detect:

- Accesses to reserved locations.
- Writes to read-only locations.
- Reads of write-only locations.

**Configuration**

In systems where this register is implemented, Arm expects that when a virtual machine is scheduled, the hypervisor ensures that this register is cleared to 0. The hypervisor might check for illegal accesses when the virtual machine is unscheduled.

**Attributes**

GICV_STATUSR is a 32-bit register.

**Field descriptions**

The GICV_STATUSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>WROD</td>
</tr>
<tr>
<td>29</td>
<td>RWOD</td>
</tr>
<tr>
<td>28</td>
<td>WRD</td>
</tr>
<tr>
<td>27</td>
<td>RRD</td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, RES0.

**WROD, bit [3]**

Write to an RO location.

<table>
<thead>
<tr>
<th>WROD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to an RO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**RWOD, bit [2]**

Read of a WO location.

<table>
<thead>
<tr>
<th>RWOD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a WO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.
WRD, bit [1]

Write to a reserved location.

<table>
<thead>
<tr>
<th>WRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

RRD, bit [0]

Read of a reserved location.

<table>
<thead>
<tr>
<th>RRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**Accessing the GICV_STATUSR**

This is an optional register. If the register is implemented, GICC_STATUSR must also be implemented. If the register is not implemented, the location is RAZ/WI.

This register is used only when System register access is not enabled. If System register access is enabled, this register is not updated. Equivalent function might be provided by appropriate traps and exceptions.

**GICV_STATUSR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC Virtual CPU interface</td>
<td>0x002C</td>
<td>GICV_STATUSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The GITS_BASER<n> characteristics are:

**Purpose**

Specifies the base address and size of the ITS translation tables.

**Configuration**

A copy of this register is provided for each ITS translation table.

Bits [63:32] and bits [31:0] are accessible independently.

A maximum of 8 GITS_BASER<n> registers can be provided. Unimplemented registers are RES0.

When GITS_CTLR.Enabled == 1 or GITS_CTLR.Quiescent == 0, writing this register is UNPREDICTABLE.

**Attributes**

GITS_BASER<n> is a 64-bit register.

**Field descriptions**

The GITS_BASER<n> bit assignments are:

<table>
<thead>
<tr>
<th>Valid</th>
<th>Indirect</th>
<th>InnerCache</th>
<th>Type</th>
<th>OuterCache</th>
<th>Entry_Size</th>
<th>Physical_Address</th>
<th>Shareability</th>
<th>Page_Size</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
</tr>
<tr>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td>45</td>
<td>44</td>
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<tr>
<td>43</td>
<td>42</td>
<td>41</td>
<td>40</td>
<td>39</td>
<td>38</td>
<td>37</td>
<td>36</td>
<td>35</td>
<td>34</td>
</tr>
<tr>
<td>33</td>
<td>32</td>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
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<tr>
<td>23</td>
<td>22</td>
<td>21</td>
<td>20</td>
<td>19</td>
<td>18</td>
<td>17</td>
<td>16</td>
<td>15</td>
<td>14</td>
</tr>
<tr>
<td>13</td>
<td>12</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Valid, bit [63]**

Indicates whether software has allocated memory for the translation table:

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No memory is allocated for the translation table. The ITS discards any writes to the interrupt translation page when either:</td>
</tr>
<tr>
<td></td>
<td>• GITS_BASER&lt;n&gt;.Type specifies any valid table entry type other than interrupt collections, that is, any value other than 0b100.</td>
</tr>
<tr>
<td></td>
<td>• GITS_BASER&lt;n&gt;.Type specifies an interrupt collection and GITS_TYPER.HCC == 0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Memory is allocated to the translation table.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

**Indirect, bit [62]**

This field indicates whether an implemented register specifies a single, flat table or a two-level table where the first level contains a list of descriptors.
**Indirect**

<table>
<thead>
<tr>
<th></th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Single Level. The Size field indicates the number of pages used by the ITS to store data associated with each table entry.</td>
</tr>
<tr>
<td>0b1</td>
<td>Two Level. The Size field indicates the number of pages which contain an array of 64-bit descriptors to pages that are used to store the data associated with each table entry. A little endian memory order model is used.</td>
</tr>
</tbody>
</table>

For more information, see ‘The ITS tables’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

This field is RAZ/WI for GIC implementations that only support flat tables. If the maximum width of the scaling factor that is identified by GITS_BASER<n>.Type and the smallest page size that is supported result in a single level table that requires multiple pages, then implementing this bit as RAZ/WI is DEPRECATED.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**InnerCache, bits [61:59]**

Indicates the Inner Cacheability attributes of accesses to the table. The possible values of this field are:

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Type, bits [58:56]**

Read only. Specifies the type of entity that requires entries in the corresponding translation table. The possible values of the field are:

<table>
<thead>
<tr>
<th>Type</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Unimplemented. This register does not correspond to a translation table.</td>
</tr>
<tr>
<td>0b01</td>
<td>Devices. This register corresponds to a translation table that scales with the width of the DeviceID. Only a single GITS_BASER&lt;n&gt; register reports this type.</td>
</tr>
<tr>
<td>0b10</td>
<td>vPEs. FEAT_GICv4 only. This register corresponds to a translation table that scales with the number of vPEs in the system. The translation table requires (ENTRY_SIZE * N) bytes of memory, where N is the number of vPEs in the system. Only a single GITS_BASER&lt;n&gt; register reports this type.</td>
</tr>
<tr>
<td>0b100</td>
<td>Interrupt collections. This register corresponds to a translation table that scales with the number of interrupt collections in the system. The translation table requires (ENTRY_SIZE * N) bytes of memory, where N is the number of interrupt collections. Not more than one GITS_BASER&lt;n&gt; register will report this type.</td>
</tr>
</tbody>
</table>

Other values are reserved.

For FEAT_GICv4p1, the registers are allocated as follows:

- GITS_BASER0.Type is 0b001 (Device).
- GITS_BASER1.Type is either 0b100 (Collection Table) or 0b000 (Unimplemented).
- GITS_BASER2.Type is either 0b010 (vPE) or 0b000 (Unimplemented).
- GITS_BASER<n>.Type, where 'n' is in the range 3 to 7, is 0b000 (Unimplemented).
For FEAT_GICv3, FEAT_GICv3p1, and FEAT_GICv4, Arm recommends that the GITS_BASER<n> use the same allocations.

Other allocations of Type values are deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**OuterCache, bits [55:53]**

Indicates the Outer Cacheability attributes of accesses to the table. The possible values of this field are:

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Entry_Size, bits [52:48]**

Read-only. Specifies the number of bytes per translation table entry, minus one.

**Physical_Address, bits [47:12]**

Physical Address. When Page_Size is 4KB or 16KB:

- Bits [51:48] of the base physical address are zero.
- This field provides bits[47:12] of the base physical address of the table.
- Bits[11:0] of the base physical address are zero.
- The address must be aligned to the size specified in the Page Size field. Otherwise the effect is CONSTRAINED UNPREDICTABLE, and can be one of the following:
  - Bits[X:12], where X is derived from the page size, are treated as zero.
  - The value of bits[X:12] are used when calculating the address of a table access.

When Page_Size is 64KB:

- Bits[15:0] of the base physical address are 0.

In implementations that support fewer than 52 bits of physical address, any unimplemented upper bits might be RAZ/WI.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Shareability, bits [11:10]**

Indicates the Shareability attributes of accesses to the table. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>
It is **IMPLEMENTATION DEFINED** whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Page Size, bits [9:8]**

The size of page that the translation table uses:

<table>
<thead>
<tr>
<th>Page Size</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>4KB.</td>
</tr>
<tr>
<td>0b01</td>
<td>16KB.</td>
</tr>
<tr>
<td>0b10</td>
<td>64KB.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b10.</td>
</tr>
</tbody>
</table>

**Note**

If the GIC implementation supports only a single, fixed page size, this field might be RO.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Size, bits [7:0]**

The number of pages of physical memory allocated to the table, minus one. GITS_BASER<n>.Page_Size specifies the size of each page.

If GITS_BASER<n>.Type == 0, this field is RAZ/WI.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the GITS_BASER<n>**

**GITS_BASER<n>** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0100  + (8 * n)</td>
<td>GITS_BASER&lt;n&gt;</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GITS_CBASER, ITS Command Queue Descriptor

The GITS_CBASER characteristics are:

Purpose

Specifies the base address and size of the ITS command queue.

Configuration

Bits [63:32] and bits [31:0] are accessible separately.

Attributes

GITS_CBASER is a 64-bit register.

Field descriptions

The GITS_CBASER bit assignments are:

<table>
<thead>
<tr>
<th>Valid</th>
<th>RES0</th>
<th>InnerCache</th>
<th>RES0</th>
<th>OuterCache</th>
<th>RES0</th>
<th>Physical_Address</th>
<th>Shareability</th>
<th>RES0</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
<td>57</td>
<td>56</td>
<td>55</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>53</td>
<td>52</td>
<td>51</td>
<td>50</td>
<td>49</td>
<td>48</td>
<td>47</td>
<td>46</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td>44</td>
<td>43</td>
<td>42</td>
<td>41</td>
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<td>2</td>
<td>1</td>
<td>0</td>
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<td></td>
</tr>
</tbody>
</table>

Valid, bit [63]

Indicates whether software has allocated memory for the command queue:

<table>
<thead>
<tr>
<th>Valid</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No memory is allocated for the command queue.</td>
</tr>
<tr>
<td>1</td>
<td>Memory is allocated to the command queue.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to 0.

Bit [62]

Reserved, RES0.

InnerCache, bits [61:59]

Indicates the Inner Cacheability attributes of accesses to the command queue. The possible values of this field are:

<table>
<thead>
<tr>
<th>InnerCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>Device-nGnRnE.</td>
</tr>
<tr>
<td>0b001</td>
<td>Normal Inner Non-cacheable.</td>
</tr>
<tr>
<td>0b010</td>
<td>Normal Inner Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b011</td>
<td>Normal Inner Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Inner Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Inner Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Inner Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Bits [58:56]

Reserved, RES0.

OuterCache, bits [55:53]

Indicates the Outer Cacheability attributes of accesses to the command queue. The possible values of this field are:

<table>
<thead>
<tr>
<th>OuterCache</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Memory type defined in InnerCache field. For Normal memory, Outer Cacheability is the same as Inner Cacheability.</td>
</tr>
<tr>
<td>0b01</td>
<td>Normal Outer Non-cacheable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Normal Outer Cacheable Read-allocate, Write-through.</td>
</tr>
<tr>
<td>0b11</td>
<td>Normal Outer Cacheable Read-allocate, Write-back.</td>
</tr>
<tr>
<td>0b100</td>
<td>Normal Outer Cacheable Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b101</td>
<td>Normal Outer Cacheable Write-allocate, Write-back.</td>
</tr>
<tr>
<td>0b110</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-through.</td>
</tr>
<tr>
<td>0b111</td>
<td>Normal Outer Cacheable Read-allocate, Write-allocate, Write-back.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bit [52]

Reserved, RES0.

Physical_Address, bits [51:12]

Bits [51:12] of the base physical address of the command queue. Bits [11:0] of the base address are 0.

In implementations supporting fewer than 52 bits of physical address, unimplemented upper bits are RES0.

If bits [15:12] are not all zeros, behavior is a CONSTRAINED UNPREDICTABLE choice:

- Bits [15:12] are treated as if all the bits are zero. The value read back from those bits is either the value written or zero.
- The result of the calculation of an address for a command queue read can be corrupted.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Shareability, bits [11:10]

Indicates the Shareability attributes of accesses to the command queue. The possible values of this field are:

<table>
<thead>
<tr>
<th>Shareability</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Non-shareable.</td>
</tr>
<tr>
<td>0b01</td>
<td>Inner Shareable.</td>
</tr>
<tr>
<td>0b10</td>
<td>Outer Shareable.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved. Treated as 0b00.</td>
</tr>
</tbody>
</table>

It is IMPLEMENTATION DEFINED whether this field has a fixed value or can be programmed by software. Implementing this field with a fixed value is deprecated.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [9:8]

Reserved, RES0.
Size, bits [7:0]

The number of 4KB pages of physical memory allocated to the command queue, minus one.

On a Warm reset, this field resets to an architecturally unknown value.

The command queue is a circular buffer and wraps at Physical Address [47:0] + (4096 * (Size + 1)).

Note

When this register is successfully written, the value of GITS_CREADR is set to zero.

Accessing the GITS_CBASER

When GITS_CTLR.Enabled == 1 or GITS_CTLR.Quiescent == 0, writing this register is unpredictable.

GITS_CBASER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0080</td>
<td>GITS_CBASER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
GITS_CREADR, ITS Read Register

The GITS_CREADR characteristics are:

**Purpose**

Specifies the offset from GITS_CBASER where the ITS reads the next ITS command.

**Configuration**

This register is cleared to 0 when a value is written to GITS_CBASER.

Bits [63:32] and bits [31:0] are accessible separately.

**Attributes**

GITS_CREADR is a 64-bit register.

**Field descriptions**

The GITS_CREADR bit assignments are:

| 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | 51 | 50 | 49 | 48 | 47 | 46 | 45 | 44 | 43 | 42 | 41 | 40 | 39 | 38 | 37 | 36 | 35 | 34 | 33 | 32 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | Offset | RES0 | Stalled |
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

**Bits [63:20]**

Reserved, RES0.

**Offset, bits [19:5]**


**Bits [4:1]**

Reserved, RES0.

**Stalled, bit [0]**

Reports whether the processing of commands is stalled because of a command error.

<table>
<thead>
<tr>
<th>Stalled</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>ITS command queue is not stalled because of a command error.</td>
</tr>
<tr>
<td>0b1</td>
<td>ITS command queue is stalled because of a command error.</td>
</tr>
</tbody>
</table>

For more information, see ‘The ITS command interface’ in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).
Accessing the GITS_CREADR

GITS_CREADR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0090</td>
<td>GITS_CREADR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.
The GITS_CTLR characteristics are:

**Purpose**

Controls the operation of an ITS.

**Configuration**

The ITS_Number (bits [7:4]) and bit [1] fields apply only in FEAT_GICv4 implementations, and are RES0 in FEAT_GICv3 implementations.

**Attributes**

GITS_CTLR is a 32-bit register.

**Field descriptions**

The GITS_CTLR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Quiescent</td>
</tr>
<tr>
<td>30</td>
<td>READ-ONLY</td>
</tr>
<tr>
<td>28</td>
<td>RESERVED, RES0</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>8</td>
<td>UMSlirq</td>
</tr>
<tr>
<td>7</td>
<td>ITS_Number, RES0</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0</td>
</tr>
</tbody>
</table>

**Quiescent, bit [31]**

Read-only. Indicates completion of all ITS operations when GITS_CTLR.Enabled == 0.

<table>
<thead>
<tr>
<th>Quiescent</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The ITS is not quiescent and cannot be powered down.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ITS is quiescent and can be powered down.</td>
</tr>
</tbody>
</table>

For the ITS to be considered inactive, there must be no transactions in progress. In addition, all operations required to ensure that mapping data is consistent with external memory must be complete.

**Note**

In distributed GIC implementations, this bit is set to 1 only after the ITS forwards any operations that have not yet been completed to the Redistributors and receives confirmation that all such operations have reached the appropriate Redistributor.

In FEAT_GICv3, FEAT_GICv3p1, and FEAT_GICv4, when GITS_CTLR.Enabled == 1, the value of GITS_CTLR.Quiiescent is UNKNOWN.

In FEAT_GICv4p1, when GITS_CTLR.Enabled == 1, the value of GITS_CTLR.Quiiescent reads as 1 until the write to Enabled has taken effect and then reads as 0.

On a Warm reset, this field resets to 1.

**Bits [30:9]**

Reserved, RES0.

**UMSlirq, bit [8]**

Unmapped MSI reporting interrupt enable.
UMSIirq | Meaning
--- | ---
0b0 | The ITS does not assert an interrupt signal when GITS_STATUSR.UMSI is 1.
0b1 | The ITS asserts an interrupt signal when GITS_STATUSR.UMSI is 1.

If GITS_TYPER.UMSIirq is 0, this field is RES0.

On a Warm reset, this field resets to 0.

**ITS_Number, bits [7:4]**

In FEAT_GICv3 implementations this field is RES0.

In FEAT_GICv4 implementations with more than one ITS instance, this field indicates the ITS number for use with 'VMOVPE GICv4.0' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

It is IMPLEMENTATION DEFINED whether this field is programmable or RO.

If this field is programmable, changing this field when GITS_CTLR.Quiescent == 0 or GITS_CTLR.Enabled == 1 is UNPREDICTABLE.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Bits [3:2]**

Reserved, RES0.

**ImDe, bit [1]**

In GICv3 implementations, this bit is RES0.

In GICv4 implementations, this bit is IMPLEMENTATION DEFINED.

On a Warm reset, this field resets to 0.

**Enabled, bit [0]**

Controls whether the ITS is enabled:

<table>
<thead>
<tr>
<th>Enabled</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The ITS is not enabled. Writes to GITS_TRANSLATER are ignored and no further command queue entries are processed.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ITS is enabled. Writes to GITS_TRANSLATER result in interrupt translations and the command queue is processed.</td>
</tr>
</tbody>
</table>

If a write to this register changes this field from 1 to 0, the ITS must ensure that both:

- Any caches containing mapping data are made consistent with external memory.
- GITS_CTLR.Quiescent == 0 until all caches are consistent with external memory.

Changing GITS_CTLR.Enabled from 0 to 1 when GITS_CTLR.Quiescent is 0 results in UNPREDICTABLE behavior.

On a Warm reset, this field resets to 0.

**Accessing the GITS_CTLR**

GITS_CTLR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0000</td>
<td>GITS_CTLR</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RW**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GITS_CWRITER, ITS Write Register

The GITS_CWRITER characteristics are:

Purpose

Specifies the offset from GITS_CBASER where software writes the next ITS command.

Configuration

Bits [63:32] and bits [31:0] are accessible separately.

Attributes

GITS_CWRITER is a 64-bit register.

Field descriptions

The GITS_CWRITER bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>62</td>
<td></td>
<td></td>
</tr>
<tr>
<td>61</td>
<td></td>
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<tr>
<td>60</td>
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<td>59</td>
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<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:20]

Reserved, RES0.

Offset, bits [19:5]

Bits [19:5] of the offset from GITS_CBASER. Bits [4:0] of the offset are zero. On a Warm reset, this field resets to an architecturally UNKNOWN value.

Bits [4:1]

Reserved, RES0.

Retry, bit [0]

Writing this bit has the following effects:

<table>
<thead>
<tr>
<th>Retry</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No effect on the processing commands by the ITS.</td>
</tr>
<tr>
<td>0b1</td>
<td>Restarts the processing of commands by the ITS if it stalled because of a command error.</td>
</tr>
</tbody>
</table>

Note

If the processing of commands is not stalled because of a command error, writing 1 to this bit has no effect.

When read, this bit is RES0.

For more information, see 'The ITS command interface' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).
If GITS_CWRITER is written with a value outside of the valid range specified by GITS_CBASER.Physical_Address and GITS_CBASER.Size, behavior is a CONSTRAINED UNPREDICTABLE choice, as follows:

- The command queue is considered invalid, and no further commands are processed until GITS_CWRITER is written with a value that is in the valid range.
- The value is treated as a valid UNKNOWN value.

An implementation might choose to report a system error in an IMPLEMENTATION DEFINED manner.

Accessing the GITS_CWRITER

GITS_CWRITER can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0088</td>
<td>GITS_CWRITER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RW.
- When an access is Secure accesses to this register are RW.
- When an access is Non-secure accesses to this register are RW.
The GITS_IIDR characteristics are:

**Purpose**

Provides information about the implementer and revision of the ITS.

**Configuration**

This register is available in all configurations of the GIC. If the GIC implementation supports two Security states, this register is Common.

**Attributes**

GITS_IIDR is a 32-bit register.

**Field descriptions**

The GITS_IIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>ProductID</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>Variant</td>
</tr>
<tr>
<td>28</td>
<td>Revision</td>
</tr>
<tr>
<td>27</td>
<td>Implementer</td>
</tr>
</tbody>
</table>

**ProductID, bits [31:24]**

An IMPLEMENTATION DEFINED product identifier.

**Bits [23:20]**

Reserved, RES0.

**Variant, bits [19:16]**

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish product variants, or major revisions of a product.

**Revision, bits [15:12]**

An IMPLEMENTATION DEFINED revision number. Typically, this field is used to distinguish minor revisions of a product.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the ITS:

- Bits [11:8] are the JEP106 continuation code of the implementer. For an Arm implementation, this field is 0x4.
- Bit [7] is always 0.
- Bits [6:0] are the JEP106 identity code of the implementer. For an Arm implementation, bits [7:0] are therefore 0x3B.
Accessing the GITS_IIDR

GITS_IIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0004</td>
<td>GITS_IIDR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GITS_MPAMIDR, Report maximum PARTID and PMG Register

The GITS_MPAMIDR characteristics are:

**Purpose**

Reports the maximum support PARTID and PMG values.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GITS_MPAMIDR are RES0.

A copy of this register is provided for each ITS.

When GITS_TYPER.MPAM==0, this register is RES0.

**Attributes**

GITS_MPAMIDR is a 32-bit register.

**Field descriptions**

The GITS_MPAMIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PMGmax</td>
</tr>
<tr>
<td>24</td>
<td>PARTIDmax</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**PMGmax, bits [23:16]**

Maximum PMG value supported.

**PARTIDmax, bits [15:0]**

Maximum PARTID value supported.

**Accessing the GITS_MPAMIDR**

GITS_MPAMIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0010</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
- When an access is Non-secure accesses to this register are RO.
GITS_MPIDR, Report ITS's affinity.

The GITS_MPIDR characteristics are:

**Purpose**

Reports ITS's affinity when the vPE Table is shared with Redistributors.

**Configuration**

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GITS_MPIDR are RES0.

A copy of this register is provided for each ITS.

When GITS_TYPER.SVPET==0, this register is RES0.

**Attributes**

GITS_MPIDR is a 32-bit register.

**Field descriptions**

The GITS_MPIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-24</td>
<td>Aff3, Affinity level 3 value for the ITS.</td>
</tr>
<tr>
<td>23-16</td>
<td>Aff2, Affinity level 2 value for the ITS.</td>
</tr>
<tr>
<td>15-8</td>
<td>Aff1, Affinity level 1 value for the ITS.</td>
</tr>
<tr>
<td>7-0</td>
<td>RES0, Reserved.</td>
</tr>
</tbody>
</table>

**Accessing the GITS_MPIDR**

GITS_MPIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0018</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTRLR.DS == 0 accesses to this register are RO.
- When an access is Secure accesses to this register are RO.
• When an access is Non-secure accesses to this register are RO.
The GITS_PARTIDR characteristics are:

**Purpose**

Sets the PARTID and PMG values used for memory accesses by the ITS.

**Configuration**

This register is present only when FEAT_GICv3p1 is implemented. Otherwise, direct accesses to GITS_PARTIDR are RES0.

A copy of this register is provided for each ITS.

When GITS_TYPER.MPAM==0, this register is RES0.

**Attributes**

GITS_PARTIDR is a 32-bit register.

**Field descriptions**

The GITS_PARTIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PMG</td>
</tr>
<tr>
<td>29</td>
<td>PARTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**PMG, bits [23:16]**

PMG value used when ITS accesses memory.

It is IMPLEMENTATION DEFINED whether bits not needed to represent PMG values in the range 0 to PMG_MAX are stateful or RES0.

On a Warm reset, this field resets to 0.

**PARTID, bits [15:0]**

PARTID value used when ITS accesses memory.

It is IMPLEMENTATION DEFINED whether bits not needed to represent PARTID values in the range 0 to PARTID_MAX are stateful or RES0.

On a Warm reset, this field resets to 0.

**Accessing the GITS_PARTIDR**

GITS_PARTIDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0014</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are \textbf{RW}.
- When an access is Secure accesses to this register are \textbf{RW}.
- When an access is Non-secure accesses to this register are \textbf{RW}.
GITS_SGIR, ITS SGI Register

The GITS_SGIR characteristics are:

Purpose

Written by software to signal a virtual SGI for translation by the ITS.

Configuration

This register is present only when FEAT_GICv4p1 is implemented. Otherwise, direct accesses to GITS_SGIR are RES0. This register is provided only in FEAT_GICv4p1 implementations.

Attributes

GITS_SGIR is a 64-bit register.

Field descriptions

The GITS_SGIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>[63:48]</td>
<td>Reserved, RES0.</td>
<td></td>
</tr>
<tr>
<td>[47:32]</td>
<td>vPEID, ID of target vPEID.</td>
<td></td>
</tr>
<tr>
<td>[31:4]</td>
<td>Reserved, RES0.</td>
<td></td>
</tr>
<tr>
<td>[3:0]</td>
<td>vINTID, INTID of virtual SGI.</td>
<td></td>
</tr>
</tbody>
</table>

Bits [63:48]

Reserved, RES0.

vPEID, bits [47:32]

ID of target vPEID.

The size of this field is IMPLEMENTATION DEFINED, and is specified by the GICD_TYPER2.VIL and GICD_TYPER2.VID fields. Unimplemented bits are RES0.

Bits [31:4]

Reserved, RES0.

Accessing the GITS_SGIR

64-bit access only.

GITS_SGIR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x20020</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTRL_DS == 0 accesses to this register are **WO**.
- When an access is Secure accesses to this register are **WO**.
- When an access is Non-secure accesses to this register are **WO**.
GITS_STATUSR, ITS Error Reporting Status Register

The GITS_STATUSR characteristics are:

Purpose

Provides software with a mechanism to detect:

• Accesses to reserved locations.
• Writes to read-only locations.
• Reads of write-only locations.
• Unmapped MSIs.

Configuration

Attributes

GITS_STATUSR is a 32-bit register.

Field descriptions

The GITS_STATUSR bit assignments are:

| Bit 31 | Bit 30 | Bit 29 | Bit 28 | Bit 27 | Bit 26 | Bit 25 | Bit 24 | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| \[31:10\] | \[9:6\] | Syndrome | Overflow | UMSI | WROD | RWOD | WRD | RRD |

Bits \[31:10\]

Reserved, RES0.

Syndrome, bits \[9:6\]

Syndrome for the MSI that set GITS_STATUSR.UMSI to 1.

<table>
<thead>
<tr>
<th>Syndrome</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>Unknown reason.</td>
</tr>
<tr>
<td>0b0010</td>
<td>DeviceID out of range.</td>
</tr>
<tr>
<td>0b0011</td>
<td>DeviceID unmapped.</td>
</tr>
<tr>
<td>0b0100</td>
<td>EventID out of range.</td>
</tr>
<tr>
<td>0b0101</td>
<td>EventID unmapped.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Collection unmapped.</td>
</tr>
<tr>
<td>0b1001</td>
<td>vPEID unmapped.</td>
</tr>
</tbody>
</table>

An implementation might not support reporting all syndromes, and might report 0b0000 for any cause.

This field is UNKNOWN when GITS_STATUSR.UMSI is 0.

Overflow, bit \[5\]

Reports whether an unmapped MSI has been received while GITS_STATUSR.UMSI is 1.

<table>
<thead>
<tr>
<th>Overflow</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No unmapped MSIs have been received since GITS_STATUSR.UMSI set to 1.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one unmapped MSIs have been received since GITS_STATUSR.UMSI set to 1.</td>
</tr>
</tbody>
</table>

A software write of 1 to the bit clears it. A write of any other value is ignored.
If \texttt{GITS\_TYPER\_UMSI} is 0, this field is \texttt{RES0}.

**UMSI, bit [4]**

Reports whether an unmapped MSI has been received

<table>
<thead>
<tr>
<th>UMSI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No unmapped MSIs have been received.</td>
</tr>
<tr>
<td>0b1</td>
<td>Unmapped MSI received.</td>
</tr>
</tbody>
</table>

A software write of 1 to the bit clears it. A write of any other value is ignored.

If \texttt{GITS\_TYPER\_UMSI} is 0, this field is \texttt{RES0}.

**WROD, bit [3]**

Write to an RO location.

<table>
<thead>
<tr>
<th>WROD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to an RO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**RWOD, bit [2]**

Read of a WO location.

<table>
<thead>
<tr>
<th>RWOD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a WO location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**WRD, bit [1]**

Write to a reserved location.

<table>
<thead>
<tr>
<th>WRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A write to a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**RRD, bit [0]**

Read of a reserved location.

<table>
<thead>
<tr>
<th>RRD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>A read of a reserved location has been detected.</td>
</tr>
</tbody>
</table>

When a violation is detected, software must write 1 to this register to reset it.

**Accessing the GITS\_STATUSR**

This is an optional register. If the register is not implemented, the location is RAZ/WI.

\texttt{GITS\_STATUSR} can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0020</td>
<td>GITS_STATUSR</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
GITS_TRANSLATER, ITS Translation Register

The GITS_TRANSLATER characteristics are:

**Purpose**

Written by a requesting Device to signal an interrupt for translation by the ITS.

**Configuration**

This register is at the same offset as GICD_SETSPI_NSR in the Distributor, and is at the same offset as GICR_SETLPIR in the Redistributor.

**Attributes**

GITS_TRANSLATER is a 32-bit register.

**Field descriptions**

The GITS_TRANSLATER bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EventID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**EventID, bits [31:0]**

An identifier corresponding to the interrupt to be translated.

**Note**

The size of the EventID is DeviceID specific, and set when the DeviceID is mapped to an ITT (using MAPD).

The number of EventID bits implemented is reported by GITS_TYPER.ID_bits. If a write specifies non-zero identifiers bits outside this range behavior is a CONSTRAINED UNPREDICTABLE choice between:

- Non-zero identifier bits outside the supported range are ignored.
- The write is ignored.

The DeviceID presented to an ITS is used to index a device table. The device table maps the DeviceID to an interrupt translation table for that device.

**Accessing the GITS_TRANSLATER**

16-bit access to bits [15:0] of this register must be supported. When this register is written by a 16-bit transaction, bits [31:16] are written as zero.

Implementations must ensure that:

- A unique DeviceID is provided for each requesting device, and the DeviceID is presented to the ITS when a write to this register occurs in a manner that cannot be spoofed by any agent capable of performing writes.
- The DeviceID presented corresponds to the DeviceID field in the ITS commands.

Writes to this register are ignored if any of the following are true:

- GITS_CTLR. Enabled == 0.
- The presented DeviceID is not mapped to an Interrupt Translation Table.
- The DeviceID is larger than the supported size.
• The DeviceID is mapped to an Interrupt Translation Table, but the EventID is outside the range specified by MAPD.
• The EventID is mapped to an Interrupt Translation Table and the EventID is within the range specified by MAPD, but the EventID is unmapped.

Translation requests that result from writes to this register are subject to certain ordering rules. For more information, see 'Ordering of translations with the output to ITS commands' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).

**GITS_TRANSLATER can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS translation</td>
<td>0x0040</td>
<td>GITS_TRANSLATER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

• When GICD_CTLR.DS == 0 accesses to this register are **WO**.
• When an access is Secure accesses to this register are **WO**.
• When an access is Non-secure accesses to this register are **WO**.
# GITS_TYPER, ITS Type Register

The GITS_TYPER characteristics are:

## Purpose

Specifies the features that an ITS supports.

## Configuration

## Attributes

GITS_TYPER is a 64-bit register.

## Field descriptions

The GITS_TYPER bit assignments are:

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63:46</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>45</td>
<td><strong>UMSI_irq</strong>, bit 45**</td>
</tr>
<tr>
<td><strong>Meaning</strong></td>
<td></td>
</tr>
<tr>
<td>0b0</td>
<td>Interrupt on unmapped MSI not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Interrupt on unmapped MSI is supported.</td>
</tr>
<tr>
<td>44</td>
<td><strong>UMSI</strong>, bit 44**</td>
</tr>
<tr>
<td><strong>Meaning</strong></td>
<td></td>
</tr>
<tr>
<td>0b0</td>
<td>Reporting of unmapped MSIs is not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reporting of unmapped MSIs is supported.</td>
</tr>
<tr>
<td>43</td>
<td><strong>nID</strong>, bit 43**</td>
</tr>
<tr>
<td><strong>Meaning</strong></td>
<td></td>
</tr>
<tr>
<td>0b0</td>
<td>Individual doorbell interrupt supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Individual doorbell interrupt not supported.</td>
</tr>
</tbody>
</table>

## Bits [63:46]

Reserved, RES0.

## UMSI_irq, bit [45]

Indicates support for generating an interrupt on receiving unmapped MSI.

## UMSI, bit [44]

Indicates support for reporting receipt of unmapped MSIs.

## nID, bit [43]

When FEAT_GICv4p1 is implemented:

### nID

<table>
<thead>
<tr>
<th>Bits</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Individual doorbell interrupt supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Individual doorbell interrupt not supported.</td>
</tr>
</tbody>
</table>
Otherwise:
Reserved, RES0.

**SVPET, bits [42:41]**

**When FEAT_GICv4p1 is implemented:**

<table>
<thead>
<tr>
<th>SVPET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>vPE Table is not shared with Redistributors.</td>
</tr>
<tr>
<td>0b01</td>
<td>vPE Table is shared with the groups of Redistributors indicated by GITS_MPIDR.Aff3.</td>
</tr>
<tr>
<td>0b10</td>
<td>vPE Table is shared with the groups of Redistributors indicated by GITS_MPIDR fields Aff3 and Aff2.</td>
</tr>
<tr>
<td>0b11</td>
<td>vPE Table is shared with the groups of Redistributors indicated by GITS_MPIDR fields Aff3, Aff2 and Aff1.</td>
</tr>
</tbody>
</table>

Otherwise:
Reserved, RES0.

**VMAPP, bit [40]**

**When FEAT_GICv4p1 is implemented:**

<table>
<thead>
<tr>
<th>VMAPP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>FEAT_GICv4 VMAPP command layout.</td>
</tr>
<tr>
<td>0b1</td>
<td>FEAT_GICv4p1 VMAPP command layout.</td>
</tr>
</tbody>
</table>

Otherwise:
Reserved, RES0.

**VSGI, bit [39]**

**When FEAT_GICv4p1 is implemented:**

<table>
<thead>
<tr>
<th>VSGI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Direct injection of SGIs is not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>Direct injection of SGIs is supported.</td>
</tr>
</tbody>
</table>

Otherwise:
Reserved, RES0.

**MPAM, bit [38]**

**When FEAT_GICv3p1 is implemented:**

<table>
<thead>
<tr>
<th>MPAM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAM is not supported.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM is supported.</td>
</tr>
</tbody>
</table>
Otherwise:

Reserved, RES0.

### VMOVP, bit [37]

Indicates the form of the VMOVP command.

<table>
<thead>
<tr>
<th>VMOVP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When moving a vPE, software must issue a VMOVP on all ITSs that have mappings for that vPE. The ITSList and Sequence Number fields in the VMOVP command must ensure synchronization, otherwise behavior is UNPREDICTABLE.</td>
</tr>
<tr>
<td>0b1</td>
<td>When moving a vPE, software must only issue a VMOVP on one of the ITSs that has a mapping for that vPE. The ITSList and Sequence Number fields in the VMOVP command are RES0.</td>
</tr>
</tbody>
</table>

### CIL, bit [36]

Collection ID Limit.

<table>
<thead>
<tr>
<th>CIL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>GITS_TYPER.CIDbits is RES0. ITS supports 16-bit Collection ID, GITS_TYPER.CIDbits is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>GITS_TYPER.CIDbits indicates supported Collection ID size</td>
</tr>
</tbody>
</table>

In implementations that do not support Collections in external memory, this bit is RES0 and the number of Collections supported is reported by GITS_TYPER.HCC.

### CIDbits, bits [35:32]

Number of Collection ID bits.

- The number of bits of Collection ID minus one.
- When GITS_TYPER.CIL == 0, this field is RES0.

### HCC, bits [31:24]

Hardware Collection Count. The number of interrupt collections supported by the ITS without provisioning of external memory.

**Note**

Collections held in hardware are unmapped at reset.

### Bits [23:20]

Reserved, RES0.

### PTA, bit [19]

Physical Target Addresses. Indicates the format of the target address:

<table>
<thead>
<tr>
<th>PTA</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The target address corresponds to the PE number specified by GICR_TYPER.Processor_Number.</td>
</tr>
<tr>
<td>0b1</td>
<td>The target address corresponds to the base physical address of the required Redistributor.</td>
</tr>
</tbody>
</table>

For more information, see 'RDbase' in ARM® Generic Interrupt Controller Architecture Specification, GIC architecture version 3.0 and version 4.0 (ARM IHI 0069).
SEIS, bit [18]

SEI support. Indicates whether the virtual CPU interface supports generation of SEIs:

<table>
<thead>
<tr>
<th>SEIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The ITS does not support local generation of SEIs.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ITS supports local generation of SEIs.</td>
</tr>
</tbody>
</table>

Devbits, bits [17:13]

The number of DeviceID bits implemented, minus one.

ID_bits, bits [12:8]

The number of EventID bits implemented, minus one.

ITT_entry_size, bits [7:4]

Read-only. Indicates the number of bytes per translation table entry, minus one.

For more information about the ITS command 'MAPD', see MAPD.

IMPLEMENTATION DEFINED, bit [3]

IMPLEMENTATION DEFINED.

CCT, bit [2]

Cumulative Collection Tables.

<table>
<thead>
<tr>
<th>CCT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The total number of supported collections is determined by the number</td>
</tr>
<tr>
<td></td>
<td>of collections held in memory only.</td>
</tr>
<tr>
<td>0b1</td>
<td>The total number of supported collections is determined by the number</td>
</tr>
<tr>
<td></td>
<td>of collections that are held in memory and the number that is indicated</td>
</tr>
<tr>
<td></td>
<td>by the GITS_TYPER.HCC.</td>
</tr>
</tbody>
</table>

If GITS_TYPER.HCC == 0, or if memory backed collections are not supported (all GITS_BASER<n>.Type != 100), this bit is RES0.

Virtual, bit [1]

When FEAT_GICv4 is implemented:

Indicates whether the ITS supports virtual LPIs and direct injection of virtual LPIs:

<table>
<thead>
<tr>
<th>Virtual</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The ITS does not support virtual LPIs or direct injection of virtual LPIs</td>
</tr>
<tr>
<td>0b1</td>
<td>The ITS supports virtual LPIs and direct injection of virtual LPIs</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

Physical, bit [0]

Indicates whether the ITS supports physical LPIs:
### Physical Meaning

<table>
<thead>
<tr>
<th>Physical</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The ITS does not support physical LPIS.</td>
</tr>
<tr>
<td>0b1</td>
<td>The ITS supports physical LPIS.</td>
</tr>
</tbody>
</table>

This field is RES1, indicating that the ITS supports physical LPIS.

## Accessing the GITS_TYPER

**GITS_TYPER can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0008</td>
<td>GITS_TYPER</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RO**.
- When an access is Non-secure accesses to this register are **RO**.

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GITS_UMSIR, ITS Unmapped MSI register

The GITS_UMSIR characteristics are:

**Purpose**

Provides the DeviceID and EventID of the unmapped MSI that set GITS_STATUSR.UMSI.

**Configuration**

This register is present only when GITS_TYPER.UMSI == 1. Otherwise, direct accesses to GITS_UMSIR are RES0.

**Attributes**

GITS_UMSIR is a 64-bit register.

**Field descriptions**

The GITS_UMSIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>DeviceID</th>
<th>EventID</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
</tr>
<tr>
<td>60</td>
<td>59</td>
<td>58</td>
</tr>
<tr>
<td>57</td>
<td>56</td>
<td>55</td>
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<tr>
<td>54</td>
<td>53</td>
<td>52</td>
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<tr>
<td>51</td>
<td>50</td>
<td>49</td>
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<tr>
<td>48</td>
<td>47</td>
<td>46</td>
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<td>45</td>
<td>44</td>
<td>43</td>
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<td>42</td>
<td>41</td>
<td>40</td>
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<td>39</td>
<td>38</td>
<td>37</td>
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<tr>
<td>36</td>
<td>35</td>
<td>34</td>
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<td>33</td>
<td>32</td>
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<td>12</td>
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<td>11</td>
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<td>10</td>
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<td></td>
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<td>9</td>
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<td>8</td>
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<td></td>
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<td>7</td>
<td></td>
<td></td>
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<tr>
<td>6</td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**DeviceID, bits [63:32]**

DeviceID of MSI that set GITS_STATUSR.UMSI to 1.

If GITS_STATUSR.UMSI is 0, this field is UNKNOWN.

**EventID, bits [31:0]**

EventID of MSI that set GITS_STATUSR.UMSI to 1.

If GITS_STATUSR.UMSI is 0, this field is UNKNOWN.

**Accessing the GITS_UMSIR**

GITS_UMSIR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>GIC ITS control</td>
<td>0x0028</td>
<td>GITS_UMSIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When GICD_CTLR.DS == 0 accesses to this register are **RO**.
- When an access is Secure accesses to this register are **RW**.
- When an access is Non-secure accesses to this register are **RW**.
The MIDR_EL1 characteristics are:

**Purpose**

Provides identification information for the PE, including an implementer code for the device and a device ID number.

**Configuration**

External register MIDR_EL1 bits [31:0] are architecturally mapped to AArch64 System register MIDR_EL1[31:0].

External register MIDR_EL1 bits [31:0] are architecturally mapped to AArch32 System register MIDR[31:0].

It is IMPLEMENTATION DEFINED whether MIDR_EL1 is implemented in the Core power domain or in the Debug power domain.

**Attributes**

MIDR_EL1 is a 32-bit register.

**Field descriptions**

The MIDR_EL1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Implementer | Variant | Architecture | PartNum | Revision |

**Implementer, bits [31:24]**

The Implementer code. This field must hold an implementer code that has been assigned by Arm. Assigned codes include the following:

<table>
<thead>
<tr>
<th>Hex representation</th>
<th>Implementer</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Reserved for software use</td>
</tr>
<tr>
<td>0xC0</td>
<td>Ampere Computing</td>
</tr>
<tr>
<td>0x41</td>
<td>Arm Limited</td>
</tr>
<tr>
<td>0x42</td>
<td>Broadcom Corporation</td>
</tr>
<tr>
<td>0x43</td>
<td>Cavium Inc.</td>
</tr>
<tr>
<td>0x44</td>
<td>Digital Equipment Corporation</td>
</tr>
<tr>
<td>0x46</td>
<td>Fujitsu Ltd.</td>
</tr>
<tr>
<td>0x49</td>
<td>Infineon Technologies AG</td>
</tr>
<tr>
<td>0x40</td>
<td>Motorola or Freescale Semiconductor Inc.</td>
</tr>
<tr>
<td>0x4E</td>
<td>NVIDIA Corporation</td>
</tr>
<tr>
<td>0x50</td>
<td>Applied Micro Circuits Corporation</td>
</tr>
<tr>
<td>0x51</td>
<td>Qualcomm Inc.</td>
</tr>
<tr>
<td>0x56</td>
<td>Marvell International Ltd.</td>
</tr>
<tr>
<td>0x69</td>
<td>Intel Corporation</td>
</tr>
</tbody>
</table>

Arm can assign codes that are not published in this manual. All values not assigned by Arm are reserved and must not be used.

**Variant, bits [23:20]**

An IMPLEMENTATION DEFINED variant number. Typically, this field is used to distinguish between different product variants, or major revisions of a product.
Architecture, bits [19:16]

Architecture version. Defined values are:

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0001</td>
<td>Armv4.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Armv4T.</td>
</tr>
<tr>
<td>0b0011</td>
<td>Armv5 (obsolete).</td>
</tr>
<tr>
<td>0b0100</td>
<td>Armv5T.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Armv5TE.</td>
</tr>
<tr>
<td>0b0110</td>
<td>Armv5TEJ.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Armv6.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Architectural features are individually identified in the ID_* registers, see 'ID registers'.</td>
</tr>
</tbody>
</table>

All other values are reserved.

PartNum, bits [15:4]

An implementation defined primary part number for the device.

On processors implemented by Arm, if the top four bits of the primary part number are 0x0 or 0x7, the variant and architecture are encoded differently.

Revision, bits [3:0]

An implementation defined revision number for the device.

Accessing the MIDR_EL1

MIDR_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0xD00</td>
<td>MIDR_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered() and !DoubleLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register are **IMPDEF**.

---

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The MPAMCFG_CMAX characteristics are:

**Purpose**

The MPAMCFG_CMAX is a 32-bit read-write register that controls the maximum fraction of the cache capacity that the PARTID selected by MPAMCFG_PART_SEL is permitted to allocate. MPAMCFG_CMAX_s controls cache maximum capacity for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_CMAX_ns controls the cache maximum capacity for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_CMAX is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_CCAP_PART == 1. Otherwise, direct accesses to MPAMCFG_CMAX are RES0.

**Attributes**

MPAMCFG_CMAX is a 32-bit register.

**Field descriptions**

The MPAMCFG_CMAX bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |
|     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |     |

**Bits [31:16]**

Reserved, RES0.

**CMAX, bits [15:0]**

Maximum cache capacity usage in fixed-point fraction format by the partition selected by MPAMCFG_PART_SEL. The fraction represents the portion of the total cache capacity that the PARTID is permitted to allocate.

The implemented width of the fixed-point fraction is given in MPAMF_CCAP_IDR.CMAX_WD. Unimplemented bits within the field are RAZ/WI. The implemented bits of the CMAX field are always the most-significant bits of the field.

The fixed-point fraction CMAX is less than 1. The implied binary point is between bits 15 and 16. This representation has as the largest fraction of the cache that can be represented in an implementation with w implemented bits is 1 - 1/ w.

**Accessing the MPAMCFG_CMAX**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_CMAX_s must be accessible from the Secure MPAM feature page. MPAMCFG_CMAX_ns must be accessible from the Non-secure MPAM feature page.
MPAMCFG_CMAX_s and MPAMCFG_CMAX_ns must be separate registers. The Secure instance (MPAMCFG_CMAX_s) accesses the cache capacity partitioning used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_CMAX_ns) accesses the cache capacity partitioning used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_CMAX access the cache maximum capacity partitioning configuration settings for the cache resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_CMAX access the cache maximum capacity partitioning configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_CMAX access the cache maximum capacity partitioning configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_CMAX access the cache maximum capacity partitioning configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

**MPAMCFG_CMAX can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0108</td>
<td>MPAMCFG_CMAX_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0108</td>
<td>MPAMCFG_CMAX_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
MPAMCFG_CPBM<n>, MPAM Cache Portion Bitmap Partition Configuration Register, n = 0 - 1023

The MPAMCFG_CPBM<n> characteristics are:

**Purpose**

The MPAMCFG_CPBM<n> register array gives access to the cache portion bitmap. Each register in the array is a read-write register that configures the cache portions numbered from \(<n \times 32>\) to \(<31 + (n \times 32)>\) that a PARTID is allowed to allocate.

After setting MPAMCFG_PART_SEL with a PARTID, software writes to the MPAMCFG_CPBM<n> register to configure which cache portions the PARTID is allowed to allocate.

The MPAMCFG_CPBM<n> register that contains the bitmap bit corresponding to cache portion \(p\) has \(n\) equal to \(p[15:5]\). The field, \(P<x>\), of that MPAMCFG_CPBM<n> register that contain the bitmap bit corresponding to cache portion \(p\) has \(x\) equal to \(p[4:0]\).

MPAMCFG_CPBM<n>_s controls cache portions for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_CPBM<n>_ns controls the cache portions for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_CPBM<n> is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_CPOR_Part == 1. Otherwise, direct accesses to MPAMCFG_CPBM<n> are res0.

**Attributes**

MPAMCFG_CPBM<n> is a 32-bit register.

**Field descriptions**

The MPAMCFG_CPBM<n> bit assignments are:

\[
P<x + (n \times 32)>, \text{bit } [x] , \text{for } x = 31 \text{ to } 0
\]

Portion allocation control bit. Each cache portion allocation control bit, MPAMCFG_CPBM<n>.P<x>, grants permission to the PARTID selected by MPAMCFG_PART_SEL to allocate cache lines within cache portion \(<x + (n \times 32)>\).

<table>
<thead>
<tr>
<th>(P&lt;x + (n \times 32)&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The PARTID is not permitted to allocate into cache portion (&lt;x + (n \times 32)&gt;).</td>
</tr>
<tr>
<td>0b1</td>
<td>The PARTID is permitted to allocate within cache portion (&lt;x + (n \times 32)&gt;).</td>
</tr>
</tbody>
</table>

The number of bits in the cache portion partitioning bit map of this component is given in MPAMF_CPOR_IDR.CPBM_WD. CPBM_WD contains a value from 1 to \(2^{15}\), inclusive. Values of CPBM_WD greater than 32 require an array of 32-bit MPAMCFG_CPBM<n> registers to access the cache portion bitmap, up to 1024 registers.
Bits MPAMCFG_CPBM<n>.P<<x + (n * 32)>>, where <x + (n * 32)> is greater than or equal to CPBM_WD, are RES0:

- If n > MPAMF_CPOR_IDR.CPBM_WD[15:5], the entire 32 P<x> are RES0.
- If n == MPAMF_CPOR_IDR.CPBM_WD[15:5], bits [31: CPBM_WD[4:0]] are RES0 and the remaining bits are valid.
- If n < MPAMF_CPOR_IDR.CPBM_WD[15:5], the entire 32 P<x> are valid.

**Accessing the MPAMCFG_CPBM<n>**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_CPBM<n>_s must be accessible from the Secure MPAM feature page. MPAMCFG_CPBM<n>_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_CPBM<n>_s and MPAMCFG_CPBM<n>_ns must be separate registers. The Secure instance (MPAMCFG_CPBM<n>_s) accesses the cache portion bitmap used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_CPBM<n>_ns) accesses the cache portion bitmap used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_CPBM<n> access the cache portion bitmap configuration settings for the cache resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_CPBM<n> access the cache portion bitmap configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_CPBM<n> access the cache portion bitmap configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_CPBM<n> access the cache portion bitmap configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

**MPAMCFG_CPBM<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x1000 + (4 * n)</td>
<td>MPAMCFG_CPBM&lt;n&gt;_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x1000 + (4 * n)</td>
<td>MPAMCFG_CPBM&lt;n&gt;_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The MPAMCFG_INTPARTID characteristics are:

**Purpose**

MPAMCFG_INTPARTID is a 32-bit read-write register that controls the mapping of the PARTID selected by MPAMCFG_PART_SEL into a narrower internal PARTID (intPARTID).

MPAMCFG_INTPARTID_s controls the mapping for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_INTPARTID_ns controls the mapping for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

The MPAMCFG_INTPARTID register associates the request PARTID (reqPARTID) in the MPAMCFG_PART_SEL register with an internal PARTID (intPARTID) in this register. To set that association, store reqPARTID into the MPAMCFG_PART_SEL register and then store the intPARTID into the MPAMCFG_INTPARTID register. To read the association, store reqPARTID into the MPAMCFG_PART_SEL register and then read MPAMCFG_INTPARTID.

If the intPARTID stored into MPAMCFG_INTPARTID is out-of-range or does not have the INTERNAL bit set, the association of reqPARTID to intPARTID is not written and MPAMF_ESR is set to indicate an intPARTID_Range error.

If MPAMCFG_PART_SEL.INTERNAL is 1 when MPAMCFG_INTPARTID is read or written, MPAMF_ESR is set to indicate an Unexpected_INTERNAL error.

**Configuration**

The power domain of MPAMCFG_INTPARTID is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_PARTID_NRW == 1. Otherwise, direct accesses to MPAMCFG_INTPARTID are RES0.

**Attributes**

MPAMCFG_INTPARTID is a 32-bit register.

**Field descriptions**

The MPAMCFG_INTPARTID bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | INTERNAL | INTPARTID |

**Bits [31:17]**

Reserved, RES0.

**INTERNAL, bit [16]**

Internal PARTID flag.

This bit must be 1 when written to the register. If written as 0, the write will not update the reqPARTID to intPARTID association.

On a read of this register, the bit will always read the value last written.
INTPARTID, bits [15:0]

This field contains the intPARTID mapped to the reqPARTID in MPAMCFG_PART_SEL.
The maximum intPARTID supported is MPAMF_PARTID_NRW_IDR.INTPARTID_MAX.

Accessing the MPAMCFG_INTPARTID

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_INTPARTID_s must be accessible from the Secure MPAM feature page. MPAMCFG_INTPARTID_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_INTPARTID_s and MPAMCFG_INTPARTID_ns must be separate registers. The Secure instance (MPAMCFG_INTPARTID_s) accesses the PARTID narrowing used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_INTPARTID_ns) accesses the PARTID narrowing used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_INTPARTID access the PARTID narrowing configuration settings without being affected by MPAMCFG_PART_SEL.RIS.

Loads and stores to MPAMCFG_INTPARTID access the PARTID narrowing configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

MPAMCFG_INTPARTID can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0600</td>
<td>MPAMCFG_INTPARTID_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0600</td>
<td>MPAMCFG_INTPARTID_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
MPAMCFG_MBW_MAX, MPAM Memory Bandwidth Maximum Partition Configuration Register

The MPAMCFG_MBW_MAX characteristics are:

**Purpose**

MPAMCFG_MBW_MAX is a 32-bit read-write register that controls the maximum fraction of memory bandwidth that the PARTID selected by MPAMCFG_PART_SEL is permitted to use. MPAMCFG_MBW_MAX controls maximum bandwidth for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_MBW_MAX ns controls the maximum bandwidth for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

A PARTID that has used more than MAX is given no access to additional bandwidth if HARDLIM == 1 or is given additional bandwidth only if there are no requests from PARTIDs that have not exceeded their MAX if HARDLIM == 0.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_MBW_MAX is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MBW_PART == 1 and MPAMF_MBW_IDR.HAS_MAX == 1. Otherwise, direct accesses to MPAMCFG_MBW_MAX are RES0.

**Attributes**

MPAMCFG_MBW_MAX is a 32-bit register.

**Field descriptions**

The MPAMCFG_MBW_MAX bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| HARDLIM | RES0 | MAX |

**HARDLIM, bit [31]**

Hard bandwidth limiting.

<table>
<thead>
<tr>
<th>HARDLIM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When MAX bandwidth is exceeded, the partition contends with a low preference for downstream bandwidth beyond MAX.</td>
</tr>
<tr>
<td>0b1</td>
<td>When MAX bandwidth is exceeded, the partition does not be use any more bandwidth until the memory bandwidth measurement for the partition falls below MAX.</td>
</tr>
</tbody>
</table>

**Bits [30:16]**

Reserved, RES0.
MAX, bits [15:0]

Memory maximum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL. MAX is in fixed-point fraction format. The fraction represents the portion of the total memory bandwidth capacity through the controlled component that the PARTID is permitted to allocate.

The implemented width of the fixed-point fraction is given in MPAMF_MBW_IDR.BWA_WD. Unimplemented bits are RAZ/WI. The implemented bits of the MAX field are always to the left of the field. For example, if BWA_WD = 3, the implemented bits are MPAMCFG_MBW_MAX[15:13] and MPAMCFG_MBW_MAX[12:0] are unimplemented.

The fixed-point fraction MAX is less than 1. The implied binary point is between bits 15 and 16. This representation has as the largest fraction of the bandwidth that can be represented in an implementation with w implemented bits is 1 - 1/w.

Accessing the MPAMCFG_MBW_MAX

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_MBW_MAX_s must be accessible from the Secure MPAM feature page. MPAMCFG_MBW_MAX_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_MBW_MAX_s and MPAMCFG_MBW_MAX_ns must be separate registers. The Secure instance (MPAMCFG_MBW_MAX_s) accesses the memory maximum bandwidth partitioning used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_MBW_MAX_ns) accesses the memory maximum bandwidth partitioning used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_MBW_MAX access the memory maximum bandwidth partitioning configuration settings for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_MBW_MAX access the memory maximum bandwidth partitioning configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_MBW_MAX access the memory maximum bandwidth partitioning configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_MBW_MAX access the memory maximum bandwidth partitioning configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

MPAMCFG_MBW_MAX can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0208</td>
<td>MPAMCFG_MBW_MAX_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0208</td>
<td>MPAMCFG_MBW_MAX_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The MPAMCFG_MBW_MIN characteristics are:

**Purpose**

MPAMCFG_MBW_MIN is a 32-bit read-write register that controls the minimum fraction of memory bandwidth that the PARTID selected by MPAMCFG_PART_SEL is permitted to use. MPAMCFG_MBW_MIN_s controls the minimum bandwidth for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_MBW_MIN_ns controls the minimum bandwidth for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

A PARTID that has used less than MIN is given preferential access to bandwidth.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_MBW_MIN is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MBW_PART == 1 and MPAMF_MBW_IDR.HAS_MIN == 1. Otherwise, direct accesses to MPAMCFG_MBW_MIN are RES0.

**Attributes**

MPAMCFG_MBW_MIN is a 32-bit register.

**Field descriptions**

The MPAMCFG_MBW_MIN bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | MIN |

**Bits [31:16]**

Reserved, RES0.

**MIN, bits [15:0]**

Memory minimum bandwidth allocated to the partition selected by MPAMCFG_PART_SEL. MIN is in fixed-point fraction format. The fraction represents the portion of the total memory bandwidth capacity through the controlled component that the PARTID is permitted to allocate.

The implemented width of the fixed-point fraction is given in MPAMF_MBW_IDR.BWA WD. Unimplemented bits are RAZ/WI. The implemented bits of the MIN field are always to the left of the field. For example, if BWA WD = 4, the implemented bits are MPAMCFG_MBW_MIN[15:12] and MPAMCFG_MBW_MIN[11:0] are unimplemented.

The fixed-point fraction MIN is less than 1. The implied binary point is between bits 15 and 16. This representation has as the largest fraction of the bandwidth that can be represented in an implementation with w implemented bits is 1 - 1/w.
Accessing the MPAMCFG_MBW_MIN

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_MBW_MIN_s must be accessible from the Secure MPAM feature page. MPAMCFG_MBW_MIN_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_MBW_MIN_s and MPAMCFG_MBW_MIN_ns must be separate registers. The Secure instance (MPAMCFG_MBW_MIN_s) accesses the memory minimum bandwidth partitioning used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_MBW_MIN_ns) accesses the memory minimum bandwidth partitioning used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_MBW_MIN access the memory minimum bandwidth partitioning configuration settings for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_MBW_MIN access the memory minimum bandwidth partitioning configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_MBW_MIN access the memory minimum bandwidth partitioning configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_MBW_MIN access the memory minimum bandwidth partitioning configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

MPAMCFG_MBW_MIN can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0200</td>
<td>MPAMCFG_MBW_MIN_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0200</td>
<td>MPAMCFG_MBW_MIN_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
The MPAMCFG_MBW_PBM<n> characteristics are:

**Purpose**

The MPAMCFG_MBW_PBM<n> register array gives access to the memory bandwidth portion bitmap. Each register in the array is a read-write register that configures the bandwidth portions \(32 \times n\) to \((32 \times n) + 31\) that a PARTID is allowed to allocate.

After setting MPAMCFG_PART_SEL with a PARTID, software writes to one or more of the MPAMCFG_MBW_PBM<n> registers to configure which bandwidth portions the PARTID is allowed to allocate.

The MPAMCFG_MBW_PBM<n> register that contains the bitmap bit corresponding to memory bandwidth portion \(p\) has \(n\) equal to \(p[11:5]\). The field, \(P<\times + (32 \times n)>\) of that MPAMCFG_MBW_PBM<n> register that contain the bitmap bit corresponding to memory bandwidth portion \(p\) has \(x\) equal to \(p[4:0]\).

The MPAMCFG_MBW_PBM<n>_s registers control the bandwidth portion bitmap for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. The MPAMCFG_MBW_PBM<n>_ns registers control the bandwidth portion bitmap for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_MBW_PBM<n> is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MBW_PART == 1 and MPAMF_MBW_IDR.HAS_PBM == 1. Otherwise, direct accesses to MPAMCFG_MBW_PBM<n> are RES0.

**Attributes**

MPAMCFG_MBW_PBM<n> is a 32-bit register.

**Field descriptions**

The MPAMCFG_MBW_PBM<n> bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>(P&lt;32 \times n + 31&gt;)</td>
<td>(P&lt;32 \times n + 30&gt;)</td>
<td>(P&lt;32 \times n + 29&gt;)</td>
<td>(P&lt;32 \times n + 28&gt;)</td>
<td>(P&lt;32 \times n + 27&gt;)</td>
<td>(P&lt;32 \times n + 26&gt;)</td>
<td>(P&lt;32 \times n + 25&gt;)</td>
</tr>
</tbody>
</table>

\(P<\times + (32 \times n)>, \text{ bit } [x]\), for \(x = 31 \text{ to } 0\)

Portion allocation control bit. Each bandwidth portion allocation control bit MPAMCFG_MBW_PBM<n>.P<<\(\times + (32 \times n)\)> grants permission to the PARTID selected by MPAMCFG_PART_SEL to allocate bandwidth within bandwidth portion \(\times + (32 \times n)\).

<table>
<thead>
<tr>
<th>(P&lt;\times + (32 \times n)&gt;)</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The PARTID is not permitted to allocate into bandwidth portion (\times + (32 \times n)).</td>
</tr>
<tr>
<td>0b1</td>
<td>The PARTID is permitted to allocate within bandwidth portion (\times + (32 \times n)).</td>
</tr>
</tbody>
</table>

The number of bits in the bandwidth portion partitioning bit map of this component is given in MPAMF_MBW_IDR.BWPBM_WD. BWPBM_WD contains a value from 1 to \(2^{12}\), inclusive. Values of BWPBM_WD greater than 32 require a group of 32-bit registers to access the bandwidth portion bitmap, up to 128 32-bit registers.
Bits MPAMCFG_MBW_PBM<n>.P<x + (32 * n)>, where <x + (32 * n)> is greater than or equal to BWPBM_WD are RES0:

- If n > MPAMF_MBW_IDR.BWPBM_WD[11:5], the entire 32 P<x> are RES0.
- If n == MPAMF_MBW_IDR.BWPBM_WD[11:5], bits [31: BWPBM_WD[4:0]] are RES0 and the remaining bits are valid.
- If n < MPAMF_MBW_IDR.BWPBM_WD[11:5], the entire 32 P<x> are valid.

**Accessing the MPAMCFG_MBW_PBM<n>**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_MBW_PBM<n>_s must be accessible from the Secure MPAM feature page. MPAMCFG_MBW_PBM<n>_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_MBW_PBM<n>_s and MPAMCFG_MBW_PBM<n>_ns must be separate registers. The Secure instance (MPAMCFG_MBW_PBM<n>_s) accesses the memory bandwidth portion bitmap used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_MBW_PBM<n>_ns) accesses the memory bandwidth portion bitmap used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_MBW_PBM<n> access the memory bandwidth portion bitmap configuration settings for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_MBW_PBM<n> access the memory bandwidth portion bitmap configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_MBW_PBM<n> access the memory bandwidth portion bitmap configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_MBW_PBM<n> access the memory bandwidth portion bitmap configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

**MPAMCFG_MBW_PBM<n> can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x2000 + (4 * n)</td>
<td>MPAMCFG_MBW_PBM&lt;n&gt;_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x2000 + (4 * n)</td>
<td>MPAMCFG_MBW_PBM&lt;n&gt;_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

30/09/2020 15:07; cceed0cb9f089f9ceec50268e82aec9e71047211

Copyright © 2010-2020 Arm Limited or its affiliates. All rights reserved. This document is Non-Confidential.
The MPAMCFG_MBW_PROP characteristics are:

**Purpose**

Controls the proportional stride of memory bandwidth that the PARTID selected by MPAMCFG_PART_SEL uses. MPAMCFG_MBW_PROP selects the bandwidth proportional stride for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_MBW_PROP ns selects the bandwidth proportional stride for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

Proportional stride is a relative cost of bandwidth requested by one PARTID in relation to the costs of the bandwidths requested by each other PARTID also competing to use the bandwidth.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_MBW_PROP is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MBW_PART == 1 and MPAMF_MBW_IDR.HAS_PROP == 1. Otherwise, direct accesses to MPAMCFG_MBW_PROP are RES0.

**Attributes**

MPAMCFG_MBW_PROP is a 32-bit register.

**Field descriptions**

The MPAMCFG_MBW_PROP bit assignments are:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>RES0</td>
<td>STRIDEM1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**EN, bit [31]**

Enable proportional stride bandwidth partitioning.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The selected partition is not regulated by proportional stride bandwidth partitioning.</td>
</tr>
<tr>
<td>0b1</td>
<td>The selected partition has bandwidth usage regulated by proportional stride bandwidth partitioning as controlled by STRIDEM1.</td>
</tr>
</tbody>
</table>

**Bits [30:16]**

Reserved, RES0.

**STRIDEM1, bits [15:0]**

Memory bandwidth stride minus 1 allocated to the partition selected by MPAMCFG_PART_SEL. STRIDEM1 represents the normalized cost of bandwidth consumption by the partition.
The proportional stride partitioning control parameter is an unsigned integer representing the normalized cost to a partition for consuming bandwidth. Larger values have a larger cost and correspond to a lesser allocation of bandwidth while smaller values indicate a lesser cost and therefore a higher allocation of bandwidth.

The implemented width of STRIDEM1 is given in MPAMF_MBW_IDR.BWA_WD.

**Accessing the MPAMCFG_MBW_PROP**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_MBW_PROP_s must be accessible from the Secure MPAM feature page. MPAMCFG_MBW_PROP_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_MBW_PROP_s and MPAMCFG_MBW_PROP_ns must be separate registers. The Secure instance (MPAMCFG_MBW_PROP_s) accesses the memory proportional stride bandwidth partitioning used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_MBW_PROP_ns) accesses the memory proportional stride bandwidth partitioning used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_MBW_PROP access the memory proportional stride bandwidth partitioning configuration settings for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_MBW_PROP access the memory proportional stride bandwidth partitioning configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_MBW_PROP access the memory proportional stride bandwidth partitioning configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_MBW_PROP access the memory proportional stride bandwidth partitioning configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

**MPAMCFG_MBW_PROP can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0500</td>
<td>MPAMCFG_MBW_PROP_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0500</td>
<td>MPAMCFG_MBW_PROP_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
The MPAMCFG_MBW_WINWD characteristics are:

**Purpose**

MPAMCFG_MBW_WINWD is a 32-bit register that shows and sets the value of the window width for the PARTID in MPAMCFG_PART_SEL. MPAMCFG_MBW_WINWD reads and controls the bandwidth control window width for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_MBW_WINWD ns reads and controls the bandwidth control window for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

MPAMCFG_MBW_WINWD is read-only if MPAMF_MBW_IDR.WINDWR == 0, and the window width is set by the hardware, even if variable.

MPAMCFG_MBW_WINWD is read-write if MPAMF_MBW_IDR.WINDWR == 1, permitting configuration of the window width for each PARTID independently on hardware that supports this functionality.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_MBW_WINWD is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_MBW_PART == 1. Otherwise, direct accesses to MPAMCFG_MBW_WINWD are RES0.

**Attributes**

MPAMCFG_MBW_WINWD is a 32-bit register.

**Field descriptions**

The MPAMCFG_MBW_WINWD bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | US_INT | US_FRAC |

**Bits [31:24]**

Reserved, RES0.

**US_INT, bits [23:8]**

Window width, integer microseconds.

This field reads (and sets) the integer part of the window width in microseconds for the PARTID selected by MPAMCFG_PART_SEL.

**US_FRAC, bits [7:0]**

Window width, fractional microseconds.

This field reads (and sets) the fractional part of the window width in microseconds for the PARTID selected by MPAMCFG_PART_SEL.
**Accessing the MPAMCFG_MBW_WINWD**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_MBW_WINWD_s must be accessible from the Secure MPAM feature page. MPAMCFG_MBW_WINWD_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_MBW_WINWD_s and MPAMCFG_MBW_WINWD_ns must be separate registers. The Secure instance (MPAMCFG_MBW_WINWD_s) accesses the window width used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_MBW_WINWD_ns) accesses the window width used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_MBW_WINWD access the window width configuration settings for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_MBW_WINWD access the window width configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_MBW_WINWD access the window width configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_MBW_WINWD access the window width configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

**MPAMCFG_MBW_WINWD can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0220</td>
<td>MPAMCFG_MBW_WINWD_s</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When MPAMF_MBW_IDR.WINDWR == 0 accesses to this register are **RO**.
- Otherwise accesses to this register are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0220</td>
<td>MPAMCFG_MBW_WINWD_ns</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When MPAMF_MBW_IDR.WINDWR == 0 accesses to this register are **RO**.
- Otherwise accesses to this register are **RW**.
The MPAMCFG_PART_SEL characteristics are:

**Purpose**

Selects a partition ID to configure. MPAMCFG_PART_SEL_s selects a Secure PARTID to configure. MPAMCFG_PART_SEL_ns selects a Non-secure PARTID to configure.

After setting this register with a PARTID, software (usually a hypervisor) can perform a series of accesses to MPAMCFG registers to configure parameters for MPAM resource controls to use when requests have that PARTID.

**Configuration**

The power domain of MPAMCFG_PART_SEL is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and (MPAMF_IDR.HAS_CCAP_PART == 1, or MPAMF_IDR.HAS_CPOR_PART == 1, or MPAMF_IDR.HAS_MBW_PART == 1, or MPAMF_IDR.HAS_PRI_PART == 1, or MPAMF_IDR.HAS_PARTID_NRW == 1, or (MPAMF_IDR.EXT == 0 and MPAMF_IDR.HAS_IMPL_IDR == 1) or (MPAMF_IDR.EXT == 1, MPAMF_IDR.HAS_IMPL_IDR == 1 and MPAMF_IDR.NO_IMPL_PART == 0)). Otherwise, direct accesses to MPAMCFG_PART_SEL are RES0.

**Attributes**

MPAMCFG_PART_SEL is a 32-bit register.

**Field descriptions**

The MPAMCFG_PART_SEL bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | RIS | RES0 | INTERNAL | PARTID_SEL |

**Bits [31:28]**

Reserved, RES0.

**RIS, bits [27:24]**

When (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented), MPAMF_IDR.EXT == 1 and MPAMF_IDR.HAS_RIS == 1:

Resource Instance Selector. RIS selects one resource to configure through MPAMCFG registers and describe with MPAMF ID registers.

Otherwise:

Reserved, RES0.

**Bits [23:17]**

Reserved, RES0.
INTERNAL, bit [16]

Internal PARTID.

If `MPAMF_IDR.HAS_PARTID_NRW = 0`, this field is RAZ/WI.

If `MPAMF_IDR.HAS_PARTID_NRW = 1`:

<table>
<thead>
<tr>
<th>INTERNAL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PARTID_SEL is interpreted as a request PARTID and ignored except for use with <code>MPAMCFG_INTPARTID</code> register access.</td>
</tr>
<tr>
<td>0b1</td>
<td>PARTID_SEL is interpreted as an internal PARTID and used for access to MPAMCFG control settings except for <code>MPAMCFG_INTPARTID</code>.</td>
</tr>
</tbody>
</table>

If PARTID narrowing is implemented as indicated by `MPAMF_IDR.HAS_PARTID_NRW = 1`, when accessing other MPAMCFG registers the value of the `MPAMCFG_PART_SEL.INTERNAL` bit is checked for these conditions:

- When the `MPAMCFG_INTPARTID` register is read or written, if the value of `MPAMCFG_PART_SEL.INTERNAL` is not 0, an Unexpected_INTERNAL error is set in `MPAMF_ESR`.
- When an MPAMCFG register other than `MPAMCFG_INTPARTID` is read or written, if the value of `MPAMCFG_PART_SEL.INTERNAL` is not 1, `MPAMF_ESR` is set to indicate an intPARTID_Range error.

In either error case listed here, the value returned by a read operation is UNPREDICTABLE, and the control settings are not affected by a write.

PARTID_SEL, bits [15:0]

Selects the partition ID to configure.

Reads and writes to other MPAMCFG registers are indexed by PARTID_SEL and by the NS bit used to access `MPAMCFG_PART_SEL` to access the configuration for a single partition.

Accessing the MPAMCFG_PART_SEL

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

`MPAMCFG_PART_SEL_s` must be accessible from the Secure MPAM feature page. `MPAMCFG_PART_SEL_ns` must be accessible from the Non-secure MPAM feature page.

`MPAMCFG_PART_SEL_s` and `MPAMCFG_PART_SEL_ns` must be separate registers. The Secure instance (`MPAMCFG_PART_SEL_s`) accesses the PARTID selector used for Secure PARTIDs, and the Non-secure instance (`MPAMCFG_PART_SEL_ns`) accesses the PARTID selector used for Non-secure PARTIDs.

**MPAMCFG_PART_SEL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0100</td>
<td>MPAMCFG_PART_SEL_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0100</td>
<td>MPAMCFG_PART_SEL_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
MPAMCFG_PRI, MPAM Priority Partition Configuration Register

The MPAMCFG_PRI characteristics are:

**Purpose**

Controls the internal and downstream priority of requests attributed to the PARTID selected by MPAMCFG_PART_SEL. MPAMCFG_PRI controls the priorities for the Secure PARTID selected by the Secure instance of MPAMCFG_PART_SEL. MPAMCFG_PRI_ns controls the priorities for the Non-secure PARTID selected by the Non-secure instance of MPAMCFG_PART_SEL.

If MPAMF_IDR.HAS_RIS is 1, the control settings accessed are those of the resource instance currently selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

**Configuration**

The power domain of MPAMCFG_PRI is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_PRI_PART == 1. Otherwise, direct accesses to MPAMCFG_PRI are RES0.

**Attributes**

MPAMCFG_PRI is a 32-bit register.

**Field descriptions**

The MPAMCFG_PRI bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|   | DSPRI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|   | INTPRI | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**DSPRI, bits [31:16]**

Downstream priority.

If MPAMF_PRI_IDR.HAS_DSPRI == 0, bits of this field are RES0 as this field is not used.

If MPAMF_PRI_IDR.HAS_DSPRI == 1, this field is a priority value applied to downstream communications from this MSC for transactions of the partition selected by MPAMCFG_PART_SEL.

The implemented width of this field is MPAMF_PRI_IDR_DSPRI_WD bits. If the implemented width is less than the width of this field, the least significant bits are used.

The encoding of priority is 0-as-lowest or 0-as-highest priority according to the value of MPAMF_PRI_IDR_DSPRI_0_IS_LOW.

**INTPRI, bits [15:0]**

Internal priority.

If MPAMF_PRI_IDR.HAS_INTPRI == 0, bits of this field are RES0 as this field is not used.

If MPAMF_PRI_IDR.HAS_INTPRI == 1, this field is a priority value applied internally inside this MSC for transactions of the partition selected by MPAMCFG_PART_SEL.

The implemented width of this field is MPAMF_PRI_IDR_INTPRI_WD bits. If the implemented width is less than the width of this field, the least significant bits are used.
The encoding of priority is 0-as-lowest or 0-as-highest priority according to the value of MPAMF_PRI_IDR.INTPRI_0 IS_LOW.

Accessing the MPAMCFG_PRI

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMCFG_PRI_s must be accessible from the Secure MPAM feature page. MPAMCFG_PRI_ns must be accessible from the Non-secure MPAM feature page.

MPAMCFG_PRI_s and MPAMCFG_PRI_ns must be separate registers. The Secure instance (MPAMCFG_PRI_s) accesses the priority partitioning used for Secure PARTIDs, and the Non-secure instance (MPAMCFG_PRI_ns) accesses the priority partitioning used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MPAMCFG_PRI access the priority partitioning configuration settings for the priority resource instance selected by MPAMCFG_PART_SEL.RIS and the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When RIS is not implemented, loads and stores to MPAMCFG_PRI access the priority partitioning configuration settings for the PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL.

When PARTID narrowing is implemented, loads and stores to MPAMCFG_PRI access the priority partitioning configuration settings for the internal PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 1.

When PARTID narrowing is not implemented, loads and stores to MPAMCFG_PRI access the priority partitioning configuration settings for the request PARTID selected by MPAMCFG_PART_SEL.PARTID_SEL, and MPAMCFG_PART_SEL.INTERNAL must be 0.

MPAMCFG_PRI can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0400</td>
<td>MPAMCFG_PRI_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0400</td>
<td>MPAMCFG_PRI_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
MPAMF_AIDR, MPAM Architecture Identification Register

The MPAMF_AIDR characteristics are:

**Purpose**

Identifies the version of the MPAM architecture that this MSC implements.

Note: The following values are defined for bits [7:0]:

- $0x01 == MPAM architecture v0.1$
- $0x10 == MPAM architecture v1.0$
- $0x11 == MPAM architecture v1.1$

**Configuration**

The power domain of MPAMF_AIDR is **IMPLEMENTATION DEFINED**.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_AIDR are **RES0**.

**Attributes**

MPAMF_AIDR is a 32-bit register.

**Field descriptions**

The MPAMF_AIDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    | RES0 |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | ArchMajorRev | ArchMinorRev |

**Bits [31:8]**

Reserved, RES0.

**ArchMajorRev, bits [7:4]**

Major revision of the MPAM architecture implemented by the MSC.

This table shows the only valid combinations of MPAM version numbers in an MSC. FORCE_NS functionality is only available in MPAM v0.1.

<table>
<thead>
<tr>
<th>ArchMajorRev</th>
<th>ArchMinorRev</th>
<th>MPAMv</th>
<th>Available</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>v0.1</td>
<td>None.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>v0.1</td>
<td>MPAMv1.0 + MPAMv1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>+ FORCE_NS</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>v1.0</td>
<td>MPAMv1.0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>v1.1</td>
<td>MPAMv1.0 + MPAMv1.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>- FORCE_NS</td>
</tr>
</tbody>
</table>

Use of MPAMv0.1 in MSCs is restricted to limited circumstances. The MSC must be able to initiate requests in the secure address space which have MPAM PARTID forced to the Non-secure space with that forcing not controllable or observable by the software that configures the the device for Secure requests. Please contact Arm before setting MPAMF_AIDR to report MPAMv0.1.
**ArchMinorRev, bits [3:0]**

Minor revision of the MPAM architecture implemented by the MSC.

See the table in the description of the ArchMajorRev field in this register.

**Accessing the MPAMF_AIDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_AIDR is read-only.

MPAMF_AIDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_AIDR must have the same contents in the Secure and Non-secure MPAM feature pages.

**MPAMF_AIDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0020</td>
<td>MPAMF_AIDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0020</td>
<td>MPAMF_AIDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The MPAMF_CCAP_IDR characteristics are:

**Purpose**

Indicates the number of fractional bits in MPAMCFG_CMAX.CMAX. MPAMF_CCAP_IDR_s indicates the number of fractional bits in the Secure instance of MPAMCFG_CMAX. MPAMF_CCAP_IDR_ns indicates the number of fractional bits in the Non-secure instance of MPAMCFG_CMAX.

When MPAMF_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selected by MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has information within the field description.

**Configuration**

The power domain of MPAMF_CCAP_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_CCAP_PART == 1. Otherwise, direct accesses to MPAMF_CCAP_IDR are RES0.

**Attributes**

MPAMF_CCAP_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_CCAP_IDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>CMAX_WD</td>
</tr>
</tbody>
</table>

**Bits [31:6]**

Reserved, RES0.

**CMAX_WD, bits [5:0]**

Number of fractional bits implemented in the cache capacity partitioning control, MPAMCFG_CMAX.CMAX, of this device. See MPAMCFG_CMAX.

This field must contain a value from 1 to 16, inclusive.

If RIS is implemented, this field indicates the number of fractional bits in the cache capacity partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Accessing the MPAMF_CCAP_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_CCAP_IDR is read-only.

MPAMF_CCAP_IDR must be readable from the Non-secure and Secure MPAM feature pages.
MPAMF_CCAP_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_CCAP_IDR_s) and Non-secure (MPAMF_CCAP_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_CCAP_IDR shows the configuration of cache capacity partitioning for the cache resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_CCAP_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0038</td>
<td>MPAMF_CCAP_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0038</td>
<td>MPAMF_CCAP_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
MPAMF_CPOR_IDR, MPAM Features Cache Portion Partitioning ID register

The MPAMF_CPOR_IDR characteristics are:

**Purpose**

Indicates the number of bits in MPAMCFG_CPB<n>. MPAMF_CPOR_IDRs indicates the number of bits in the Secure instance of MPAMCFG_CPB<n>. MPAMF_CPOR_IDRns indicates the number of bits in the Non-secure instance of MPAMCFG_CPB<n>.

When MPAMF_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selector, MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has information within the field description.

**Configuration**

The power domain of MPAMF_CPOR_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_CPOR_PART == 1. Otherwise, direct accesses to MPAMF_CPOR_IDR are RES0.

**Attributes**

MPAMF_CPOR_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_CPOR_IDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| CPBM WD | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

**Bits [31:16]**

Reserved, RES0.

**CPBM WD, bits [15:0]**

Number of bits in the cache portion partitioning bit map of this device. See MPAMCFG_CPB<n>.

This field must contain a value from 1 to 32768, inclusive. Values greater than 32 require a group of 32-bit registers to access the CPBM, up to 1024 if CPBM WD is the largest value.

If RIS is implemented, this field indicates the number bits in the cache portion bitmap for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Accessing the MPAMF_CPOR_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_CPOR_IDR is read-only.

MPAMF_CPOR_IDR must be readable from the Non-secure and Secure MPAM feature pages.
MPAMF_CPOR_IDR, MPAM Features Cache Portion Partitioning ID register

MPAMF_CPOR_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_CPOR_IDR_s) and Non-secure (MPAMF_CPOR_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_CPOR_IDR shows the configuration of cache portion partitioning for the cache resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_CPOR_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0030</td>
<td>MPAMF_CPOR_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0030</td>
<td>MPAMF_CPOR_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
MPAMF_CSUMON_IDR, MPAM Features Cache Storage Usage Monitoring ID register

The MPAMF_CSUMON_IDR characteristics are:

Purpose

Indicates the number of cache storage usage monitor instances and other properties of the CSU monitoring. MPAMF_CSUMON_IDR_s indicates the number and properties of Secure cache storage usage monitoring. MPAMF_CSUMON_IDR_ns indicates the number and properties of Non-secure cache storage usage monitoring.

If MPAMF_IDR.HAS_RIS is 1, fields that mention RIS must reflect the properties of the resource instance currently selected by MPAMCFG_PART_SEL.RIS. Fields that do not mention RIS are constant across all resource instances.

Configuration

The power domain of MPAMF_CSUMON_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_CSU == 1. Otherwise, direct accesses to MPAMF_CSUMON_IDR are RES0.

Attributes

MPAMF_CSUMON_IDR is a 32-bit register.

Field descriptions

The MPAMF_CSUMON_IDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| HAS_CAPTURE | CSU_RO | RES0 | NUM_MON |

HAS_CAPTURE, bit [31]

The implementation supports copying an MSMON_CSU to the corresponding MSMON_CSU_CAPTURE on a capture event.

<table>
<thead>
<tr>
<th>HAS_CAPTURE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_CSU_CAPTURE is not implemented and there is no support for capture events in the CSU monitor.</td>
</tr>
<tr>
<td>0b1</td>
<td>The MSMON_CSU_CAPTURE register is implemented and the CSU monitor supports the capture event behavior.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that CSU monitor capture is implemented for the resource instance selected by MPAMCFG_PART_SEL.RIS.

CSU_RO, bit [30]

The implementation of MSMON_CSU is read-only.

<table>
<thead>
<tr>
<th>CSU_RO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_CSU is read-write.</td>
</tr>
<tr>
<td>0b1</td>
<td>MSMON_CSU is read-only.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that the MSMON_CSU monitor register is read-only for the resource instance selected by MPAMCFG_PART_SEL.RIS.
Bits [29:16]

Reserved, RES0.

**NUM_MON, bits [15:0]**

The number of cache storage usage monitor instances implemented.

The largest **MSMON_CFG_MON_SEL**.MON_SEL value is NUM_MON minus 1.

If RIS is implemented, this field indicates the number of CSU monitor instances implemented for the resource instance selected by **MPAMCFG_PART_SEL**.RIS.

**Accessing the MPAMF_CSUMON_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_CSUMON_IDR is read-only.

MPAMF_CSUMON_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_CSUMON_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_CSUMON_IDR_s) and Non-secure (MPAMF_CSUMON_IDR_ns) MPAM feature pages.

When **MPAMF_IDR**.HAS_RIS is 1, MPAMF_CSUMON_IDR shows the configuration of cache storage usage monitoring for the cache resource instance selected by **MPAMCFG_PART_SEL**.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

Access to MPAMF_CSUMON_IDR is not affected by **MSMON_CFG_MON_SEL**.RIS.

**MPAMF_CSUMON_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0088</td>
<td>MPAMF_CSUMON_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0088</td>
<td>MPAMF_CSUMON_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
MPAMF_ECR, MPAM Error Control Register

The MPAMF_ECR characteristics are:

**Purpose**

MPAMF_ECR is a 32-bit read-write register that controls MPAM error interrupts for this MSC. MPAMF_ECR_s controls Secure MPAM error handling. MPAMF_ECR_ns controls Non-secure MPAM error handling.

**Configuration**

The power domain of MPAMF_ECR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_ECR are RES0.

If a MSC cannot encounter any of the error conditions listed in section 15.1, both the MPAMF_ESR and MPAMF_ECR must be RAZ/WI.

**Attributes**

MPAMF_ECR is a 32-bit register.

**Field descriptions**

The MPAMF_ECR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>INTEN</td>
</tr>
<tr>
<td>28</td>
<td>Interrupt Enable.</td>
</tr>
<tr>
<td>27</td>
<td>MPAM error interrupts are not generated.</td>
</tr>
<tr>
<td>26</td>
<td>MPAM error interrupts are generated.</td>
</tr>
</tbody>
</table>

**Accessing the MPAMF_ECR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_ECR_s must be accessible from the Secure MPAM feature page. MPAMF_ECR_ns must be accessible from the Non-secure MPAM feature page.

MPAMF_ECR_s and MPAMF_ECR_ns must be separate registers. The Secure instance (MPAMF_ECR_s) accesses the error interrupt controls used for Secure PARTIDs, and the Non-secure instance (MPAMF_ECR_ns) accesses the error interrupt controls used for Non-secure PARTIDs.

**MPAMF_ECR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>
Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x00F0</td>
<td>MPAMF_ECR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
The MPAMF_ESR characteristics are:

**Purpose**

Indicates MPAM error status for this MSC. MPAMF_ESR_s reports Secure MPAM errors. MPAMF_ESR_ns reports Non-secure MPAM errors.

Software should write this register after reading the status of an error to reset ERRCODE to 0x0000 and OVRWR to 0 so that future errors are not reported with OVRWR set.

**Configuration**

The power domain of MPAMF_ESR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_ESR are RES0.

MAMPF_ESR is 64-bit register when MPAM v0.1 or v1.1 is implemented and MPAMF_IDR.HAS_EXTD_ESR == 1.

Otherwise, MAMPF_ESR is a 32-bit register.

If a MSC cannot encounter any of the error conditions listed in 'Errors in MSCs' in Arm® Architecture Reference Manual Supplement, Memory System Resource Partitioning and Monitoring (MPAM), for Armv8-A (ARM DDI 0598), both the MPAMF_ESR and MPAMF_ECR must be RAZ/WI.

**Attributes**

MPAMF_ESR is a:

- 64-bit register when (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented) and MPAMF_IDR.HAS_EXTD_ESR == 1
- 32-bit register otherwise

**Field descriptions**

The MPAMF_ESR bit assignments are:

**When (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented) and MPAMF_IDR.HAS_EXTD_ESR == 1:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>35</td>
<td>Resource Instance Selector. Where applicable to the ERRCODE, captures the RIS value for the error.</td>
</tr>
</tbody>
</table>

**Bits [63:36]**

Reserved, RES0.

**RIS, bits [35:32]**

When MPAMF_IDR.HAS_RIS == 1:

Resource Instance Selector. Where applicable to the ERRCODE, captures the RIS value for the error.
Otherwise:

Reserved, RES0.

OVRWR, bit [31]

Overwritten.

If 0 and ERRCODE == 0b0000, no errors have occurred.

If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register.

If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error.

The state where this bit is 1 and ERRCODE is zero must not be produced by hardware and is only reached when software writes this combination into this register.

Bits [30:28]

Reserved, RES0.

ERRCODE, bits [27:24]

Error code.

<table>
<thead>
<tr>
<th>ERRCODE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No error.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PARTID_SEL_Range.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Req_PARTID_Range.</td>
</tr>
<tr>
<td>0b0011</td>
<td>MSMONCFG_ID_RANGE.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Req_PMG_Range.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Monitor.Range.</td>
</tr>
<tr>
<td>0b0110</td>
<td>intPARTID_Range.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Unexpected_INTERNAL.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Undefined_RIS_PART_SEL.</td>
</tr>
<tr>
<td>0b1001</td>
<td>RIS_No_Control.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Undefined_RIS_MON_SEL.</td>
</tr>
<tr>
<td>0b1011</td>
<td>RIS_No_Monitor.</td>
</tr>
<tr>
<td>0b1100</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1101</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

PMG, bits [23:16]

Program monitoring group.

Set to the PMG on an error that captures PMG. Otherwise, set to 0x00 on an error that does not capture PMG.

PARTID_MON, bits [15:0]

PARTID or monitor.

Set to the PARTID on an error that captures PARTID.

Set to the monitor index on an error that captures MON.

On an error that captures neither PARTID nor MON, this field is set to 0.

Otherwise:
MPAMF_ESR, MPAM Error Status Register

OVRWR, bit [31]

Overwritten.

If 0 and ERRCODE == 0b0000, no errors have occurred.

If 0 and ERRCODE is non-zero, a single error has occurred and is recorded in this register.

If 1 and ERRCODE is non-zero, multiple errors have occurred and this register records the most recent error.

The state where this bit is 1 and ERRCODE is 0 must not be produced by hardware and is only reached when software writes this combination into this register.

Bits [30:28]

Reserved, RES0.

ERRCODE, bits [27:24]

Error code.

<table>
<thead>
<tr>
<th>ERRCODE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>No error.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PARTID_SEL Range.</td>
</tr>
<tr>
<td>0b0010</td>
<td>Req_PARTID Range.</td>
</tr>
<tr>
<td>0b0011</td>
<td>MSMONCFG_ID_RANGE.</td>
</tr>
<tr>
<td>0b0100</td>
<td>Req_PMG Range.</td>
</tr>
<tr>
<td>0b0101</td>
<td>Monitor Range.</td>
</tr>
<tr>
<td>0b0110</td>
<td>intPARTID Range.</td>
</tr>
<tr>
<td>0b0111</td>
<td>Unexpected_INTERNAL.</td>
</tr>
<tr>
<td>0b1000</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1001</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1010</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1011</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1100</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1101</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1110</td>
<td>Reserved.</td>
</tr>
<tr>
<td>0b1111</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

PMG, bits [23:16]

Program monitoring group.

Set to the PMG on an error that captures PMG. Otherwise, set to 0x00 on an error that does not capture PMG.

PARTID_MON, bits [15:0]

PARTID or monitor.

Set to the PARTID on an error that captures PARTID.

Set to the monitor index on an error that captures MON.

On an error that captures neither PARTID nor MON, this field is set to 0x0000.

Accessing the MPAMF_ESR

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_ESR_s must be accessible from the Secure MPAM feature page. MPAMF_ESR_ns must be accessible from the Non-secure MPAM feature page.
MPAMF_ESR_s and MPAMF_ESR_ns must be separate registers. The Secure instance (MPAMF_ESR_s) accesses the error status used for Secure PARTIDs, and the Non-secure instance (MPAMF_ESR_ns) accesses the error status used for Non-secure PARTIDs.

**MPAMF_ESR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x00F8</td>
<td>MPAMF_ESR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x00F8</td>
<td>MPAMF_ESR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
MPAMF_IDR, MPAM Features Identification Register

The MPAMF_IDR characteristics are:

**Purpose**

Indicates which memory partitioning and monitoring features are present on this MSC. MPAMF_IDR_s indicates the MPAM features accessed from the Secure MPAM feature page. MPAMF_IDR_ns indicates the MPAM features accessed from the Non-secure MPAM feature page.

When MPAMF_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selected by MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has that information within the field description.

**Configuration**

The power domain of MPAMF_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_IDR are RES0.

MAMPF_IDR is 64-bit register when MPAM v0.1 or v1.1 is implemented.

Otherwise, MAMPF_IDR is a 32-bit register.

**Attributes**

MPAMF_IDR is a:

- 64-bit register when FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented
- 32-bit register otherwise

**Field descriptions**

The MPAMF_IDR bit assignments are:

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>HAS_PARTID_NRWM</td>
<td>HAS_MSMON</td>
<td>HAS_IMPL_IDR</td>
<td>EXT</td>
<td>HAS_PRI_PART</td>
<td>HAS_MBW_PART</td>
<td>HAS_CPOR_PART</td>
<td>HAS_CCAP_PART</td>
<td>PMG_MAX</td>
<td>PARTID_MAX</td>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
</tr>
</tbody>
</table>

Bits [63:60]

Reserved, RES0.

**RIS_MAX, bits [59:56]**

When MPAMF_IDR.EXT == 1 and MPAMF_IDR.HAS_RIS == 1:

Maximum RIS value supported in MPAMCFG_PART_SEL. Must be 0b0000 if MPAMF_IDR.HAS_RIS == 0.

Otherwise:

Reserved, RES0.
Bits [55:40]
Reserved, RES0.

HAS_ESR, bit [39]

When MPAMF_IDR.EXT == 1:

**MPAMF_ESR** is implemented.

<table>
<thead>
<tr>
<th>HAS_ESR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAMF_ESR, MPAMF_ECR</strong>, and MPAM error handling are not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAMF_ESR, MPAMF_ECR</strong>, and MPAM error handling are implemented.</td>
</tr>
</tbody>
</table>

Otherwise:
Reserved, RES0.

HAS_EXTD_ESR, bit [38]

When MPAMF_IDR.EXT == 1:

**MPAMF_ESR** is 64 bits.

<table>
<thead>
<tr>
<th>HAS_EXTD_ESR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAMF_ESR</strong> is 32 bits.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAMF_ESR</strong> is 64 bits.</td>
</tr>
</tbody>
</table>

When **MPAMF_IDR.HAS_RIS** and **MPAMF_IDR.HAS_ESR**, this field must be 1.

Otherwise:
Reserved, RES0.

NO_IMPL_MSMON, bit [37]

When MPAMF_IDR.EXT == 1 and MPAMF_IDR.HAS_IMPL_IDR == 1:

**MPAMF_IMPL_IDR** defines no **IMPLEMENTATION DEFINED** resource monitors.

<table>
<thead>
<tr>
<th>NO_IMPL_MSMON</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><strong>MPAMF_IMPL_IDR</strong> defines at least one <strong>IMPLEMENTATION DEFINED</strong> resource monitor.</td>
</tr>
<tr>
<td>0b1</td>
<td><strong>MPAMF_IMPL_IDR</strong> does not define any <strong>IMPLEMENTATION DEFINED</strong> resource monitors.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of **IMPLEMENTATION DEFINED** resource monitors described in **MPAMF_IMPL_IDR** for the selected resource instance.

Otherwise:
Reserved, RES0.

NO_IMPL_PART, bit [36]

When MPAMF_IDR.EXT == 1 and MPAMF_IDR.HAS_IMPL_IDR == 1:

**MPAMF_IMPL_IDR** defines no **IMPLEMENTATION DEFINED** resource controls.
MPAMF_IDR, MPAM Features Identification Register

<table>
<thead>
<tr>
<th>NO_IMPL_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAMF_IMPL_IDR defines at least one IMPLEMENTATION DEFINED resource control.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAMF_IMPL_IDR does not define any IMPLEMENTATION DEFINED resource controls.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of IMPLEMENTATION DEFINED resource controls described in MPAMF_IMPL_IDR for the selected resource instance.

Otherwise:

Reserved, RES0.

**Bits [35:33]**

Reserved, RES0.

**HAS_RIS, bit [32]**

When MPAMF_IDR.EXT == 1:

Has resource instance selector. Indicates that MPAMCFG_PART_SEL contains the RIS field that selects a resource instance to control.

<table>
<thead>
<tr>
<th>HAS_RIS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAMCFG_PART_SEL does not implement the MPAMCFG_PART_SEL.RIS field or multiple resource instance support.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAMCFG_PART_SEL implements the MPAMCFG_PART_SEL.RIS field and MPAM resource instance numbers up to and including MPAMF_IDR.RIS_MAX.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

**HAS_PARTID_NRW, bit [31]**

Has PARTID narrowing.

<table>
<thead>
<tr>
<th>HAS_PARTID_NRW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have MPAMF_PARTID_NRW_IDR, MPAMCFG_INTPARTID or intPARTID mapping support.</td>
</tr>
<tr>
<td>0b1</td>
<td>Supports the MPAMF_PARTID_NRW_IDR, MPAMCFG_INTPARTID registers.</td>
</tr>
</tbody>
</table>

**HAS_MSMON, bit [30]**

Has resource monitors. Indicates whether this MSC has MPAM resource monitors.

<table>
<thead>
<tr>
<th>HAS_MSMON</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support MPAM resource monitoring by groups or MPAMF_MSMON_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Supports resource monitoring by matching a combination of PARTID and PMG. See MPAMF_MSMON_IDR.</td>
</tr>
</tbody>
</table>
HAS_IMPL_IDR, bit [29]

Has MPAM_IMPL_IDR. Indicates whether this MSC has the implementation-specific MPAM features register, MPAM_IMPL_IDR.

<table>
<thead>
<tr>
<th>HAS_IMPL_IDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have MPAM_IMPL_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAM_IMPL_IDR.</td>
</tr>
</tbody>
</table>

EXT, bit [28]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Extended MPAM_IDR.

<table>
<thead>
<tr>
<th>EXT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAM_IDR has no defined bits in [63:32]. The register is</td>
</tr>
<tr>
<td></td>
<td>effectively 32 bits.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAM_IDR has bits defined in [63:32]. The register is 64-bits.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

HAS_PRI_PART, bit [27]

Has priority partitioning. Indicates that MPAM priority partitioning is implemented and MPAM_PRI_IDR exists.

<table>
<thead>
<tr>
<th>HAS_PRI_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support priority partitioning or have</td>
</tr>
<tr>
<td></td>
<td>MPAM_PRI_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has priority partitioning and MPAM_PRI_IDR.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of priority partitioning resource controls as described in MPAM_PRI_IDR for the selected resource instance.

HAS_MBW_PART, bit [26]

Has memory bandwidth partitioning. Indicates whether this MSC implements MPAM memory bandwidth partitioning and MPAM_MBW_IDR.

<table>
<thead>
<tr>
<th>HAS_MBW_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support memory bandwidth partitioning or have</td>
</tr>
<tr>
<td></td>
<td>MPAM_MBW_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAM_MBW_IDR.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of memory bandwidth partitioning resource controls as described in MPAM_MBW_IDR for the selected resource instance.

HAS_CPOR_PART, bit [25]

Has cache portion partitioning. Indicates whether this MSC implements MPAM cache portion partitioning and MPAM_CPOR_IDR.

<table>
<thead>
<tr>
<th>HAS_CPOR_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support cache portion partitioning or have</td>
</tr>
<tr>
<td></td>
<td>MPAM_CPOR_IDR or MPAMCFG_CPBM&lt;n&gt; registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAM_CPOR_IDR and MPAMCFG_CPBM&lt;n&gt; registers.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of cache portion partitioning resource controls as described in MPAM_CPOR_IDR for the selected resource instance.
HAS_CCAP_PART, bit [24]

Has cache capacity partitioning. Indicates whether this MSC implements MPAM cache capacity partitioning and the
MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.

<table>
<thead>
<tr>
<th>HAS_CCAP_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support cache capacity partitioning or have MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of cache capacity partitioning resource controls as described in
MPAMF_CPOR_IDR for the selected resource instance.

PMG_MAX, bits [23:16]

Maximum value of Non-secure PMG supported by this component.

PARTID_MAX, bits [15:0]

Maximum value of Non-secure PARTID supported by this component.

Otherwise:

31 30 29 28 27 26 25 24 23
HAS_PARTID_NRW HAS_MSMON HAS_IMPL_IDR EXT HAS_PRI_PART HAS_MBW_PART HAS_CPOR_PART HAS_CCAP_PART

HAS_PARTID_NRW, bit [31]

Has PARTID narrowing.

<table>
<thead>
<tr>
<th>HAS_PARTID_NRW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have MPAMF_PARTID_NRW_IDR, MPAMCFG_INTPARTID or intPARTID mapping support.</td>
</tr>
<tr>
<td>0b1</td>
<td>Supports the MPAMF_PARTID_NRW_IDR, MPAMCFG_INTPARTID registers.</td>
</tr>
</tbody>
</table>

HAS_MSMON, bit [30]

Has resource monitors. Indicates whether this MSC has MPAM resource monitors.

<table>
<thead>
<tr>
<th>HAS_MSMON</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support MPAM resource monitoring by groups or MPAMF_MSMON_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Supports resource monitoring by matching a combination of PARTID and PMG. See MPAMF_MSMON_IDR.</td>
</tr>
</tbody>
</table>

HAS_IMPL_IDR, bit [29]

Has MPAMF_IMPL_IDR. Indicates whether this MSC has the implementation-specific MPAM features register, MPAMF_IMPL_IDR.

<table>
<thead>
<tr>
<th>HAS_IMPL_IDR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have MPAMF_IMPL_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_IMPL_IDR.</td>
</tr>
</tbody>
</table>
EXT, bit [28]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Extended MPAMF_IDR.

<table>
<thead>
<tr>
<th>EXT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MPAMF_IDR has no defined bits in [63:32]. The register is effectively 32 bits.</td>
</tr>
<tr>
<td>0b1</td>
<td>MPAMF_IDR has bits defined in [63:32]. The register is 64-bits.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

HAS_PRI_PART, bit [27]

Has priority partitioning. Indicates whether this MSC implements MPAM priority partitioning and MPAMF_PRI_IDR.

<table>
<thead>
<tr>
<th>HAS_PRI_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support priority partitioning or have MPAMF_PRI_IDR.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_PRI_IDR.</td>
</tr>
</tbody>
</table>

HAS_MBW_PART, bit [26]

Has memory bandwidth partitioning. Indicates whether this MSC implements MPAM memory bandwidth partitioning and MPAMF_MBW_IDR.

<table>
<thead>
<tr>
<th>HAS_MBW_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support memory bandwidth partitioning or have MPAMF_MBW_IDR register.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_MBW_IDR register.</td>
</tr>
</tbody>
</table>

HAS_CPOR_PART, bit [25]

Has cache portion partitioning. Indicates whether this MSC implements MPAM cache portion partitioning and MPAMF_CPOR_IDR.

<table>
<thead>
<tr>
<th>HAS_CPOR_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support cache portion partitioning or have MPAMF_CPOR_IDR or MPAMCFG_CPBM&lt;n&gt; registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_CPOR_IDR and MPAMCFG_CPBM&lt;n&gt; registers.</td>
</tr>
</tbody>
</table>

HAS_CCAP_PART, bit [24]

Has cache capacity partitioning. Indicates whether this MSC implements MPAM cache capacity partitioning and the MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.

<table>
<thead>
<tr>
<th>HAS_CCAP_PART</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support cache capacity partitioning or have MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has MPAMF_CCAP_IDR and MPAMCFG_CMAX registers.</td>
</tr>
</tbody>
</table>

PMG_MAX, bits [23:16]

Maximum value of Non-secure PMG supported by this component.

MPAMF_IDR, MPAM Features Identification Register
**PARTID_MAX, bits [15:0]**

Maximum value of Non-secure PARTID supported by this component.

**Accessing the MPAMF_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_IDR is read-only.

MPAMF_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_IDR_s) and Non-secure (MPAMF_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_IDR shows the configuration of MSC MPAM for the resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0000</td>
<td>MPAMF_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0000</td>
<td>MPAMF_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
MPAMF_IIDR, MPAM Implementation Identification Register

The MPAMF_IIDR characteristics are:

**Purpose**

Uniquely identifies the MSC implementation by the combination of implementer, product ID, variant and revision.

**Configuration**

The power domain of MPAMF_IIDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_IIDR are RES0.

**Attributes**

MPAMF_IIDR is a 32-bit register.

**Field descriptions**

The MPAMF_IIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit positions</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-20</td>
<td>ProductID</td>
</tr>
<tr>
<td>19-16</td>
<td>Variant</td>
</tr>
<tr>
<td>15-12</td>
<td>Revision</td>
</tr>
<tr>
<td>11-0</td>
<td>Implementer</td>
</tr>
</tbody>
</table>

**ProductID, bits [31:20]**

IMPLEMENTATION DEFINED value identifying the MPAM MSC.

The MSC implementer as identified in the MPAMF_IIDR.Implementer field must assure each product has a unique ProductID from any other with the same Implementer value.

**Variant, bits [19:16]**

IMPLEMENTATION DEFINED value used to distinguish product variants, or major revisions of the product.

*Note*

Implementations of ProductID with differing software interfaces are expected to have different values in the MPAMF_IIDR.Variant field.

**Revision, bits [15:12]**

IMPLEMENTATION DEFINED value used to distinguish minor revisions of the product.

*Note*

This field is intended to differentiate product revisions that are minor changes and are largely software compatible with previous revisions.

**Implementer, bits [11:0]**

Contains the JEP106 code of the company that implemented the MPAM MSC.
(11:8) must contain the JEP106 continuation code of the implementer.

(7) must always be 0.

(6:0) must contain the JEP106 identity code of the implementer.

For an Arm implementation, bits(11:0) are 0x43B.

**Accessing the MPAMF_IIDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_IIDR is read-only.

MPAMF_IIDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_IIDR must have the same contents in the Secure and Non-secure MPAM feature pages.

**MPAMF_IIDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0018</td>
<td>MPAMF_IIDR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASENs</td>
<td>0x0018</td>
<td>MPAMF_IIDR</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
**MPAMF_IMPL_IDR, MPAM Implementation-Specific Partitioning Feature Identification Register**

The MPAMF_IMPL_IDR characteristics are:

**Purpose**

Indicates the implementation-defined partitioning and monitoring features and parameters of the MSC. MPAMF_IMPL_IDR_s indicates implementation-defined partitioning and monitoring features accessed from the Secure MPAM feature page. MPAMF_IMPL_IDR_ns indicates those accessed from the Non-secure MPAM feature page.

If MPAMF_IDR.HAS_RIS is 1, this register gives the implementation-specific features and parameters of the resource instance selected by MPAMCFG_PART_SEL.RIS for any features that are specific to the resource.

**Configuration**

The power domain of MPAMF_IMPL_IDR is implementation defined.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_IMPL_IDR == 1. Otherwise, direct accesses to MPAMF_IMPL_IDR are RES0.

**Attributes**

MPAMF_IMPL_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_IMPL_IDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Bit Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
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<tr>
<td>29</td>
<td></td>
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<td>28</td>
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<td>24</td>
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<td>23</td>
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<td>12</td>
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<td>11</td>
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<td>10</td>
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<td>8</td>
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<td>7</td>
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<tr>
<td>6</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**IMPLFEAT, bits [31:0]**

All 32 bits of this register are available to be used as the implementer sees fit to indicate the presence of implementation-defined MPAM features in this MSC and to give additional implementation-specific read-only information about the parameters of implementation-specific MPAM features to software.

If RIS is implemented, this register indicates the implementation-specific features and parameters of the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Accessing the MPAMF_IMPL_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_IMPL_IDR is read-only.

MPAMF_IMPL_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_IMPL_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_IMPL_IDR_s) and Non-secure (MPAMF_IMPL_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_IMPL_IDR shows the configuration of implementation-specific features for the resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.
**MPAMF_IMPL_IDR** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0028</td>
<td>MPAMF_IMPL_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0028</td>
<td>MPAMF_IMPL_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
The MPAM_F_BW_IDR characteristics are:

Purpose

Indicates which MPAM bandwidth partitioning features are present on this MSC. MPAM_F_BW_IDR_s indicates bandwidth partitioning features accessed from the Secure MPAM feature page. MPAM_F_BW_IDR_ns indicates bandwidth partitioning features accessed from the Non-secure MPAM feature page.

When MPAM_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selected by MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has that information within the field description.

Configuration

The power domain of MPAM_F_BW_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPM is implemented and MPAM_IDR.HAS_MBW_PART == 1. Otherwise, direct accesses to MPAM_F_BW_IDR are RES0.

Attributes

MPAM_F_BW_IDR is a 32-bit register.

Field descriptions

The MPAM_F_BW_IDR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | BWPBM_WD | RES0 | WINDWR | HAS_PROP | HAS_PBM | HAS_MAX | HAS_MIN | RES0 | BWA_WD |

Bits [31:29]

Reserved, RES0.

BWPBM_WD, bits [28:16]

Bandwidth portion bitmap width.

The number of bandwidth portion bits in the MPAMCFG_MBW_PBM<n> register array.

If MPAM_F_BW_IDR.HAS_PBM is 1, this field must contain a value from 1 to 4096, inclusive. Values greater than 32 require a group of 32-bit registers to access the BWPBM, up to 128 if BWPBM_WD is the largest value.

If MPAM_F_BW_IDR.HAS_PBM is 0, this field must be ignored by software.

If RIS is implemented, this field indicates the width of the memory bandwidth portion bitmap partitioning control for the resource instance selected by MPAMCFG_PART_SEL.RIS.

Bit [15]

Reserved, RES0.
**WINDWR, bit [14]**

Indicates the bandwidth accounting period register is writable.

<table>
<thead>
<tr>
<th>WINDWR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The bandwidth accounting period is readable from <code>MPAMCFG_MBW_WINWD</code> which might be fixed or vary due to clock rate reconfiguration of the memory channel or memory controller.</td>
</tr>
<tr>
<td>0b1</td>
<td>The bandwidth accounting width is readable and writable per partition in <code>MPAMCFG_MBW_WINWD</code>.</td>
</tr>
</tbody>
</table>

**HAS_PROP, bit [13]**

Indicates that this MSC implements proportional stride bandwidth partitioning and the `MPAMCFG_MBW_PROP` register can be accessed.

<table>
<thead>
<tr>
<th>HAS_PROP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no memory bandwidth proportional stride control and the <code>MPAMCFG_MBW_PROP</code> register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>The proportional stride memory bandwidth partitioning scheme is supported and the <code>MPAMCFG_MBW_PROP</code> register can be accessed.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of the memory bandwidth proportional stride partitioning control for the resource instance selected by `MPAMCFG_PART_SEL.RIS`.

**HAS_PBM, bit [12]**

Indicates that bandwidth portion partitioning is implemented and the `MPAMCFG_MBW_PBM<n>` register array can be accessed.

<table>
<thead>
<tr>
<th>HAS_PBM</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no memory bandwidth portion control and the <code>MPAMCFG_MBW_PBM</code> is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>The memory bandwidth portion allocation scheme exists and the <code>MPAMCFG_MBW_PBM</code> register can be accessed.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of the memory bandwidth portion partitioning control for the resource instance selected by `MPAMCFG_PART_SEL.RIS`.

**HAS_MAX, bit [11]**

Indicates that this MSC implements maximum bandwidth partitioning and the `MPAMCFG_MBW_MAX` register can be accessed.

<table>
<thead>
<tr>
<th>HAS_MAX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no maximum memory bandwidth control and the <code>MPAMCFG_MBW_MAX</code> register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>The maximum memory bandwidth allocation scheme is supported and the <code>MPAMCFG_MBW_MAX</code> register can be accessed.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of the maximum bandwidth partitioning control for the resource instance selected by `MPAMCFG_PART_SEL.RIS`.

**HAS_MIN, bit [10]**

Indicates that this MSC implements minimum bandwidth partitioning and the `MPAMCFG_MBW_MIN` register can be accessed.
Meaning

<table>
<thead>
<tr>
<th>HAS_MIN</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>There is no minimum memory bandwidth control and the $	ext{MPAMCFG_MBW_MIN}$ register is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>The minimum memory bandwidth allocation scheme is supported and the $	ext{MPAMCFG_MBW_MIN}$ register can be accessed.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the presence of the minimum bandwidth partitioning control for the resource instance selected by $	ext{MPAMCFG_PART_SEL.RIS}$.

**Bits [9:6]**

Reserved, RES0.

**BWA_WD, bits [5:0]**

Number of implemented bits in the bandwidth allocation fields: MIN, MAX and STRIDE. See $	ext{MPAMCFG_MBW_MIN}$, $	ext{MPAMCFG_MBW_MAX}$ and $	ext{MPAMCFG_MBW_PROP}$.

In any of these bandwidth allocation fields exist, this field must have a value from 1 to 16, inclusive. Otherwise, it is permitted to be 0.

If RIS is implemented, this field indicates the number of implemented bits in the bandwidth allocation control fields for the resource instance selected by $	ext{MPAMCFG_PART_SEL.RIS}$.

**Accessing the MPAMF_MBW_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_MBW_IDR is read-only.

MPAMF_MBW_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_MBW_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_MBW_IDR_s) and Non-secure (MPAMF_MBW_IDR_ns) MPAM feature pages.

When MPAMF_IDR HAS_RIS is 1, MPAMF_MBW_IDR shows the configuration of memory bandwidth partitioning for the bandwidth resource instance selected by $	ext{MPAMCFG_PART_SEL.RIS}$. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_MBW_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0040</td>
<td>MPAMF_MBW_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0040</td>
<td>MPAMF_MBW_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
**Purpose**

Indicates the number of memory bandwidth usage monitor instances implemented. This register also indicates several properties of MBWU monitoring, including whether the implementation supports capture, scaling or long counters.

MPAMF_MBWUMON_IDR indicates the number of Secure memory bandwidth usage monitor instances.

MPAMF_MBWUMON_IDR_ns indicates the number of Non-secure memory bandwidth usage monitor instances.

If MPAMF_IDR.HAS_RIS is 1, fields that mention RIS must reflect the properties of the resource instance currently selected by MPAMCFG_PART_SEL.RIS. Fields that do not mention RIS are constant across all resource instances.

**Configuration**

The power domain of MPAMF_MBWUMON_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_MBWU == 1. Otherwise, direct accesses to MPAMF_MBWUMON_IDR are RES0.

**Attributes**

MPAMF_MBWUMON_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_MBWUMON_IDR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>272625242322212019181716151413121110 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>HAS_CAPTURE</td>
<td>HAS_LONG</td>
<td>LWD</td>
<td>HAS_RWBW</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**HAS_CAPTURE, bit [31]**

The implementation supports copying an MSMON_MBWU to the corresponding MSMON_MBWU_CAPTURE on a capture event.

<table>
<thead>
<tr>
<th>HAS_CAPTURE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_MBWU_CAPTURE is not implemented and there is no support for capture events in the MBWU monitor.</td>
</tr>
<tr>
<td>0b1</td>
<td>The MSMON_MBWU_CAPTURE register is implemented and the MBWU monitor supports the capture event behavior.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that MBWU monitor capture is implemented for the resource instance selected by MPAMCFG_PART_SEL.RIS.

If MPAMF_MBWUMON_IDR.HAS_LONG is 1, this also indicates that MSMON_MBWU_L_CAPTURE is implemented.

**HAS_LONG, bit [30]**

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Indicates whether MSMON_MBWU_L is implemented.

If HAS_CAPTURE is 1, indicates whether MSMON_MBWU_L_CAPTURE is implemented.
HAS_LONG

<table>
<thead>
<tr>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
</tr>
<tr>
<td>0b1</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that the long MBWU monitor is implemented for the resource instance selected by MPAMCFG_PART_SEL.RIS.

If MPAMF_MBWUMON_IDR.HAS_CAPTURE is 1, this also indicates that MSMON_MBWU_L_CAPTURE is implemented.

Otherwise:

Reserved, RES0.

LWD, bit [29]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Long register VALUE width.

If MPAMF_MBWUMON_IDR.HAS_LONG is 0, MPAMF_MBWUMON_IDR.LWD must also be 0.

<table>
<thead>
<tr>
<th>LWD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>If MPAMF_MBWUMON_IDR.HAS_LONG is 1, MSMON_MBWU_L has 44-bit VALUE field in bits [43:0]. Bits [62:44] are RES0. If HAS_LONG is 1 and MPAMF_MBWUMON_IDR.HAS_CAPTURE is 1, MSMON_MBWU_L_CAPTURE also has 44-bit VALUE field in bits [43:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>MSMON_MBWU_L has 63-bit VALUE field in bits [62:0]. If MPAMF_MBWUMON_IDR.HAS_CAPTURE == 1, MSMON_MBWU_L_CAPTURE also has 63-bit VALUE field in bits [62:0].</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the length of the MSMON_MBWU_L.VALUE field implemented for the resource instance selected by MPAMCFG_PART_SEL.RIS.

Otherwise:

Reserved, RES0.

HAS_RWBW, bit [28]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Read/write bandwidth selection is implemented in MSMON_CFG_MBWU_FLT.

<table>
<thead>
<tr>
<th>HAS_RWBW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Read/write bandwidth selection is not implemented.</td>
</tr>
<tr>
<td>0b1</td>
<td>Read/write bandwidth selection is implemented.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates whether read/write bandwidth collection selection is available in MSMON_CFG_MBWU_FLT for resource instance selected by MPAMCFG_PART_SEL.RIS.

Otherwise:

Reserved, RES0.

Bits [27:21]

Reserved, RES0.
SCALE, bits [20:16]

Scaling of MSMON_MBWU.VALUE in bits. If scaling is enabled by MSMON_CFG_MBWU_CTL.SCLEN, the byte count in the VALUE field has been shifted by SCALE bits to the right.

<table>
<thead>
<tr>
<th>SCALE</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00000</td>
<td>Scaling is not implemented.</td>
</tr>
<tr>
<td>0bxxxxx</td>
<td>Other values are right shift count when scaling is enabled.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates the scale value for MSMON_MBWU.VALUE field for the resource instance selected by MPAMCFG_PART_SEL.RIS.

NUM_MON, bits [15:0]

The number of memory bandwidth usage monitor instances implemented. The largest monitor instance selector, MSMON_CFG_MON_SEL.MON_SEL, is NUM_MON minus 1.

If RIS is implemented, this field indicates the number of MBWU monitor instances for MSMON_MBWU.VALUE field for the resource instance selected by MPAMCFG_PART_SEL.RIS.

Accessing the MPAMF_MBWUMON_IDR

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_MBWUMON_IDR is read-only.

MPAMF_MBWUMON_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_MBWUMON_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_MBWUMON_IDR_s) and Non-secure (MPAMF_MBWUMON_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_MBWUMON_IDR shows the configuration of memory bandwidth monitoring for the bandwidth resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

Access to MPAMF_MBWUMON_IDR is not affected by MSMON_CFG_MON_SEL.RIS.

MPAMF_MBWUMON_IDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE</td>
<td>0x0090</td>
<td>MPAMF_MBWUMON_IDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE</td>
<td>0x0090</td>
<td>MPAMF_MBWUMON_IDR</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
The MPAMF_MSMON_IDR characteristics are:

**Purpose**

Indicates which MPAM monitoring features are present on this MSC. MPAMF_MSMON_IDR_s indicates Secure monitoring features. MPAMF_MSMON_IDR_ns indicates Non-secure monitoring features.

If MPAMF_IDR.Has_RIS is 1, fields that mention RIS must reflect the properties of the resource instance currently selected by MPAMCFG_PART_SEL.RIS. Fields that do not mention RIS are constant across all resource instances.

**Configuration**

The power domain of MPAMF_MSMON_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_MSMON == 1. Otherwise, direct accesses to MPAMF_MSMON_IDR are RES0.

**Attributes**

MPAMF_MSMON_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_MSMON_IDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>HAS_LOCAL_CAPT_EVNT</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>MSMON_MBWU</td>
</tr>
<tr>
<td>28</td>
<td>MSMON_CSU</td>
</tr>
<tr>
<td>17</td>
<td>RES0</td>
</tr>
<tr>
<td>16</td>
<td>RES0</td>
</tr>
<tr>
<td>15</td>
<td>RES0</td>
</tr>
<tr>
<td>14</td>
<td>RES0</td>
</tr>
<tr>
<td>13</td>
<td>RES0</td>
</tr>
<tr>
<td>12</td>
<td>RES0</td>
</tr>
<tr>
<td>11</td>
<td>RES0</td>
</tr>
<tr>
<td>10</td>
<td>RES0</td>
</tr>
<tr>
<td>9</td>
<td>RES0</td>
</tr>
<tr>
<td>8</td>
<td>RES0</td>
</tr>
<tr>
<td>7</td>
<td>RES0</td>
</tr>
<tr>
<td>6</td>
<td>RES0</td>
</tr>
<tr>
<td>5</td>
<td>RES0</td>
</tr>
<tr>
<td>4</td>
<td>RES0</td>
</tr>
<tr>
<td>3</td>
<td>RES0</td>
</tr>
<tr>
<td>2</td>
<td>RES0</td>
</tr>
<tr>
<td>1</td>
<td>RES0</td>
</tr>
<tr>
<td>0</td>
<td>RES0</td>
</tr>
</tbody>
</table>

**HAS_LOCAL_CAPT_EVNT, bit [31]**

Has local capture event generator. Indicates whether this MSC has the MPAM local capture event generator and the MSMON_CAPT_EVNT register.

<table>
<thead>
<tr>
<th>HAS_LOCAL_CAPT_EVNT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not support MPAM local capture event generator or MSMON_CAPT_EVNT.</td>
</tr>
<tr>
<td>0b1</td>
<td>Supports the MPAM local capture event generator and the MSMON_CAPT_EVNT register.</td>
</tr>
</tbody>
</table>

**Bits [30:18]**

Reserved, RES0.

**MSMON_MBWU, bit [17]**

Memory bandwidth usage monitoring. Indicates whether MPAM monitoring for Memory Bandwidth Usage by PARTID and PMG is implemented and whether the following bandwidth usage registers are accessible:

- [MPAMF_MBWUMON_IDR](#), [MSMON_CFG_MBWU_CTL](#), [MSMON_CFG_MBWUFLT](#), [MSMON_MBWU](#).
- The optional [MSMON_MBWU_CAPTURE](#).
- If MPAM v0.1 or MPAM v1.1 is implemented, the optional [MSMON_MBWUL](#) and the optional [MSMON_MBWUL_CAPTURE](#).
**MSMON_MBWU, bit [0]**

Does not have monitoring for memory bandwidth usage and does not use the bandwidth usage registers.

**Meaning**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have monitoring for memory bandwidth usage and does not use the bandwidth usage registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has monitoring of memory bandwidth usage and uses the bandwidth usage registers.</td>
</tr>
</tbody>
</table>

**MSMON_CSU, bit [16]**

Cache storage usage monitoring. Indicates whether MPAM monitoring of cache storage usage by PARTID and PMG is implemented and the following registers are accessible:

- **MPAMF_CSUMON_IDR**, **MSMON_CFG_CSU_CTL**, **MSMON_CFG_CSU_FLT**, **MSMON_CSU**, **MSMON_CSU_CAPTURE**

**Meaning**

<table>
<thead>
<tr>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Does not have monitoring for cache storage usage or the <strong>MPAMF_CSUMON_IDR</strong>, <strong>MSMON_CFG_CSU_CTL</strong>, <strong>MSMON_CFG_CSU_FLT</strong>, <strong>MSMON_CSU</strong>, or <strong>MSMON_CSU_CAPTURE</strong> registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Has monitoring of cache storage usage and the <strong>MPAMF_CSUMON_IDR</strong>, <strong>MSMON_CFG_CSU_CTL</strong>, <strong>MSMON_CFG_CSU_FLT</strong>, <strong>MSMON_CSU</strong>, and optional <strong>MSMON_CSU_CAPTURE</strong> registers.</td>
</tr>
</tbody>
</table>

**Bits [15:0]**

Reserved, RES0.

**Accessing the MPAMF_MSMON_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

**MPAMF_MSMON_IDR** is read-only.

**MPAMF_MSMON_IDR** must be readable from the Non-secure and Secure MPAM feature pages.

**MPAMF_MSMON_IDR** is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_MSMON_IDR_s) and Non-secure (MPAMF_MSMON_IDR_ns) MPAM feature pages.

When **MPAMF_IDR.HAS_RIS** is 1, **MPAMF_MSMON_IDR** shows the configuration of memory system monitoring for the resource instance selected by **MPAMCFG_PART_SEL.RIS** as described in **MPAMF_MBWUMON_IDR**.

Access to **MPAMF_MSMON_IDR** is not affected by **MSMON_CFG_MON_SEL.RIS**.

**MPAMF_MSMON_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0080</td>
<td>MPAMF_MSMON_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
Accesses on this interface are **RO**.
The MPAMF_PARTID_NRW_IDR characteristics are:

**Purpose**

Indicates the largest internal PARTID for this MSC. MPAMF_PARTID_NRW_IDR_s indicates the largest Secure internal PARTID. MPAMF_PARTID_NRW_IDR_ns indicates the largest Non-secure internal PARTID.

PARTID narrowing is global to the MSC and does not vary by resource instance.

**Configuration**

The power domain of MPAMF_PARTID_NRW_IDR is implementation defined.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_PARTID_NRW == 1. Otherwise, direct accesses to MPAMF_PARTID_NRW_IDR are RES0.

**Attributes**

MPAMF_PARTID_NRW_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_PARTID_NRW_IDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>RES0</td>
</tr>
<tr>
<td>28</td>
<td>RES0</td>
</tr>
<tr>
<td>27</td>
<td>RES0</td>
</tr>
<tr>
<td>26</td>
<td>RES0</td>
</tr>
<tr>
<td>25</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td>RES0</td>
</tr>
<tr>
<td>23</td>
<td>RES0</td>
</tr>
<tr>
<td>22</td>
<td>RES0</td>
</tr>
<tr>
<td>21</td>
<td>RES0</td>
</tr>
<tr>
<td>20</td>
<td>RES0</td>
</tr>
<tr>
<td>19</td>
<td>RES0</td>
</tr>
<tr>
<td>18</td>
<td>RES0</td>
</tr>
<tr>
<td>17</td>
<td>RES0</td>
</tr>
<tr>
<td>16</td>
<td>RES0</td>
</tr>
<tr>
<td>15</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>14</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>13</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>12</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>11</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>10</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>9</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>8</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>7</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>6</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>5</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>4</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>3</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>2</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>1</td>
<td>INTPARTID_MAX</td>
</tr>
<tr>
<td>0</td>
<td>INTPARTID_MAX</td>
</tr>
</tbody>
</table>

**Bits [31:16]**

Reserved, RES0.

**INTPARTID_MAX, bits [15:0]**

The largest intPARTID supported in this MSC.

**Accessing the MPAMF_PARTID_NRW_IDR**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_PARTID_NRW_IDR is read-only.

MPAMF_PARTID_NRW_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_PARTID_NRW_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_PARTID_NRW_IDR_s) and Non-secure (MPAMF_PARTID_NRW_IDR_ns) MPAM feature pages.

MPAMF_PARTID_NRW_IDR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
</table>

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Accesses on this interface are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0050</td>
<td>MPAMF_PARTID_NRW_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RO.
MPAMF_PRI_IDR, MPAM Priority Partitioning Identification Register

The MPAMF_PRI_IDR characteristics are:

**Purpose**

Indicates which MPAM priority partitioning features are present on this MSC. MPAMF_PRI_IDR_s indicates priority partitioning features accessed from the Secure MPAM feature page. MPAMF_PRI_IDR_ns indicates priority partitioning features accessed from the Non-secure MPAM feature page.

When MPAMF_IDR.HAS_RIS is 1, some fields in this register give information for the resource instance selected by MPAMCFG_PART_SEL.RIS. The description of every field that is affected by MPAMCFG_PART_SEL.RIS has that information within the field description.

**Configuration**

The power domain of MPAMF_PRI_IDR is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and MPAMF_IDR.HAS_PRI_PART == 1. Otherwise, direct accesses to MPAMF_PRI_IDR are RES0.

**Attributes**

MPAMF_PRI_IDR is a 32-bit register.

**Field descriptions**

The MPAMF_PRI_IDR bit assignments are:

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RES0 DSPRI_WD RES0 DSPRI_0_IS_LOW HAS_DSPRI RES0 INTPRI_WD RES0 INTPRI_0_IS_LOW HAS_INTPRI
```

**Bits [31:26]**

Reserved, RES0.

**DSPRI_WD, bits [25:20]**

Number of implemented bits in the downstream priority field (DSPRI) of MPAMCFG_PRI.

If HAS_DSPRI == 1, this field must contain a value from 1 to 16, inclusive.

If HAS_DSPRI == 0, this field must be 0.

If RIS is implemented, this field indicates the number of downstream priority bits for the resource instance selected by MPAMCFG_PART_SEL.RIS.

**Bits [19:18]**

Reserved, RES0.

**DSPRI_0_IS_LOW, bit [17]**

Indicates whether 0 in MPAMCFG_PRI DSPRI is the lowest or the highest downstream priority.
**DSPRI_0_IS_LOW**

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>In the <code>MPAMCFG_PRI</code>.DSPRI field, a value of 0 means the highest priority.</td>
</tr>
<tr>
<td>0b1</td>
<td>In the <code>MPAMCFG_PRI</code>.DSPRI field, a value of 0 means the lowest priority.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that 0 is the lowest downstream priority for the resource instance selected by `MPAMCFG_PART_SEL`.RIS.

**HAS_DSPRI, bit [16]**

Indicates that the `MPAMCFG_PRI` register implements the DSPRI field.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>This MSC supports priority partitioning, but does not implement a downstream priority (DSPRI) field in the <code>MPAMCFG_PRI</code> register.</td>
</tr>
<tr>
<td>0b1</td>
<td>This MSC supports downstream priority partitioning and implements the downstream priority (DSPRI) field in the <code>MPAMCFG_PRI</code> register.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that downstream priority is implemented for the resource instance selected by `MPAMCFG_PART_SEL`.RIS.

**Bits [15:10]**

Reserved, RES0.

**INTPRI_WD, bits [9:4]**

Number of implemented bits in the internal priority field (INTPRI) in the `MPAMCFG_PRI` register.

If HAS_INTPRI == 1, this field must contain a value from 1 to 16, inclusive.

If HAS_INTPRI == 0, this field must be 0.

If RIS is implemented, this field indicates the number of internal priority bits for the resource instance selected by `MPAMCFG_PART_SEL`.RIS.

**Bits [3:2]**

Reserved, RES0.

**INTPRI_0_IS_LOW, bit [1]**

Indicates whether 0 in `MPAMCFG_PRI`.INTPRI is the lowest or the highest internal priority.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>In the <code>MPAMCFG_PRI</code>.INTPRI field, a value of 0 means the highest priority.</td>
</tr>
<tr>
<td>0b1</td>
<td>In the <code>MPAMCFG_PRI</code>.INTPRI field, a value of 0 means the lowest priority.</td>
</tr>
</tbody>
</table>

If RIS is implemented, this field indicates that 0 is the lowest internal priority for the resource instance selected by `MPAMCFG_PART_SEL`.RIS.

**HAS_INTPRI, bit [0]**

Indicates that this MSC implements the INTPRI field in the `MPAMCFG_PRI` register.
The MSC supports priority partitioning, but does not implement the internal priority (INTPRI) field in the MPAMCFG_PRI register.

This MSC supports internal priority partitioning and implements the internal priority (INTPRI) field in the MPAMCFG_PRI register.

If RIS is implemented, this field indicates that internal priority is implemented for the resource instance selected by MPAMCFG_PART_SEL.RIS.

### Accessing the MPAMF_PRI_IDR

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MPAMF_PRI_IDR is read-only.

MPAMF_PRI_IDR must be readable from the Non-secure and Secure MPAM feature pages.

MPAMF_PRI_IDR is permitted to have the same contents when read from either the Secure and Non-secure MPAM feature pages unless the register contents is different for Secure and Non-secure versions, when there must be separate registers in the Secure (MPAMF_PRI_IDR_s) and Non-secure (MPAMF_PRI_IDR_ns) MPAM feature pages.

When MPAMF_IDR.HAS_RIS is 1, MPAMF_PRI_IDR shows the configuration of priority partitioning for the resource instance selected by MPAMCFG_PART_SEL.RIS. Fields that mention RIS in their field descriptions have values that track the implemented properties of the resource instance. Fields that do not mention RIS are constant across all resource instances.

**MPAMF_PRI_IDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0048</td>
<td>MPAMF_PRI_IDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0048</td>
<td>MPAMF_PRI_IDR_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
MPAMF_SIDR, MPAM Features Secure Identification Register

The MPAMF_SIDR characteristics are:

**Purpose**

The MPAMF_SIDR is a 32-bit read-only register that indicates the maximum Secure PARTID and Secure PMG on this MSC.

**Configuration**

The power domain of MPAMF_SIDR is **IMPLEMENTATION DEFINED**.

This register is present only when FEAT_MPAM is implemented. Otherwise, direct accesses to MPAMF_SIDR are **RES0**.

**Attributes**

MPAMF_SIDR is a 32-bit register.

**Field descriptions**

The MPAMF_SIDR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>24</td>
<td>S_PMG_MAX</td>
</tr>
<tr>
<td>15</td>
<td>S_PARTID_MAX</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**S_PMG_MAX, bits [23:16]**

Maximum value of Secure PMG supported by this component.

**S_PARTID_MAX, bits [15:0]**

Maximum value of Secure PARTID supported by this component.

**Accessing the MPAMF_SIDR**

This register is only within the Secure MPAM feature page memory frame.

MPAMF_SIDR is read-only.

MPAMF_SIDR must only be readable from the Secure MPAM feature page. If the system or the MSC does not support the Secure address map, this register must not be accessible.

**MPAMF_SIDR can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0008</td>
<td>MPAMF_SIDR_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RO**.
**MSMON\_CAPT\_EVNT, MPAM Capture Event Generation Register**

The MSMON\_CAPT\_EVNT characteristics are:

**Purpose**

Generates a local capture event when written with bit[0] as 1. MSMON\_CAPT\_EVNT_s generates local capture events for Secure monitors only or for Secure and Non-secure monitors. MSMON\_CAPT\_EVNT_ns generates local capture events for Non-secure monitors only.

**Configuration**

The power domain of MSMON\_CAPT\_EVNT is IMPLEMENTATION DEFINED.

This register is present only when FEAT\_MPAM is implemented, MPAMF\_IDR.HAS\_MSMON == 1 and MPAMF\_MSMON\_IDR.HAS\_LOCAL\_CAPT\_EVNT == 1. Otherwise, direct accesses to MSMON\_CAPT\_EVNT are RES0.

**Attributes**

MSMON\_CAPT\_EVNT is a 32-bit register.

**Field descriptions**

The MSMON\_CAPT\_EVNT bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| RES0 | ALL | NOW |

**Bits [31:2]**

Reserved, RES0.

**ALL, bit [1]**

In the Secure instance of this register, if ALL written as 1 and NOW is also written as 1, signal a capture event to Secure and Non-secure monitor instances in this MSC that are configured with CAPT\_EVNT = 7.

If written as 0 and NOW is written as 1, signal a capture event to Secure monitor instances in this MSC that are configured with CAPT\_EVNT = 7.

In the Non-secure instance of this register, this bit is RAZ/WI.

This bit always reads as zero.

<table>
<thead>
<tr>
<th>ALL</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Send capture event to Secure monitors only.</td>
</tr>
<tr>
<td>0b1</td>
<td>Send capture event to both Secure and Non-secure monitors.</td>
</tr>
</tbody>
</table>

**NOW, bit [0]**

When written as 1, this bit causes an event to all monitors in this MSC with CAPT\_EVNT set to the value of 7.

When this bit is written as 0, no event is signaled.

This bit always reads as zero.
**Accessing the MSMON_CAPT_EVNT**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_CAPT_EVNT_s must be accessible from the Secure MPAM feature page. MSMON_CAPT_EVENT_ns must be accessible from the Non-secure MPAM feature page.

The two instances of MSMON_CAPT_EVNT must be separate registers. The Secure instance (MSMON_CAPT_EVNT_s) can generate capture events for both Secure and Non-secure PARTID monitors, and the Non-secure instance (MSMON_CAPT_EVNT_ns) can generate capture events for Non-secure PARTID monitors only.

**MSMON_CAPT_EVNT can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0808</td>
<td>MSMON_CAPT_EVNT_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0808</td>
<td>MSMON_CAPT_EVNT_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
**MSMON_CFG_CSU_CTL, MPAM Memory System Monitor Configure Cache Storage Usage Monitor Control Register**

The MSMON_CFG_CSU_CTL characteristics are:

**Purpose**

Controls the CSU monitor selected by `MSMON_CFG_MON_SEL`. MSMON_CFG_CSU_CTL_s controls the Secure cache storage usage monitor instance selected by the Secure instance of `MSMON_CFG_MON_SEL`. MSMON_CFG_CSU_CTL_ns controls Non-secure cache storage usage monitor instance selected by the Non-secure instance of `MSMON_CFG_MON_SEL`.

If `MPAMF_IDR.HAS_RIS` is 1, the monitor instance configuration accessed is for the resource instance currently selected by `MSMON_CFG_MON_SEL.RIS` and the monitor instance of that resource instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

**Configuration**

The power domain of MSMON_CFG_CSU_CTL is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_CSU == 1. Otherwise, direct accesses to MSMON_CFG_CSU_CTL are RES0.

**Attributes**

MSMON_CFG_CSU_CTL is a 32-bit register.

**Field descriptions**

The MSMON_CFG_CSU_CTL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>EN</th>
<th>CAPT_EVNT</th>
<th>CAPT_RESET</th>
<th>OFLOW_STATUS</th>
<th>OFLOW_INTR</th>
<th>OFLOW_FRZ</th>
<th>SUBTYPE</th>
<th>RES0</th>
<th>MATCH_PMG</th>
<th>MATCH_PARTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>EN</td>
<td>CAPT_EVNT</td>
<td>CAPT_RESET</td>
<td>OFLOW_STATUS</td>
<td>OFLOW_INTR</td>
<td>OFLOW_FRZ</td>
<td>SUBTYPE</td>
<td>RES0</td>
<td>MATCH_PMG</td>
<td>MATCH_PARTID</td>
</tr>
</tbody>
</table>

**EN, bit [31]**

Enabled.

<table>
<thead>
<tr>
<th>Value</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is disabled and must not collect any information.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is enabled to collect information according to the configuration of the instance.</td>
</tr>
</tbody>
</table>

**CAPT_EVNT, bits [30:28]**

Capture event selector.

Select the event that triggers capture from the following:
<table>
<thead>
<tr>
<th>CAPT_EVNT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>No capture event is triggered.</td>
</tr>
<tr>
<td>0b001</td>
<td>External capture event 1 (optional but recommended)</td>
</tr>
<tr>
<td>0b010</td>
<td>External capture event 2 (optional)</td>
</tr>
<tr>
<td>0b011</td>
<td>External capture event 3 (optional)</td>
</tr>
<tr>
<td>0b100</td>
<td>External capture event 4 (optional)</td>
</tr>
<tr>
<td>0b101</td>
<td>External capture event 5 (optional)</td>
</tr>
<tr>
<td>0b110</td>
<td>External capture event 6 (optional)</td>
</tr>
<tr>
<td>0b111</td>
<td>Capture occurs when a MSMON_CAPT_EVNT register in this MSC is written and causes a capture event for the security state of this monitor. (optional)</td>
</tr>
</tbody>
</table>

The values marked as optional indicate capture event sources that can be omitted in an implementation. Those values representing non-implemented event sources must not trigger a capture event.

If capture is not implemented for the CSU monitor type as indicated by MPAMF_CSUMON_IDR.HAS_CAPTURE = 0, this field is RAZ/WI.

**CAPT_RESET, bit [27]**

Reset after capture.

Controls whether the value of MSMON_CSU is reset to zero immediately after being copied to MSMON_CSU_CAPTURE.

<table>
<thead>
<tr>
<th>CAPT_RESET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Monitor is not reset on capture.</td>
</tr>
<tr>
<td>0b1</td>
<td>Monitor is reset on capture.</td>
</tr>
</tbody>
</table>

If capture is not implemented for the CSU monitor type as indicated by MPAMF_CSUMON_IDR.HAS_CAPTURE = 0, this field is RAZ/WI.

Because the CSU monitor type produces a measurement rather than a count, it might not make sense to ever reset the value after a capture. If there is no reason to ever reset a CSU monitor, this field is RAZ/WI.

**OFLOW_STATUS, bit [26]**

Overflow status.

Indicates whether the value of MSMON_CSU has overflowed.

<table>
<thead>
<tr>
<th>OFLOW_STATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No overflow has occurred.</td>
</tr>
<tr>
<td>0b1</td>
<td>At least one overflow has occurred since this bit was last written to zero.</td>
</tr>
</tbody>
</table>

If overflow is not possible for a CSU monitor in the implementation, this field is RAZ/WI.

**OFLOW_INTR, bit [25]**

Overflow Interrupt.

Controls whether an overflow interrupt is generated when the value of MSMON_CSU has overflowed.

<table>
<thead>
<tr>
<th>OFLOW_INTR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No interrupt is signaled on an overflow of MSMON_CSU.</td>
</tr>
<tr>
<td>0b1</td>
<td>On overflow, an implementation-specific interrupt is signaled.</td>
</tr>
</tbody>
</table>

If OFLOW_INTR is not supported by the implementation, this field is RAZ/WI.

**OFLOW_FRZ, bit [24]**

Freeze Monitor on Overflow.
Controls whether the value of **MSMON_CSU** freezes on an overflow.

<table>
<thead>
<tr>
<th>OFLOW_FRZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Monitor count wraps on overflow.</td>
</tr>
<tr>
<td>0b1</td>
<td>Monitor count freezes on overflow. The frozen value might be 0 or another value if the monitor overflowed with an increment larger than 1.</td>
</tr>
</tbody>
</table>

If overflow is not possible for a CSU monitor in the implementation, this field is RAZ/WI.

**SUBTYPE, bits [23:20]**

Subtype. Type of cache storage usage counted by this monitor.

This field is not currently used for CSU monitors, but reserved for future use.

This field is RAZ/WI.

**Bits [19:18]**

Reserved, RES0.

**MATCH_PMG, bit [17]**

Match PMG.

Controls whether the monitor measures only storage used with PMG matching **MSMON_CFG_CSU_FLT**.PMG.

<table>
<thead>
<tr>
<th>MATCH_PMG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor measures storage used with any PMG value.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor only measures storage used with the PMG value matching <strong>MSMON_CFG_CSU_FLT</strong>.PMG.</td>
</tr>
</tbody>
</table>

If MATCH_PMG == 1 and MATCH_PARTID == 0, it is CONSTRAINED UNPREDICTABLE whether the monitor instance:

- Measures the storage used with matching PMG and with any PARTID.
- Measures no storage usage, that is, **MSMON_CSU**.VALUE is zero.
- Measures the storage used with matching PMG and PARTID, that is, treats MATCH_PARTID as == 1.

**MATCH_PARTID, bit [16]**

Match PARTID.

Controls whether the monitor measures only storage used with PARTID matching **MSMON_CFG_CSU_FLT**.PARTID.

<table>
<thead>
<tr>
<th>MATCH_PARTID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor measures storage used with any PARTID value.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor only measures storage used with the PARTID value matching <strong>MSMON_CFG_CSU_FLT</strong>.PARTID.</td>
</tr>
</tbody>
</table>

**Bits [15:8]**

Reserved, RES0.

**TYPE, bits [7:0]**

Monitor Type Code. The CSU monitor is TYPE = 0x43.

TYPE is a read-only constant indicating the type of the monitor.

Reads as 0x43.
Accessing the MSMON_CFG_CSU_CTL

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_CFG_CSU_CTL_s must be accessible from the Secure MPAM feature page. MSMON_CFG_CSU_CTL_ns must be accessible from the Non-secure MPAM feature page.

MSMON_CFG_CSU_CTL_s and MSMON_CFG_CSU_CTL_ns must be separate registers. The Secure instance (MSMON_CFG_CSU_CTL_s) accesses the cache storage usage monitor controls used for Secure PARTIDs, and the Non-secure instance (MSMON_CFG_CSU_CTL_ns) accesses the cache storage usage monitor controls used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MSMON_CFG_CSU_CTL access the cache storage usage monitor configuration settings for the cache resource instance selected by MSMON_CFG_MON_SEL.RIS and the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, loads and stores to MSMON_CFG_CSU_CTL access the cache storage usage monitor configuration settings for the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

MSMON_CFG_CSU_CTL can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0818</td>
<td>MSMON_CFG_CSU_CTL_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0818</td>
<td>MSMON_CFG_CSU_CTL_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
MSMON_CFG_CSU_FLT, MPAM Memory System Monitor Configure Cache Storage Usage Monitor Filter Register

The MSMON_CFG_CSU_FLT characteristics are:

**Purpose**

Configures PARTID and PMG to measure or count in the CSU monitor selected by MSMON_CFG_MON_SEL. MSMON_CFG_CSU_FLT sets filter conditions for the Secure cache storage usage monitor instance selected by the Secure instance of MSMON_CFG_MON_SEL. MSMON_CFG_CSU_CTL sets filter conditions for the Non-secure cache storage usage monitor instance selected by the Non-secure instance of MSMON_CFG_MON_SEL.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance filter configuration accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_CFG_CSU_FLT is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_CSU == 1. Otherwise, direct accesses to MSMON_CFG_CSU_FLT are RES0.

**Attributes**

MSMON_CFG_CSU_FLT is a 32-bit register.

**Field descriptions**

The MSMON_CFG_CSU_FLT bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PMG</td>
</tr>
<tr>
<td>29</td>
<td>PARTID</td>
</tr>
</tbody>
</table>

**Bits [31:24]**

Reserved, RES0.

**PMG, bits [23:16]**

Performance monitoring group to filter cache storage usage monitoring.

If MSMON_CFG_CSU_CTL.MATCH PMG == 0, this field is not used to match cache storage to a PMG and the contents of this field is ignored.

If MSMON_CFG_CSU_CTL.MATCH PMG == 1 and MSMON_CFG_CSU_CTL.MATCH PARTID == 1, the monitor instance selected by MSMON_CFG_MON_SEL measures or counts cache storage labeled with PMG equal to this field and PARTID equal to the PARTID field.

If MSMON_CFG_CSU_CTL.MATCH PMG == 1 and MSMON_CFG_CSU_CTL.MATCH PARTID == 0, the behavior of the monitor instance selected by MSMON_CFG_MON_SEL is CONSTRAINED UNPREDICTABLE. See MSMON_CFG_CSU_CTL.MATCH_PMG for more information.

**PARTID, bits [15:0]**

Partition ID to filter cache storage usage monitoring.
If `MSMON_CFG_CSU_CTL.MATCH_PARTID` == 0 and `MSMON_CFG_CSU_CTL.MATCH_PMG` == 0, the monitor measures all allocated cache storage.

If `MSMON_CFG_CSU_CTL.MATCH_PARTID` == 0 and `MSMON_CFG_CSU_CTL.MATCH_PMG` == 1, the behavior of the monitor is CONSTRAINED UNPREDICTABLE. See the description of `MSMON_CFG_CSU_CTL.MATCH_PMG`.

If `MSMON_CFG_CSU_CTL.MATCH_PARTID` == 1 and `MSMON_CFG_CSU_CTL.MATCH_PMG` == 0, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts cache storage labeled with PARTID equal to this field.

If `MSMON_CFG_CSU_CTL.MATCH_PARTID` == 1 and `MSMON_CFG_CSU_CTL.MATCH_PMG` == 1, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts cache storage labeled with PARTID equal to this field and PMG equal to the PMG field.

**Accessing the MSMON_CFG_CSU_FLT**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

`MSMON_CFG_CSU_FLT_s` must be accessible from the Secure MPAM feature page. `MSMON_CFG_CSU_FLT_ns` must be accessible from the Non-secure MPAM feature page.

`MSMON_CFG_CSU_FLT_s` and `MSMON_CFG_CSU_FLT_ns` must be separate registers. The Secure instance (`MSMON_CFG_CSU_FLT_s`) accesses the PARTID and PMG matching for a cache storage usage monitor used for Secure PARTIDs, and the Non-secure instance (`MSMON_CFG_CSU_FLT_ns`) accesses the PARTID and PMG matching for a cache storage usage monitor used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to `MSMON_CFG_CSU_FLT` access the monitor configuration settings for the resource instance selected by `MSMON_CFG_MON_SEL.RIS` and the cache storage usage monitor instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

When RIS is not implemented, loads and stores to `MSMON_CFG_CSU_FLT` access the monitor configuration settings for the cache storage usage monitor instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

`MSMON_CFG_CSU_FLT` can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0810</td>
<td>MSMON_CFG_CSU_FLT_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0810</td>
<td>MSMON_CFG_CSU_FLT_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The MSMON_CFG_MBWU_CTL characteristics are:

**Purpose**

Controls the MBWU monitor selected by `MSMON_CFG_MON_SEL`. MSMON_CFG_MBWU_CTL controls the Secure memory bandwidth usage monitor instance selected by the Secure instance of `MSMON_CFG_MON_SEL`. MSMON_CFG_MBWU_CTL ns controls Non-secure memory bandwidth usage monitor instance selected by the Non-secure instance of `MSMON_CFG_MON_SEL`.

If `MPAMF_IDR.HAS_RIS` is 1, the monitor instance configuration accessed is for the resource instance currently selected by `MSMON_CFG_MON_SEL.RIS` and the monitor instance of that resource instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

**Configuration**

The power domain of MSMON_CFG_MBWU_CTL is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_MBWU == 1. Otherwise, direct accesses to MSMON_CFG_MBWU_CTL are RES0.

**Attributes**

MSMON_CFG_MBWU_CTL is a 32-bit register.

**Field descriptions**

The MSMON_CFG_MBWU_CTL bit assignments are:

```
<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
</tr>
</thead>
<tbody>
<tr>
<td>EN</td>
<td>CAPT_EVNT</td>
<td>CAPT_RESET</td>
<td>OFLOW_STATUS</td>
<td>OFLOW_INTR</td>
<td>OFLOW_FRZ</td>
<td>SUBTYPE</td>
<td>SCLEN</td>
<td>RES0</td>
<td>MATCH_PMG</td>
<td>MATCH_PARTID</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
```

**EN, bit [31]**

Enabled.

<table>
<thead>
<tr>
<th>EN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is disabled and must not collect any information.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is enabled to collect information according to the configuration of the instance.</td>
</tr>
</tbody>
</table>

**CAPT_EVNT, bits [30:28]**

Capture event selector.

When the selected capture event occurs, `MSMON_MBWU` of the monitor instance is copied to `MSMON_MBWU_CAPTURE` of the same instance. If the long counter is also implemented, `MSMON_MBWU_L` is also copied to `MSMON_MBWU_L_CAPTURE`.

Select the event that triggers capture from the following:
Meaning

<table>
<thead>
<tr>
<th>CAPT_EVNT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b000</td>
<td>No capture event is triggered.</td>
</tr>
<tr>
<td>0b001</td>
<td>External capture event 1 (optional but recommended)</td>
</tr>
<tr>
<td>0b010</td>
<td>External capture event 2 (optional)</td>
</tr>
<tr>
<td>0b011</td>
<td>External capture event 3 (optional)</td>
</tr>
<tr>
<td>0b100</td>
<td>External capture event 4 (optional)</td>
</tr>
<tr>
<td>0b101</td>
<td>External capture event 5 (optional)</td>
</tr>
<tr>
<td>0b110</td>
<td>External capture event 6 (optional)</td>
</tr>
<tr>
<td>0b111</td>
<td>Capture occurs when a MSMON_CAPT_EVNT register in this MSC is written and causes a capture event for the security state of this monitor. (optional)</td>
</tr>
</tbody>
</table>

The values marked as optional indicate capture event sources that can be omitted in an implementation. Those values representing non-implemented event sources must not trigger a capture event.

If capture is not implemented for the MBWU monitor type as indicated by MPAMF_MBWUMON_IDR.HAS_CAPTURE = 0, this field is RAZ/WI.

CAPT_RESET, bit [27]

Reset MSMON_MBWU.VALUE after capture.

Controls whether the VALUE field of the monitor instance is reset to zero immediately after being copied to the corresponding capture register.

<table>
<thead>
<tr>
<th>CAPT_RESET</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_MBWU.VALUE field of the monitor instance is not reset on capture.</td>
</tr>
<tr>
<td>0b1</td>
<td>MSMON_MBWU.VALUE field of the monitor instance is reset on capture.</td>
</tr>
</tbody>
</table>

If capture is not implemented for the MBWU monitor type as indicated by MPAMF_MBWUMON_IDR.HAS_CAPTURE = 0, this field is RAZ/WI.

This control bit affects both MSMON_MBWU and MSMON_MBWU_L in implementations that include MSMON_MBWU_L.

OFLOW_STATUS, bit [26]

Overflow status.

Indicates whether the value of MSMON_MBWU has overflowed.

<table>
<thead>
<tr>
<th>OFLOW_STATUS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_MBWU.VALUE has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>MSMON_MBWU.VALUE has overflowed at least once since this bit was last written to zero.</td>
</tr>
</tbody>
</table>

If overflow is not possible for an MBWU monitor in the MSC implementation, this field is RAZ/WI.

Overflow status for MSMON_MBWU_L.VALUE is reported in MSMON_CFG_MBWU_CTL.OFLOW_STATUS_L.

OFLOW_INTR, bit [25]

Enable interrupt on overflow of MSMON_MBWU.VALUE.

<table>
<thead>
<tr>
<th>OFLOW_INTR</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No interrupt is signaled on an overflow of MSMON_MBWU.VALUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>An implementation-specific interrupt is signaled on an overflow of MSMON_MBWU.VALUE.</td>
</tr>
</tbody>
</table>

If overflow is not possible for an MBWU monitor in the MSC implementation, this field is RAZ/WI.

If overflow interrupt is not supported by the MSC implementation, this field is RAZ/WI.
Interrupt enable for overflow of `MSMON_MBWU.VALUE` is controlled by `MSMON_CFG_MBWU_CTL.OFLOW_INTR_L`.

**OFLOW_FRZ, bit [24]**

Freeze monitor instance on overflow.

Controls whether `MSMON_MBWU.VALUE` field of the monitor instance freezes on an overflow.

<table>
<thead>
<tr>
<th>OFLOW_FRZ</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>MSMON_MBWU.VALUE</code> field of the monitor instance wraps on overflow.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>MSMON_MBWU.VALUE</code> field of the monitor instance freezes on overflow. If the increment that caused the overflow was 1, the frozen value is the post-increment value of 0. If the increment that caused the overflow was larger than 1, the frozen value of the monitor might be 0 or a larger value less than the final increment.</td>
</tr>
</tbody>
</table>

If overflow is not possible for the instance of the MBWU monitor in the implementation, this field is RAZ/WI.

This control bit affects both `MSMON_MBWU` and `MSMON_MBWU_L` in implementations that include `MSMON_MBWU_L`.

**SUBTYPE, bits [23:20]**

Subtype. Type of bandwidth counted by this monitor.

This field is not currently used for MBWU monitors, but reserved for future use.

This field is RAZ/WI.

**SCLEN, bit [19]**

`MSMON_MBWU.VALUE` Scaling Enable.

Enables scaling of `MSMON_MBWU.VALUE` by `MPAMF_MBWUMON_IDR.SCALE`.

<table>
<thead>
<tr>
<th>SCLEN</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td><code>MSMON_MBWU.VALUE</code> has bytes counted by the monitor instance.</td>
</tr>
<tr>
<td>0b1</td>
<td><code>MSMON_MBWU.VALUE</code> has bytes counted by the monitor instance, shifted right by <code>MPAMF_MBWUMON_IDR.SCALE</code>.</td>
</tr>
</tbody>
</table>

**Bit [18]**

Reserved, RES0.

**MATCH_PMG, bit [17]**

Match PMG.

Controls whether the monitor instance only counts data transferred with PMG matching `MSMON_CFG_MBWU_FLT.PMG`.

<table>
<thead>
<tr>
<th>MATCH_PMG</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance counts data transferred with any PMG value.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance only counts data transferred with the PMG value matching <code>MSMON_CFG_MBWU_FLT.PMG</code>.</td>
</tr>
</tbody>
</table>
MATCH_PARTID, bit [16]

Match PARTID.

Controls whether the monitor instance counts only data transferred with PARTID matching
MSMON_CFG_MBWU_FLT.PARTID.

<table>
<thead>
<tr>
<th>MATCH_PARTID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance counts data transferred with any PARTID value.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance only counts data transferred with the PARTID value matching MSMON_CFG_MBWU_FLT.PARTID.</td>
</tr>
</tbody>
</table>

OFLOW_STATUS_L, bit [15]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Overflow Status of MSMON_MBWU_L.VALUE of the monitor instance.

Indicates whether MSMON_MBWU_L.VALUE has overflowed.

<table>
<thead>
<tr>
<th>OFLOW_STATUS_L</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>MSMON_MBWU_L.VALUE has not overflowed.</td>
</tr>
<tr>
<td>0b1</td>
<td>MSMON_MBWU_L.VALUE has overflowed at least once since this bit was last written to zero.</td>
</tr>
</tbody>
</table>

If MPAMF_MBWUMON_IDR.HAS_LONG == 0, this bit is RES0.

Overflow status of MSMON_MBWU.VALUE is reported in MSMON_CFG_MBWU_CTL.OFLOW_STATUS.

Otherwise:

Reserved, RES0.

OFLOW_INTR_L, bit [14]

When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:

Overflow Interrupt for MSMON_MBWU.L.

Controls whether an MPAM overflow interrupt is generated when MSMON_MBWU.L.VALUE overflows.

<table>
<thead>
<tr>
<th>OFLOW_INTR_L</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No interrupt is signaled on an overflow of MSMON_MBWU.L.VALUE.</td>
</tr>
<tr>
<td>0b1</td>
<td>An implementation-specific interrupt is signalled on overflow of MSMON_MBWU.L.VALUE.</td>
</tr>
</tbody>
</table>

If overflow is not possible for an MBWU monitor in the MSC implementation, this field is RAZ/WI.

If the overflow interrupt is not supported by the MSC implementation, this field is RAZ/WI.

If MPAMF_MBWUMON_IDR.HAS_LONG == 0, this bit is RES0.

Otherwise:

Reserved, RES0.

Bits [13:8]

Reserved, RES0.
**TYPE, bits [7:0]**

Monitor Type Code. The MBWU monitor is TYPE = 0x42.

TYPE is a read-only constant indicating the type of the monitor.

Reads as 0x42.

**Accessing the MSMON_CONFIG_MBWU_CTL**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_CONFIG_MBWU_CTL_s must be accessible from the Secure MPAM feature page. MSMON_CONFIG_MBWU_CTL_ns must be accessible from the Non-secure MPAM feature page.

MSMON_CONFIG_MBWU_CTL_s and MSMON_CONFIG_MBWU_CTL_ns must be separate registers. The Secure instance (MSMON_CONFIG_MBWU_CTL_s) accesses the memory bandwidth usage monitor controls used for Secure PARTIDs, and the Non-secure instance (MSMON_CONFIG_MBWU_CTL_ns) accesses the memory bandwidth usage monitor controls used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MSMON_CONFIG_MBWU_CTL access the monitor configuration settings for the bandwidth resource instance selected by MSMON_CONFIG_MON_SEL.RIS and the memory bandwidth usage monitor instance selected by MSMON_CONFIG_MON_SEL.MON_SEL.

When RIS is not implemented, loads and stores to MSMON_CONFIG_MBWU_CTL access the monitor configuration settings for the memory bandwidth usage monitor instance selected by MSMON_CONFIG_MON_SEL.MON_SEL.

**MSMON_CONFIG_MBWU_CTL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0828</td>
<td>MSMON_CONFIG_MBWU_CTL_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0828</td>
<td>MSMON_CONFIG_MBWU_CTL_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

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MSMON_CFG_MBWU_FLT, MPAM Memory System Monitor Configure Memory Bandwidth Usage Monitor Filter Register

The MSMON_CFG_MBWU_FLT characteristics are:

**Purpose**

Controls PARTID and PMG to measure or count in the MBWU monitor selected by MSMON_CFG_MON_SEL. MSMON_CFG_MBWU_FLT sets filter conditions for the Secure memory bandwidth usage monitor instance selected by the Secure instance of MSMON_CFG_MON_SEL. MSMON_CFG_MBWU_CTL sets filter conditions for the Non-secure memory bandwidth usage monitor instance selected by the Non-secure instance of MSMON_CFG_MON_SEL.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance filter configuration accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_CFG_MBWU_FLT is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_MBWU == 1. Otherwise, direct accesses to MSMON_CFG_MBWU_FLT are RES0.

**Attributes**

MSMON_CFG_MBWU_FLT is a 32-bit register.

**Field descriptions**

The MSMON_CFG_MBWU_FLT bit assignments are:

**When FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented:**

<table>
<thead>
<tr>
<th>RWBW</th>
<th>RES0</th>
<th>PMG</th>
<th>PARTID</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
</tr>
<tr>
<td>27</td>
<td>26</td>
<td>25</td>
<td>24</td>
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<tr>
<td>23</td>
<td>22</td>
<td>21</td>
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<td>13</td>
<td>12</td>
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<td>11</td>
<td>10</td>
<td>9</td>
<td>8</td>
</tr>
<tr>
<td>7</td>
<td>6</td>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

RW filtering.

**RWBW, bits [31:30]**

When MPAMF_MBWUMON_IDR.HAS_RWBW == 1:

Read/write bandwidth filter. Configures the selected monitor instance to count all bandwidth, only read bandwidth or only write bandwidth.

<table>
<thead>
<tr>
<th>RWBW</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Monitor instance counts read bandwidth and write bandwidth.</td>
</tr>
<tr>
<td>0b01</td>
<td>Monitor instance counts write bandwidth only.</td>
</tr>
<tr>
<td>0b10</td>
<td>Monitor instance counts read bandwidth only.</td>
</tr>
<tr>
<td>0b11</td>
<td>Reserved.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.
Bits [29:24]

Reserved, RES0.

PMG, bits [23:16]

Performance monitoring group to filter memory bandwidth usage monitoring.

If `MSMON_CFG_MBWU_CTL.MATCH_PMG == 0`, this field is not used to match memory bandwidth to a PMG and the contents of this field is ignored.

If `MSMON_CFG_MBWU_CTL.MATCH_PMG == 1`, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts memory bandwidth labeled with PMG equal to this field.

PARTID, bits [15:0]

Partition ID to filter memory bandwidth usage monitoring.

If `MSMON_CFG_MBWU_CTL.MATCH_PARTID == 0`, this field is not used to match memory bandwidth to a PARTID and the contents of this field is ignored.

If `MSMON_CFG_MBWU_CTL.MATCH_PARTID == 1`, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts memory bandwidth labeled with PARTID equal to this field.

Otherwise:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
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<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>PMG</td>
<td>PARTID</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
</tbody>
</table>

Bits [31:24]

Reserved, RES0.

PMG, bits [23:16]

Performance monitoring group to filter memory bandwidth usage monitoring.

If `MSMON_CFG_MBWU_CTL.MATCH_PMG == 0`, this field is not used to match memory bandwidth to a PMG and the contents of this field is ignored.

If `MSMON_CFG_MBWU_CTL.MATCH_PMG == 1`, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts memory bandwidth labeled with PMG equal to this field.

PARTID, bits [15:0]

Partition ID to filter memory bandwidth usage monitoring.

If `MSMON_CFG_MBWU_CTL.MATCH_PARTID == 0`, this field is not used to match memory bandwidth to a PARTID and the contents of this field is ignored.

If `MSMON_CFG_MBWU_CTL.MATCH_PARTID == 1`, the monitor selected by `MSMON_CFG_MON_SEL` measures or counts memory bandwidth labeled with PARTID equal to this field.

Accessing the `MSMON_CFG_MBWUFLT`

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

`MSMON_CFG_MBWUFLT_s` must be accessible from the Secure MPAM feature page. `MSMON_CFG_MBWUFLT_ns` must be accessible from the Non-secure MPAM feature page.

`MSMON_CFG_MBWUFLT_s` and `MSMON_CFG_MBWUFLT_ns` must be separate registers. The Secure instance (`MSMON_CFG_MBWUFLT_s`) accesses the PARTID and PMG matching for a memory bandwidth usage monitor used
for Secure PARTIDs, and the Non-secure instance (MSMON_CFG_MBWU_FLT_ns) accesses the PARTID and PMG matching for a memory bandwidth usage monitor used for Non-secure PARTIDs.

When RIS is implemented, loads and stores to MSMON_CFG_MBWU_FLT access the monitor configuration settings for the bandwidth resource instance selected by MSMON_CFG_MON_SEL, RIS and the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL_MON_SEL.

When RIS is not implemented, loads and stores to MSMON_CFG_MBWU_FLT access the monitor configuration settings for the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL_MON_SEL.

**MSMON_CFG_MBWU_FLT can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0820</td>
<td>MSMON_CFG_MBWU_FLT_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0820</td>
<td>MSMON_CFG_MBWU_FLT_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
MSMON_CFG_MON_SEL, MPAM Monitor Instance Selection Register

The MSMON_CFG_MON_SEL characteristics are:

**Purpose**

Selects a monitor instance to access through the MSMON configuration and counter registers. MSMON_CFG_MON_SEL selects a Secure monitor instance to access via the Secure MPAM feature page. MSMON_CFG_MON_SEL_ns selects a Non-secure monitor instance to access via the Non-secure MPAM feature page.

**Note**

Different performance monitoring features within a MSC could have different numbers of monitor instances. See the NUM_MON field in the corresponding ID register. This means that a monitor out-of-bounds error might be signaled when an MSMON_CFG register is accessed because the value in MSMON_CFG_MON_SEL.MON_SEL is too large for the particular monitoring feature.

To configure a monitor, set MON_SEL in this register to the index of the monitor instance to configure, then write to the MSMON_CFG_x register to set the configuration of the monitor. At a later time, read the monitor register (for example MSMON_MBWU) to get the value of the monitor.

**Configuration**

The power domain of MSMON_CFG_MON_SEL is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented and (MPAMF_IDR.HAS_MSMON == 1, or (MPAMF_IDR.HAS_IMPL_IDR == 1 and MPAMF_IDR.EXT == 0) or (MPAMF_IDR.HAS_IMPL_IDR == 1, MPAMF_IDR.EXT == 1 and MPAMF_IDR.NO_IMPL_MSMON == 0)). Otherwise, direct accesses to MSMON_CFG_MON_SEL are RES0.

**Attributes**

MSMON_CFG_MON_SEL is a 32-bit register.

**Field descriptions**

The MSMON_CFG_MON_SEL bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| RIS | RES0| MON_SEL

**Bits [31:28]**

Reserved, RES0.

**RIS, bits [27:24]**

When (FEAT_MPAMv0p1 is implemented or FEAT_MPAMv1p1 is implemented), MPAMF_IDR.EXT == 1 and MPAMF_IDR.HAS_RIS == 1:

Resource Instance Selector. RIS selects one resource to configure through MSMON_CFG registers.
Otherwise:

Reserved, RES0.

**Bits [23:16]**

Reserved, RES0.

**MON_SEL, bits [15:0]**

Selects the monitor instance to configure or read.

Reads and writes to other MSMON registers are indexed by MON_SEL and by the NS bit used to access
MSMON_CFG_MON_SEL to access the configuration for a single monitor.

**Accessing the MSMON_CFG_MON_SEL**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_CFG_MON_SEL_s must be accessible from the Secure MPAM feature page. MSMON_CFG_MON_SEL_ns must be accessible from the Non-secure MPAM feature page.

MSMON_CFG_MON_SEL_s and MSMON_CFG_MON_SEL_ns must be separate registers. The Secure instance (MSMON_CFG_MON_SEL_s) accesses the monitor instance selector used for Secure PARTIDs, and the Non-secure instance (MSMON_CFG_MON_SEL_ns) accesses the monitor instance selector used for Non-secure PARTIDs.

**MSMON_CFG_MON_SEL can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0800</td>
<td>MSMON_CFG_MON_SEL_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0800</td>
<td>MSMON_CFG_MON_SEL_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
The MSMON_CSU characteristics are:

**Purpose**

Accesses the CSU monitor instance selected by `MSMON_CFG_MON_SEL`. MSMON_CSU_s is a Secure cache storage usage monitor instance selected by the Secure instance of `MSMON_CFG_MON_SEL`, MSMON_CSU_ns is a Non-secure cache storage usage monitor instance selected by the Non-secure instance of `MSMON_CFG_MON_SEL`.

If `MPAMF_IDR.HAS_RIS` is 1, the monitor instance accessed is for the resource instance currently selected by `MSMON_CFG_MON_SEL.RIS` and the monitor instance of that resource instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

**Configuration**

The power domain of MSMON_CSU is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, `MPAMF_IDR.HAS_MSMON` == 1 and `MPAMF_MSMON_IDR.MSMON_CSU` == 1. Otherwise, direct accesses to MSMON_CSU are RES0.

**Attributes**

MSMON_CSU is a 32-bit register.

**Field descriptions**

The MSMON_CSU bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>NRDY</td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
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<td>25</td>
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<td>24</td>
<td></td>
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<td>23</td>
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<td>22</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>VALUE</td>
</tr>
</tbody>
</table>

**NRDY, bit [31]**

Not Ready. Indicates whether the monitor instance has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is ready and the MSMON_CSU.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is not ready and the contents of the MSMON_CSU.VALUE field might be inaccurate or otherwise not represent the actual cache storage usage.</td>
</tr>
</tbody>
</table>

**VALUE, bits [30:0]**

Cache storage usage measurement value if MSMON_CSU.NRDY is 0. Invalid if MSMON_CSU.NRDY is 1.

VALUE is the cache storage usage measured in bytes meeting the criteria set in `MSMON_CFG_CSUFLT` and `MSMON_CFG_CSU_CTL` for the monitor instance selected by `MSMON_CFG_MON_SEL`.

**Accessing the MSMON_CSU**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.
MSMON_CSU_s must be accessible from the Secure MPAM feature page. MSMON_CSU_ns must be accessible from the Non-secure MPAM feature page.

MSMON_CSU_s and MSMON_CSU_ns must be separate registers. The Secure instance (MSMON_CSU_s) accesses the cache storage usage monitor used for Secure PARTIDs, and the Non-secure instance (MSMON_CSU_ns) accesses the cache storage usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to MSMON_CSU access the cache storage usage monitor monitor instance for the cache resource instance selected by MSMON_CFG_MON_SEL.RIS and the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, reads and writes to MSMON_CSU access the cache storage usage monitor monitor instance for the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**MSMON_CSU can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0840</td>
<td>MSMON_CSU_s</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When MPAMF_CSUMON_IDR.CSU_RO == 0 accesses to this register are RW.
- When MPAMF_CSUMON_IDR.CSU_RO == 1 accesses to this register are RO.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0840</td>
<td>MSMON_CSU_ns</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When MPAMF_CSUMON_IDR.CSU_RO == 0 accesses to this register are RW.
- When MPAMF_CSUMON_IDR.CSU_RO == 1 accesses to this register are RO.
MSMON_CSU_CAPTURE, MPAM Cache Storage Usage Monitor Capture Register

The MSMON_CSU_CAPTURE characteristics are:

**Purpose**

MSMON_CSU_CAPTURE is a 32-bit read-write register that accesses the captured MSMON_CSU monitor instance selected by MSMON_CFG_MON_SEL. MSMON_CSU_CAPTURE_s is the Secure cache storage usage monitor capture instance selected by the Secure instance of MSMON_CFG_MON_SEL. MSMON_CSU_CAPTURE_ns is the Non-secure cache storage usage monitor capture instance selected by the Non-secure instance of MSMON_CFG_MON_SEL.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance capture register accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_CSU_CAPTURE is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1, MPAMF_MSMON_IDR.MSMON_CSU == 1 and MPAMF_CSUMON_IDR.HAS_CAPTURE == 1. Otherwise, direct accesses to MSMON_CSU_CAPTURE are RES0.

**Attributes**

MSMON_CSU_CAPTURE is a 32-bit register.

**Field descriptions**

The MSMON_CSU_CAPTURE bit assignments are:

<table>
<thead>
<tr>
<th></th>
<th>NRDY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td></td>
<td></td>
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<tr>
<td>30</td>
<td></td>
<td></td>
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<td>2</td>
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<td></td>
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<tr>
<td>1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NRDY, bit [31]**

Not Ready. Indicates whether the captured monitor value has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The captured monitor instance was ready and the MSMON_CSU_CAPTURE.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The captured monitor instance was not ready and the contents of the MSMON_CSU_CAPTURE.VALUE field might be inaccurate or otherwise not represent the actual cache storage usage.</td>
</tr>
</tbody>
</table>

**VALUE, bits [30:0]**

Captured cache storage usage measurement if MSMON_CSU_CAPTURE.NRDY is 0. Invalid if MSMON_CSU_CAPTURE.NRDY is 1.

VALUE is the captured cache storage usage measurement in bytes meeting the criteria set in MSMON_CFG_CSU_FLT and MSMON_CFG_CSU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.
Accessing the MSMON_CSU_CAPTURE

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_CSU_CAPTURE_s must be accessible from the Secure MPAM feature page. MSMON_CSU_CAPTURE_ns must be accessible from the Non-secure MPAM feature page.

MSMON_CSU_CAPTURE_s and MSMON_CSU_CAPTURE_ns must be separate registers. The Secure instance (MSMON_CSU_CAPTURE_s) accesses the captured cache storage usage monitor used for Secure PARTIDs, and the Non-secure instance (MSMON_CSU_CAPTURE_ns) accesses the captured cache storage usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to MSMON_CSU_CAPTURE access the monitor instance for the cache resource instance selected by MSMON_CFG_MON_SEL.RIS and the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, reads and writes to MSMON_CSU_CAPTURE access the monitor instance for the cache storage usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

MSMON_CSU_CAPTURE can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0848</td>
<td>MSMON_CSU_CAPTURE_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0848</td>
<td>MSMON_CSU_CAPTURE_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
MSMON_MBWU, MPAM Memory Bandwidth Usage Monitor Register

The MSMON_MBWU characteristics are:

**Purpose**

Accesses the monitor instance selected by MSMON_CFG_MON_SEL. MSMON_MBWU_s is the Secure memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL_s. MSMON_MBWU_ns is the Non-secure memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL_ns.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance register accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_MBWU is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1 and MPAMF_MSMON_IDR.MSMON_MBWU == 1. Otherwise, direct accesses to MSMON_MBWU are RES0.

**Attributes**

MSMON_MBWU is a 32-bit register.

**Field descriptions**

The MSMON_MBWU bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
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<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>NRDY</td>
<td>VALUE</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>

**NRDY, bit [31]**

Not Ready. Indicates whether the monitor has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is ready and the MSMON_MBWU.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is not ready and the contents of the MSMON_MBWU.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

**VALUE, bits [30:0]**

Memory bandwidth usage counter value if MSMON_MBWU.NRDY is 0. Invalid if MSMON_MBWU.NRDY is 1.

VALUE is the scaled count of bytes transferred since the monitor was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.

If MSMON_CFG_MBWU_CTL.SCLEN enables scaling, the count in VALUE is the number of bytes shifted right by MPAMF_MBWUMON_IDR.SCALE bit positions and rounded.
**Accessing the MSMON_MBWU**

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_MBWU_s must be accessible from the Secure MPAM feature page. MSMON_MBWU_ns must be accessible from the Non-secure MPAM feature page.

MSMON_MBWU_s and MSMON_MBWU_ns must be separate registers. The Secure instance (MSMON_MBWU_s) accesses the memory bandwidth usage monitor used for Secure PARTIDs, and the Non-secure instance (MSMON_MBWU_ns) accesses the memory bandwidth usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to MSMON_MBWU access the memory bandwidth usage monitor instance for the resource instance selected by MSMON_CFG_MON_SEL.RIS and the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, reads and writes to MSMON_MBWU access the memory bandwidth usage monitor instance for the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**MSMON_MBWU can be accessed through the memory-mapped interfaces:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0860</td>
<td>MSMON_MBWU_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0860</td>
<td>MSMON_MBWU_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
MSMON_MBWU_CAPTURE, MPAM Memory Bandwidth Usage Monitor Capture Register

The MSMON_MBWU_CAPTURE characteristics are:

**Purpose**

Accesses the captured MSMON_MBWU monitor instance selected by `MSMON_CFG_MON_SEL`. MSMON_MBWU_CAPTURE_s is the Secure memory bandwidth usage monitor capture instance selected by the Secure instance of `MSMON_CFG_MON_SEL`. MSMON_MBWU_CAPTURE_ns is the Non-secure memory bandwidth usage monitor capture instance selected by the Non-secure instance of `MSMON_CFG_MON_SEL`.

If `MPAMF_IDR.HAS_RIS` is 1, the monitor instance capture register accessed is for the resource instance currently selected by `MSMON_CFG_MON_SEL.RIS` and the monitor instance of that resource instance selected by `MSMON_CFG_MON_SEL.MON_SEL`.

**Configuration**

The power domain of MSMON_MBWU_CAPTURE is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1, MPAMF_MSMON_IDR.MSMON_MBWU == 1 and MPAMF_MBWUMON_IDR.HAS_CAPTURE == 1. Otherwise, direct accesses to MSMON_MBWU_CAPTURE are RES0.

**Attributes**

MSMON_MBWU_CAPTURE is a 32-bit register.

**Field descriptions**

The MSMON_MBWU_CAPTURE bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>NRDY Not Ready. The captured NRDY bit from the corresponding instance of MSMON_MBWU. This bit indicates whether the captured monitor value has possibly inaccurate data.</td>
</tr>
<tr>
<td>30-0</td>
<td>VALUE Captured memory bandwidth usage counter value if MSMON_MBWU_CAPTURE.NRDY is 0. Invalid if MSMON_MBWU_CAPTURE.NRDY is 1.</td>
</tr>
</tbody>
</table>

**NRDY, bit [31]**

Not Ready. The captured NRDY bit from the corresponding instance of MSMON_MBWU. This bit indicates whether the captured monitor value has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The captured monitor instance was ready and the MSMON_MBWU_CAPTURE.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The captured monitor instance was not ready and the contents of the MSMON_MBWU_CAPTURE.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

**VALUE, bits [30:0]**

Captured memory bandwidth usage counter value if MSMON_MBWU_CAPTURE.NRDY is 0. Invalid if MSMON_MBWU_CAPTURE.NRDY is 1.

VALUE is the captured VALUE field from the corresponding instance of MSMON_MBWU, the count of bytes transferred since the monitor was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.
VALUE captures the **MSMON_MBWU(VALUE)** and preserves any scaling that had been performed on the VALUE field in that register.

### Accessing the MSMON_MBWU_CAPTURE

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

**MSMON_MBWU_CAPTURE_s** must be accessible from the Secure MPAM feature page. **MSMON_MBWU_CAPTURE_ns** must be accessible from the Non-secure MPAM feature page.

**MSMON_MBWU_CAPTURE_s** and **MSMON_MBWU_CAPTURE_ns** must be separate registers. The Secure instance (**MSMON_MBWU_CAPTURE_s**) accesses the captured memory bandwidth usage monitor used for Secure PARTIDs, and the Non-secure instance (**MSMON_MBWU_CAPTURE_ns**) accesses the captured memory bandwidth usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to **MSMON_MBWU_CAPTURE** access the monitor instance for the bandwidth resource instance selected by **MSMON_CFG_MON_SEL.RIS** and the memory bandwidth usage monitor instance selected by **MSMON_CFG_MON_SEL.MON_SEL**.

When RIS is not implemented, reads and writes to **MSMON_MBWU_CAPTURE** access the monitor instance for the memory bandwidth usage monitor instance selected by **MSMON_CFG_MON_SEL.MON_SEL**.

**MSMON_MBWU_CAPTURE** can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0868</td>
<td>MSMON_MBWU_CAPTURE_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0868</td>
<td>MSMON_MBWU_CAPTURE_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
MSMON_MBWU_L, MPAM Long Memory Bandwidth Usage Monitor Register

The MSMON_MBWU_L characteristics are:

**Purpose**

Accesses the monitor instance selected by MSMON_CFG_MON_SEL. MSMON_MBWU_L is the Secure memory bandwidth usage monitor instance selected by the Secure instance of MSMON_CFG_MON_SEL. MSMON_MBWU_L_ns is the Non-secure memory bandwidth usage monitor instance selected by the Non-secure instance of MSMON_CFG_MON_SEL.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance long monitor register accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_MBWU_L is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1, MPAMF_MSMON_IDR.MSMON_MBWU == 1 and MPAMF_MBWUMON_IDR.HAS_LONG == 1. Otherwise, direct accesses to MSMON_MBWU_L are RES0.

**Attributes**

MSMON_MBWU_L is a 64-bit register.

**Field descriptions**

The MSMON_MBWU_L bit assignments are:

When MPAMF_MBWUMON_IDR.LWD == 0:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>NRDY, bit [63]</td>
</tr>
<tr>
<td>62</td>
<td>Not Ready. Indicates whether the monitor instance has possibly inaccurate data.</td>
</tr>
<tr>
<td>61</td>
<td>60</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
</tr>
</tbody>
</table>

NRDY, bit [63]

Not Ready. Indicates whether the monitor instance has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is ready and the MSMON_MBWU_L.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is not ready and the contents of the MSMON_MBWU_L.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

Bits [62:44]

Reserved, RES0.
VALUE, bits [43:0]

Long (44-bit) memory bandwidth usage counter value if MSMON_MBWU_L.NRDY is 0. Invalid if MSMON_MBWU_L.NRDY is 1.

VALUE is the long count of bytes transferred since the monitor was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.

When MPAMF_MBWMON_IDR.LWD == 1:

<table>
<thead>
<tr>
<th>NRDY</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
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<tr>
<td>33</td>
<td></td>
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<tr>
<td>32</td>
<td></td>
</tr>
</tbody>
</table>

NRDY, bit [63]

Not Ready. Indicates whether the monitor instance has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The monitor instance is ready and the MSMON_MBWU_L.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The monitor instance is not ready and the contents of the MSMON_MBWU_L.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

VALUE, bits [62:0]

Long (63-bit) memory bandwidth usage counter value if MSMON_MBWU_L.NRDY is 0. Invalid if MSMON_MBWU_L.NRDY is 1.

VALUE is the long count of bytes transferred since the monitor instance was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.

Accessing the MSMON_MBWU_L

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_MBWU_L_s must be accessible from the Secure MPAM feature page. MSMON_MBWU_L_ns must be accessible from the Non-secure MPAM feature page.

MSMON_MBWU_L_s and MSMON_MBWU_L_ns must be separate registers. The Secure instance (MSMON_MBWU_L_s) accesses the long memory bandwidth usage monitor used for Secure PARTIDs, and the Non-secure instance (MSMON_MBWU_L_ns) accesses the long memory bandwidth usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to MSMON_MBWU_L access the long memory bandwidth usage monitor instance for the bandwidth resource instance selected by MSMON_CFG_MON_SEL.RIS and the monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, reads and writes to MSMON_MBWU_L access the long memory bandwidth usage monitor instance for the monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

MSMON_MBWU_L can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0880</td>
<td>MSMON_MBWU_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
Accesses on this interface are **RW**.

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0080</td>
<td>MSMON_MBWU_ns</td>
</tr>
</tbody>
</table>
The MSMON_MBWU_L_CAPTURE characteristics are:

**Purpose**

Accesses the captured MSMON_MBWU_L monitor instance selected by MSMON_CFG_MON_SEL.

MSMON_MBWU_L_CAPTURE_s is the Secure memory bandwidth usage monitor capture instance selected by the Secure instance of MSMON_CFG_MON_SEL.

MSMON_MBWU_L_CAPTURE_ns is the Non-secure memory bandwidth usage monitor capture instance selected by the Non-secure instance of MSMON_CFG_MON_SEL.

If MPAMF_IDR.HAS_RIS is 1, the monitor instance long capture register accessed is for the resource instance currently selected by MSMON_CFG_MON_SEL.RIS and the monitor instance of that resource instance selected by MSMON_CFG_MON_SEL.MON_SEL.

**Configuration**

The power domain of MSMON_MBWU_L_CAPTURE is IMPLEMENTATION DEFINED.

This register is present only when FEAT_MPAM is implemented, MPAMF_IDR.HAS_MSMON == 1, MPAMF_MSMON_IDR.MSMON_MBWU == 1, MPAMF_MBWUMON_IDR.HAS_CAPTURE == 1 and MPAMF_MBWUMON_IDR.HAS_LONG == 1. Otherwise, direct accesses to MSMON_MBWU_L_CAPTURE are RES0.

**Attributes**

MSMON_MBWU_L_CAPTURE is a 64-bit register.

**Field descriptions**

The MSMON_MBWU_L_CAPTURE bit assignments are:

**When MPAMF_MBWUMON_IDR.LWD == 0:**

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>NRDY, bit [63]</td>
</tr>
<tr>
<td>62</td>
<td>Not Ready. Indicates whether the monitor has possibly inaccurate data.</td>
</tr>
<tr>
<td>61</td>
<td>The captured monitor instance was ready and the MSMON_MBWU_L_CAPTURE.VALUE field is accurate.</td>
</tr>
<tr>
<td>60</td>
<td>The captured monitor instance was not ready and the contents of the MSMON_MBWU_L_CAPTURE.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

**Bits [62:44]**

Reserved, RES0.
VALUE, bits [43:0]

Captured long memory bandwidth usage counter value if MSMON_MBWU_L_CAPTURE.NRDY is 0. Invalid if MSMON_MBWU_L_CAPTURE.NRDY is 1.

VALUE is the captured 44-bit count of bytes transferred since the monitor instance was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.

When MPAMF_MBWUMON_IDR.LWD == 1:

<table>
<thead>
<tr>
<th></th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VALUE</td>
</tr>
<tr>
<td>63</td>
<td>62</td>
</tr>
<tr>
<td>61</td>
<td>60</td>
</tr>
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<td>59</td>
<td>58</td>
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<td>39</td>
<td>38</td>
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<td>37</td>
<td>36</td>
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<td>35</td>
<td>34</td>
</tr>
<tr>
<td>33</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>NRDY</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
</tr>
<tr>
<td>29</td>
<td>28</td>
</tr>
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<td>27</td>
<td>26</td>
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<td>11</td>
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<td>8</td>
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<td>7</td>
<td>6</td>
</tr>
<tr>
<td>5</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

NRDY, bit [63]

Not Ready. Indicates whether the monitor has possibly inaccurate data.

<table>
<thead>
<tr>
<th>NRDY</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The captured monitor instance was ready and the MSMON_MBWU_L_CAPTURE.VALUE field is accurate.</td>
</tr>
<tr>
<td>0b1</td>
<td>The captured monitor instance was not ready and the contents of the MSMON_MBWU_L_CAPTURE.VALUE field might be inaccurate or otherwise not represent the actual memory bandwidth usage.</td>
</tr>
</tbody>
</table>

VALUE, bits [62:0]

The captured long memory bandwidth usage counter value if MSMON_MBWU_L_CAPTURE.NRDY is 0. Invalid if MSMON_MBWU_L_CAPTURE.NRDY is 1.

VALUE is the captured 63-bit count of bytes transferred since the monitor instance was last reset that meet the criteria set in MSMON_CFG_MBWU_FLT and MSMON_CFG_MBWU_CTL for the monitor instance selected by MSMON_CFG_MON_SEL.

Accessing the MSMON_MBWU_L_CAPTURE

This register is within the MPAM feature page memory frames. In a system that supports Secure and Non-secure memory maps, there must be both Secure and Non-secure MPAM feature pages.

MSMON_MBWU_L_CAPTURE_s must be accessible from the Secure MPAM feature page.

MSMON_MBWU_L_CAPTURE_ns must be accessible from the Non-secure MPAM feature page.

MSMON_MBWU_L_CAPTURE_s and MSMON_MBWU_L_CAPTURE_ns must be separate registers. The Secure instance (MSMON_MBWU_L_CAPTURE_s) accesses the captured long memory bandwidth usage monitor used for Secure PARTIDs, and the Non-secure instance (MSMON_MBWU_L_CAPTURE_ns) accesses the captured long memory bandwidth usage monitor used for Non-secure PARTIDs.

When RIS is implemented, reads and writes to MSMON_MBWU_L_CAPTURE access the monitor instance for the bandwidth resource instance selected by MSMON_CFG_MON_SEL.RIS and the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

When RIS is not implemented, reads and writes to MSMON_MBWU_L_CAPTURE access the monitor instance for the memory bandwidth usage monitor instance selected by MSMON_CFG_MON_SEL.MON_SEL.

MSMON_MBWU_L_CAPTURE can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_s</td>
<td>0x0890</td>
<td>MSMON_MBWU_CAPTURE_s</td>
</tr>
</tbody>
</table>

Accesses on this interface are RW.
<table>
<thead>
<tr>
<th>Component</th>
<th>Frame</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>MPAM</td>
<td>MPAMF_BASE_ns</td>
<td>0x0890</td>
<td>MSMON_MBWU_CAPTURE_ns</td>
</tr>
</tbody>
</table>

Accesses on this interface are **RW**.
OSLAR_EL1, OS Lock Access Register

The OSLAR_EL1 characteristics are:

**Purpose**

Used to lock or unlock the OS lock.

**Configuration**

External register OSLAR_EL1 bits [31:0] are architecturally mapped to AArch64 System register OSLAR_EL1[31:0].

External register OSLAR_EL1 bits [31:0] are architecturally mapped to AArch32 System register DBGOSLAR[31:0].

OSLAR_EL1 is in the Core power domain.

If FEAT_Debugv8p2 is not implemented, it is IMPLEMENTATION DEFINED whether external debug accesses to OSLAR_EL1 are ignored and return an error when AllowExternalDebugAccess() returns FALSE for the access.

If FEAT_Debugv8p2 is implemented, external debug accesses to OSLAR_EL1 are ignored and return an error when AllowExternalDebugAccess() returns FALSE for the access.

**Attributes**

OSLAR_EL1 is a 32-bit register.

**Field descriptions**

The OSLAR_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>29</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>28</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>27</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>26</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>25</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>24</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>23</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>22</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>21</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>20</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>19</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>18</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>17</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>16</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>15</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>14</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>13</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>12</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>11</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>10</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>9</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>6</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>5</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>4</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>3</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>2</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>1</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>0</td>
<td>Reserved, RES0.</td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reserved, RES0.

**OSLK, bit [0]**

On writes to OSLAR_EL1, bit[0] is copied to the OS lock.

Use EDPRSR. OSLK to check the current status of the lock.

**Accessing the OSLAR_EL1**

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalDebugAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

OSLAR_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Debug</td>
<td>0x300</td>
<td>OSLAR_EL1</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When \texttt{IsCorePowered()}, \texttt{!DoubleLockStatus()}, \texttt{AllowExternalDebugAccess()} and \texttt{SoftwareLockStatus()} accesses to this register are \texttt{WI}.
- When \texttt{IsCorePowered()}, \texttt{!DoubleLockStatus()}, \texttt{AllowExternalDebugAccess()} and \texttt{!SoftwareLockStatus()} accesses to this register are \texttt{WO}.
- When \texttt{IsCorePowered()}, \texttt{!DoubleLockStatus()}, \texttt{!AllowExternalDebugAccess()} and \texttt{FEAT_Debugv8p2} is not implemented accesses to this register are \texttt{IMPDEF}.
- Otherwise accesses to this register generate an error response.
PMAUTHSTATUS, Performance Monitors Authentication Status register

The PMAUTHSTATUS characteristics are:

**Purpose**

Provides information about the state of the IMPLEMENTATION DEFINED authentication interface for Performance Monitors.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is OPTIONAL, and is required for CoreSight compliance. Arm recommends that this register is implemented.

**Attributes**

PMAUTHSTATUS is a 32-bit register.

**Field descriptions**

The PMAUTHSTATUS bit assignments are:

<table>
<thead>
<tr>
<th>Bit assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7-6</td>
<td>SNID, holds the same value as DBGAUTHSTATUS_EL1.SNID.</td>
</tr>
<tr>
<td>5-4</td>
<td>SID, secure invasive debug. Possible values:</td>
</tr>
<tr>
<td>3-2</td>
<td>NSNID, holds the same value as DBGAUTHSTATUS_EL1.NSNID.</td>
</tr>
<tr>
<td>1-0</td>
<td>NSID, non-secure invasive debug. Possible values:</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SNID, bits [7:6]**

Holds the same value as DBGAUTHSTATUS_EL1.SNID.

**SID, bits [5:4]**

Secure invasive debug. Possible values:

<table>
<thead>
<tr>
<th>SID</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b00</td>
<td>Not implemented.</td>
</tr>
</tbody>
</table>

All other values are reserved.

**NSNID, bits [3:2]**

Holds the same value as DBGAUTHSTATUS_EL1.NSNID.

**NSID, bits [1:0]**

Non-secure invasive debug. Possible values:
All other values are reserved.

Accessing the PMAUTHSTATUS

PMAUTHSTATUS can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFB8</td>
<td>PMAUTHSTATUS</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMCCFILTR_EL0, Performance Monitors Cycle Counter Filter Register

The PMCCFILTR_EL0 characteristics are:

**Purpose**

Determines the modes in which the Cycle Counter, PMCCNTR_EL0, increments.

**Configuration**

External register PMCCFILTR_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMCCFILTR_EL0[31:0].

External register PMCCFILTR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCCFILTR[31:0].

PMCCFILTR_EL0 is in the Core power domain.

On a Warm or Cold reset, RW fields in this register reset:

- To architecturally **UNKNOWN** values if the reset is to an Exception level that is using AArch64.
- To 0 if the reset is to an Exception level that is using AArch32.

The register is not affected by an External debug reset.

**Attributes**

PMCCFILTR_EL0 is a 32-bit register.

**Field descriptions**

The PMCCFILTR_EL0 bit assignments are:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| P  | U  | NSK | NSU | NSH | M  | RES0 | SH | RES0 |
```

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMCCFILTR_EL0.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL1.</td>
</tr>
</tbody>
</table>

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMCCFILTR_EL0.NSU bit.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count cycles in EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count cycles in EL0.</td>
</tr>
</tbody>
</table>
NSK, bit [29]

When EL3 is implemented:

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of the PMCCFILTR_EL0.P bit, cycles in Non-secure EL1 are counted.
Otherwise, cycles in Non-secure EL1 are not counted.

Otherwise:

Reserved, RES0.

NSU, bit [28]

When EL3 is implemented:

Non-secure EL0 (Unprivileged) filtering bit. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of the PMCCFILTR_EL0.U bit, cycles in Non-secure EL0 are counted.
Otherwise, cycles in Non-secure EL0 are not counted.

Otherwise:

Reserved, RES0.

NSH, bit [27]

When EL2 is implemented:

EL2 (Hypervisor) filtering bit. Controls counting in EL2.

If FEAT_SEL2 and EL3 are implemented, counting in Secure EL2 is further controlled by the PMCCFILTR_EL0.SH bit.

<table>
<thead>
<tr>
<th>NSH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not count cycles in EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count cycles in EL2.</td>
</tr>
</tbody>
</table>

Otherwise:

Reserved, RES0.

M, bit [26]

When EL3 is implemented:

Secure EL3 filtering bit.

If the value of this bit is equal to the value of the PMCCFILTR_EL0.P bit, cycles in Secure EL3 are counted.
Otherwise, cycles in Secure EL3 are not counted.

Most applications can ignore this field and set its value to 0.

Note

This field is not visible in the AArch32 PMCCFILTR System register.
Otherwise:

Reserved, RES0.

**Bit [25]**

Reserved, RES0.

**SH, bit [24]**

*When FEAT_SEL2 is implemented and EL3 is implemented:*

Secure EL2 filtering.

If the value of this bit is not equal to the value of the PMCCFILTR_EL0.NSH bit, cycles in Secure EL2 are counted.

Otherwise, cycles in Secure EL2 are not counted.

If Secure EL2 is disabled, this field is RES0.

**Note**

This field is not visible in the AArch32 PMCCFILTR System register.

Otherwise:

Reserved, RES0.

**Bits [23:0]**

Reserved, RES0.

**Accessing the PMCCFILTR_EL0**

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

**PMCCFILTR_EL0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x47C</td>
<td>PMCCFILTR_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
PMCCNTR_EL0, Performance Monitors Cycle Counter

The PMCCNTR_EL0 characteristics are:

Purpose

Holds the value of the processor Cycle Counter, CCNT, that counts processor clock cycles. For more information, see 'Time as measured by the Performance Monitors cycle counter'.

PMCCFILTR_EL0 determines the modes and states in which the PMCCNTR_EL0 can increment.

Configuration

External register PMCCNTR_EL0 bits [63:0] are architecturally mapped to AArch64 System register PMCCNTR_EL0[63:0].

External register PMCCNTR_EL0 bits [63:0] are architecturally mapped to AArch32 System register PMCCNTR[63:0].

PMCCNTR_EL0 is in the Core power domain.

Attributes

PMCCNTR_EL0 is a 64-bit register.

Field descriptions

The PMCCNTR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Assignment</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>CCNT</td>
</tr>
<tr>
<td>62</td>
<td>CCNT</td>
</tr>
<tr>
<td>61</td>
<td></td>
</tr>
<tr>
<td>60</td>
<td></td>
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<td>59</td>
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<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

CCNT, bits [63:0]

Cycle count. Depending on the values of PMCR_EL0.{LC,D}, the cycle count increments in one of the following ways:

- Every processor clock cycle.
- Every 64th processor clock cycle.

Writing 1 to PMCR_EL0.C sets this field to 0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the PMCCNTR_EL0

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMCCNTR_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x0F8</td>
<td>PMCCNTR_EL0</td>
<td>31:0</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x0FC</td>
<td>PMCCNTR_EL0</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
PMCEID0, Performance Monitors Common Event Identification register 0

The PMCEID0 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x0000 to 0x001F

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

For more information about the common events and the use of the PMCEIDn registers, see ‘The PMU event number space and common events’.

**Note**

- Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.
- This view of the register was previously called PMCEID0_EL0.

**Configuration**

External register PMCEID0 bits [31:0] are architecturally mapped to AArch64 System register PMCEID0_EL0[31:0].

External register PMCEID0 bits [31:0] are architecturally mapped to AArch32 System register PMCEID0[31:0].

PMCEID0 is in the Core power domain.

**Attributes**

PMCEID0 is a 32-bit register.

**Field descriptions**

The PMCEID0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| D31 | D30 | D29 | D28 | D27 | D26 | D25 | D24 | D23 | D22 | D21 | D20 | D19 | D18 | D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

ID<n>, bit [n], for n = 31 to 0

ID[n] corresponds to common event n.

For each bit:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n> registers of that earlier version of the PMU architecture.
Accessing the PMCEID0

Note

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMCEID0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE20</td>
<td>PMCEID0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and AllowExternalPMUAccess() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMCEID1, Performance Monitors Common Event Identification register 1

The PMCEID1 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x020 to 0x03F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

For more information about the common events and the use of the PMCEIDn registers, see ‘The PMU event number space and common events’.

**Note**

- Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.
- This view of the register was previously called PMCEID1_EL0.

**Configuration**

External register PMCEID1 bits [31:0] are architecturally mapped to AArch64 System register PMCEID1_EL0[31:0].

External register PMCEID1 bits [31:0] are architecturally mapped to AArch32 System register PMCEID1[31:0].

PMCEID1 is in the Core power domain.

**Attributes**

PMCEID1 is a 32-bit register.

**Field descriptions**

The PMCEID1 bit assignments are:

<table>
<thead>
<tr>
<th>ID&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**

Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n> registers of that earlier version of the PMU architecture.
Accessing the PMCEID1

Note

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMCEID1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE24</td>
<td>PMCEID1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and AllowExternalPMUAccess() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMCEID2, Performance Monitors Common Event Identification register 2

The PMCEID2 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x4000 to 0x401F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

---

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

For more information about the common events and the use of the PMCEIDn registers, see 'The PMU event number space and common events'.

**Configuration**

External register PMCEID2 bits [31:0] are architecturally mapped to AArch64 System register PMCEID0_EL0[63:32].

External register PMCEID2 bits [63:32] are architecturally mapped to AArch32 System register PMCEID2[31:0].

PMCEID2 is in the Core power domain.

This register is present only when FEAT_PMUv3p1 is implemented. Otherwise, direct accesses to PMCEID2 are RES0.

**Attributes**

PMCEID2 is a 32-bit register.

**Field descriptions**

The PMCEID2 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dhi31</td>
<td>Dhi30</td>
<td>Dhi29</td>
<td>Dhi28</td>
<td>Dhi27</td>
<td>Dhi26</td>
<td>Dhi25</td>
<td>Dhi24</td>
<td>Dhi23</td>
<td>Dhi22</td>
<td>Dhi21</td>
<td>Dhi20</td>
<td>Dhi19</td>
<td>Dhi18</td>
<td>Dhi17</td>
<td>Dhi16</td>
<td>Dhi15</td>
</tr>
</tbody>
</table>

DHi<n>, bit [n], for n = 31 to 0

DHi[n] corresponds to common event (0x4000 + n).

For each bit:

<table>
<thead>
<tr>
<th>IDHi&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

---

**Note**
Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n> registers of that earlier version of the PMU architecture.

## Accessing the PMCEID2

**Note**

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

### PMCEID2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE28</td>
<td>PMCEID2</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and AllowExternalPMUAccess() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMCEID3, Performance Monitors Common Event Identification register 3

The PMCEID3 characteristics are:

**Purpose**

Defines which common architectural events and common microarchitectural events are implemented, or counted, using PMU events in the range 0x4020 to 0x403F.

When the value of a bit in the register is 1 the corresponding common event is implemented and counted.

**Note**

Arm recommends that, if a common event is never counted, the value of the corresponding register bit is 0.

For more information about the common events and the use of the PMCEIDn registers, see ‘The PMU event number space and common events’.

**Configuration**

External register PMCEID3 bits [31:0] are architecturally mapped to AArch64 System register PMCEID1_EL0[63:32].

External register PMCEID3 bits [63:32] are architecturally mapped to AArch32 System register PMCEID3[31:0].

PMCEID3 is in the Core power domain.

This register is present only when FEAT_PMUv3p1 is implemented. Otherwise, direct accesses to PMCEID3 are RES0.

**Attributes**

PMCEID3 is a 32-bit register.

**Field descriptions**

The PMCEID3 bit assignments are:

```
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15
IDhi31|IDhi30|IDhi29|IDhi28|IDhi27|IDhi26|IDhi25|IDhi24|IDhi23|IDhi22|IDhi21|IDhi20|IDhi19|IDhi18|IDhi17|IDhi16|IDhi15|D
```

IDhi\[n\], bit [n], for n = 31 to 0

IDhi[n] corresponds to common event (0x4020 + n).

For each bit:

```
<table>
<thead>
<tr>
<th>IDhi[n]</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>The common event is not implemented, or not counted.</td>
</tr>
<tr>
<td>0b1</td>
<td>The common event is implemented.</td>
</tr>
</tbody>
</table>
```

A bit that corresponds to a reserved event number is reserved. The value might be used in a future revision of the architecture to identify an additional common event.

**Note**
Such an event might be added retrospectively to an earlier version of the PMU architecture, provided the event does not require any additional PMU features and has an event number that can be represented in the PMCEID<n> registers of that earlier version of the PMU architecture.

### Accessing the PMCEID3

**Note**

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

**PMCEID3 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE2C</td>
<td>PMCEID3</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and AllowExternalPMUAccess() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMCFGR, Performance Monitors Configuration Register

The PMCFGR characteristics are:

**Purpose**

Contains PMU-specific configuration data.

**Configuration**

PMCFGR is in the Core power domain.

**Attributes**

PMCFGR is a 32-bit register.

**Field descriptions**

The PMCFGR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| NCG | RES0 | FZO | RES0 | UEN | WT | NA | EXC | CCD | CC | SIZE | N |

**NCG, bits [31:28]**

This feature is not supported, so this field is RAZ.

**Bits [27:22]**

Reserved, RES0.

**FZO, bit [21]**

Freeze-on-overflow supported. Defined values are:

<table>
<thead>
<tr>
<th>FZO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Freeze-on-overflow mechanism not supported. PMCR_EL0.FZO is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Freeze-on-overflow mechanism supported. PMCR_EL0.FZO is RW.</td>
</tr>
</tbody>
</table>

Accessing this field has the following behavior:

- When FEAT_PMUv3p7 is implemented, access to this field is RAO/WI.
- When FEAT_PMUv3p7 is not implemented, access to this field is RAZ/WI.

**Bit [20]**

Reserved, RES0.

**UEN, bit [19]**

User-mode Enable Register supported. PMUSERENR_EL0 is not visible in the external debug interface, so this bit is RAZ.
WT, bit [18]

This feature is not supported, so this bit is RAZ.

NA, bit [17]

This feature is not supported, so this bit is RAZ.

EX, bit [16]

Export supported. Value is IMPLEMENTATION DEFINED.

<table>
<thead>
<tr>
<th>EX</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PMCR_EL0.X is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMCR_EL0.X is read/write.</td>
</tr>
</tbody>
</table>

CCD, bit [15]

Cycle counter has prescale.

This is RES1 if AArch32 is supported at any Exception level, and RAZ otherwise.

<table>
<thead>
<tr>
<th>CCD</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>PMCR_EL0.D is RES0.</td>
</tr>
<tr>
<td>0b1</td>
<td>PMCR_EL0.D is read/write.</td>
</tr>
</tbody>
</table>

CC, bit [14]

Dedicated cycle counter (counter 31) supported. This bit is RAO.

SIZE, bits [13:8]

Size of counters, minus one. This field defines the size of the largest counter implemented by the Performance Monitors Unit.

From Armv8, the largest counter is 64-bits, so the value of this field is 0b111111.

This field is used by software to determine the spacing of the counters in the memory-map. From Armv8, the counters are a doubleword-aligned addresses.

N, bits [7:0]

Number of counters implemented in addition to the cycle counter, PMCCNTR_EL0. The maximum number of event counters is 31.

<table>
<thead>
<tr>
<th>N</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00</td>
<td>Only PMCCNTR_EL0 implemented.</td>
</tr>
<tr>
<td>0x01</td>
<td>PMCCNTR_EL0 plus one event counter implemented.</td>
</tr>
</tbody>
</table>

and so on up to 0b00011111, which indicates PMCCNTR_EL0 and 31 event counters implemented.

Accessing the PMCFGR

**Note**

AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.
**PMCFGR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE00</td>
<td>PMCFGR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When `IsCorePowered()`, `!DoubleLockStatus()`, `!OSLockStatus()` and `AllowExternalPMUAccess()` accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
**PMCID1SR, CONTEXTIDR_EL1 Sample Register**

The PMCID1SR characteristics are:

**Purpose**

Contains the sampled value of `CONTEXTIDR_EL1`, captured on reading `PMPCSR[31:0]`.

**Configuration**

PMCID1SR is in the Core power domain.

This register is present only when FEAT_PCSRv8p2 is implemented. Otherwise, direct accesses to PMCID1SR are RES0.

---

**Note**

Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of `EDDEVID.PCSample`.

---

**Attributes**

PMCID1SR is a 32-bit register.

**Field descriptions**

The PMCID1SR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

`CONTEXTIDR_EL1`, bits [31:0]

Context ID. The value of CONTEXTIDR that is associated with the most recent `PMPCSR` sample. When the most recent `PMPCSR` sample was generated:

- If EL1 is using AArch64, then the Context ID is sampled from `CONTEXTIDR_EL1`.
- If EL1 is using AArch32, then the Context ID is sampled from `CONTEXTIDR`.
- If EL3 is implemented and is using AArch32, then `CONTEXTIDR` is a banked register and PMCID1SR samples the current banked copy of `CONTEXTIDR` for the Security state that is associated with the most recent `PMPCSR` sample.

Because the value written to PMCID1SR is an indirect read of CONTEXTIDR, it is constrained unpredictable whether PMCID1SR is set to the original or new value if `PMPCSR` samples:

- An instruction that writes to CONTEXTIDR.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMCID1SR**

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.
PMCID1SR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x208</td>
<td>PMCID1SR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x228</td>
<td>PMCID1SR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
The PMCID2SR characteristics are:

**Purpose**

Contains the sampled value of CONTEXTIDR_EL2, captured on reading PMPCSR[31:0].

**Configuration**

PMCID2SR is in the Core power domain.

This register is present only when FEAT_PCSRv8p2 is implemented and EL2 is implemented. Otherwise, direct accesses to PMCID2SR are RES0.

---

**Note**

If FEAT_PCSRv8p2 is not implemented, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

---

**Attributes**

PMCID2SR is a 32-bit register.

**Field descriptions**

The PMCID2SR bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

CONTEXTIDR_EL2, bits [31:0]

Context ID. The value of CONTEXTIDR_EL2 that is associated with the most recent PMPCSR sample. When the most recent PMPCSR sample was generated:

- If EL2 is using AArch64, then this field is set to the Context ID sampled from CONTEXTIDR_EL2.
- If EL2 is using AArch32, then this field is set to an UNKNOWN value.

Because the value written to PMCID2SR is an indirect read of CONTEXTIDR_EL2, it is CONSTRAINED UNPREDICTABLE whether PMCID2SR is set to the original or new value if PMPCSR samples:

- An instruction that writes to CONTEXTIDR_EL2.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMCID2SR**

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.
PMCID2SR can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x22C</td>
<td>PMCID2SR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMCIDR0, Performance Monitors Component Identification Register 0

The PMCIDR0 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMCIDR0 is a 32-bit register.

**Field descriptions**

The PMCIDR0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>PRMBL_0</td>
</tr>
<tr>
<td>30</td>
<td>Reserved, RES0</td>
</tr>
<tr>
<td>28</td>
<td>PRMBL_0, bits [7:0]</td>
</tr>
<tr>
<td>27</td>
<td>Preamble</td>
</tr>
<tr>
<td>26</td>
<td>Reads as 0x0D</td>
</tr>
</tbody>
</table>

**Accessing the PMCIDR0**

**PMCIDR0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFF0</td>
<td>PMCIDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
The PMCIDR1 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMCIDR1 is a 32-bit register.

**Field descriptions**

The PMCIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>CLASS</td>
<td>PRMBL_1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**CLASS, bits [7:4]**

Component class.

<table>
<thead>
<tr>
<th>CLASS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b1001</td>
<td>CoreSight component.</td>
</tr>
</tbody>
</table>

Other values are defined by the CoreSight Architecture.

This field reads as 0x9.

**PRMBL_1, bits [3:0]**

Preamble. RAZ.

Reads as 0b0000.
Accessing the PMCIDR1

PMCIDR1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFF4</td>
<td>PMCIDR1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
The PMCIDR2 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMCIDR2 is a 32-bit register.

**Field descriptions**

The PMCIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>PRMBL_2</td>
</tr>
<tr>
<td>29</td>
<td>Reserved</td>
</tr>
<tr>
<td>28</td>
<td>Reserved</td>
</tr>
<tr>
<td>27</td>
<td>Reserved</td>
</tr>
<tr>
<td>26</td>
<td>Reserved</td>
</tr>
<tr>
<td>25</td>
<td>Reserved</td>
</tr>
<tr>
<td>24</td>
<td>Reserved</td>
</tr>
<tr>
<td>23</td>
<td>Reserved</td>
</tr>
<tr>
<td>22</td>
<td>Reserved</td>
</tr>
<tr>
<td>21</td>
<td>Reserved</td>
</tr>
<tr>
<td>20</td>
<td>Reserved</td>
</tr>
<tr>
<td>19</td>
<td>Reserved</td>
</tr>
<tr>
<td>18</td>
<td>Reserved</td>
</tr>
<tr>
<td>17</td>
<td>Reserved</td>
</tr>
<tr>
<td>16</td>
<td>Reserved</td>
</tr>
<tr>
<td>15</td>
<td>Reserved</td>
</tr>
<tr>
<td>14</td>
<td>Reserved</td>
</tr>
<tr>
<td>13</td>
<td>Reserved</td>
</tr>
<tr>
<td>12</td>
<td>Reserved</td>
</tr>
<tr>
<td>11</td>
<td>Reserved</td>
</tr>
<tr>
<td>10</td>
<td>Reserved</td>
</tr>
<tr>
<td>9</td>
<td>Reserved</td>
</tr>
<tr>
<td>8</td>
<td>Reserved</td>
</tr>
<tr>
<td>7</td>
<td>Reserved</td>
</tr>
<tr>
<td>6</td>
<td>Reserved</td>
</tr>
<tr>
<td>5</td>
<td>Reserved</td>
</tr>
<tr>
<td>4</td>
<td>Reserved</td>
</tr>
<tr>
<td>3</td>
<td>Reserved</td>
</tr>
<tr>
<td>2</td>
<td>Reserved</td>
</tr>
<tr>
<td>1</td>
<td>Reserved</td>
</tr>
<tr>
<td>0</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**PRMBL_2, bits [7:0]**

Preamble.

Reads as 0x05.

**Accessing the PMCIDR2**

PMCIDR2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFF8</td>
<td>PMCIDR2</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMCIDR3, Performance Monitors Component Identification Register 3

The PMCIDR3 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Component Identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMCIDR3 is a 32-bit register.

**Field descriptions**

The PMCIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Field Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td></td>
</tr>
<tr>
<td>29</td>
<td>PRMBL_3</td>
<td></td>
</tr>
</tbody>
</table>

Reserved, RES0.

PRMBL_3, bits [7:0]

Preamble.

Reads as 0xB1.

**Accessing the PMCIDR3**

PMCIDR3 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFFC</td>
<td>PMCIDR3</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMCNTENCLR_EL0, Performance Monitors Count Enable Clear register

The PMCNTENCLR_EL0 characteristics are:

Purpose

Disables the Cycle Count Register, PMCCNTR_EL0, and any implemented event counters PMEVCNTR<n>. Reading this register shows which counters are enabled.

Configuration

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMCNTENCLR_EL0[31:0].

External register PMCNTENCLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCNTENCLR[31:0].

PMCNTENCLR_EL0 is in the Core power domain.

Attributes

PMCNTENCLR_EL0 is a 32-bit register.

Field descriptions

The PMCNTENCLR_EL0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

C, bit [31]

PMCCNTR_EL0 disable bit. Disables the cycle counter register. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, disables the cycle counter.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

P<n>, bit [n], for n = 30 to 0

Event counter disable bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are RAZ/WI.

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;n&gt;_EL0 is enabled. When written, disables PMEVCNTR&lt;n&gt;_EL0.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMCNTENCLR_EL0

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMCNTENCLR_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xC20</td>
<td>PMCNTENCLR_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
PMCNTENSET_EL0, Performance Monitors Count Enable Set register

The PMCNTENSET_EL0 characteristics are:

**Purpose**

Enables the Cycle Count Register, PMCCNTR_EL0, and any implemented event counters PMEVCNTR<n>. Reading this register shows which counters are enabled.

**Configuration**

External register PMCNTENSET_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMCNTENSET_EL0[31:0].

External register PMCNTENSET_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMCNTENSET[31:0].

PMCNTENSET_EL0 is in the Core power domain.

**Attributes**

PMCNTENSET_EL0 is a 32-bit register.

**Field descriptions**

The PMCNTENSET_EL0 bit assignments are:

```
<table>
<thead>
<tr>
<th>C</th>
<th>PMCCNTR_EL0 enable bit. Enables the cycle counter register. Possible values are:</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter is enabled. When written, enables the cycle counter.</td>
</tr>
</tbody>
</table>
```

On a Warm reset, this field resets to an architecturally UNKNOWN value.

```
P<n>, bit [n], for n = 30 to 0
```

Event counter enable bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are RAZ/WI.

```
P<n>                      Meaning
0b0                       When read, means that PMEVCNTR<n>_EL0 is disabled. When written, has no effect.
0b1                       When read, means that PMEVCNTR<n>_EL0 event counter is enabled. When written, enables PMEVCNTR<n>_EL0.
```

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMCNTENSEL_EL0

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMCNTENSEL_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xC00</td>
<td>PMCNTENSEL_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMCR_EL0, Performance Monitors Control Register

The PMCR_EL0 characteristics are:

**Purpose**

Provides details of the Performance Monitors implementation, including the number of counters implemented, and configures and controls the counters.

**Configuration**

External register PMCR_EL0 bits [7:0] are architecturally mapped to AArch32 System register PMCR[7:0].

External register PMCR_EL0 bits [7:0] are architecturally mapped to AArch64 System register PMCR_EL0[7:0].

PMCR_EL0 is in the Core power domain.

This register is only partially mapped to the internal PMCR System register. An external agent must use other means to discover the information held in PMCR[31:11], such as accessing PMCFGR and the ID registers.

**Attributes**

PMCR_EL0 is a 32-bit register.

**Field descriptions**

The PMCR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RAZ/WI</td>
</tr>
<tr>
<td>30</td>
<td>RES0</td>
</tr>
<tr>
<td>29</td>
<td>FZO</td>
</tr>
<tr>
<td>28</td>
<td>RES0</td>
</tr>
<tr>
<td>27</td>
<td>LP</td>
</tr>
<tr>
<td>26</td>
<td>LC</td>
</tr>
<tr>
<td>25</td>
<td>DP</td>
</tr>
<tr>
<td>24</td>
<td>X</td>
</tr>
<tr>
<td>23</td>
<td>D</td>
</tr>
<tr>
<td>22</td>
<td>C</td>
</tr>
<tr>
<td>21</td>
<td>P</td>
</tr>
<tr>
<td>20</td>
<td>E</td>
</tr>
</tbody>
</table>

Bits [31:11]

Reserved, RAZ/WI.

Hardware must implement this field as RAZ/WI. Software must not rely on the register reading as zero, and must use a read-modify-write sequence to write to the register.

Bit [10]

Reserved, RES0.

**FZO, bit [9]**

When FEAT_PMUv3p7 is implemented:

Freeze-on-overflow. Stop event counters on overflow.

<table>
<thead>
<tr>
<th>FZO</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not freeze on overflow.</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counters do not count when PMOVSVCLR_EL0[(N-1):0] is nonzero, where N is the value of MDCR_EL2.HPMN if EL2 is implemented, and PMCR_EL0.N otherwise.</td>
</tr>
</tbody>
</table>

If EL2 is implemented, then:

- This bit affects the operation of event counters in the range [0 .. (MDCR_EL2.HPMN-1)].
- If MDCR_EL2.HPMN is less than PMCR_EL0.N:
This bit does not affect the operation of event counters in the range [MDCR_EL2.HPMN .. (PMCR_EL0.N-1)].

The operation of this bit ignores the values of PMOVCLR_EL0[(PMCR_EL0.N-1):MDCR_EL2.HPMN].

- This applies even when EL2 is disabled in the current Security state.

This bit does not affect the operation of PMCCNTR_EL0.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**Bit [8]**

Reserved, RES0.

**LP, bit [7]**

*When FEAT_PMUv3p5 is implemented:*

Long event counter enable. Determines when unsigned overflow is recorded by a counter overflow bit.

<table>
<thead>
<tr>
<th>LP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;n&gt;_EL0[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Event counter overflow on increment that causes unsigned overflow of PMEVCNTR&lt;n&gt;_EL0[63:0].</td>
</tr>
</tbody>
</table>

If EL2 is implemented and MDCR_EL2.HPMN is less than PMCR_EL0.N, this bit does not affect the operation of event counters in the range [MDCR_EL2.HPMN:(PMCR_EL0.N-1)].

If EL2 is implemented and HDCR.HPMN is less than PMCR_EL0.N, this bit does not affect the operation of event counters in the range [HDCR.HPMN:(PMCR_EL0.N-1)].

**Note**

The effect of MDCR_EL2.HPMN or HDCR.HPMN on the operation of this bit always applies if EL2 is implemented, at all Exception levels including EL2 and EL3, and regardless of whether EL2 is enabled in the current Security state. For more information, see the description of MDCR_EL2.HPMN or HDCR.HPMN.

If the highest implemented Exception level is using AArch32, it is IMPLEMENTATION DEFINED whether this bit is RW or RAZ/WI.

**Otherwise:**

Reserved, RES0.

**LC, bit [6]**

*When AArch32 is supported at any Exception level:*

Long cycle counter enable. Determines when unsigned overflow is recorded by the cycle counter overflow bit.

<table>
<thead>
<tr>
<th>LC</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR_EL0[31:0].</td>
</tr>
<tr>
<td>0b1</td>
<td>Cycle counter overflow on increment that causes unsigned overflow of PMCCNTR_EL0[63:0].</td>
</tr>
</tbody>
</table>
Arm deprecates use of `PMCR_EL0.LC = 0`.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**Otherwise:**

Reserved, **RES1**.

**DP, bit [5]**

When EL3 is implemented or (FEAT_PMUv3p1 is implemented and EL2 is implemented):

Disable cycle counter when event counting is prohibited. The possible values of this bit are:

<table>
<thead>
<tr>
<th>DP</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Cycle counting by <code>PMCCNTR_EL0</code> is not affected by this bit.</td>
</tr>
<tr>
<td>0b1</td>
<td>When event counting for counters in the range [0..(MDCR_EL2.HPMN-1)] is prohibited, cycle counting by <code>PMCCNTR_EL0</code> is disabled.</td>
</tr>
</tbody>
</table>

For more information, see 'Prohibiting event counting'.

When this register has an architecturally-defined reset value, if this field is implemented as an RW field it resets to:

- A value that is architecturally **UNKNOWN** if the reset is into an Exception level that is using AArch64.
- 0 if the reset is into an Exception level that is using AArch32.

**Otherwise:**

Reserved, **RES0**.

**X, bit [4]**

When the implementation includes a PMU event export bus:

Enable export of events in an **IMPLEMENTATION DEFINED** PMU event export bus.

<table>
<thead>
<tr>
<th>X</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not export events.</td>
</tr>
<tr>
<td>0b1</td>
<td>Export events where not prohibited.</td>
</tr>
</tbody>
</table>

This field enables the exporting of events over an **IMPLEMENTATION DEFINED** PMU event export bus to another device, for example to an **OPTIONAL** PE trace unit.

No events are exported when counting is prohibited.

This field does not affect the generation of Performance Monitors overflow interrupt requests or signaling to a cross-trigger interface (CTI) that can be implemented as signals exported from the PE.

When this register has an architecturally-defined reset value, if this field is implemented as an RW field it resets to:

- A value that is architecturally **UNKNOWN** if the reset is into an Exception level that is using AArch64.
- 0 if the reset is into an Exception level that is using AArch32.

**Otherwise:**

Reserved, RAZ/WI.

**D, bit [3]**

When AArch32 is supported at any Exception level:

Clock divider.
### D

<table>
<thead>
<tr>
<th>Meaning</th>
<th>0b0</th>
<th>When enabled, <code>PMCCNTR_EL0</code> counts every clock cycle.</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0b1</td>
<td>When enabled, <code>PMCCNTR_EL0</code> counts once every 64 clock cycles.</td>
</tr>
</tbody>
</table>

If `PMCR_EL0.LC` == 1, this bit is ignored and the cycle counter counts every clock cycle.

Arm deprecates use of `PMCR_EL0.D = 1`.

When this register has an architecturally-defined reset value, if this field is implemented as an RW field it resets to:

- A value that is architecturally `UNKNOWN` if the reset is into an Exception level that is using AArch64.
- 0 if the reset is into an Exception level that is using AArch32.

**Otherwise:**

Reserved, `RES0`.

### C, bit [2]

Cycle counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset <code>PMCCNTR_EL0</code> to zero.</td>
</tr>
</tbody>
</table>

**Note**

Resetting `PMCCNTR_EL0` does not change the cycle counter overflow bit.

Access to this field is `WO/RAZ`.

### P, bit [1]

Event counter reset. The effects of writing to this bit are:

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action.</td>
</tr>
<tr>
<td>0b1</td>
<td>Reset all event counters, not including <code>PMCCNTR_EL0</code>, to zero.</td>
</tr>
</tbody>
</table>

**Note**

Resetting the event counters does not change the event counter overflow bits.

If `FEAT_PMUv3p5` is implemented, the value of `MDCR_EL2.HLP`, or `PMCR_EL0.LP` is ignored and bits [63:0] of all event counters are reset.

Access to this field is `WO/RAZ`.

### E, bit [0]

Enable.

<table>
<thead>
<tr>
<th>E</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>All event counters in the range [0..(PMN-1)] and <code>PMCCNTR_EL0</code> are disabled.</td>
</tr>
<tr>
<td>0b1</td>
<td>All event counters in the range [0..(PMN-1)] and <code>PMCCNTR_EL0</code> are enabled by <code>PMCNTENSET_EL0</code>.</td>
</tr>
</tbody>
</table>

If EL2 is implemented then:

- If EL2 is using AArch32, PMN is `HDCR.HPMN`.
- If EL2 is using AArch64, PMN is `MDCR_EL2.HPMN`.
- If PMN is less than `PMCR_EL0.N`, this bit does not affect the operation of event counters in the range `[PMN..(PMCR_EL0.N-1)]`. 

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If EL2 is not implemented, PMN is PMCR_EL0.N.

---

**Note**

The effect of the following fields on the operation of this bit applies if EL2 is implemented regardless of whether EL2 is enabled in the current Security state:

- **HDCR.**HPMN. See the description of **HDCR.**HPMN for more information.
- **MDCR_EL2.**HPMN. See the description of **MDCR_EL2.**HPMN for more information.

---

On a Warm reset, this field resets to 0.

## Accessing the PMCR_EL0

---

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

---

**PMCR_EL0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE04</td>
<td>PMCR_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMDEVAFF0, Performance Monitors Device Affinity register 0

The PMDEVAFF0 characteristics are:

**Purpose**

Copy of the low half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the Performance Monitor component relates to.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required if the external interface to the PMU is implemented.

**Attributes**

PMDEVAFF0 is a 32-bit register.

**Field descriptions**

The PMDEVAFF0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**MPIDR_EL1lo, bits [31:0]**

MPIDR_EL1 low half. Read-only copy of the low half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the PMDEVAFF0**

PMDEVAFF0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFA8</td>
<td>PMDEVAFF0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMDEVAFF1, Performance Monitors Device Affinity register 1

The PMDEVAFF1 characteristics are:

**Purpose**

Copy of the high half of the PE MPIDR_EL1 register that allows a debugger to determine which PE in a multiprocessor system the Performance Monitor component relates to.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required if the external interface to the PMU is implemented.

**Attributes**

PMDEVAFF1 is a 32-bit register.

**Field descriptions**

The PMDEVAFF1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
|    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    | MPIDR_EL1hi |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |    |

**MPIDR_EL1hi, bits [31:0]**

MPIDR_EL1 high half. Read-only copy of the high half of MPIDR_EL1, as seen from the highest implemented Exception level.

**Accessing the PMDEVAFF1**

PMDEVAFF1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFAC</td>
<td>PMDEVAFF1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMDEVARCH, Performance Monitors Device Architecture register

The PMDEVARCH characteristics are:

**Purpose**

Identifies the programmers' model architecture of the Performance Monitor component.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

PMDEVARCH is a 32-bit register.

**Field descriptions**

The PMDEVARCH bit assignments are:

```
| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ARCHITECT | PRESENT | REVISION | ARCHID |
```

**ARCHITECT, bits [31:21]**

Defines the architecture of the component. For Performance Monitors, this is Arm Limited.

Bits [31:28] are the JEP106 continuation code, 0x4.

Bits [27:21] are the JEP106 ID code, 0x3B.

**PRESENT, bit [20]**

When set to 1, indicates that the DEVARCH is present.

This field is 1 in Armv8.

**REVISION, bits [19:16]**

Defines the architecture revision. For architectures defined by Arm this is the minor revision.

For Performance Monitors, the revision defined by Armv8 is 0x0.

All other values are reserved.

**ARCHID, bits [15:0]**

Defines this part to be an Armv8 debug component. For architectures defined by Arm this is further subdivided.

For Performance Monitors:

- Bits [15:12] are the architecture version, 0x2.
- Bits [11:0] are the architecture part number, 0xA16.

This corresponds to Performance Monitors architecture version PMUv3.
Note

The PMUv3 memory-mapped programmers' model can be used by devices other than Armv8 processors. Software must determine whether the PMU is attached to an Armv8 processor by using the PMDEVAFF0 and PMDEVAFF1 registers to discover the affinity of the PMU to any Armv8 processors.

Accessing the PMDEVARCH

PMDEVARCH can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFB0</td>
<td>PMDEVARCH</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMDEVID, Performance Monitors Device ID register

The PMDEVID characteristics are:

**Purpose**

Provides information about features of the Performance Monitors implementation.

**Configuration**

If FEAT_DoPD is implemented, this register is in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required from Armv8.2 and in any implementation that includes FEAT_PCSRv8p2. Otherwise, its location is RES0.

**Note**

Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

**Attributes**

PMDEVID is a 32-bit register.

**Field descriptions**

The PMDEVID bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:4]**

Reserved, RES0.

**PCSample, bits [3:0]**

Indicates the level of PC Sample-based Profiling support using Performance Monitors registers.

<table>
<thead>
<tr>
<th>PCSample</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0000</td>
<td>PC Sample-based Profiling Extension is not implemented in the Performance Monitors register space.</td>
</tr>
<tr>
<td>0b0001</td>
<td>PC Sample-based Profiling Extension is implemented in the Performance Monitors register space.</td>
</tr>
</tbody>
</table>

All other values are reserved.

FEAT_PCSRv8p2 implements the functionality identified by the value 0b0001.
Accessing the PMDEVID

PMDEVID can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFC8</td>
<td>PMDEVID</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMDEVTYPE, Performance Monitors Device Type register

The PMDEVTYPE characteristics are:

**Purpose**

Indicates to a debugger that this component is part of a PE's performance monitor interface.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

**Attributes**

PMDEVTYPE is a 32-bit register.

**Field descriptions**

The PMDEVTYPE bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31:8</td>
<td>RES0</td>
<td>Reserved</td>
</tr>
<tr>
<td>7:4</td>
<td>SUB</td>
<td>Subtype. Must read as 0x1 to indicate this is a component within a PE.</td>
</tr>
<tr>
<td>3:0</td>
<td>MAJOR</td>
<td>Major type. Must read as 0x6 to indicate this is a performance monitor component.</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SUB, bits [7:4]**

Subtype. Must read as 0x1 to indicate this is a component within a PE.

**MAJOR, bits [3:0]**

Major type. Must read as 0x6 to indicate this is a performance monitor component.

**Accessing the PMDEVTYPE**

PMDEVTYPE can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFCC</td>
<td>PMDEVTYPE</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMEVCNTR\text{n}_EL0, Performance Monitors Event Count Registers, n = 0 - 30

The PMEVCNTR\text{n}_EL0 characteristics are:

**Purpose**

Holds event counter \( n \), which counts events, where \( n \) is 0 to 30.

**Configuration**

External register PMEVCNTR\text{n}_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMEVCNTR\text{n}_EL0[31:0].

External register PMEVCNTR\text{n}_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMEVCNTR\text{n}[31:0].

PMEVCNTR\text{n}_EL0 is in the Core power domain.

**Attributes**

PMEVCNTR\text{n}_EL0 is a:

- 64-bit register when FEAT_PMUv3p5 is implemented
- 32-bit register otherwise

**Field descriptions**

The PMEVCNTR\text{n}_EL0 bit assignments are:

**When FEAT_PMUv3p5 is implemented:**

<table>
<thead>
<tr>
<th>63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32</th>
</tr>
</thead>
<tbody>
<tr>
<td>Event counter ( n )</td>
</tr>
<tr>
<td>Event counter ( n )</td>
</tr>
<tr>
<td>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td>
</tr>
</tbody>
</table>

**Bits [63:0]**

Event counter \( n \). Value of event counter \( n \), where \( n \) is the number of this register and is a number from 0 to 30.

If the highest implemented Exception level is using AArch32, the optional external interface to the performance monitors is implemented, and the PMCR LP and HDCR HLP bits are RAZ/WI, then locations in the external interface to the performance monitors that map to PMEVCNTR\text{n}_EL0[63:32] return UNKNOWN values on reads.

If the implementation does not support AArch64 at any Exception level, bits [63:32] of the event counters are not required to be implemented.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

<table>
<thead>
<tr>
<th>31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Event counter ( n )</td>
</tr>
</tbody>
</table>
Bits [31:0]

Event counter n. Value of event counter n, where n is the number of this register and is a number from 0 to 30.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

Accessing the PMEVCNTR<n>_EL0

External accesses to the performance monitors ignore PMUSERENR_EL0 and, if implemented, MDCR_EL2 {TPM, TPMCR, HPMN} and MDCR_EL3.TPM. This means that all counters are accessible regardless of the current Exception level or privilege of the access.

If FEAT_PMUv3p5 is not implemented, when IsCorePowered(), DoubleLockStatus(), OSLockStatus() or !AllowExternalPMUAccess(), 32-bit accesses to 0x004+8×n have a CONSTRAINED UNPREDICTABLE behavior.

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMEVCNTR<n>_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x000 + (8 * n)</td>
<td>PMEVCNTR&lt;n&gt;_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMEVTYPER\textsubscript{n} \_EL0, Performance Monitors Event Type Registers, n = 0 - 30

The PMEVTYPER\textsubscript{n} \_EL0 characteristics are:

**Purpose**

Configures event counter \( n \), where \( n \) is 0 to 30.

**Configuration**

External register PMEVTYPER\textsubscript{n} \_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMEVTYPER\textsubscript{n} \_EL0[31:0].

External register PMEVTYPER\textsubscript{n} \_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMEVTYPER\textsubscript{n}[31:0].

PMEVTYPER\textsubscript{n} \_EL0 is in the Core power domain.

If event counter \( n \) is not implemented:

- When IsCorePowered() && !DoubleLockStatus() && !OSLockStatus() && AllowExternalPMUAccess(), accesses are RES0.
- Otherwise, it is CONSTRAINED UNPREDICTABLE whether accesses to this register are RES0 or generate an error response.

**Attributes**

PMEVTYPER\textsubscript{n} \_EL0 is a 32-bit register.

**Field descriptions**

The PMEVTYPER\textsubscript{n} \_EL0 bit assignments are:

\[
\begin{array}{ccccccccccccccccccccccc}
\hline
\end{array}
\]

**P, bit [31]**

Privileged filtering bit. Controls counting in EL1.

If EL3 is implemented, then counting in Non-secure EL1 is further controlled by the PMEVTYPER\textsubscript{n} \_EL0.NSK bit.

<table>
<thead>
<tr>
<th>P</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events in EL1.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count events in EL1.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**U, bit [30]**

User filtering bit. Controls counting in EL0.

If EL3 is implemented, then counting in Non-secure EL0 is further controlled by the PMEVTYPER\textsubscript{n} \_EL0.NSU bit.

<table>
<thead>
<tr>
<th>U</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events in EL0.</td>
</tr>
<tr>
<td>0b1</td>
<td>Do not count events in EL0.</td>
</tr>
</tbody>
</table>
On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

**NSK, bit [29]**

*When EL3 is implemented:*

Non-secure EL1 (kernel) modes filtering bit. Controls counting in Non-secure EL1.

If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.P bit, events in Non-secure EL1 are counted. Otherwise, events in Non-secure EL1 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**NSU, bit [28]**

*When EL3 is implemented:*

Non-secure EL0 (Unprivileged) filtering bit. Controls counting in Non-secure EL0.

If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.U bit, events in Non-secure EL0 are counted. Otherwise, events in Non-secure EL0 are not counted.

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**NSH, bit [27]**

*When EL2 is implemented:*

EL2 (Hypervisor) filtering bit. Controls counting in EL2.

If FEAT_SEL2 and EL3 are implemented, counting in Secure EL2 is further controlled by the PMEVTYPER<n>_EL0.SH bit.

<table>
<thead>
<tr>
<th>NSH</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Do not count events in EL2.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count events in EL2.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally **UNKNOWN** value.

Otherwise:

Reserved, RES0.

**M, bit [26]**

*When EL3 is implemented:*

Secure EL3 filtering bit.

If the value of this bit is equal to the value of the PMEVTYPER<n>_EL0.P bit, events in Secure EL3 are counted. Otherwise, events in Secure EL3 are not counted.
Most applications can ignore this field and set its value to 0b0.

**Note**

This field is not visible in the AArch32 PMEVTYPEPER<n> System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**MT, bit [25]**

When (FEAT_MTPMU is implemented and enabled) or an IMPLEMENTATION DEFINED multi-threaded PMU Extension is implemented:

Multithreading.

<table>
<thead>
<tr>
<th>MT</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Count events only on controlling PE.</td>
</tr>
<tr>
<td>0b1</td>
<td>Count events from any PE with the same affinity at level 1 and above as this PE.</td>
</tr>
</tbody>
</table>

**Note**

- When the lowest level of affinity consists of logical PEs that are implemented using a multi-threading type approach, an implementation is described as multi-threaded. That is, the performance of PEs at the lowest affinity level is highly interdependent.
- Events from a different thread of a multithreaded implementation are not Attributable to the thread counting the event.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**SH, bit [24]**

When FEAT_SEL2 is implemented and EL3 is implemented:

Secure EL2 filtering.

If the value of this bit is not equal to the value of the PMEVTYPEPER<n>_EL0.NSH bit, events in Secure EL2 are counted.

Otherwise, events in Secure EL2 are not counted.

**Note**

This field is not visible in the AArch32 PMEVTYPEPER<n> System register.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.
**Bits [23:16]**

Reserved, RES0.

**evtCount[15:10], bits [15:10]**

*When FEAT_PMUV3p1 is implemented:*

Extension to evtCount[9:0]. See evtCount[9:0] for more details.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

*Otherwise:*

Reserved, RES0.

**evtCount[9:0], bits [9:0]**

Event to count. The event number of the event that is counted by event counter PMEVCNTR<n>_EL0.

Software must program this field with an event that is supported by the PE being programmed.

The ranges of event numbers allocated to each type of event are shown in ‘Allocation of the PMU event number space’.

If evtCount is programmed to an event that is reserved or not supported by the PE, the behavior depends on the value written:

- For the range 0x0000 to 0x003F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- If 16-bit evtCount is implemented, for the range 0x4000 to 0x403F, no events are counted, and the value returned by a direct or external read of the evtCount field is the value written to the field.
- For IMPLEMENTATION DEFINED events, it is UNPREDICTABLE what event, if any, is counted, and the value returned by a direct or external read of the evtCount field is UNKNOWN.

**Note**

UNPREDICTABLE means the event must not expose privileged information.

Arm recommends that the behavior across a family of implementations is defined such that if a given implementation does not include an event from a set of common IMPLEMENTATION DEFINED events, then no event is counted and the value read back on evtCount is the value written.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**Accessing the PMEVTYPER<n>_EL0**

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

**PMEVTYPER<n>_EL0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x400 + (4 * n)</td>
<td>PMEVTYPER&lt;n&gt;_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
• When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and
  !SoftwareLockStatus() accesses to this register are RW.
• Otherwise accesses to this register generate an error response.
PMINTENCLR_EL1, Performance Monitors Interrupt Enable Clear register

The PMINTENCLR_EL1 characteristics are:

**Purpose**

Disables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR_EL0, and the event counters PMEVCNTR<n>_EL0. Reading the register shows which overflow interrupt requests are enabled.

**Configuration**

External register PMINTENCLR_EL1 bits [31:0] are architecturally mapped to AArch64 System register PMINTENCLR_EL1[31:0].

External register PMINTENCLR_EL1 bits [31:0] are architecturally mapped to AArch32 System register PMINTENCLR[31:0].

PMINTENCLR_EL1 is in the Core power domain.

**Attributes**

PMINTENCLR_EL1 is a 32-bit register.

**Field descriptions**

The PMINTENCLR_EL1 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9  | 8  | 7  | 6  | 5  | 4  | 3  | 2  | 1  | 0  |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|

**C, bit [31]**

PMCCNTR_EL0 overflow interrupt request disable bit. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter overflow interrupt request is enabled. When written, disables the cycle count overflow interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow interrupt request disable bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are RAZ/WI.

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is enabled. When written, disables the PMEVCNTR&lt;n&gt;_EL0 interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMINTENCLR_EL1

Note
SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMINTENCLR_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xC60</td>
<td>PMINTENCLR_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMINTENSET_EL1, Performance Monitors Interrupt Enable Set register

The PMINTENSET_EL1 characteristics are:

**Purpose**

Enables the generation of interrupt requests on overflows from the Cycle Count Register, PMCCNTR_EL0, and the event counters PMEVCNTR<n>_EL0. Reading the register shows which overflow interrupt requests are enabled.

**Configuration**

External register PMINTENSET_EL1 bits [31:0] are architecturally mapped to AArch64 System register PMINTENSET_EL1[31:0].

External register PMINTENSET_EL1 bits [31:0] are architecturally mapped to AArch32 System register PMINTENSET[31:0].

PMINTENSET_EL1 is in the Core power domain.

**Attributes**

PMINTENSET_EL1 is a 32-bit register.

**Field descriptions**

The PMINTENSET_EL1 bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Bit Assignment</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>[31]</td>
<td>PMCCNTR_EL0 overflow interrupt request enable bit. Possible values are:</td>
</tr>
<tr>
<td>P&lt;n&gt;</td>
<td>[n] (n = 30 to 0)</td>
<td>PMEVCNTR&lt;n&gt;_EL0 event counter overflow interrupt request enable bit. Possible values are:</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PMCCNTR_EL0** overflow interrupt request enable bit. Possible values are:

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter overflow interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter overflow interrupt request is enabled. When written, enables the cycle count overflow interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**PMEVCNTR<n>_EL0** event counter overflow interrupt request enable bit. Possible values are:

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is disabled. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that the PMEVCNTR&lt;n&gt;_EL0 event counter interrupt request is enabled. When written, enables the PMEVCNTR&lt;n&gt;_EL0 interrupt request.</td>
</tr>
</tbody>
</table>

On a Warm reset, this field resets to an architecturally UNKNOWN value.
Accessing the PMINTENSET_EL1

Note

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMINTENSET_EL1 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xC40</td>
<td>PMINTENSET_EL1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMITCTRL, Performance Monitors Integration mode Control register

The PMITCTRL characteristics are:

**Purpose**

Enables the Performance Monitors to switch from default mode into integration mode, where test software can control directly the inputs and outputs of the PE, for integration testing or topology detection.

**Configuration**

It is IMPLEMENTATION DEFINED whether PMITCTRL is implemented in the Core power domain or in the Debug power domain.

Implementation of this register is OPTIONAL.

**Attributes**

PMITCTRL is a 32-bit register.

**Field descriptions**

The PMITCTRL bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>IME</td>
</tr>
<tr>
<td>29</td>
<td></td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
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<tr>
<td>26</td>
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<tr>
<td>3</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:1]**

Reserved, RES0.

**IME, bit [0]**

Integration mode enable. When IME == 1, the device reverts to an integration mode to enable integration testing or topology detection. The integration mode behavior is IMPLEMENTATION DEFINED.

<table>
<thead>
<tr>
<th>IME</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Normal operation.</td>
</tr>
<tr>
<td>0b1</td>
<td>Integration mode enabled.</td>
</tr>
</tbody>
</table>

The following resets apply:

- If the register is implemented in the Core power domain:
  - On a Cold reset, this field resets to 0.
  - On an External debug reset, the value of this field is unchanged.
  - On a Warm reset, the value of this field is unchanged.

- If the register is implemented in the External debug power domain:
  - On a Cold reset, the value of this field is unchanged.
  - On an External debug reset, this field resets to 0.
  - On a Warm reset, the value of this field is unchanged.
Accessing the PMITCTRL

PMITCTRL can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xF00</td>
<td>PMITCTRL</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register are **IMPDEF**.
PMLAR, Performance Monitors Lock Access Register

The PMLAR characteristics are:

**Purpose**

Allows or disallows access to the Performance Monitors registers through a memory-mapped interface.

The optional Software Lock provides a lock to prevent memory-mapped writes to the Performance Monitors registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the Performance Monitors registers. It does not, and cannot, prevent all accidental or malicious damage.

**Configuration**

If FEAT_DoPD is implemented, Software Lock is not implemented by the architecturally-defined debug components of the PE in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

Software uses PMLAR to set or clear the lock, and PMLSR to check the current status of the lock.

**Attributes**

PMLAR is a 32-bit register.

**Field descriptions**

The PMLAR bit assignments are:

**When Software Lock is implemented:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
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</tbody>
</table>

**KEY**

**KEY, bits [31:0]**

Lock Access control. Writing the key value 0xC5ACCE55 to this field unlocks the lock, enabling write accesses to this component's registers through a memory-mapped interface.

Writing any other value to this register locks the lock, disabling write accesses to this component's registers through a memory-mapped interface.

**Otherwise:**

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
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<th>27</th>
<th>26</th>
<th>25</th>
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<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
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</tr>
</tbody>
</table>

**RES0**

Otherwise

**Bits [31:0]**

Reserved, RES0.
Accessing the PMLAR

PMLAR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFB0</td>
<td>PMLAR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **WO**.
- Otherwise accesses to this register generate an error response.
PMLSR, Performance Monitors Lock Status Register

The PMLSR characteristics are:

Purpose

Indicates the current status of the software lock for Performance Monitors registers.

The optional Software Lock provides a lock to prevent memory-mapped writes to the Performance Monitors registers. Use of this lock mechanism reduces the risk of accidental damage to the contents of the Performance Monitors registers. It does not, and cannot, prevent all accidental or malicious damage.

Configuration

If FEAT_DoPD is implemented, Software Lock is not implemented by the architecturally-defined debug components of the PE in the Core power domain.

If FEAT_DoPD is not implemented, this register is in the Debug power domain.

Software uses PMLAR to set or clear the lock, and PMLSR to check the current status of the lock.

Attributes

PMLSR is a 32-bit register.

Field descriptions

The PMLSR bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
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<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RES0</td>
<td></td>
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<td></td>
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<td></td>
<td>nTT</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Bits [31:3]

Reserved, RES0.

nTT, bit [2]

Not thirty-two bit access required. RAZ.

SLK, bit [1]

When Software Lock is implemented and FEAT_DoPD is not implemented:

Software Lock status for this component. For an access to LSR that is not a memory-mapped access, or when Software Lock is not implemented, this field is RES0.

For memory-mapped accesses when Software Lock is implemented, possible values of this field are:

<table>
<thead>
<tr>
<th>SLK</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Lock clear. Writes are permitted to this component's registers.</td>
</tr>
<tr>
<td>0b1</td>
<td>Lock set. Writes to this component's registers are ignored, and reads have no side effects.</td>
</tr>
</tbody>
</table>

On an External debug reset, this field resets to 1.
Otherwise:

Reserved, RAZ.

SLI, bit [0]

Software Lock implemented. For an access to LSR that is not a memory-mapped access, this field is RAZ. For memory-mapped accesses, the value of this field is IMPLEMENTATION DEFINED. Permitted values are:

<table>
<thead>
<tr>
<th>SLI</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Software Lock not implemented or not memory-mapped access.</td>
</tr>
<tr>
<td>0b1</td>
<td>Software Lock implemented and memory-mapped access.</td>
</tr>
</tbody>
</table>

Accessing the PMLSR

PMLSR can be accessed through the memory-mapped interfaces:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFB4</td>
<td>PMLSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMMIR, Performance Monitors Machine Identification Register

The PMMIR characteristics are:

**Purpose**

Describes Performance Monitors parameters specific to the implementation.

**Configuration**

PMMIR is in the Core power domain.

This register is present only when FEAT_PMUv3p4 is implemented. Otherwise, direct accesses to PMMIR are RES0.

**Attributes**

PMMIR is a 32-bit register.

**Field descriptions**

The PMMIR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>SLOTS</td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**SLOTS, bits [7:0]**

Operation width. The largest value by which the STALL SLOT event might increment by in a single cycle. If the STALL SLOT event is implemented, this field must not be zero.

**Accessing the PMMIR**

If the Core power domain is off or in a low-power state, access on this interface returns an Error.

**PMMIR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xE40</td>
<td>PMMIR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When !IsCorePowered(), or DoubleLockStatus(), or OSLockStatus() or !AllowExternalPMUAccess() accesses to this register generate an error response.
- Otherwise accesses to this register are RO.
PMOVSCLR_EL0, Performance Monitors Overflow Flag Status Clear register

The PMOVSCLR_EL0 characteristics are:

**Purpose**

Contains the state of the overflow bit for the Cycle Count Register, PMCCNTR_EL0, and each of the implemented event counters PMEVCNTR<n>. Writing to this register clears these bits.

**Configuration**

External register PMOVSCLR_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMOVSCLR_EL0[31:0].

External register PMOVSCLR_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMOVR[31:0].

PMOVSCLR_EL0 is in the Core power domain.

**Attributes**

PMOVSCLR_EL0 is a 32-bit register.

**Field descriptions**

The PMOVSCLR_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
<th>17</th>
<th>16</th>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

**C, bit [31]**

Cycle counter overflow clear bit.

<table>
<thead>
<tr>
<th>C</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means the cycle counter has overflowed since this bit was last cleared. When written, clears the cycle counter overflow bit to 0.</td>
</tr>
</tbody>
</table>

PMCR_EL0.LC controls whether an overflow is detected from unsigned overflow of PMCCNTR_EL0[31:0] or unsigned overflow of PMCCNTR_EL0[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow clear bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are RAZ/WI.
### PMOVSCLR_EL0, Performance Monitors Overflow Flag Status Clear register

<table>
<thead>
<tr>
<th>$P&lt;n&gt;$</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>When read, means that PMEVCNTR&lt;$n&gt;_EL0 has not overflowed since this bit was last cleared. When written, has no effect.</td>
</tr>
<tr>
<td>0b1</td>
<td>When read, means that PMEVCNTR&lt;$n&gt;_EL0 has overflowed since this bit was last cleared. When written, clears the PMEVCNTR&lt;$n&gt;_EL0 overflow bit to 0.</td>
</tr>
</tbody>
</table>

If FEAT_PMUV3p5 is implemented, MDCR_EL2.HLP and PMCR_EL0.LP control whether an overflow is detected from unsigned overflow of PMEVCNTR<$n>_EL0[31:0] or unsigned overflow of PMEVCNTR<$n>_EL0[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

### Accessing the PMOVSCLR_EL0

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

PMOVSCLR_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xC80</td>
<td>PMOVSCLR_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **RO**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **RW**.
- Otherwise accesses to this register generate an error response.
PMOVSSET_EL0, Performance Monitors Overflow Flag Status Set register

The PMOVSSET_EL0 characteristics are:

**Purpose**

Sets the state of the overflow bit for the Cycle Count Register, PMCCNTR_EL0, and each of the implemented event counters PMEVCNTR<n>.

**Configuration**

External register PMOVSSET_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMOVSSET_EL0[31:0].

External register PMOVSSET_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMOVSSET[31:0].

PMOVSSET_EL0 is in the Core power domain.

**Attributes**

PMOVSSET_EL0 is a 32-bit register.

**Field descriptions**

The PMOVSSET_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>Field</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>C</td>
<td>Cycle counter overflow set bit.</td>
</tr>
</tbody>
</table>

- **C, bit [31]**
  - 0b0: When read, means the cycle counter has not overflowed since this bit was last cleared. When written, has no effect.
  - 0b1: When read, means the cycle counter has overflowed since this bit was last cleared. When written, sets the cycle counter overflow bit to 1.

PMCR_EL0.LC controls whether an overflow is detected from unsigned overflow of PMCCNTR_EL0[31:0] or unsigned overflow of PMCCNTR_EL0[63:0].

On a Warm reset, this field resets to an architecturally UNKNOWN value.

**P<n>, bit [n], for n = 30 to 0**

Event counter overflow set bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are RAZ/WI.
When read, means that $\text{PMEVCNTR}_{n, \text{EL0}}$ has not overflowed since this bit was last cleared. When written, has no effect.

When read, means that $\text{PMEVCNTR}_{n, \text{EL0}}$ has overflowed since this bit was last cleared. When written, sets the $\text{PMEVCNTR}_{n, \text{EL0}}$ overflow bit to 1.

If FEAT_PMUv3p5 is implemented, $\text{MDCR}_{\text{EL2}}$.HLP and $\text{PMCR}_{\text{EL0}}$.LP control whether an overflow is detected from unsigned overflow of $\text{PMEVCNTR}_{n, \text{EL0}}[31:0]$ or unsigned overflow of $\text{PMEVCNTR}_{n, \text{EL0}}[63:0]$.

On a Warm reset, this field resets to an architecturally UNKNOWN value.

## Accessing the PMOVSSET_EL0

**Note**

SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

### PMOVSSET_EL0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xCC0</td>
<td>PMOVSSET_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are RO.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are RW.
- Otherwise accesses to this register generate an error response.
PMPCSR, Program Counter Sample Register

The PMPCSR characteristics are:

**Purpose**

Holds a sampled instruction address value.

**Configuration**

PMPCSR is in the Core power domain.

This register is present only when FEAT_PCSRv8p2 is implemented. Otherwise, direct accesses to PMPCSR are RES0.

**Note**

Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

Support for 64-bit atomic reads is IMPLEMENTATION DEFINED. If 64-bit atomic reads are implemented, a 64-bit read of PMPCSR has the same side-effect as a 32-bit read of PMCSR[31:0] followed by a 32-bit read of PMPCSR[63:32], returning the combined value. For example, if the PE is in Debug state then a 64-bit atomic read returns bits[31:0] == 0xFFFFFFFF and bits[63:32] UNKNOWN.

**Attributes**

PMPCSR is a 64-bit register.

**Field descriptions**

The PMPCSR bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>NS</th>
<th>EL</th>
<th>RES0</th>
<th>PCSample[55:32]</th>
<th>PCSample[31:0]</th>
</tr>
</thead>
<tbody>
<tr>
<td>63</td>
<td>62</td>
<td>61</td>
<td>60</td>
<td>59</td>
<td>58</td>
</tr>
<tr>
<td>31</td>
<td>30</td>
<td>29</td>
<td>28</td>
<td>27</td>
<td>26</td>
</tr>
</tbody>
</table>

**NS, bit [63]**

Non-secure state sample. Indicates the Security state that is associated with the most recent PMPCSR sample or, when it is read as a single atomic 64-bit read, the current PMPCSR sample.

If EL3 is not implemented, this bit indicates the Effective value of SCR.NS.

<table>
<thead>
<tr>
<th>NS</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>Sample is from Secure state.</td>
</tr>
<tr>
<td>0b1</td>
<td>Sample is from Non-secure state.</td>
</tr>
</tbody>
</table>

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**EL, bits [62:61]**

Exception level status sample. Indicates the Exception level that is associated with the most recent PMPCSR sample or, when it is read as a single atomic 64-bit read, the current PMPCSR sample.
On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Bits [60:56]**

Reserved, RES0.

**PCSample[55:32], bits [55:32]**

Bits[55:32] of the sampled instruction address value. The translation regime that PMPCSR samples can be determined from PMPCSR.(NS,EL).

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**PCSample[31:0], bits [31:0]**

Bits[31:0] of the sampled instruction address value.

PMPCSR[31:0] reads as **0xFFFFFFFF** when any of the following are true:

- The PE is in Debug state.
- PC Sample-based profiling is prohibited.

If an instruction has retired since the PE left Reset state, then the first read of PMPCSR[31:0] is permitted but not required to return **0xFFFFFFFF**.

PMPCSR[31:0] reads as an **UNKNOWN** value when any of the following are true:

- The PE is in Reset state.
- No instruction has retired since the PE left Reset state, Debug state, or a state where PC Sample-based Profiling is prohibited.
- No instruction has retired since the last read of PMPCSR[31:0].

For the cases where a read of PMPCSR[31:0] returns **0xFFFFFFFF** or an **UNKNOWN** value, the read has the side-effect of setting PMPCSR[63:32], **PMCID1SR**, **PMCID2SR**, and **PMVIDSR** to **UNKNOWN** values.

Otherwise, a read of PMPCSR[31:0] returns bits [31:0] of the sampled instruction address value and has the side-effect of indirectly writing to PMPCSR[63:32], **PMCID1SR**, **PMCID2SR**, and **PMVIDSR**. The translation regime that PMPCSR samples can be determined from PMPCSR.(NS,EL).

For a read of PMPCSR[31:0] from the memory-mapped interface, if PMLSR.SLK == 1, meaning the **OPTIONAL** Software Lock is locked, then the side-effect of the access does not occur and PMPCSR[63:32], **PMCID1SR**, **PMCID2SR**, and **PMVIDSR** are unchanged.

On a Cold reset, this field resets to an architecturally **UNKNOWN** value.

**Accessing the PMPCSR**

**IMPLEMENTATION DEFINED** extensions to external debug might make the value of this register **UNKNOWN**, see 'Permitted behavior that might make the PC Sample-based profiling registers **UNKNOWN**'.

**PMPCSR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x200</td>
<td>PMPCSR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
PMPCSR, Program Counter Sample Register

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x204</td>
<td>PMPCSR</td>
<td>63:32</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x220</td>
<td>PMPCSR</td>
<td>31:0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
<th>Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x224</td>
<td>PMPCSR</td>
<td>63:32</td>
</tr>
</tbody>
</table>
The PMPIDR0 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMPIDR0 is a 32-bit register.

**Field descriptions**

The PMPIDR0 bit assignments are:

| 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| Res0 | Part_0 |

**Bits [31:8]**

Reserved, RES0.

**Part_0, bits [7:0]**

Part number, least significant byte.

**Accessing the PMPIDR0**

PMPIDR0 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFE0</td>
<td>PMPIDR0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
The PMPIDR1 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMPIDR1 is a 32-bit register.

**Field descriptions**

The PMPIDR1 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
</tr>
<tr>
<td>30</td>
<td>DES_0</td>
</tr>
<tr>
<td>29</td>
<td>PART_1</td>
</tr>
<tr>
<td>28</td>
<td></td>
</tr>
<tr>
<td>27</td>
<td></td>
</tr>
<tr>
<td>26</td>
<td></td>
</tr>
<tr>
<td>25</td>
<td></td>
</tr>
<tr>
<td>24</td>
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<td>23</td>
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<tr>
<td>22</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td></td>
</tr>
<tr>
<td>18</td>
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<td>17</td>
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<td>3</td>
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<tr>
<td>2</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

**Bits [31:8]**

Reserved, RES0.

**DES_0, bits [7:4]**

Designer, least significant nibble of JEP106 ID code. For Arm Limited, this field is 0b1011.

**PART_1, bits [3:0]**

Part number, most significant nibble.

**Accessing the PMPIDR1**

**PMPIDR1 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFE4</td>
<td>PMPIDR1</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
The PMPIDR2 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMPIDR2 is a 32-bit register.

**Field descriptions**

The PMPIDR2 bit assignments are:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31</td>
<td>RES0</td>
<td>Reserved, unused</td>
</tr>
<tr>
<td>30</td>
<td>REVISION</td>
<td>Part major revision. Parts can also use this field to extend Part number to 16-bits.</td>
</tr>
<tr>
<td>29</td>
<td>JEDEC</td>
<td>RA0. Indicates a JEP106 identity code is used.</td>
</tr>
<tr>
<td>28</td>
<td>DES_1</td>
<td>Designer, most significant bits of JEP106 ID code. For Arm Limited, this field is 0b011.</td>
</tr>
</tbody>
</table>

**Accessing the PMPIDR2**

PMPIDR2 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFE8</td>
<td>PMPIDR2</td>
</tr>
</tbody>
</table>
This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
The PMPIDR3 characteristics are:

**Purpose**

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

**Configuration**

Implementation of this register is **OPTIONAL**.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

**Attributes**

PMPIDR3 is a 32-bit register.

**Field descriptions**

The PMPIDR3 bit assignments are:

<table>
<thead>
<tr>
<th>Bit Assignment</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RES0</td>
<td>Reserved, reserved (RES0)</td>
</tr>
<tr>
<td>REVAND</td>
<td>Part minor revision. Parts using PMPIDR2.REVISION as an extension to the Part number must use this field as a major revision number.</td>
</tr>
<tr>
<td>CMOD</td>
<td>Customer modified. Indicates someone other than the Designer has modified the component.</td>
</tr>
</tbody>
</table>

**Accessing the PMPIDR3**

PMPIDR3 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFEC</td>
<td>PMPIDR3</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are **RO**.
- Otherwise accesses to this register generate an error response.
The PMPIDR4 characteristics are:

### Purpose

Provides information to identify a Performance Monitor component.

For more information, see 'About the Peripheral identification scheme'.

### Configuration

Implementation of this register is OPTIONAL.

If FEAT_DoPD is implemented, this register is in the Core power domain. If FEAT_DoPD is not implemented, this register is in the Debug power domain.

This register is required for CoreSight compliance.

### Attributes

PMPIDR4 is a 32-bit register.

### Field descriptions

The PMPIDR4 bit assignments are:

<table>
<thead>
<tr>
<th>Bit assignments</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>31-8</td>
<td>Reserved, RES0.</td>
</tr>
<tr>
<td>7-4</td>
<td>SIZE, bits [7:4]. Size of the component. RAZ. Log₂ of the number of 4KB pages from the start of the component to the end of the component ID registers.</td>
</tr>
<tr>
<td>3-0</td>
<td>DES_2, bits [3:0]. Designer, JEP106 continuation code, least significant nibble. For Arm Limited, this field is 0b0100.</td>
</tr>
</tbody>
</table>

### Accessing the PMPIDR4

PMPIDR4 can be accessed through the external debug interface:

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xFD0</td>
<td>PMPIDR4</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When FEAT_DoPD is not implemented or IsCorePowered() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.
PMSWINC_EL0, Performance Monitors Software Increment register

The PMSWINC_EL0 characteristics are:

**Purpose**

Increments a counter that is configured to count the Software increment event, event 0x00. For more information, see SW_INCR.

**Configuration**

External register PMSWINC_EL0 bits [31:0] are architecturally mapped to AArch64 System register PMSWINC_EL0[31:0].

External register PMSWINC_EL0 bits [31:0] are architecturally mapped to AArch32 System register PMSWINC[31:0].

PMSWINC_EL0 is in the Core power domain.

Implementation of this register is **OPTIONAL**.

If this register is implemented, use of it is deprecated.

If 1 is written to bit [n] from the external debug interface, it is **CONSTRAINED UNPREDICTABLE** whether or not a SW_INCR event is created for counter n. This is consistent with not implementing the register in the external debug interface.

**Attributes**

PMSWINC_EL0 is a 32-bit register.

**Field descriptions**

The PMSWINC_EL0 bit assignments are:

<table>
<thead>
<tr>
<th>31</th>
<th>30</th>
<th>29</th>
<th>28</th>
<th>27</th>
<th>26</th>
<th>25</th>
<th>24</th>
<th>23</th>
<th>22</th>
<th>21</th>
<th>20</th>
<th>19</th>
<th>18</th>
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<th>16</th>
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<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
</table>

**Bit [31]**

Reserved, RES0.

**P<n>, bit [n], for n = 30 to 0**

Event counter software increment bit for PMEVCNTR<n>_EL0.

If PMCFGR.N is less than 31, bits [30:PMCFGR.N] are WI.

<table>
<thead>
<tr>
<th>P&lt;n&gt;</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td>0b0</td>
<td>No action. The write to this bit is ignored.</td>
</tr>
<tr>
<td>0b1</td>
<td>It is <strong>CONSTRAINED UNPREDICTABLE</strong> whether a SW_INCR event is generated for event counter n.</td>
</tr>
</tbody>
</table>

**Accessing the PMSWINC_EL0**

**Note**
SoftwareLockStatus() depends on the type of access attempted and AllowExternalPMUAccess() has a new definition from Armv8.4. Refer to the Pseudocode definitions for more information.

**PMSWINC_EL0 can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0xCA0</td>
<td>PMSWINC_EL0</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and SoftwareLockStatus() accesses to this register are **WI**.
- When IsCorePowered(), !DoubleLockStatus(), !OSLockStatus(), AllowExternalPMUAccess() and !SoftwareLockStatus() accesses to this register are **WO**.
- Otherwise accesses to this register generate an error response.
PMVIDSR, VMID Sample Register

The PMVIDSR characteristics are:

**Purpose**

Contains the sampled VMID value that is captured on reading PMPCSR[31:0].

**Configuration**

PMVIDSR is in the Core power domain.

This register is present only when FEAT_PCSRv8p2 is implemented and EL2 is implemented. Otherwise, direct accesses to PMVIDSR are RES0.

---

**Note**

Before Armv8.2, the PC Sample-based Profiling Extension can be implemented in the external debug register space, as indicated by the value of EDDEVID.PCSample.

---

**Attributes**

PMVIDSR is a 32-bit register.

**Field descriptions**

The PMVIDSR bit assignments are:

| 31  | 30  | 29  | 28  | 27  | 26  | 25  | 24  | 23  | 22  | 21  | 20  | 19  | 18  | 17  | 16  | 15  | 14  | 13  | 12  | 11  | 10  | 9   | 8   | 7   | 6   | 5   | 4   | 3   | 2   | 1   | 0   |
|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| RES0| VMID[15:8] | VMID |

**Bits [31:16]**

Reserved, RES0.

**VMID[15:8], bits [15:8]**

When FEAT_Vomid16 is implemented:

Extension to VMID[7:0]. See VMID[7:0] for more details.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

**Otherwise:**

Reserved, RES0.

**VMID, bits [7:0]**

VMID sample. The VMID associated with the most recent PMPCSR sample. When the most recent PMPCSR sample was generated:

- This field is set to an UNKNOWN value if any of the following apply:
  - EL2 is disabled in the current Security state.
  - The PE is executing at EL2.
EL2 is enabled in the current Security state, the PE is executing at EL0, EL2 is using AArch64, HCR_EL2.E2H == 1, and HCR_EL2.TGE == 1.

- Otherwise:
  - If EL2 is using AArch64 and either FEAT_VMID16 is not implemented or VTCR_EL2.VS is 1, this field is set to VTTBR_EL2.VMID.
  - If EL2 is using AArch64, FEAT_VMID16 is implemented, and VTCR_EL2.VS is 0, PMVIDSR.VMID[7:0] is set to VTTBR_EL2.VMID[7:0] and PMVIDSR.VMID[15:8] is RES0.
  - If EL2 is using AArch32, this field is set to VTTBR.VMID.

Because the value written to PMVIDR is an indirect read of the VMID value, it is CONSTRAINED UNPREDICTABLE whether PMVIDSR is set to the original or new value if PMPCSR samples:

- An instruction that writes to the VMID value.
- The next Context synchronization event.
- Any instruction executed between these two instructions.

On a Cold reset, this field resets to an architecturally UNKNOWN value.

## Accessing the PMVIDSR

IMPLEMENTATION DEFINED extensions to external debug might make the value of this register UNKNOWN, see 'Permitted behavior that might make the PC Sample-based profiling registers UNKNOWN'.

**PMVIDSR can be accessed through the external debug interface:**

<table>
<thead>
<tr>
<th>Component</th>
<th>Offset</th>
<th>Instance</th>
</tr>
</thead>
<tbody>
<tr>
<td>PMU</td>
<td>0x20C</td>
<td>PMVIDSR</td>
</tr>
</tbody>
</table>

This interface is accessible as follows:

- When IsCorePowered(), !DoubleLockStatus() and !OSLockStatus() accesses to this register are RO.
- Otherwise accesses to this register generate an error response.