



PrimeCell® Infrastructure AMBA™ 3 AXI™ Internal Memory Interface (BP140)

Revision: r0p0

Technical Overview

This technical overview describes the functionality of the AXI internal memory interface in the following sections:

- *Preliminary material* on page 2
- *About the internal memory interface* on page 3
- *Functional description* on page 4
- *Physical data* on page 6
- *Signal descriptions* on page 8.

1 Preliminary material

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1.1 Release information

Changes to this document are listed in Table 1.

Table 1 Change history

Date	Issue	Change
26 November 2004	A	First issue for r0p0

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1.4 Product status

The information in this document is for an final product, that is a developed product.

1.5 Web address

<http://www.arm.com>

2 About the internal memory interface

The AXI internal memory interface, IntMemAxi, has the following features:

- It provides a single-port memory interface configurable for synchronous SRAM or ROM.
- The HDL code is supplied as Verilog.
- The memory footprint is that of the connected SRAM or ROM.
- It accepts a single address for each of the read and write channels.
- It uses round-robin arbitration between read and write transactions, the default is read.
- For write transactions, the first data transfer can take place 2 cycles after the address is accepted. Subsequent data transfers can complete in consecutive cycles.
- For read transactions:
 - With one wait state
 - The first data transfer can take place 2 cycles after the address is accepted. Subsequent data transfers can complete in consecutive cycles.
 - With zero wait states
 - The first data transfer can take place 3 cycles after the address is accepted. Subsequent data transfers take 2 cycles.
- It supports:
 - all AMBA AXI channels except the low power channel
 - all AXI burst types
 - aligned and unaligned transfer types.
- You can configure the following parameters:
 - data width of 64 bits or 32 bits
 - ID width
 - wait states, single or none, for SRAM and ROM reads
 - whether the interface is to be used with SRAM or ROM
 - memory read access to be zero or one wait-state
 - MEM_ADDR_WIDTH, MEM_INIT_FILE_0, and MEM_INIT_FILE_1 for IntMemBhavAxi.

3 Functional description

Figure 1 shows how you can use the IntMemAxi component to interface to a synthesized SRAM. It can also be connected to ROM.

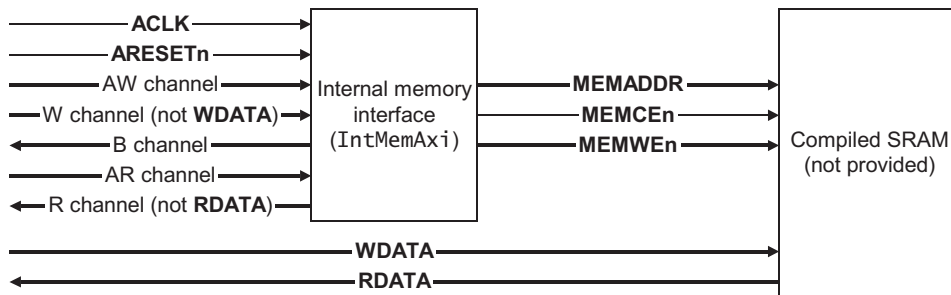


Figure 1 Internal memory interface connected to compiled SRAM

Figure 2 shows how you can use the internal memory behavioral component, IntMemBhavAxi. This includes the memory interface and a behavioral SRAM model. You can use this as a memory slave for behavioral testbenches.

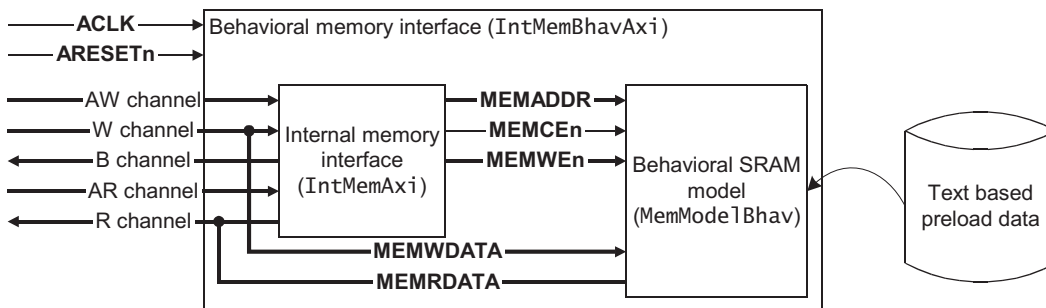


Figure 2 Behavioral memory interface

The interface does not have an AXI low-power interface because it does not initiate transactions or have a low-power mode of operation.

3.1 Interface attributes

Table 1 lists the slave interface attributes for the IntMemAxi.

Table 1 Slave interface attributes

Attribute	Description	Value
Write acceptance capability	The maximum number of active write transactions that a slave can accept.	1
Read acceptance capability	The maximum number of active read transactions that a slave can accept.	1
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	1
Read data reorder depth	The number of active read transactions for which a slave may transmit data. This is counted from the earliest transaction.	1

4 Physical data

Physical data is provided in:

- *AC characteristics*
- *Gate count* on page 7.

4.1 AC characteristics

The interface conforms to the following timing guidelines:

- AXI inputs must be valid for 30% of the cycle before the rising edge of **CLK** and outputs must become valid within 20% of cycle after the rising edge of **CLK**.
- Timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

The signals on the memory port of the interface conform to the timing requirements required by the single ported synchronous memory component produced by RAM Compiler for the TSMC CL013G process technology with the following compiled features:

- 16384x32
- Mux 32
- Drive 6
- 8-bit mask write.

4.2 Gate count

Table 2 lists estimated NAND2X1 equivalent gate counts for the target frequency and library specified in *AC characteristics* on page 6.

Table 2 Gate count estimates

Data bus width	Read wait-state implementation	Gate count
64-bit	zero	1720
	single	1720
32-bit	zero	1720
	single	1720

Note

The gate count estimates in Table 2 do not include scan logic.

5 Signal descriptions

The AXI interface of the internal memory interface uses the signals described in the *AMBA AXI Protocol Specification*. The memory interface signals are described in *Memory interface* on page 9. Figure 3 shows the interface signal connections.

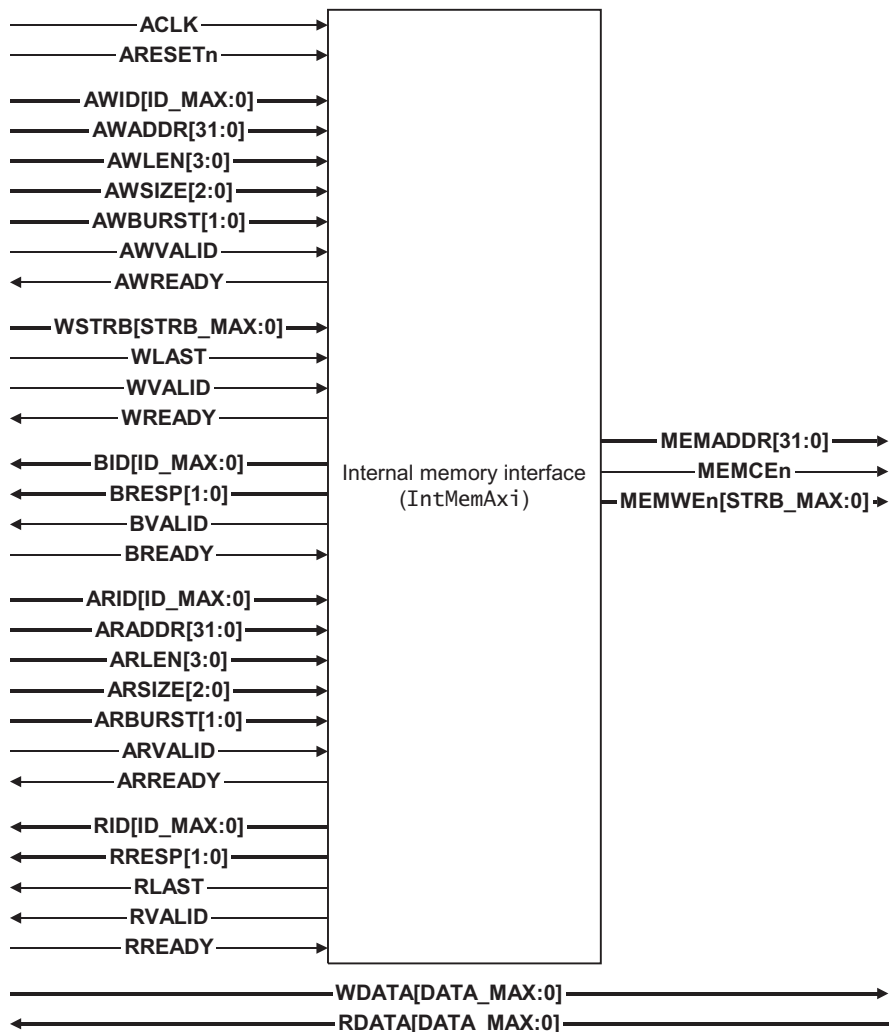


Figure 3 Internal memory interface signal connections

————— **Note** —————
WDATA and **RDATA** bypass the component.

5.1 Memory interface

Table 3 lists the connection information for the memory interface signals.

Table 3 Memory interface signal descriptions

SRAM signal	Connection	SRAM	SRAM	Interface signal name	Signal direction
CLK	Connect to ACLK	Yes	Yes	-	-
CEn^a	Output from IntMemAxi	Yes	Yes	MEMCEn	Output
WEn^a	Output from IntMemAxi	Yes	No	MEMWEn[STRB_MAX:0]	Output
OEn^a	Tied permanently enabled if present	-	-	-	-
Q	Connect to RDATA	Yes	Yes	-	-
D	Connect to WDATA	Yes	No	-	-
A	Output from IntMemAxi	Yes	Yes	MEMADDR[31:0]	Output

a. Active-LOW.

