PrimeCell® Infrastructure AMBA™ 3 AXI™ to AMBA 2 AHB™ Bridges (BP137)

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Technical Overview

ARM®

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PrimeCell Infrastructure AMBA 3 AXI to AMBA 2 AHB Bridges (BP137)
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Release Information

The following changes have been made to this book.

Change History

Date	Issue	Confidentiality	Change
17 December 2004	A	Non-Confidential	Issue for r0p0.
08 September 2005	B	Non-Confidential	Issue for r0p1.
08 February 2006	C	Non-Confidential	Update for r0p2, sideband signal information.

Proprietary Notice

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The information in this document is final, that is for a developed product.

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Chapter 1
AXI to AHB bridges

This Technical Overview describes the AXI to AHB bridges. It contains the following sections:

1.1 About the AXI to AHB bridges

The following sections describe the configurations that you can implement for an AXI to AHB bridge:

- *AXI to ARM11 AHB-Lite bridge*
- *AXI to ARM11 AHB-Lite master bridge*
- *AXI to ARM11 AHB-Lite master bridge with OVL assertions* on page 1-3
- *AXI to ARM11 AHB-Lite slave bridge* on page 1-4.

1.1.1 AXI to ARM11 AHB-Lite bridge

The AXI to ARM11 AHB-Lite bridge implements an AXI slave port and an ARM11 AHB-Lite master port to enable, for example, an ARM11 AHB-Lite system to be connected to an AXI master.

The *Systems IP ARM11 AMBA AHB Extensions Specification* defines the ARM11 extensions to the standard AHB specification.

For more information on AHB-Lite see *AHB Lite Overview* (ARM DVI 0044).

1.1.2 AXI to ARM11 AHB-Lite master bridge

The AXI to AHB-Lite master bridge that Figure 1-1 shows, implements the AXI to ARM11 AHB-Lite bridge together with the components required to provide an AHB-Lite master interface. This enables, for example, an AHB-Lite system to be connected to an AXI master.

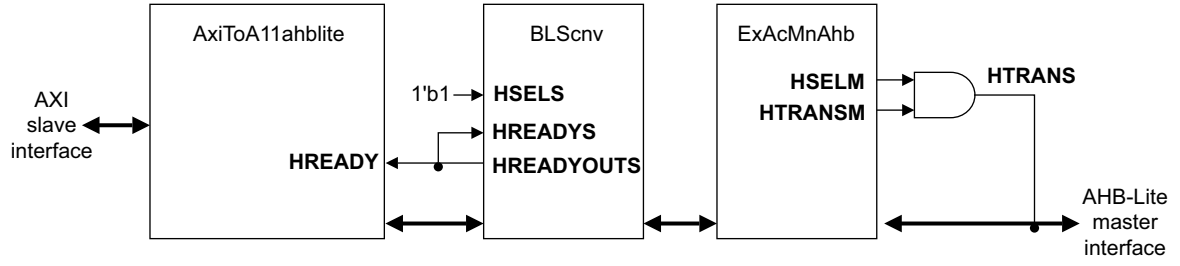

Figure 1-1 AXI to AHB_Lite master bridge

The other components in Figure 1-1 on page 1-2 are:

Byte lane strobe converter

The byte lane strobe converter, **BLScnv**, is an AHB slave gasket that supports the byte lane strobe functionality that the *Systems IP ARM11 AMBA AHB Extensions Specification* defines.

Exclusive access monitor

The exclusive access monitor, `ExAcMn`, is an AHB slave gasket that supports the exclusive access functionality that the *Systems IP ARM11 AMBA AHB Extensions Specification* defines. It grants up to two masters exclusive access to a slave.

1.1.3 AXI to ARM11 AHB-Lite master bridge with OVL assertions

If you do not require the complexity of the configuration that *AXI to ARM11 AHB_Lite master bridge* on page 1-12 describes then you can configure the component as a bridge that converts the ARM11 AHB-Lite master interface into an AHB-Lite master interface. This is achieved by tying-off the following signals:

- **HPROT[5:4]** are not propagated. There is no support for exclusive, cache allocate transfer indication.
- **HBSTRB** and **HUNALIGN** are not propagated. There is no support for unaligned or sparse transfers.
- **HRESP[2]** is tied LOW. There is no support for exclusive responses.

The AXI to AHB-Lite bridge wraps the AxiToA11Lite bridge selectively to create an AHB-Lite master interface. The bridge contains OVL assertions that guard against unsupported features of the AXI protocol. Figure 1-2 shows the bridge.

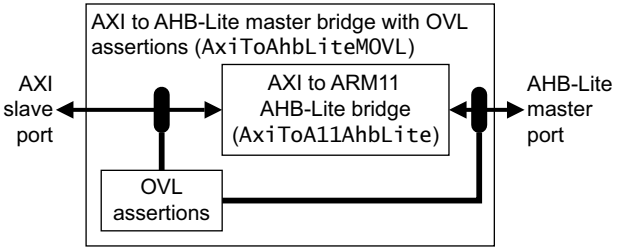

Figure 1-2 AXI to AHB-Lite master bridge with OVL assertions

1.1.4 AXI to ARM11 AHB-Lite slave bridge

The AXI to AHB-Lite slave bridge that Figure 1-3 shows implements the AXI to ARM11 AHB-Lite bridge together with the components required to provide an AHB-Lite slave-gasket interface. This enables, for example, an AHB-Lite slave to be connected to an AXI system.

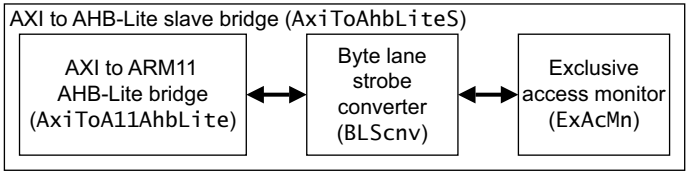

Figure 1-3 AXI to AHB_Lite slave bridge

The bridge uses the byte lane strobe converter and exclusive access monitor as *AXI to ARM11 AHB_Lite master bridge* on page 1-12 describes.

1.2 Functional description

The AXI to ARM11 AHB-Lite bridge has the following features:

- It translates AXI transactions to AHB-Lite bursts with the following restrictions:
  - exclusive accesses are available by using the bridge and an external exclusive access monitor
  - unaligned and sparse accesses are available by using the AXI ARM11 AHB-Lite bridge together with an ARM11-capable AHB interconnect, or an external byte lane strobe converter.
- The bridge only supports one outstanding transaction at any one time on each address channel. *Interface attributes* on page 1-6 describes this.
- Initiation of AHB write bursts are related to AXI address and write channel transfers:

  there is a minimum latency of two clock cycles from the acceptance of an AXI transaction, **AWVALID** or **ARVALID** asserted, to the start of the AHB transaction when **HTRANS** is driven to **NONSEQ**
  - the first data transfer in a write burst waits for the AXI address, **AWVALID**, and the first AXI write transfer, **WVALID**
  - subsequent data transfers in a write burst wait for the AXI write transfer, **WVALID**, and busy cycles are issued on the AHB domain until the data arrives
  - the AXI write response is issued on the completion of the final write data data transfer of the burst.
- Initiation of AHB read bursts are related to AXI address and read channel transfers:
  - the first AHB address is issued on or after the arrival of the AXI address transfer, **ARVALID**
  - subsequent AHB transfers wait for the acceptance of the read data by the AXI read channel, **RREADY**, and busy cycles are issued on the AHB domain until the data has been accepted.
- Only the **OKAY**, **EXOKAY** and **SLVERR** responses are generated:
  - an error response returned on any data transfer of an AHB write burst causes a write response of **SLVERR**
  - read responses are translated on a per transfer basis

  - an AHB **XFAIL** response results in an AXI **OKAY** response and an AHB **OKAY** response to an exclusive access results in an AXI **EXOKAY** response.

- All AXI transactions are mapped, where possible, to an equivalent AHB burst:
  - wrapping and incrementing bursts of length 4, 8, and 16 are converted into the equivalent length AHB bursts
  - incrementing bursts of length 1, wrapping bursts of length 2, and all fixed address transactions are converted to sequences of AHB SINGLE bursts
  - any burst that crosses a 1KB address boundary is converted into **INCR** bursts with the burst restarted, **HTRANS** is overridden to **NONSEQ**, when the boundary is crossed
  - all remaining incrementing and wrapping bursts are converted into AHB **INCR** bursts.
- AXI **xUSER** sideband signals are mapped onto additional AHB domain sideband signals:
  - AXI **ARUSER** and **AWUSER**, as appropriate, are used for **HAUSER**, an address phase signal
  - AXI **WUSER** is used for **HWUSER**, a data phase signal
  - a data phase **HRUSER** signal is used for the AXI **RUSER** signal
  - the AXI **BUSER** signal is unused.

  You can parametrize the width of the address phase signals and data phase signals between 1 and 32.
- The address transfer ID is used for read and write transfers:
  - ARID is used for the associated **RID**, and for **HMASTER** during AHB read transfers
  - AWID is used for the associated **BID**, and for **HMASTER** during AHB write transfers.
- HDL code is supplied as Verilog.

1.2.1 Interface attributes

Table 1-1 on page 1-7 lists the interface attributes for the AXI to AHB bridges.

Table 1-1 Slave interface attributes

Attribute	Description	Value
Write acceptance capability	The maximum number of active write transactions that a slave can accept.	1
Read acceptance capability	The maximum number of active read transactions that a slave can accept.	1
Write interleave depth	The number of active write transactions for which the slave can receive data. This is counted from the earliest transaction.	1
Read data reorder depth	The number of active read transactions for which a slave can transmit data. This is counted from the earliest transaction.	1

1.3 Physical data

Physical data is provided in:

- *AC characteristics*
- *Gate count* on page 1-10.

1.3.1 AC characteristics

Timing closure might be difficult to obtain in a complex system because the AXI to AHB gasket contains combinatorial paths. The easiest way to rectify this is to use an AXI register slice or buffer on any channels that do not meet timing. This, however, incurs a latency penalty that might not be desirable if interfacing to an AHB or APB interrupt controller.

Trial synthesis using Synopsys Design Compiler was performed with a clock cycle of 5ns, 200MHz, skew 2.5%, on the Artisan SAGE HS library for the TSMC CL013G process, sample 0.13µm cell library, slow-slow process corner, with no resulting timing violations.

The following sections provide the timing constraints:

- *AXI to ARM11 AHB_Lite bridge timing constraints*
- *AXI to ARM11 AHB_Lite master bridge timing constraints* on page 1-9
- *AXI to ARM11 AHB_Lite slave bridge timing constraints* on page 1-9.

AXI to ARM11 AHB_Lite bridge timing constraints

Figure 1-4 on page 1-9 shows the constraint strategy used for the AXI ARM11 AHB-Lite bridge core during development. The figures denote the percentage of clock cycle permitted for each function. The timing constraints are:

- paths from inputs to registers are permitted 30% of the clock cycle
- paths from registers to outputs are permitted 20% of the clock cycle
- combinatorial through paths between AXI and AHB ports are permitted 30% of the clock cycle.

Note

These figures are also relevant for the AXI to AHB-Lite master bridge with OVL assertions.

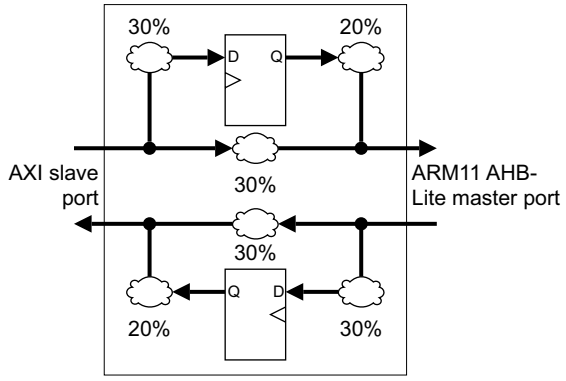

Figure 1-4 AXI to AHB-Lite bridge timing constraints

AXI to ARM11 AHB_Lite master bridge timing constraints

The timing constraints are:

- paths from inputs to registers are permitted 40% of the clock cycle
- paths from registers to outputs are permitted 30% of the clock cycle
- combinatorial through paths between AXI and AHB ports are permitted 40% of the clock cycle.

AXI to ARM11 AHB_Lite slave bridge timing constraints

The timing constraints are:

- paths from inputs to registers are permitted 40% of the clock cycle
- paths from registers to outputs are permitted 30% of the clock cycle
- combinatorial through paths between AXI and AHB ports are permitted 40% of the clock cycle.

1.3.2 Gate count

Table 1-2 lists the estimated gate count in the library that *AC characteristics* on page 1-8 specifies.

Table 1-2 Gate counts

Bridge	NAND2X1 equivalents	
	32-bit data width	62-bit data width
AXI to ARM11 AHB-Lite	3700	4800
AXI to AHB-Lite master	6700	8300
AXI to AHB-Lite master with OVL assertions	3500	4500
AXI to AHB-Lite slave	6800	8300

Note

These gate count estimates do not include scan logic.

The ID_WIDTH parameter was set to 4 for all estimates.

1.4 Signal descriptions

The following sections describe the signals that the bridges use:

- *AXI to ARM11 AHB_Lite bridge*
- *AXI to ARM11 AHB_Lite master bridge* on page 1-12
- *AXI to ARM11 AHB_Lite master bridge with OVL assertions* on page 1-13
- *AXI to ARM11 AHB_Lite slave bridge* on page 1-13.

Note

The upper value of some bus widths is provided as a name to indicate that the number of signal lines in the bus is derived from user-defined generics or parameters. *PrimeCell Infrastructure AMBA 3 AXI to AMBA 2 AHB Bridges (BP137) Design Manual* describes these.

1.4.1 AXI to ARM11 AHB_Lite bridge

The AXI to ARM11 AHB-Lite bridge signals that Figure 1-5 on page 1-12 shows are:

- standard AXI signals that the *AMBA AXI Protocol Specification* describes
- ARM11 AHB-Lite signals that the *Systems IP ARM11 AMBA AHB Extensions Specification* and the *AMBA Specification (Rev 2.0)* describe.

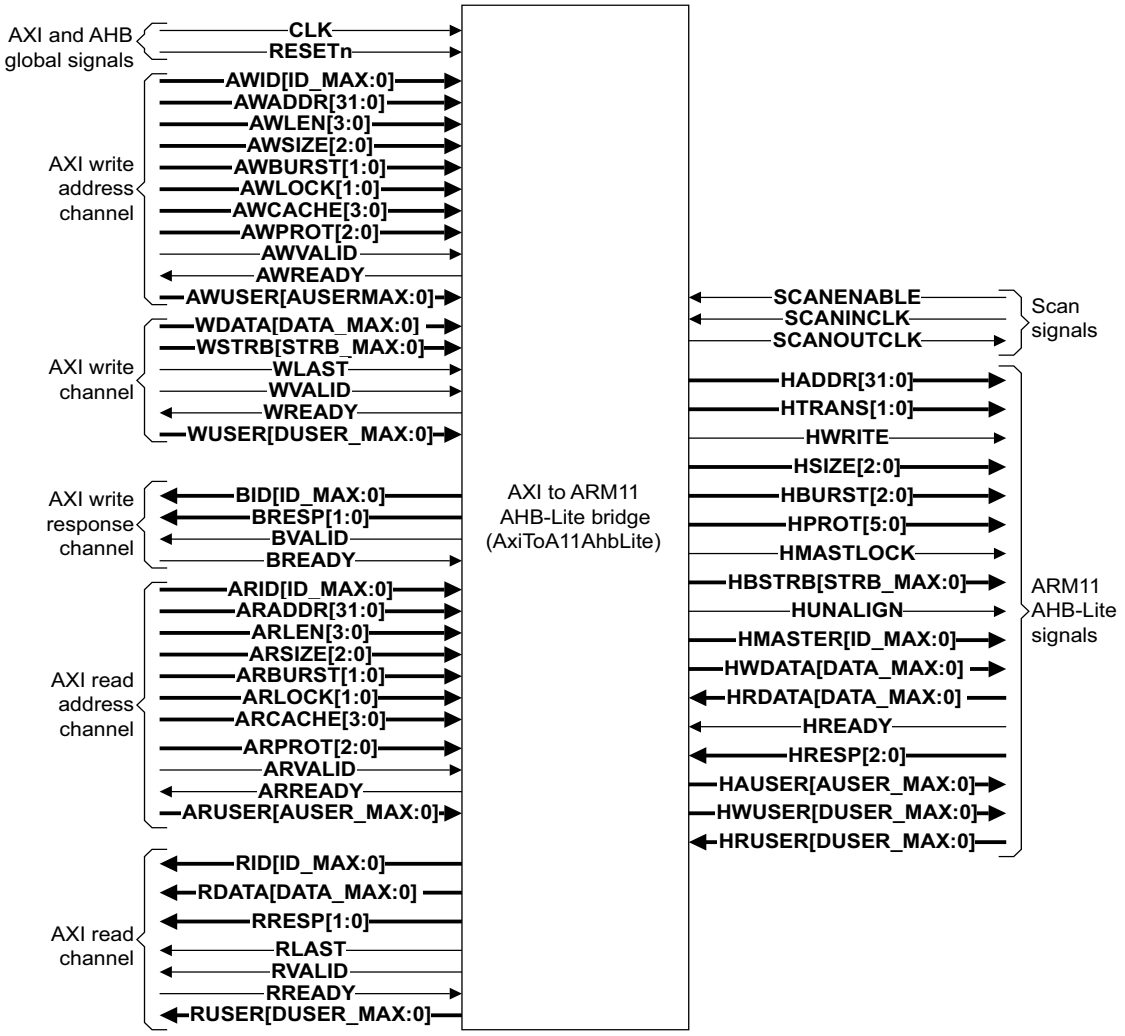

Figure 1-5 AXI to ARM11 AHB-Lite bridge signal connections

1.4.2 AXI to ARM11 AHB_Lite master bridge

The AXI to AHB-Lite master bridge signals are standard:

- Figure 1-5 shows:
  - the AXI and AHB global clock and reset signals
  - the scan signals.

- the *AMBA AXI Protocol Specification* describes the AXI signals, and Figure 1-5 on page 1-12 shows them
- the *AMBA Specification (Rev 2.0)* describes the AHB-Lite signals, and Figure 1-6 shows them.

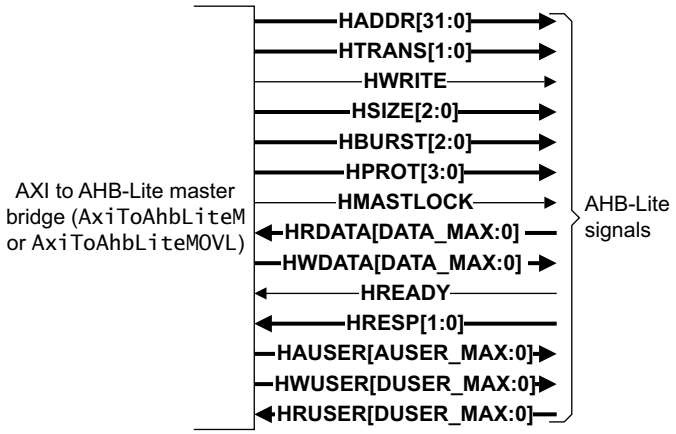

Figure 1-6 AXI to AHB-Lite master bridge signal connections

1.4.3 AXI to ARM11 AHB_Lite master bridge with OVL assertions

The AXI to AHB-Lite master bridge signals are standard:

- Figure 1-5 on page 1-12 shows:
  - — the AXI and AHB global clock and reset signals
  - — the scan signals.
- the *AMBA AXI Protocol Specification* describes the AXI signals, and Figure 1-5 on page 1-12 shows them
- the *AMBA Specification (Rev 2.0)* describes the AHB-Lite signals, and Figure 1-6 shows them.

1.4.4 AXI to ARM11 AHB_Lite slave bridge

The AXI to AHB-Lite slave bridge signals are standard:

- Figure 1-5 on page 1-12 shows:
  - — the AXI and AHB global clock and reset signals
  - — the scan signals.

- the *AMBA AXI Protocol Specification* describes the AXI signals, and Figure 1-5 on page 1-12 shows them
- the *AMBA Specification (Rev 2.0)* describes the AHB-Lite signals, and Figure 1-6 on page 1-13 shows them.

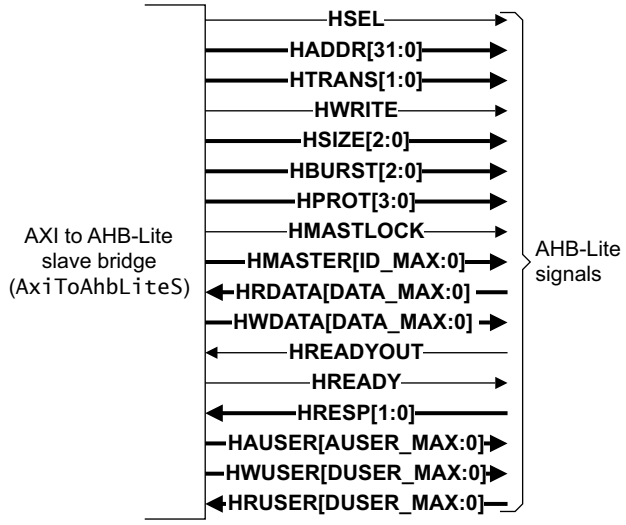

Figure 1-7 AXI to AHB_Lite slave bridge signal connections