ARM®

PrimeCell® Infrastructure AMBA™ 3 AXI Downsizer (BP131) Revision: r0p0
Technical Overview

This Technical Overview describes the functionality of the AXI downsizer in the following sections:

1 Preliminary material

1.1 Release information

Table 1 lists the changes to this document.

Table 1 Change History

Date	Issue	Confidentiality	Change
28 June 2005	A	Non-Confidential	First issue for r0p0

1.2 Proprietary notice

1.3 Confidentiality status

This document is Non-Confidential. This document can only be distributed in accordance with the terms set out in your license agreement.

1.4 Product status

The information in this document is final, that is for a developed product.

1.5 Web address

http://www.arm.com

2 About the AXI downsizer

DownsizerAxi is an AXI infrastructure component that enables you to connect a 64-bit AXI bus to a 32-bit AXI bus. It converts 64-bit AXI transactions into appropriate 32-bit transactions, and handles the multiplexing of the data channels.

The AXI downsizer has the following features:

- Implements a 64-bit data-width AXI slave port and a 32-bit AXI master port.
- Address transfers of 8, 16, and 32-bit pass through unchanged. The associated data transfers are multiplexed onto the correct byte lanes on each port.
- The latency of DownsizerAXI is as follows:
  - **AxVALIDS** to **AxVALIDM**, one clock cycle[1]
  - **ARVALIDS** to **RVALIDS**, two clock cycles in pass-through mode, and three clock cycles in downsize mode[2]
  - **AWVALIDS** to **WVALIDM**, two clock cycles[2, 3].
- Each data channel, read and write, includes buffering for two active transactions, that enables the address translation latency to be isolated from the maximum data bandwidth for transactions with lengths greater than 1.
- 64-bit transactions are modified as follows:
  - **AxSIZE** is changed to indicate 32-bit[1]
  - any WRAP or INCR burst of length eight or less is doubled in length, **AxLEN** changed[1]
  - any INCR burst of length nine or more is split into two transactions, **AxLEN** copied[1]
  - any 16-word aligned WRAP burst of length 16 is split into two INCR transactions
  - any WRAP burst of length 16 that is not 16-word aligned is split into three INCR transactions
  - any FIXED burst is split into a number of transactions equal to the length of the FIXED burst. Each of the transactions generated is a length 2 INCR burst, unless the original FIXED burst is unaligned, then the length is 1.

1. x can be either R or W.
2. This applies to the first data transfer of the transaction.
3. This assumes that **WVALID** for the first write data transfer is asserted when AWVALID is asserted.

- For locked sequences, if the terminating unlocked transfer is 64-bit, and results in multiple 32-bit transactions, then all 32-bit transactions except the ultimate one are locked.
- 64-bit exclusive accesses are supported except for transactions that would result in two or more 32-bit transactions. The AXI protocol defines that only a single outstanding exclusive transaction is permitted.

3 Functional description

DownsizerAxi is an AXI infrastructure component that enables you to connect a 64-bit AXI bus to a 32-bit AXI bus. It converts 64-bit AXI transactions into appropriate 32-bit transactions, and handles the multiplexing of the data channels.

The AXI Downsizer supports simultaneous read and write transactions. The read and write channels of DownsizerAxi operate in one of two modes:

- *Pass-through mode*
- *Downsize mode*.

3.1 Pass-through mode

When the size of an incoming transaction is 32 bits or less, DownsizerAxi operates in pass-through mode. In pass-through mode, the first data transfer of the transaction can take place two clock cycles after **AxVALIDS** is asserted. When a transaction is in progress, the input and output data channels are connected by combinatorial logic and data transfer continues at one data transfer per clock cycle.

3.2 Downsize mode

When the size of an incoming transaction is 64 bits, DownsizerAxi operates in downsize mode. In downsize mode, DownsizerAxi converts the incoming 64-bit transaction into one or more 32-bit transactions. The number of 32-bit transactions that DownsizerAxi generates depends on the burst type, **AxBURST**, and length, **AxLEN**, of the 64-bit transaction.

The first 32-bit data transfer of the transaction can take place two clock cycles after **AxVALIDS** is asserted. The first 64-bit transfer can complete three clock cycles after **AxVALIDS** is asserted. The extra clock cycle is required because the 64-bit data transfer is made up of two 32-bit data transfers.

When a transaction is in progress, data transfer continues at the maximum possible bandwidth of one 64-bit data transfer every two clock cycles.

3.3 AXI port attributes

Table 2 lists the AXI slave port attributes.

Table 2 AXI slave port attributes

Attribute	Value	Note
Write acceptance capability	2	The address translation core can accept two outstanding write address transactions
Read acceptance capability	2	The address translation core can accept two outstanding read address transactions
Write interleave depth	1	-

Table 3 lists the AXI master port attributes.

Table 3 AXI master port attributes

Attribute	Value	Note
Write issuing capability	32	Maximum of 32 only possible when translating two length 16 fixed transactions.
Write ID capability	See note	Limited by the writeID capability of the master port attached to the slave port of `DownsizerAxi`. That is, if the master attached to the `DownsizerAxi` slave port has a write ID capability of 1, then the `DownsizerAxi` master port write ID capability is limited to 1 in that system.
Write interleave capability	1	No write interleaving is performed.
Read issuing capability	32	Maximum of 32 only possible when translating two length 16 fixed transactions.
Read ID capability	See note	Limited by the read ID capability of the master port attached to the slave port of `DownsizerAxi`, as per write ID capability.

4 Physical data

Physical data is provided in:

- *AC characteristics*
- *Gate count*.

4.1 AC characteristics

The AXI downsizer conforms to the following timing parameters. The values refer to the percentage of the clock cycle allowed for each function:

- AXI inputs must be valid for 30% prior to the rising edge of the clock
- AXI outputs must be valid for 25% after the rising edge of the clock
- AXI-AXI combinatorial path delay for a maximum of 30% of the clock cycle.

Note

There are combinatorial paths from:

- RVALIDM to RREADYM
- RIDM to RREADYM.

The delay on these paths is a maximum of 30% of the clock cycle.

Timing characteristics are confirmed by performing synthesis on the block using the slow-slow process point of the Artisan SAGE HS library for the TSMC CL013G process at a target speed of 200MHz.

4.2 Gate count

The estimated gate count is 4 100 NAND-gate equivalents in the library specified in *AC characteristics*.

5 Signal descriptions

Figure 1 shows the AXI downsizer signal connections.

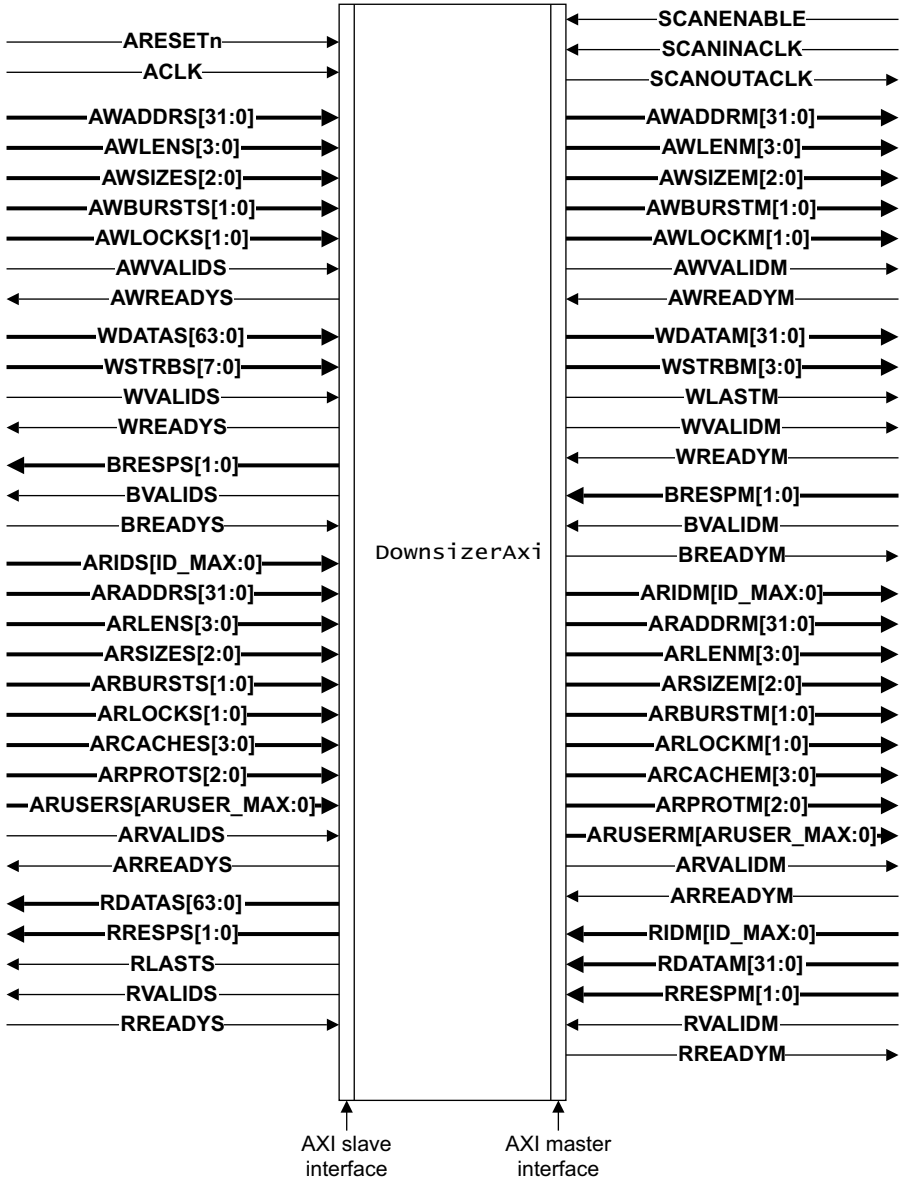

Figure 1 AXI downsizer signal connections

5.1 Non-standard signals

Table 4 lists the signals that are present on the downsizer, but that the *AMBA AXI Protocol Specification* does not describe.

Table 4 Non-standard signals

Name	Type	Source/destination	Description
SCANENABLE	Input	Scan logic	Scan mode enable
SCANINACLK	Input	Scan logic	Scan chain input
SCANOUTACLK	Output	Scan logic	Scan chain output

Note

The signals that Table 4 does not list are standard AMBA AXI signals that the *AMBA AXI Protocol Specification* describes. The signal names are appended with:

- the letter **M** for signals that connect to the component master interface
- the letter **S** for signals that connect to the component slave interface.

