

ARM920T/940T Header Card

(KPI-0043A and KPI-0034A)

User Guide

ARM

ARM920T/940T Header Card User Guide

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Release information

Change history

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Preface

This preface introduces the ARM920T/940T Header Card and its reference documentation. It contains the following sections:

- *About this document* on page iv
- *Further reading* on page vi
- *Feedback* on page vii.

About this document

This document is the ARM920T/940T Header Card User Guide.

Intended audience

This document has been written for experienced hardware and software engineers who wish to use an ARM920T or ARM940T header card, with their ARM development board, for code development and evaluation.

Organization

This document is organized into the following chapters:

Chapter 1 *Overview of the ARM920T/940T Header Card*

Read this chapter for an introduction to the ARM920T/940T Header Card.

Chapter 2 *Setting up your System*

Read this chapter for a description of how to set up the ARM development board to work with the ARM920T/940T Header Card.

Chapter 3 *Configuring the ARM920T/940T Header Card*

Read this chapter for a description of how to configure the ARM920T/940T Header Card.

Chapter 4 *Circuit Descriptions*

Read this chapter for a description of the circuit board of the ARM920T/940T Header Card.

Typographical conventions

The following typographical conventions are used in this document:

bold	Highlights ARM processor signal names within text, and interface elements such as menu names. May also be used for emphasis in descriptive lists where appropriate.
<i>italic</i>	Highlights special terminology, cross-references and citations.
typewriter	Denotes text that may be entered at the keyboard, such as commands, file names and program names, and source code.

typewriter Denotes a permitted abbreviation for a command or option. The underlined text may be entered instead of the full command or option name.

typewriter italic Denotes arguments to commands or functions where the argument is to be replaced by a specific value.

typewriter bold Denotes language keywords when used outside example code.

Further reading

This section lists publications by ARM Limited.

ARM publications

For additional information, refer to the following:

- *ARM Target Development System User Guide* (ARM DUI 0061).
- *ARM Multi-ICE User Guide* (ARM DUI 0048).
- *ARM Software Development Toolkit User Guide* (ARM DUI 0040).
- *Logic Expansion Card User Guide* (ARM DUI 0074).

Feedback

ARM Limited welcomes feedback both on the ARM920T/940T header card, and on the documentation.

Feedback on this document

If you have any comments on this document, please send email to errata@arm.com giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the ARM920T/940T header card

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- a concise explanation of your comments.

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Chapter 1

Overview of the ARM920T/940T Header Card

This chapter introduces the ARM920T/940T header card and contains the following sections:

- *Introduction to the ARM920T/940T header card* on page 1-2
- *Board layout* on page 1-3.

1.1 Introduction to the ARM920T/940T header card

The ARM920T/940T header card (HBI-0046A) is a processor daughter board for the ARM development board (HBI-0011B). It is available fitted with either an ARM920T (part number KPI 0043A) or ARM940T processor (part number KPI 0034A). This guide describes how to set up your ARM development board and ARM920T/940T header card.

The header card and development board combination provides a suitable platform for code development and evaluation of the ARM920T or the ARM940T processor.

Together with the *ARM Software Development Toolkit*, the user can download, execute and debug code. This can be with either the Multi-ICE debugging system (available separately from ARM) or the Angel debug monitor.

1.1.1 System requirements

To use the ARM920T/940T header card you will need the following:

- ARM development board (HBI-0011B)
- ARM debugger, such as:
 - Multi-ICE (recommended)
 - Angel.
- ARM Software Development Toolkit.

1.1.2 Features of the ARM920T/940T header card

The main features of the ARM920T/940T header card are:

- selectable core frequency up to 160MHz or more
- logic analyzer connectors for every signal of the ARM920T/940T
- Multi-ICE connector for debugging using the EmbeddedICE macrocell.

1.2 Board layout

Figure 1-1 shows the layout of the main components of the ARM920T/940T header card.

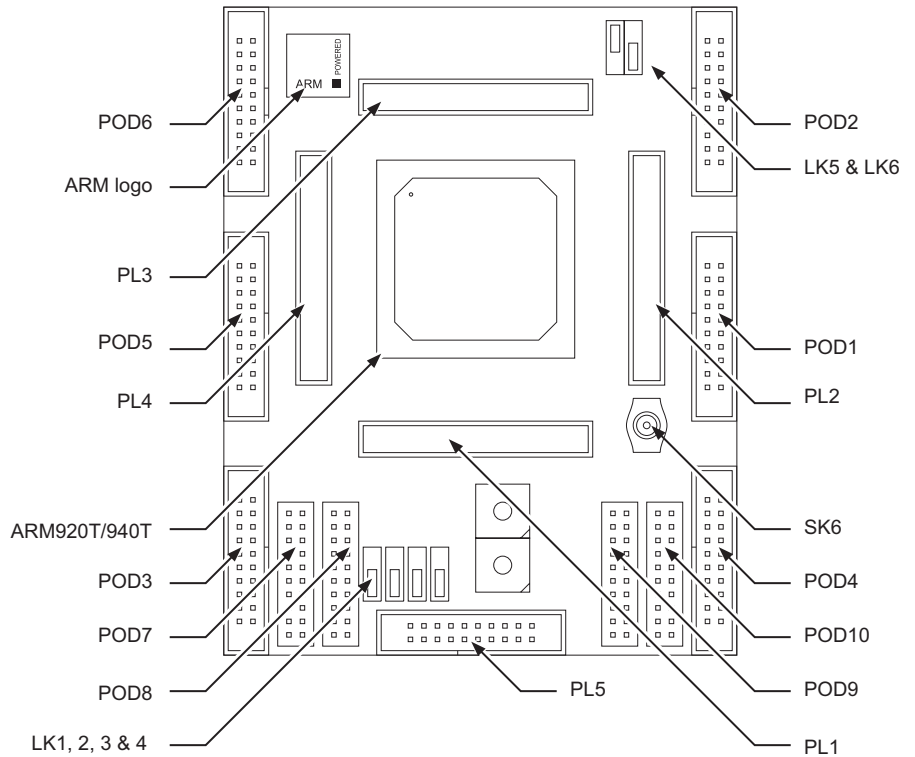


Figure 1-1 Board layout

1.2.1 Schematic diagrams

The complete set of schematic diagrams for the ARM920T/940T header card is supplied in pdf format on the accompanying disk.

Chapter 2

Setting up your System

This chapter describes how to set up your ARM development board to work with the ARM920T/940T header card and gives details of connecting debuggers. It contains the following sections:

- *Setting up your ARM development board* on page 2-2
- *Debugging using Angel* on page 2-4
- *Debugging using Multi-ICE* on page 2-5.

2.1 Setting up your ARM development board

The ARM920T/940T header card plugs into the top left hand corner of the development board, the ARM logo on the silk-screen of the card to the top left corner, so that the header is flush with the development board. The correct way to mount the header card is shown in Figure 2-1.

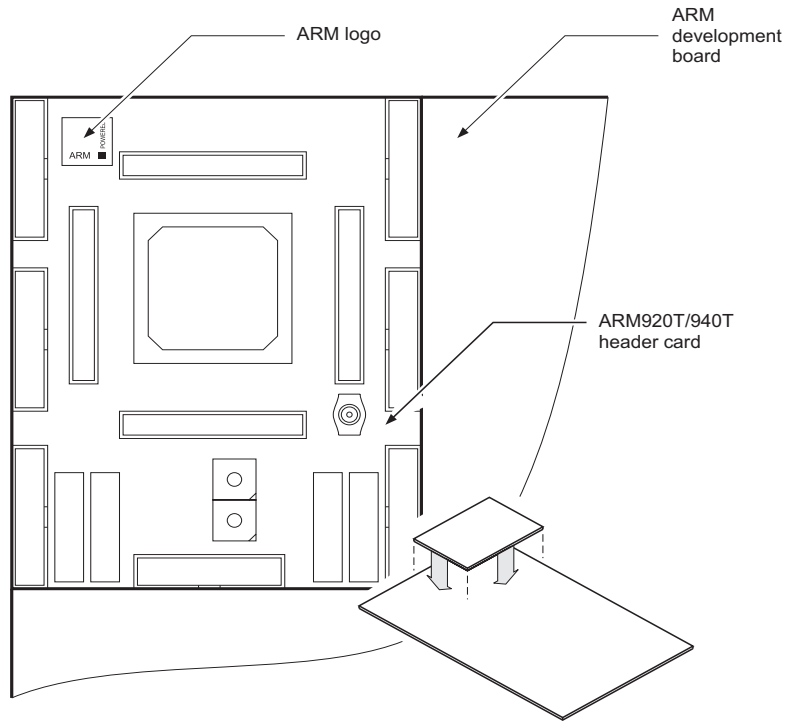


Figure 2-1 Mounting the header card

The ARM920T/940T can be debugged using one of the following:

- Multi-ICE debugging system (available separately)
- Angel debug monitor (supplied with the ARM development board).

———— **Note** ————

An EmbeddedICE unit cannot be used to debug ARM9 family processors.

2.1.1 Setting the bus clock frequency

The ARM920T/940T header card requires the bus clock frequency, **BCLK**, of the ARM development board to be set to 4, 8, 16 or 20MHz. This is set by changing the **FREQ SELECT** switch, S1, on the ARM development board, shown in Figure 2-2.

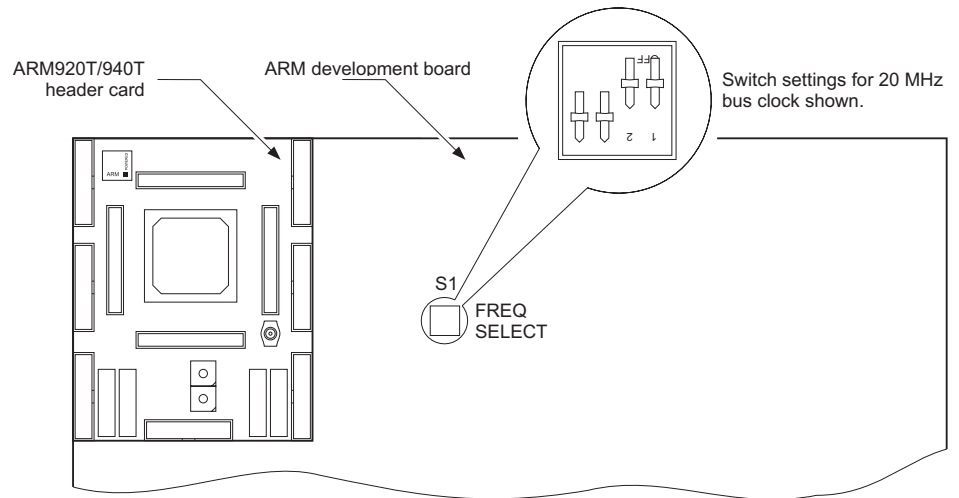


Figure 2-2 Position of switch S1

Table 2-1 shows the switch settings for the allowable bus clock frequencies.

Table 2-1 Bus clock settings

Position 4	Position 3	Position 2	Position 1	BCLK (MHz)
On	On	On	On	4
On	On	On	Off	8
On	On	Off	On	16
On	On	Off	Off	20

Note

Do not select any combination other than shown in the table.

2.2 Debugging using Angel

Angel is a program that enables rapid development and debugging of applications running on ARM-based hardware. Angel runs on the ARM development board or a development version of the product hardware alongside your application. It communicates with a debugger that can handle the Angel communications protocol, such as the *ARM Debugger for Windows*, or *armsd*. A serial/parallel or ethernet connection to the host debugging system is required.

The binary image for the Angel is supplied with the ARM development board. To download, execute and debug code the host needs to be running the *ARM Debugger for Windows* or *armsd* program supplied as part of the *ARM Software Development Toolkit*, available separately from ARM.

———— **Note** —————

If debugging with Angel is required, jumper links on the ARM development board may need to be changed. Please refer to the manual *ARM Target Development System User Guide* for details of how to establish a debug link between the board and the host system.

2.3 Debugging using Multi-ICE

The Multi-ICE debugging system provides a nonintrusive debugging system with fast download and is available separately from ARM.

The ARM920T/940T header card provides a Multi-ICE connector, PL5, which connects via a 20-way ribbon cable to the Multi-ICE hardware. The Multi-ICE server and debugger software should be run on the host computer. To download, execute and debug code the host needs to be running the *ARM Multiprocessor Debugger for Windows* software, available separately from ARM. Please refer to the *Multi-ICE Installation Guide* for installation instructions and the *Multi-ICE User Guide* for use of the Multi-ICE software.

The Multi-ICE debugging system should be set up as shown in Figure 2-3.

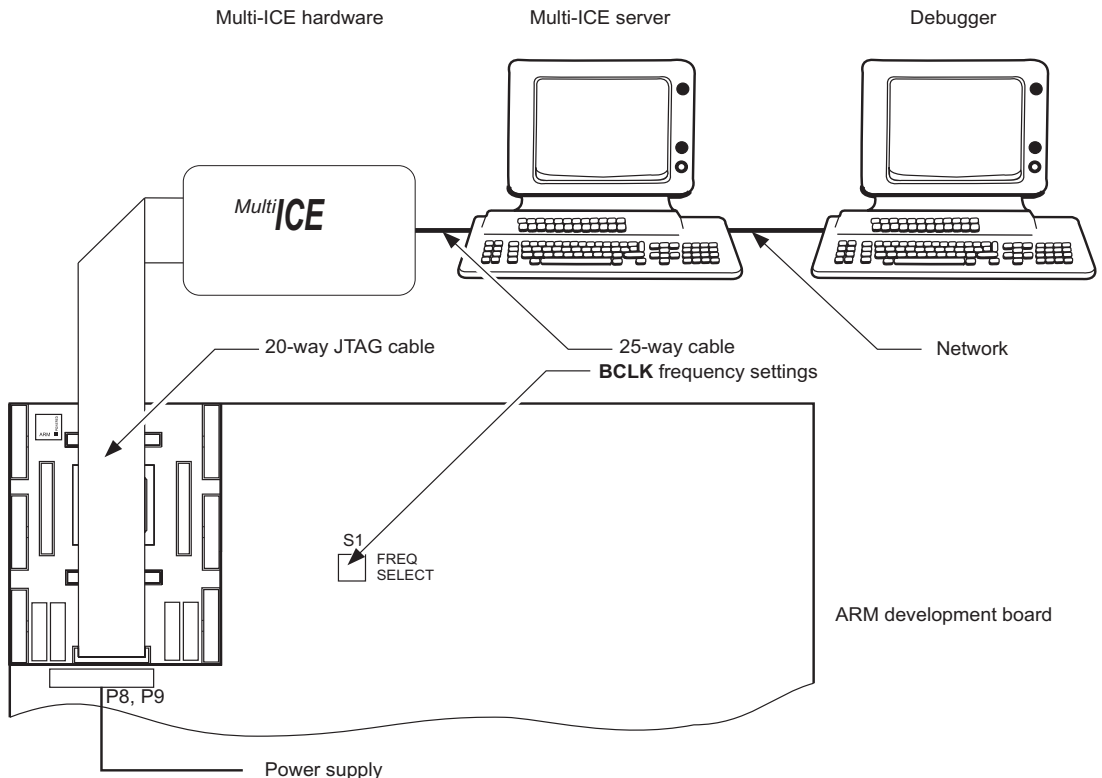


Figure 2-3 Multi-ICE debugging system

Note

Debugger and Multi-ICE server can be the same machine or two networked machines.

Chapter 3

Configuring the ARM920T/940T Header Card

This chapter describes the board link and switch settings that configure the ARM920T/940T header card. It contains the following sections:

- *Setting the core clock frequency* on page 3-2.
- *Surface mount links* on page 3-3.
- *Using the external clock input* on page 3-5
- *Setting the endianness* on page 3-6.

3.1 Setting the core clock frequency

On the ARM920T/940T header card, a phase-locked loop chip performs the core clock generation. This multiplies a reference frequency of 1MHz by a user programmable factor. The factor is eight plus the value dialled up on the rotary DIL switches (S2 and S1). See Figure 3-1.

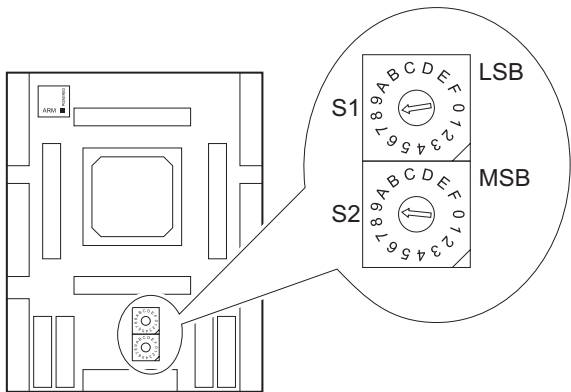


Figure 3-1 Position of switches S1 and S2

Typical settings and their corresponding frequency values are shown in Table 3-1.

Table 3-1 Typical S1 and S2 values for setting clock PLL chip

MSB(S2)	LSB(S1)	HEX VALUE	DECIMAL VALUE	Core clock frequency (MHz)
2	A	2A	42	50
5	C	5C	92	100
8	E	8E	142	150
9	8	98	152	160
C	0	C0	192	200 (see note)

Operation is guaranteed only for values from 0x04 to 0x98, which generate frequencies from 12 to 160MHz. Under typical conditions the oscillator will operate at higher frequencies such as 200MHz (0xC0) or even higher.

Note

Operation of the oscillator chip beyond 160MHz is not guaranteed.

3.2 Surface mount links

The ARM920T/940T header card has six surface mount links. These links should not be moved from their default position for normal operation.

3.2.1 Links LK1 to LK4

Links LK1 to LK4 are used to select from alternative signals that can be routed to the header card. Figure 3-2 shows the default positions of LK1, 2, 3, and 4.

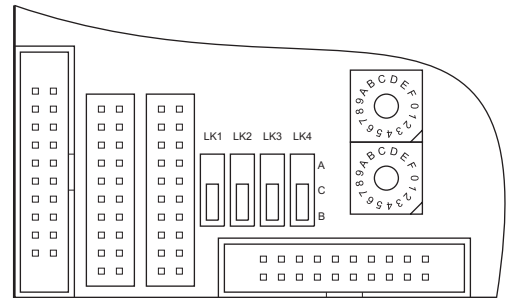


Figure 3-2 Default position of links LK1, LK2, LK3 and LK4

Table 3-2 shows the signals selected by these links in their default position.

Table 3-2 Signals selected by LK1 to LK4 in default positions

Link	Name	Default position
LK1	TESTCFG	C-B
LK2	ISYNC	C-B
LK3	TRACK	C-B
LK4	TSYNCEN	C-B

3.2.2 Links LK5 and LK6

Links LK5 and LK6 determine which **AGNT** and **AREQ** sources are used. The default position of links LK5 and LK6 (both links set to A-C) is shown in Figure 3-3. The position of these links should not be changed for normal operation.

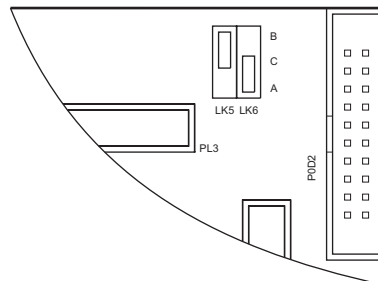


Figure 3-3 Default position of links LK5 and LK6

Table 3-3 shows the signals selected by these links in their default position.

Table 3-3 Signals selected by LK5 and LK6 in default positions

Link	Name	Default position
LK5	AGNT	A-C
LK6	AREQ	A-C

3.3 Using the external clock input

The external clock input can be configured by changing the arrangement of surface mount resistors, as shown in Table 3-4. This allows an AC-coupled input from either an RF signal generator or a standard CMOS clock generator input to drive ARM920T/940T directly or via a buffer.

Table 3-4 Clock modes to ARM920T/940T

Clock mode to ARM920T/940T	R33	R34	R35	R36	R37	R38
On board PLL source (default)	33Ω	33Ω	omit	omit	33Ω	omit
RF signal generator via a buffer	omit	omit	omit	33Ω	33Ω	33Ω
RF signal generator direct to ARM920T/940T	omit	omit	0Ω	omit	omit	33Ω

The positions of resistors R33 to R38, and the external clock input (SK6) are shown in Figure 3-4.

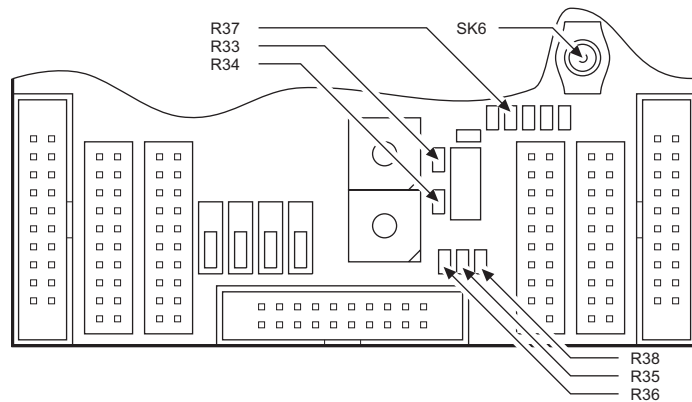


Figure 3-4 Position of resistors R33 to R38 and external clock input

The input impedance of SK6 is 50-ohms. See *External clock input* on page 4-4 for details of how to change the input impedance to match sources other than 50-ohms.

3.4 Setting the endianness

The ARM920T/940T header card can be configured for either little-endian or big-endian operation. The factory setting is for little-endian operation.

3.4.1 Little-endian memory system

To configure the ARM920T/940T header card for little-endian operation:

1. Remove BIGEND link (LK4) on the ARM development board.
2. Reset the ARM920T/940T. It automatically assumes a little-endian memory system, so no software configuration is required.

3.4.2 Big-endian memory system

To configure the ARM920T/940T header card for big-endian operation:

1. Fit BIGEND link (LK4) on the ARM development board.
2. Reset the ARM920T/940T. It automatically assumes a little-endian memory system.
3. Change the ARM920T/940T to BIGEND mode by setting bit 7 of coprocessor 15 register 1, see Example 3-1.

———— **Note** —————

Any byte accesses before this bit is set will be little-endian so will not access the expected data.

Example 3-1 Setting the ARM920T/940T into BIGEND mode

```
MRC p15,0,r0,c1,0 ; read coprocessor 15 register 1
ORR r0,r0,#0x80   ; set bit 7
MCR p15,0,r0,c1,0 ; write coprocessor 15 register 1
```

Chapter 4

Circuit Descriptions

This chapter describes the operation of the ARM920T/940T header card. It contains the following sections:

- *The header card circuit board* on page 4-2
- *Power measurements* on page 4-9.

4.1 The header card circuit board

The header card is an 8-layer board and consists of:

- the ARM920T/940T processor
- a *phase-locked loop* (PLL) clock-generation chip and buffer
- external clock input
- connectors for a logic analyzer and a Multi-ICE connector.

4.1.1 Processor in BGA

The ARM920T/940T processor is supplied in a 388-pin ball grid array package, a number of inputs are tied to default values through resistors. These are listed in Table 4-1.

Table 4-1 Values of tied inputs

ARM920T signal names	ARM940T signal names	Value
CHSDE0	CHSDE0	LOW
CHSDE1	CHSDE1	HIGH
CHSEX0	CHSEX0	LOW
CHSEX1	CHSEX1	HIGH
CPDIN[31:0]	CPDIN[31:0]	LOW
SELSCANOUT0	DABORT	LOW
DBGEN	DBGEN	HIGH
DEWPT	DEWPT	LOW
DSEL	DSEL	LOW
EBE	EBE	HIGH
EDBGRQ	EDBGRQ	LOW
EDBGRQ	EDBGRQ	LOW
EXTERN0	EXTERN0	LOW
EXTERN1	EXTERN1	LOW
No connection	GCLK	LOW
SELSCANOUT1	IABE	HIGH

Table 4-1 Values of tied inputs (continued)

ARM920T signal names	ARM940T signal names	Value
IEKPT	IEKPT	LOW
RINGOSCEN	No connection	LOW
TEST	No connection	LOW
SDOUTBS	nRESET	LOW
nTRST	nTRST	HIGH
TBE	TBE	HIGH
TCK	TCK	HIGH
TDI	TDI	HIGH
TMS	TMS	HIGH
TRACK	TRACK	LOW

4.1.2 Clock generation

A PLL chip (U2, ICS525) generates the high speed clock, **FCLK**, which is used to clock the core of ARM920T/940T.

The two rotary DIL switches (S1 and S2) can be used to set the core clock, **FCLK**, frequency, as shown in Table 2-1 on page 2-3.

The ICS525 requires 5 volts to operate which is taken from the ARM development board and passes through a ferrite bead. The purpose of the ferrite bead is to filter out any parasitic noise from the supply.

Before applying the clock to the ARM920T/940T it is converted to a 3.3V level signal by a 5V tolerant high-speed inverting buffer (U3, 74LCX04).

Two buffers are used to split the output of **FCLK** to the header connectors and **FCLK** to the ARM920T/940T. The resistors R33-R38 provide series termination on the outputs of the buffer chip.

4.1.3 External clock input

The ARM920T/940T header card has a 50-ohm mini-coaxial connector socket (SK6) to allow the use of an external clock signal from an external clock generator. This is usually only required if the operating frequency is greater than 160MHz or less than 12MHz.

The ARM920T/940T header card clock input is terminated in a 50-ohm load impedance on the board, depending on the link settings shown in Table 3-4 on page 3-5, to match the external clock source impedance. Resistors R30 and R40 can be changed, if required, to allow proper termination of a clock frequency source of other than 50-ohms output impedance.

4.2 Connectors

The ARM920T/940T header card has five 60-way sockets (SK1-5) mounted on the underneath. Four of these correspond to the four 60-way plug connectors (PL1-PL4) on the development card, which allow the header card to be fitted to the development board. The fifth socket carries the extra coprocessor signals. These are not connected to the ARM development board, but can be connected to the ARM logic expansion card if required. For further details see Section 2.1 of the *Logic Expansion Card User Guide*.

4.2.1 Logic analyzer connectors

Six 20-way box headers, POD1 to 6, are provided to allow connection of Hewlett Packard 20-pin (HP 01650-63203) pods suitable for use with a HP1600 or 16500-series logic analyzer and thus trace the ARM920T/940T activity. These connectors can also be used for expansion purposes and give access to coprocessor buses, **CPID[31:0]**, **CPDOUT[31:0]** and **CPDIN[31:0]**. The pinout of connectors POD1 to 6 is given in Figure 4-1 on page 4-6.

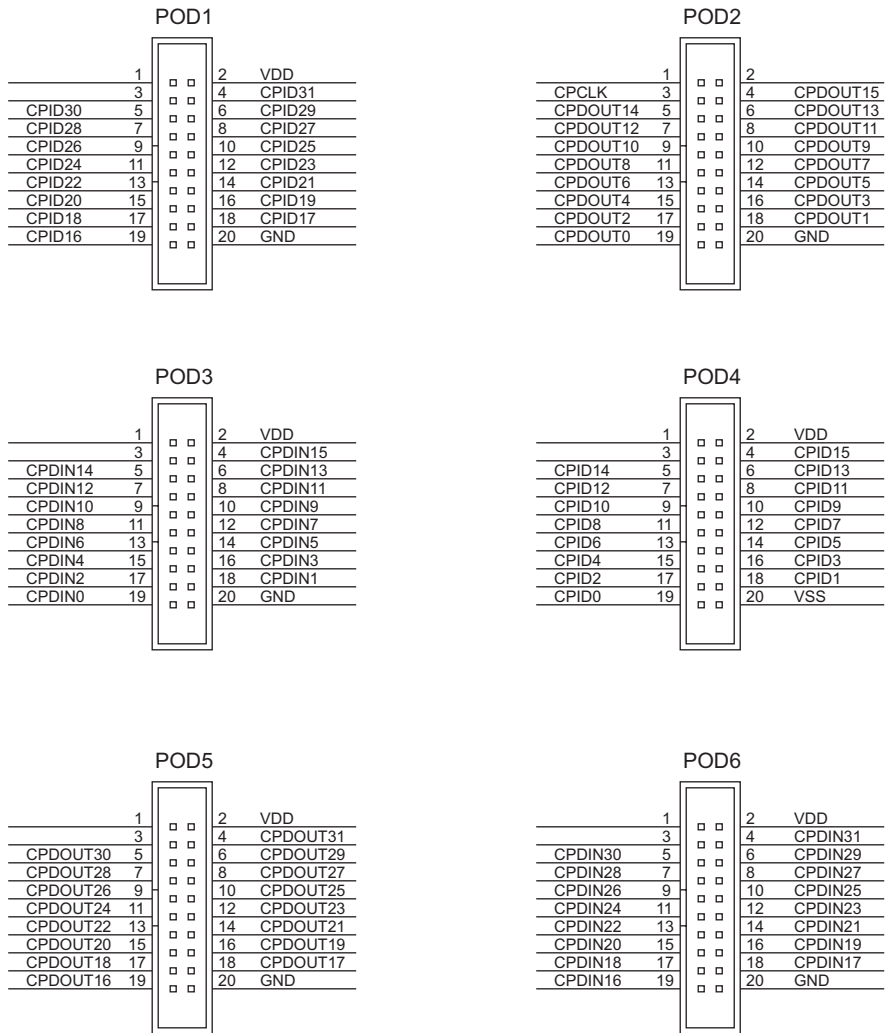


Figure 4-1 Boxed header pinouts

Four more 20-way header connectors (without a box), POD7-10, allow other clock and status ARM920T/940T signals to be monitored. The pinout of connectors POD7-10 is given in Figure 4-2.

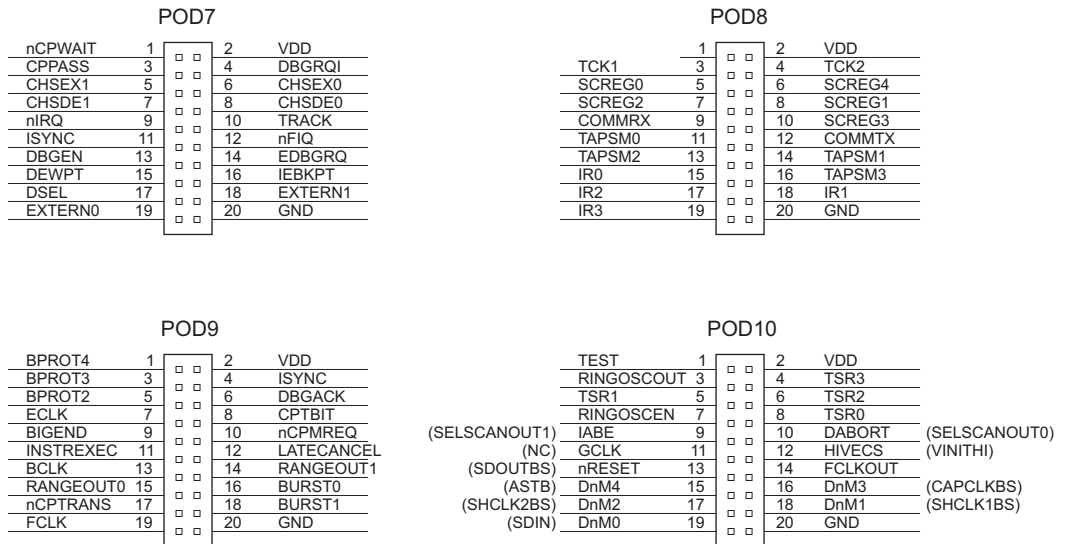


Figure 4-2 Unboxed header pinouts

4.2.2 Multi-ICE connector

A 20-way connector, PL5, allows debugging of the ARM920T/940T using Multi-ICE. The position of PL5 is shown in Figure 1-1 on page 1-3.

The Multi-ICE connector has the standard five JTAG signals, **nTRST**, **TDI**, **TMS**, **TCK** and **TDO**, which are interspersed with ground pins to reduce noise. The pinout for PL5 is shown in Figure 4-3.

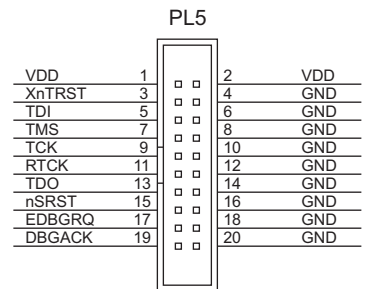


Figure 4-3 PL5 pinout

The signal **RTCK** (returned **TCK**), is connected to **TCK** on the header card, to allow the Multi-ICE to make use of the *adaptive clock timing* option for debugging TrackingICE targets. See *Application Note 41: TrackingICE* for information about TrackingICE.

The signal **nSRST** can be used by the Multi-ICE unit to reset the ARM920T/940T header card and the ARM development board.

The **DBGRQ** and **DBGACK** signals are not used by Multi-ICE.

4.3 Power measurements

The header card has a wire link jumper, WL1, which can be removed to allow the current consumption of the core to be measured. Figure 4-4 shows the location of wire link WL1.

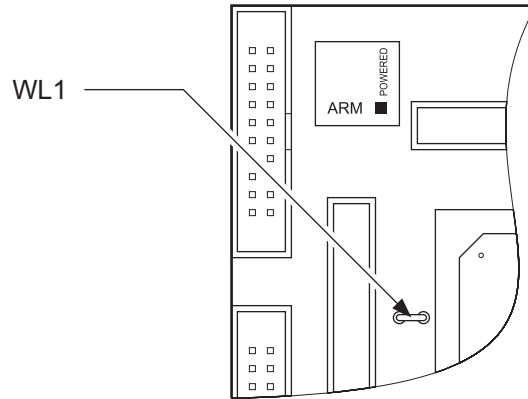


Figure 4-4 Position of WL1

Removal of the link allows an external power supply to be introduced, permitting a variable voltage source to be used to set the required core voltage (VDD).

It is not recommended to measure core current using an in-line ammeter because of losses due to lead impedances. However, if a low-value resistor (for example 10 Ω) is fitted as shown in Figure 4-5, the core current can be found more accurately by measuring the voltage across the resistor and then calculating the current through it, and so the power.

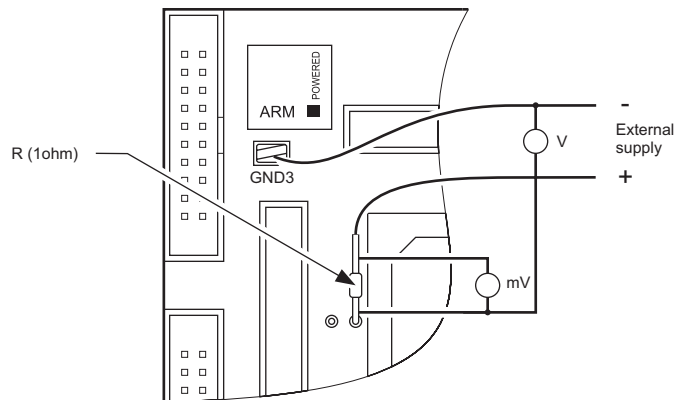


Figure 4-5 Setup for core power consumption measurement

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