ARM Integrator/AM

User Guide

ARM

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ARM Integrator/AM
User Guide

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This document is Open Access. This means there is no restriction on the distribution of the information.

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Contents
ARM Integrator/AM User Guide

Preface

This preface introduces the ARM Integrator/AM Analyzer Module and its reference documentation. It contains the following sections:

About this document

This document describes how to set up and use the ARM Integrator/AM.

Intended audience

This document is intended for software and hardware engineers developing ARM-based products with the Integrator system. It assumes that you are familiar with operation of the Integrator system, including motherboards, core module, and logic modules.

Using this manual

This document is organized into the following chapters:

Chapter 1 *Introduction*

Read this chapter for an introduction to the Integrator/AM.

Chapter 2 *Getting Started*

Read this chapter for information about installing the Integrator/AM and how to start using it.

Chapter 3 *Using the Integrator/AM*

Read this chapter for information about connecting a logic analyzer, using the EPROM socket, the hexadecimal switch, and the LED array.

Typographical conventions

The following typographical conventions are used in this document:

bold Highlights ARM processor signal names, and interface elements such as menu names. Also used for terms in descriptive lists, where appropriate.

italic Highlights special terminology, cross-references and citations.

`typewriter` Denotes text that may be entered at the keyboard, such as commands, file names and program names, and source code.

`type`writer Denotes a permitted abbreviation for a command or option. The underlined text may be entered instead of the full command or option name.

`typewriter italic`
Denotes arguments to commands or functions where the argument is to be replaced by a specific value.

`typewriter bold`
Denotes language keywords when used outside example code.

Further reading

This section lists publications by ARM Limited, and by third parties.

ARM periodically provides updates and corrections to its documentation. See `http://www.arm.com` for current errata sheets and addenda.

See also the ARM Frequently Asked Questions list at:
`http://www.arm.com/DevSupp/Sales+Support/faq.html`

ARM publications

This document contains information that is specific to the ARM Integrator/AM. Refer to the following documents for information about related ARM products and toolkits:

- *ARM Integrator/AP User Guide* (ARM DUI 0098)
- *ARM Integrator/SP User Guide* (ARM DUI 0099)
- *ARM Multi-ICE User Guide* (ARM DUI 0048)
- *AMBA Specification* (ARM IHI 0011)
- *ARM Architectural Reference Manual* (ARM DDI 0100)
- *ARM Firmware Suite Reference Guide* (ARM DUI 0102)
- *ARM Software Development Toolkit User Guide* (ARM DUI 0040)
- *ARM Software Development Toolkit Reference Guide* (ARM DUI 0041)
- *ADS Tools Guide* (ARM DUI 0067)
- *ADS Debuggers Guide* (ARM DUI 0066)
- *ADS Debug Target Guide* (ARM DUI 0058)
- *ADS Developer Guide* (ARM DUI 0056)
- *ADS CodeWarrior IDE Guid*e (ARM DUI 0065).

Feedback

ARM Limited welcomes feedback both on the ARM Integrator/AM, and on the documentation.

Feedback on the ARM Integrator/AM

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- a concise explanation of your comments.

Feedback on this document

If you have any comments about this document, please send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- a concise explanation of your comments.

General suggestions for additions and improvements are also welcome.

Chapter 1
Introduction

This chapter introduces the ARM Integrator/AM. It contains the following sections:

1.1 About the ARM Integrator/AM

The ARM Integrator/AM (*Analyzer Module*) gives you access to the Integrator system buses and allows you to fit an EPROM or EPROM emulator. When multiple modules are stacked on a motherboard the analyzer module is always placed at the top.

An Integrator system typically employs two buses:

- a local memory bus on the core module
- a system bus which interconnects core and logic modules with the motherboard.

The two buses are independent and can conform to different standards. For example, a CM740T uses an ASB-based local memory bus, but might have an AHB system bus. Some core modules have logic analyzer connection points to allow the memory bus to be monitored.

The logic analyzer connection points are AMP Mictor connectors (AMP 2-767004-2), which are specified by both Agilent and Tektronix as suitable for connection to a range of analyzers.

Figure 1-1 on page 1-3 shows the layout of the Integrator/AM. Sockets for the HDRA/EXPA, HDRB/EXPB, and EXPM connectors on the motherboard and other Integrator modules are mounted on the underside of the board. All other components are mounted on the top, allowing you to connect flying leads and test equipment.

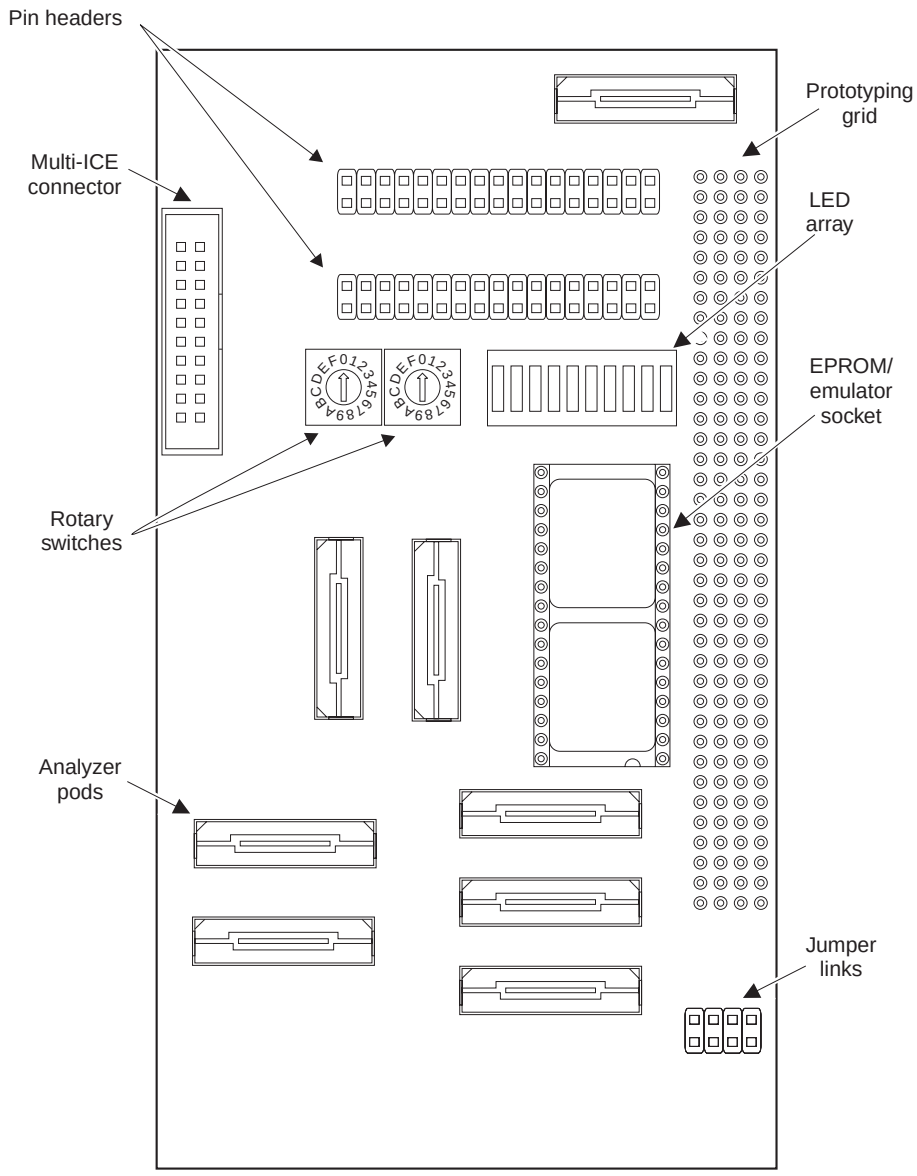

Figure 1-1 Integrator/AP outline

1.2 Analyzer layout

The analyzer module provides the following features:

- system bus and expansion connectors
- eight Mictor connectors
- test points
- two 34-pin headers
- two rotary hexadecimal switches
- LED array
- EPROM socket
- Multi-ICE connector
- prototyping grid.

The system bus and expansion bus connectors are fitted on the underside of the analyzer module. This allows you to mount the analyzer module on a core module stack (HDRA and HDRB) or the logic module stack (EXPA and EXPB).

When the analyzer module is placed on the logic module stack (EXPA and EXPB) the 32-bit GPIO lines from the system controller are connected to two 34-pin headers on the module. This allows you to connect external equipment and to connect the GPIO lines to the LEDs and rotary switches. A small prototyping grid allows you to connect GPIO to external equipment.

A 32-pin DIL socket enables you to fit an 8-bit EPROM or emulator. The external chip-select 0 line (**nXCS0**) selects the device. When enabled, this allows a motherboard to boot from the EPROM rather than the boot ROM on the motherboard.

Note

The motherboard FPGA configuration is always loaded from the boot ROM. This mechanism allows the board to run an alternative program to the boot monitor, without overwriting the standard ROM. It also provides a debugging route for those who prefer to use an emulator rather than JTAG debugging or a debug monitor.

Chapter 2
Getting Started

This chapter describes how to prepare to use the ARM Integrator/AM. It contains the following sections:

2.1 Connecting the analyzer module to a core or logic module

The analyzer module connects on top of a core or logic module to monitor the bus signals carried between the modules and the motherboard on which they are mounted.

2.1.1 Using the analyzer module with an Integrator/AP

On an Integrator/AP, you can fit the AM in two positions:

- on the HDRA/HRDB connectors
- on the EXPA/EXPB connectors.

Mounting the analyzer module on the HDRA/HDRB connectors

Mounting the AM on the HDRA/HDRB connectors on top of a core module leaves the EXPA/EXPB connectors free for a logic module:

Advantage You can accurately monitor of the signals on the HDRA and HDRB connectors.

Disadvantage The top of the core module is covered.

Figure 2-1 on page 2-3 shows a analyzer module mounted on the HDRA/HDRB connectors and a logic module mounted on the EXPA/EXPB connectors.

Mounting the analyzer module on the EXPA/EXPB connectors

Mounting the analyzer module directly on the EXPA/EXPB connectors allows access to the core module:

Advantage This allows you to trace the EXPA, EXPB, and EXPM connectors and also allows access to the core module at the top of the HDRA/HDRB stack.

Disadvantage There are differences between the signals on the HDRB and EXPB connectors, particularly the arbitration and interrupts signals. This means that these signals cannot be monitored correctly (see *Differences between HDRB and EXPB* on page 2-10).

Figure 2-2 on page 2-4 shows an analyzer module mounted on the EXPA/EXPB connectors and a logic module mounted on the HDRA/HDRB connectors.

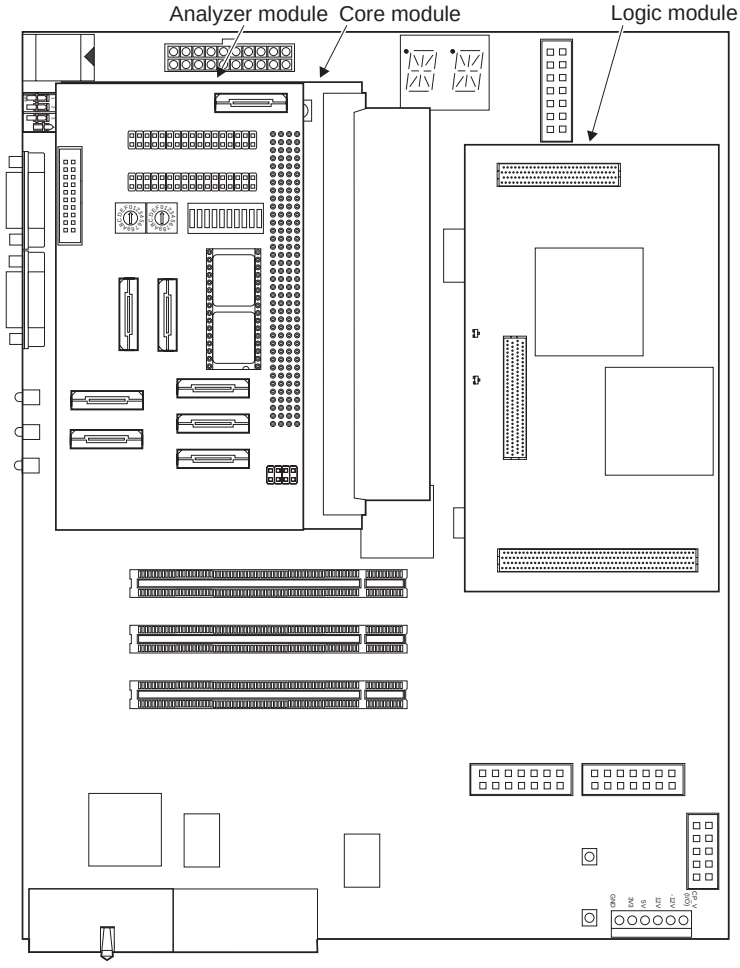

Figure 2-1 The analyzer module mounted on the HRDA/HDRB stack

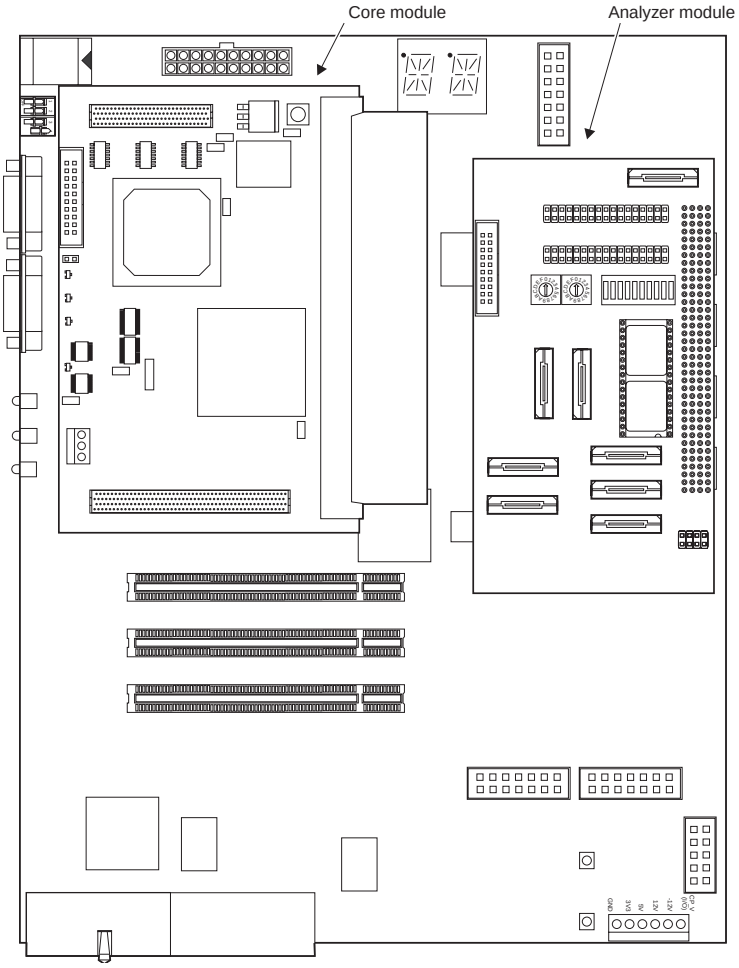

Figure 2-2 The analyzer module mounted on the EXPA/EXPB stack

2.1.2 Using the AM with an Integrator/SP

You acn use the analyzer module with an Integrator/SP motherboard. The SP provides only one stack position. This means that you install the AM on top of a core module.

2.1.3 Signal rotations

A number of signals on the HDRB and EXPB connector rotate in groups of four as they ascend the stack. The schematics for each of the core and logic modules are labeled as if they are the only module in a stack. This means, for example, that the signal labeled **nIRQ0** on a core module appears in position **nIRQ3** when it is monitored on the analyzer module. Rotation applies to the following groups of signals:

- **SREQ[3:0]**
- **SGNT[3:0]**
- **SLOCK[3:0]**
- **ID[3:0]**
- **nFIQ[3:0]**
- **nIRQ[3:0]**
- **nPPRES[3:0]**
- **nEPRES[3:0]**
- **SYSCLK[3:0]**

2.2 Connectors

Table 2-1 describes the function of each of the connectors.

Table 2-1 Connector summary

Reference	Label	Type	Name	Notes
POD2	ADDR	Mictor	System bus address	ASB – **BA[31:0]** AHB – **HADDR[31:0]**
POD4	DATA	Mictor	System bus data	ASB – **BD[31:0]** AHB – **HDATA[31:0]**
POD6	CONTROL1	Mictor	System bus control	AMBA control signals
POD7	BUSB	Mictor	System bus B	Not used on standard systems, reserved for expansion
POD5	CONTROL2	Mictor	System bus control	Arbitration, interrupt, and miscellaneous signals
POD8	GPIO/BUSF	Mictor	System bus F/GPIO	Not used on standard systems, reserved for expansion
POD1	MADDR	Mictor	Memory bus address and control	*External Bus Interface* (EBI) address and control signals from the static memory controller
POD3	MDATA	Mictor	Memory bus data	*External Bus Interface* (EBI) data signals from the static memory controller
J1	-	34-way 0.1 inch header	**GPIO[15:0]**	Allows external equipment to be connected to GPIO, or link pins to connect switches and LEDs
J5	-	34-way 0.1 inch header	**GPIO[31:16]**	Allows external equipment to be connected to GPIO, or link pins to pull down for configuration options
J6	EPROM	32-pin DIL socket	Memory bus	Allows EPROM or emulator to be fitted
J7	JTAG	20-way 0.1 inch box header	JTAG equipment	Connection for Multi-ICE when the module is in a stack
J2	HDRA/EXPA	200-way socket	-	Connects to motherboard

Table 2-1 Connector summary (continued)

Reference	Label	Type	Name	Notes
J3	HDRB/EXPB	120-way socket	-	Connects to motherboard
J4	EXPM	120-way socket	-	Connects to motherboard
J8	-	-	-	See Table 2-3 on page 2-9.

2.3 Test points, vias, and links

Test points are provided on all power supplies as follows:

- **+3V3**
- **+5V**
- **+12V**
- **–12V**
- **FLVPP** (flash VPP).

There are also four ground points for securing an oscilloscope ground lead and two signal test points, **nFLWP** (flash write protect) and **nSYSRST** (system reset). Other signals are brought out to vias so that you can add wires if necessary. Table 2-2 lists the test points and vias.

Table 2-2 Test points and vias

Reference	Label	Source	Type	Notes
TP1	5V	Motherboard	Test point	Monitoring point for power supply
TP2	3V3	Motherboard	Test point	Monitoring point for power supply
TP3	-12V	Motherboard	Test point	Monitoring point for power supply
TP4	+12V	Motherboard	Test point	Monitoring point for power supply
TP5	**nFLWP**	Motherboard	Test point	Monitoring point for flash write protect signal
TP6	**FLVPP**	Motherboard	Test point	Monitoring point for flash programming voltage
TP7	**nSYSRST**	Motherboard	Test point	Connect to EPROM emulator when supported so that the emulation software can detect board resets
V1	-	**nMADV**	Via	Memory bus advance (for synchronous memory)
V2	-	CONTROL2	Via	Clock input (**ACLK**) to logic analyzer

Table 2-2 Test points and vias (continued)

Reference	Label	Source	Type	Notes
V3	-	CONTROL2	Via	Clock input (**BCLK**) to logic analyzer
V4	-	BUSB	Via	Clock input (**BCLK**) to logic analyzer
V5	-	BUSB	Via	Clock input (**ACLK**) to logic analyzer
V6	-	BUSB	Via	Signal input (**A15**) to logic analyzer
V7	-	HDRB/EXPB	Via	**SYSCLK** signal

Table 2-3 lists the links at J8. The default for each link is NOT fitted.

Caution

Refer to the motherboard and core module documentation for descriptions of the function of these links. Inserting links can prevent the motherboard from functioning correctly.

Table 2-3 Links

Label	Source	Function
MCSOEN	EXPM	Chip select 0 enable, insert link to enable EPROM emulator socket. **nXCS0** is be used instead of **nMCS0**.
MRDY	EXPM	Memory ready, insert link or drive LOW to add wait states to external bus interface.
EBIEN	EXPM	EBI enable, insert link to prevent the external bus interface driving static memories.
nCFGEN	JTAG	Configuration enable, insert link to enable JTAG programming of FPGAs/PLDs on motherboard and modules.

2.4 Differences between HDRB and EXPB

This section provides information about the differences between some signals on the HDRB and EXPB connectors. There are three gorups of signals that are affected:

- *Interrupts*
- *Arbitration signals SREQ, SGNT, and SLOCK* on page 2-11
- *GPIO signals* on page 2-11.

2.4.1 Interrupts

In general, core modules receive interrupts but logic modules, which implement peripherals, generate interrupts.

The signals on HDRB and EXPB concerned with interrupts are different, as shown in Table 2-4. All signals on these pins are driven open-collector (open-drain) so that there is no conflict when logic and core modules are connected together.

Table 2-4 Interrupt pins on HDRB and EXPB

EXPB			HDRB		
Signal	**Label**	**Description**	**Signal**	**Label**	**Description**
nFIQ0	H16	Fast interrupt to module 0	-	E16	Not used
nFIQ1	H17	Fast interrupt to module 1	-	E17	Not used
nFIQ2	H18	Fast interrupt to module 2	-	E18	Not used
nFIQ3	H19	Fast interrupt to module 3	-	E19	Not used
nIRQ0	H20	Interrupt to module 0	**IRQSRC0**	E20	Interrupt source from module 0 to interrupt controller
nIRQ1	H21	Interrupt to module 1	**IRQSRC1**	E21	Interrupt source from module 1 to interrupt controller
nIRQ2	H22	Interrupt to module 2	**IRQSRC2**	E22	Interrupt source from module 2 to interrupt controller
nIRQ3	H23	Interrupt to module 3	**IRQSRC3**	E23	Interrupt source from module 3 to interrupt controller

2.4.2 Arbitration signals SREQ, SGNT, and SLOCK

The Integrator arbiter on the motherboard supports up to six system bus masters, including the internal PCI master on the motherboard itself. The arbiter signals are routed so that they are shared across the two module stacks. The signals on HDRB and EXPB concerned with arbitration are shown in Table 2-5.

Table 2-5 Arbitration pins on HDRB and EXPB

HDRB		EXPB		Description
Signal	**Label**	**Signal**	**Label**	
SREQ0	E0	**SREQ4**	H0	System bus request
SREQ1	E1	**SREQ3**	H1	
SREQ2	E2	**SREQ2**	H2	
SREQ3	E3	**SREQ1**	H3	
SGNT0	E4	**SGNT4**	H4	System bus grant
SGNT1	E5	**SGNT3**	H5	
SGNT2	E6	**SGNT2**	H6	
SGNT3	E7	**SGNT1**	H7	
SLOCK0	E8	**SLOCK4**	H8	System bus lock (AHB only)
SLOCK1	E9	**SLOCK3**	H9	
SLOCK2	E10	**SLOCK2**	H10	
SLOCK3	E11	**SLOCK1**	H11	

2.4.3 GPIO signals

On the Integrator/AP motherboard, the 32 GPIO signals are routed to the EXPB connector, but not the HDRB connector. The GPIO signals are not available on the Integrator/SP motherboard.

2.5 Connecting Multi-ICE

The Multi-ICE unit is connected to the analyzer module, when in use, using the standard 20-way box header. Refer to the *Multi-ICE User Guide* for full details about how to use Multi-ICE.

Chapter 3
Using the Integrator/AM

This chapter describes how to use the ARM Integrator/AM. It contains the following sections:

3.1 Mictor connectors

Connect your logic analyzer to the Integrator/AM using the high-density AMP Mictor connectors. Each one of these connectors carries up to 32 signals and 2 clocks (or qualifiers for Tektronix). Figure 3-1 shows the connector and identification of pin 1.

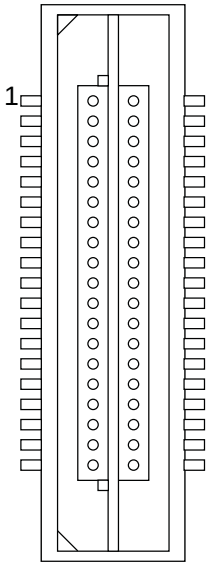

Figure 3-1 AMP Mictor connector

Note

Agilent and Tektronix label these connectors differently, but the assignments of signals to physical pins is appropriate for both systems and pin 1 is always in the same place. The schematic is labeled according to the Agilent pin assignment.

The signals are arranged to allow you to analyze the AMBA bus (ASB or AHB) using the three Mictor connectors, ADDR, DATA, and CONTROL1. A fourth connector, CONTROL2, gives you access to additional arbitration information and interrupt signals.

When monitoring multi-bus master systems, the fourth connector is required to identify which bus master is currently granted. You can determine this by monitoring the **MASTER[2:0]** signals. These identify the current bus master. However, the current master might not be the one that is granted, because the grant signal (**SGNT**, which is **AGNT** for ASB, **HGRANT** for AHB) might be asserted before the present transaction has completed.

3.2 Using an Agilent logic analyzer

You need the following Agilent component to use an Agilent logic analyzer with the Integrator/AM:

- Agilent E5346A High-Density Termination Adapter
- Agilent E5351A High-Density Adapter
- Agilent E5346-44701 Support Shroud
- Agilent E5346-60002 High-Speed Mictor Adapter
- Agilent E5346-63201 Right-Angle Adapter.

Agilent label the Mictor connector (AMP 2-767004-2) as shown in Table 3-1.

Table 3-1 Agilent Mictor connector labeling

Channel	Pin	Pin	Channel
+5V DC	1	2	No connect
GND	3	4	No connect
LCLK	5	6	**HCLK**
D15 EVEN	7	8	D15 ODD
D14 EVEN	9	10	D14 ODD
D13 EVEN	11	12	D13 ODD
D12 EVEN	13	14	D12 ODD
D11 EVEN	15	16	D11 ODD
D10 EVEN	17	18	D10 ODD
D9 EVEN	19	20	D9 ODD
D8 EVEN	21	22	D8 ODD
D7 EVEN	23	24	D7 ODD
D6 EVEN	25	26	D6 ODD
D5 EVEN	27	28	D5 ODD
D4 EVEN	29	30	D4 ODD
D3 EVEN	31	32	D3 ODD
D2 EVEN	33	34	D2 ODD
D1 EVEN	35	36	D1 ODD
D0 EVEN	37	38	D0 ODD

Refer to your Agilent representative for details of support for ARM.

3.2.1 Inverse assembler

The signals are been assigned so that you can use the Agilent Inverse Assembler for ARM. An ASB version of the inverse assembler is available. When using the inverse assembler, configure the tool to mask the following signals because they are not present on the Integrator/AM:

- **DMA**
- **nEXEC**
- **DBGACK**

3.3 Using a Tektronix logic analyzer

You need the following Tektronix component to use a Tektronixlogic analyzer with the Integrator/AM:

- 070-9793-01 P6434 Mass Termination Adapter
- 105-1088-00 Edge (Straddle) Mount P6434 Latch
- 105-1089-00 Surface Mount P6434 Latch.

Tektronix label the Mictor connector (AMP 2-767004-2) as shown in Table 3-2.

Table 3-2 Tektronix Mictor connector labeling

Channel	Pin	Pin	Channel
No connect	1	38	No connect
No connect	2	37	No connect
CLK/QUAL	3	36	**CLK/QUAL**
D3:7	4	35	D1:7
D3:6	5	34	D1:6
D3:5	6	33	D1:5
D3:4	7	32	D1:4
D3:3	8	31	D1:3
D3:2	9	30	D1:2
D3:1	10	29	D1:1
D3:0	11	28	D1:0
D2:7	12	27	D0:7
D2:6	13	26	D0:6
D2:5	14	25	D0:5
D2:4	15	24	D0:4
D2:3	16	23	D0:3
D2:2	17	22	D0:2
D2:1	18	21	D0:1
D2:0	19	20	D0:0

Refer to your Tektronix representative for details of ARM support.

3.4 Using the EPROM socket

The pinout for the EPROM socket follows the JEDEC standard for 32-pin devices. Both the VCC and VPP pins connect to **3V3**. Ensure that the EPROM or emulator operates at this voltage.

Caution

If an emulator does not draw power from the target board, then you must ensure that it does not drive signals greater than 3.3V, otherwise components on the motherboard could be damaged. The FPGA is 5V tolerant but the other memory devices might not be.

To use the EPROM socket fit a jumper to J8 in the MCS0EN position. This disables the boot ROM on the motherboard. The EPROM is connected to **nXCS0**, which is enabled when **MCS0EN** is LOW. Accesses to addresses in the range `0x20000000` to `0x23FFFFFF` select the EPROM during normal operation. At boot time this device is located at `0x00000000` if the motherboard DIL switch 1 is in the ON position.

3.5 Using the LEDs and rotary switches

You can connect the two rotary switches (S1) and LED array to GPIO signals by inserting jumpers between pins of J1, as shown in Figure 3-2.

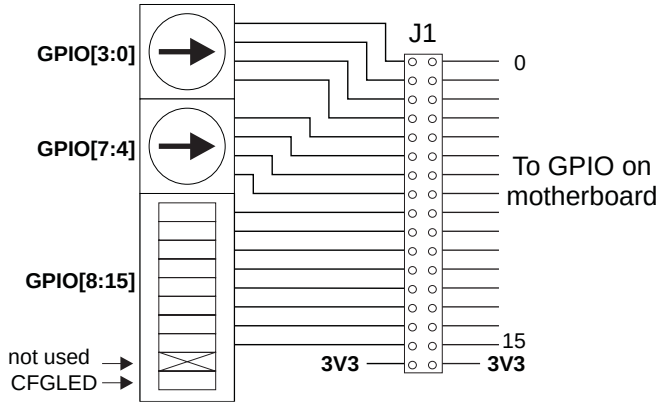

Figure 3-2 GPIO connections to rotary switches and LEDs

Appendix A
Mictor connector pinouts

This appendix provides pinouts for the Mictor connectors. It contains the following sections:

A.1 System bus

The system bus can be ASB or AHB. The system clock (**SYSCLK**) is **BCLK** on ASB and **HCLK** on AHB. The system reset (**nSYSRST**) is **BnRES** on ASB and **HRESETn** on AHB.

POD2 pin 5 (C1) is **BTRAN1** on ASB and **HTRANS1** on AHB. You can use this pin to qualify addresses on active cycles.

POD4 pin 5 (C12) is **BWAIT** on ASB and **HREADY** on AHB. You can use this pin to qualify data transfers. **A[31:0]** is **BA[31:0]** for ASB and **HADDR[31:0]** for AHB. **D[31:0]** is **BD[31:0]** for ASB and **HDATA[31:0]** for AHB.

Note

For full details of ASB and AHB, including signal encoding, refer to the *AMBA Specification*.

A.1.1 Capturing ASB system bus signals

To correctly capture ASB transactions in state mode, the system bus signals should be sampled on different edges of the system clock (**BCLK**).

ADDR (POD2) and CONTROL1-EVEN (POD6) should be captured on the rising edge of **BCLK**.

DATA (POD4) and CONTROL1-ODD (POD6) should be captured on the falling edge of **BCLK**. When using an Agilent logic analyzer, set up **BCLK** rising as the master clock and **BCLK** falling as the slave clock. This arrangement is compatible with all ASB systems and previous ARM development boards.

The Integrator ASB implementation ensures that **BTRAN[1:0]**, **BLOK**, **BWRITE**, **BSIZE[1:0]**, **BPROT[1:0]** and **BA[31:0]** are always valid on both the rising and falling However, **BWAIT**, **BERROR** and **BLAST** are only valid about the rising edge of **BCLK**.

A.1.2 Capturing AHB system bus signals

To correctly capture AHB transactions in state mode, all system bus signals should be sampled on the rising edge of the system clock (**HCLK**).

Table A-1 shows the pinout of POD2.

Table A-1 ADDR (POD2)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
C1	5	6	**SYSCLK**
A31	7	8	A15
A30	9	10	A14
A29	11	12	A13
A28	13	14	A12
A27	15	16	A11
A26	17	18	A10
A25	19	20	A9
A24	21	22	A8
A23	23	24	A7
A22	25	26	A6
A21	27	28	A5
A20	29	30	A4
A19	31	32	A3
A18	33	34	A2
A17	35	36	A1
A16	37	38	A0

POD2 pin 5 (C1) is **BTRAN1** on ASB and **HTRANS1** on AHB. You can use this pin to qualify addresses on active cycles.

Table A-2 shows the pinout of POD4.

Table A-2 DATA (POD4)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
C12	5	6	**SYSCLK**
D31	7	8	D15
D30	9	10	D14
D29	11	12	D13
D28	13	14	D12
D27	15	16	D11
D26	17	18	D10
D25	19	20	D9
D24	21	22	D8
D23	23	24	D7
D22	25	26	D6
D21	27	28	D5
D20	29	30	D4
D19	31	32	D3
D18	33	34	D2
D17	35	36	D1
D16	37	38	D0

POD4 pin 5 (C12) is **BWAIT** on ASB and **HREADY** on AHB. You can use this pin to qualify data transfers. **A[31:0]** is **BA[31:0]** for ASB and **HADDR[31:0]** for AHB. **D[31:0]** is **BD[31:0]** for ASB and **HDATA[31:0]** for AHB.

The control bus signals have different meanings depending on whether the system is ASB or AHB. The ASB/AHB specific signals are indicated in italics. Signals marked * are **nIRQ** when analyzing HDRB and **nIRQSRC** when analyzing EXPB. All **nFIQ** signals are *No connects* when analyzing EXPB.

Table A-3 shows the pinout of POD5 and POD6 for an ASB implementation.

Table A-3 CONTROL 1 (POD6) and CONTROL 2 (POD5) for ASB

POD6				POD5			
Channel	**Pin**	**Pin**	**Channel**	**Channel**	**Pin**	**Pin**	**Channel**
No connect	1	2	No connect	No connect	1	2	No connect
GND	3	4	No connect	**GND**	3	4	No connect
nSYSRST	5	6	***SYSCLK***	To via V2	5	6	To via V3
C31	7	8	C26	**BANK7**	7	8	**nIRQ3***
C30	9	10	C25	**BANK6**	9	10	**nIRQ2***
C29	11	12	C24	**BANK5**	11	12	**nIRQ1***
C28	13	14	C23	**BANK4**	13	14	**nIRQ0***
C27	15	16	C22	**nMADV**	15	16	**nFIQ3**
C4	17	18	C21	**nRTCKEN**	17	18	**nFIQ2**
C10	19	20	C20	**GLB_DONE**	19	20	**nFIQ1**
BLAST	21	22	C19	**CFGSEL1**	21	22	**nFIQ0**
BERROR	23	24	C18	**CFGSEL0**	23	24	Reserved
BWAIT	25	26	C17	**MASTER2**	25	26	Reserved
BLOK	27	28	C16	**MASTER1**	27	28	Reserved
BSIZE1	29	30	C7	**MASTER0**	29	30	Reserved
BSIZE0	31	32	C6	***AGNT3***	31	32	***AREQ3***
BPROT1	33	34	C5	***AGNT2***	33	34	***AREQ2***
BPROT0	35	36	***BTRAN1***	***AGNT1***	35	36	***AREQ1***
BWRITE	37	38	***BTRAN0***	***AGNT0***	37	38	***AREQ0***

Table A-4 shows the pinout of POD5 and POD6 for an AHB implementation.

Table A-4 CONTROL1 (POD6) and CONTROL2 (POD5) for AHB

POD6				POD5			
Channel	**Pin**	**Pin**	**Channel**	**Channel**	**Pin**	**Pin**	**Channel**
No connect	1	2	No connect	No connect	1	2	No connect
GND	3	4	No connect	**GND**	3	4	No connect
nSYSRST	5	6	***SYSCLK***	To via V2	5	6	To via V3
C31	7	8	C26	**BANK7**	7	8	**nIRQ3***
C30	9	10	C25	**BANK6**	9	10	**nIRQ2***
C29	11	12	C24	**BANK5**	11	12	**nIRQ1***
C28	13	14	C23	**BANK4**	13	14	**nIRQ0***
C27	15	16	C22	**nMADV**	15	16	**nFIQ3**
HPROT3	17	18	***HSPLIT5***	**nRTCKEN**	17	18	**nFIQ2**
HPROT2	19	20	***HSPLIT4***	**GLB_DONE**	19	20	**nFIQ1**
HRESP1	21	22	***HSPLIT3***	**CFGSEL1**	21	22	**nFIQ0**
HRESP0	23	24	***HSPLIT2***	**CFGSEL0**	23	24	***HLOCK3***
HREADY	25	26	***HSPLIT1***	**MASTER2**	25	26	***HLOCK2***
HMASTLOCK	27	28	***HSPLIT0***	**MASTER1**	27	28	***HLOCK1***
HSIZE1	29	30	***HBURST2***	**MASTER0**	29	30	***HLOCK0***
HSIZE0	31	32	***HBURST1***	***HGRANT3***	31	32	***HBUSREQ3***
HPROT1	33	34	***HBURST0***	***HGRANT2***	33	34	***HBUSREQ2***
HPROT0	35	36	***HTRAN1***	***HGRANT1***	35	36	***HBUSREQ1***
HWRITE	37	38	***HTRAN0***	***HGRANT0***	37	38	***HBUSREQ0***

Table A-5 shows the pinout of POD7.

Table A-5 BUSB (POD7)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
To via V5	5	6	To via V4
B31 (to via V6)	7	8	B15
B30	9	10	B14
B29	11	12	B13
B28	13	14	B12
B27	15	16	B11
B26	17	18	B10
B25	19	20	B9
B24	21	22	B8
B23	23	24	B7
B22	25	26	B6
B21	27	28	B5
B20	29	30	B4
B19	31	32	B3
B18	33	34	B2
B17	35	36	B1
B16	37	38	B0

Table A-6 shows the pinout of POD8.

Table A-6 GPIO/BUSF (POD8)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
To via V8	5	6	To via V9
GPIO/F31	7	8	GPIO/F15
GPIO/F30	9	10	GPIO/F14
GPIO/F29	11	12	GPIO/F13
GPIO/F28	13	14	GPIO/F12
GPIO/F27	15	16	GPIO/F11
GPIO/F26	17	18	GPIO/F10
GPIO/F25	19	20	GPIO/F9
GPIO/F24	21	22	GPIO/F8
GPIO/F23	23	24	GPIO/F7
GPIO/F22	25	26	GPIO/F6
GPIO/F21	27	28	GPIO/F5
GPIO/F20	29	30	GPIO/F4
GPIO/F19	31	32	GPIO/F3
GPIO/F18	33	34	GPIO/F2
GPIO/F17	35	36	GPIO/F1
GPIO/F16	37	38	GPIO/F0

A.2 Memory bus

Table A-7 shows the pinout of POD1.

Table A-7 MADDR (POD1)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
nMWR0	5	6	**nMWR1**
nMWR3	7	8	**MA15**
nMWR2	9	10	**MA14**
nMCS3	11	12	**MA13**
nMCS2	13	14	**MA12**
nMCS1	15	16	**MA11**
nMCS0	17	18	**MA10**
MA25	19	20	**MA9**
MA24	21	22	**MA8**
MA23	23	24	**MA7**
MA22	25	26	**MA6**
MA21	27	28	**MA5**
MA20	29	30	**MA4**
MA19	31	32	**MA3**
MA18	33	34	**MA2**
MA17	35	36	**MA1**
MA16	37	38	**MA0**

Table A-8 shows the pinout of POD3.

Table A-8 MDATA (POD3)

Channel	Pin	Pin	Channel
No connect	1	2	No connect
GND	3	4	No connect
MEMCLK	5	6	**nMOE**
MD31	7	8	**MD15**
MD30	9	10	**MD14**
MD29	11	12	**MD13**
MD28	13	14	**MD12**
MD27	15	16	**MD11**
MD26	17	18	**MD10**
MD25	19	20	**MD9**
MD24	21	22	**MD8**
MD23	23	24	**MD7**
MD22	25	26	**MD6**
MD21	27	28	**MD5**
MD20	29	30	**MD4**
MD19	31	32	**MD3**
MD18	33	34	**MD2**
MD17	35	36	**MD1**
MD16	37	38	**MD0**