Integrator™/IM-LT1

Interface Module

User Guide

ARM®

ARM DUI 0187B

Integrator/IM-LT1

User Guide

Release Information

Description	Issue	Change
23 Oct. 2002	A	New document
28 May 2004	B	Update header pin naming

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

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Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

The Integrator generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- ensure attached cables do not lie across the card
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- consult the dealer or an experienced radio/TV technician for help

Note

It is recommended that wherever possible shielded interface cables be used.

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Integrator/IM-LT1 User Guide

Appendix A Signal Descriptions

Preface

This preface introduces the reference documentation for the ARM Integrator/IM-LT1 Interface Module. It contains the following sections:

About this document

This document describes how to set up and use the ARM Integrator/IM-LT1 Interface Module.

Intended audience

This document has been written for experienced hardware and software developers to aid the development of ARM-based products using the Interface Module and a Logic Tile as part of a development system.

Organization

This document is organized into the following chapters:

Chapter 1 ***Introduction***

Read this chapter for an introduction to the Interface Module. This chapter shows the physical layout of the Interface Module and identifies the main components.

Chapter 2 ***Getting Started***

Read this chapter for a description of how to set up and start using the Interface Module with a Logic Tile. This chapter describes how to connect the Interface Module and how to apply power.

Chapter 3 ***Hardware Description***

Read this chapter for a description of the hardware architecture of the Interface Module. This chapter describes the clocks, resets, and debug hardware provided by the Interface Module and interconnections between the Interface Module and Logic Tiles.

Appendix A ***Signal Descriptions***

Refer to this appendix for a description of the signals on the Interface Module connectors.

Appendix B ***Specifications***

Refer to this appendix for electrical, timing, and mechanical specifications.

Typographical conventions

The following typographical conventions are used in this book:

`monospace` Denotes text that can be entered at the keyboard, such as commands, file and program names, and source code.

`mono`space Denotes a permitted abbreviation for a command or option. The underlined text can be entered instead of the full command or option name.

`monospace italic`

Denotes arguments to commands and functions where the argument is to be replaced by a specific value.

italic Highlights important notes, introduces special terminology, denotes internal cross-references, and citations.

bold Highlights interface elements, such as menu names and buttons. Also used for terms in descriptive lists, where appropriate.

`monospace bold`

Denotes language keywords when used outside example code and ARM processor signal names.

Further reading

This section lists related publications by ARM Limited and other companies provide additional information.

ARM publications

The following publications provide information about related ARM products and toolkits:

- *Integrator/XC2V4000+ Logic Tile User Guide* (ARM DUI 0186)
- *ARM Integrator/AP User Guide* (ARM DUI 0098)
- *ETM10 Technical Reference Manual* (ARM DDI 0206)
- *ARM Multi-ICE User Guide* (ARM DUI 0048)
- *AMBA Specification* (ARM IHI 0011)
- *ARM Architectural Reference Manual* (ARM DDI 0100)
- *ARM Firmware Suite Reference Guide* (ARM DUI 0102)
- *Multi-ICE™ User Guide* (ARM DUI 0048)
- *RealView™ ICE User Guide* (ARM DUI 0155)

- *Trace Debug Tools User Guide* (ARM DUI 0118)
- *ARM MultiTrace® User Guide* (ARM DUI 0150)
- *ARM RealView Logic Tile LT-XC2V4000+ User Guide* (ARM DUI 0186)
- *RealView Debugger User Guid*e (ARM DUI 0153)
- *RealView Compilation Tools Compilers and Libraries Guide* (ARM DUI 0205)
- *RealView Compilation Tools Developer Guide* (ARM DUI 0203)
- *RealView Compilation Tools Linker and Utilities Guid*e (ARM DUI 0206)
- *Versatile/Core Tile User Guide* (ARM DUI0273)
- *Versatile/IT1 Interface Tile User Guide* (ARM DUI0188).

Other publications

The following publication provides information about the clock controller chip used on the Integrator module:

- *ICS Serially Programmable Clock Source Data Sheet* (ICS307), MicroClock Division of ICS, San Jose, CA.

Feedback

ARM Limited welcomes feedback both on the ARM Integrator/IM-LT1 Interface Module and on the documentation.

Feedback on this document

If you have any comments about this document, please send email to `errata@arm.com` giving:

- the document title
- the document number
- the page number(s) to which your comments refer
- an explanation of your comments.

General suggestions for additions and improvements are also welcome.

Feedback on the Interface Module

If you have any comments or suggestions about this product, please contact your supplier giving:

- the product name
- an explanation of your comments.

Chapter 1
Introduction

This chapter introduces the ARM Integrator/IM-LT1 Interface Module. It contains the following sections:

1.1 About the Interface Module

The Integrator/IM-LT1 Interface Module is an Interface Module that allows you to connect Integrator tiles to an Integrator/AP or Integrator/CP motherboard. This provides you with a development platform for ARM Integrator tiles (for example, the ARM Integrator/XC2V4000+ Logic Tile). Typical uses for the Interface Module and tile include:

- peripheral development for use with an ARM core
- prototyping a SOC (in one or more Logic Tiles) and developing code for it
- developing code for an ARM core synthesized in a Logic Tile FPGA.

Figure 1-1 shows the IM-LT1 Interface Module and its components.

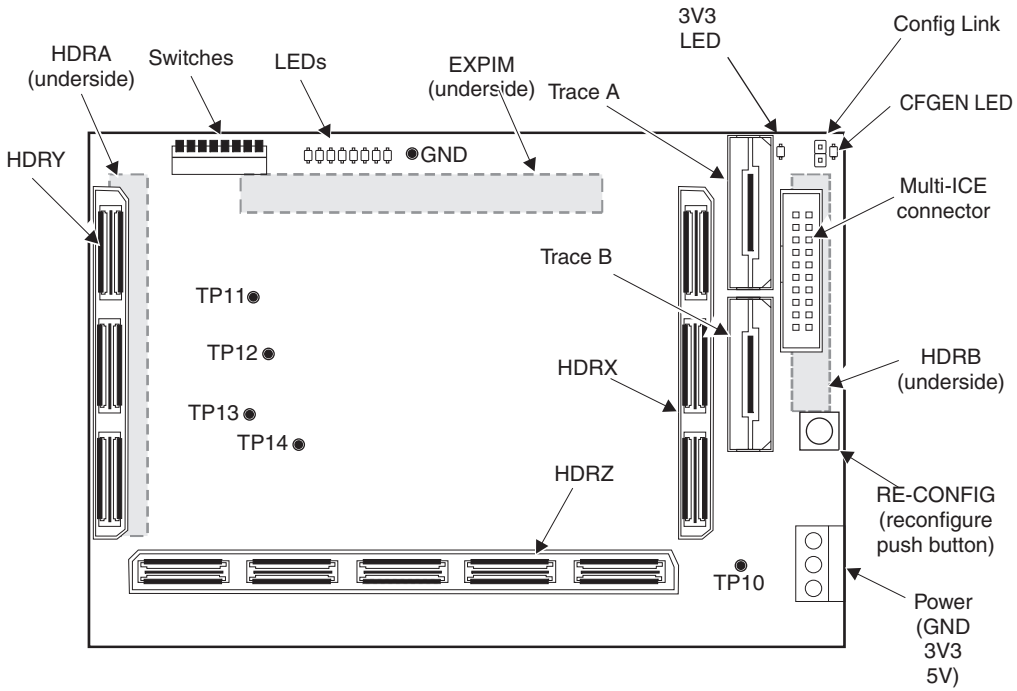


Figure 1-1 Integrator/IM-LT1 Interface Module layout

1.2 Interface module architecture

The IM-LT1 contains connectors and logic that enables a Logic Tile to be connected:

- Integrator/AP style connectors HDRA, HDRB, and EXPIM
- Integrator tile connectors HDRX, HDRY, and HDRZ
- Power-on reset logic
- Multi-ICE (JTAG) connector and routing logic
- Trace port analyzer connectors
- LEDs and switches.

1.2.1 System architecture

The primary function of the Interface Module is to provide a connection between an Integrator motherboard and Integrator tiles. (The Integrator/AP and Integrator/CP use a different connector type and signal organization than the Integrator tiles.) The Interface Module also has connectors for Multi-ICE and trace. Figure 1-2 shows the architecture of the IM-LT1 Interface Module.

Note

The same PCB is used for the IM-LT1 and the IM-LT2. The IM-LT2 has additional logic and provides additional functionality to a Logic Tile implementing an ARM processor core. There are solder links on the Interface Module that bridge signals that are connected to an FPGA on the IM-LT2. The solder links are set at build time and are not user configurable.

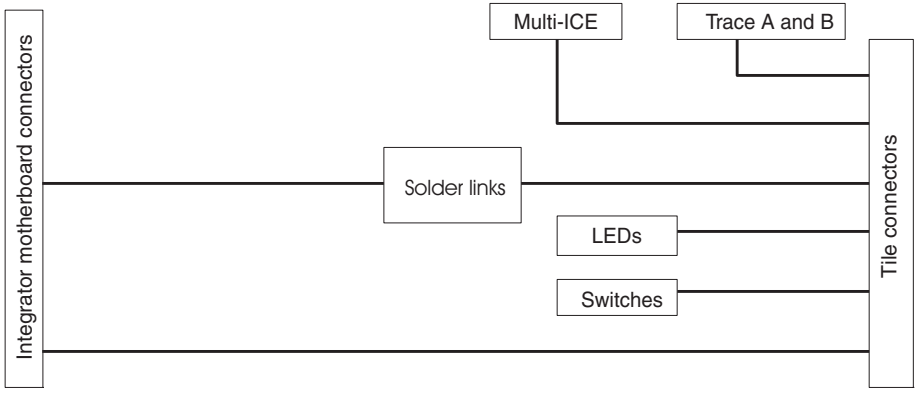


Figure 1-2 IM-LT1 block diagram

1.2.2 Multi-ICE connector

The Multi-ICE connector enables JTAG equipment, such as Multi-ICE, to be connected to the Interface Module. The JTAG signals are routed to all tiles stacked on the Interface Module and enables reprogramming of all programmable logic and onboard flash memory. See *JTAG support* on page 3-12.

1.2.3 Power supplies

The Interface Module requires two voltage sources:

5V Power supply for expansion circuitry (tiles use this voltage to generate additional voltages required for the tile FPGA)

3.3V Power supply for tile logic and interface circuits.

1.3 Precautions

This section contains safety information and advice on how to avoid damage to the Interface Module.

1.3.1 Ensuring safety

The Interface Module is powered from 3.3V and 5V DC supplies.

Warning

To avoid a safety hazard, only connect *Safety Extra Low Voltage* (SELV) equipment to the Interface Module connectors (for example, the JTAG interface).

Do not use the board near equipment which is sensitive to electromagnetic emissions (such as medical equipment)

1.3.2 Preventing damage

The Interface Module is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure which leaves the board sensitive to electrostatic discharges and allows electromagnetic emissions.

Caution

To avoid damage to the board, observe the following precautions.

- Never subject the board to high electrostatic potentials.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- When removing the module from a motherboard, take care not to damage the connectors. Do not apply a twisting force to the ends of the connectors.
- Avoid touching the component pins or any other metallic element.
- Do not use the board near a transmitter of electromagnetic emissions.
- Use the Interface Module and tiles in a clean environment and avoid debris fouling the connectors on the underside of the PCB. Blocked holes result in damage to connectors. Visually inspect the tile to ensure that connector holes are clear before mounting it onto another board.
- The power blades on the header connectors can carry up to 9A. Typically this will supply up to six tiles. Always turn off the power supply before adding or removing tiles.

Chapter 2
Getting Started

This chapter describes how to set up and prepare the Interface Module for use. It contains the following sections:

2.1 Configuration

The Interface Module must be used together with one or more tiles.

A typical configuration is an Integrator/AP motherboard, Integrator core module, IM-LT1, and one or more Logic Tiles configured for peripheral development.

The Integrator/AP motherboard provides memory and standard I/O, the Integrator core module is installed on the HDRA/HDRB connectors, and the Interface Module and Logic Tile is installed on the EXPA/EXPB connectors. The Logic Tile FPGA contains an implementation of synthesized peripherals.

The power supply is connected to the Integrator motherboard. The Multi-ICE connector on the core module is used for downloading and debugging software and the Multi-ICE connector on the Interface Module is used to update FPGA images in the Logic Tile flash memory.

2.2 Using the Interface Module with an Integrator motherboard

Attach the Interface Module onto a motherboard (for example, the ARM Integrator/AP shown in Figure 2-1) by engaging the connectors on the bottom of the Interface Module with the corresponding connectors on the top of the motherboard.

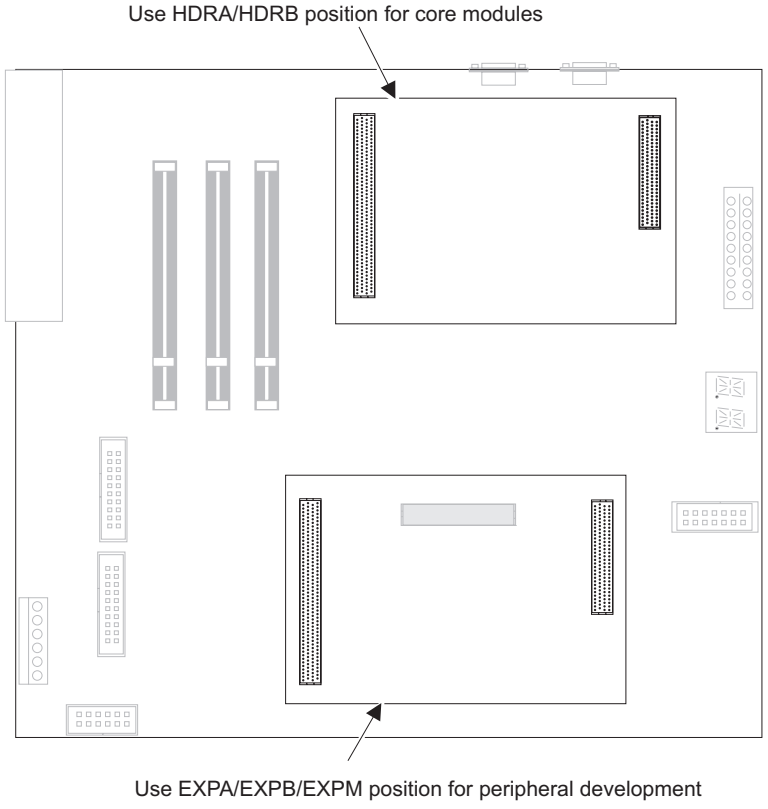


Figure 2-1 Header location on Integrator/AP motherboard

2.2.1 Integrator/AP motherboard

To use a Logic Tile with an Integrator/AP:

1. Connect a core module to the HDRA and HDRB sockets on the motherboard.
2. Connect one or more Logic Tiles to the Interface Module.
3. Connect the Interface Module to the EXPA and EXPB sockets on the motherboard.
4. Connect Multi-ICE to the Interface Module if you are downloading images to the Logic Tile. Connect to the core module if you are running code. (see *Connecting Multi-ICE* on page 2-6).
5. Supply power to the Integrator motherboard.
6. The Logic Tiles are shipped with pre-installed example images. You can, however, download two of your own FPGA images to the Logic Tile. For more information, see the sections on getting started and example images in the documentation supplied with your tile.

2.2.2 Integrator/CP baseboard

To use a Logic Tile with an Integrator/CP:

1. Connect an Integrator/CP compatible core module to the HDRA and HDRB sockets on the CP baseboard.
2. Connect one or more Logic Tiles to the Interface Module.
3. Connect the Interface Module to the HDRA and HDRB sockets on the core module.
4. Connect Multi-ICE to the Interface Module. (see *Connecting Multi-ICE* on page 2-6).
5. Supply power to the Integrator baseboard.
6. The Logic Tiles are shipped with pre-installed example images. You can, however, download two of your own FPGA images to the Logic Tile. For more information, see the sections on getting started and example images in the documentation supplied with your tile.

2.2.3 Powering the assembled Integrator development system

Power the assembled Integrator development system by either:

- connecting a bench power supply to the motherboard (or for the Integrator/CP, use the power supply provided with the board)
- for the Integrator/AP, installing the motherboard in a card cage or an ATX-type PC case, depending on type.

For further information, refer to the user guide for the Integrator motherboard you are using.

2.3 Connecting Multi-ICE

Multi-ICE can be used to download images to the configuration flash on attached Logic Tiles or other boards. The Multi-ICE connection to the Interface Module is shown in Figure 2-1.

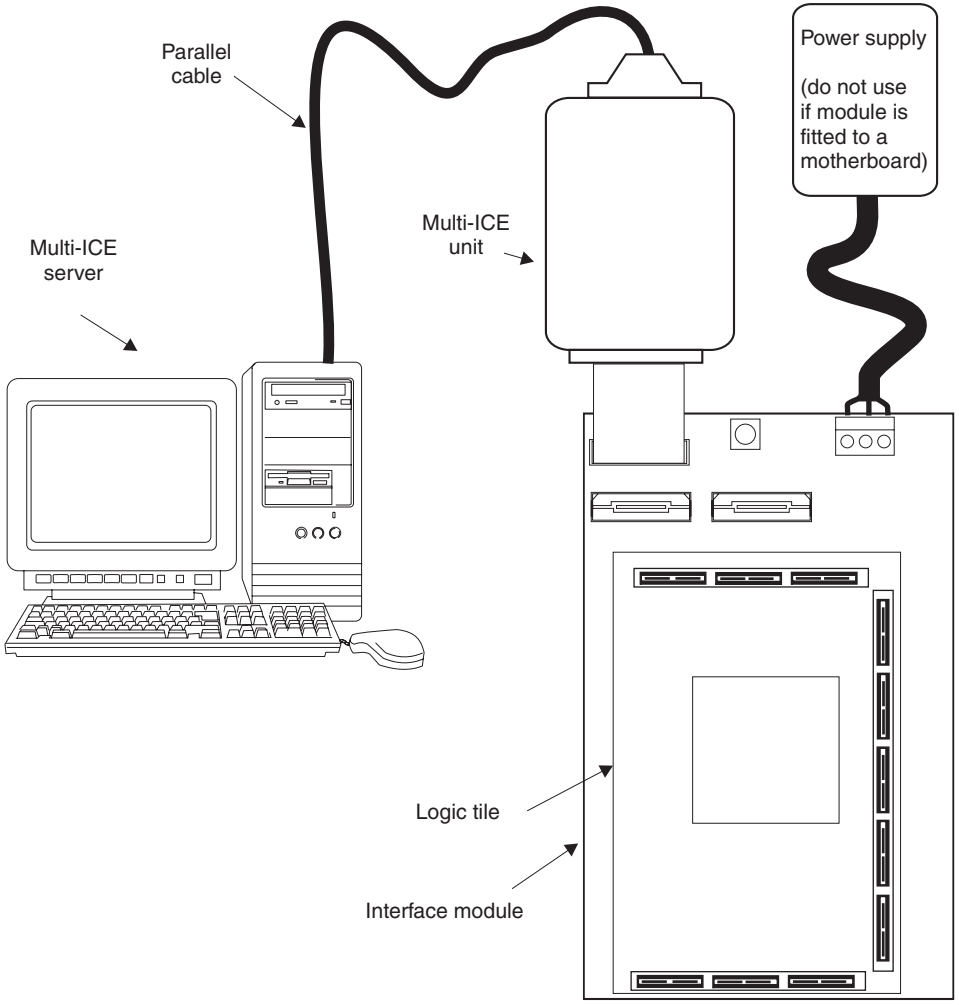


Figure 2-1 Multi-ICE connection to a Interface Module

If more than one Logic Tile is attached, the Multi-ICE connections are routed through the additional tiles.

2.4 Switches, links, and indicators

The Interface Module link, switches, and LEDs are shown in Figure 2-2.

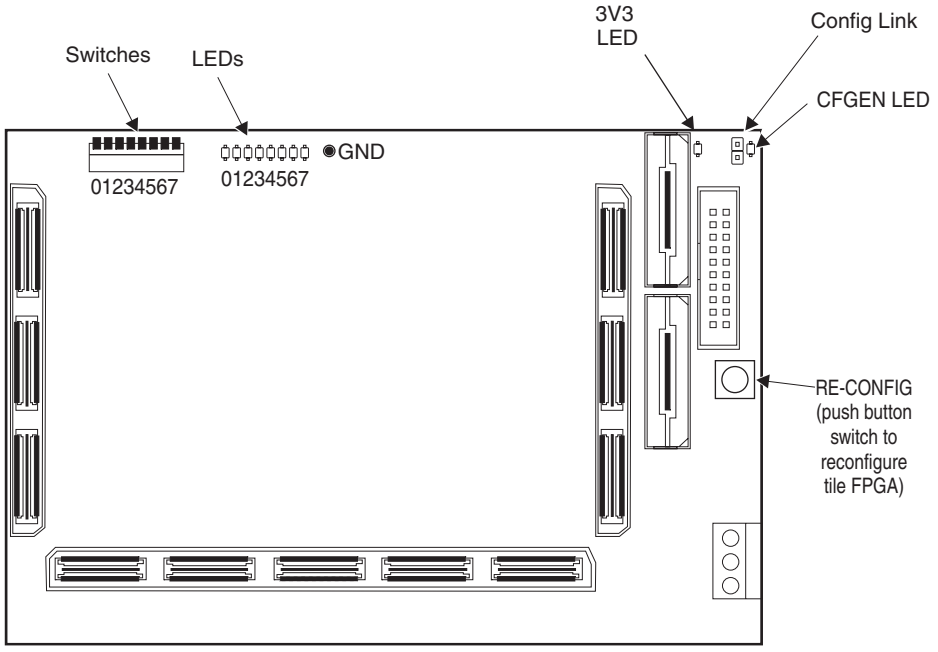


Figure 2-2 Links, switches, and indicators

2.4.1 User switches

There is a push button and a DIP switch bank fitted to the IM-LT1:

S2 RE-CONFIG

This switch reconfigures all tile FPGAs in the system.

S3[7:0] These switches can be read from I/O on the Logic Tile. (The numbers refer to the register bits. The switches are actually labeled 8:1.)

2.4.2 Multi-ICE CONFIG link

The Interface Module has only one link, configuration enable (marked CFGEN link). This is left open during normal operation (debug mode). It is only fitted when downloading new FPGA or PLD configuration information (config mode).

2.4.3 User LEDs

LEDs [7:0] can be lit from I/O on a connected Logic Tile.

2.4.4 Status indicators

The functions of the surface-mounted LEDs are summarized in Table 2-1.

Table 2-1 LED functional summary

Name	Color	Function
3V3	Green	This LED illuminates to indicate that a 3.3V supply is present
CFGEN	Orange	This LED illuminates to indicate that the CONFIG link is fitted

Chapter 3
Hardware Description

This chapter describes the on-board hardware. It contains the following sections:

3.1 IM-LT1 overview

The IM-LT1 Interface Module allows an Integrator tile to connect to an Integrator/AP or Integrator/CP system. The Interface Module has the following logic and connectors:

- user switches and LEDs
- Multi-ICE connector
- two trace connectors
- HDRA,HDRB, and EXPIM for connection to a motherboard
- HDRX, HDRY, and HDRZ connectors for connection to Logic Tiles
- Power-on reset circuitry
- reconfigure circuitry
- standalone power connector.

3.2 Reset control

Figure 3-1 shows the architecture of the reset circuitry. Figure 3-2 on page 3-4 shows the power-on reset timing. In debug mode (see *Debug mode* on page 3-13), the following resets can be implemented in your design:

- **nSYSRST**
- **nSYSPOR**
- **D_nSRST**
- **D_nTRST**.

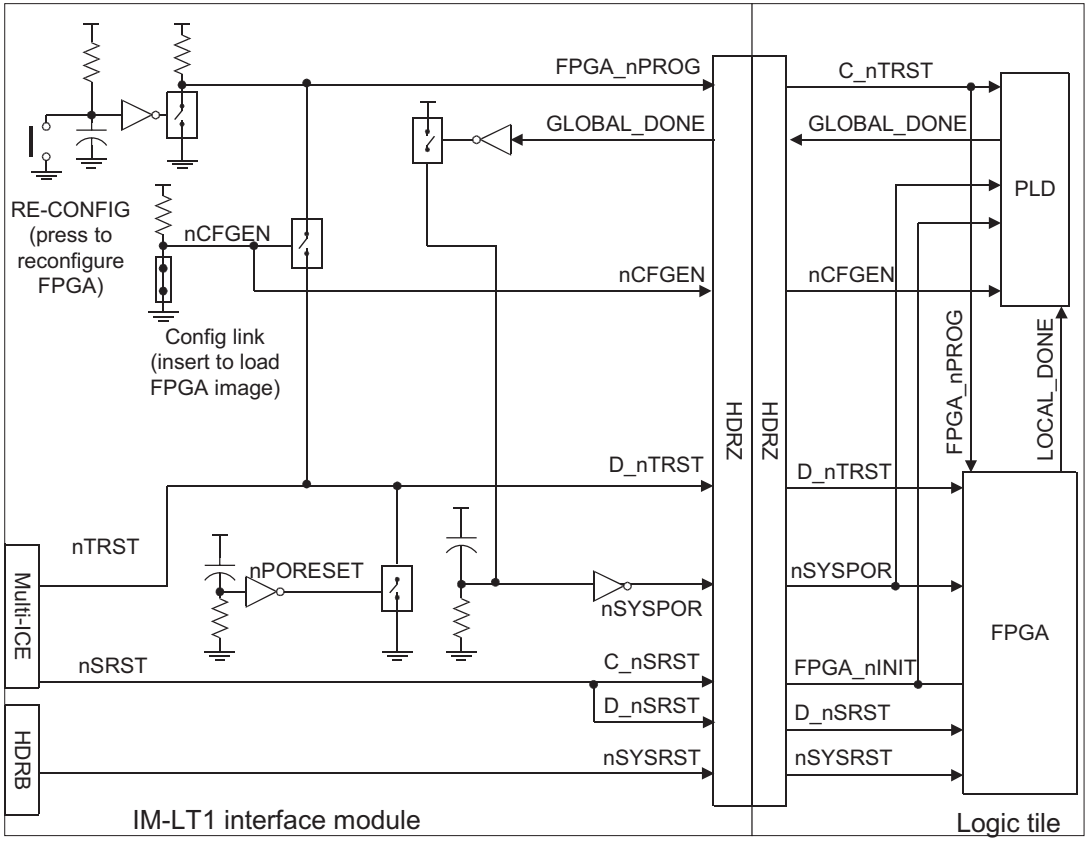


Figure 3-1 Reset and image loading control

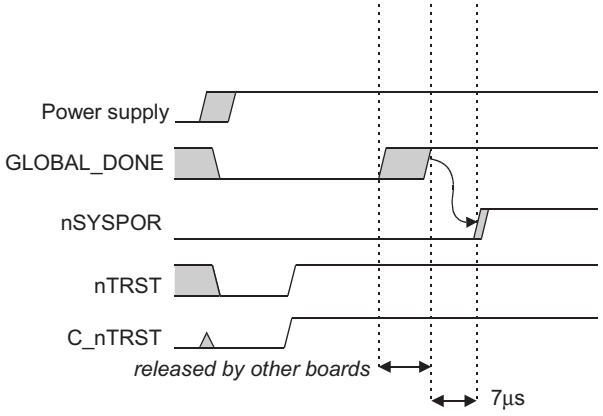


Figure 3-2 Power-on reset timing

Note

The release time for **GLOBAL_DONE** depends on other boards in the system. It might be held low longer if other boards take longer to configure.

Table 3-1 on page 3-5 describes the external reset signals.

Table 3-1 Reset signal descriptions

Name	Description	Function
nPORESET	Power-on reset	This signal is used to generate the **D_nTRST** pulse at power on.
nSRST	System reset	**nSRST** is an active LOW open-collector signal that can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when you have reset a board. When the signal is driven LOW by the reset controller on the tile, the motherboard resets the whole system by driving **nSYSRST** LOW. This is also used in configuration mode to control the initialization pin (**nINIT**) on the FPGAs. Though not a JTAG signal, **nSRST** is described because it can be controlled by JTAG equipment. **Note** **nSRST** splits into two signals, **D_nSRST** and **C_nSRST**, to provide the debug and configuration signals on HDRZ.
nSYSRST	System reset	A system-wide, master reset signal from the platform board (for example the Integrator/AP and IM-LT1). This signal is typically used to reset ARM cores, peripherals and user logic. Can be activated from several sources, including **GLOBAL_DONE**=0. (See the *Integrator/AP Motherboard User Guide* or the *Integrator/CP Compact Platform User Guide* for further information on motherboard signals.)
FPGA_nPROG	Configuration reload	The **FPGA_nPROG** signal forces all FPGAs in the system to reconfigure.
GLOBAL_DONE	Configuration done	Open-collector signal that goes HIGH when all FPGAs have finished configuring. The system is held in reset until this signal goes HIGH.
nSYSPOR	Power-on reset	This is a post-configuration reset signal that is passed to all Logic Tiles in a stack. It is generated by analogue circuitry on the Interface Module. It can be used to reset user logic if required. It remains active for between 1 and 10µS after **GLOBAL_DONE** goes HIGH.

Table 3-1 Reset signal descriptions (continued)

Name	Description	Function
D_nTRST	TAP controller reset	A system-wide, open collector signal that can be driven LOW by Multi-ICE. This is the debug version of the **nTRST** signal. It is connected to an FPGA input/output pin to provide a reset input to the *virtual* TAP controller. The Multi-ICE connector is the source of the **D_nTRST** signal.
D_nSRST	Multi-ICE system reset	A system-wide, open collector signal that can be driven LOW by Multi-ICE. This is the debug version of the **nSRST** signal.
C_nTRST	TAP controller reset	An open-collector signal that can be driven LOW by Multi-ICE when using the Progcards utility to program the Logic Tile FPGA. (This signal is connected to the **PROG** pin of the FPGA.) This is the config version of the **nTRST** signal.
C_nSRST	Multi-ICE system reset	A system-wide, open-collector signal. The Interface Tile shorts this signal to **D_nSRST**. This signal can be driven LOW by Multi-ICE when using the Progcards utility to program the Logic Tile FPGA. (This signal is connected to the **INIT** pin of the FPGA.) This is the config version of the **nSRST** signal. **Note** On the Integrator/AP, the expansion connector (EXPB) **nSRST** signal is completely separate from the core module (HDRB) **nSRST** signal (see the *Integrator/AP User Guide* for more details).

3.3 Header connectors

The Interface Module provides Integrator/AP style connectors (HDRA, HDRB, and EXPIM) on the bottom of the board and tile connectors (HDRX, HDRY, and HDRZ) on the top.

3.3.1 Interconnection between lower and upper headers

Some signals are connected directly from the pins on the lower headers to pins on the upper headers. Depending on the signal, they might also be connected to logic on the Interface Module.

3.3.2 Voltages on header pins

The voltages on the upper connectors depends on the connector and on configuration settings:

- A 3.3V supply is present on HDRZ.
- All HDRZ signals operate at 3.3V.
  - Signals on pins 1 – 124 (IM_ABANK[61:0] and IM_BBANK[61:0]) are connected to the Integrator EXPIM connector.
  - Signals on pins 125 –172 (the central group) carry clocks, JTAG, and other system signals.
  - Signals on pins 173 – 300 are allocated to A, B, C, and D 32-bit buses.
- A 5V supply is present on HDRX and HDRY. This voltage is used by the Logic Tiles to generate other required voltages.
- Attached tiles can use variable I/O signal levels on the HDRX and HDRY connectors. The signal levels are set by the **VCCOn** signal (where n is the bank number) on the tile fitted to the Interface Module. Many of the HDRX and HDRY signals on the IM-LT1 are connected directly to the Integrator HDRA and HDRB signals that must operate at 3.3V logic levels. The VCCO signals on the lower connectors for the tile must be set to 3.3V (the default).

Figure 3-1 on page 3-8 shows the voltages present on the HDRX, HDRY, and HRDZ tile connectors.

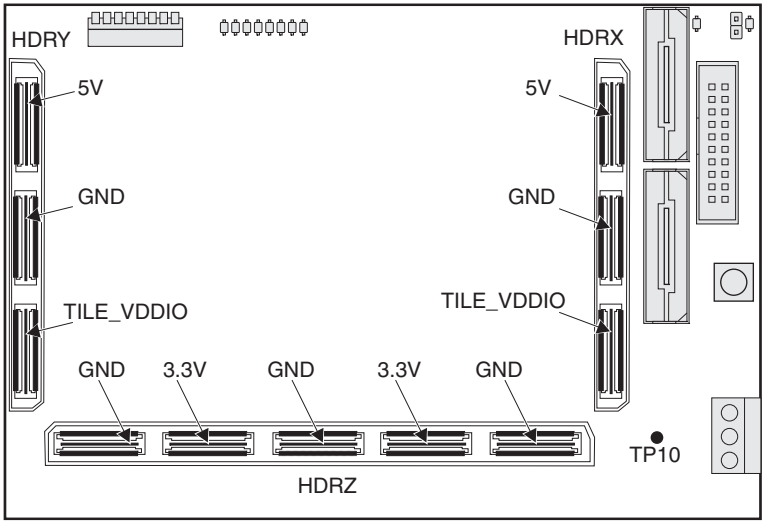


Figure 3-1 Voltages present on tile connector blades

3.3.3 Address decoding

The Integrator system implements a distributed address decoding system. Each core or logic module must decode its own area of the memory map. The central decoder in the system controller FPGA (on the motherboard) responds with an error code for all areas of the address space that are not occupied by a module. This default response is disabled for a memory region occupied by a module that is fitted.

The signals **nPRES[3:0]** are used to signal the presence of modules to the central decoder. The signals **HDRID[3:0]** indicate to the module its position in the stack and the address range that its own decoder must respond to. These signals rotate as they pass up the stack of core or logic modules. Only one signal in each group is pulled LOW for each module. Refer to the documentation supplied with your motherboard for more information.

The **nPRES[3:0]** signals are connected to the FPGA on the Logic Tile (see Figure 3-1 on page 3-9). By convention, a module always drives **nPRES[0]** LOW. However, if a module requires additional address space, higher **nPRES** signals can also be driven LOW.

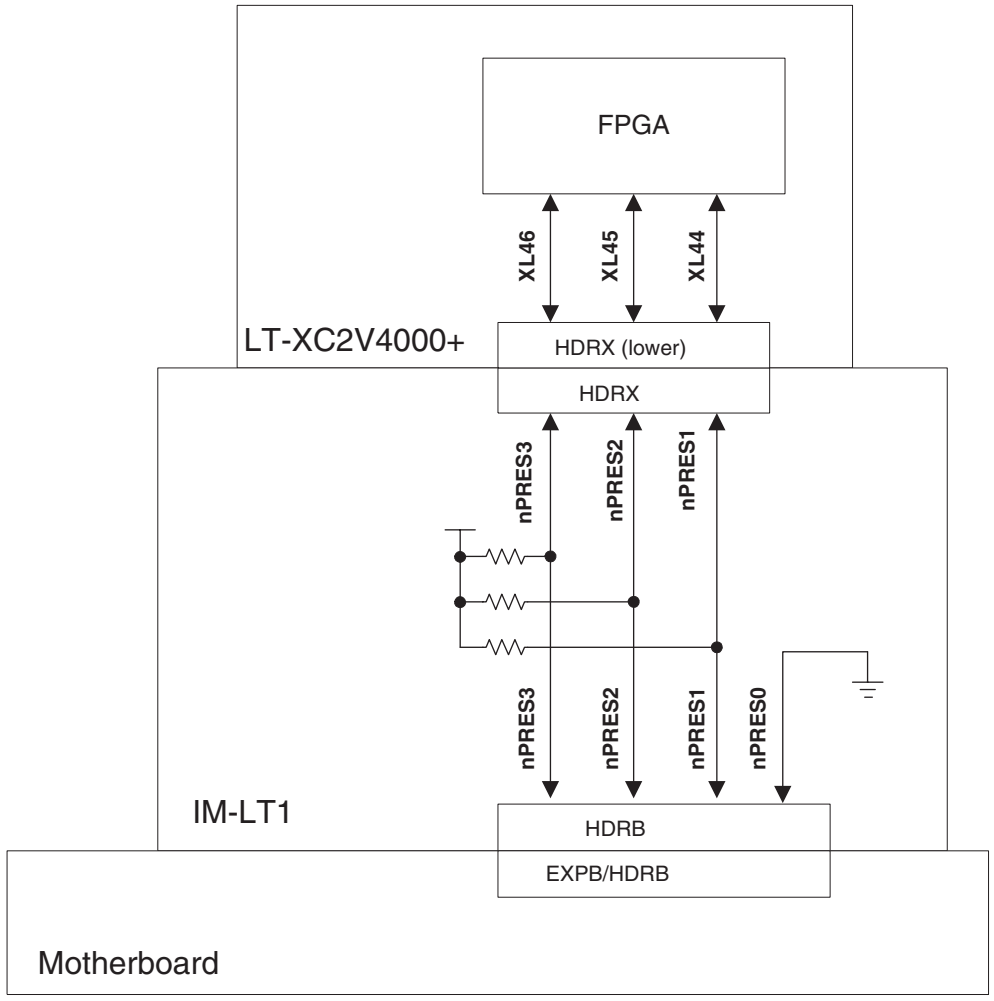


Figure 3-1 Interface module address selection

3.4 Clocks

There are no clocks generated on the Interface Module. Clocks present on the HDRB or EXPIM connectors are connected to the tile headers to provide system clocks.

For more information on the Logic Tile clocking schemes, see the *Integrator/XC2V4000+ Logic Tile User Guide*.

3.4.1 Clock routing to and from the Interface Module

Figure 3-1 shows the connections between motherboard and tile clock signals.

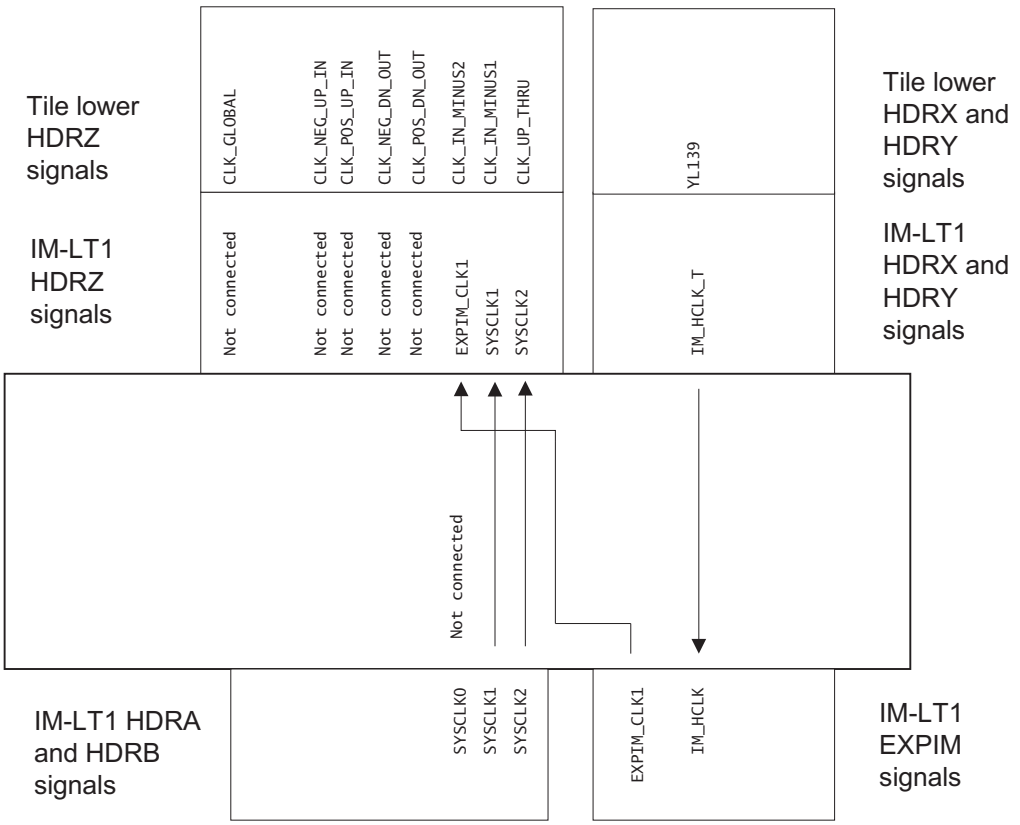


Figure 3-1 Clock signal routing between tiles

The Interface Module clock signals are listed in Table 3-1 on page 3-11. (For a description of JTAG and Trace clocks, see *JTAG support* on page 3-12).

Table 3-1 Interface module clocks

Signal	Source	Description
EXPIM_CLK1	Logic module (if fitted)	This general-purpose clock source is provided as an alternative clock.
IM_HCLK_T	Tile	This general-purpose clock source is available for use by the motherboard. The signal connects to the **IM_HCLK** signal on the EXPIM connector.
SYSCLK1	Integrator/AP or Integrator/CP	This clock signal from the motherboard is not connected to circuitry on the Interface Module, but passes up to the first tile in the stack.
SYSCLK2	Integrator/AP or Integrator/CP	This clock signal from the motherboard is not connected to circuitry on the Interface Module, but passes up to the second tile in the stack.

3.5 JTAG support

The Interface Module supports debugging and configuration using JTAG. This is described in the following subsections:

- *Multi-ICE connection*
- *JTAG scan paths* on page 3-13
- *JTAG signals* on page 3-17.

3.5.1 Multi-ICE connection

Figure 3-1 shows the Multi-ICE connector, CFGEN link and LED.

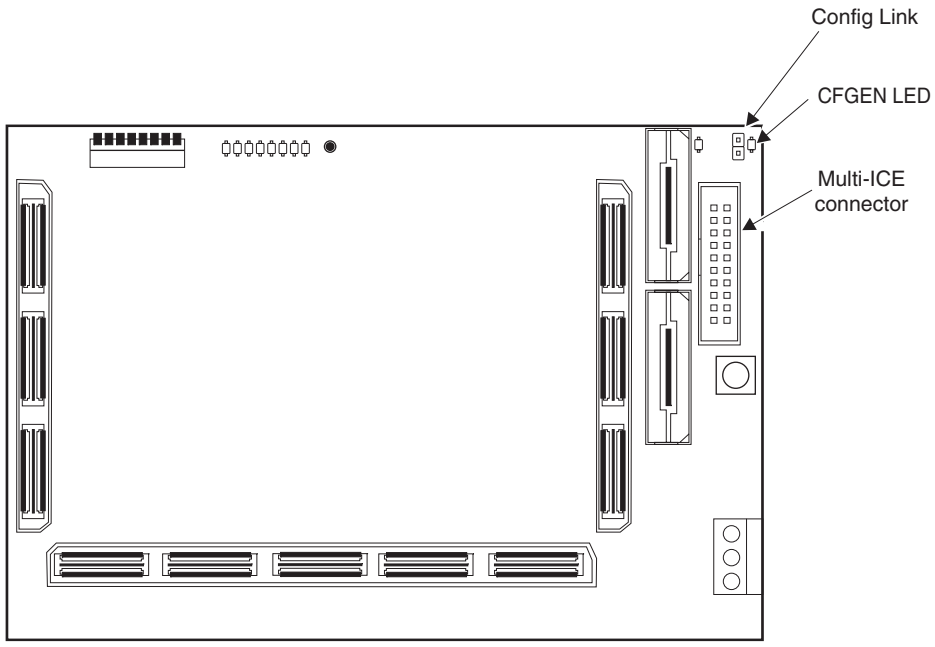


Figure 3-1 JTAG connector, CFGEN link, and LED

The CONFIG link is used to enable in-circuit programming of any tile FPGA and PLDs using Multi-ICE (see *JTAG scan paths* on page 3-13).

The Multi-ICE connector provides a set of JTAG signals that allow JTAG debugging equipment to be used (see *JTAG signals* on page 3-17). If you are debugging a development system with multiple tiles, connect the JTAG debugging equipment to the Interface Module and the JTAG signals are routed through any connected tiles.

3.5.2 JTAG scan paths

The system is capable of operating in debug mode (the normal operating mode) or configuration mode (used to load flash or FPGA images).

Debug mode

Debug mode is selected by default (when a jumper is not fitted on the CONFIG link, see Figure 3-1 on page 3-12). In this mode, the scan chain connects to any CPU cores in the stack of boards.

For tiles in the stack that implement a synthesized core and tap controller in the FPGA, the scan chain connects to the FPGA I/O pins for the tap controller.

Configuration mode

In configuration mode the configuration TAP controllers of all FPGAs and PLDs in the system are connected into the scan chain. This allows the board to be configured or upgraded using Multi-ICE or other JTAG debugging equipment.

To select configuration mode, fit a jumper to the CONFIG link on the Interface Module (see Figure 3-1 on page 3-12). This has the effect of pulling the **nCFGEN** signal LOW which illuminates the CFGEN LED on the Interface Module and reroutes the JTAG scan path. The LED provides an indication that the development system is in the configuration mode.

After upgrading the flash FPGA images:

1. Remove the CONFIG link.
2. Power cycle the development system.

The configuration mode allows FPGA and PLD code to be updated as follows:

- The FPGAs are volatile, but load their configuration from flash memory. Flash memory, which itself does not have a JTAG port, can be programmed by loading designs into the FPGAs and PLDs which handle the transfer of data to the flash using JTAG.
- The PLDs are nonvolatile devices which can be programmed directly by JTAG.

Data path

Figure 3-1 shows a simplified diagram of the data path in config mode.

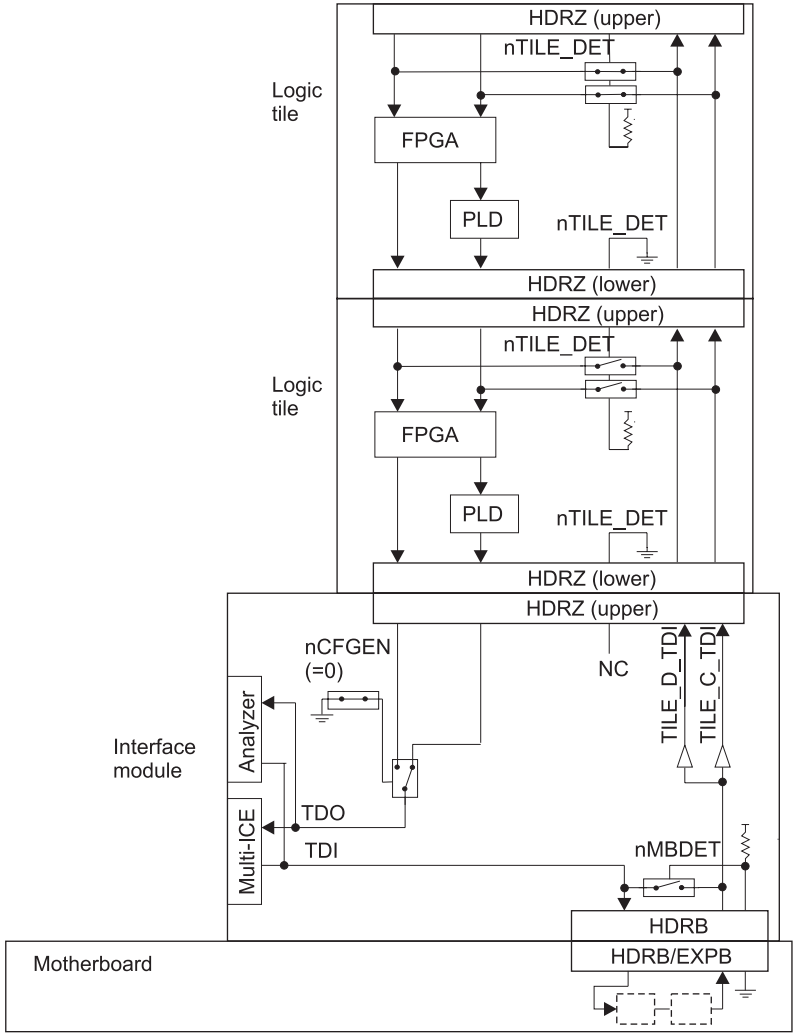


Figure 3-1 JTAG data path

When you use the Interface Module and tile as a standalone development system, the data path is routed to the Logic Tile and back to the Multi-ICE connector.

If the Interface Module and tile is attached to an Integrator motherboard, the **TDI** signal from the Interface Module is routed down through the HDRB connectors to the motherboard. From the motherboard, **TDI** is routed back up the stack through each tile, before being returned to the Multi-ICE connector as **TDO**. The motherboard detect signal, **nMBDET**, controls a switching circuit on the Interface Module and, therefore, the routing of **TDI**.

The PLDs and FPGAs are included in the scan chain if the core tile is in configuration mode, as described in *Multi-ICE connection* on page 3-12.

Clock path

The clock path is routed in a similar way to the data path, although in the opposite direction. Figure 3-2 shows a simplified diagram of the clock path.

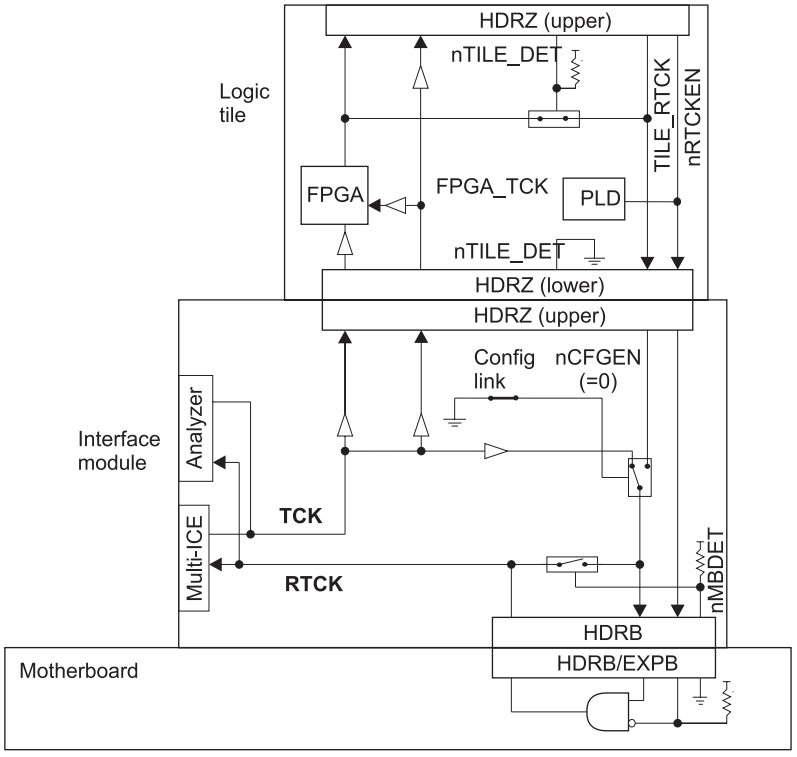


Figure 3-2 JTAG clock path

A number of synthesized cores sample **TCK**. This introduces a delay into the clock path. Cores of this type pass on the delayed clock signal as **RTCK**, which is fed to the **TCK** input of the next device in the chain. The **RTCK** signal at the Multi-ICE connector is used by Multi-ICE to regulate the advance of **TCK** (see the *ARM Multi-ICE User Guide*).

The routing of the **TCK/RTCK** signals through the stack is controlled by switches in a similar way to the data path. The routing of **RTCK** is controlled by the signal **nRTCKEN** and an AND gate on the motherboard. See the *Integrator/XC2V4000+ User Guide* for details on control of nRTCKEN.

TMS path

TMS controls transitions in the tap controller state machine. TMS connects to all JTAG components in the scan chain as the signal flows through the tile stack. Figure 3-1 shows the TMS path.

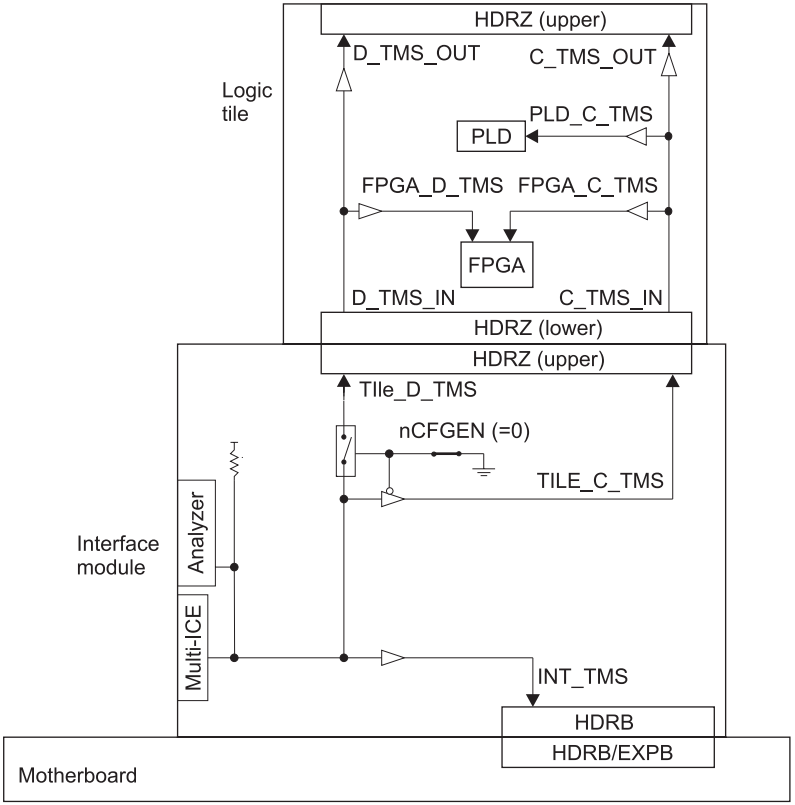


Figure 3-1 TMS path

3.5.3 JTAG signals

Figure 3-3 shows the pinout of the Multi-ICE connector and Table 3-1 provides a description of the JTAG and related signals.

Note

In the description in Table 3-1, the term JTAG equipment refers to any hardware that can drive the JTAG signals to devices in the scan chain.Typically this is Multi-ICE, although hardware from other suppliers can also be used to debug ARM processors.

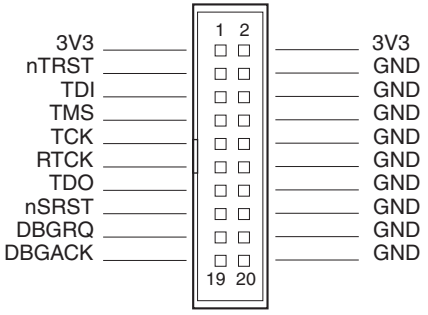


Figure 3-3 Multi-ICE connector pinout

Table 3-1 Multi-ICE signal description

Name	Description	Function
nTRST	Test reset (from JTAG equipment)	This active low open-collector is used to reset the JTAG port and the associated debug circuitry on the tile. It is asserted at power-up by each tile, and can be driven by the JTAG equipment. This signal is also used in configuration mode to control the programming pin (**nPROG**) on FPGAs.
TDI	Test data in (from JTAG equipment)	**TDI** goes down to the motherboard and then up to the top tile in the stack. The signal connects each component in the scan chain.
TMS	Test mode select (from JTAG equipment)	**TMS** controls transitions in the tap controller state machine. **TMS** connects to all JTAG components in the scan chain as the signal flows through the tile stack.

Table 3-1 Multi-ICE signal description (continued)

Name	Description	Function
TCK	Test clock (from JTAG equipment)	**TCK** synchronizes all JTAG transactions. **TCK** connects to all JTAG components in the scan chain. Buffers are used to reduce reflections and maintain good signal integrity. **TCK** flows up the stack of tiles and connects to each JTAG component. However, if there is a device in the scan chain that synchronizes **TCK** to some other clock, then all down-stream devices are connected to the **RTCK** signal on that component (see **RTCK**).
RTCK	Return TCK (to JTAG equipment)	Some devices sample **TCK** (for example a synthesizable core with only one clock), and this has the effect of delaying the time at which a component actually captures data. The **RTCK** signal is returned by the core to the JTAG equipment, and the clock is not advanced until the core has captured the data. Multi-ICE can be configured to wait for an edge on **RTCK** before changing **TCK**. In a multiple device JTAG chain, the **RTCK** output from a component connects to the **TCK** input of the next device in the chain. The **RTCK** signal on the tile connectors HDRB returns **TCK** to the JTAG equipment. If there are no synchronizing components in the scan chain then it is unnecessary to use the **RTCK** signal and it is connected to ground on the motherboard.
TDO	Test data out (to JTAG equipment)	**TDO** is the return path of the data input signal **TDI**. The tile connectors HDRZ have three pins labeled **TDI**, **TDO_IN**, and **TDO_OUT**. **TDI** refers to data flowing up the stack and **TDO** to data flowing down the stack. The JTAG components are connected in the return path so that the length of track driven by the last component in the chain is kept as short as possible.
nSRST	System reset (bidirectional)	**nSRST** is an active LOW open-collector signal which can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when a board has been reset by the user. When the signal is driven LOW by the reset controller on the tile, the motherboard resets the whole system by driving **nSYSRST** LOW. This is also used in configuration mode to control the initialization pin (**nINIT**) on the FPGAs. Though not a JTAG signal, **nSRST** is described because it can be controlled by JTAG equipment.
DBGRQ	Debug request (from JTAG equipment)	**DBGRQ** is a request for the processor core to enter the debug state. It is provided for compatibility with third-party JTAG equipment.

Table 3-1 Multi-ICE signal description (continued)

Name	Description	Function
DBGACK	Debug acknowledge (to JTAG equipment)	**DBGACK** indicates to the debugger that the processor core has entered debug mode. It is provided for compatibility with third-party JTAG equipment.
nRTCKEN	Return TCK enable (from core tile to motherboard, not present on connector)	**nRTCKEN** is an active LOW signal driven by any core module or tile that requires **RTCK** to be routed back to the JTAG equipment. If **nRTCKEN** is HIGH, the motherboard drives **RTCK** LOW. If **nRTCKEN** is LOW, the motherboard drives the **TCK** signal back up the stack to the JTAG equipment.
GLOBAL_DONE	All FPGAs configured (not present on connector)	**GLOBAL_DONE** is an open-collector signal that indicates when all FPGA configurations are complete. Although this signal is not a JTAG signal, it does effect **nSRST**. The **GLOBAL_DONE** signal is routed between all FPGAs in the system through the HDRB and HDRZ connectors. The master reset controller on the motherboard senses this signal and holds all the boards in reset (by driving **nSRST** LOW) until all FPGAs are configured.
nCFGEN	Configuration enable (from jumper on the Interface Module, not present on connector)	**nCFGEN** is an active LOW signal used to put the boards into configuration mode. The **nCFGEN** signal is routed between all FPGAs in the system through the HDRB connectors. In configuration mode all FPGAs and PLDs are connected to the scan chain so that they can be configured by the JTAG equipment.

Appendix A
Signal Descriptions

This index provides a summary of signals present on the Interface Module main connectors. It contains the following sections:

A.1 Connector pinouts

This section describes the pinouts and signals for the interface connectors:

A.1.1 HDRX tile connector

Table A-1 shows the signals on HDRX. Figure A-1 shows the Samtec connector pin arrangement.

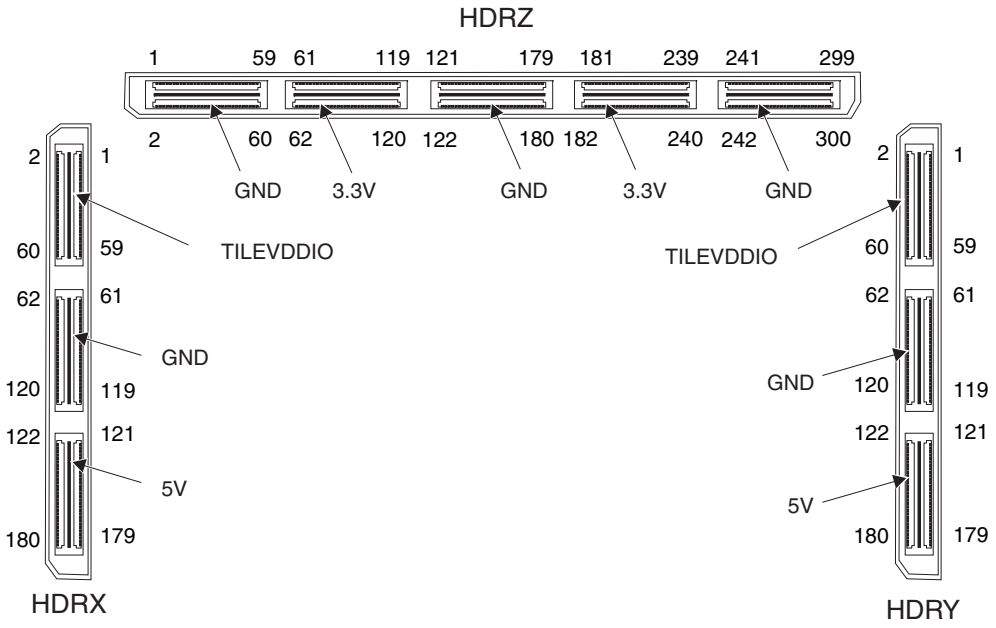


Figure A-1 HDRX, HDRY, and HDRZ connectors

Table A-1 HDRX (J2) pinout

Signal	Header pin number		Signal
NC	1	2	NC
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC

Table A-1 HDRX (J2) pinout (continued)

Signal	Header pin number		Signal
NC	17	18	NC
NC	19	20	NC
NC	21	22	NC
NC	23	24	NC
NC	25	26	NC
NC	27	28	NC
NC	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	NC
NC	37	38	NC
NC	39	40	NC
NC	41	42	NC
NC	43	44	NC
F31	45	46	NC
F30	47	48	NC
F29	49	50	**HDRID3**
F28	51	52	**HDRID2**
F27	53	54	**HDRID1**
F26	55	56	**HDRID0**
F25	57	58	**SLOCK3**
F24	59	60	**SLOCK2**
F23	61	62	**SLOCK1**
F22	63	64	**SREQ3**

Table A-1 HDRX (J2) pinout (continued)

Signal	Header pin number		Signal
F21	65	66	**SREQ2**
F20	67	68	**SREQ1**
F19	69	70	**SGNT3**
F18	71	72	**SGNT2**
F17	73	74	**SGNT1**
F16	75	76	**SYS_nIRQ3**
F15	77	78	**SYS_nIRQ2**
F14	79	80	**SYS_nIRQ1**
F13	81	82	**SYS_nFIQ3**
F12	83	84	**SYS_nFIQ2**
F11	85	86	**SYS_nFIQ1**
F10	87	88	**nPRES3**
F9	89	90	**nPRES2**
F8	91	92	**nPRES1**
F7	93	94	**X43** (to J12)
F6	95	96	**X42** (to J11)
F5	97	98	**X41** (to J11)
F4	99	100	NC
F3	101	102	NC
F2	103	104	**X38** (to J12)
F1	105	106	**X37** (to J12)
F0	107	108	**X36** (to J12)
NC	109	110	**X35** (to J12)
NC	111	112	**X34** (to J12)
NC	113	114	**X33** (to J12)

Table A-1 HDRX (J2) pinout (continued)

Signal	Header pin number		Signal
NC	115	116	**X32** (to J12)
NC	117	118	**X31** (to J12)
NC	119	120	**X30** (to J12)
NC	121	122	**X29** (to J12)
NC	123	124	**X28** (to J12)
NC	125	126	**X27** (to J12)
NC	127	128	**X26** (to J12)
NC	129	130	**X25** (to J12)
NC	131	132	**X24** (to J12)
NC	133	134	**X23** (to J12)
NC	135	136	**X22** (to J12)
NC	137	138	**X21** (to J12)
NC	139	140	**X20** (to J12)
NC	141	142	**X19** (to J11)
NC	143	144	**X18** (to J11)
NC	145	146	**X17** (to J11)
NC	147	148	**X16** (to J11)
NC	149	150	**X15** (to J11)
NC	151	152	**X14** (to J11)
NC	153	154	**X13** (to J11)
NC	155	156	**X12** (to J11)
NC	157	158	**X11** (to J11)
NC	159	160	**X10** (to J11)
NC	161	162	**X9** (to J11)

Table A-1 HDRX (J2) pinout (continued)

Signal	Header pin number		Signal
NC	163	164	**X8** (to J11)
NC	165	166	**X7** (to J11)
NC	167	168	**X6** (to J11)
NC	169	170	**X5** (to J11)
NC	171	172	**X4** (to J11)
NC	173	174	**X3** (to J11)
NC	175	176	**X2** (to J11)
NC	177	178	**X1** (to J11)
NC	179	180	**X0** (to J11)

A.1.2 HDRY tile connector

Table A-1 shows the signals on HDRY. Figure A-1 on page A-3 shows the connector pin arrangement.

Table A-1 HDRY (J1) pinout

Signal	Header pin number		Signal
NC	1	2	NC
NC	3	4	NC
NC	5	6	NC
NC	7	8	NC
NC	9	10	NC
NC	11	12	NC
NC	13	14	NC
NC	15	16	NC
NC	17	18	NC
NC	19	20	NC
NC	21	22	NC
NC	23	24	NC
NC	25	26	NC
NC	27	28	NC
NC	29	30	NC
NC	31	32	NC
NC	33	34	NC
NC	35	36	NC
NC	37	38	NC
NC	39	40	NC
NC	41	42	NC

Table A-1 HDRY (J1) pinout (continued)

Signal	Header pin number		Signal
NC	43	44	NC
NC	45	46	NC
NC	47	48	NC
NC	49	50	NC
NC	51	52	NC
NC	53	54	NC
NC	55	56	NC
NC	57	58	NC
LED7	59	60	NC
LED6	61	62	NC
LED5	63	64	NC
LED4	65	66	NC
LED3	67	68	NC
LED2	69	70	NC
LED1	71	72	NC
LED0	73	74	NC
SW7	75	76	NC
SW6	77	78	NC
SW5	79	80	NC
SW4	81	82	NC
SW3	83	84	**SREQ0**
SW2	85	86	**SLOCK0**
SW1	87	88	**SGNT0**
SW0	89	90	**SYS_nIRQ0**

Table A-1 HDRY (J1) pinout (continued)

Signal	Header pin number		Signal
NC	91	92	**SYS_nFIQ0**
NC	93	94	**HMASTER2**
NC	95	96	**HMASTER1**
NC	97	98	**HMASTER0**
NC	99	100	**IM_HCLK_T**
NC	101	102	**DIMM_HCLK4_T**
NC	103	104	**DIMM_HCLK3_T**
NC	105	106	**DIMM_HCLK2_T**
NC	107	108	**DIMM_HCLK1_T**
NC	109	110	NC
NC	111	112	NC
NC	113	114	NC
NC	115	116	NC
NC	117	118	NC
NC	119	120	NC
NC	121	122	NC
NC	123	124	NC
NC	125	126	NC
NC	127	128	NC
NC	129	130	NC
NC	131	132	NC
NC	133	134	NC
NC	135	136	NC
NC	137	138	NC

Table A-1 HDRY (J1) pinout (continued)

Signal	Header pin number		Signal
NC	139	140	NC
NC	141	142	NC
NC	143	144	NC
NC	145	146	NC
NC	147	148	NC
NC	149	150	NC
NC	151	152	NC
NC	153	154	NC
NC	155	156	NC
NC	157	158	NC
NC	159	160	NC
NC	161	162	NC
NC	163	164	NC
NC	165	166	NC
NC	167	168	NC
NC	169	170	NC
NC	171	172	NC
NC	173	174	NC
NC	175	176	NC
NC	177	178	NC
NC	179	180	NC

A.1.3 HDRZ tile connector

Table A-1 shows the signals on HDRZ. Figure A-1 on page A-3 shows the connector pin arrangement.

Table A-1 HDRZ (J3) pinout

Signal	Header pin number		Signal
IM_ABANK61	1	2	**IM_BBANK61**
IM_ABANK60	3	4	**IM_BBANK60**
IM_ABANK59	5	6	**IM_BBANK59**
IM_ABANK58	7	8	**IM_BBANK58**
IM_ABANK57	9	10	**IM_BBANK57**
IM_ABANK56	11	12	**IM_BBANK56**
IM_ABANK55	13	14	**IM_BBANK55**
IM_ABANK54	15	16	**IM_BBANK54**
IM_ABANK53	17	18	**IM_BBANK53**
IM_ABANK52	19	20	**IM_BBANK52**
IM_ABANK51	21	22	**IM_BBANK51**
IM_ABANK50	23	24	**IM_BBANK50**
IM_ABANK49	25	26	**IM_BBANK49**
IM_ABANK48	27	28	**IM_BBANK48**
IM_ABANK47	29	30	**IM_BBANK47**
IM_ABANK46	31	32	**IM_BBANK46**
IM_ABANK45	33	34	**IM_BBANK45**
IM_ABANK44	35	36	**IM_BBANK44**
IM_ABANK43	37	38	**IM_BBANK43**
IM_ABANK42	39	40	**IM_BBANK42**
IM_ABANK41	41	42	**IM_BBANK41**
IM_ABANK40	43	44	**IM_BBANK40**

Table A-1 HDRZ (J3) pinout (continued)

Signal	Header pin number		Signal
IM_ABANK39	45	46	**IM_BBANK39**
IM_ABANK38	47	48	**IM_BBANK38**
IM_ABANK37	49	50	**IM_BBANK37**
IM_ABANK36	51	52	**IM_BBANK36**
IM_ABANK35	53	54	**IM_BBANK35**
IM_ABANK34	55	56	**IM_BBANK34**
IM_ABANK33	57	58	**IM_BBANK33**
IM_ABANK32	59	60	**IM_BBANK32**
IM_ABANK31	61	62	**IM_BBANK31**
IM_ABANK30	63	64	**IM_BBANK30**
IM_ABANK29	65	66	**IM_BBANK29**
IM_ABANK28	67	68	**IM_BBANK28**
IM_ABANK27	69	70	**IM_BBANK27**
IM_ABANK26	71	72	**IM_BBANK26**
IM_ABANK25	73	74	**IM_BBANK25**
IM_ABANK24	75	76	**IM_BBANK24**
IM_ABANK23	77	78	**IM_BBANK23**
IM_ABANK22	79	80	**IM_BBANK22**
IM_ABANK21	81	82	**IM_BBANK21**
IM_ABANK20	83	84	**IM_BBANK20**
IM_ABANK19	85	86	**IM_BBANK19**
IM_ABANK18	87	88	**IM_BBANK18**
IM_ABANK17	89	90	**IM_BBANK17**
IM_ABANK16	91	92	**IM_BBANK16**
IM_ABANK15	93	94	**IM_BBANK15**

Table A-1 HDRZ (J3) pinout (continued)

Signal	Header pin number		Signal
IM_ABANK14	95	96	**IM_BBANK14**
IM_ABANK13	97	98	**IM_BBANK13**
IM_ABANK12	99	100	**IM_BBANK12**
IM_ABANK11	101	102	**IM_BBANK11**
IM_ABANK10	103	104	**IM_BBANK10**
IM_ABANK9	105	106	**IM_BBANK9**
IM_ABANK8	107	108	**IM_BBANK8**
IM_ABANK7	109	110	**IM_BBANK7**
IM_ABANK6	111	112	**IM_BBANK6**
IM_ABANK5	113	114	**IM_BBANK5**
IM_ABANK4	115	116	**IM_BBANK4**
IM_ABANK3	117	118	**IM_BBANK3**
IM_ABANK2	119	120	**IM_BBANK2**
IM_ABANK1	121	122	**IM_BBANK1**
IM_ABANK0	123	124	**IM_BBANK0**
NC	125	126	NC
NC	127	128	NC
nSRST	129	130	NC
nTRST	131	132	NC
TILE_D_TDO	133	134	NC
TILE_D_TDI	135	136	NC
TILE_D_TCK	137	138	**EXPIM_CLK1**
TILE_D_TMS	139	140	**SYSCLK1**
TILE_RTCK	141	142	**SYSCLK2**
nSRST	143	144	NC

Table A-1 HDRZ (J3) pinout (continued)

Signal	Header pin number		Signal
FPGA_nPROG	145	146	NC
TILE_C_TDO	147	148	NC
TILE_C_TDI	149	150	**CLK_GLOBAL**
TILE_C_TCK	151	152	**FPGA_IMAGE**
TILE_C_TMS	153	154	**nSYSPOR**
NC	155	156	**nSYSRST**
nCFGEN	157	158	**nRTCKEN**
GLOBAL_DONE	159	160	NC
NC	161	162	NC
NC	163	164	NC
NC	165	166	NC
NC	167	168	NC
NC	169	170	NC
NC	171	172	NC
C31	173	174	**B0**
C30	175	176	**B1**
C29	177	178	**B2**
C28	179	180	**B3**
C27	181	182	**B4**
C26	183	184	**B5**
C25	185	186	**B6**
C24	187	188	**B7**
C23	189	190	**B8**
C22	191	192	**B9**
C21	193	194	**B10**

Table A-1 HDRZ (J3) pinout (continued)

Signal	Header pin number		Signal
C20	195	196	**B11**
C19	197	198	**B12**
C18	199	200	**B13**
C17	201	202	**B14**
C16	203	204	**B15**
C15	205	206	**B16**
C14	207	208	**B17**
C13	209	210	**B18**
C12	211	212	**B19**
C11	213	214	**B20**
C10	215	216	**B21**
C9	217	218	**B22**
C8	219	220	**B23**
C7	221	222	**B24**
C6	223	224	**B25**
C5	225	226	**B26**
C4	227	228	**B27**
C3	229	230	**B28**
C2	231	232	**B29**
C1	233	234	**B30**
C0	235	236	**B31**
D31	237	238	**A0**
D30	239	240	**A1**
D29	241	242	**A2**
D28	243	244	**A3**

Table A-1 HDRZ (J3) pinout (continued)

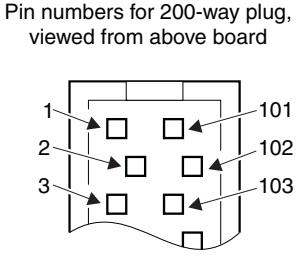
Signal	Header pin number		Signal
D27	245	246	**A4**
D26	247	248	**A5**
D25	249	250	**A6**
D24	251	252	**A7**
D23	253	254	**A8**
D22	255	256	**A9**
D21	257	258	**A10**
D20	259	260	**A11**
D19	261	262	**A12**
D18	263	264	**A13**
D17	265	266	**A14**
D16	267	268	**A15**
D15	269	270	**A16**
D14	271	272	**A17**
D13	273	274	**A18**
D12	275	276	**A19**
D11	277	278	**A20**
D10	279	280	**A21**
D9	281	282	**A22**
D8	283	284	**A23**
D7	285	286	**A24**
D6	287	288	**A25**
D5	289	290	**A26**
D4	291	292	**A27**
D3	293	294	**A28**

Table A-1 HDRZ (J3) pinout (continued)

Signal	Header pin number		Signal
D2	295	296	**A29**
D1	297	298	**A30**
D0	299	300	**A31**

A.1.4 HDRA Integrator connector

Figure A-2 shows the pin numbers of the HDRA socket on the underside of the Interface Module (viewed from above, through the board).



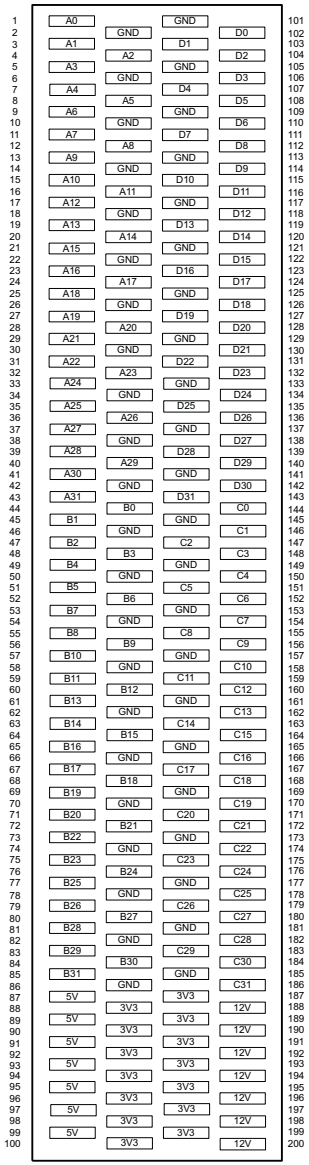


Figure A-2 HDRA socket pin numbering

The signals are described in Table A-1.

Table A-1 Bus bit assignment

Pin label	Signal	Description
A[31:0]	**HADDR[31:0]**	System address bus
B[31:0]	Not used	-
C[31:16]	Not used	-
C15	**HMASTLOCK**	Locked transaction
C14	**HRESP1**	Slave response
C13	**HRESP0**	Slave response
C12	**HREADY**	Slave wait response
C11	**HWRITE**	Write transaction
C10	**HPROT2**	Transaction protection type
C[9:8]	**HPROT[1:0]**	Transaction protection type
C[7:5]	**HBURST[2:0]**	Transaction burst size
C4	**HPROT[3]**	Transaction protection type
C[3:2]	**HSIZE[1:0]**	Transaction width
C[1:0]	**HTRAN[1:0]**	Transaction type
D[31:0]	**HDATA[31:0]**	System data bus

A.1.5 HDRB Integrator connector

Figure A-3 shows the pin numbers of the HDRB socket on the underside of the Interface Module (viewed from above, through the board).

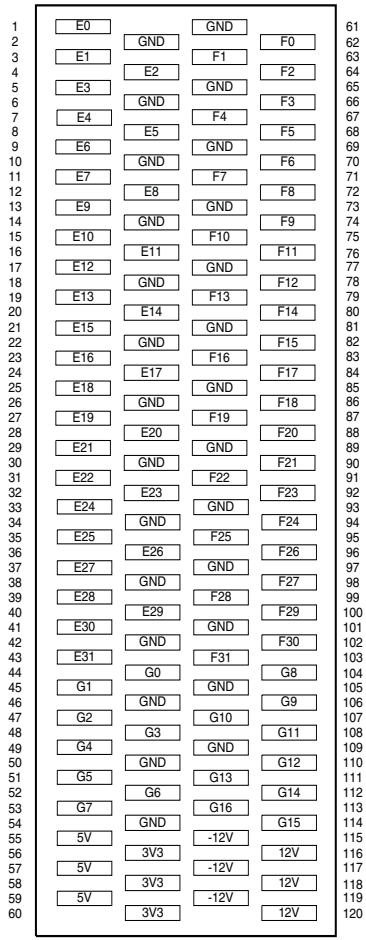


Figure A-3 HDRB socket pin numbering

HDRB signal descriptions

Table A-1 and Table A-1 describe the signals for an AMBA AHB system bus on the core module position and the expansion position of an Integrator motherboard. (The function of some pin positions differ depending on whether the module is placed on the core module position or the expansion position. The Interface Module will typically be used in the expansion position and used to develop peripheral logic.)

Table A-1 HDRB signal description (AHB core module)

Pin label	Name	Description
E[31:28]	**SYSCLK[3:0]**	System clock.
E[27:24]	**nPPRES[3:0]**	Processor module present.
E[23:20]	**nIRQ[3:0]**	Interrupt request to processors 3, 2, 1, and 0 respectively.
E[19:16]	**nFIQ[3:0]**	Fast interrupt requests to processors 3, 2, 1, and 0 respectively.
E[15:12]	**HDRID[3:0]**	Core tile stack position indicator.
E[11:8]	**HLOCK[3:0]**	System bus lock from processor 3, 2, 1, and 0 respectively.
E[7:4]	**HGRANT[3:0]**	System bus grant to processor 3, 2, 1, and 0 respectively.
E[3:0]	**HBUSREQ[3:0]**	System bus request from processors 3, 2, 1, and 0 respectively.
F[31:0]	**GPIO[31:0]**	GPIO to system controller.
G16	**nRTCKEN**	RTCK AND gate enable.
G[15:14]	**CFGSEL[1:0]**	FPGA configuration select.
G13	**nCFGEN**	Sets motherboard into configuration mode.
G12	**nSRST**	Multi-ICE reset (open collector).
G11	**FPGADONE**	Indicates when FPGA configuration is complete (open collector).
G10	**RTCK**	Returned JTAG test clock.
G9	**nSYSRST**	Buffered system reset.
G8	**nTRST**	JTAG reset.

Table A-1 HDRB signal description (AHB core module) (continued)

Pin label	Name	Description
G7	**TDO**	JTAG test data out.
G6	**TDI**	JTAG test data in.
G5	**TMS**	JTAG test mode select.
G4	**TCK**	JTAG test clock.
G[3:1]	**MASTER[2:0]**	Master ID. Binary encoding of the master currently performing a transfer on the bus. Corresponds to the tile ID and to the **HBUSREQ** and **HGRANT** line numbers.
G0	**nMBDET**	Motherboard detect pin.

Table A-2 EXPB signal description (AHB expansion)

Pin label	Name	Description
E[31:28]	**SYSCLK[3:0]**	System clock Logic Tile.
E[27:24]	**nEPRES[3:0]**	Expansion module present.
E[23:20]	**nIRQSRC[3:0]**	Interrupt from expansion module 3, 2, 1, and 0 respectively.
E[19:16]	NC	Not connected
E[15:12]	**HDRID[3:0]**	Expansion module stack position indicator.
E[11:8]	**HLOCK[3:0]**	System bus lock from expansion position 3, 2, 1, and 0 respectively.
E[7:4]	**HGRANT[3:0]**	System bus grant to expansion position 3, 2, 1, and 0 respectively.
E[3:0]	**HBUSREQ[3:0]**	System bus request from expansion position 3, 2, 1, and 0 respectively.
F[31:0]	**GPIO[31:0]**	GPIO to system controller.
G16	**EXP_nRTCKEN**	RTCK AND gate enable.
G[15:14]	**CFGSEL[1:0]**	FPGA configuration select.
G13	**EXP_nCFGEN**	Sets expansion module stack into configuration mode.

Table A-2 EXPB signal description (AHB expansion) (continued)

Pin label	Name	Description
G12	**nSRST**	Multi-ICE reset (open collector).
G11	**FPGADONE**	Indicates when FPGA configuration is complete (open collector).
G10	**RTCK**	Returned JTAG test clock.
G9	**nSYSRST**	Buffered system reset.
G8	**EXP_nTRST**	JTAG reset.
G7	**EXP_TDO**	JTAG test data out.
G6	**EXP_TDI**	JTAG test data in.
G5	**EXP_TMS**	JTAG test mode select.
G4	**EXP_TCK**	JTAG test clock.
G[3:1]	**MASTER[2:0]**	Master ID. Binary encoding of the master currently performing a transfer on the bus. Corresponds to the tile ID and to the **HBUSREQ** and **HGRANT** line numbers.
G0	**nMBDET**	Motherboard detect pin.

Note

The pin labels in Table A-1 on page A-22 and Table A-2 on page A-23 refer to Figure A-3 on page A-21. The Integrator/AP uses different pin labeling for the expansion connector EXPB.

A.1.6 EXPIM Integrator connector

This connector is the same type as HDRA. Figure A-4 shows the pin numbers for EXPIM socket (viewed from above, through the board).

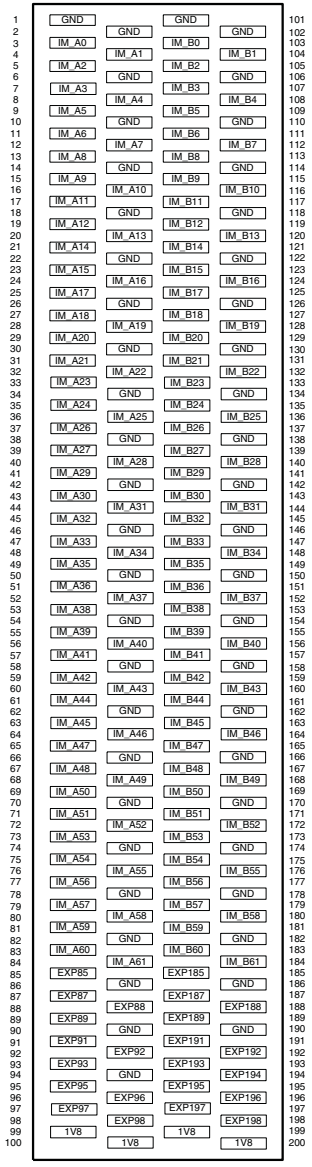


Figure A-4 EXPIM socket pin numbering

This connector provides expansion connections to the Logic Tile. Table A-1 shows the signals for the EXPIM connector.

Table A-1 EXPIM signal description

Label	Signal	Description
IM_A[61:0]	**IM_ABANK[61:0]**	I/O pins
IM_B[61:0]	**IM_BBANK[61:0]**	I/O pins
EXP189	**EXPIM_CLK1**	Clock signal from a logic module below and passed to Logic Tile above

A.1.7 Analyzer port connectors

The analyzer connectors pins are connected to signals on the HDRX connector and to the JTAG signals. These connectors can be used to monitor signals from custom logic in an external Logic Tile.

Table A-1 shows the pinout of the analyzer port connector J11.

Table A-1 Analyzer connector A (J11)

Signal	Pin		Signal
NC	1	2	NC
NC	3	4	NC
NC	5	6	**X41**
NC	7	8	NC
NC	9	10	NC
TDO	11	12	**TILE_VDDIO**
RTCK	13	14	**3V3**
TCK	15	16	**X7**
TMS	17	18	**X6**
TDI	19	20	**X5**
nTRST	21	22	**X4**
X15	23	24	**X3**
X14	25	26	**X2**
X13	27	28	**X1**
X12	29	30	**X0**
X11	31	32	**X19**
X10	33	34	**X18**
X9	35	36	**X17**
X8	37	38	**X16**

Table A-2 shows the pinout of the analyzer port connector J12.

Table A-2 Analyzer connector B (J12)

Signal	Pin	Pin	Signal
NC	1	2	NC
NC	3	4	NC
NC	5	6	**X43**
NC	7	8	NC
NC	9	10	NC
NC	11	12	**TILE_VDDIO**
NC	13	14	**3V3**
NC	15	16	**X27**
NC	17	18	**X26**
NC	19	20	**X25**
NC	21	22	**X24**
X35	23	24	**X23**
X34	25	26	**X22**
X33	27	28	**X21**
X32	29	30	**X20**
X31	31	32	**X39**
X30	33	34	**X38**
X29	35	36	**X37**
X28	37	38	**X36**

Figure A-5 shows the pinout of the analyzer port connector J11.

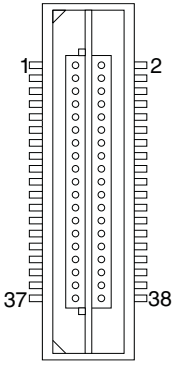


Figure A-5 Analyzer connector pin numbering

A.2 Electrical specification

This section provides details of the voltage and current characteristics for the Interface Module.

A.2.1 Bus interface characteristics

Table A-1 shows the Interface Module electrical characteristics. The Interface Module uses 3.3V and 5V sources. The 12V inputs are supplied by the motherboard but not used by the Interface Module or tile.

Table A-1 Interface electrical characteristics

Symbol	Description	Min	Max	Unit
3V3	Supply voltage (interface signals)	3.1	3.5	V
5V	Supply voltage	4.75	5.25	V
V_{IH}	High-level input voltage	2.0	3.6	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage	2.4	-	V
V_{OL}	Low-level output voltage	-	0.4	V
C_{IN}	Input capacitance	-	20	pF

A.2.2 Current requirements

Table A-2 on page A-31 shows the current requirements at room temperature and nominal voltage. These measurements include the current drawn by Multi-ICE, which is approximately 160mA at 3.3V.

The power blades on the header connectors are rated for 9A. This typically can supply up to six Logic Tiles. The clock frequencies, however, might have to be reduced if you are using this many tiles.

Caution

The actual current depends on the complexity of the design in the Logic Tile and the clock speed used for the system.

Do not add or remove tiles while power is connected to the Interface Module.

Table A-2 Current requirements

System	At 3.3V	At 5V
Example 1, standalone operation (Interface Module and one tile)	180mA	20mA
Example 2, motherboard, Interface Module, and one tile	1.2A	600mA

A.3 Mechanical details

The Interface Module is designed to be stacked on a motherboard (Integrator/AP or Integrator/CP for example).

Figure A-1 and Figure A-2 on page A-33 shows the header locations.

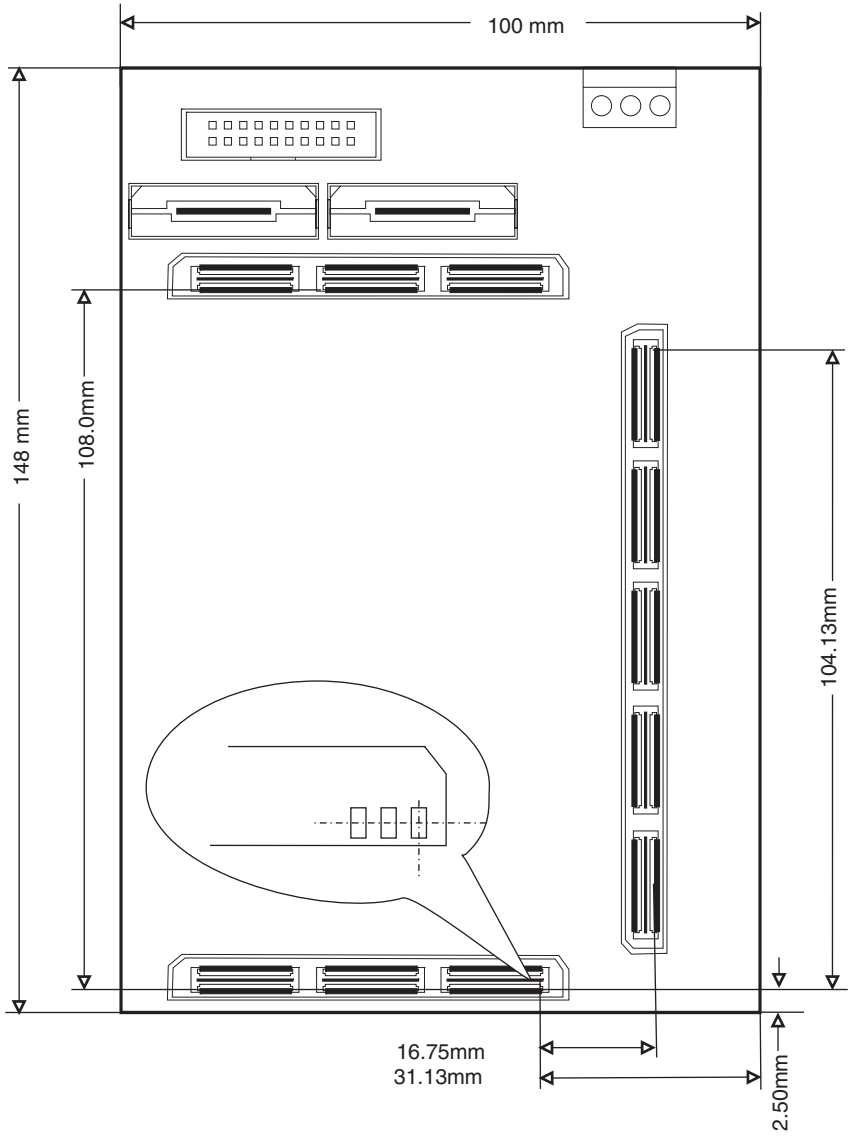
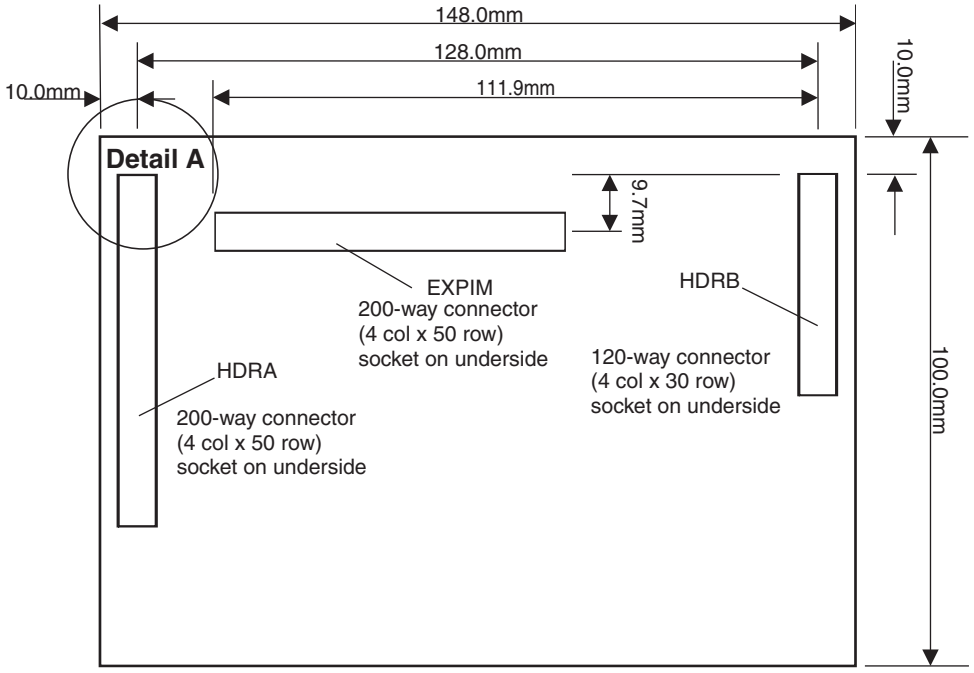


Figure A-1 HDRX, HDRY, and HDRZ location



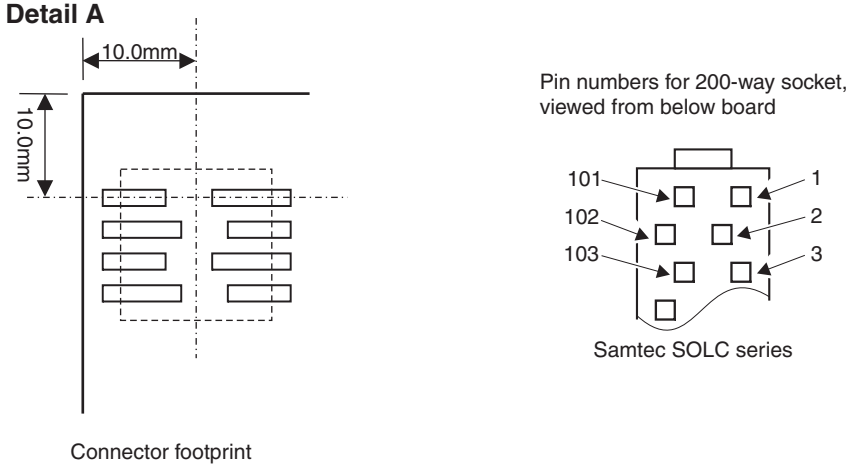


Figure A-2 HDRA and HDRB location (looking through the board)

Index

The items in this index are listed in alphabetical order, with symbols and numerics appearing at the end. The references given are to page numbers.

M

N

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S

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U

