CoreTile Express™ A5x2

Cortex™-A5 MPCore (V2P-CA5s)

Technical Reference Manual

ARM®

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CoreTile Express A5x2
Technical Reference Manual

Release Information

The following changes have been made to this book.

Change history

Date	Issue	Confidentiality	Change
28 March 2011	A	Non-Confidential	First release
14 August 2012	B	Non-Confidential	Second release
31 March 2013	C	Non-Confidential	Third release

Proprietary Notice

Confidentiality Status

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Product Status

The information in this document is final, that is for a developed product.

Web Address

`http://www.arm.com`

Conformance Notices

This section contains conformance notices.

Federal Communications Commission Notice

This device is test equipment and consequently is exempt from part 15 of the FCC Rules under section 15.103 (c).

CE Declaration of Conformity

CE

The system should be powered down when not in use.

The daughterboard generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures:

- Ensure attached cables do not lie across the card.
- Reorient the receiving antenna.
- Increase the distance between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Note

It is recommended that wherever possible shielded interface cables be used.

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Preface

This preface introduces the *CoreTile Express A5x2 Technical Reference Manual*. It contains the following sections:

- *About this book* on page vii
- *Feedback* on page xi.

About this book

This book is for the CoreTile Express A5x2 daughterboard.

Intended audience

This document is written for experienced hardware and software developers to aid the development of ARM-based products using the CoreTile Express A5x2 daughterboard with the Motherboard Express µATX as part of a development system.

Using this book

This book is organized into the following chapters:

Chapter 1 *Introduction*

Read this for an introduction to the CoreTile Express A5x2 daughterboard.

Chapter 2 *Hardware Description*

Read this for a description of the hardware present on the daughterboard.

Chapter 3 *Programmers Model*

Read this for a description of the configuration registers present on the daughterboard.

Appendix A *Signal Descriptions*

Read this for a description of the signals present on the daughterboard.

Appendix B *HDLCD controller*

Read this for a description of the HDLCD controller in the Cortex-A5 test chip.

Appendix C *Electrical Specifications*

Read this for a description of the electrical specifications of the daughterboard.

Appendix D *Revisions*

Read this for a description of the technical changes between released issues of this book.

Glossary

The *ARM Glossary* is a list of terms used in ARM documentation, together with definitions for those terms. The *ARM Glossary* does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See *ARM Glossary*, `http://infocenter.arm.com/help/topic/com.arm.doc.aeg0014-/index.html`.

Conventions

This book uses the conventions that are described in:

- *Typographical conventions* on page viii.
- *Timing diagrams* on page viii.
- *Signals* on page ix.

Typographical conventions

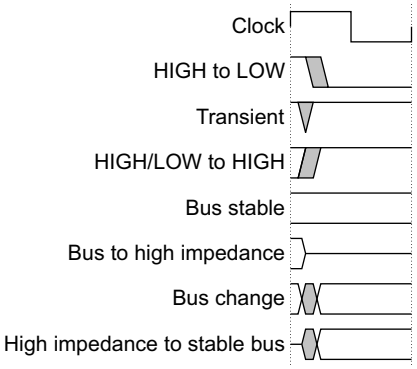
The following table describes the typographical conventions:

Style	Purpose
italic	Introduces special terminology, denotes cross-references, and citations.
bold	Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.
`monospace`	Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.
`mono`space	Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.
`monospace` *`italic`*	Denotes arguments to monospace text where the argument is to be replaced by a specific value.
`monospace bold`	Denotes language keywords when used outside example code.
<and>	Encloses replaceable terms for assembler syntax where they appear in code or code fragments. For example: `MRC p15, 0 <Rd>, <CRn>, <CRm>, <Opcode_2>`
SMALL CAPITALS	Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

Timing diagrams

The figure named *Key to timing diagram conventions* explains the components used in timing diagrams. Variations, when they occur, have clear labels. You must not assume any timing information that is not explicit in the diagrams.

Shaded bus and signal areas are UNDEFINED, so the bus or signal can assume any value within the shaded area at that time. The actual level is unimportant and does not affect normal operation.



Key to timing diagram conventions

Timing diagrams sometimes show single-bit signals as HIGH and LOW at the same time and they look similar to the bus change shown in *Key to timing diagram conventions*. If a timing diagram shows a single-bit signal in this way then its value does not affect the accompanying description.

Signals

The signal conventions are:

Signal level The level of an asserted signal depends on whether the signal is active-HIGH or active-LOW. Asserted means:
- HIGH for active-HIGH signals
- LOW for active-LOW signals.

Lower-case n At the start or end of a signal name denotes an active-LOW signal.

Additional reading

This section lists publications by ARM and by third parties.

See Infocenter, http://infocenter.arm.com, for access to ARM documentation.

ARM publications

This book contains information that is specific to this product. See the following documents for other relevant information:

- *Motherboard Express™ µATX Technical Reference Manual* (ARM DUI 0447)
- *Versatile Express Configuration Guide* (ARM DDI 0496)
- *Programmer Module (V2M-CP1)* (ARM DDI 0495)
- *LogicTile Express™ 3MG Technical Reference Manual* (ARM DUI 0449)
- *LogicTile Express™ 13MG Technical Reference Manual* (ARM DUI 0556)
- *Versatile Express™ Boot Monitor Technical Reference Manual* (ARM DUI 0465)
- *Cortex™-A5 MPCore™ Technical Reference Manual* (ARM DDI 0434)
- *AMBA® Network Interconnect (NIC-301) Technical Reference Manual* (ARM DDI 0397)
- *ARM PrimeCell™ DDR2 Dynamic Memory Controller (PL341) Technical Reference Manual* (ARM DDI 0418)
- *ARM PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual* (ARM DDI 0380)
- *AMBA Level 2 Cache Controller (L2C-310) Technical Reference Manual* (ARM DDI 0246)
- *ARM PrimeCell External Bus Interface (PL220) Technical Reference Manual* (ARM DDI 0249).

The following publications provide information about related ARM products and toolkits:

- *ARM®DSTREAM® System and Interface Design Reference* (ARM DUI 0449)
- *ARM®DSTREAM® Setting up the Hardware* (ARM DUI 0481)
- *ARM® DSTREAM® and RVI® Using the Debug Hardware Configuration Utilities* (ARM DUI 0498)
- *ARM CoreSight™ ETM™-A5 Technical Reference Manual* (ARM DDI 0435)

- *ARM CoreSight Components Technical Reference Manual* (ARM DDI 0314)
- Application note AN243, *Example LogicTile Express 3MG design for a CoreTile Express A5x2*.

Other publications

This section lists relevant documents published by third parties:

- See the JEDEC Solid State Technology Association web site, www.jedec.org for information on *Small Outline Dual In-line Memory Modules* (SO-DIMM).

Feedback

ARM welcomes feedback on this product and its documentation.

Feedback on this product

If you have any comments or suggestions about this product, contact your supplier and give:

- The product name.
- The product revision or version.
- An explanation with as much information as you can provide. Include symptoms and diagnostic procedures if appropriate.

Feedback on content

If you have comments on content then send an e-mail to `errata@arm.com`. Give:

- The title.
- The number, DUI 0541C.
- The page numbers to which your comments apply.
- A concise explanation of your comments.

ARM also welcomes general suggestions for additions and improvements.

Chapter 1
Introduction

This chapter provides an introduction to the CoreTile Express A5x2 daughterboard. It contains the following sections:

- *About the CoreTile Express A5x2 daughterboard* on page 1-2
- *Precautions* on page 1-4.

1.1 About the CoreTile Express A5x2 daughterboard

The CoreTile Express A5x2 daughterboard is designed as a platform for developing systems based on *Advanced Microcontroller Bus Architecture* (AMBA®) that use the *Advanced eXtensible Interface* (AXI™) or custom logic for use with ARM cores.

You can use the CoreTile Express A5x2 daughterboard to create prototype systems.

Note

The CoreTile Express A5x2 daughterboard must be used with a Motherboard Express µATX. See the *Motherboard Express µATX Technical Reference Manual* for information about interconnection.

The daughterboard comprises the following hardware and interfaces:

- Cortex-A5 MPCore test chip with NEON, FPU, and Jazelle support. The test chip is a structured ASIC that operates at lower speeds than a full ASIC. The default speed is 100MHz. It contains:
  - Cortex-A5 MPCore cluster, consisting of two processor cores.
  - DDR2 interface, *Dynamic Memory Controller* (DMC), *Static Memory Controller* (SMC) interface to SRAM, flash and peripherals on the motherboard, HDLCD controller, and other on-chip peripherals. See *Cortex-A5 MPCore test chip* on page 2-4 and *Programmable peripherals and interfaces* on page 3-7.
- Daughterboard Configuration Controller.
- Multiplexed AMBA AXI master and slave buses to an optional LogicTile Express daughterboard.
- Serial configuration SPI Flash.
- Configuration EEPROM.
- Six programmable oscillators.
- 1 GB of external DDR2 64-bit memory using *Small Outline Dual In-Line Memory Module* (SO-DIMM).
- CoreSight software debug and 32-bit trace ports.
- HDRX header with one AMBA AXI master and one AMBA AXI slave bus that connect to the other daughterboard site.
- HDRY header with four buses to the motherboard.

Note

The Cortex-A5 test chip does not support TrustZone®.

Figure 1-1 on page 1-3 shows the layout of the daughterboard.

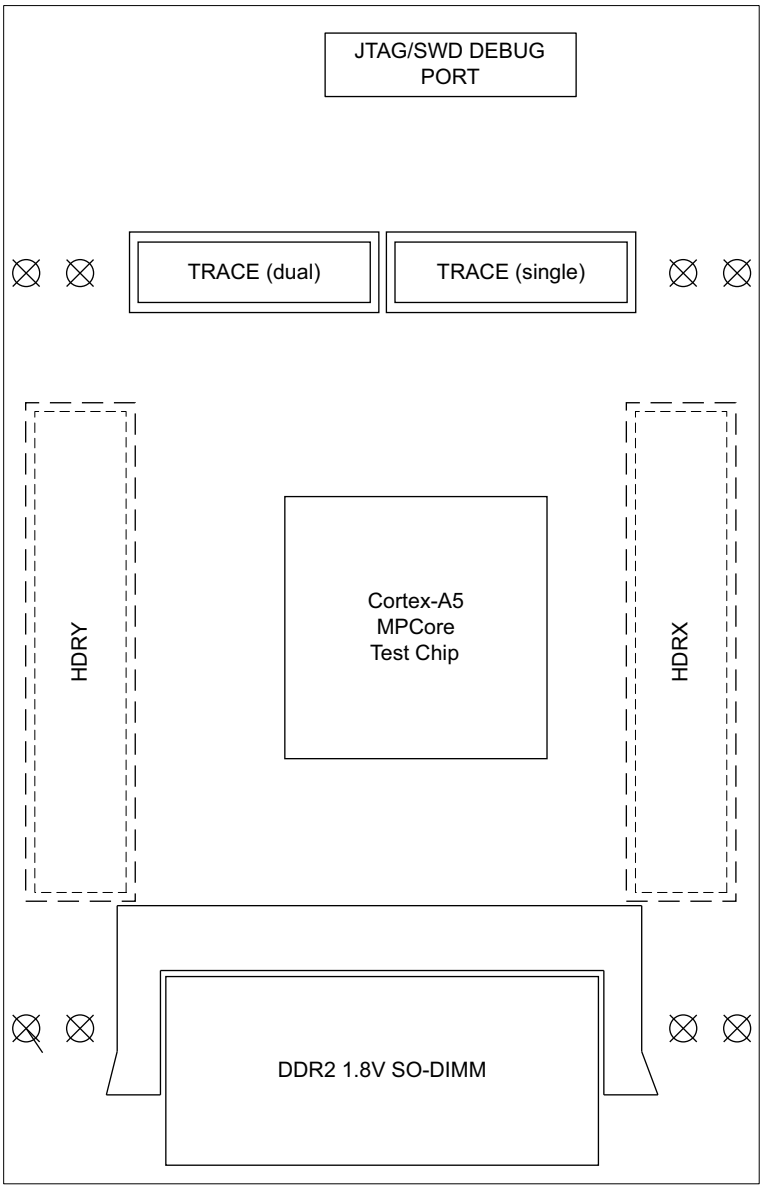


Figure 1-1 CoreTile Express A5x2 daughterboard layout

Note

The Cortex-A5 test chip is marked *Cortex-A5 MPCore, r0p1_RC0, ETM R0P1*

Note

The header connectors, HDRY and HDRX, shown as dashed lines in Figure 1-1, are on the lower face of the board, that is, the face that connects to the motherboard. The other components, shown as solid lines, are on the upper face of the board.

1.2 Precautions

This section contains advice about how to prevent damage to your daughterboard.

1.2.1 Ensuring safety

The daughterboard is supplied with a range of DC voltages. Power is supplied to the daughterboard through the header connectors.

Warning

Do not use the board near equipment that is sensitive to electromagnetic emissions, for example medical equipment.

1.2.2 Preventing damage

The daughterboard is intended for use within a laboratory or engineering development environment. It is supplied without an enclosure and this leaves the board sensitive to electrostatic discharges and permits electromagnetic emissions.

Caution

To avoid damage to the daughterboard, observe the following precautions.

- Never subject the board to high electrostatic potentials. Observe *ElectroStatic Discharge* (ESD) precautions when handling any board.
- Always wear a grounding strap when handling the board.
- Only hold the board by the edges.
- Avoid touching the component pins or any other metallic element.
- Do not use the board near a transmitter of electromagnetic emissions.

Chapter 2
Hardware Description

This chapter describes the hardware on the CoreTile Express A5x2 daughterboard. It contains the following sections:

- *Overview of the CoreTile Express A5x2 daughterboard* on page 2-2
- *Cortex-A5 MPCore test chip* on page 2-4
- *System interconnect signals* on page 2-5
- *Power-up configuration and resets* on page 2-8
- *Clocks* on page 2-15
- *Interrupts* on page 2-19
- *Serial configuration controller* on page 2-22
- *Temperature monitoring* on page 2-24
- *Debug* on page 2-25
- *DDR2 SO-DIMM memory interface* on page 2-27
- *HDLCD* on page 2-28.

2.1 Overview of the CoreTile Express A5x2 daughterboard

Figure 2-1 shows a block diagram of the daughterboard.

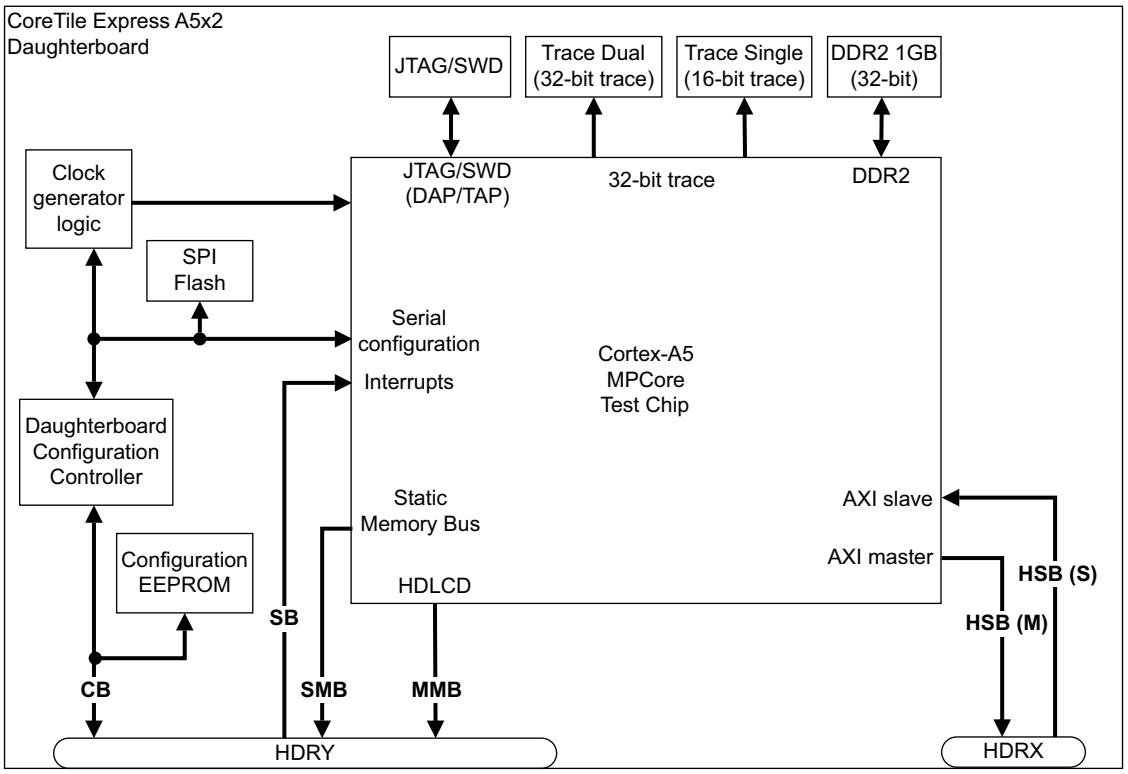


Figure 2-1 CoreTile Express A5x2 daughterboard block diagram

The daughterboard contains the following devices and interfaces:

Cortex-A5 MPCore test chip

The test chip includes the following components and interfaces:

- Cortex-A5 MPCore cluster.
- L2C-310 *Level 2 Cache Controller* (L2CC) consisting of 256KB of L2 unified cache.
- PL341 64-bit *Double Data Rate* 2 (DDR2) *Dynamic Memory Controller* (DMC) interface to the onboard 1GB DDR2 SO-DIMM.
- PL354 32-bit *Static Memory Bus* (SMB) controller, SMC.
- 24-bit *Color HDLCD* (CLCD) controller.
- Multiplexed 64-bit AXI master interface.
- Multiplexed 64-bit AXI slave interface.
- CoreSight debug and trace interface to the onboard connectors.
- Daughterboard Configuration Controller interface.

Daughterboard Configuration Controller

The Daughterboard Configuration Controller initiates, controls, and configures the test chip. It interfaces with the Motherboard Express µATX.

A *Motherboard Configuration Controller* (MCC) on the Motherboard Express µATX configures the daughterboard and communicates with the Daughterboard Configuration Controller to configure the test chip.

Configuration EEPROM

The daughterboard EEPROM contains information for identification and detection of the daughterboard and stores the filename of the SPI flash image and its file creation date.

DDR2 SO-DIMM

The daughterboard supports 1GB of 64-bit DDR2 SO-DIMM memory.

Clock generator logic

The daughterboard provides six on-board OSCCLKS to drive the CPU and internal AXI, AXIM, DDR2, SMC, and HDLCD interfaces.

CoreSight software debug and trace ports

The Cortex-A5 MPCore test chip CoreSight system supports both the SWD and JTAG protocols.

A 32-bit trace interface is provided through the standard dual 16-bit *Matched Impedance ConnecTOR* (MICTOR) connectors.

System interconnect buses

See *System interconnect signals* on page 2-5.

2.2 Cortex-A5 MPCore test chip

Figure 2-2 shows the main components of the test chip.

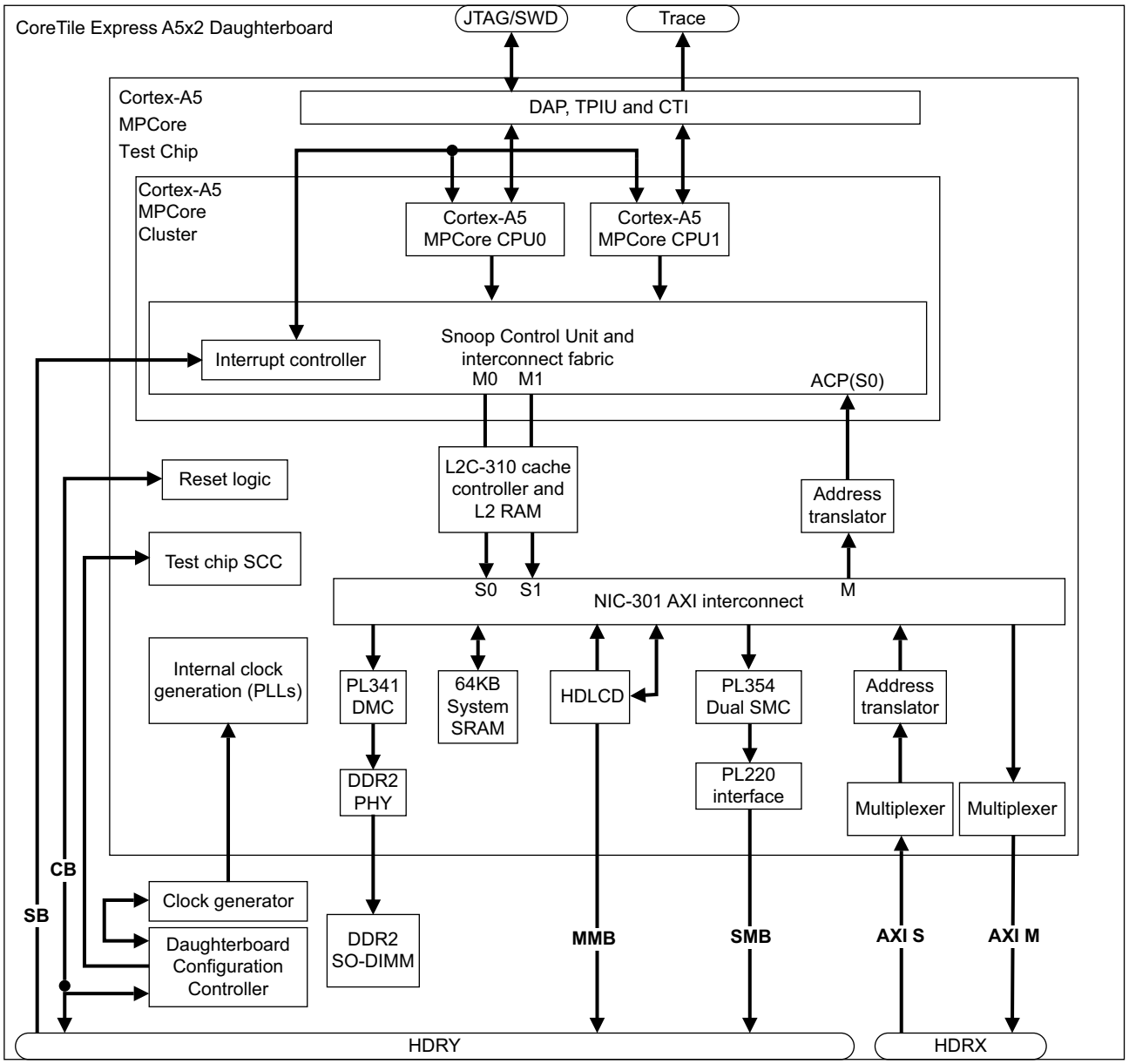


Figure 2-2 Top-level view of the Cortex-A5 MPCore test chip components

Note

Bus lines with single-headed arrows indicate the direction of control, not the direction of data flow. That is, each arrow points from bus master to bus slave.

2.3 System interconnect signals

This section provides an overview of the signals present on the header connectors.

Figure 2-3 shows the daughterboard system interconnect to the Motherboard Express µATX development system, and to an optional LogicTile Express 3MG FPGA daughterboard. For more information about the global interconnect scheme, see the *Motherboard Express µATX Technical Reference Manual*.

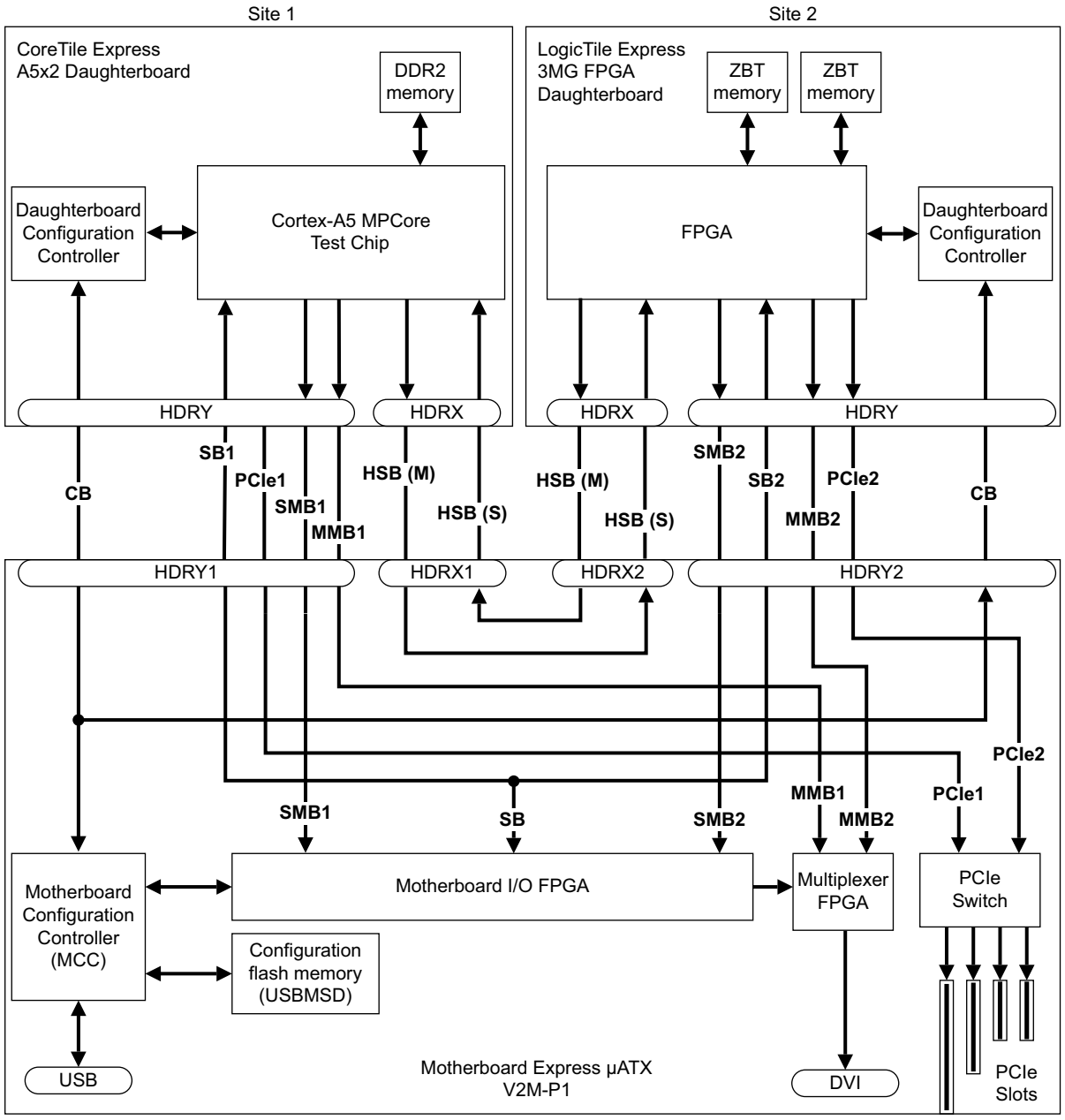


Figure 2-3 System connect example with optional LogicTile Express 3MG daughterboard

Note

- CoreTile Express daughterboards, including the CoreTile Express A5x2 daughterboard, are typically fitted in site 1. LogicTile Express daughterboards are typically fitted in site 2.

- Application note AN243, *Example LogicTile Express 3MG design for a CoreTile Express A5x2*, provided by ARM, implements an example AMBA system using the LogicTile Express 3MG daughterboard to interconnect with the CoreTile Express A5x2 daughterboard. See the documentation supplied on the accompanying media and the *Application Notes* listing for more information at, `http://infocenter.arm.com`.

2.3.1 High-Speed Buses (HSBs) to other daughterboard

The HSB link to the other daughterboard consists of the following buses between the Cortex-A5 MPCore test chip and the daughterboard fitted in the other site on the motherboard:

- A 64-bit multiplexed AXI master bus, HSB M, to the external AXI slave on the other daughterboard in Site 2.
- A 64-bit multiplexed AXI slave bus, HSB S, from the external AXI master on the other daughterboard in Site 2.

The HSB connection to the other daughterboard is through header HDRX on the daughterboard, dedicated headers HDRX1 and HDRX2 on the motherboard, and header HDRX on the other daughterboard.

For information about the multiplexing scheme for the AXI buses, see Appendix A *Signal Descriptions*.

Note

Application note AN243, *Example LogicTile Express 3MG design for a CoreTile Express A5x2*, provides an example AXI design implementing external multiplexed AXI master and slave buses at the HDRX header on the FPGA daughterboard in site 2.

2.3.2 *Static Memory Bus* (SMB)

The *Static Memory Bus* (SMB) connects the Cortex-A5 test chip SMC to the motherboard. You can use it to access the motherboard peripherals such as the NOR Flash, SRAM, Ethernet, USB, MMC, CF, KMI, CLCD, UARTs, and system registers.

2.3.3 *MultiMedia Bus* (MMB)

The *MultiMedia Bus* (MMB) consists of a video bus that connects the 24-bit RGB HDLCD controller directly to the motherboard MUXFPGA. The motherboard IOFPGA implements a CLCD controller. The motherboard MUXFPGA selects the source for the motherboard DVI connector from:

- The MMB bus from the CoreTile Express A5x2, that is, the 24-bit RGB from the HDLCD controller.
- The MMB bus from the LogicTile Express daughterboard in site 2.
- The CLCD controller in the motherboard IOFPGA.

2.3.4 *System Bus* (SB)

The *System Bus* (SB) connects 48 Interrupt lines from motherboard peripherals to the *Generic Interrupt Controller* (GIC) in the MPCore cluster in the test chip.

2.3.5 *Configuration Bus* (CB)

The Configuration Bus connects the Daughterboard Configuration Controller to the *Motherboard Configuration Controller* (MCC). The Daughterboard Configuration Controller configures the OSCCLKS, SPI Flash, Cortex-A5 test chip SCC, PLLs, and registers. The SPI Flash configures the test chip using dedicated configuration logic in the test chip. The Daughterboard Configuration Controller also controls daughterboard resets and temperature monitoring. The CB connects the daughterboard EEPROM directly to the MCC and enables automatic detection and identification of the daughterboard.

2.4 Power-up configuration and resets

This section describes the CoreTile Express A5x2 daughterboard power-up, configuration, and resets. It contains the following subsections:

- *Configuration architecture*
- *Resets* on page 2-11
- *Configuration and reset signals* on page 2-12.

2.4.1 Configuration architecture

Figure 2-4 shows the power-up, configuration, and reset architecture when the CoreTile Express A5x2 daughterboard is fitted to a Motherboard Express, V2M-P1.

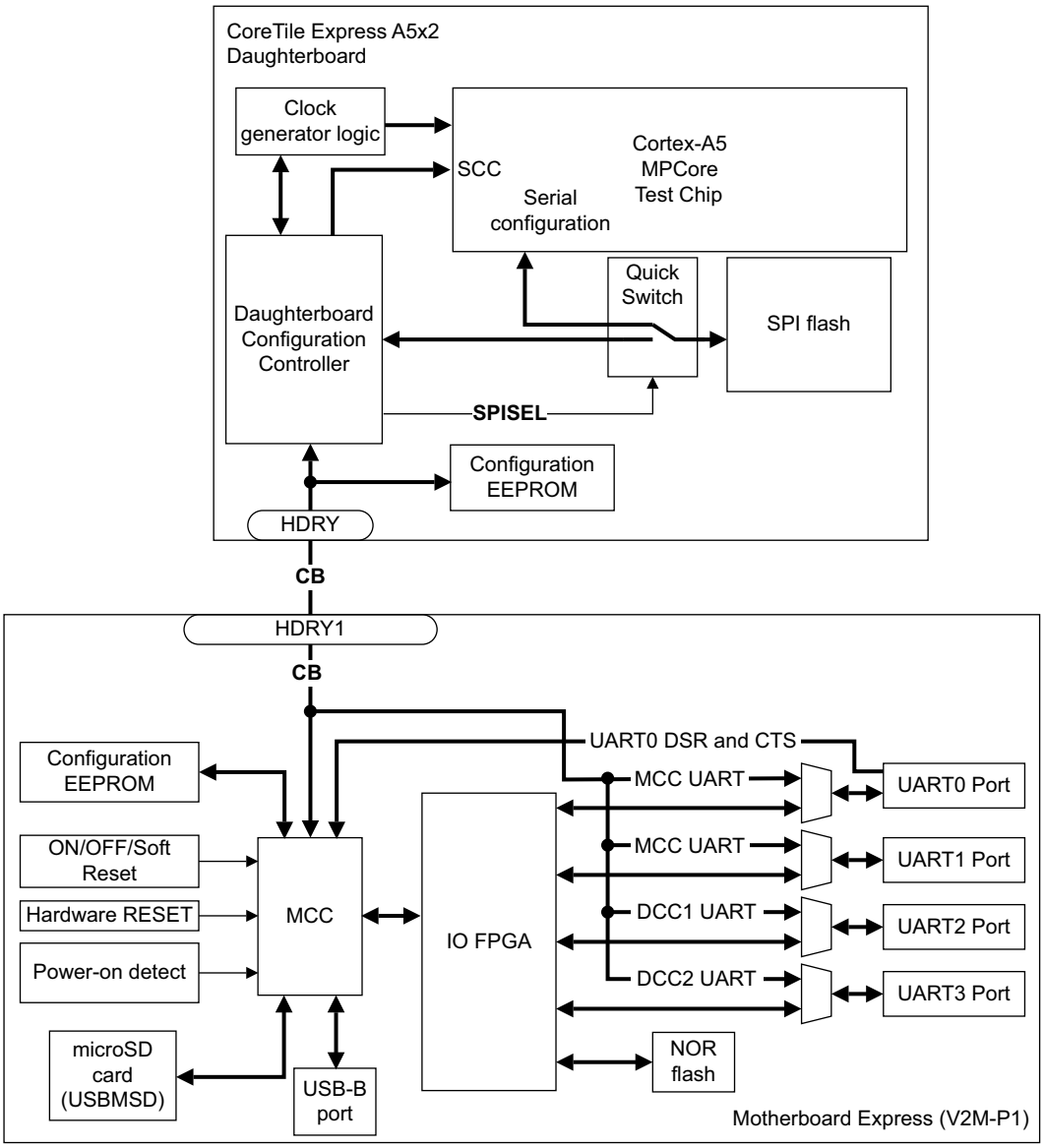


Figure 2-4 CoreTile Express A5x2 configuration architecture with Motherboard Express, V2M-P1

Note

ARM recommends that you fit the CoreTile Express A5x2 daughterboard in site 1.

The configuration environment of the CoreTile Express A5x2 daughterboard fitted to the Motherboard Express, V2M-P1, consists of the following hardware components:

- *Motherboard Configuration Controller* (MCC) on the Motherboard Express, V2M-P1.
- Daughterboard Configuration Controller on the CoreTile Express daughterboard and on the LogicTile Express daughterboard.
- Configuration microSD card or *Universal Serial Bus Mass Storage Device* (USBMSD) on the Motherboard Express, V2M-P1.
- Configuration EEPROM on the Motherboard Express, V2M-P1.
- Clock generator logic on the V2P-CA5s daughterboard.
- ON/OFF/Soft Reset and Hardware RESET buttons on the on the Motherboard Express, V2M-P1.
- USB-B port on the Motherboard Express, V2M-P1.
- Four UART ports on the Motherboard Express, V2M-P1.
- NOR flash on the Motherboard Express, V2M-P1.
- Power-on detect on the Motherboard Express, V2M-P1.
- Configuration EEPROM on the V2-CA5s daughterboard.
- SPI Flash on the V2P-CA5s daughterboard.
- Quick Switch on the daughterboard.
- HDRY headers on the Motherboard Express, V2M-P1, and V2P-CA5s daughterboard.

Figure 2-5 on page 2-10 shows the power-up, configuration and reset architecture when the CoreTile Express A5x2 daughterboard is fitted to a V2M-CP1 Programmer Module and custom motherboard built under the ARM Design Assist Program.

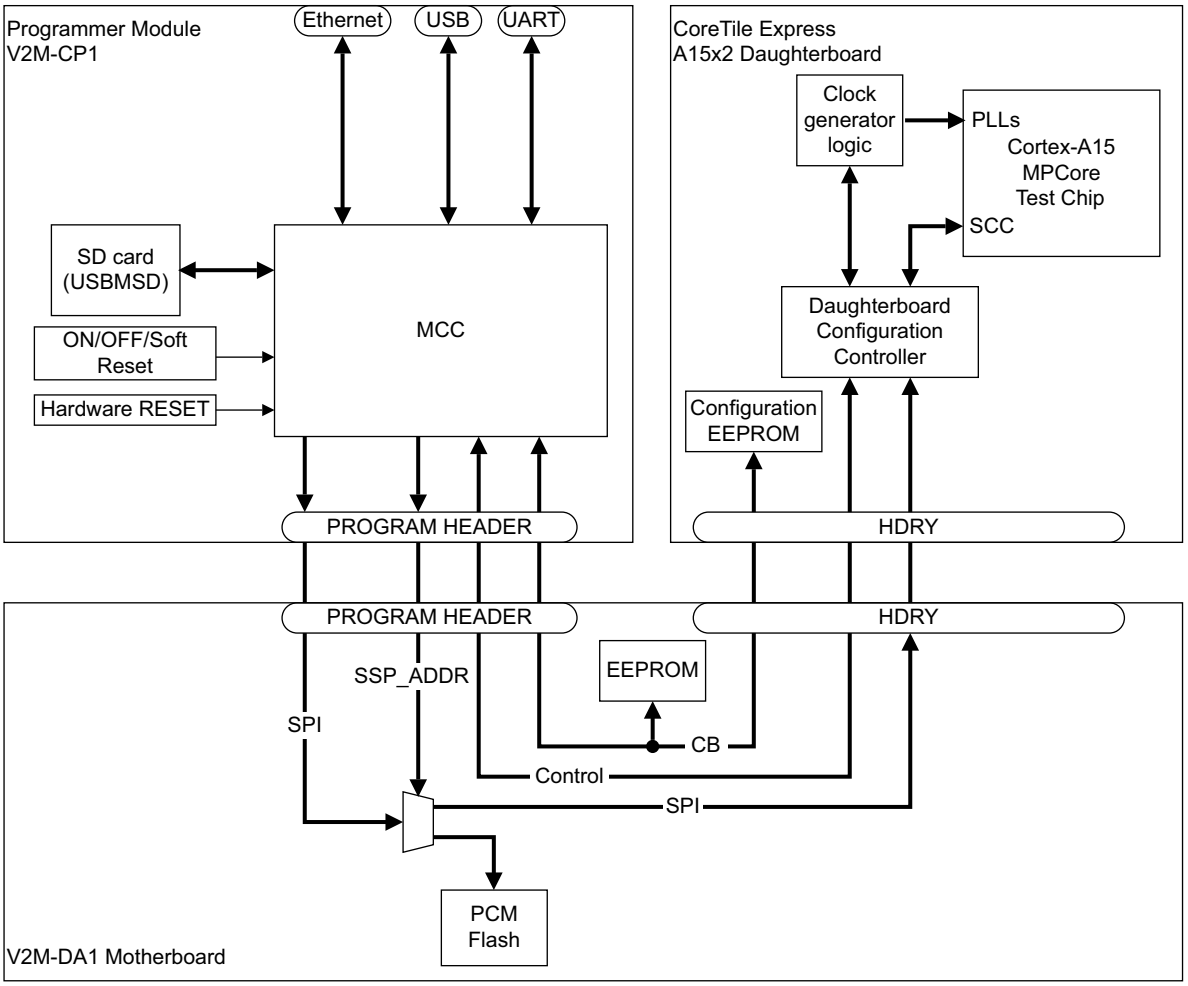


Figure 2-5 CoreTile Express A5x2 configuration architecture with custom motherboard

The configuration environment of a V2P-CA5s daughterboard fitted to a custom motherboard and a V2M-CP1 Programmer Module consists of:

- *Motherboard Configuration Controller* (MCC) on the V2M-CP1.
- Daughterboard Configuration Controller on the V2P-CA15 daughterboard.
- Configuration microSD card or *Universal Serial Bus Mass Storage Device* (USBMSD) on the V2M-CP1 Programmer Module.
- ON/OFF/Soft Reset and Hardware RESET buttons on the on the V2M-CP1 Programmer Module.
- USB port on the V2M-CP1 Programmer Module.
- Ethernet port on the V2M-CP1 Programmer Module.

  Note

  The V2M-CP1 Programmer Module does not support the ethernet port.

- Configuration EEPROM on the custom motherboard.
- Configuration EEPROM on V2P-CA5s daughterboard.

- SPI Flash on the V2P-CA5s daughterboard.
- Quick Switch on the daughterboard.
- Clock generator logic on the V2P-CA5s daughterboard.

2.4.2 System configuration

The Cortex-A5 MPCore test chip is a structured ASIC that must be configured by the SPI Flash. The motherboard USBMSD HBI sub-directory, corresponding to the CoreTile Express A5x2 daughterboard, contains image files for the Daughterboard Configuration Controller and SPI flash memory on the daughterboard.

If a new SPI flash image is available, the MCC validates it and copies it to the Daughterboard Configuration Controller on the daughterboard. The Quick Switch isolates the SPI Flash from the Cortex-A5 MPCore test chip and connects the SPI Flash to the Daughterboard Configuration Controller. The Daughterboard Configuration Controller then loads the new image into the SPI Flash memory. The MCC then updates the information in the daughterboard EEPROM. The Quick Switch isolates the SPI Flash from the Daughterboard Configuration Controller and connects the SPI Flash to the development chip. The SPI Flash then loads the new image into the test chip.

If a new SPI Flash image is not available, the Quick Switch isolates the SPI Flash from the Daughterboard Configuration Controller and the SPI Flash then loads the current image into the Cortex-A5 MPCore test chip.

See the *Versatile Express Configuration Technical Reference Manual* and *Motherboard Express (µATX)* or *Programmer Module (V2M-CP1)* for information on how to configure the V2P-CA5s daughterboard using the configuration files on the motherboard.

Caution

ARM recommends that you use the configuration files for all system configuration. *Programmable peripherals and interfaces* on page 3-7, however, describes registers that directly modify the test chip configuration.

2.4.3 Resets

The Daughterboard Configuration Controller manages reset signals between the motherboard and the development chip in response to reset requests from the motherboard MCC as a result of, for example, pressing the motherboard Power/Reset push button.

Figure 2-6 on page 2-12 shows an overview of the daughterboard reset signals and includes configuration signals.

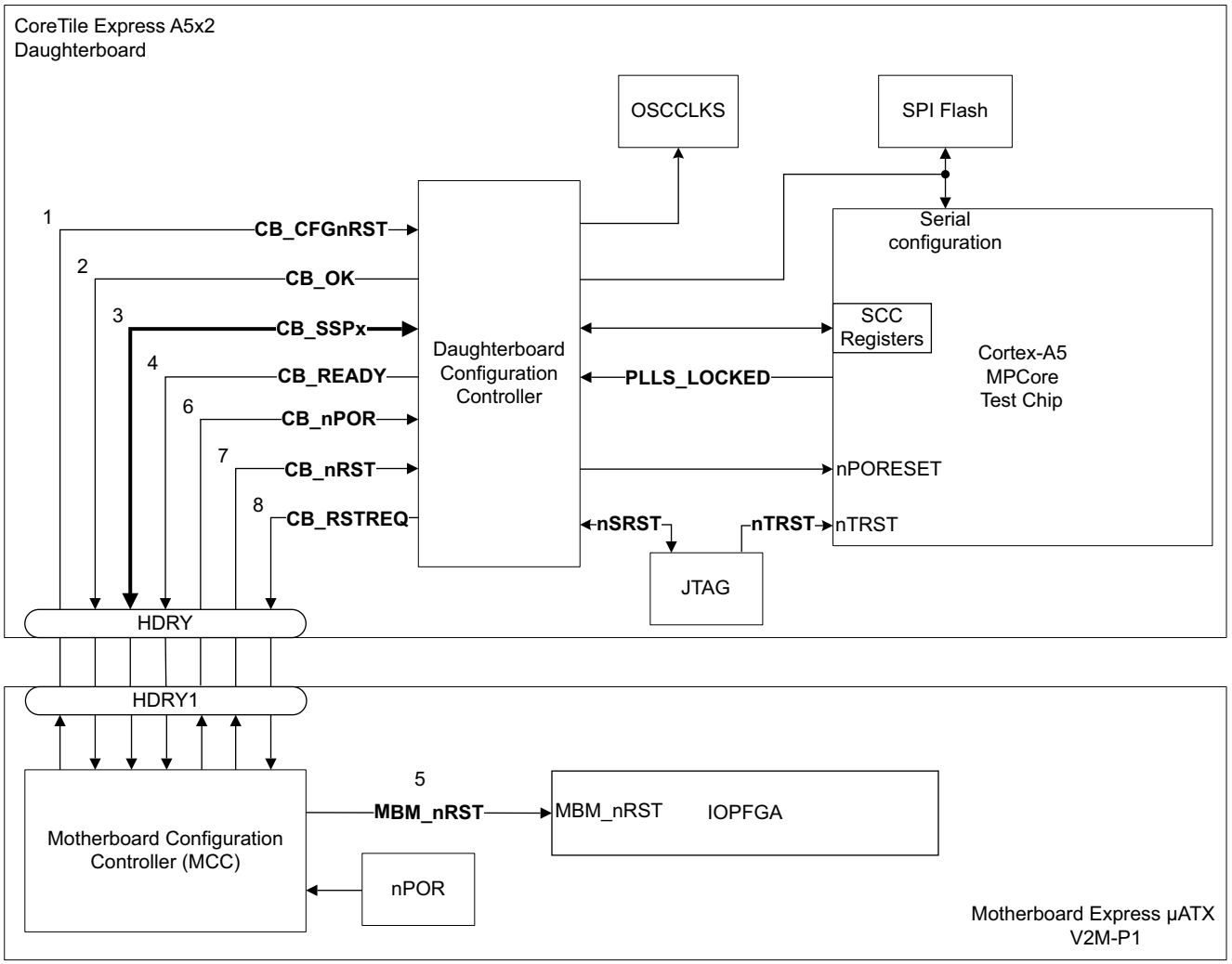


Figure 2-6 CoreTile Express A5x2 daughterboard resets

Note

The numbers in Figure 2-6 refer to stages in the reset and configuration process. See Figure 2-7 on page 2-13.

2.4.4 Configuration and reset signals

This section describes the configuration and reset signals and their sequences and timings.

Figure 2-7 on page 2-13 shows the CoreTile Express A5x2 daughterboard power-up configuration and reset timing cycle.

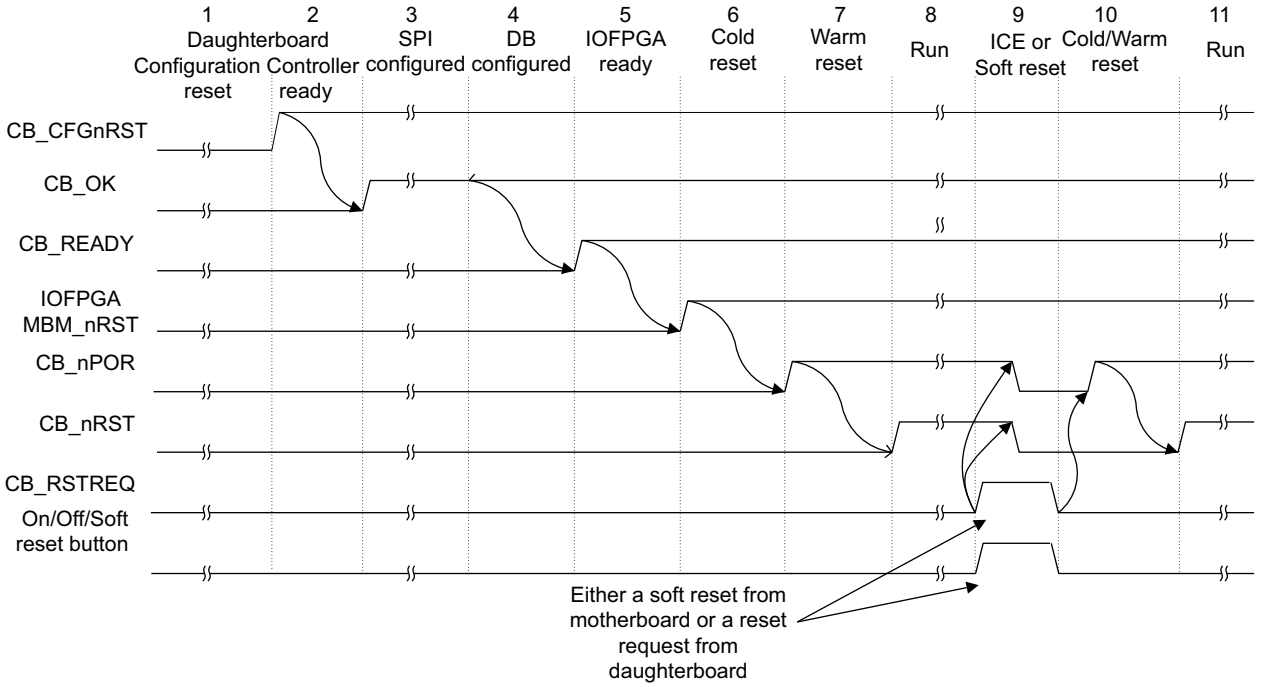


Figure 2-7 CoreTile Express A5x2 daughterboard configuration and reset timing cycle

Table 2-1 shows the Cortex-A5 MPCore test chip configuration and reset signals.

Table 2-1 Configuration and reset signals

Reset source	Destination	Description
CB_CFGnRST	Daughterboard Configuration Controller	Initiate the daughterboard configuration process.
CB_OK	MCC	Daughterboard Configuration Controller ready.
CB_SSPx[a]	Daughterboard Configuration Controller-MCC	Signal transactions during time period 3, *SPI configured*, that cause the Daughterboard Configuration Controller to configure the Cortex-A5 MPCore test chip SCC registers and daughterboard OSCCLKs.
CB_READY	MCC	Daughterboard configured and ready. The **PLLS_LOCKED**[a] signal and the control signals between the Daughterboard Configuration Controller, Cortex-A5 MPCore test chip, and the daughterboard OSCLCLKS indicate to the Daughterboard Configuration Controller and MCC that the PLLs are locked and the daughterboards OSCCLKS are operating.
CB_nPOR	Not applicable	Not used.
CB_nRST	Test chip internal signal **nPORESET**	This is a hard reset from the motherboard that resets the Cortex-A5 MPCore test chip, the AMBA subsystem, and the debug logic.
JTAG **nTRST**[a]	Test chip internal signal **nTRST**	This is the test logic reset to the Cortex-A5 MPCore test chip TAP controller and the Daughterboard Configuration Controller.

Table 2-1 Configuration and reset signals (continued)

Reset source	Destination	Description
JTAG **nSRST**[a]	**CB_RSTREQ** to motherboard MCC	If an external source asserts the JTAG **nSRST** signal, the daughterboard generates a reset request to the motherboard MCC. The motherboard hardware is reset and the MCC asserts **CB_nRST** and, optionally, **CB_nPOR**[b]. The **nSRST** signal remains LOW until the reset sequence completes.
CB_RSTREQ[b]	MCC	Reset request from the daughterboard to the motherboard.
Test Chips Watchdogs	Test chip internal **nPORESET**	If the internal Test Chip watchdog timers are configured and they trigger, they force an internal test chip **nPORESET**. The external system components on the motherboard are not reset.

a. Figure 2-7 on page 2-13 does not include these signals.

b. The reset request from the daughterboard results in the motherboard asserting **CB_nRST**.

CB_nPOR can optionally be asserted by correctly defining the value of the control value **ASSERTNPOR**, that can be TRUE or FALSE in the `config.txt` motherboard configuration file. See the *Motherboard Express µATX Technical Reference Manual* for an example `config.txt` file.

2.5 Clocks

This section describes the daughterboard clocks. It contains the following subsections.

- *Overview of clocks*
- *Programmable clock generators* on page 2-16
- *External clocks* on page 2-17.

2.5.1 Overview of clocks

The daughterboard sends and receives clocks to and from the motherboard, and also generates local clocks that are imported into the Cortex-A5 MPCore test chip. Additional PLLs inside the test chip provide phase-shifted and frequency-multiplied versions of these imported clocks as Figure 2-9 on page 2-16 shows.

Figure 2-8 shows a functional overview of the CoreTile Express A5x2 daughterboard clocks and their connections to the motherboard, and a LogicTile Express FPGA daughterboard.

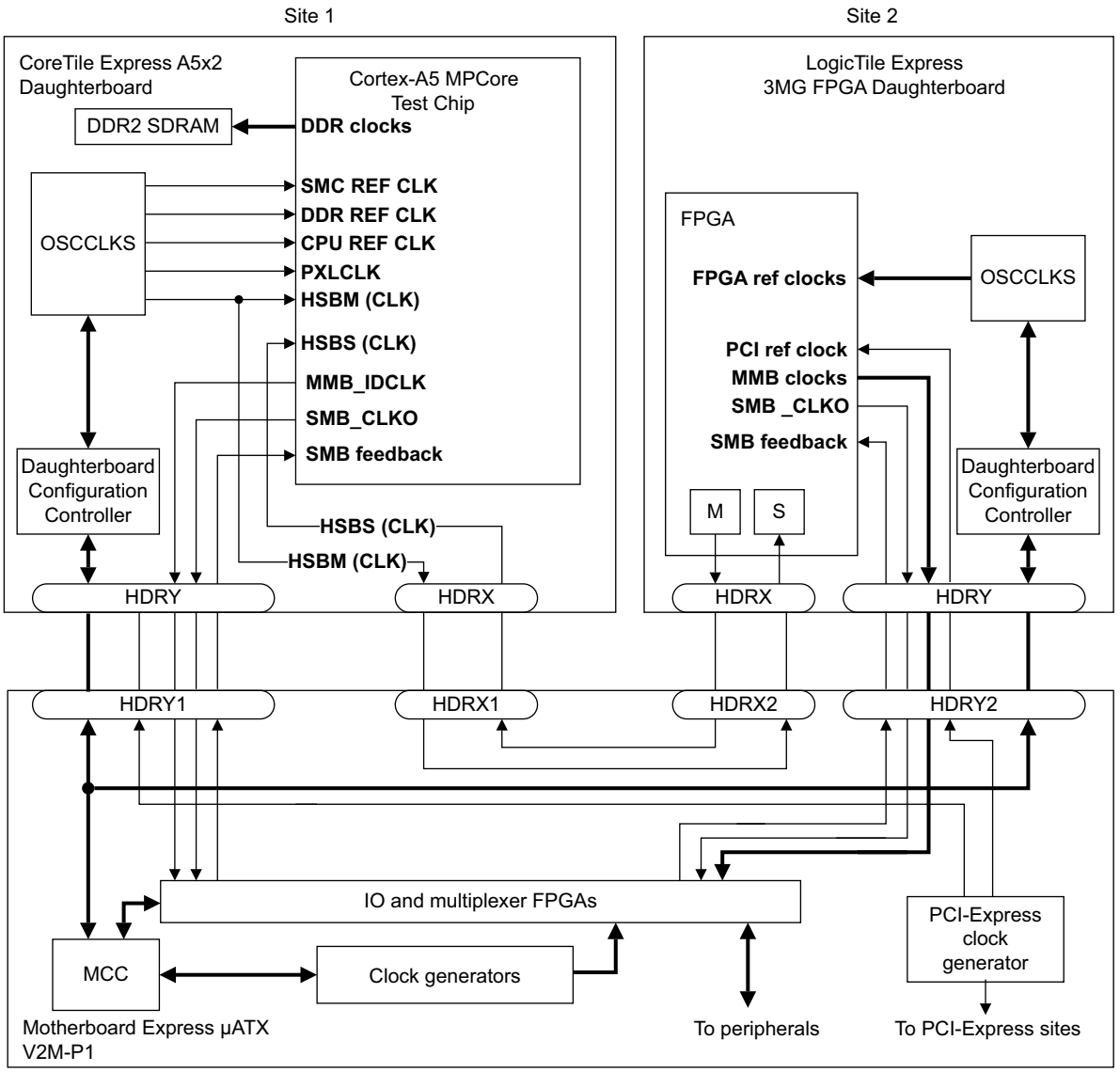


Figure 2-8 System clocks overview

Note

In the CoreTile Express A5x2 daughterboard, MMB clocks are generated from **PXLCLK**, and this originates from OSC3.

Figure 2-9 shows a functional view of the CoreTile Express A5x2 daughterboard clocks.

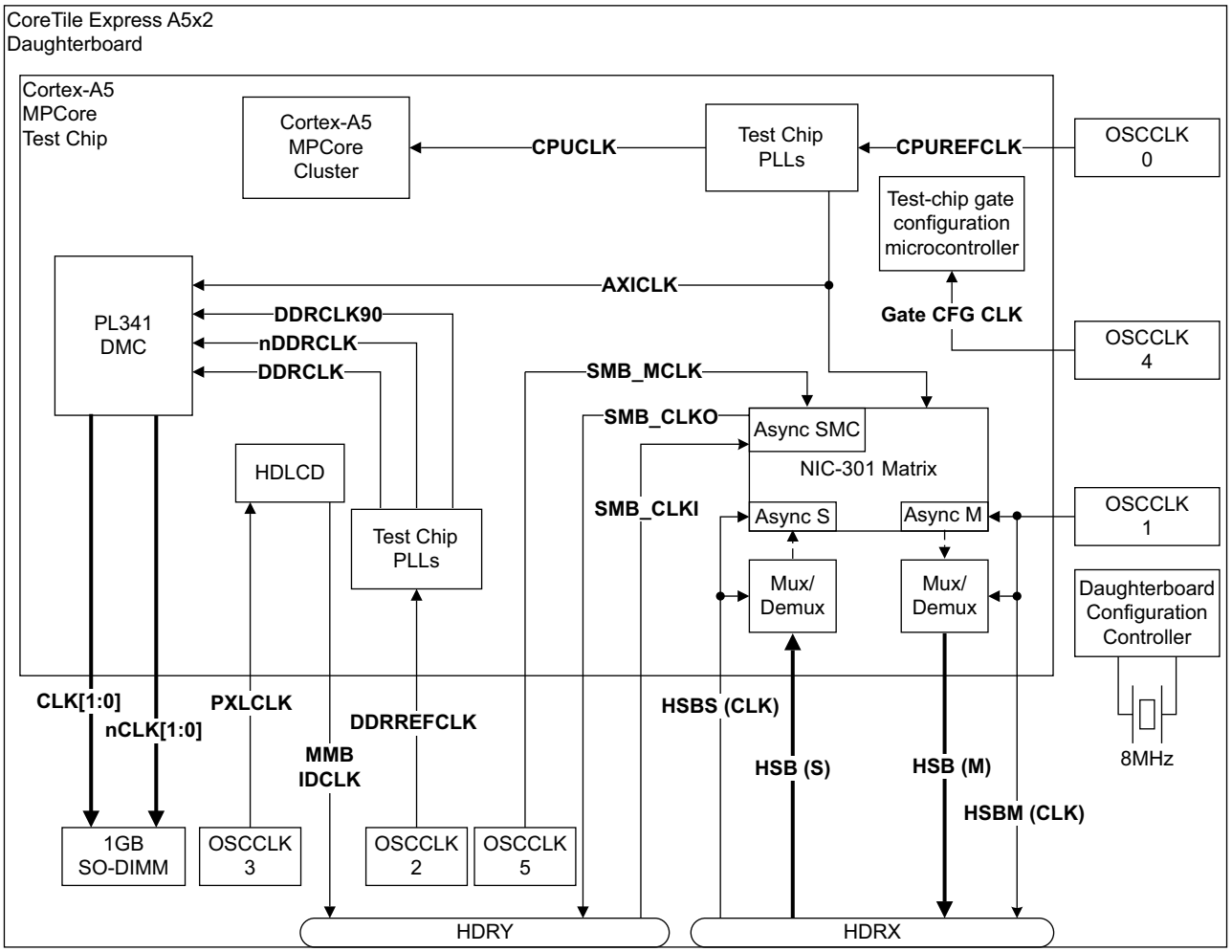


Figure 2-9 CoreTile Express A5x2 daughterboard clocks

Note

You can select the polarity of **MMB_IDCLK** relative to **PXLREFCLK**. It can be either in phase with **PXLREFCLK** or inverted. See *Polarities Register* on page B-17.

During power-up, the test-chip gate configuration microcontroller, together with the SPI flash, loads the SPI flash image into the test-chip to physically configure the test-chip circuit.

2.5.2 Programmable clock generators

The motherboard MCC and daughterboard Daughterboard Configuration Controller use the `board.txt` configuration file for the daughterboard to set the frequency of the daughterboard clock generators. The clocks can be adjusted during run-time by using the motherboard SYS_CFG register interface. For more information, see *Power-up configuration and resets* on page 2-8 and the *Motherboard Express µATX Technical Reference Manual*.

Table 2-2 shows the local daughterboard clocks that the programmable clock generators on the CoreTile Express A5x2 daughterboard generate. The local daughterboard clock frequencies are defined in the motherboard USBMSD `board.txt` file. See the *Versatile Express Configuration Technical Reference Manual* for an example `board.txt` file.

Table 2-2 Daughterboard OSCCLK clock sources

Test chip signal	Function	Source	Frequency range	Description
CPUREFCLK	CPU and internal AXI reference clock	OSCCLK0	50MHz-100MHz	CPU and AXI clock, default 80MHz. Reference clock for the test chip internal clock generators, PLLs, that produce the following clocks: **CPUCLK** For the Cortex-A5 core. **AXICLK** For the internal AXI infrastructure.
HSBM (CLK)	Multiplexed AXI master clock	OSCCLK1	5MHz-50MHz	AXI master clock, default 50MHz.
DDRREFCLK	DDR2	OSCCLK2	80MHz-120MHz	DDR2 DMC clock, default 120MHz. Reference clock for the test chip internal clock generator, PLL, that produces the following clocks for the DDR2 DMC interface: • **DDDRCLK**. • **nDDRCLK**. • **DDRCLK90**.
PXLCLK	HDLCD	OSCCLK3	23.75MHz-165MHz	Reference clock for the HDLCD controller in the test chip. You must adjust the frequency of this clock to match your target screen resolution. The HDLCD controller is capable of displaying up to 1920 × 1080p pixel resolution at 60Hz with **PXLCLK** set to 165MHz. See Appendix B *HDLCD controller*.
GateCFG CLK	Test chip gate configuration	OSCCLK4	80MHz	This clocks a microprocessor, test-chip gate configuration microcontroller, inside the test chip that configures the physical circuit of the test chip on power-up. This clock must be 80MHz.
SMB_MCLK	SMB clock	OSCCLK5	See the *Motherboard Express µATX Technical Reference Manual*	Static memory controller clock.

The clock generators have an absolute accuracy of better than 1%. If you enter a setting that cannot be precisely generated, the value is approximated to the nearest usable value.

2.5.3 External clocks

Table 2-3 on page 2-18 shows the external bus clocks that connect:

- Between the CoreTile Express A5x2 daughterboard and the motherboard.
- Between the CoreTile Express A5x2 daughterboard and the optional FPGA daughterboard in Site 2.

Table 2-3 External clock sources

Test chip signal	Function	Source	Frequency range	Description
HSBS (CLK)	Multiplexed AXI master clock	FPGA daughterboard in site 2	5MHz-80MHz	AXI slave clock Default 50MHz
SMB_CLKI	The SMC uses this to adjust for optimum timing	Motherboard	See the *Motherboard Express µATX Technical Reference Manual*	A skew-controlled version of the SMB clock that is sent from the motherboard to the SMC in the test chip
SMB_CLKO	The SMC clock to motherboard	OSCCLK5	See the *Motherboard Express µATX Technical Reference Manual*	Clock to motherboard SMB derived from **SMB_MCLK**

2.6 Interrupts

This section describes the daughterboard interrupts. It contains the following subsections:

- *Overview of interrupts*
- *Test chip interrupts* on page 2-20.

2.6.1 Overview of interrupts

The Cortex-A5 MPCore test chip implements a *Generic Interrupt Controller* (GIC) with 32 internal interrupts and 96 external interrupts as follows:

- Internal interrupts:
  - The 32 internal interrupts connect internally between the CPUs and the GIC.
- External interrupts:
  - The *System Bus* (SB) connects 17 of the 96 external interrupts between the motherboard and the daughterboard.
  - The test chip peripherals connect to 12 of the external interrupts.
  - 67 external interrupts are reserved.

Figure 2-10 shows an overview of the interrupt signals between the CoreTile Express A5x2 daughterboard and the motherboard.

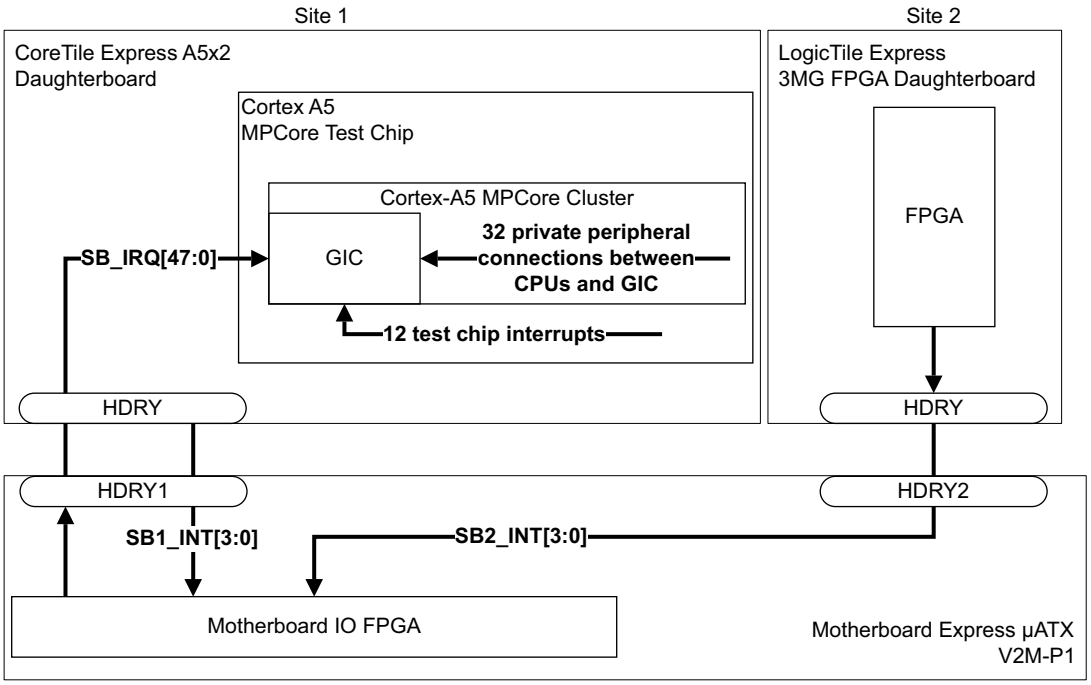


Figure 2-10 CoreTile Express A5x2 daughterboard interrupt overview

2.6.2 Test chip interrupts

Table 2-4 shows the interrupts from the motherboard IOFPGA, the interrupts from the test chip peripherals, the interrupts from the MPCore cluster and the reserved interrupts.

Table 2-4 Test chip interrupts

GIC interrupt	SB_IRQ[] interrupt from the motherboard	Source	Signal	Description
0:31	Not applicable	MPCore cluster	-	Private peripheral connections between CPUs and GIC
32	0	IOFPGA	**WDOG0INT**	Watchdog timer
33	1	IOFPGA	**SWINT**	Software interrupt
34	2	IOFPGA	**TIM01INT**	Dual Timer 0/1 interrupt
35	3	IOFPGA	**TIM23INT**	Dual Timer 2/3 interrupt
36	4	IOFPGA	**RTCINTR**	Real time clock interrupt
37	5	IOFPGA	**UART0INTR**	UART0 interrupt
38	6	IOFPGA	**UART1INTR**	UART1 interrupt
39	7	IOFPGA	**UART2INTR**	UART2 interrupt
40	8	IOFPGA	**UART3INTR**	UART3 interrupt
41	9	IOFPGA	**MCI_INTR[0]**	Media card interrupt
42	10	IOFPGA	**MCI_INTR[1]**	Media card interrupt
43	11	IOFPGA	**AACI_INTR**	Audio CODEC interrupt
44	12	IOFPGA	**KMI0_INTR**	Keyboard, mouse interrupt
45	13	IOFPGA	**KMI1_INTR**	Keyboard, mouse interrupt
46	14	IOFPGA	**CLCDINTR**	Display interrupt
47	15	IOFPGA	**ETH_INTR**	Ethernet interrupt
48	16	IOFPGA	**USB_nINT**	USB interrupt
49	17	IOFPGA	**PCIE_GPEN**	PCI-Express interrupt
53:50	21:18	IOFPGA	**SB1_INT[3:0]**	Copy of **SB_IRQ[35:32]**
57:54	25:22	IOFPGA	**SB2_INT[3:0]**	Copy of **SB_IRQ[39:36]**
63:58	31:26	IOFPGA	-	Tied to `b0` in IOFPGA
67:64	35:32	IOFPGA	**SB1_INT[3:0]**	Interrupts **INT[3:0]** from Site 1 daughterboard when you fit the V2P-CA5s daughterboard in site 2
71:68	39:36	IOFPGA	**SB2_INT[3:0]**	Interrupts **INT[3:0]** from Site 2 daughterboard when you fit the V2P-CA5s daughterboard in site 1
79:72	47:40	IOFPGA	-	Tied to `b0` in IOFPGA
99:80	Not applicable	`b0`	-	Reserved
100	Not applicable	Test chip	-	CPU0 performance monitor unit

Table 2-4 Test chip interrupts (continued)

GIC interrupt	SB_IRQ[] interrupt from the motherboard	Source	Signal	Description
101	Not applicable	Test chip	-	CPU1 performance monitor unit
102	Not applicable	Test chip	-	Reserved
103	Not applicable	Test chip	-	Reserved
104	Not applicable	Test chip	-	CPU0 cross trigger interrupt
105	Not applicable	Test chip	-	CPU1 cross trigger interrupt
106	Not applicable	Test chip	-	Reserved
107	Not applicable	Test chip	-	Reserved
108	Not applicable	Test chip	-	CPU0 CP14 DTR COMMTX Interrupt
109	Not applicable	Test chip	-	CPU1 CP14 DTR COMMTX interrupt
110	Not applicable	Test chip	-	Reserved
111	Not applicable	Test chip	-	Reserved
112	Not applicable	Test chip	-	CPU0 CP14 DTR COMMRX interrupt
113	Not applicable	Test chip	-	CPU1 CP14 DTR COMMRX interrupt
114	Not applicable	Test chip	-	Reserved
115	Not applicable	Test chip	-	Reserved
116	Not applicable	Test chip	-	L2 cache controller interrupt
117	Not applicable	Test chip	-	HDLCD interrupt
118	Not applicable	Test chip	-	SMC interface 0 interrupt
119	Not applicable	Test chip	-	SMC interface 1 interrupt
127:120	Not applicable	`b0`	-	Reserved

Note

- For more information on the motherboard peripherals that generate interrupts to the test chip, see the *Motherboard Express µATX Technical Reference Manual*.

2.7 Serial configuration controller

The *Serial Configuration Controller* (SCC) is a block of registers internal to the test chip that the Daughterboard Configuration Controller writes to through a serial interface. The Daughterboard Configuration Controller uses the SCC during power-up configuration to set the test chip PLLs and other default values from the board configuration files stored on the motherboard microSD card. The MCC also uses the SCC to read values from the test chip, for example, the device ID.

You can also read and write to the SCC registers, while the system is running, using the motherboard SYS_CFG register interface.

Figure 2-11 shows an overview of the SCC connectivity.

Figure 2-12 on page 2-23 and Figure 2-13 on page 2-23 show the timing diagrams for the SCC read and write operations. The SCC operates a 12-bit address and 32-bit data phase.

See Chapter 3 *Programmers Model* for a full description of the SCC registers.

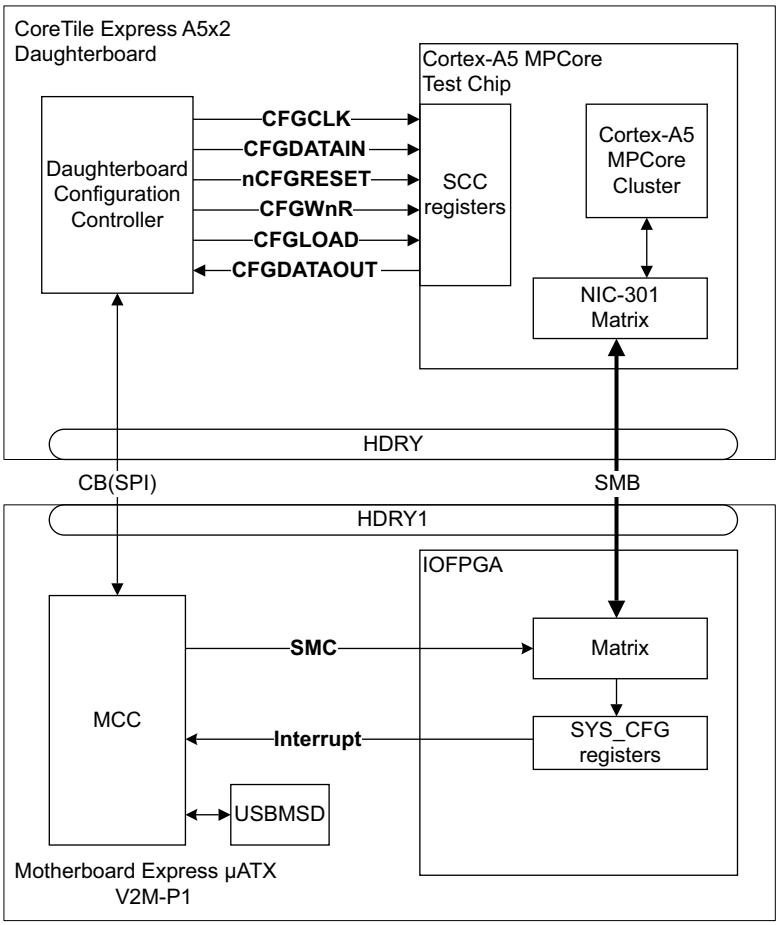


Figure 2-11 Overview of SCC connectivity

Figure 2-12 on page 2-23 shows the timing diagram for the SCC read operations.

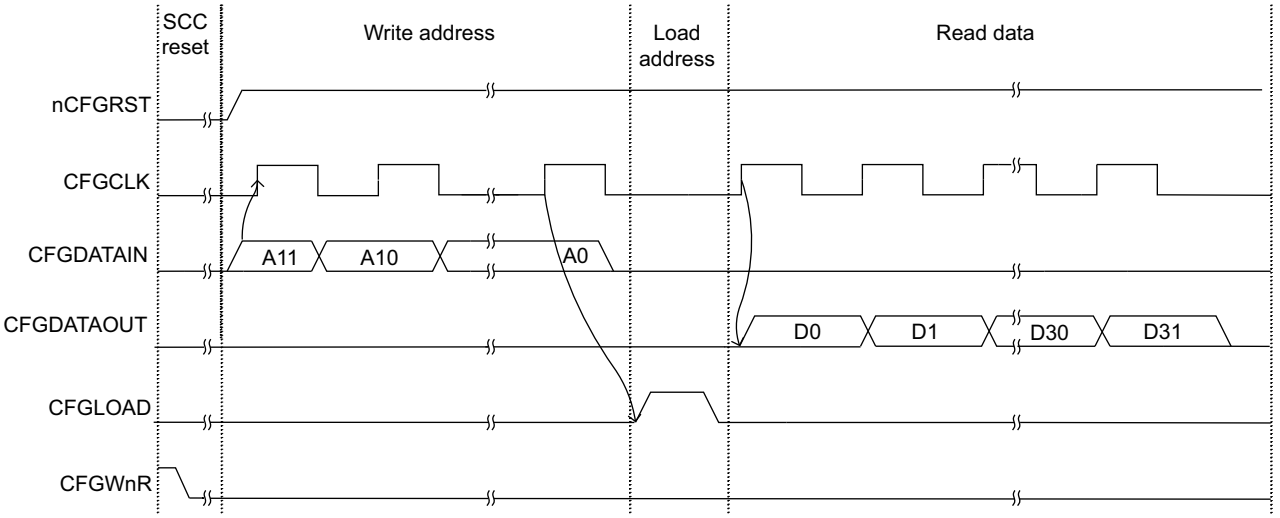


Figure 2-12 Daughterboard Configuration Controller read from SCC

Figure 2-13 shows the timing diagram for the SCC write operation.

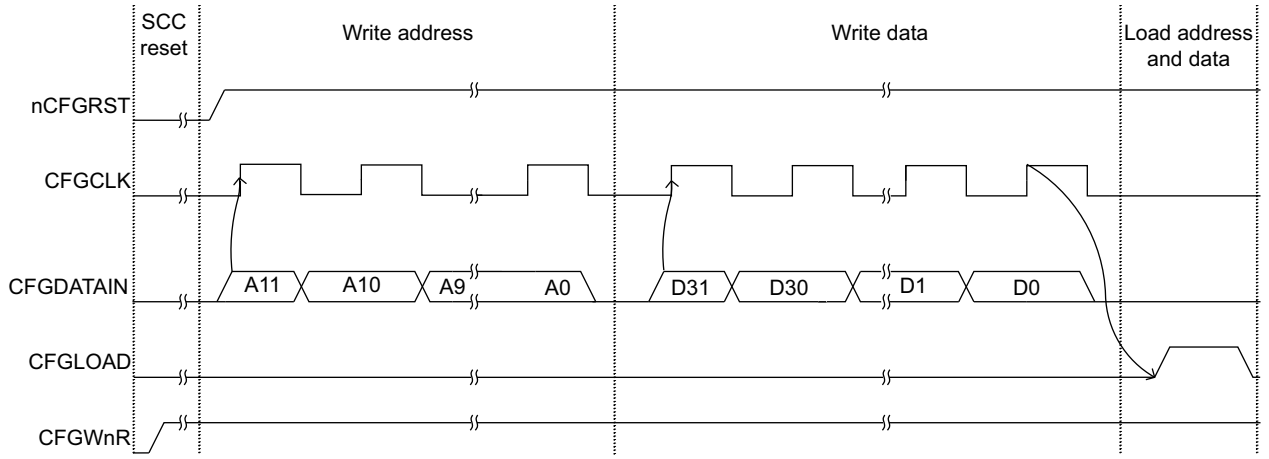


Figure 2-13 Daughterboard Configuration Controller write to SCC

2.8 Temperature monitoring

The Daughterboard Configuration Controller transmits information about its own temperature to the motherboard where it can be read from the SYS_CFGCTRL interface.

Table 2-5 shows the device number for the Daughterboard Configuration Controller temperature.

Table 2-5 Device number Daughterboard Configuration Controller temperature monitoring

Device	Daughterboard Configuration Controller temperature	Temperature range	Description
0	VD10	0-50°C	Daughterboard Configuration Controller internal operating temperature

2.9 Debug

You can attach a JTAG debugger to the daughterboard JTAG connector to execute programs to the daughterboard and debug them. For convenience, connect the cable from the rear panel JTAG connector to the daughterboard JTAG. For example, you can connect the RealView Debugger to this debug interface using an external RealView ICE interface box.

Note

The daughterboard does not support adaptive clocking. The **RTCK** signal is tied LOW on the JTAG ICE connector.

See Figure 1-1 on page 1-3 for the location of the JTAG ICE connector.

Figure 2-14 shows an overview of the CoreSight system.

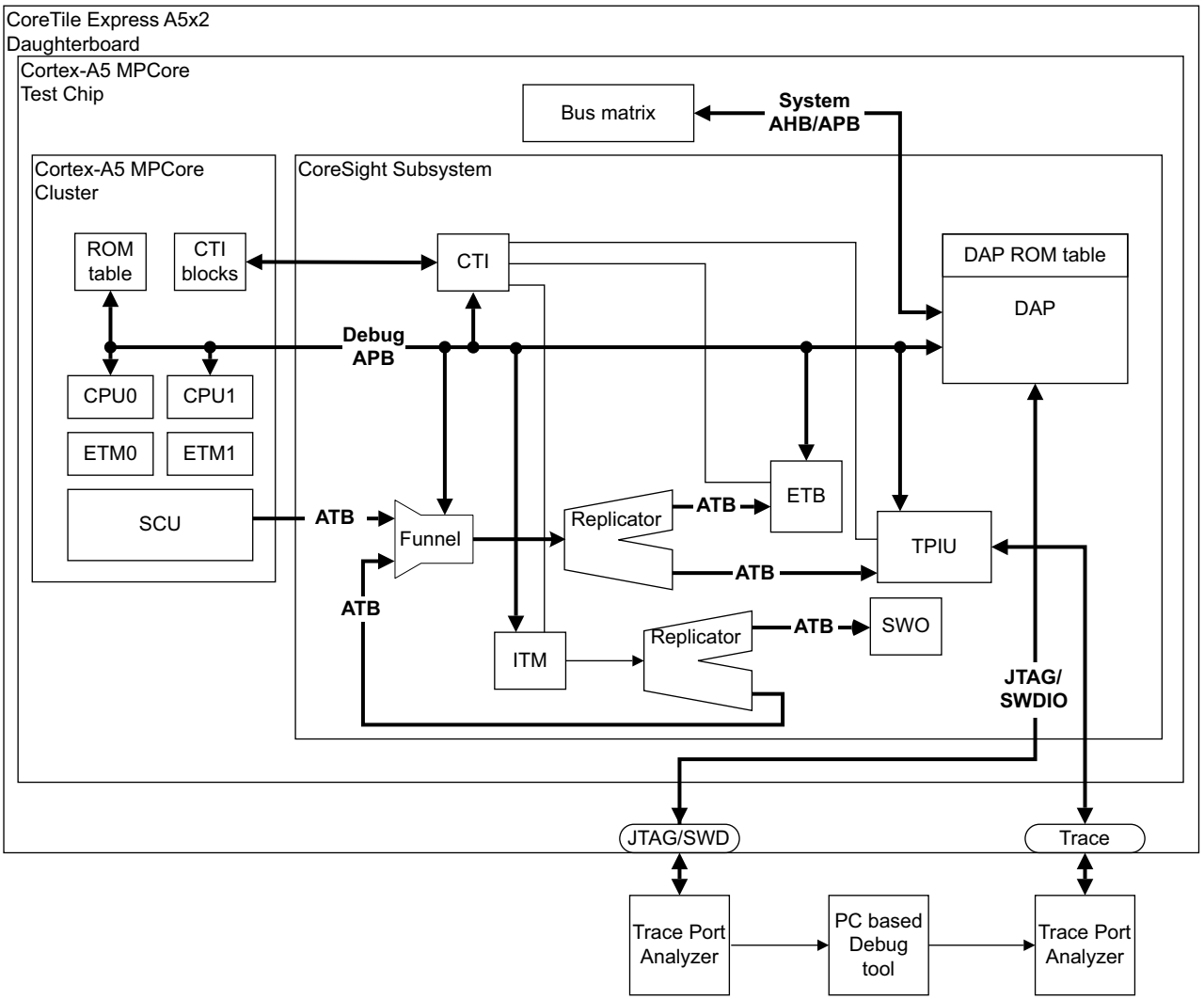


Figure 2-14 CoreTile Express A5x2 CoreSight and Trace

For information on CoreSight components, see the *CoreSight Components Technical Reference Manual*.

For information on Cortex-A5 ETM, see the *CoreSight ETM-A5 Technical Reference Manual*.

The daughterboard supports up to 32-bit trace in *continuous* mode. There are two MICTOR connectors for JTAG trace. See Figure 1-1 on page 1-3 for the location of these connectors.

To set up a trace connection to either of the cores on the test chip, you must know the funnel port number and ETM base address connection information associated with each core. Table 2-6 defines these addresses for both cores on the test chip.

Table 2-6 Test chip Trace connection addresses

Core	Core base address	Funnel port	ETM base address
Core 0	0x22010000	0	0x2201C000
Core 1	0x22012000	1	0x2201D000

See *Daughterboard memory map* on page 3-3 for the memory addresses of all CoreSight components.

2.10 DDR2 SO-DIMM memory interface

The Cortex-A5 DDR2 SO-DIMM memory interface uses a PL341 *Dynamic Memory Controller* (DMC). The DMC runs asynchronously to the AXI matrix so the AXI sub-system does not impose frequency limitations on the DMC interface.

Figure 2-15 shows a functional overview of the DDR2 SO-DIMM memory interface.

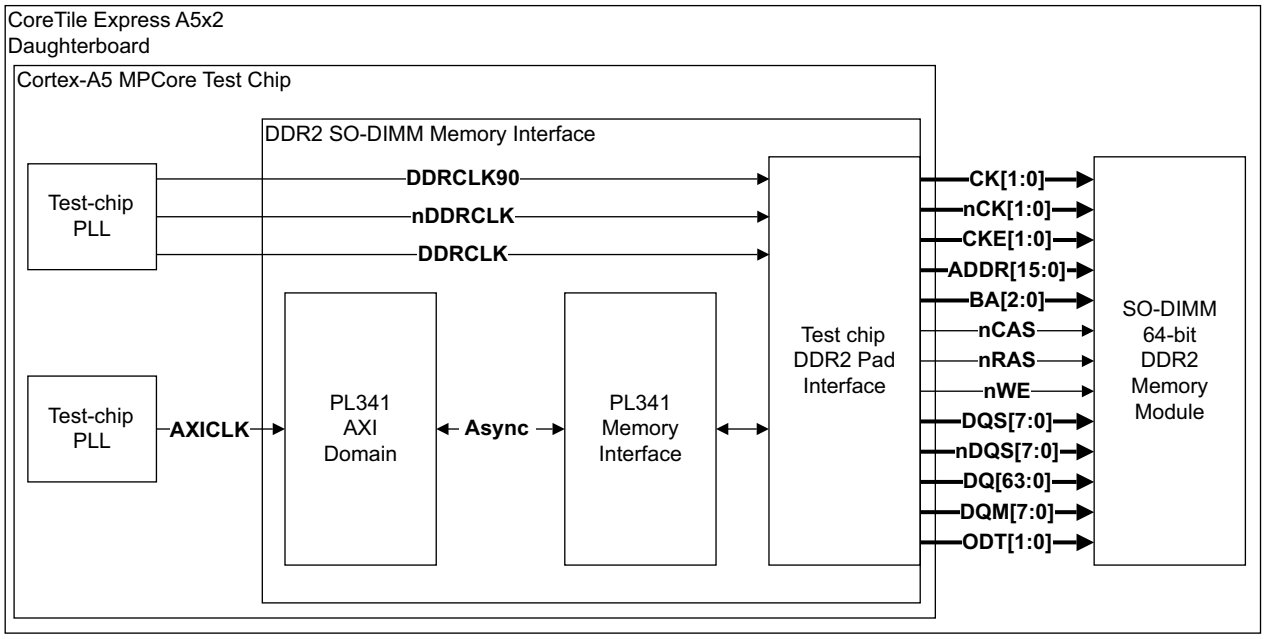


Figure 2-15 DDR2 SO-DIMM memory interface

Note

- OSCCLK2 is the source for DDRCLK90, nDDRCLK, and DDRCLK.

  OSCCLK0 is the source for AXICLK.

  See Figure 2-9 on page 2-16 and Table 2-2 on page 2-17.
- ARM recommends that you use the SO-DIMM memory supplied with the CoreTile Express A5x2 daughterboard. ARM does not recommend using alternative DIMMs.

2.11 HDLCD

An ARM HDLCD controller in the Cortex-A5 MPCore test chip provides graphic display capabilities. The controller is a frame buffer device that is capable of displaying up to 1920×1080p pixel resolution at 60Hz with a 165MHz pixel clock from OSCCLK3. The *MultiMedia Bus* (MMB) connects the 24-bit RGB data directly between the test chip and the motherboard through header HDRY. The multiplexer FPGA on the motherboard can select this bus to drive the analog and digital interfaces for the DVI connector.

The HDLCD frame buffer is located in DDR2 memory serviced by the DMC from the test chip bus matrix. This ensures maximum data bandwidth between the Cortex-A5 MPCore cluster, the HDLCD controller, and DDR2 memory without accessing off-chip devices.

Figure 2-16 shows a functional overview of the HDLCD controller and its connections to the Cortex-A5 test chip and the motherboard.

See Appendix B *HDLCD controller* for a full description of the HDLCD controller.

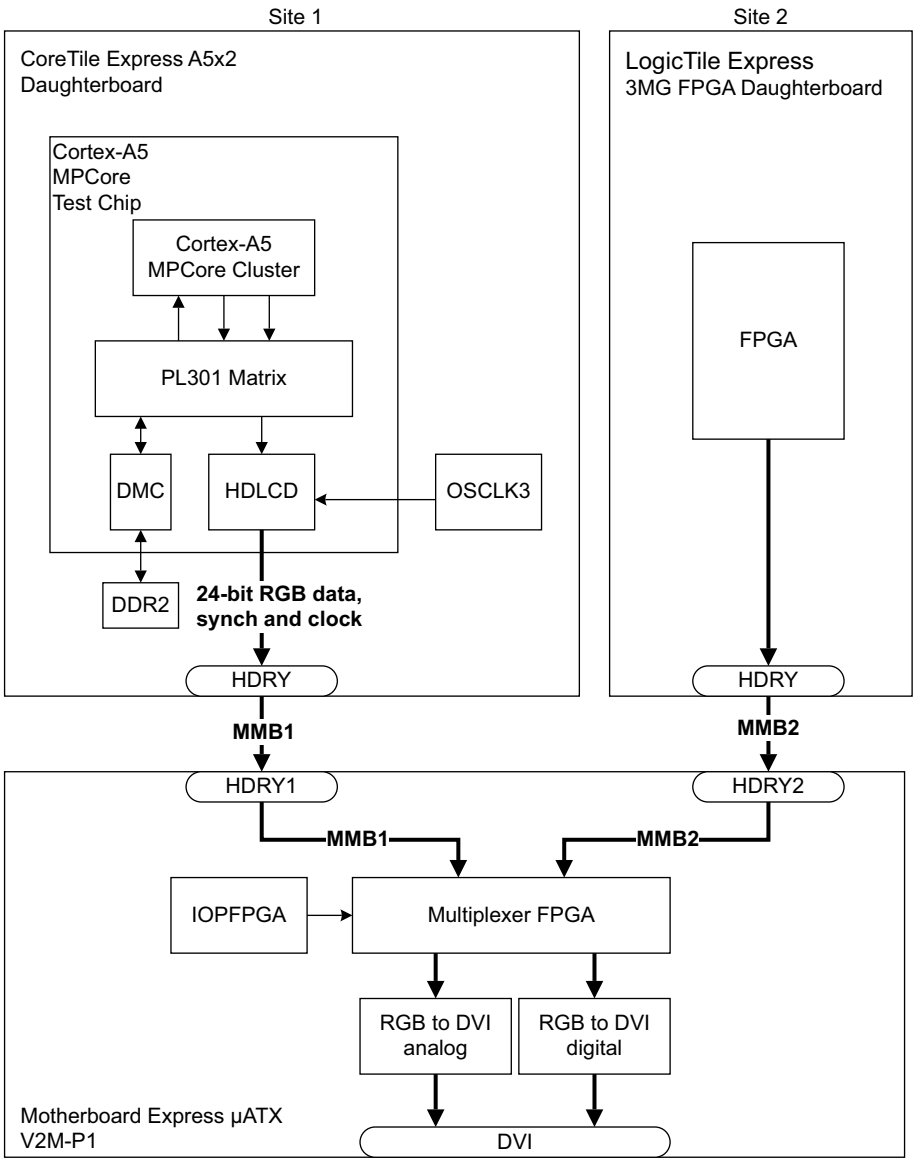


Figure 2-16 HDLCD graphics system interconnect

Chapter 3
Programmers Model

This chapter describes the memory map and the configuration registers for the peripherals on the daughterboard. It contains the following sections:

- *About this programmers model* on page 3-2
- *Daughterboard memory map* on page 3-3
- *Programmable peripherals and interfaces* on page 3-7.

3.1 About this programmers model

The following information applies to the SCC:

- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or power-on reset.
  - Access type in Table 3-2 on page 3-10 is described as follows:

    RW Read and write.

    RO Read only.

    WO Write only.

3.2 Daughterboard memory map

The CoreTile Express A5x2 daughterboard uses the ARM *Cortex-A Series* memory map. Figure 3-1 shows the daughterboard memory map.

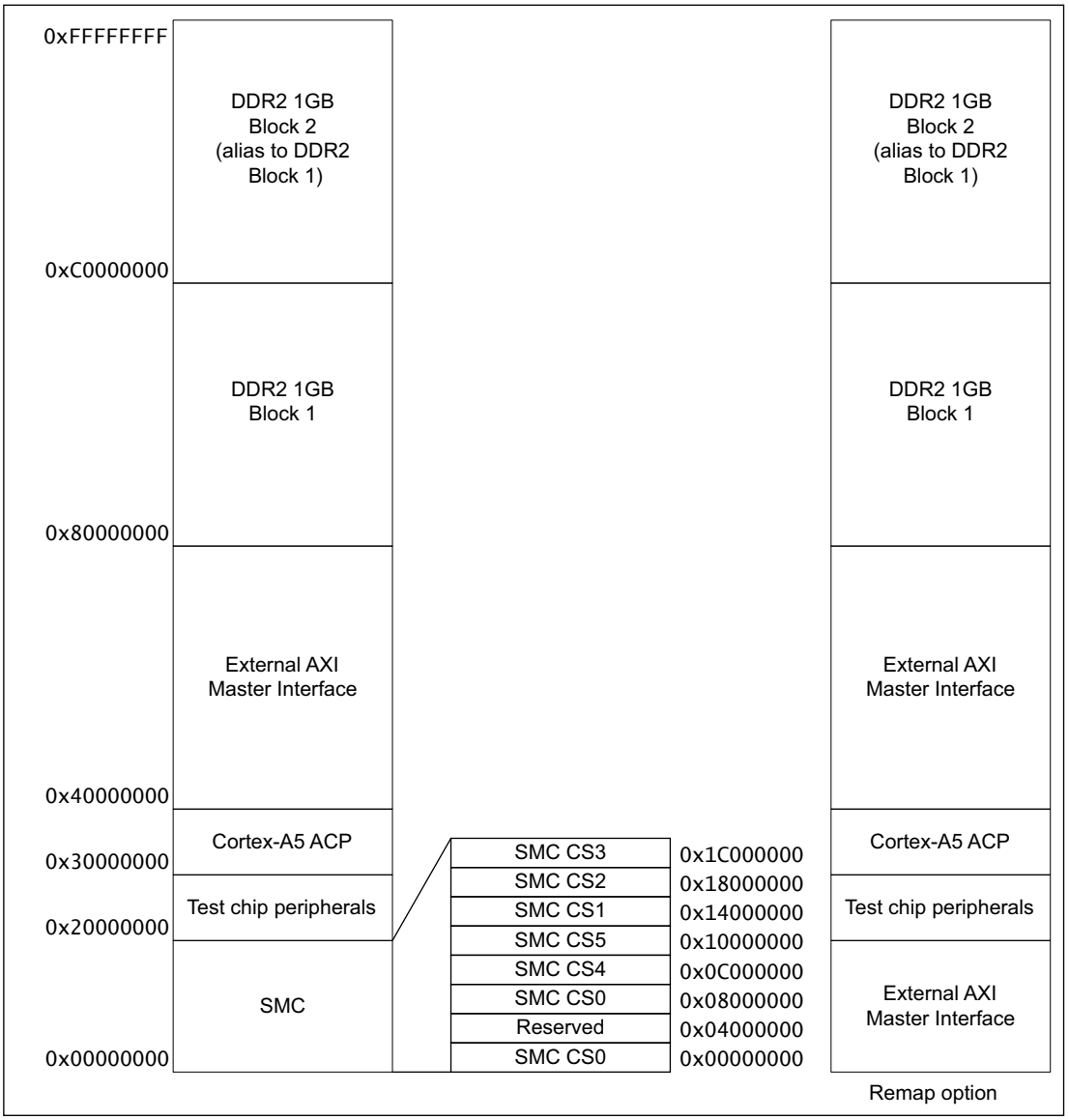


Figure 3-1 CoreTile Express A5x2 daughterboard memory map

A typical system boots from SMC CS0 that addresses the motherboard NOR flash 0. See *Remapping memory* on page 3-4. After DDR2 configuration is complete, the exception vectors are moved into the DDR2 area using the CoreSight vector offset registers.

Table 3-1 shows the daughterboard peripheral interfaces.

Table 3-1 Peripheral memory map

Address range	Size	Description
0x0000_0000-0x03FF_FFFF	64MB	CS0-Motherboard NOR flash 0.
0x0400_0000-0x07FF_FFFF	64MB	Reserved.
0x0800_0000-0x0BFF_FFFF	64MB	CS0-Motherboard NOR flash 0.
0x0C00_0000-0x0FFF_FFFF	64MB	CS4-Nor flash 1.
0x1000_0000-0x13FF_FFFF	64MB	CS5-Reserved.
0x1400_0000-0x17FF_FFFF	64MB	CS1-PSRAM.
0x1800_0000-0x1BFF_FFFF	64MB	CS2-Video/ETH/USB.
0x1C00_0000-0x1FFF_FFFF	64MB	CS3-system registers and peripherals.
0x0000_0000-0x1FFF_FFFF	512MB	External AXI master interface. Remap option.
0x2000_0000-0x2FFF_FFFF	256MB	Test chip peripherals.
0x3000_0000-0x3FFF_FFFF	256MB	Cortex-A5 *Accelerator Coherency Port* (ACP)
0x4000_0000-0x7FFF_FFFF	1GB	External AXI between daughterboards.
0x8000_0000-0xBFFF_FFFF	1GB	CoreTile Express A5x2 daughterboard DDR2. Block 1.
0xC000_0000-0xFFFF_FFFF	1GB	CoreTile Express A5x2 daughterboard DDR2. Alias to Block 1.

3.2.1 Remapping memory

This section describes the remap options for address 0x0 and contains the following subsections:

- *SMC or AXI*
- *Chip-select remap*
- *Memory remapping at power-on during run-time* on page 3-5.

SMC or AXI

SCC register bit CFGRW0[0] controls whether AXI or SMC is mapped to the lower 512MB of memory. This enables booting from external AXI.

Chip-select remap

SCC register bits CFGRW0[31:30] control whether CS0 or CS4 is addressed at address 0x0. See *Test chip SCC Register 0* on page 3-11.

Note

Chip-select remap operates only when you have selected SMC mapping to 0x0. See *Test chip SCC Register 0* on page 3-11.

The processor fetches its first instructions from address 0x0, but the actual memory read depends on the remapped memory region. See *Test chip SCC Register 0* on page 3-11.

Memory remapping at power-on during run-time

You can configure the remap option at power-on or during run time.

Remapping at power-on

Use the `board.txt` file if the remap option is required when the processor starts from a reset. The `SCC: 0x000` entry in the `board.txt` file controls the settings for the SCC register CFGRW0. See the *Versatile Express Configuration Technical Reference Manual*.

Remapping during run time

Write directly to the SCC register CFGRW0 to change remapping after power-on. See *Test chip SCC Register 0* on page 3-11. See the Boot Monitor `sys_boot.s` file for an example of reconfiguring while running.

Caution

ARM recommends that you use the configuration file rather than directly writing to the control registers. You must perform remapping during run-time with care. You must not do this when code is running from the remapped area.

3.2.2 Overview of the memory map for the on-chip peripherals

Figure 3-2 on page 3-6 shows the on-chip peripheral memory map.

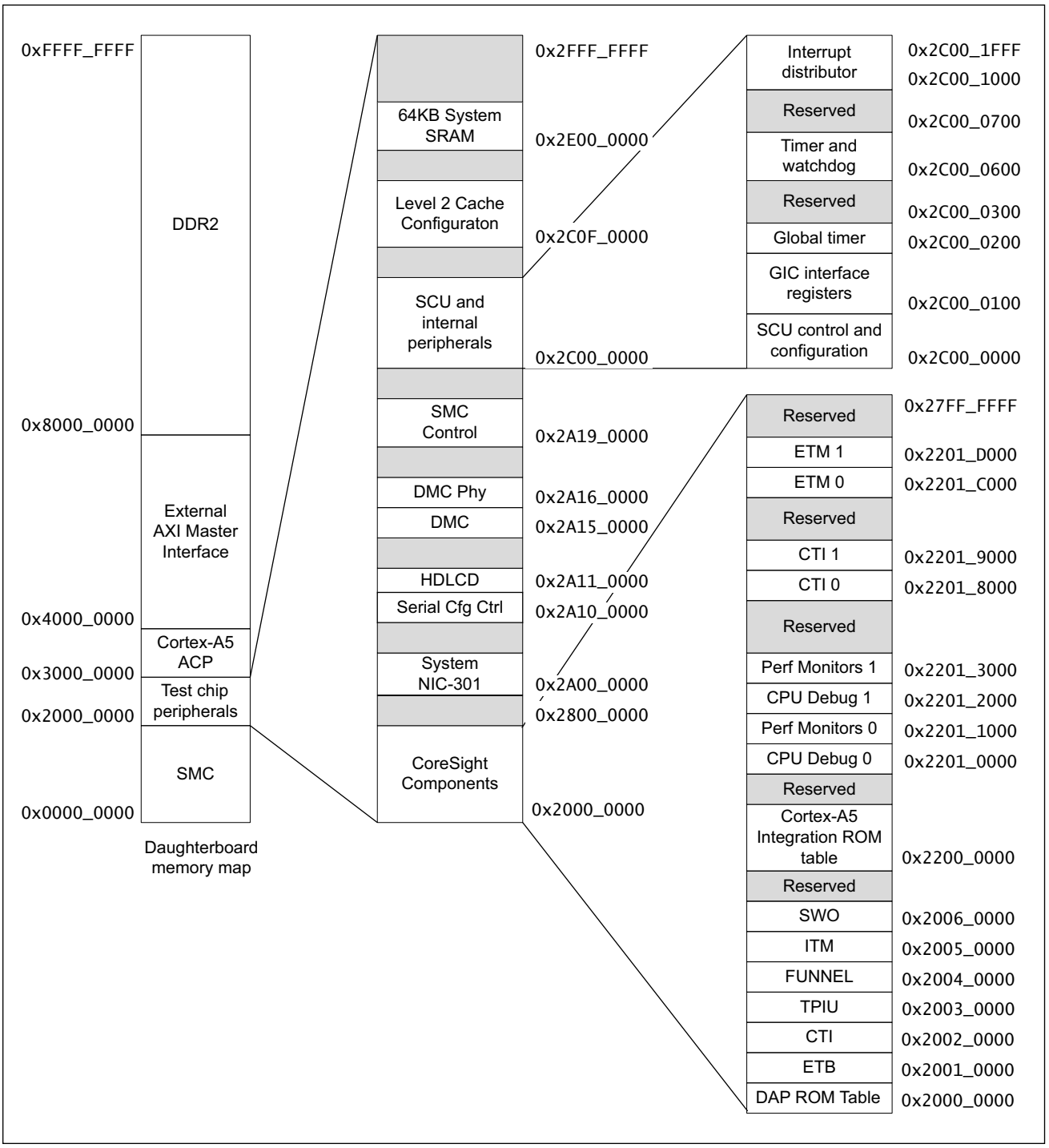


Figure 3-2 Cortex-A5 MPCore on-chip peripheral memory map

3.3 Programmable peripherals and interfaces

The following sections describe the configurable modules in the test chip:

- *Cortex-A5 MPCore cluster*
- *AMBA network interconnect, NIC-301* on page 3-8
- *HDLCD controller* on page 3-8
- *L2 cache controller, L2C-310* on page 3-8
- *PrimeCell DDR2 DMC interface, PL341* on page 3-8
- *PrimeCell SMC dual SRAM memory interface, PL354* on page 3-9
- *Test chip SCC registers* on page 3-10.

See also the reference manual for the peripheral for more information on programming these devices.

3.3.1 Cortex-A5 MPCore cluster

The Cortex-A5 MPCore cluster consists of a Cortex-A5 MPCore multiprocessor that includes two Cortex-A5 CPUs with NEON media processing technology. The L1 memory subsystem has 32KB of instruction cache and 32KB of data cache for each CPU.

The MPCore cluster contains the following programmable devices located at `2C000000`:

- Snoop Control Unit.
- GIC consisting of:
  - Controller.
  - Distributor.
- Global timer.
- One private timer and one watchdog for each core.

For information about the programmable devices within the Cortex-A5 MPCore processor, see the *Cortex-A5 MPCore Technical Reference Manual*.

3.3.2 AMBA network interconnect, NIC-301

The configuration interface for this component is located at address `0x2A000000` on the system *Advanced Peripheral Bus* (APB).

The frequency of the internal AXI clock is fixed at half the frequency of **CPUCLK**.

See the *AMBA Network Interconnect (NIC-301) Technical Reference Manual*.

3.3.3 HDLCD controller

The base memory address of the HDLCD controller is `2A110000`. See Appendix B *HDLCD controller* for a full description of the HDLCD video controller.

3.3.4 L2 cache controller, L2C-310

The configuration for the L2 cache controller is as follows:

- The L2 control register has 4KB of memory space. This page is located at address `0x2C0F0000`.
- The L2 memory consists of 256KB of L2 unified cache. You can change the actual amount of L2 memory used by writing to the L2 control registers.
- The Way Size is 32KB, 8-way associative.
- The L2 cache controller does not use parity.
- The L2 cache controller does not support address filtering.
- The L2 cache controller does not support *Intelligent Energy Management* (IEM).
- The L2 cache controller and the Cortex-A5 MPCore multiprocessor are synchronous. L2 cache operates at the core frequency and **CPUCLK** drives it.
- The L2 RAM operates at the same frequency as the L2 cache controller. The controller generates the clocking for the RAM.
- You can enable the L2 cache controller using the L2 control register. The L2 cache is disabled by default.

See the *AMBA Level 2 Cache Controller (L2C-310) Technical Reference Manual*.

3.3.5 PrimeCell DDR2 DMC interface, PL341

The configuration for the DDR2 DMC interface in the test chip is as follows:

- The DDR2 DMC configuration register has 4KB of address space. This page is located at address `0x2A150000`.
- 64-bit AXI data width and 64-bit external bus width.
- One chip-select.
- The PL341 AXI interface runs synchronously to the internal AXI interconnect, NIC-301. The external memory interface for the DDR2 memory devices runs asynchronously at the frequency that OSCCLK2 defines. See the example `board.txt` file in section *Versatile Express Configuration Technical Reference Manual* for information on how to set OSCCLK2.
- Arbitration FIFO depth of 16 stages.

- Read data FIFO depth of 32 stages.
- Write data FIFO depth of 32 stages.
- Three exclusive access monitors.

See the *PrimeCell DDR2 Dynamic Memory Controller (PL341) Technical Reference Manual*.

Note

The DDR2 Dynamic Memory Controller settings typically do not require user adjustment.

For software configuration information, see the following file:

`\BootMonitor\Firmware\Platform\Source\sys_dmc_v2p_ca5.s`.

3.3.6 PrimeCell SMC dual SRAM memory interface, PL354

This section contains information about the PrimeCell SMC dual SRAM memory interface in the following subsections:

- *SMC organization*
- *SMC configuration*
- *PrimeCell External Bus Interface, PL220*.

SMC organization

The SMC accesses devices using the following chip selects:

CS0 NOR flash 0 on the motherboard.
CS1 PSRAM.
CS2 Video/ETH/USB.
CS3 system registers and peripherals.
CS4 NOR flash 1 on the motherboard.
CS5 Reserved.
CS6 Reserved.
CS7 Reserved.

SMC configuration

The configuration for the dual SRAM memory interface is as follows:

- The dual SRAM memory interface configuration register has 4KB of address space. This page is located at address `0x2A190000`.
- 64-bit AXI data width and 32-bit memory data width.
- Eight chip selects on each interface.
- The dual SRAM memory interface is asynchronous to asynchronous CPU clock and runs from OSCCLK5.

See the *PrimeCell Static Memory Controller (PL350 series) Technical Reference Manual* for more information.

PrimeCell External Bus Interface, PL220

A PL220 *External Bus Interface* (EBI) multiplexes the dual SRAM memory interface to reduce pin count and to facilitate board layout.

See the *PrimeCell External Bus Interface (PL220) Technical Reference Manual* for more information.

3.3.7 Test chip SCC registers

The SCC register interface enables configuration of power-up in addition to reading and writing of system parameters. The SCC registers use a dedicated interface to the Daughterboard Configuration Controller that communicates with the MCC over an SPI interface.

The MCC on the motherboard reads the `config.txt` and `board.txt` configuration files and uses the Daughterboard Configuration Controller to configure the motherboard and attached daughterboards. The Daughterboard Configuration Controller loads some of the registers in the test chip SCC.

Run-time read and write operations are performed through the SYS_CFG registers, or directly through the APB interface at base address `0x2A100000`.

Note

ARM recommends that, where possible, you perform all system configuration by loading configuration files into the flash memory on the motherboard rather than writing directly to the test chip controller. The settings in the `board.txt` file are applied to the daughterboard before reset is released.

Interface to test chip SCC

You can read from and write to the Cortex-A5 MPCore test chip SCC registers:

- The interface supports word writes to the configuration controller registers.
- Writes to read-only registers are ignored.
- Writes to unused words fail. ARM recommends that you use a read-modify-write sequence to update the configuration controller registers.
- Read accesses to the peripheral support reading back 32 bits of the register at a time.
- Reads from unused words in the register return zero.
- The base address of the SCC registers is `0x2A100000`.

Table 3-2 shows the configuration registers and corresponding offsets from the base memory address. The offsets are also their `board.txt` entries.

Table 3-2 Test chip SCC register summary

Offset	Name	Type	Reset	Description
`SCC: 0x000`	CFGRW0	RW	`0x400F0000`	*Test chip SCC Register 0* on page 3-11.
`SCC: 0x004`	CFGRW1	RW	`0x40882110`	*Test chip SCC Register 1* on page 3-12.
`SCC: 0x010`	CFGRW2	RW	`0x14FC00FC`	*Test chip SCC Register 2* on page 3-14.
`SCC: 0x014`	CFGRW3	RW	`0x01CFC18FC`	*Test chip SCC Register 3* on page 3-14.
`SCC: 0x018`	CFGRW4	RW	`0x10FC0CFC`	*Test chip SCC Register 4* on page 3-15.
`SCC: 0x01C`	CFGRW5	RW	`0x08FC04FC`	*Test chip SCC Register 5* on page 3-16.
`SCC: 0x190`	CFGRW6	RO	`0x07220477`	*Test chip SCC Register 6* on page 3-16.

Table 3-2 Test chip SCC register summary (continued)

Offset	Name	Type	Reset	Description
SCC: 0x194	CFGRW7	RO	-	*Test chip SCC Register 7* on page 3-17.
SCC: 0x008-0xFF0	-	-	-	Reserved. Do not write to or read from these registers.
SCC: 0xFF4	APBCLEAR	WO	-	*Test chip SCC Register APBCLEAR* on page 3-17.
SCC: 0xFF8	DEVICEID	RO	0x00050387	*Test chip SCC Register DEVICEID* on page 3-18.
SCC: 0xFFC	CPUID	RO	0x410FC051	*Test chip SCC Register CPUID* on page 3-18.

Test chip SCC Register 0

The CFGRW0 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints CFGRW0[31:30] = 00 or 11 are reserved and must not be used. These bits are valid only if CFGRW0[0] is b0.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-3 shows the bit assignments.

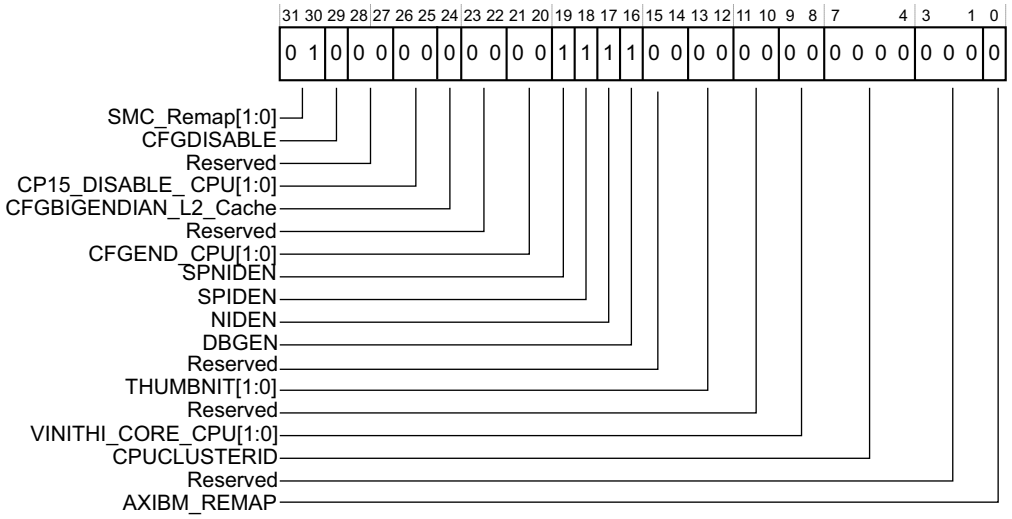


Figure 3-3 Test chip CFGRW0 Register bit assignments

Table 3-3 shows the bit assignments.

Table 3-3 Test chip CFGRW0 Register bit assignments

Bits	Name	Function
[31:30]	SMC remap	These map to the **SMC_REMAP[1:0]** bus: `b00` Reserved. `b01` CS0. `b10` CS4. `b11` Reserved. These bits are valid only if SMC is mapped to `0x0`, that is CFGRW0[0] = `b0`.
[29]	CFGDISABLE	GIC configuration disable.
[28:27]	-	Reserved. Do not modify.
[26:25]	CP15_DISABLE_CPU[1:0]	Maps to the **CP15_DISABLE_CPU[1:0]** bus.
[24]	CFGBIGENDIAN_L2_Cache	Maps to the **CFGBIGENDIAN_L2_Cache** signal.
[23:22]	-	Reserved. Do not modify.
[21:20]	CFGEND[1:0]	Maps to the **CFGEND[1:0]** bus. Configures CPUs as bigend.
[19]	SPNIDEN	Maps to the **SPNIDEN** secure non-invasive debug signal for both CPUs.
[18]	SPIDEN	Maps to the **SPIDEN** secure invasive debug signal for both CPUs.
[17]	NIDEN	Maps to the **NIDEN** non-invasive debug enable signal.
[16]	DBGEN	Maps to the **DBGEN** invasive debug enable signal.
[15:14]	-	Reserved. Do not modify.
[13:12]	THUMBNIT_CORE[1:0]	Thumbnit input for CPU[1:0]
[11:10]	-	Reserved. Do not modify.
[9:8]	VINITHI_CORE[1:0]	Vinithi input for CPU[1:0].
[7:4]	CLUSTERID	Maps to the **CLUSTERID[3:0]** bus.
[3:1]	-	Reserved. Do not modify.
[0]	AXIBM_REMAP	NIC-301 AMBA AXI memory map: `b0` SMC mapped to `0x0`. `b1` AXI Master interface mapped to `0x0`.

Test chip SCC Register 1

The CFGRW1 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints There are no usage constraints.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-4 on page 3-13 shows the bit assignments.

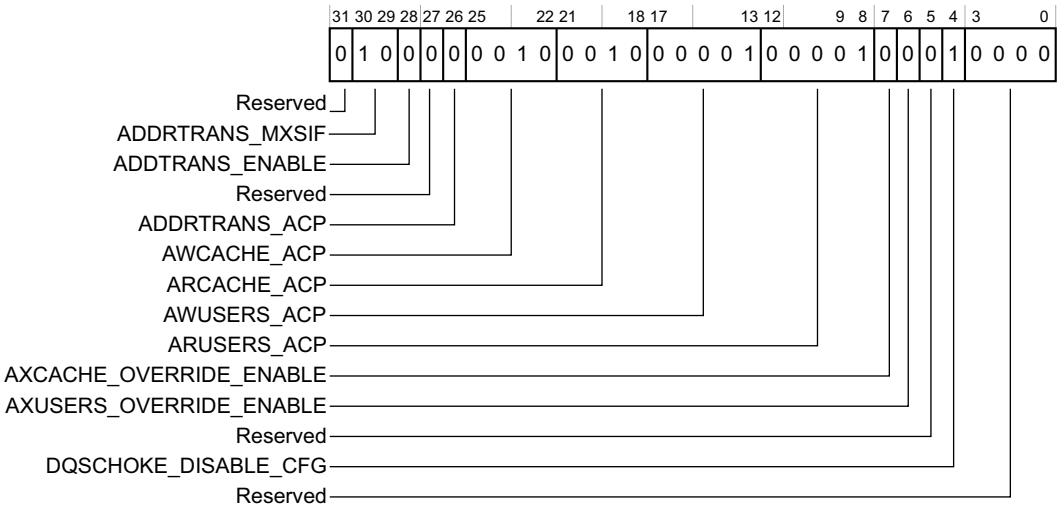


Figure 3-4 Test chip CFGRW1 Register bit assignments

Table 3-4 shows the bit assignments.

Table 3-4 Test chip CFGRW1 register bit assignments

Bits	Name	Function
[31]	-	Reserved. Do not modify.

[30:29]	ADDRTRANS_MXSIF	Translates External Slave Interface address by overriding bits [31:30] of AxADDR:
		`b00` `0x0000_0000`
		`b10` `0x8000_0000`
		`b11` `0xC000_0000`
		For V2P-CA5s, `0xC000_0000` is aliased to `0x8000_000`.

[28]	ADDRTRANS_ENABLE	Enables external slave interface address translation.
[27]	-	Reserved. Do not modify.

[26]	ADDRTRANS_ACP	Translates the ACP address by overriding bit 28 of AxADDR of the cluster ACP port.
		`b0` `0xE000_0000`
		For V2 A5, `0xE000_0000` is aliased to `0xA000_0000`.
		`b1` `0xF000_0000`
		For V2P-CA5s, `0xF000_0000` is aliased to `0xB000_000`.

[25:22]	AWCACHE_ACP	ACP AWCACHE override, default cacheable but do not allocate.
[21:18]	ARCACHE_ACP	ACP ARCACHE override, default cacheable but do not allocate.
[17:13]	AWUSERS_ACP	ACP AWUSERS override, default shareable.
[12:8]	ARUSERS_ACP	ACP ARUSERS override, default shareable.
[7]	AXCACHE_OVERRIDE_ENABLE	Enables override of caching attributes on the CPU coherency port.
[6]	AXUSERS_OVERRIDE_ENABLE	Enables override of share attributes on the CPU coherency port.

Table 3-4 Test chip CFGRW1 register bit assignments (continued)

Bits	Name	Function
[5]	-	Reserved. Do not modify.
[4]	DQSCHOKE_DISABLE_CFG	Disable internal masking of DQS in between DDR2 reads.
[3:0]	-	Reserved. Do not modify.

Test chip SCC Register 2

The CFGRW2 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints There are no usage constraints.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-5 shows the bit assignments.

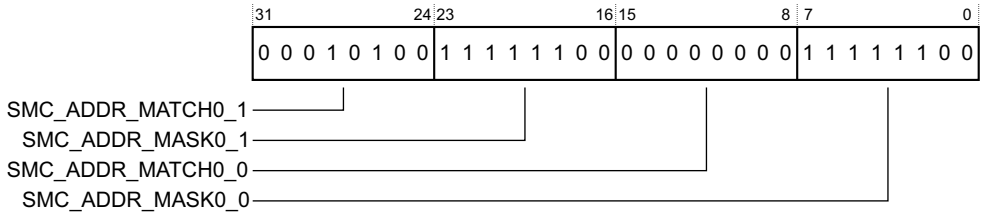


Figure 3-5 Test chip CFGRW2 Register bit assignments

Table 3-5 shows the bit assignments.

Table 3-5 Test chip CFGRW2 Register bit assignments

Bits	Name	Function
[31:24]	SMC_ADDR_MATCH0_1	SMC CS1 address match of top 8 bits
[23:16]	SMC_ADDR_MASK0_1	SMC CS1 address mask of top 8 bits
[15:8]	SMC_ADDR_MATCH0_0	SMC CS0 address match of top 8 bits
[7:0]	SMC_ADDR_MASK0_0	SMC CS0 address mask of top 8 bits

Test chip SCC Register 3

The CFGRW3 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints There are no usage constraints.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-6 on page 3-15 shows the bit assignments.

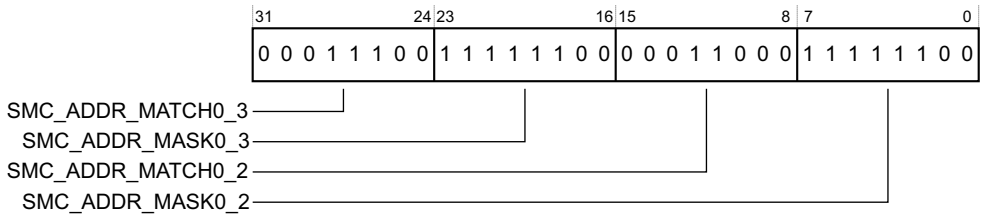


Figure 3-6 Test chip CFGRW3 Register bit assignments

Table 3-6 shows the bit assignments.

Table 3-6 Test chip CFGRW3 Register bit assignments

Bits	Name	Function
[31:24]	SMC_ADDR_MATCH0_3	SMC CS3 address match of top 8 bits
[23:16]	SMC_ADDR_MASK0_3	SMC CS3 address mask of top 8 bits
[15:8]	SMC_ADDR_MATCH0_2	SMC CS2 address match of top 8 bits
[7:0]	SMC_ADDR_MASK0_2	SMC CS2 address mask of top 8 bits

Test chip SCC Register 4

The CFGRW4 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints There are no usage constraints.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-7 shows the bit assignments.

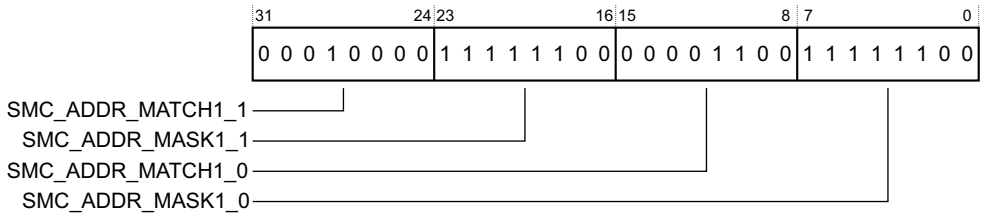


Figure 3-7 Test chip CFGRW4 Register bit assignments

Table 3-7 shows the bit assignments.

Table 3-7 Test chip CFGRW4 Register bit assignments

Bits	Name	Function
[31:24]	SMC_ADDR_MATCH1_1	SMC CS5 address match of top 8 bits
[23:16]	SMC_ADDR_MASK1_1	SMC CS5 address mask of top 8 bits
[15:8]	SMC_ADDR_MATCH1_0	SMC CS4 address match of top 8 bits
[7:0]	SMC_ADDR_MASK1_0	SMC CS4 address mask of top 8 bits

Test chip SCC Register 5

The CFGRW5 Register characteristics are:

Purpose Enables you to read and write test chip configuration settings.

Usage constraints There are no usage constraints.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-8 shows the bit assignments.

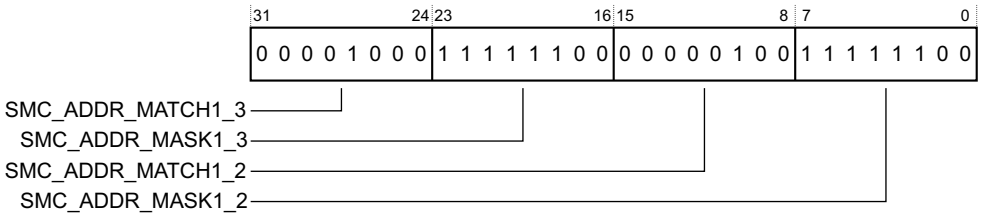


Figure 3-8 Test chip CFGRW5 Register bit assignments

Table 3-8 shows the bit assignments.

Table 3-8 Test chip CFGRW5 Register bit assignments

Bits	Name	Function
[31:24]	SMC_ADDR_MATCH1_3	SMC CS7 address match of top 8 bits
[23:16]	SMC_ADDR_MASK1_3	SMC CS7 address mask of top 8 bits
[15:8]	SMC_ADDR_MATCH1_2	SMC CS6 address match of top 8 bits
[7:0]	SMC_ADDR_MASK1_2	SMC CS6 address mask of top 8 bits

Test chip SCC Register 6

The CFGRW6 Register characteristics are:

Purpose Enables you to read the DAP ROM default target ID.

Usage constraints This register is read only.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-9 shows the bit assignments.

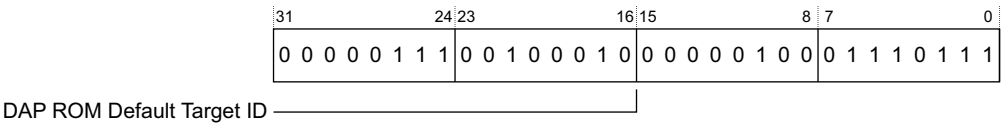


Figure 3-9 Test chip CFGRW6 Register bit assignments

Table 3-9 shows the bit assignments.

Table 3-9 Test chip CFGRW6 Register bit assignments

Bits	Name	Function
[31:0]	-	DAP ROM default target ID

Test chip SCC Register 7

The CFGRW7 Register characteristics are:

Purpose Enables you to read the DAP ROM default instance ID.

Usage constraints This register is read only.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-10 shows the bit assignments.

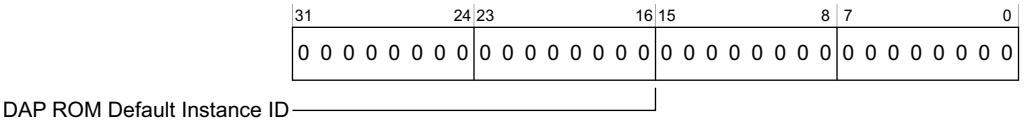


Figure 3-10 Test chip CFGRW7 Register bit assignments

Table 3-10 shows the bit assignments.

Table 3-10 Test chip CFGRW7 Register bit assignments

Bits	Name	Function
[31:0]	-	DAP ROM default instance ID

Test chip SCC Register APBCLEAR

The APBCLEAR Register characteristics are:

Purpose Writing `0xA50FF05A` to this register reverts the serial control registers to the values loaded through the serial configuration values.

Usage constraints This register is write-only.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-11 shows the bit assignments.

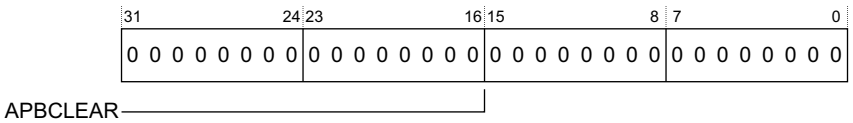


Figure 3-11 Test chip APBCLEAR Register bit assignments

Table 3-11 shows the bit assignments.

Table 3-11 Test chip APBCLEAR Register bit assignments

Bits	Name	Function
[31:0]	-	Writing `0xA50FF05A` to this register reverts the serial control registers to the values loaded through the serial configuration values.

Test chip SCC Register DEVICEID

The DEVICEID Register characteristics are:

Purpose Enables you to read the Cortex-A5 MPCore test chip specific device ID.

Usage constraints This register is read-only.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-12 shows the bit assignments.

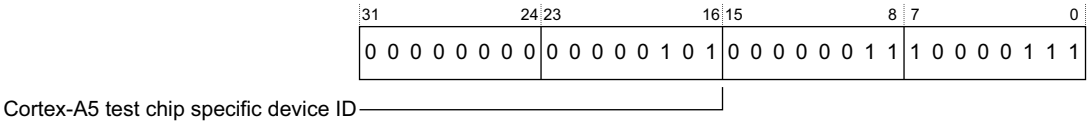


Figure 3-12 Test chip DEVICEID Register bit assignments

Table 3-12 shows the bit assignments.

Table 3-12 Test chip DEVICEID Register bit assignments

Bits	Name	Function
[31:0]	-	Cortex-A5 test chip device ID

Test chip SCC Register CPUID

The CPUID Register characteristics are:

Purpose Enables you to read the Cortex-A5 MPCore test chip CPU ID.

Usage constraints This register is read-only.

Configurations Available in all CoreTile Express A5x2 daughterboard configurations.

Attributes See Table 3-2 on page 3-10.

Figure 3-13 shows the bit assignments.

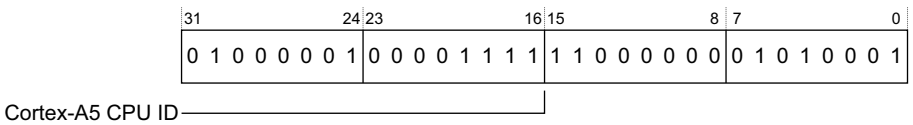


Figure 3-13 Test chip CPUID Register bit assignments

Table 3-13 shows the bit assignments.

Table 3-13 Test chip CPUID Register bit assignments

Bits	Name	Function
[31:0]	-	Cortex-A5 CPU ID

Test chip SCC Registers `0x008-0xFF0`

These registers are reserved. You must not attempt to write to or read from them.

Appendix A
Signal Descriptions

This appendix describes the signals present at the interface connectors. It contains the following sections:

- *Daughterboard connectors* on page A-2
- *HDRX HSB multiplexing scheme* on page A-3
- *Header Connectors* on page A-5
- *Debug and trace connectors* on page A-6
- *SO-DIMM connector* on page A-9.

Note

See also the *Motherboard Express µATX Technical Reference Manual*.

A.1 Daughterboard connectors

Figure A-1 shows the connectors fitted to the daughterboard.

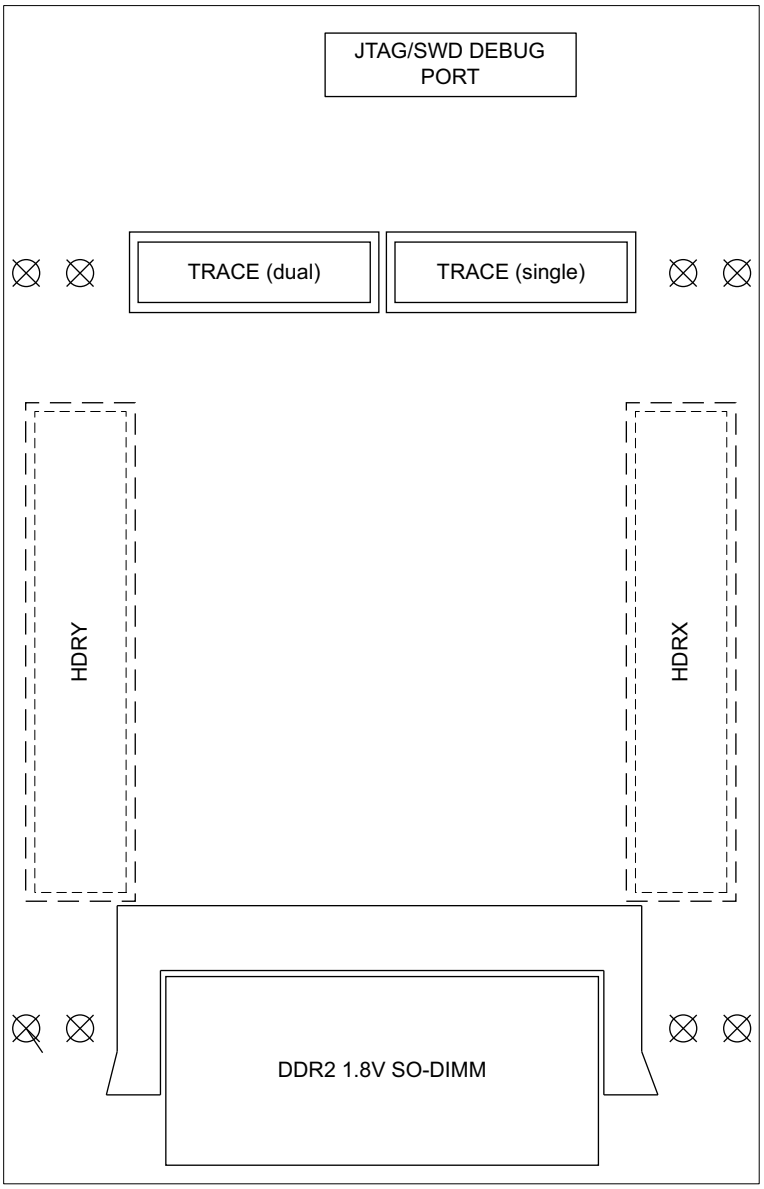


Figure A-1 CoreTile Express A5x2 daughterboard connectors

Note

The header connectors, HDRY and HDRX, shown as dashed lines in Figure A-1, are on the lower face of the board, that is, the face of the board that connects to the motherboard. The other connectors, shown as solid lines, are on the upper face of the board.

A.2 HDRX HSB multiplexing scheme

A bus multiplexing scheme is necessary to reduce the number of pins required on the HDRX header for the 64-bit AXI master and slave on the HSBM and HSBS buses. The LogicTile Express daughterboard must implement a similar multiplexing scheme to be compatible with the CoreTile Express signals.

OSCCLK1, on the CoreTile Express A5x2 daughterboard, generates the AXI master bus clock. This clocks the test chip master multiplex and demultiplex logic. This logic is positive- and negative-edge triggered to avoid the requirement for a PLL or double-rate clock in the test chip. Double-edge clocking also enables operation at low speed for use with emulation systems.

The AXI slave bus uses a similar method, but the clock source is on site 2. See Figure A-2.

Note

All signals on the **HSB (M)** and **HSB (S)** buses are 1.8V.

Figure A-2 shows a simplified block diagram of the multiplexing scheme for the two AXI buses.

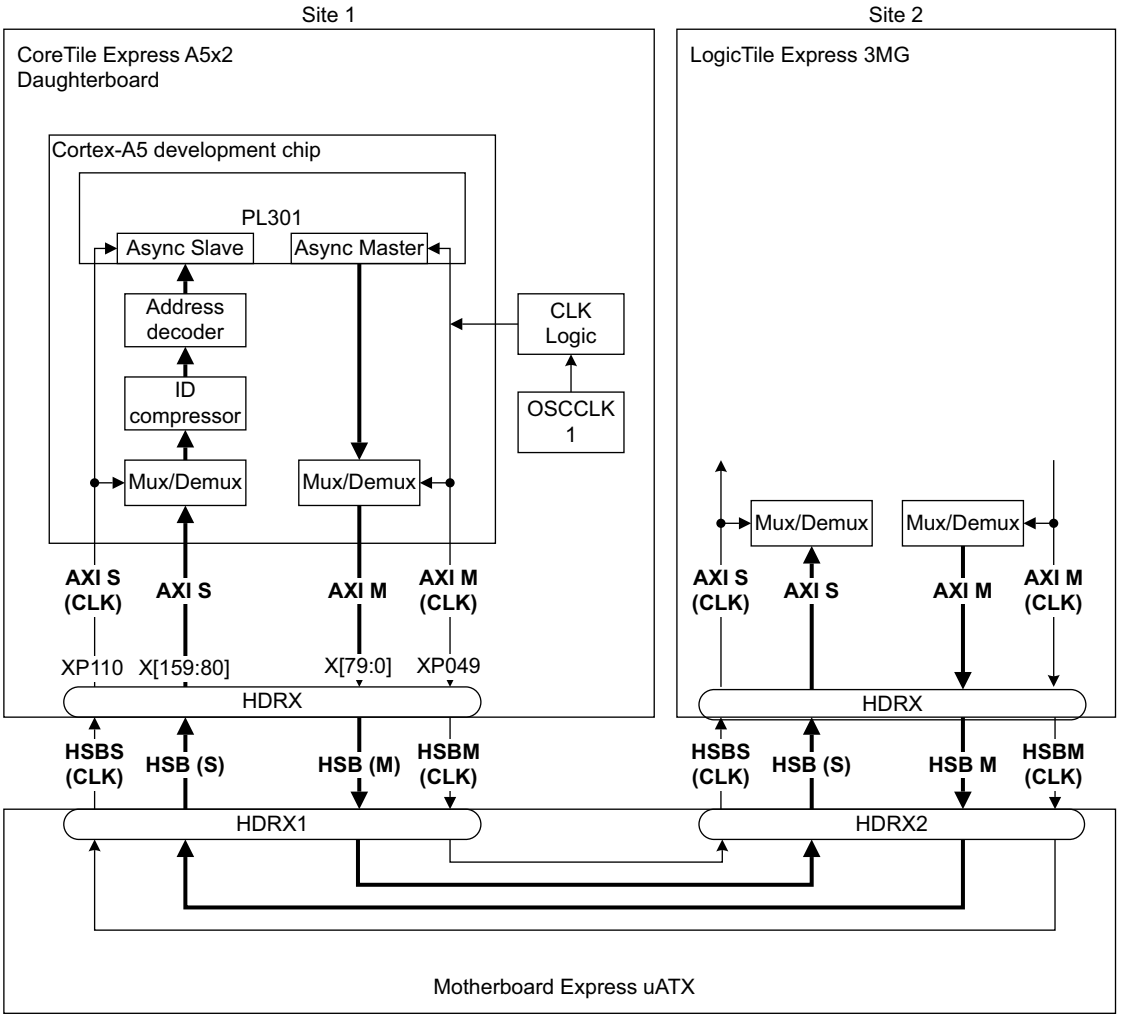


Figure A-2 HSB multiplexing

Application note AN243, *Example LogicTile Express 3MG design for a CoreTile Express A5x2*, provided by ARM, implements an example AMBA system using a LogicTile Express 3MG daughterboard to interconnect with the CoreTile Express A5x2 daughterboard. See the documentation supplied on the accompanying media and the *Application Notes* listing for more information at, http://infocenter.arm.com.

A.3 Header Connectors

There are two high-density headers fitted to the underside of the daughterboard. These headers, designated HDRX, J1, and HDRY, J2, route the signal and power interconnect to the motherboard and to the other daughterboard site. See the `an243_revx.ucf` constraints files, available in application note AN243, *Example LogicTile Express 3MG design for a CoreTile Express A5x2*.

A.4 Debug and trace connectors

This section describes the debug and trace connectors on the daughterboard.

Caution

- Your external debug interface unit must adapt its interface voltages to the voltage level of the daughterboard JTAG. All the trace and JTAG signals operate at 1.8V.
- There is no guaranteed support for JTAG on the trace connector. Use the dedicated JTAG connector on the daughterboard.

A.4.1 JTAG connector

The JTAG connector is provided on the daughterboard to enable connection of DSTREAM, or a compatible third-party debugger. Figure A-3 shows that the P-JTAG connector, J5, is connected to FPGA 2.

Note

- **DBGRQ** has a pull-down resistor to 0V. **DBGACK** has no pull-up or pull-down resistor. All other signal connections on the P-JTAG connector have pull-up resistors to 1V8.
- Pins 7 and 9 of the JTAG connector are dual mode pins that enable the Cortex-A5 MPCore test chip to support both the JTAG and SWD protocols.

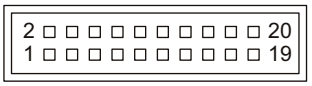


Figure A-3 JTAG connector, J5

Table A-1 shows the JTAG pin mapping for each JTAG signal.

Table A-1 P-JTAG connector, J5, signal list

Pin	Signal	Pin	Signal
1	**VIREF**	2	**VSUPPLYA**
3	**nTRST**	4	**GND**
5	**TDI**	6	**GND**
7	**TMS/SWDIO**	8	**GND**
9	**TCK/SWCLK**	10	**GND**
11	**RTCK**	12	**GND**
13	**TDO**	14	**GND**
15	**nSRST**	16	**GND**
17	**DBGRQ**	18	**GND**
19	**DBGACK**	20	**GND**

A.4.2 Trace connectors

The test chip supports up to 32-bit trace output from the CoreSight *Trace Port Interface Unit* (TPIU) and enables connection of a compatible trace unit. See Figure 2-14 on page 2-25. Two MICTOR trace connectors, labeled *Trace Dual* and *Trace Single*, are connected to the TPIU. The two connectors used together support 32-bit trace, and the connector labeled *Trace Single*, used alone, supports 16-bit trace.

Note

- DSTREAM is an example of a trace module that can be used.
- All the trace and JTAG signals operate at 1.8V.
- The trace connector cannot supply power to a trace unit.
- The interface does not support the **TRACECTL** signal. This is always driven LOW.

Figure A-4 shows the MICTOR connector, part number AMP 2-5767004-2.

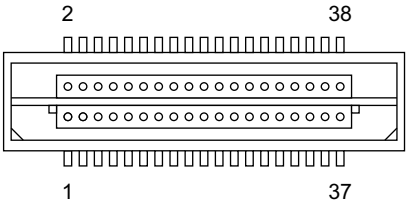


Figure A-4 Trace Connector, J6 and J7

Table A-2 shows the trace pin mapping for each *Trace Dual* signal.

Table A-2 Trace Single connector, J6, signal list

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKA**
7	**TRACEDBGRQ**	8	**TRACEDBGACK**
9	**nSRST**	10	**TRACEEXTTRIGX**
11	**TDO**	12	**VTREFA**, 1V8
13	**RTCK**	14	**VSUPPYLYA**, 1V8
15	**TCK**	16	**TRACEDATA7**
17	**TMS**	18	**TRACEDATA6**
19	**TDI**	20	**TRACEDATA5**
21	**nTRST**	22	**TRACEDATA4**
23	**TRACEDATA15**	24	**TRACEDATA3**
25	**TRACEDATA14**	26	**TRACEDATA2**
27	**TRACEDATA13**	28	**TRACEDATA1**
29	**TRACEDATA12**	30	**GND**

Table A-2 Trace Single connector, J6, signal list (continued)

Pin	Signal	Pin	Signal
31	**TRACEDATA11**	32	**GND**
33	**TRACEDATA10**	34	**VTREFA**, 1V8
35	**TRACEDATA9**	36	**TRACECTL**
37	**TRACEDATA8**	38	**TRACEDATA0**

Table A-3 shows the trace pin mapping for each *Trace Single* signal.

Table A-3 Trace Dual connector, J7, signal list

Pin	Signal	Pin	Signal
1	Not connected	2	Not connected
3	Not connected	4	Not connected
5	**GND**	6	**TRACECLKB**
7	Not connected	8	Not connected
9	Not connected	10	Not connected
11	Not connected	12	**VTREF**, 1V8
13	Not connected	14	Not connected
15	Not connected	16	**TRACEDATA23**
17	Not connected	18	**TRACEDATA22**
19	Not connected	20	**TRACEDATA21**
21	Not connected	22	**TRACEDATA20**
23	**TRACEDATA31**	24	**TRACEDATA19**
25	**TRACEDATA30**	26	**TRACEDATA18**
27	**TRACEDATA29**	28	**TRACEDATA17**
29	**TRACEDATA28**	30	**GND**
31	**TRACEDATA27**	32	**GND**
33	**TRACEDATA26**	34	**VTREF**, 1V8
35	**TRACEDATA25**	36	**GND**
37	**TRACEDATA24**	38	**TRACEDATA16**

A.5 SO-DIMM connector

The SO-DIMM connector is on the upper face of the board, facing away from the motherboard, and drives 1GB of 64-bit DDR2 memory. You can download the signal list and connector information from the JEDEC web site. See *Other publications* on page x.

Note

ARM recommends that you use the SO-DIMM memory supplied with the CoreTile Express A5x2 daughterboard. ARM does not recommend using alternative DIMMs.

Appendix B
HDLCD controller

This appendix describes the HDLCD controller. It contains the following sections:

- *About the HDLCD controller* on page B-2
- *HDLCD programmers model* on page B-3.

B.1 About the HDLCD controller

This appendix describes the LCD controller supporting *High Definition* (HD) resolutions.

The HDLCD controller has the following features:

- Resolution:
  - 2048×2048, sufficient for full 1080p HDTV resolution.
- Frame buffer:
  - Supports all common non-indexed RGB formats.
  - Frame buffer can be placed anywhere in memory.
  - Scan lines must be a multiple of 8 bytes long, and aligned to 8-byte boundaries. There are no other restrictions on size or placement. Line pitch configurable in multiples of 8 bytes.
- Management:
  - Frame buffer address can be updated at any time, and applies from the next full frame.
  - Frame buffer size, color depth, and timing can only be changed while the display is disabled.
- Maskable interrupts:
  - DMA-end, last part of frame read from bus.
  - VSYNC.
  - Underrun.
  - Bus error.
- Color depths:
  - Supports 8-bit per color. Frame buffers with other color depths are truncated or interpolated to 8 bits per component.
- Interfaces:
  - AMBA 3 APB interface for configuration.
  - Read-only AXI bus for frame buffer reads.
  - Standard LCD external interface. All timings and polarities are configurable.
  - APB, AXI, and pixel clock can run on separate asynchronous clocks.
- Buffering:
  - Internal 1KB buffer.
  - After underrun, it blanks the rest of the frame and resynchronizes from the next frame.

B.2 HDLCD programmers model

This section describes the programmers model. It contains the following subsections:

- *About the HDLCD controller programmers model*
- *Register summary*
- *Register descriptions* on page B-4.

B.2.1 About the HDLCD controller programmers model

The following information applies to the HDLCD controller registers:

- The base address is not fixed, and can be different for any particular system implementation. The offset of each register from the base address is fixed.
- Do not attempt to access reserved or unused address locations. Attempting to access these locations can result in UNPREDICTABLE behavior.
- Unless otherwise stated in the accompanying text:
  - Do not modify undefined register bits.
  - Ignore undefined register bits on reads.
  - All register bits are reset to a logic 0 by a system or power-on reset.
- Access type in Table B-1 is described as follows:
  RW Read and write.
  RO Read only.
  WO Write only.

B.2.2 Register summary

Table B-1 shows the registers in offset order from the base memory address. The base memory address of the HDLCD controller on the Cortex-A5 MPCore test chip is `0x2A11_0000`.

Table B-1 Register summary

Offset	Name	Type	Reset	Width	Description
`0x0000`	VERSION	RO	VERSION	32	*Version Register* on page B-4
`0x0010`	INT_RAWSTAT	RW	`0x0`	32	*Interrupt Raw Status Register* on page B-5
`0x0014`	INT_CLEAR	WO	N/A	32	*Interrupt Clear Register* on page B-6
`0x0018`	INT_MASK	RW	`0x0`	32	*Interrupt Mask Register* on page B-7
`0x001C`	INT_STATUS	RO	`0x0`	32	*Interrupt Status Register* on page B-8
`0x0100`	FB_BASE	RW	`0x0`	32	*Frame Buffer Base Address Register* on page B-9
`0x0104`	FB_LINE_LENGTH	RW	`0x0`	32	*Frame Buffer Line Length Register* on page B-9
`0x0108`	FB_LINE_COUNT	RW	`0x0`	32	*Frame Buffer Line Count Register* on page B-10
`0x010C`	FB_LINE_PITCH	RW	`0x0`	32	*Frame Buffer Line Pitch Register* on page B-11
`0x0110`	BUS_OPTIONS	RW	`0x408`	32	*Bus Options Register* on page B-11
`0x0200`	V_SYNC	RW	`0x0`	32	*Vertical Synch Width Register* on page B-12
`0x0204`	V_BACK_PORCH	RW	`0x0`	32	*Vertical Back Porch Width Register* on page B-13
`0x0208`	V_DATA	RW	`0x0`	32	*Vertical Data Width Register* on page B-13

Table B-1 Register summary (continued)

Offset	Name	Type	Reset	Width	Description
0x020C	V_FRONT_PORCH	RW	0x0	32	*Vertical Front Porch Width Register* on page B-14
0x0210	H_SYNC	RW	0x0	32	*Horizontal Synch Width Register* on page B-14
0x0214	H_BACK_PORCH	RW	0x0	32	*Horizontal Back Porch Width Register* on page B-15
0x0218	H_DATA	RW	0x0	32	*Horizontal Data Width Register* on page B-15
0x021C	H_FRONT_PORCH	RW	0x0	32	*Horizontal Front Porch Width Register* on page B-16
0x0220	POLARITIES	RW	0x0	32	*Polarities Register* on page B-17
0x0230	COMMAND	RW	0x0	32	*Command Register* on page B-17
0x0240	PIXEL_FORMAT	RW	0x0	32	*Pixel Format Register* on page B-18
0x0244	RED_SELECT	RW	0x0	32	*Color Select Registers* on page B-19
0x0248	GREEN_SELECT	RW	0x0	32	*Color Select Registers* on page B-19
0x024C	BLUE_SELECT	RW	0x0	32	*Color Select Registers* on page B-19

B.2.3 Register descriptions

This section describes the HDLCD controller registers. Table B-1 on page B-3 provides cross references to individual registers.

Version Register

The VERSION Register characteristics are:

Purpose Holds a static version number for the LCD controller. Changes to the processor that affect registers and data structures increment the VERSION_MAJOR value and reset the VERSION_MINOR value.

Other changes that do not affect the binary compatibility only increment the VERSION_MINOR number.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD configurations.

Attributes See Table B-1 on page B-3.

Figure B-1 shows the bit assignments.

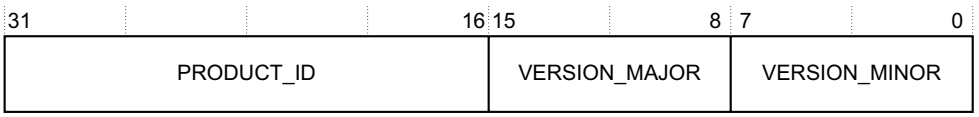


Figure B-1 Version Register bit assignments

Table B-2 shows the bit assignments.

Table B-2 Version Register bit assignments

Bits	Name	Function
[31:16]	PRODUCT_ID	Product ID number `0x1CDC`.
[15:8]	VERSION_MAJOR	These bits provide the major product version information. For release r0p0, the value is `0x00`.
[7:0]	VERSION_MINOR	These bits provide the minor product version information. For release r0p0, the value is `0x00`.

Interrupt Raw Status Register

The INT_RAWSTAT Register characteristics are:

Purpose Shows the unmasked status of the interrupt sources.

Writing a 1 to the bit of an interrupt source forces this bit to be set and generates an interrupt if it is not masked by the corresponding bit in the *Interrupt Mask Register* on page B-7.

Writing a 0 to the bit of an interrupt source has no effect.

Use the *Interrupt Clear Register* on page B-6 to clear interrupts.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-2 shows the bit assignments.

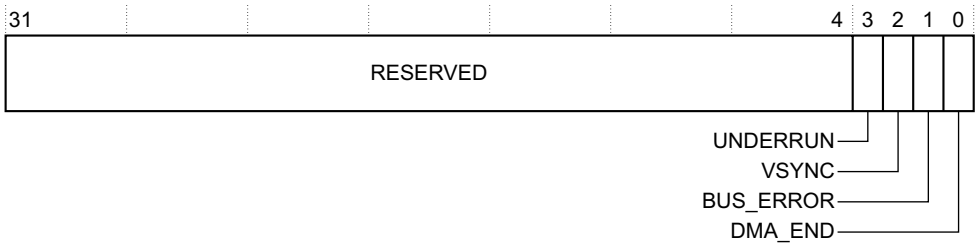


Figure B-2 Interrupt Raw Status Register bit assignments

Table B-3 shows the bit assignments.

Table B-3 Interrupt Raw Status Register bit assignments

Bits	Name	Function
[31:4]	-	Reserved. Write as zero, read undefined.
[3]	UNDERRUN	No data was available to display while **DATAEN** was active. This interrupt triggers if the controller does not have pixel data available to drive when **DATAEN** is active. When this occurs, the controller drives the default color for the rest of the screen and attempts to display the next frame correctly.

Table B-3 Interrupt Raw Status Register bit assignments (continued)

Bits	Name	Function
[2]	VSYNC	Vertical sync is active. This interrupt triggers at the moment the **VSYNC** output goes active.
[1]	BUS_ERROR	The DMA module received a bus error while reading data. This interrupt triggers if any frame buffer read operation ever reports an error.
[0]	DMA_END	The DMA module has finished reading a frame. This interrupt triggers when the last piece of data for a frame has been read. The DMA immediately continues on the next frame, so this interrupt only ensures that the frame buffer for the previous frame is no longer required.

Interrupt Clear Register

The INT_CLEAR Register characteristics are:

Purpose Clears interrupt sources. Writing a 1 to the bit of an asserted source clears the interrupt in the *Interrupt Raw Status Register* on page B-5, and in the *Interrupt Status Register* on page B-8 if it is not masked.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-3 shows the bit assignments.

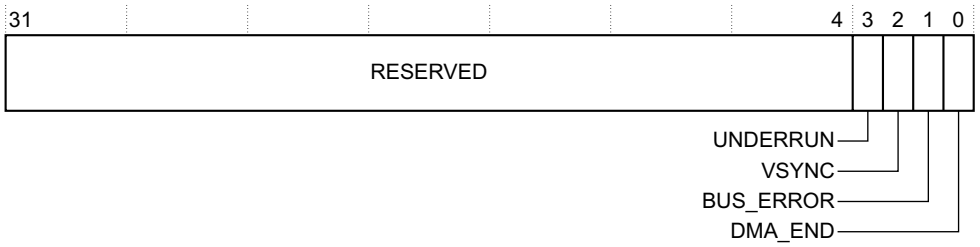


Figure B-3 Interrupt Clear Register bit assignments

Table B-4 shows the bit assignments.

Table B-4 Interrupt Clear Register bit assignments

Bits	Name	Function
[31:4]	-	Reserved. Write as zero.
[3]	UNDERRUN	No data was available to display while **DATAEN** was active. This interrupt triggers if the controller does not have pixel data available to drive when **DATAEN** is active. When this occurs, the controller drives the default color for the rest of the screen and attempts to display the next frame correctly.

Table B-4 Interrupt Clear Register bit assignments (continued)

Bits	Name	Function
[2]	VSYNC	Vertical sync is active. This interrupt triggers at the moment the **VSYNC** output goes active.
[1]	BUS_ERROR	The DMA module received a bus error while reading data. This interrupt triggers if any frame buffer read operation ever reports an error.
[0]	DMA_END	The DMA module has finished reading a frame. This interrupt triggers when the last piece of data for a frame has been read. The DMA immediately continues on the next frame, so this interrupt only ensures that the frame buffer for the previous frame is no longer required.

Interrupt Mask Register

The INT_MASK Register characteristics are:

Purpose Holds the bit mask that enables an interrupt source if the corresponding mask bit is set to 1.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-4 shows the bit assignments.

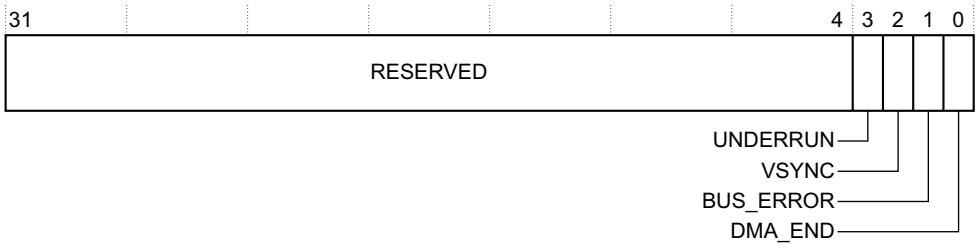


Figure B-4 Interrupt Mask Register bit assignments

Table B-5 shows the bit assignments.

Table B-5 Interrupt Mask Register bit assignments

Bits	Name	Function
[31:4]	-	Reserved. Write as zero, read undefined.
[3]	UNDERRUN	No data was available to display while **DATAEN** was active. This interrupt triggers if the controller does not have pixel data available to drive when **DATAEN** is active. When this occurs, the controller drives the default color for the rest of the screen and attempts to display the next frame correctly.

Table B-5 Interrupt Mask Register bit assignments (continued)

Bits	Name	Function
[2]	VSYNC	Vertical sync is active. This interrupt triggers at the moment the **VSYNC** output goes active.
[1]	BUS_ERROR	The DMA module received a bus error while reading data. This interrupt triggers if any frame buffer read operation ever reports an error.
[0]	DMA_END	The DMA module has finished reading a frame. This interrupt triggers when the last piece of data for a frame has been read. The DMA immediately continues on the next frame, so this interrupt only ensures that the frame buffer for the previous frame is no longer required.

Interrupt Status Register

The INT_STATUS Register characteristics are:

Purpose This register is the *Interrupt Raw Status Register* on page B-5 ANDed with the *Interrupt Mask Register* on page B-7 and shows the active and masked interrupt sources. Bits selected by the *Interrupt Mask Register* on page B-7 are active in the *Interrupt Status Register*. These bits show the status of the interrupt sources. Bits not selected by the Interrupt Mask are inactive. If any of the sources are asserted in the *Interrupt Status Register*, then the external **IRQ** line is asserted.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-5 shows the bit assignments.

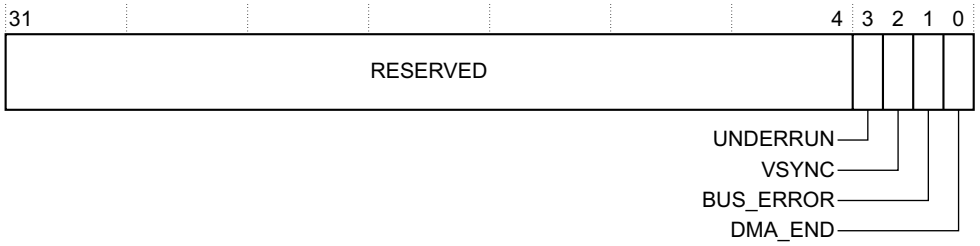


Figure B-5 Interrupt Status Register bit assignments

Table B-6 shows the bit assignments.

Table B-6 Interrupt Status Register bit assignments

Bits	Name	Function
[31:4]	-	Reserved, read undefined.
[3]	UNDERRUN	No data was available to display while **DATAEN** was active. This interrupt triggers if the controller does not have pixel data available to drive when **DATAEN** is active. When this occurs, the controller drives the default color for the rest of the screen and attempts to display the next frame correctly.
[2]	VSYNC	Vertical sync is active. This interrupt triggers at the moment the **VSYNC** output goes active.
[1]	BUS_ERROR	The DMA module received a bus error while reading data. This interrupt triggers if any frame buffer read operation ever reports an error.
[0]	DMA_END	The DMA module has finished reading a frame. This interrupt triggers when the last piece of data for a frame has been read. The DMA immediately continues on the next frame, so this interrupt only ensures that the frame buffer for the previous frame is no longer required.

Frame Buffer Base Address Register

The FB_BASE Register characteristics are:

Purpose Holds the address of the first pixel of the first line in the frame buffer.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-6 shows the bit assignments.

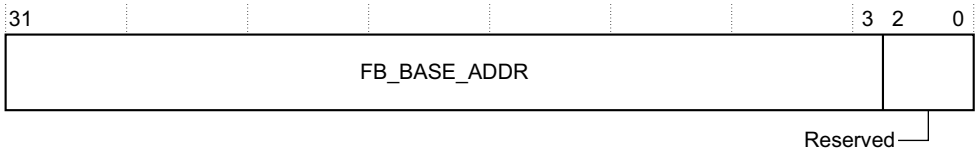


Figure B-6 Frame Buffer Base Address Register bit assignments

Table B-7 shows the bit assignments.

Table B-7 Frame Buffer Base Address Register bit assignments

Bits	Name	Function
[31:3]	FB_BASE_ADDR	Frame buffer base address
[2:0]	-	Reserved. Write as zero, read undefined.

Frame Buffer Line Length Register

The FB_LINE_LENGTH Register characteristics are:

Purpose Holds the length of each frame buffer line in bytes.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-7 shows the bit assignments.

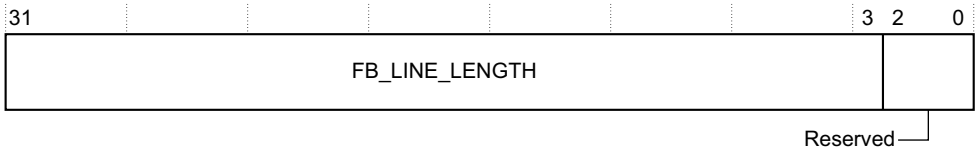


Figure B-7 Frame Buffer Line Length Register bit assignments

Table B-8 shows the bit assignments.

Table B-8 Frame Buffer Line Length Register bit assignments

Bits	Name	Function
[31:3]	FB_LINE_LENGTH	Frame buffer line length
[2:0]	-	Reserved. Write as zero, read undefined.

Frame Buffer Line Count Register

The FB_LINE_COUNT Register characteristics are:

Purpose Holds the number of lines to read from the frame buffer.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-8 shows the bit assignments.

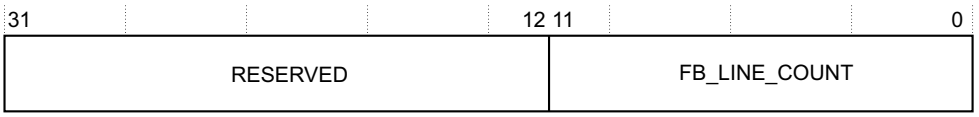


Figure B-8 Frame Buffer Line Count Register bit assignments

Table B-9 shows the bit assignments.

Table B-9 Frame Buffer Line Count Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	FB_LINE_COUNT	Frame buffer line count

Frame Buffer Line Pitch Register

The FB_LINE_PITCH Register characteristics are:

Purpose Holds the number of bytes between the start of one line in the frame buffer, and the start of the next line. This value is treated as a signed 2's complement number, enabling negative pitch if required.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-9 shows the bit assignments.

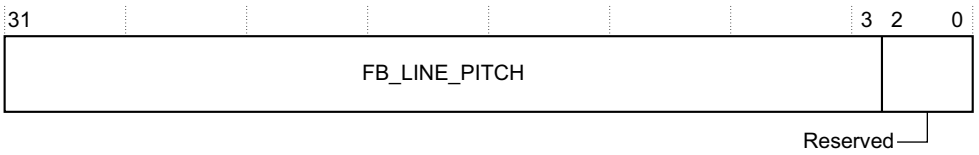


Figure B-9 Frame Buffer Line Count Pitch bit assignments

Table B-10 shows the bit assignments.

Table B-10 Frame Buffer Line Pitch Register bit assignments

Bits	Name	Function
[31:3]	FB_LINE_PITCH	Frame buffer line pitch
[2:0]	-	Reserved. Write as zero, read undefined.

Bus Options Register

The BUS_OPTIONS Register characteristics are:

Purpose Controls aspects of how the LCD controller accesses the bus. This value can be tuned to better match the characteristics of the memory controller and other units in the system.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-10 on page B-12 shows the bit assignments.

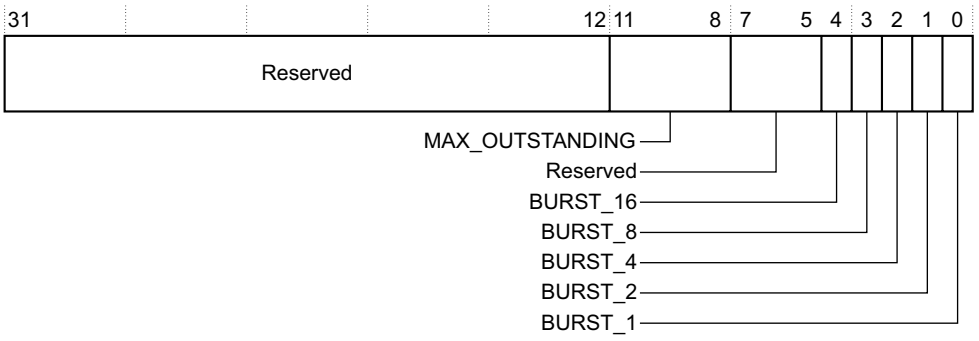


Figure B-10 Bus Options Register bit assignments

Table B-11 shows the bit assignments.

Table B-11 Bus Options Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined.
[11:8]	MAX_OUTSTANDING	Maximum number of outstanding requests the LCD controller is permitted to have on the bus at any time. **Caution** A value of zero disables all bus transfers
[7:5]	-	Reserved. Write as zero, read undefined.
[4]	BURST_16	Permit the use of 16-beat bursts.
[3]	BURST_8	Permit the use of 8-beat bursts.
[2]	BURST_4	Permit the use of 4-beat bursts.
[1]	BURST_2	Permit the use of 2-beat bursts.
[0]	BURST_1	Permit the use of 1-beat bursts.

Note

- If the scan line length does not end up at a multiple of the permitted burst lengths, the controller uses smaller bursts to read the remaining few pixels in each scan line. If no bursts are permitted, this mechanism also triggers, and has the same effect as permitting all bursts.
- Incorrectly configuring this register can degrade the performance of both the LCD controller and the rest of the system.

Vertical Synch Width Register

The V_SYNC Register characteristics are:

Purpose Holds the width of the vertical synch signal, counted in number of horizontal scan lines.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-11 shows the bit assignments.

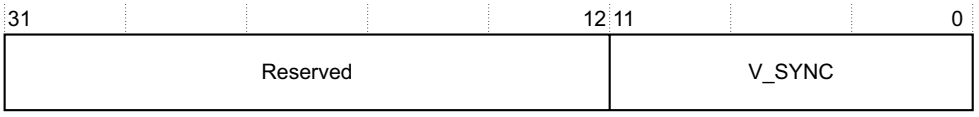


Figure B-11 Vertical Synch Width Register bit assignments

Table B-12 shows the bit assignments.

Table B-12 Vertical Synch Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined.
[11:0]	V_SYNC	Vertical synch width -1.

Vertical Back Porch Width Register

The V_BACK_PORCH Register characteristics are:

Purpose Holds the width of the interval between the vertical sync and the first visible line, counted in number of horizontal scan lines.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-12 shows the bit assignments.

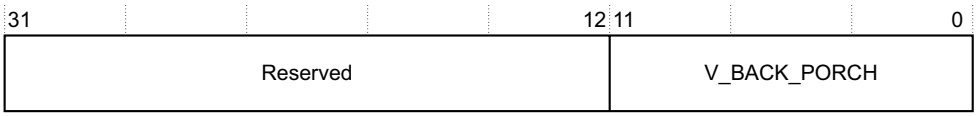


Figure B-12 Vertical Back Porch Width Register bit assignments

Table B-13 shows the bit assignments.

Table B-13 Vertical Back Porch Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	V_BACK_PORCH	Vertical back porch width -1

Vertical Data Width Register

The V_DATA Register characteristics are:

Purpose Holds the width of the vertical data area, that is, the number of visible lines, counted in the number of horizontal scan lines.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-13 shows the bit assignments.

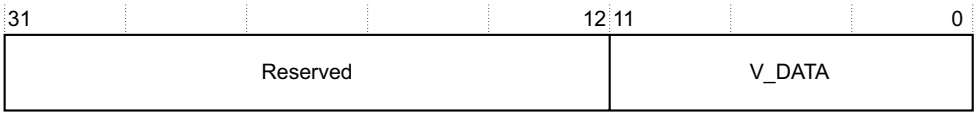


Figure B-13 Vertical Data Width Register bit assignments

Table B-14 shows the bit assignments.

Table B-14 Vertical Data Width Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	V_DATA	Vertical data width -1

Vertical Front Porch Width Register

The V_FRONT_PORCH Register characteristics are:

Purpose Holds the width of the interval between the last visible line and the next vertical synchronization, counted in number of horizontal scan lines.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-14 shows the bit assignments.

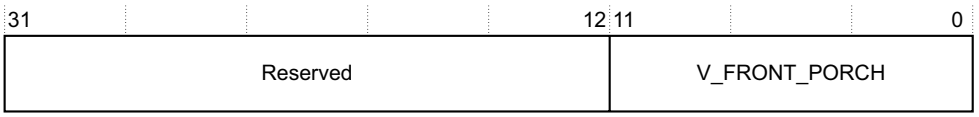


Figure B-14 Vertical Front Porch Width Register bit assignments

Table B-15 shows the bit assignments.

Table B-15 Vertical Front Porch Width Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	V_FRONT_PORCH	Vertical front porch width -1

Horizontal Synch Width Register

The H_SYNCH Register characteristics are:

Purpose Holds the width of the horizontal synch signal, counted in pixel clocks.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-15 shows the bit assignments.

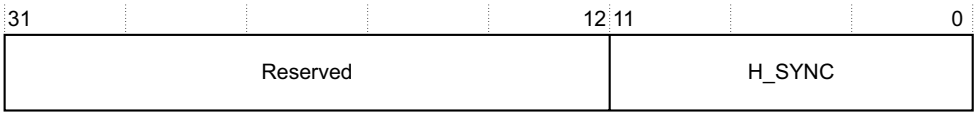


Figure B-15 Horizontal Synch Width Register bit assignments

Table B-16 shows the bit assignments.

Table B-16 Horizontal Synch Width Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	H_SYNC	Horizontal synch width -1

Horizontal Back Porch Width Register

The H_BACK_PORCH Register characteristics are:

Purpose Holds the width of the interval between the horizontal sync and the first visible column, counted in pixel clocks.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-16 shows the bit assignments.

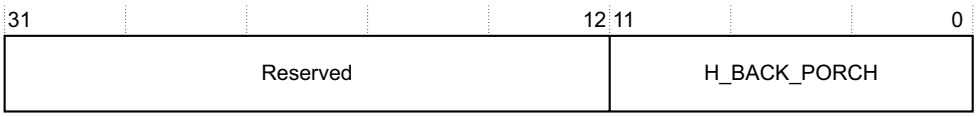


Figure B-16 Horizontal Back Porch Width Register bit assignments

Table B-17 shows the bit assignments.

Table B-17 Horizontal Back Porch Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	H_BACK_PORCH	Horizontal back porch width -1

Horizontal Data Width Register

The H_DATA Register characteristics are:

Purpose Holds the width of the horizontal data area, that is, the number of visible columns counted in pixel clocks.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-17 shows the bit assignments.

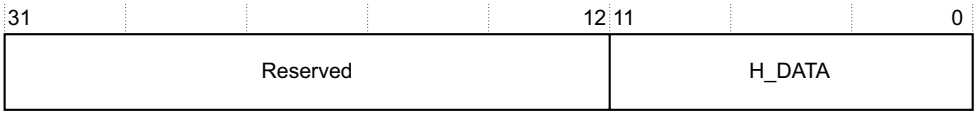


Figure B-17 Horizontal Data Width Register bit assignments

Table B-18 shows the bit assignments.

Table B-18 Horizontal Data Width Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	H_DATA	Horizontal data width -1

Horizontal Front Porch Width Register

The H_FRONT_PORCH Register characteristics are:

Purpose Holds the width of the interval between the last visible column and the next horizontal synchronization, counted in pixel clocks.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-18 shows the bit assignments.

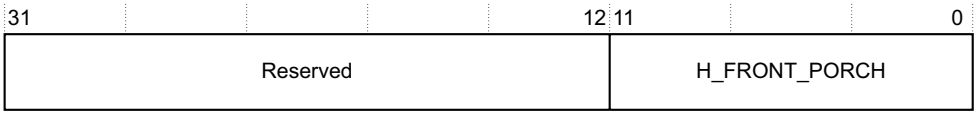


Figure B-18 Horizontal Front Porch Width Register bit assignments

Table B-19 shows the bit assignments.

Table B-19 Horizontal Front Porch Register bit assignments

Bits	Name	Function
[31:12]	-	Reserved. Write as zero, read undefined
[11:0]	H_FRONT_PORCH	Horizontal front porch width -1

Polarities Register

The POLARITIES Register characteristics are:

Purpose Controls the polarities of the synchronization signals and **PXLCLK** that is exported from the CoreTile Express A5x2 daughterboard.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-19 shows the bit assignments.

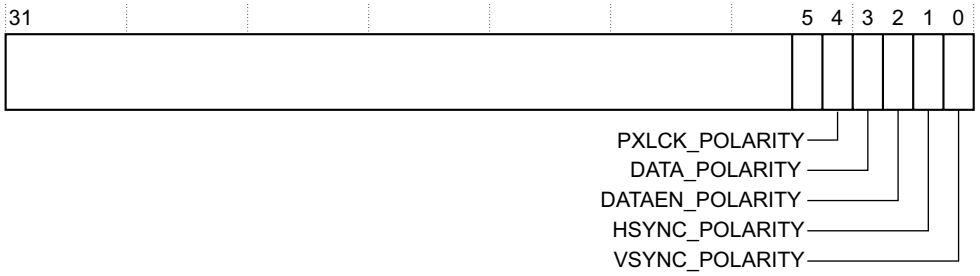


Figure B-19 Polarities Register bit assignments

Table B-20 shows the bit assignments.

Table B-20 Polarities Register bit assignments

Bits	Name	Function
[31:5]	-	Reserved. Write as zero, read undefined.
[4]	PXLCLK_POLARITY	Holds value of the PXLCLKPOL output. This is intended to be used for controlling the polarity of the pixel clock that is exported from the CoreTile Express A5x2 daughterboard. **Note** • PXLCLK_POLARITY=`b1`; — **PXLCLK**, HDLCD, and **MMB_IDCLK**, export, are the same polarity. • PXLCLK_POLARITY=`b0`; — **PXLCLK**, HDLCD, and **MMB_IDCLK**, export, are the opposite polarity.
[3]	DATA_POLARITY	Holds active level of DATA output.
[2]	DATAEN_POLARITY	Holds active level of DATAEN output.
[1]	HSYNC_POLARITY	Holds active level of HSYNC output.
[0]	VSYNC_POLARITY	Holds active level of VSYNC output.

Command Register

The COMMAND Register characteristics are:

Purpose Starts and stops the LCD controller.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-20 shows the bit assignments.

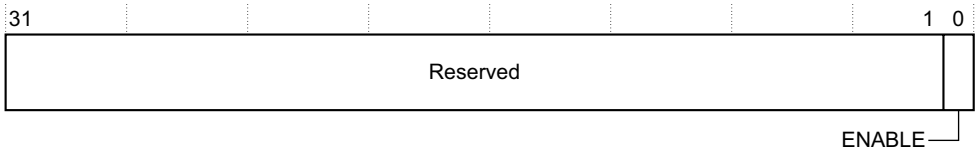


Figure B-20 Command Register bit assignments

Table B-21 shows the bit assignments.

Table B-21 Command Register bit assignments

Bits	Name	Function
[31:1]	-	Reserved. Write as zero, read undefined
[0]	ENABLE	Enable the LCD controller

Pixel Format Register

The PIXEL_FORMAT Register characteristics are:

Purpose BYTES_PER_PIXEL plus one bytes are extracted from the internal buffer. The extracted bytes are used to form a 32-bit value. The individual bytes are then optionally reordered if BIG_ENDIAN is set before the color components are extracted.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-21 shows the little endian byte layout.

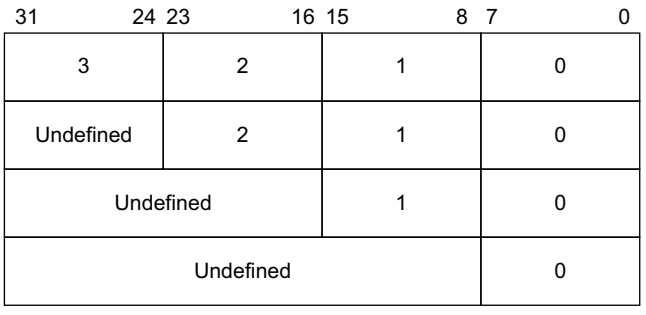


Figure B-21 Little endian byte layout

Figure B-22 on page B-19 shows the big endian byte layout.

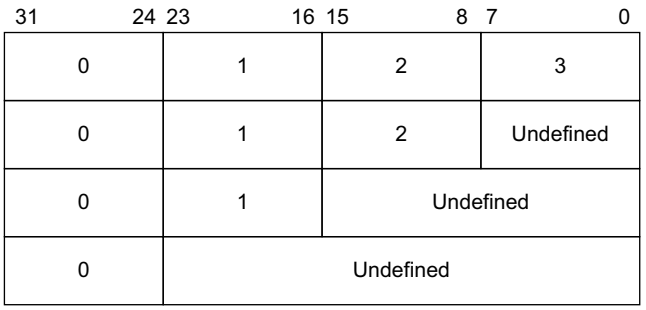


Figure B-22 Big endian byte layout

Figure B-23 shows the bit assignments for the big endian format.

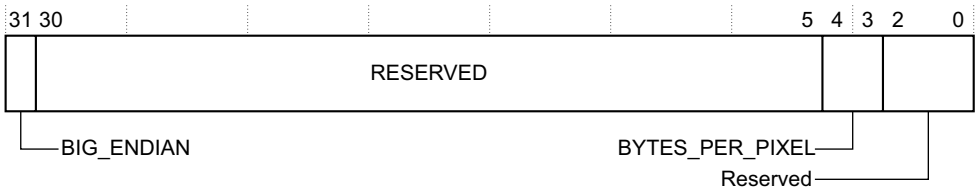


Figure B-23 Pixel Format Register bit assignments

Table B-22 shows the bit assignments for the big endian format.

Table B-22 Pixel Format Register bit assignments

Bits	Name	Function
[31]	BIG_ENDIAN	Use big endian byte order
[30:5]	-	Reserved. Write as zero, read undefined
[4:3]	BYTES_PER_PIXEL	Number of bytes to extract from the buffer for each pixel to display, minus one
[2:0]	-	Reserved. Write as zero, read undefined

Color Select Registers

The RED_SELECT, GREEN_SELECT and BLUE_SELECT Registers characteristics are:

Purpose The bytes extracted from the internal buffer are presented as a 32-bit value. These registers select how many bits at which position are used to extract and use as the red, green, and blue color components. If no bits are extracted or no data is available, the default color is used.

Usage constraints There are no usage constraints.

Configurations Available in all HDLCD controller configurations.

Attributes See Table B-1 on page B-3.

Figure B-24 on page B-20 shows the bit assignments.

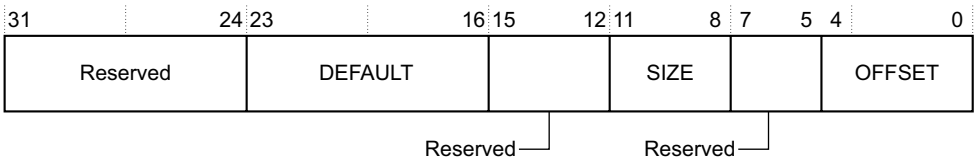


Figure B-24 Color Select Register bit assignments

Table B-23 shows the bit assignments.

Table B-23 Color Select Register bit assignments

Bits	Name	Function
[31:24]	-	Reserved. Write as zero, read undefined.
[23:16]	DEFAULT	Default color. This color is used any of the following occur: • SIZE is zero. • The buffer underruns. • While outside the visible frame area.
[15:12]	-	Reserved. Write as zero, read undefined.
[11:8]	SIZE	Number of bits to extract. If this value is zero, the default color is used. If this value is in the range 1-7, the extracted MSBs are repeated for the LSBs until eight bits are reached. If this value is larger than 8, the behavior is UNDEFINED.
[7:5]	-	Reserved. Write as zero, read undefined.
[4:0]	OFFSET	Index of the lowest bit to extract. If OFFSET + SIZE >= 8 + 8 x BYTES_PER_PIXEL, the behavior is UNDEFINED.

Appendix C
Electrical Specifications

This appendix contains the electrical specification for the daughterboard. It contains the following section:

- *AC characteristics*.

C.1 AC characteristics

Table C-1 shows the recommended AC operating characteristics for the Cortex-A5 MPCore test chip.

For more information on each interface that Table C-1 describes, see the appropriate technical reference manual in *Additional reading* on page ix.

Table C-1 AC characteristics

Interface	Parameter	Symbol	Minimum	Maximum	Description
Multiplexed slave AXI port	Clock cycle	t_{MPcyc}	25ns	-	Cmax=49.3pF Cmin=26.13pF
	Output valid time before clock rising edge	t_{MPov}	-	13ns	
	Output hold time after clock rising edge	t_{MPoh}	2.75ns	-	
	Input setup time to clock rising edge	t_{MPis}	-	12.5ns	
	Input hold time after clock rising edge	t_{MPih}	2.75ns	-	
Multiplexed master AXI port	Clock cycle	t_{SPcyc}	25ns	-	Cmax=47.8pF Cmin=23.88pF
	Output valid time before clock edge	t_{SPov}	-	7.5ns	
	Output hold time after clock edge	t_{SPoh}	2.75ns		
	Input setup time to clock edge	t_{SPis}	-	7ns	
	Input hold time after clock edge	t_{SPih}	2.75ns	-	
Trace	Clock cycle	$t_{TRACEcyc}$	10ns	-	Cmax=22.5pF Cmin=16.5pF
	Output valid time before clock rising edge	$t_{TRACEov}$	-	7ns	
	Output hold time after clock rising edge	$t_{TRACEoh}$	5ns	-	
JTAG	Clock cycle	$t_{JTAGcyc}$	4ns	-	Cmax=48.5pF Cmin=10.5pF
	Output valid time before clock rising edge	t_{JTAGov}	-	8ns	
	Output hold time after clock rising edge	t_{JTAGoh}	4ns	-	
	Input setup time to clock rising edge	t_{JTAGis}	-	12ns	
	Input hold time after clock rising edge	t_{JTAGih}	8ns	-	

Appendix D
Revisions

This appendix describes the technical changes between released issues of this book.

Table D-1 Issue A

Change	Location	Affects
First release	-	-

Table D-2 Differences between Issue A and Issue B

Change	Location	Affects
Updated AC characteristics.	Table C-1 on page C-2	All revisions
Included MMB from FPGA daughterboard as input to IOFPGA on Versatile Express motherboards.	*MultiMedia Bus (MMB)* on page 2-6	All revisions
Included MCC in description of signal **CB_READY**.	Table 2-1 on page 2-13	All revisions
Additional reading section of Preface refers to DSTREAM documents instead of RVI.	*Additional reading* on page ix	All revisions
Updated clock names: SMB output clock. MMB output clock. MMB output clock.	 Figure 2-8 on page 2-15 Figure 2-8 on page 2-15 Table B-20 on page B-17	All revisions
Inserted note underneath Figure 2-9 on page 2-16 to explain control of polarity of **MMB_IDCLK**.	*Overview of clocks* on page 2-15	All revisions

Table D-2 Differences between Issue A and Issue B (continued)

Change	Location	Affects
Updated figure to remove AXI RAM block.	Figure 2-2 on page 2-4	All revisions
Shortened Configuration chapter. Information is now in a new document: *Versatile Express Configuration Technical Reference Manual.* Added other information about custom motherboard.	*Configuration architecture* on page 2-8	All revisions
Added new documents to Additional Reading section of Preface: *Versatile Express Configuration Technical Reference Manual* *Programmer Module (V2M-CP1)* *LogicTile Express 13MG Technical Reference Manual*.	*Additional reading* on page ix	All revisions

Table D-3 Differences between Issue B and Issue C

Change	Location	Affects
Updated interrupt description.	*Interrupts* on page 2-19 Figure 2-10 on page 2-19 Table 2-4 on page 2-20	All revisions