ARMv8-A Foundation Platform

User Guide

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Release Information

<table>
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<tr>
<th>Issue</th>
<th>Date</th>
<th>Confidentiality</th>
<th>Change</th>
</tr>
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<tr>
<td>A</td>
<td>10 October 2012</td>
<td>Non-Confidential</td>
<td>First release.</td>
</tr>
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<td>B</td>
<td>01 May 2013</td>
<td>Non-Confidential</td>
<td>Minor updates. Directory structure changed.</td>
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<td>C</td>
<td>13 November 2013</td>
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<td>30 November 2015</td>
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Preface

This preface introduces the *ARMv8-A Foundation Platform User Guide*.

It contains the following:

About this book

This document describes the ARMv8-A Foundation Platform for the ARMv8-A architecture. It is an aid for hardware and software developers in developing ARMv8-A products.

Using this book

This book is organized into the following chapters:

**Chapter 1 Introduction**
This chapter describes the ARMv8-A Foundation Platform for the ARMv8-A architecture.

**Chapter 2 Getting Started**
This chapter describes validation and testing on the ARMv8-A Foundation Platform.

**Chapter 3 Programming Reference**
This chapter describes the ARMv8-A Foundation Platform.

Glossary

The ARM Glossary is a list of terms used in ARM documentation, together with definitions for those terms. The ARM Glossary does not contain terms that are industry standard unless the ARM meaning differs from the generally accepted meaning.

See the *ARM Glossary* for more information.

Typographic conventions

- **italic**
  Introduces special terminology, denotes cross-references, and citations.

- **bold**
  Highlights interface elements, such as menu names. Denotes signal names. Also used for terms in descriptive lists, where appropriate.

- **monospaced**
  Denotes text that you can enter at the keyboard, such as commands, file and program names, and source code.

- **monospaced italic**
  Denotes a permitted abbreviation for a command or option. You can enter the underlined text instead of the full command or option name.

- **monospaced bold**
  Denotes arguments to monospaced text where the argument is to be replaced by a specific value.

- **<and>**
  Denotes language keywords when used outside example code.

- **SMALL CAPITALS**
  Used in body text for a few terms that have specific technical meanings, that are defined in the *ARM glossary*. For example, IMPLEMENTATION DEFINED, IMPLEMENTATION SPECIFIC, UNKNOWN, and UNPREDICTABLE.

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• ARM Information Center.
• ARM Technical Support Knowledge Articles.
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• ARM Glossary.
Chapter 1
Introduction

This chapter describes the ARMv8-A Foundation Platform for the ARMv8-A architecture.

It contains the following sections:

• 1.1 Platform introduction on page 1-9.
• 1.2 ARMv8 64-bit architecture overview on page 1-10.
• 1.3 Software requirements on page 1-11.
• 1.4 Platform overview on page 1-12.
1.1 Platform introduction

The ARMv8-A Foundation Platform is an enabling platform for the ARMv8-A architecture.

It is a simple platform model capable of running bare-metal semi-hosted applications and booting a full operating system, with processor cluster, RAM, and some basic I/O devices such as Universal Asynchronous Receiver/Transmitters (UARTs), block storage, and network support. It also contains a simple web interface to indicate the status of the platform. It is supplied as a platform with configuration of the simulation from the command line and control using peripherals in the platform.

The processors in this platform are not based on any existing processor design, but conform to the ARMv8-A architectural specifications. This means that you can use the platform for confirming software functionality, but you must not rely on the accuracy of cycle counts, low-level component interactions, or other hardware-specific behavior.

Related concepts
3.6 Web interface on page 3-30.
1.2 ARMv8 64-bit architecture overview

The ARMv8 architecture is both an extension and a successor to the ARMv7-A architecture. The first release of the ARMv8 architecture covers the A-profile only.

The ARMv8-A architecture extends the existing 32-bit architecture by introducing two execution states:

- A 32-bit AArch32 state.
- A 64-bit AArch64 state.

A number of changes have been made to the AArch32 functionality, but it remains compatible with the ARMv7-A architecture. Code conforming to AArch32 can run on ARMv7-A devices. The A32 (ARM®) and T32 (Thumb®) instruction sets have new instructions relative to the ARMv7-A Instruction Set Architecture (ISA).

The AArch64 state introduces a new fixed-length 32-bit instruction set (A64) while maintaining support for the same architectural capabilities as ARMv7-A, such as TrustZone® and Virtualization. Some of the new enhancements in A64 are applicable to A32, so software written for AArch32 is not be compatible with ARMv7-A.

AArch64 has four Exception levels, 0-3, that replace the eight processor modes in ARMv7-A.

The least privileged, EL0, is equivalent to user-mode.

EL1 is equivalent to kernel-mode.

EL2 is used for hypervisors.

The highest privilege level, EL3, is used for the TrustZone security monitor.

Like ARMv7-A, AArch32 includes 13 general registers, R0-12, the Program Counter, R15, and two banked registers that contain the Stack Pointer, R13, and Link Register, R14. The User and System modes share these 16 registers and a Program Status Register (PSR). The new general purpose registers are all 64-bits wide to handle larger addresses, so 32-bit accesses use the lower halves of registers and either ignore or zero out the upper halves. The AArch32 registers map onto the lower halves of the AArch64 registers, and this permits AArch32 exceptions to be taken in AArch64 at a higher Exception level.

The two forms of instruction operate on either 32-bit or 64-bit values within the 64-bit general-purpose register file. Where a 32-bit instruction form is selected, the following holds true:

- The upper 32 bits of the source registers are ignored.
- The upper 32 bits of the destination registers are set to zero.
- Condition flags, where set by the instruction, are computed from the lower 32 bits.

For more information about the ARMv8 Instruction Set, see the ARMv8 Instruction Set Overview.

For more information about the ARMv8-A architecture, see the ARM® Architecture Reference Manual.
1.3 Software requirements

This section describes the host software that is required to run the ARMv8-A Foundation Platform.

Operating Systems

- Redhat Enterprise Linux version 5.x for 64-bit Intel architectures.
- Redhat Enterprise Linux version 6.x for 64-bit Intel architectures.
- Ubuntu 10.04 or later for 64-bit Intel architectures.

Note

Currently, there is no support for running the platform on other operating systems. However, the platform runs on any recent x86 64-bit Linux OS provided glibc v2.3.2, or higher, and libstdc++ 6.0.0, or higher, are present.

UART Output

For the Universal Asynchronous Receiver/Transmitter (UART) output to be visible, both xterm and telnet must be installed on the host, and be specified in your PATH.
1.4 Platform overview

This section describes the features and limitations of the Foundation Platform, and the types of network support that are provided.

This section contains the following subsections:

• 1.4.1 Features and network support of the Foundation Platform on page 1-12.

• 1.4.2 Limitations of the Foundation Platform on page 1-14.

1.4.1 Features and network support of the Foundation Platform

The ARMv8-A foundation platform has numerous features and two types of network support.

The platform provides:

• An ARMv8-A cluster model containing 1-4 cores that implements:
  — AArch64 at all Exception levels.
  — AArch32 support at EL0 and EL1.
  — Little and big endian at all Exception levels.
  — Generic timers.
  — Self-hosted debug.
  — GICv2, and optional GICv3 memory-mapped processor interfaces and distributor.

• 8GB of RAM.

——— Note ————

The platform simulates up to 8GB of RAM.

To simulate a system with 4GB of RAM, you require a host with at least 8GB of RAM.

To simulate a system with 8GB of RAM, you require a host with at least 12GB of RAM.

———

• Four PL011 UARTs connected to xterms.

• Platform peripherals including a Real-time clock, Watchdog timer, Real-time timer, and Power controller.

• Secure peripherals including a Trusted watchdog, Random number generator, Non-volatile counters, and Root-key storage.

• A network device model that is connected to host network resources.

• A block storage device that is implemented as a file on the host.

• A small system register block with LEDs and switches visible using a web server.

• Host filesystem access that is implemented as Plan 9 filesystem.

Caches are modeled as stateless and there are no write buffers. This gives the effect of perfect memory coherence on the data side. The instruction side has a variable size prefetch buffer so requires correct barriers to be used in target code to operate correctly.

The platform runs as fast as possible unless all the cores in the cluster are *Wait for Interrupt* (WFI) or *Wait for Exception* (WFE). In the case of WFE, the platform idles until an interrupt or external event occurs.

The Foundation Platform has been revised to support the ARM *Trusted Base System Architecture* (TBSA) and *Server Base System Architecture* (SBSA). Several peripheral devices have been added, with corresponding changes to the memory map. It has also been updated to align more closely with peripherals present in the Versatile™ Express baseboard and the ARM Fast Models.
Software that is written to target the previous versions of the platform work unmodified on the platform using the default `--no-gicv3` configuration option. Only software that uses the early blocks of RAM is likely to require some adjustments.

![Diagram of ARMv8-A Foundation Platform](image)

**Figure 1-1 Block diagram of ARMv8-A Foundation Platform**

--- **Note** ---

The behavior of the address decoding block depends on whether the `--secure-memory` command-line option is used.

---

The platform provides the following types of network support:

**NAT, IPv4 based**

NAT, IPv4-based networking provides limited IP connectivity by using user-level IP services. This requires no extra privileges to set up or use, but has inherent limitations. System-level services, or services conflicting with those services on the host, can be provided using port remapping.

**Bridged**

Bridged networking requires the setup of an ethernet bridge device to bridge between the ethernet port on the host and the network interface that the platform provides. This usually requires administrator privileges. See the documentation in the Linux bridge-utils package for more information.

The ARMv8-A Foundation Platform uses ARM Fast Model technology and forms part of a comprehensive suite of modeling solutions for ARM processors. These modeling solutions are available in the portfolio of models that are delivered through the ARM Fast Models product. For more information, see the *Fast Models User Guide.*
Related references

3.1 ARMv8-A Foundation Platform memory map on page 3-20.

1.4.2 Limitations of the Foundation Platform

There are some restrictions that apply to the ARMv8-A Foundation Platform.

- Write buffers are not modeled.
- Interrupts are not taken at every instruction boundary.
- Caches are modeled as stateless.
- There is no Component Architecture Debug Interface (CADI), CADI Server, Trace, or other plug-in support.
- There is no support for Thumb2EE.
- There is no support for the ARMv8 cryptography extensions.
- ARM does not offer direct customer support for the Foundation Platform. For technical support use the ARM Connected Community, http://community.arm.com.
Chapter 2
Getting Started

This chapter describes validation and testing on the ARMv8-A Foundation Platform.

It contains the following sections:

• 2.1 Verifying the installation on page 2-16.
• 2.2 The example program on page 2-17.
• 2.3 Using Linux on page 2-18.
2.1 Verifying the installation

The Foundation Platform is available only as a prebuilt platform binary.

The installation directory contents are:

- **examples**
  - Includes a C version and .axf file of the example program. It also includes the Makefile and the example source code for the device tree Foundation_Platform.dts.
  - **Foundation_Platform**
    - The ARMv8-A Foundation Platform executable file.
  - **libMAXCOREInitSimulationEngine.so**
    - Helper library required by the platform.
  - **libarmctmodel.so**
    - Code translation library.
  - **FoundationPlatform_Readme.txt**
    - Read me file. A short summary of this user guide.
  - **DUIO677_foundation_platform_ug.pdf**
    - This document.
  - **LES-PRE-20164v_1_0__Foundation_Platform.txt**
    - End-User License Agreement text.

**Related tasks**

2.2.1 Running the example program on page 2-17.
2.2 The example program

You can use the example program that is supplied to confirm that the ARMv8-A Foundation Platform is working correctly.

This section contains the following subsections:

• 2.2.1 Running the example program on page 2-17.
• 2.2.2 Troubleshooting the example program on page 2-17.

2.2.1 Running the example program

This section describes how to run the example program.

Run the platform with the following command line:

Procedure
1. ./Foundation_Platform --image hello.axf
2. Add --quiet to suppress everything except for the output from the example program.

You receive a similar output to the following:

    terminal_0: Listening for serial connection on port 5000
    terminal_1: Listening for serial connection on port 5001
    terminal_2: Listening for serial connection on port 5002
    terminal_3: Listening for serial connection on port 5003
    Simulation is started
    Hello, 64-bit world!
    Simulation is terminating. Reason: Simulation stopped

The example demonstrates that the platform initializes correctly as it loads and executes the example program. It also demonstrates that the semihosting calls to print output and stop the platform work properly.

2.2.2 Troubleshooting the example program

You can encounter common error messages when running the example program.

• If you attempt to run the example program on a 32-bit Linux host, it gives an error similar to the following:

    ./Foundation_Platform: /lib64/ld-linux-x86-64.so.2: bad ELF interpreter: No such file or directory

• If libstdc++ is not installed on your system, you get the following error on startup:

    ./Foundation_Platform: error while loading shared libraries: libstdc++.so.6: cannot open shared object file

• If your system glibc is too old, or your libstdc++ is too old, you get the following messages:

    ./Foundation_Platform: /usr/lib64/libstdc++.so.6: version `GLIBCXX_3.4' not found (required by Foundation_Platform)
    ./Foundation_Platform: /lib64/libc.so.6: version `GLIBC_2.3.2' not found (required by Foundation_Platform)
    ./Foundation_Platform: /lib64/libc.so.6: version `GLIBC_2.2.5' not found (required by Foundation_Platform)

libstdc++ and glibc are normally part of your core OS installation.
2.3 Using Linux

You can also use Linux with the ARMv8-A Foundation Platform.

For information on configuring and building the arm64 port of Linux to run on the ARMv8-A Foundation Platform, see the Linaro website at http://www.linaro.org/engineering/armv8.
This chapter describes the ARMv8-A Foundation Platform.

It contains the following sections:

- 3.1 ARMv8-A Foundation Platform memory map on page 3-20.
- 3.2 Clock and timer on page 3-23.
- 3.3 Interrupt maps on page 3-24.
- 3.4 System register block on page 3-26.
- 3.5 Command-line overview on page 3-28.
- 3.6 Web interface on page 3-30.
- 3.7 UARTs on page 3-31.
- 3.8 Multicore configuration on page 3-32.
- 3.9 Semihosting overview on page 3-33.
3.1 ARMv8-A Foundation Platform memory map

This section describes the memory map for the ARMv8-A Foundation Platform.

The following list shows the Secure and Non-secure access permissions that are enabled by using the --(no-)secure-memory parameter.

<table>
<thead>
<tr>
<th>--no-secure-memory</th>
<th>--secure-memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>S</td>
<td>Secure access is permitted, Non-secure access aborts.</td>
</tr>
<tr>
<td>S/NS</td>
<td>Secure and Non-secure accesses are permitted. Secure and Non-secure accesses are permitted.</td>
</tr>
</tbody>
</table>

The following table shows the global memory map for the ARMv8-A Foundation Platform. This map is based on the Versatile Express RS2 memory map with extensions.

Note
- Unless you use the --quiet command-line option, areas of memory that is highlighted in the table return a warning to the console, together with RAZ/WI access behavior. This rule is applicable to Foundation Model v2 and Foundation Platform v9.
- Writes are ignored.
- Accesses from Foundation Model v1 cause an abort exception.

Note
- The Security column in the following table applies to the Foundation Model v2 and Foundation Platform v9 only.

<table>
<thead>
<tr>
<th>Start address</th>
<th>End address</th>
<th>Foundation v1 peripheral</th>
<th>Foundation v2 and v9 peripherals</th>
<th>Size</th>
<th>Security (v2 and v9 only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00_0000_0000</td>
<td>0x00_03FF_FFFF</td>
<td>RAM</td>
<td>Trusted Boot ROM, secureflash</td>
<td>64MB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_0400_0000</td>
<td>0x00_0403_FFFF</td>
<td>RAM</td>
<td>Trusted SRAM</td>
<td>256KB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_0600_0000</td>
<td>0x00_07FF_FFFF</td>
<td>RAM</td>
<td>Trusted DRAM</td>
<td>32MB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_0800_0000</td>
<td>0x00_0BFF_FFFF</td>
<td>-</td>
<td>NOR flash, flash0</td>
<td>64MB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_0C00_0000</td>
<td>0x00_0FFF_FFFF</td>
<td>-</td>
<td>NOR flash, flash1</td>
<td>64MB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1800_0000</td>
<td>0x00_19FF_FFFF</td>
<td>-</td>
<td>Warning + RAZ/WI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x00_1A00_0000</td>
<td>0x00_1AFF_FFFF</td>
<td>Ethernet, SMSC 91C111</td>
<td>Ethernet, SMSC 91C111</td>
<td>16MB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1C01_0000</td>
<td>0x00_1C01_FFFF</td>
<td>System Registers</td>
<td>System Registers</td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1C02_0000</td>
<td>0x00_1C02_FFFF</td>
<td>-</td>
<td>System Controller, SP810</td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1C04_0000</td>
<td>0x00_1C07_FFFF</td>
<td>-</td>
<td>Warning + RAZ/WI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x00_1C09_0000</td>
<td>0x00_1C09_FFFF</td>
<td>UART0, PL011</td>
<td>UART0, PL011</td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1C0A_0000</td>
<td>0x00_1C0A_FFFF</td>
<td>UART1, PL011</td>
<td>UART1, PL011</td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_1C0B_0000</td>
<td>0x00_1C0B_FFFF</td>
<td>UART2, PL011</td>
<td>UART2, PL011</td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>Start address</td>
<td>End address</td>
<td>Foundation v1 peripheral</td>
<td>Foundation v2 and v9 peripherals</td>
<td>Size</td>
<td>Security (v2 and v9 only)</td>
</tr>
<tr>
<td>--------------</td>
<td>-------------</td>
<td>--------------------------</td>
<td>---------------------------------</td>
<td>-------</td>
<td>--------------------------</td>
</tr>
<tr>
<td>0x00_1C0C_0000 0x00_1C0C_FFFF</td>
<td>UART3, PL011</td>
<td>UART3, PL011</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C0D_0000 0x00_1C0D_FFFF</td>
<td>-</td>
<td>Warning + RAZ/W</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_1C0F_0000 0x00_1C0F_FFFF</td>
<td>-</td>
<td>Watchdog, SP805</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C10_0000 0x00_1C10_FFFF</td>
<td>-</td>
<td>Base Platform Power Controller</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
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<tr>
<td>0x00_1C11_0000 0x00_1C11_FFFF</td>
<td>-</td>
<td>Dual-Timer 0, SP804</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C12_0000 0x00_1C12_FFFF</td>
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<td>Dual-Timer 1, SP804</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C13_0000 0x00_1C13_FFFF</td>
<td>Virtio block device</td>
<td>Virtio block device</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C14_0000 0x00_1C16_FFFF</td>
<td>-</td>
<td>Virtio Plan 9 for v9, Warning + RAZ/W for v2.1</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_1C17_0000 0x00_1C17_FFFF</td>
<td>-</td>
<td>Realtime Clock, PL031</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_1C1A_0000 0x00_1FFF_FFFF</td>
<td>-</td>
<td>Warning + RAZ/W</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_1F00_0000 0x00_1F00_0FFF</td>
<td>-</td>
<td>Non-trusted ROM</td>
<td>4KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2A43_0000 0x00_2A43_FFFF</td>
<td>-</td>
<td>REFCLK CNTControl, Generic Timer</td>
<td>64KB</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>0x00_2A44_0000 0x00_2A44_FFFF</td>
<td>-</td>
<td>EL2 Generic Watchdog Control</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2A45_0000 0x00_2A45_FFFF</td>
<td>-</td>
<td>EL2 Generic Watchdog Refresh</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2A49_0000 0x00_2A49_FFFF</td>
<td>-</td>
<td>Trusted Watchdog, SP805</td>
<td>64KB</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>0x00_2A4A_0000 0x00_2A4A_FFFF</td>
<td>-</td>
<td>Warning + RAZ/W</td>
<td>-</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_2A80_0000 0x00_2A80_FFFF</td>
<td>-</td>
<td>REFCLK CNTRead, Generic Timer</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2A81_0000 0x00_2A81_FFFF</td>
<td>-</td>
<td>AP_REFCLK CNTCTL, Generic Timer</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2A82_0000 0x00_2A82_FFFF</td>
<td>-</td>
<td>AP_REFCLK CNTBase0, Generic Timer</td>
<td>64KB</td>
<td>S</td>
<td></td>
</tr>
<tr>
<td>0x00_2A83_0000 0x00_2A83_FFFF</td>
<td>-</td>
<td>AP_REFCLK CNTBase1, Generic Timer</td>
<td>64KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_0000 0x00_2C00_1FFF</td>
<td>-</td>
<td>GIC Physical CPU interface, GICC</td>
<td>8KB</td>
<td>S/NS</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_1000 0x00_2C00_1FFF</td>
<td>GIC Distributor</td>
<td>GIC Distributorb</td>
<td>4KB</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_2000 0x00_2C00_2FFF</td>
<td>GIC Processor Interface</td>
<td>GIC Processor Interfaceb</td>
<td>4KB</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_4000 0x00_2C00_4FFF</td>
<td>GIC Processor Hyp Interface</td>
<td>GIC Processor Hyp Interfaceb</td>
<td>4KB</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_5000 0x00_2C00_5FFF</td>
<td>GIC Hyp Interface</td>
<td>GIC Hyp Interfaceb</td>
<td>4KB</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>0x00_2C00_6000 0x00_2C00_7FFF</td>
<td>GIC Virtual CPU Interface</td>
<td>GIC Virtual CPU Interfaceb</td>
<td>8KB</td>
<td>-</td>
<td></td>
</tr>
</tbody>
</table>

---

a The Foundation Model v2.1 only. Not the Foundation Platform.
b The Foundation Platform uses the GICv2 memory map by default, or if you use the --no-gicv3 configuration parameter.
### Table 3-2 ARMv8-A Foundation Platform memory map (continued)

<table>
<thead>
<tr>
<th>Start address</th>
<th>End address</th>
<th>Foundation v1 peripheral</th>
<th>Foundation v2 and v9 peripherals</th>
<th>Size</th>
<th>Security (v2 and v9 only)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x00_2C01_0000 0x00_2C01_0FFF</td>
<td>-</td>
<td>GIC Virtual Interface Control, GIC</td>
<td></td>
<td>4KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_2C02_F000 0x00_2C03_0FFF</td>
<td>-</td>
<td>GIC Virtual CPU Interface, GICV</td>
<td></td>
<td>8KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_2C09_0000 0x00_2C09_FFFF</td>
<td>-</td>
<td>Warning + RAZ/W</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0x00_2E00_0000 0x00_2E00_FFFF</td>
<td>-</td>
<td>Non-trusted SRAM</td>
<td></td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_2F00_0000 0x00_2F00_FFFF</td>
<td>-</td>
<td>GICv3 Distributor GICD(^a)</td>
<td></td>
<td>64KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_2F02_0000 0x00_2F03_FFFF</td>
<td>-</td>
<td>GICv3 Distributor ITS</td>
<td></td>
<td>128KB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_2F10_0000 0x00_2F1F_FFFF</td>
<td>-</td>
<td>GICv3 Distributor GICR</td>
<td></td>
<td>1MB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x00_7FE6_0000 0x00_7FE6_0FFF</td>
<td>-</td>
<td>Trusted Random Number Generator</td>
<td></td>
<td>4KB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_7FE7_0000 0x00_7FE7_0FFF</td>
<td>-</td>
<td>Trusted Non-volatile counters</td>
<td></td>
<td>4KB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_7FE8_0000 0x00_7FE8_0FFF</td>
<td>-</td>
<td>Trusted Root-Key Storage</td>
<td></td>
<td>4KB</td>
<td>S</td>
</tr>
<tr>
<td>0x00_8000_0000 0x00_FFFF_FFFF</td>
<td>DRAM (0GB - 2GB)</td>
<td>DRAM (0GB - 2GB)</td>
<td></td>
<td>2GB</td>
<td>S/NS</td>
</tr>
<tr>
<td>0x08_8000_0000 0x09_FFFF_FFFF</td>
<td>DRAM (2GB - 8GB)</td>
<td>DRAM (2GB - 8GB)</td>
<td></td>
<td>6GB</td>
<td>S/NS</td>
</tr>
</tbody>
</table>

**Related references**

*3.5 Command-line overview on page 3-28.*
3.2 Clock and timer

This section describes the frequencies of the clock and timer.

Cluster clk_in frequency parameter
100MHz.

GenericTimer base_frequency parameter
100MHz.
### 3.3 Interrupt maps

You can find information on the SPIs and PPIs on the GIC that the platform assigns.

--- **Note** ---

*Shared Peripheral Interrupt* (SPI) and *Private Peripheral Interrupt* (PPI) numbers are mapped onto GIC interrupt IDs as the *ARM\textsuperscript{®} Generic Interrupt Controller Architecture Specification* describes.

The following table lists the SPI assignments.

<table>
<thead>
<tr>
<th>IRQ ID</th>
<th>SPI offset</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>32</td>
<td>0</td>
<td>Watchdog, SP805</td>
</tr>
<tr>
<td>34</td>
<td>2</td>
<td>Dual-Timer 0, SP804</td>
</tr>
<tr>
<td>35</td>
<td>3</td>
<td>Dual-Timer 1, SP804</td>
</tr>
<tr>
<td>36</td>
<td>4</td>
<td>Realtime Clock, PL031</td>
</tr>
<tr>
<td>37</td>
<td>5</td>
<td>UART0, PL011</td>
</tr>
<tr>
<td>38</td>
<td>6</td>
<td>UART1, PL011</td>
</tr>
<tr>
<td>39</td>
<td>7</td>
<td>UART2, PL011</td>
</tr>
<tr>
<td>40</td>
<td>8</td>
<td>UART3, PL011</td>
</tr>
<tr>
<td>41</td>
<td>9</td>
<td>MCI, PL180, MCIINTR0</td>
</tr>
<tr>
<td>47</td>
<td>15</td>
<td>Ethernet, SMSC 91C111</td>
</tr>
<tr>
<td>56</td>
<td>24</td>
<td>Trusted Watchdog, SP085</td>
</tr>
<tr>
<td>57</td>
<td>25</td>
<td>AP_REFCLK, Generic Timer, CNTPSIRQ</td>
</tr>
<tr>
<td>58</td>
<td>26</td>
<td>AP_REFCLK, Generic Timer, CNTPSIRQ1</td>
</tr>
<tr>
<td>59</td>
<td>27</td>
<td>EL2 Generic Watchdog WS0</td>
</tr>
<tr>
<td>60</td>
<td>28</td>
<td>EL2 Generic Watchdog WS1</td>
</tr>
<tr>
<td>74</td>
<td>42</td>
<td>Virtio block device</td>
</tr>
<tr>
<td>75</td>
<td>43</td>
<td>Virtio Plan 9</td>
</tr>
<tr>
<td>92</td>
<td>60</td>
<td>cpu0 PMUIRQ</td>
</tr>
<tr>
<td>93</td>
<td>61</td>
<td>cpu1 PMUIRQ</td>
</tr>
<tr>
<td>94</td>
<td>62</td>
<td>cpu2 PMUIRQ</td>
</tr>
<tr>
<td>95</td>
<td>63</td>
<td>cpu3 PMUIRQ</td>
</tr>
</tbody>
</table>

The following table shows the PPI assignments:

<table>
<thead>
<tr>
<th>PPI</th>
<th>Device</th>
</tr>
</thead>
<tbody>
<tr>
<td>9</td>
<td>Virtual maintenance interrupt</td>
</tr>
<tr>
<td>10</td>
<td>Hypervisor timer event</td>
</tr>
<tr>
<td>PPI</td>
<td>Device</td>
</tr>
<tr>
<td>-----</td>
<td>---------------------------------------</td>
</tr>
<tr>
<td>11</td>
<td>Virtual timer event</td>
</tr>
<tr>
<td>13</td>
<td>Secure physical timer event</td>
</tr>
<tr>
<td>14</td>
<td>Non-secure physical timer event</td>
</tr>
</tbody>
</table>
3.4 System register block

The system register block provides a minimal set of registers. This component only accepts word writes and aligned reads.

<table>
<thead>
<tr>
<th>Offset</th>
<th>Type</th>
<th>Bits</th>
<th>Register</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0000</td>
<td>R/O</td>
<td>[31:0]</td>
<td>System ID Register</td>
</tr>
<tr>
<td>0x0004</td>
<td>R/W</td>
<td>[7:0]</td>
<td>User Programmable Switches</td>
</tr>
<tr>
<td>0x0008</td>
<td>R/W</td>
<td>[7:0]</td>
<td>LEDs</td>
</tr>
<tr>
<td>0x00A0</td>
<td>R/W</td>
<td>[31:0]</td>
<td>System configuration data</td>
</tr>
<tr>
<td>0x00A4</td>
<td>R/W</td>
<td>[31:0]</td>
<td>System configuration control</td>
</tr>
<tr>
<td>0x00A8</td>
<td>R/W</td>
<td>[31:0]</td>
<td>System configuration status</td>
</tr>
</tbody>
</table>

The System ID Register is divided into fields:

- **ID[31:28] Revision.**
  - 0x0: Foundation Model v2.
  - 0x1: Foundation Model v2.1.
  - 0x2: Foundation Platform v9.

- **ID[27:16] HBI board number.**
  - 0x010: ARMv8-A Foundation Platform, default.
  - 0x020: ARM Base Platform FVP.

- **ID[15:12] Build variant.** The value depends on the following command-line options:
  - 0x0: Variant A is the Foundation Platform with the GICv2 legacy map, when the `--no-gicv3` command-line option is used. This is the default.
  - 0x1: Variant B is the Foundation Platform with the GICv3 64kB memory map, when the `--gicv3` command-line option is used.

- **ID[11:8] Platform type:**
  - 0x0: Board.
  - 0x1: Model, default.
  - 0x2: Emulator.
  - 0x3: Simulator.
  - 0x4: FPGA.
  - 0x5: Not used.
The System ID register is not implemented in the Foundation Model v1. All unimplemented registers in the Foundation Model v1 system register block return the value 0xDEADDEAD on reads. You can use this value to distinguish Foundation Model v1 from both Foundation Model v2 and Foundation Platform v9, and FVP VE Base Platform.

The user-programmable Switches store 8 bits of state that can be read or written by software on the platform. You can configure the startup value, val, using --switches=val.

You can view and set the switches at run time from the web interface.

The LEDs store 8 bits of state that software can read or write on the platform and can be viewed at runtime from the web interface.

The system configuration control register provides two functions:

- Writing the value 0xC0800000 stops the simulation and returns control to the command line.
- Writing the value 0xC0900000 asserts and then clears the reset pins on all components in the simulation. It resets the system without clearing the contents of the RAMs.

Note

Writes to the system configuration register can take several instructions to complete. Therefore, a write to this register must be followed by a DSB and infinite loop.

The system configuration data and status registers always return 0 on reads, and writes are ignored.

Related concepts

3.6 Web interface on page 3-30.
3.5 Command-line overview

Command-line arguments provide all platform configuration. Run the platform with --help to obtain a summary of the available commands.

The syntax to use on the command line is:

```
./Foundation_Platform [OPTIONS...]
```

Table 3-6 Command-line options

<table>
<thead>
<tr>
<th>Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>--bigendian</td>
<td>Start processors in big endian mode. The default is little endian.</td>
</tr>
<tr>
<td>--block-device=file</td>
<td>Image file to use as persistent block storage.</td>
</tr>
<tr>
<td>--cores=N</td>
<td>Specify the number of cores, where N ranges 1-4. The default is 1.</td>
</tr>
<tr>
<td>--(ns)data=file@address</td>
<td>Raw file to load at an address in Non-secure or Secure memory.</td>
</tr>
<tr>
<td>--(no-)gicv3</td>
<td>Enable GICv3 or legacy compatible GICv2 as interrupt controller The default is --no-gicv3, that is, GICv2 mode.</td>
</tr>
<tr>
<td>--help</td>
<td>Display the help message and quit.</td>
</tr>
<tr>
<td>--image=file</td>
<td>Executable and Linking Format (ELF) image to load.</td>
</tr>
<tr>
<td>--network=(none</td>
<td>nat</td>
</tr>
<tr>
<td>--network-bridge=dev</td>
<td>Bridged network device name. The default is ARM0.</td>
</tr>
<tr>
<td>--network-mac-address</td>
<td>MAC address to use for networking. The default is 00:02:f7:ef:f6:74.</td>
</tr>
<tr>
<td>--network-nat-ports=M</td>
<td>Optional comma-separated list of NAT port mappings in the form: host_port=model_port, for example, 8022-&gt;22.</td>
</tr>
<tr>
<td>--network-nat-subnet=S</td>
<td>Subnet used for NAT networking. The default is 172.20.51.0/24.</td>
</tr>
<tr>
<td>--p9_root_dir</td>
<td>Host folder to be shared with the guest.</td>
</tr>
<tr>
<td>--quiet</td>
<td>Suppress any non-simulated output on stdout or stderr.</td>
</tr>
<tr>
<td>--(no-)rate-limit</td>
<td>Restrict simulation speed so that simulation time more closely matches real time rather than running as fast as possible. The default is disabled.</td>
</tr>
<tr>
<td>--read-only</td>
<td>Mount block device image in read-only mode.</td>
</tr>
<tr>
<td>--(no-)secure-memory</td>
<td>Enable or disable separate Secure and Non-secure address spaces. The default is disabled.</td>
</tr>
<tr>
<td>--(no-)semihost</td>
<td>Enable or disable semihosting support. The default is enabled.</td>
</tr>
<tr>
<td>--semihost-cmd=cmd</td>
<td>A string that is used as the semihosting command line.</td>
</tr>
<tr>
<td>--switches=val</td>
<td>Initial setting of switches in the system register block (default: 0).</td>
</tr>
<tr>
<td>--uart-start-port=P</td>
<td>Attempt to listen on a free TCP port in the range P to P+100 for each UART. The default is 5000.</td>
</tr>
<tr>
<td>--use-real-time</td>
<td>Sets the generic timer registers to report a view of real time as it is seen on the host platform. The generic timer registers are irrespective of how slow or fast the simulation runs.</td>
</tr>
<tr>
<td>--version</td>
<td>Display the version and build numbers and quit.</td>
</tr>
<tr>
<td>--(no-)visualization</td>
<td>Starts a small web server to visualize platform state. The default is disabled.</td>
</tr>
</tbody>
</table>

You can specify more than one --image, --data, or --nsdata option. The images and data are loaded in the order that they appear on the command line. The simulation starts from the entry point of the last ELF specified.
Related concepts
3.8 Multicore configuration on page 3-32.
3.6 Web interface on page 3-30.
3.9.1 Semihosting on page 3-33.
3.6 Web interface

This section describes the syntax to use on the command line.

You can use one of the following options in the command line:

- `./Foundation_Platform --visualization`
- `./Foundation_Platform --no-visualization`

Running the platform with the `--visualization` option, and without the `--quiet` option, shows the additional output:

- `terminal_0: Listening for serial connection on port 5000`
- `terminal_1: Listening for serial connection on port 5001`
- `terminal_2: Listening for serial connection on port 5002`
- `terminal_3: Listening for serial connection on port 5003`
- `Visualization web server started on port 2001`

The `terminal_n` lines relate to the UARTs.

Go to the address `http://127.0.0.1:2001` with your web browser.

The browser displays a visualization window.

![Visualization window](image)

**Figure 3-1 Visualization window**

The visualization window provides a dynamic view of the state of various parts of the platform and the ability to change the state of platform switches.

**Related concepts**

*3.7 UARTs on page 3-31.*
3.7 UARTs

When the Foundation Platform starts, it initializes four UARTs. For each UART, it searches for a free TCP port to use for telnet access to the UART. It searches by sequentially scanning a range of 100 ports and using the first free port. The start port defaults to 5000 and you can change it using the `--uart-start-port` command-line parameter.

Connecting a terminal or program to the given port displays and receives output from the associated UART and permits input to the UART.

If no terminal or program is connected to the port when data is output from the UART, a terminal is started automatically.

---------- Note ----------
A terminal only starts automatically if the `DISPLAY` environment variable is set and not empty.

----------

UART output

For the UART output to be visible, both `xterm` and `telnet` must be installed on the host, and be specified in your PATH.
3.8 Multicore configuration

By default, the platform starts up with a single core that begins executing from the entry point in the last provided ELF image, or address 0 if no ELF images are provided.

You can configure the platform using `--cores=N` to have up to four processor cores. Each core starts executing the same set of images, starting at the same address. The `--visualization` command-line option which is used with the multicore option, results in a visualization window.

![Foundation Platform](image)

**Figure 3-2 Multicore option with number of cores = 4**
3.9  **Semihosting overview**

This section describes semihosting and semihosting configuration.

This section contains the following subsections:
- 3.9.1 *Semihosting* on page 3-33.
- 3.9.2 *Semihosting configuration* on page 3-33.

### 3.9.1 Semihosting

Semihosting enables code running on a platform model to directly access the I/O facilities on a host computer.

Examples of these facilities include console I/O and file I/O. For more information on semihosting, see the *ARM® Compiler Toolchain Developing Software for ARM® Processors*.

The simulator handles semihosting by either:
- Intercepting SVC 0x123456 or 0xAB in AArch32 depending on whether the processor is in the ARM or Thumb state.
- Intercepting HLT 0xF000 in AArch64.

### 3.9.2 Semihosting configuration

You can use different commands for the semihosting configuration.

The syntax to use on the command line to enable or disable semihosting is as follows:

```
./Foundation_Platform --(no-)semihost
```

The syntax to use on the command line to set the semihosting command-line string is as follows:

```
./Foundation_Platform --semihost-cmd=<command string>
```